EPROM Products

1993/1994 Data Book/Handbook

Advanced
Micro
Devices

AMD's Marketing Communications Department specifies environmentally sound agricultural inks and recycled papers, making this book highly recyclable.

EPROM Products

Data Book/Handbook

1993/1994

ADVANCED MICRO DEVICES

Advanced Micro Devices continues to be at the forefront of non-volatile memory technology. Our technology leadership is evidenced by the world's fastest and highest density EPROMs.

Our CMOS EPROM product portfolio is the broadest available. Today we offer EPROM densities ranging from 64K to 4 Megabit in both ceramic windowed and plastic one-time-programmable packages. Our superior EPROM process technology yields access times as fast as 35 ns enabling you to maximize system performance based on today's high speed microprocessors. Furthermore, we have expanded our product service by providing ExpressROM™ memories. These preprogrammed and fully tested devices provide users with a cost-effective alternative to EPROMs without the long lead-time associated with ROMs.

We are now proud to announce a family of true Low Voltage EPROMs to complement our product offering. Our low voltage product family consists of 1 Megabit and 2 Megabit devices with speeds of 120 ns and 150 ns respectively. The voltage range has been extended to make them suitable for systems that have regulated power supplies (3.0 V to 3.6 V) and those that are battery powered (2.7 V to 3.6 V). We have also expanded our package portfolio to include Thin Small Outline Packages (TSOP).

There has never been a better time to take advantage of AMD's family of non-volatile memories.

Walid Maghribi

Vice President and General Manager
Non-Volatile Memory Division

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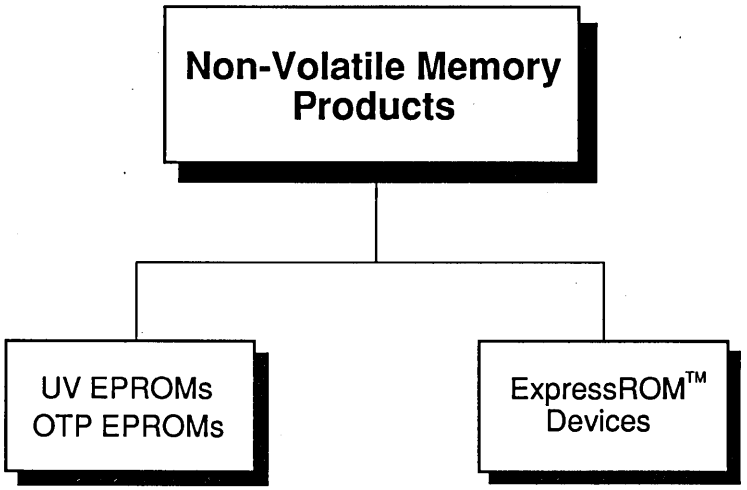
SECTION

1 PRODUCT SELECTOR GUIDES

Non-Volatile EPROM Memory Products



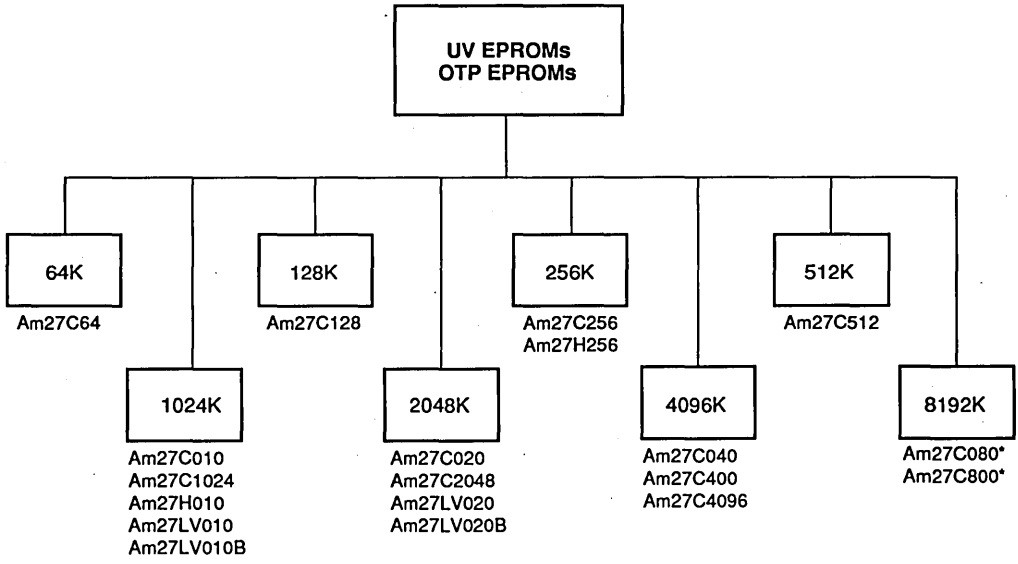
Introduction

The Non-Volatile Memory Division manufactures a broad range of high performance memory products. These products include traditional windowed EPROMs, plastic OTP EPROMs, and ExpressROM devices. They offer the system designer an extensive choice of economical alternatives for program storage.

AMD's EPROM offerings are manufactured using advanced CMOS process technology yielding access times as fast as 35 ns. Product densities range from 64K to 4 megabits. Designers challenged with extending useful battery life in portable applications will appreciate the 3 Volt EPROM product family. All EPROM products are offered in windowed ceramic and One-Time Programmable (OTP) plastic packages.

A new concept from AMD is the ExpressROM device. These are quick-turn ROMs produced from EPROM wafers. Lead times of these devices are typically half that of ROMs.

AMD is committed to leadership in high-performance CMOS non-volatile memories. These products offer industry-leading speeds and densities that will contribute to the competitive advantages of your design.



UV EPROMs & OTP EPROMs

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (DIP/PLCC) (TSOP)	Supply Voltage
Am27C64-55	8K x 8	55	C	D, L	28/32	5 V ± 5%
Am27C64-70	8K x 8	70	C	D, L	28/32	5 V ± 10%
Am27C64-90	8K x 8	90	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C64-120	8K x 8	120	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C64-150	8K x 8	150	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C64-200	8K x 8	200	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C64-255	8K x 8	250	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C128-55	16K x 8	55	C	D, L	28/32	5 V ± 5%
Am27C128-70	16K x 8	70	C	D, L	28/32	5 V ± 10%
Am27C128-90	16K x 8	90	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C128-120	16K x 8	120	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C128-150	16K x 8	150	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C128-200	16K x 8	200	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C128-255	16K x 8	250	C, I	D, L, P, J	28/32	5 V ± 5%
Am27H256-35	32K x 8	35	C	D, L	28/32	5 V ± 10%
Am27H256-35V05	32K x 8	35	C	D, L	28/32	5 V ± 5%
Am27H256-45	32K x 8	45	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27H256-55	32K x 8	55	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27H256-70	32K x 8	70	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C256-55	32K x 8	55	C	D, L	28/32	5 V ± 5%
Am27C256-70	32K x 8	70	C	D, L	28/32	5 V ± 10%
Am27C256-90	32K x 8	90	C, I, E, M	D, L, P, J, E	28/32	5 V ± 10%
Am27C256-120	32K x 8	120	C, I, E, M	D, L, P, J, E	28/32	5 V ± 10%
Am27C256-150	32K x 8	150	C, I, E, M	E	28/32	5 V ± 10%
Am27C256-200	32K x 8	200	C, I, E, M	D, L, P, J, E	28/32	5 V ± 10%
Am27C256-255	32K x 8	250	C, I	D, L, P, J	28/32	5 V ± 5%

Notes: see page 1-8

UV EPROMs & OTP EPROMs *(Cont.)*

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (DIP/PLCC) (TSOP)	Supply Voltage
Am27C512-75	64K x 8	70	C	D, L	28/32	5 V ± 5%
Am27C512-90	64K x 8	90	C, I, E, M	D, L	28/32	5 V ± 10%
Am27C512-120	64K x 8	120	C, I, E, M	D, L	28/32	5 V ± 10%
Am27C512-150	64K x 8	150	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512-200	64K x 8	200	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512-255	64K x 8	250	C, I, E, M	D, L, P, J	28/32	5 V ± 5%
Am27H010-45	128K x 8	45	C	D, L	32/32	5 V ± 10%
Am27H010-45V05	128K x 8	45	C	D, L	32/32	5 V ± 5%
Am27H010-55	128K x 8	55	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27H010-70	128K x 8	70	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27H010-90	128K x 8	90	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27H010-90V05	128K x 8	90	C, I, E, M	D, L, P, J	32/32	5 V ± 5%
Am27C010-105	128K x 8	100	C	D, L	32/32	5 V ± 5%
Am27C010-120	128K x 8	120	C, I	D, L, P, J, E	32/32	5 V ± 10%
Am27C010-150	128K x 8	150	C, I, E, M	D, L, P, J, E	32/32	5 V ± 10%
Am27C010-200	128K x 8	200	C, I, E, M	D, L, P, J, E	32/32	5 V ± 10%
Am27C010-255	128K x 8	250	C, I	D, L, P, J, E	32/32	5 V ± 5%
Am27LV010-120	128K x 8	120	C, I, E	D, L	32	3.3 V ± 10%
Am27LV010-150	128K x 8	150	C, I, E, M	D, L, J, E	32	3.3 V ± 10%
Am27LV010-200	128K x 8	200	C, I, E, M	D, L, J, E	32	3.3 V ± 10%
Am27LV010-250	128K x 8	250	C, I, E, M	D, L, J, E	32	3.3 V ± 10%
Am27LV010-300	128K x 8	300	C, I, E, M	D, L, J, E	32	3.3 V ± 10%
Am27LV010B-150	128K x 8	150	C, I, E	D, L, J, E	32	2.7 V – 3.6 V
Am27LV010B-200	128K x 8	200	C, I, E	D, L, J, E	32	2.7 V – 3.6 V
Am27LV010B-250	128K x 8	250	C, I, E, M	D, L, J, E	32	2.7 V – 3.6 V
Am27LV010B-300	128K x 8	300	C, I, E, M	D, L, J, E	32	2.7 V – 3.6 V
Am27C1024-85	64K x 16	85	C	D	40	5 V ± 5%
Am27C1024-90	64K x 16	90	C, I	D, L	40/44	5 V ± 10%
Am27C1024-120	64K x 16	120	C, I, E, M	D, L	40/44	5 V ± 10%
Am27C1024-150	64K x 16	150	C, I, E, M	D, L	40/44	5 V ± 10%
Am27C1024-200	64K x 16	200	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C1024-255	64K x 16	250	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C020-120	256K x 8	120	C, I	D, L	32/32	5 V ± 10%
Am27C020-150	256K x 8	150	C, I, E, M	D, L, P, J*	32/32	5 V ± 10%
Am27C020-200	256K x 8	200	C, I, E, M	D, L, P, J*	32/32	5 V ± 10%
Am27C020-250	256K x 8	250	M	D, L*	32/32	5 V ± 10%
Am27C020-255	256K x 8	250	C, I	D, L, P, J*	32/32	5 V ± 5%
Am27LV020-150	256K x 8	150	C, I, E	D, L, J	32	3.3 V ± 10%
Am27LV020-200	256K x 8	200	C, I, E, M	D, L, J	32	3.3 V ± 10%
Am27LV020-250	256K x 8	250	C, I, E, M	D, L, J	32	3.3 V ± 10%
Am27LV020-300	256K x 8	300	C, I, E, M	D, L, J	32	3.3 V ± 10%
Am27LV020B-200	128K x 8	200	C, I, E	D, L, J	32	2.7 V – 3.6 V
Am27LV020B-250	128K x 8	250	C, I, E, M	D, L, J	32	2.7 V – 3.6 V
Am27LV020B-300	128K x 8	300	C, I, E, M	D, L, J	32	2.7 V – 3.6 V
Am27C2048-105*	128K x 16	100	C	D, L	40/44	5 V ± 5%
Am27C2048-120	128K x 16	120	C, I	D, L	40/44	5 V ± 10%
Am27C2048-150	128K x 16	150	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C2048-200	128K x 16	200	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C2048-250	128K x 16	250	M	D, L	40/44	5 V ± 10%
Am27C2048-255	128K x 8	250	C, I	D, L, P, J	40/44	5 V ± 5%

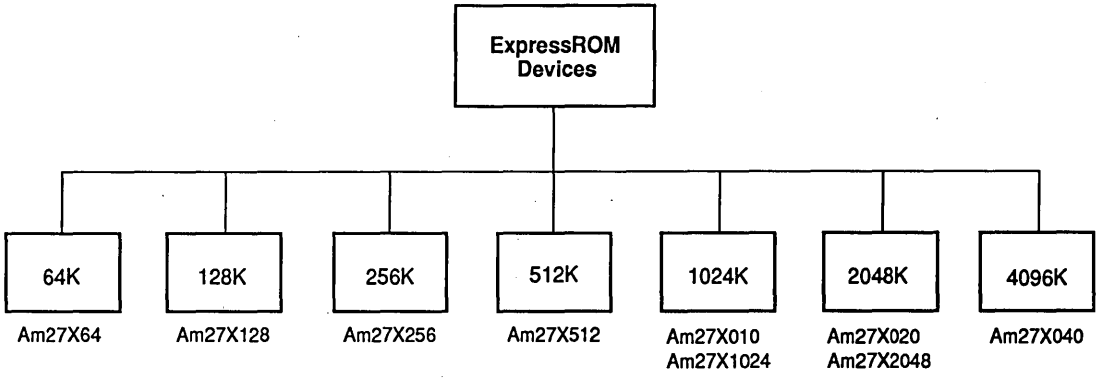
Notes: see page 1-8

UV EPROMs & OTP EPROMs *(Cont.)*

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (DIP/PLCC) (TSOP)	Supply Voltage
Am27C040-120	512K x 8	120	C, I	D, L	32/32	5 V ± 10%
Am27C040-125	512K x 8	120	C, I	D, L	32/32	5 V ± 5%
Am27C040-150	512K x 8	150	C, I, E, M	D, L	32/32	5 V ± 10%
Am27C040-200	512K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C040-250	512K x 8	250	M	D, L	32/32	5 V ± 10%
Am27C040-255	512K x 8	250	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C400-125	512K x 8/256K x 16	120	C, I	D	40	5 V ± 5%
Am27C400-120	512K x 8/256K x 16	120	C, I	D	40	5 V ± 10%
Am27C400-150	512K x 8/256K x 16	150	C, I	D	40	5 V ± 10%
Am27C400-200	512K x 8/256K x 16	200	C, I	D	40	5 V ± 10%
Am27C400-255	512K x 8/256K x 16	250	C, I	D	40	5 V ± 5%
Am27C4096-125	256K x 16	120	C, I	D, L	40/44	5 V ± 5%
Am27C4096-120	256K x 16	120	C, I	D, L	40/44	5 V ± 10%
Am27C4096-150	256K x 16	150	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C4096-200	256K x 16	200	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C4096-250	256K x 16	250	M	D, L	40/44	5 V ± 10%
Am27C4096-255	256K x 16	250	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C080-105*	1 Megabit x 8	100	C, I	D, L	32/32	5 V ± 5%
Am27C080-120*	1 Megabit x 8	120	C, I	D, L	32/32	5 V ± 10%
Am27C080-150*	1 Megabit x 8	150	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C080-200*	1 Megabit x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C080-250*	1 Megabit x 8	250	M	D, L	32/32	5 V ± 10%
Am27C080-255*	1 Megabit x 8	250	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C800-125*	1 Megabit x 8/512K x 16	120	C, I	D, L	42/44	5 V ± 5%
Am27C800-120*	1 Megabit x 8/512K x 16	120	C, I	D, L	42/44	5 V ± 10%
Am27C800-150*	1 Megabit x 8/512K x 16	150	C, I, E, M	D, L, P, J	42/44	5 V ± 10%
Am27C800-200*	1 Megabit x 8/512K x 16	200	C, I, E, M	D, L, P, J	42/44	5 V ± 10%
Am27C800-250*	1 Megabit x 8/512K x 16	250	M	D, L	42/44	5 V ± 10%
Am27C800-255*	1 Megabit x 8/512K x 16	250	C, I	D, L, P, J	42/44	5 V ± 5%

*Contact the local AMD sales office for the availability of this device.

Notes: see page 1-8



ExpressROM Devices

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (PDIP/PLCC)	Supply Voltage
Am27X64-90	8K x 8	90	C, I	P, J	28/32	5 V ± 10%
Am27X64-120	8K x 8	120	C, I	P, J	28/32	5 V ± 10%
Am27X64-150	8K x 8	150	C, I	P, J	28/32	5 V ± 10%
Am27X64-200	8K x 8	200	C, I	P, J	28/32	5 V ± 10%
Am27X64-255	8K x 8	250	C, I	P, J	28/32	5 V ± 5%
Am27X128-90	16K x 8	90	C, I	P, J	28/32	5 V ± 10%
Am27X128-120	16K x 8	120	C, I	P, J	28/32	5 V ± 10%
Am27X128-150	16K x 8	150	C, I	P, J	28/32	5 V ± 10%
Am27X128-200	16K x 8	200	C, I	P, J	28/32	5 V ± 10%
Am27X128-255	16K x 8	250	C, I	P, J	28/32	5 V ± 5%
Am27X256-90	32K x 8	90	C, I	P, J	28/32	5 V ± 10%
Am27X256-120	32K x 8	120	C, I	P, J	28/32	5 V ± 10%
Am27X256-150	32K x 8	150	C, I	P, J	28/32	5 V ± 10%
Am27X256-200	32K x 8	200	C, I	P, J	28/32	5 V ± 10%
Am27X256-255	32K x 8	250	C, I	P, J	28/32	5 V ± 5%
Am27XH256-45	32K x 8	45	C, I	P, J	28/32	5 V ± 10%
Am27XH256-55	32K x 8	55	C, I	P, J	28/32	5 V ± 10%
Am27XH256-70	32K x 8	70	C, I	P, J	28/32	5 V ± 10%
Am27X512-90	64K x 8	90	C, I	P, J	28/32	5 V ± 10%
Am27X512-120	64K x 8	120	C, I	P, J	28/32	5 V ± 10%
Am27X512-150	64K x 8	150	C, I	P, J	28/32	5 V ± 10%
Am27X512-200	64K x 8	200	C, I	P, J	28/32	5 V ± 10%
Am27X512-255	64K x 8	250	C, I	P, J	28/32	5 V ± 5%
Am27X010-105	128K x 8	105	C, I	P, J	32/32	5 V ± 5%
Am27X010-120	128K x 8	120	C, I	P, J	32/32	5 V ± 10%
Am27X010-150	128K x 8	150	C, I	P, J	32/32	5 V ± 10%
Am27X010-200	128K x 8	200	C, I	P, J	32/32	5 V ± 10%
Am27X010-255	128K x 8	250	C, I	P, J	32/32	5 V ± 5%
Am27XH010-55	128K x 8	55	C, I	P, J	32/32	5 V ± 10%
Am27XH010-70	128K x 8	70	C, I	P, J	32/32	5 V ± 10%
Am27XH010-90	128K x 8	90	C, I	P, J	32/32	5 V ± 10%

Notes: see page1-8

ExpressROM Devices *(Cont.)*

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (PDIP/PLCC)	Supply Voltage
Am27X1024-120	64K x 16	120	C, I	P, J	40/44	5 V ± 10%
Am27X1024-150	64K x 16	150	C, I	P, J	40/44	5 V ± 10%
Am27X1024-200	64K x 16	200	C, I	P, J	40/44	5 V ± 10%
Am27X1024-255	64K x 16	250	C, I	P, J	40/44	5 V ± 5%
Am27X020-125	256K x 8	125	C, I	P	32/32	5 V ± 10%
Am27X020-150	256K x 8	150	C, I	P	32/32	5 V ± 10%
Am27X020-200	256K x 8	200	C, I	P	32/32	5 V ± 10%
Am27X020-255	256K x 8	250	C, I	P	32/32	5 V ± 5%
Am27X2048-125	128K x 16	120	C, I	P, J	40/44	5 V ± 10%
Am27X2048-150	128K x 16	150	C, I	P, J	40/44	5 V ± 10%
Am27X2048-200	128K x 16	200	C, I	P, J	40/44	5 V ± 10%
Am27X2048-255	128K x 16	250	C, I	P, J	40/44	5 V ± 5%
Am27X040-150	512K x 8	150	C, I	P, J	32/32	5 V ± 10%
Am27X040-200	512K x 8	200	C, I	P, J	32/32	5 V ± 10%

Notes:

1. Temperature Range
   - C = Commercial (0°C to 70°C)
   - I = Industrial (–40°C to +85°C)
   - E = Extended Commercial (–55°C to +125°C)
   - M = Military (–55°C to +125°C) most products available in both APL and DESC versions.

2. Package Type
   - D = Ceramic DIP
   - L = Rectangular Ceramic Leadless Chip Carrier
   - P = Plastic DIP
   - J = Rectangular Plastic Leaded Chip Carrier
   - E = Thin Small Outline Package – standard pin-out
   - F = Thin Small Outline Package – reverse pin-out

SECTION

2 CMOS ERASABLE PROGRAMMABLE READ ONLY MEMORIES (EPROMs)

INSIDE AMD'S CMOS EPROM TECHNOLOGY

TECHNOLOGY DESCRIPTION

AMD's CMOS EPROM memories use standard CMOS periphery with an n-channel floating-gate memory array. The output buffers of the devices are designed to be compatible with both TTL and CMOS circuits. An n-channel pull-down and a p-channel pull-up provide full rail-to-rail switching of the outputs. The CMOS technology also allows very low standby power dissipation: 1.0 mA maximum TTL standby and 100 µA maximum CMOS standby currents.

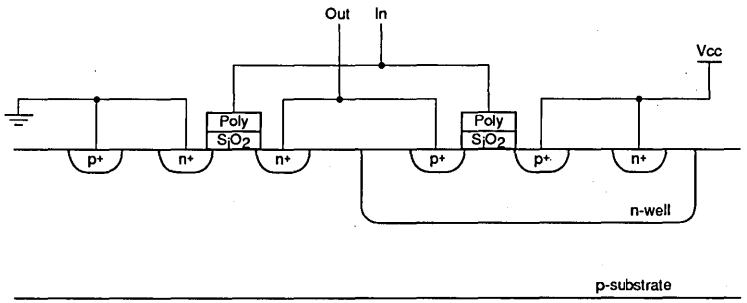
Figure 1 shows a cross-section of a basic inverter. The gates consist of polysilicon; the other connections are made with metal. The technology used for the periphery transistors is CMOS (Complementary MOS) technology which combines n and p channel devices on the same silicon. In this case, a non-epitaxial p-type substrate is used for the n-channel transistors and a deep diffused n-well is used for the p-channel transistors.

The fabrication of CMOS EPROM memories is a complex process where every step must be rigorously monitored and controlled. This complex processing is heavily dependent on the following underlying technologies:

Photolithography

The photo or masking technology is key to the manufacturing of integrated circuits (ICs). It allows the same circuits to be printed hundreds of times on the same wafer. It is also inherent to the patterning of the various structures on the wafer necessary to the fabrication of the ICs. Today, with the improved capability of wafer steppers, AMD's EPROM products are manufactured on geometries of one micron and below.

Figure 2-1 CMOS Inverter Cross-Section



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Ion Implantation

Ion implantation provides precision dopant control that is so critical for the manufacturing of AMD's EPROM products on sub-micron technology. Ion implantation equipment is a combination of mass spectrometry, linear acceleration, high resolution, current integration, ion beam scanning and high vacuum technologies. This process uses charged dopant atoms that are accelerated by an electric field and are implanted into the silicon wafer at a depth determined by the acceleration energy.

Diffusion

The furnace operations are required for silicon oxidation and driving in dopants. Oxidation cycles are used to grow the gate and isolation oxides inherent to the fabrication and operation of the MOS transistors. Drive cycles are used to diffuse the dopant material into the silicon to give the desired profile and depth.

Thin Films

Thin films deposited on the silicon include: polysilicon for gate electrodes and interconnection, interlayer dielectrics, metal layers for interconnection and passivation layers to seal the topside.

AMD EPROM Technology

The manufacturing technology for AMD's EPROM products involves a complex combination and blending of the previously mentioned processes. Each processing step requires a tremendous level of development, optimization and control. Before any new product is put into manufacturing, it must satisfy AMD's commitment to customer satisfaction, quality and reliability. To meet these standards, every new process and new product must pass many rigorous requirements. These requirements are outlined in greater depth in the reliability section.

The AMD EPROM products are being built on the CS19/19A family of technologies. These technologies are all based on a double-poly, single-metal n-well CMOS process. This process has been optimized for high density as well as high performance non-volatile memory devices. The basic features of this family of technologies are:

- n-well CMOS
- non-epitaxial, grounded substrate
- double-poly, single-metal

	CS19	CS19A
■ minimum feature (microns)	1.0	0.85
■ gate length (Leff) (microns)	0.9	0.7
■ gate oxide (Angstrom)	190	190
■ contacts (microns)	1.0	0.85
■ metal pitch (microns)	3.0	2.7

CS19

This is a 1.0 µm minimum feature conventional technology and is used to manufacture the low density and high speed EPROM products offered by AMD.

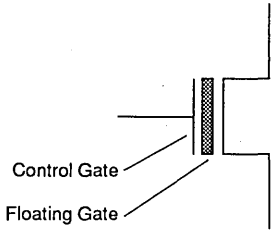
CS19A

This is an 0.85 µm minimum feature conventional technology and is used to manufacture the medium to high density EPROM products and the family of low voltage EPROM products offered by AMD.

UV-ERASABLE TECHNOLOGY

AMD's CMOS EPROM technology is based upon the concept of stored charge. The charge is stored on a floating gate, that is a gate that has no connection to the rest of the circuit. The storage transistor actually has two gates: one that floats, and the other that acts as a control gate. The control gate is used to establish the field across the floating gate (see Figure 2).

Figure 2-2 Floating-Gate MOS Transistor



17061A-2

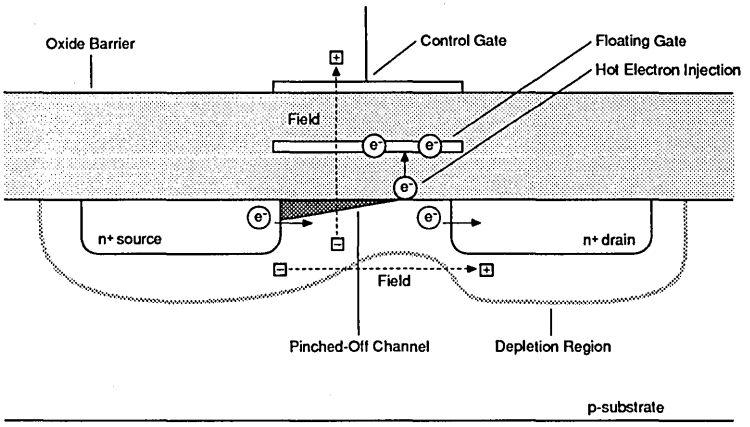
Hot electron injection is used for programming EPROM devices. With this scheme, a bias is set up between the source and drain of the transistor, and between the control gate and the substrate (see Figure 3). The channel is pinched off, and a strong current flows. Because of the high fields, the electrons are hot. The two fields (source-to-drain, and substrate-to-control-gate) combine to form a field in a diagonal direction, but because of the oxide barrier, electrons cannot flow in that direction. Occasionally, electrons acquire enough energy to cross the barrier in the shortest direction—from the channel to the floating gate. This is referred to as hot electron injection.

Once an electron is on the other side of the oxide, it is on the floating gate, with no conductive path to get off. It is therefore effectively trapped and remains there. During programming, large fields are set up so that a significant number of electrons are injected.

Erasing these devices requires exposure to ultraviolet light. The energy from the ultraviolet light causes the electrons to cross back over the oxide barrier thereby erasing the device. For this to happen, the device package must have a window that lets the ultraviolet light pass through.

The program and erase mechanisms of all of AMD's EPROM products are fundamentally identical irrespective of the type of technology (CS19 or CS19A) used.

Figure 2-3 Programming by Hot-Electron Injection



17061A-3

Erasing AMD EPROMs

In order to clear all locations of their programmed contents, it is necessary to expose the EPROM to an ultraviolet light source. A dosage of 15 W sec/cm^2 is required to completely erase an EPROM. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The EPROM should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the EPROM, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å, although erasure times will be much longer than with UV sources at 2537 Å. Nevertheless, the exposure to fluorescent light and sunlight will eventually erase the EPROM and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming AMD EPROMs

Upon delivery, or after each erasure, the EPROM has all bits in the "ONE," or HIGH state. "Zeros" are loaded into the EPROM through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. For programming, the data to be programmed is applied in parallel to the data input-output pins.

The Flashrite™ programming algorithm reduces programming time by using an initial 100 μs pulse followed by a byte verification operation to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for up to a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

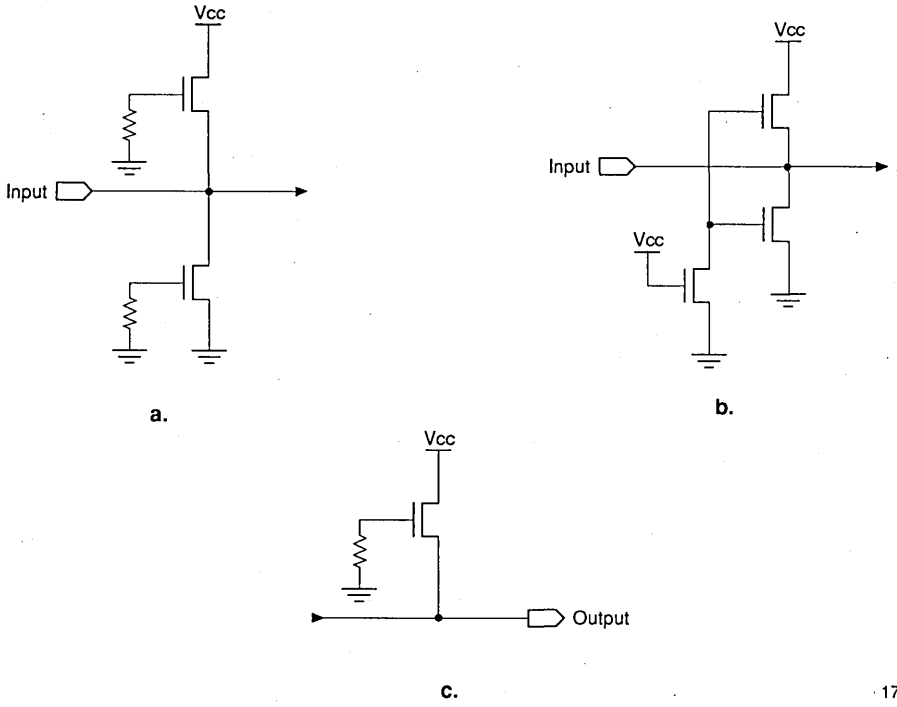
The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP} = 5.25$ V.

ESD

Every pin on the device is protected against electrostatic discharge (ESD), a formal name for static electricity shocks. Output pins rely on the large output drivers as protection. Inputs normally do not have large drivers, so a circuit must be added for input protection. In addition to ESD protection, these input protection circuits also help provide clamping against negative overshoot.

AMD CMOS EPROMs make use of ESD protection circuits as shown in Figures 4a through 4c. Most input pins use the circuit in Figure 4b. On output pins the ESD protection circuit has been modified as shown in Figure 4c.

Figure 2-4 ESD Protection: a. New Version; b. Standard; c. Output Pins



Latch-Up

All of AMD's CMOS devices are guaranteed to endure a current pulse of 100 mA into or out of the pin without inducing latch-up; most devices can actually withstand over 200 mA. Since AMD's CMOS EPROMs have true CMOS outputs, hot insertion is not recommended.

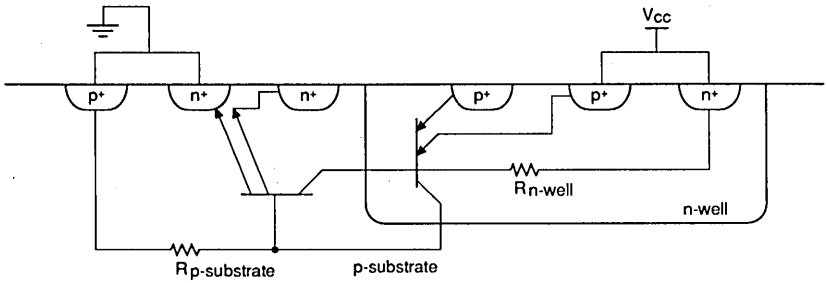
Latch-up may occur as a result of parasitic bipolar transistors between the n-channel and p-channel devices (see Figure 5a). These transistors form a parasitic Silicon Control Rectifier (SCR) (see Figure 5b), which turns ON when triggered, conducting large amounts of current. It is usually impossible to shut OFF without removing all the power from the device. The amount of current drain is so high that it can either overload

a power supply or, if the power supply can supply huge amounts of current, destroy the device.

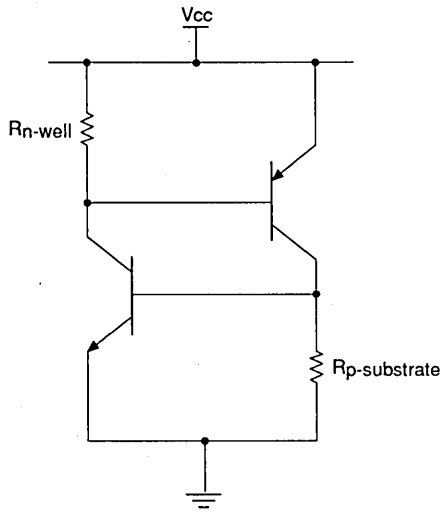
Latch-up is normally triggered by an input or output at a voltage significantly above V_{CC} or below ground, with enough current drawn to cause the SCR to turn on. This condition usually occurs when hot-socketing a part; i.e., plugging a part into a powered-up board or inserting a board into a powered-up system. When this happens, the inputs and V_{CC} power up uncontrolled, and there is a risk of latch-up.

For CMOS outputs, the SCR is an intrinsic part of the CMOS structure and cannot be eliminated. The SCR must be made as difficult as possible to turn ON by using guard rings and very carefully laying out input and output circuits.

Figure 2-5 Latch-Up Mechanism: a. Cross-Section; b. Equivalent Schematic



a.



b.

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System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4 µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The location of the capacitor should be as close to where the power supply is connected to the array.

SUMMARY

By concentrating on the needs of CMOS users, AMD has developed industry-leading CMOS technology that can provide cost-effective EPROMs of unsurpassed quality, reliability and performance. AMD provides value through:

- Robust technology and circuit design which
  - Does not generate high current transients, and
  - Has high immunity to system noise
- An extremely broad offering of products:
  - 64K through 4 Mbit commodity EPROM densities
  - High-speed family with access times as fast as 35 ns
  - Low-voltage products
    - Regulated (3.0 V – 3.6 V)
    - Unregulated (2.7 V – 3.6 V)

This note has detailed many of the aspects of the technology that make it superior to other alternatives. This, together with the information in the individual data sheets, qualification books, and a crew of applications engineers, should provide answers to your questions as you make use of AMD's CMOS EPROM technology.

FINAL

Am27C64

64 Kilobit (8,192 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 45 ns
- **Low power consumption**
  - — 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite™ programming**
  - — Typical programming time of 1 second
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions
- **Standard 28-pin DIP, PDIP, 32-pin LCC and PLCC packages**

GENERAL DESCRIPTION

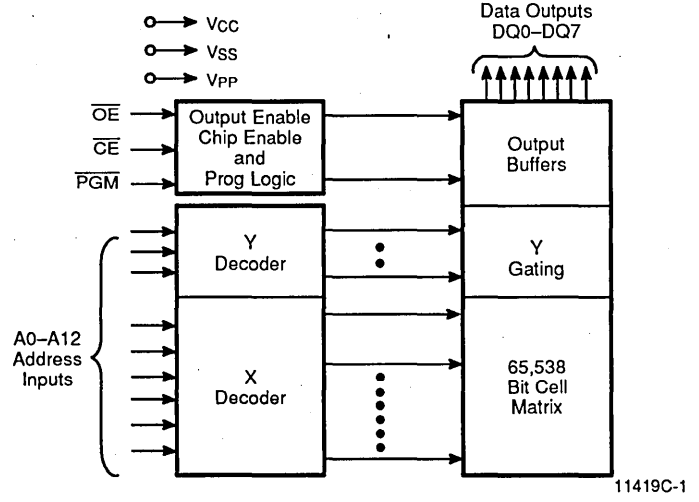
The Am27C64 is a 64-Kbit ultraviolet erasable programmable read-only memory. It is organized as 8K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP, and PLCC packages.

Typically, any byte can be accessed in less than 45 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C64 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C64 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in a typical programming time of 1 second.

BLOCK DIAGRAM



Publication#.11419 Rev. C Amendment/0
Issue Date: July 1993

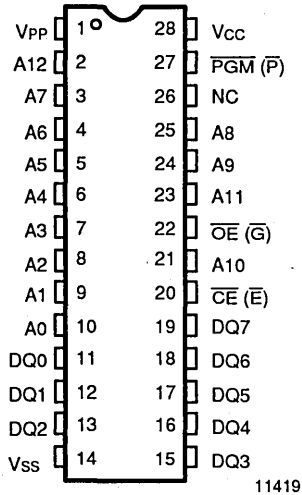
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C64							
Ordering Part No: Vcc ± 5%								-255
Vcc ± 10%	-45	-55	-70	-90	-120	-150	-200	-250
Max Access Time (ns)	45	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	45	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	30	35	40	40	50	65	75	100

CONNECTION DIAGRAMS

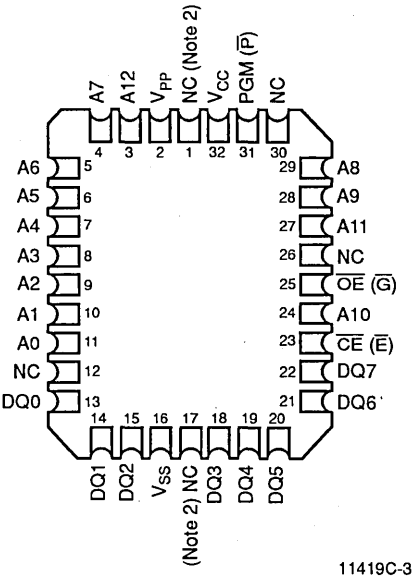
Top View

DIP



11419C-2

PLCC/LCC



11419C-3

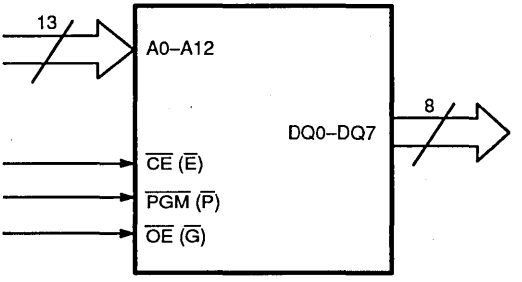
Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *Don't use (DU) for PLCC.*

PIN DESIGNATIONS

A0–A12	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable
DQ0–DQ7	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
Vcc	=	Vcc Supply Voltage
VPP	=	Program Supply Voltage
VSS	=	Ground

LOGIC SYMBOL

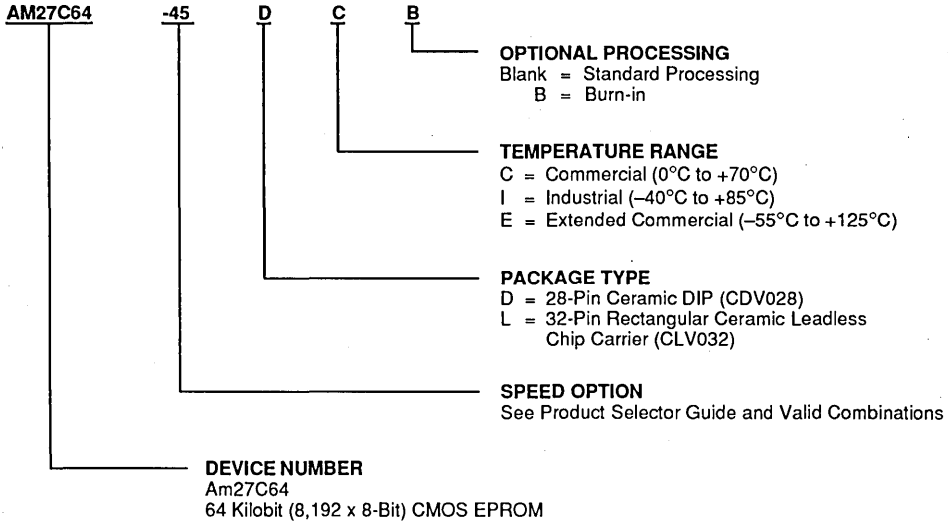


11419C-4

ORDERING INFORMATION

EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C64-45	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C64-55	
AM27C64-70	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C64-90	
AM27C64-120	
AM27C64-150	
AM27C64-200	
AM27C64-255	

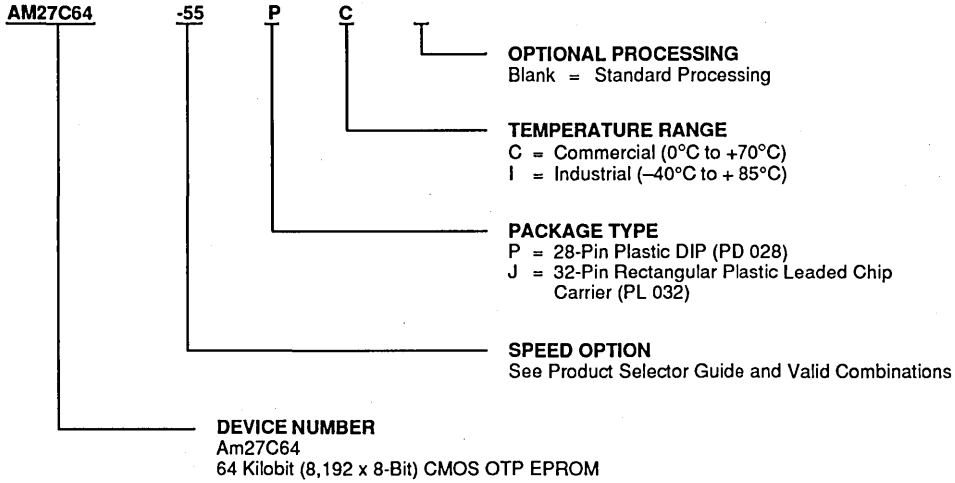
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C64-55	JC, PC, JI, PI,
AM27C64-70	
AM27C64-90	
AM27C64-120	
AM27C64-150	
AM27C64-200	
AM27C64-255	

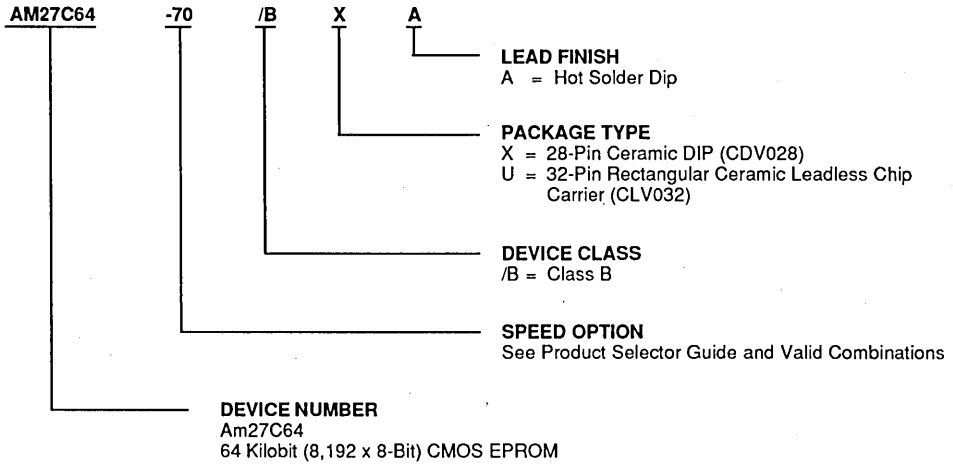
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combination.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C64-70	/BXA, /BUA
AM27C64-90	
AM27C64-120	
AM27C64-150	
AM27C64-200	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C64

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C64 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C64. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C64 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C64 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C64 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C64

Upon delivery or after each erasure the Am27C64 has all 65,536 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C64 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL} and $\overline{PGM}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C64. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C64 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C64 may be common. A TTL low-level program pulse applied to an Am27C64 $\overline{PGM}$ input with V_{PP} = 12.75 V ± 0.25 V and $\overline{CE}$ Low will program that Am27C64. A high-level $\overline{CE}$ input inhibits the other Am27C64 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C64.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C64. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code, and byte 1 ($A0 = V_{IH}$), the device code. For the Am27C64, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C64 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C64 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C64 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{CC}	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	V_{CC}	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	V_{CC}	Hi-Z
Standby (CMOS)		V_{CC} ± 0.3 V	X	X	X	X	V_{CC}	Hi-Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{CC}	15H

Notes:

1. *V_H = 12.0 V ± 0.5 V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A10–A12 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect To V_{SS}
- All pins except A9, V_{PP}, V_{CC} . −0.6 V to V_{CC} + 0.5 V
- A9 and V_{PP} ..... −0.6 V to +13.5 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C64-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27C64-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2, 3 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{CC1}	Vcc Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA			25	mA
I_{CC2}	Vcc TTL Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC3}	Vcc CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C64 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

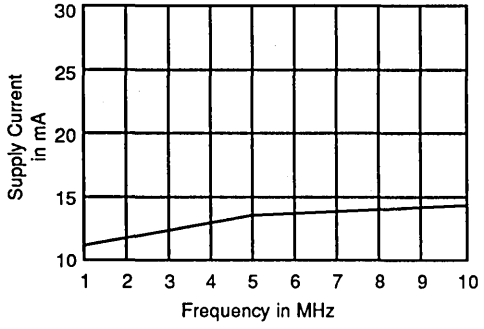


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

11419C-5

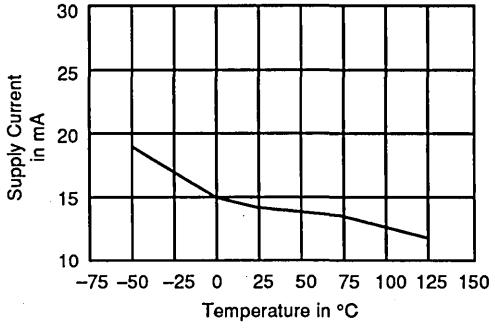


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

11419C-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CLV032		CDV028		PL 032		PD 028		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	7	10	8	10	6	10	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	11	14	8	12	8	10	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9,10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C64								Unit
JEDEC	Standard				-45	-55	-70	-90	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	–	
				Max	45	55	70	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	–	
				Max	45	55	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	–	–	–	
				Max	30	35	40	40	50	50	50	50	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	–	–	
				Max	25	25	25	25	30	30	30	30	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	0	0	
				Max	–	–	–	–	–	–	–	–	ns

Notes:

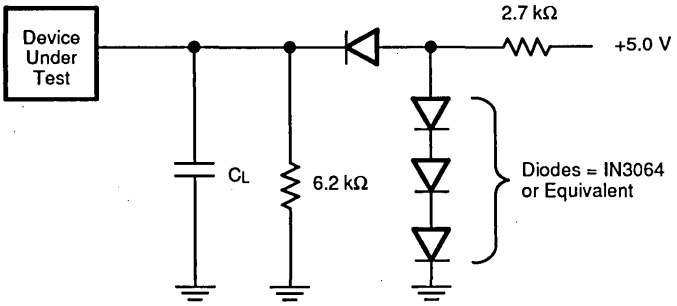
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C64 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *For the -45, -55 and -70:*

   Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

   For all other versions:

   Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V inputs and outputs

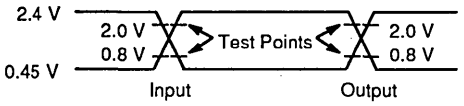
SWITCHING TEST CIRCUIT

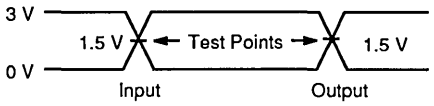


C_L = 100 pF including jig capacitance (30 pF for -45, -55, -70)

11419C-7

SWITCHING TEST WAVEFORM





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AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.

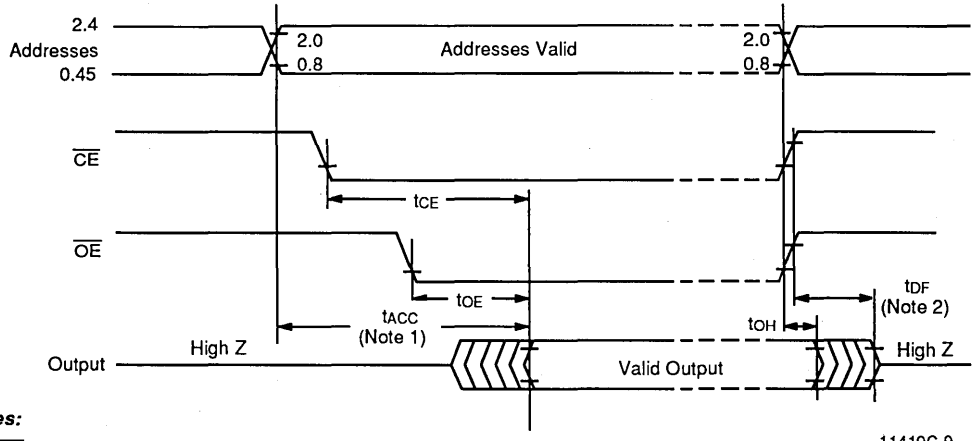
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -45, -55 and -70.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

11419C-9

FINAL

Am27C128

128 Kilobit (16,384 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 45 ns
- **Low power consumption**
  - — 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite™ programming**
  - — Typical programming time of 2 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions
- **Standard 28-pin DIP, PDIP, 32-pin LCC and PLCC packages**
- **DESC SMD No. 5962–87661**

GENERAL DESCRIPTION

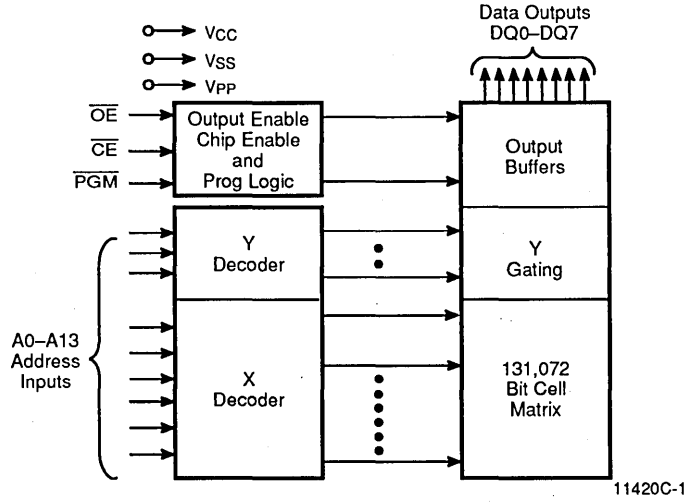
The Am27C128 is a 128K-bit ultraviolet erasable programmable read-only memory. It is organized as 16K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 45 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C128 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C128 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in a typical programming time of 2 seconds.

BLOCK DIAGRAM



11420C-1

Publication# 11420 Rev. C Amendment/0
Issue Date: July 1993

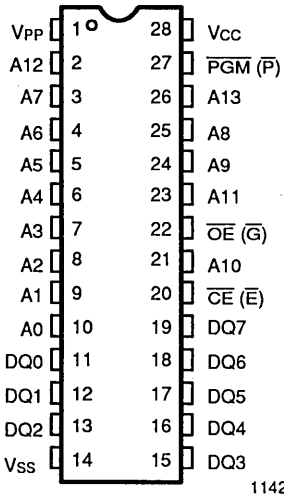
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C128							
Ordering Part No: Vcc ± 5%								-255
Vcc ± 10%	-45	-55	-70	-90	-120	-150	-200	-250
Max Access Time (ns)	45	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	45	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	30	35	40	40	50	65	75	100

CONNECTION DIAGRAMS

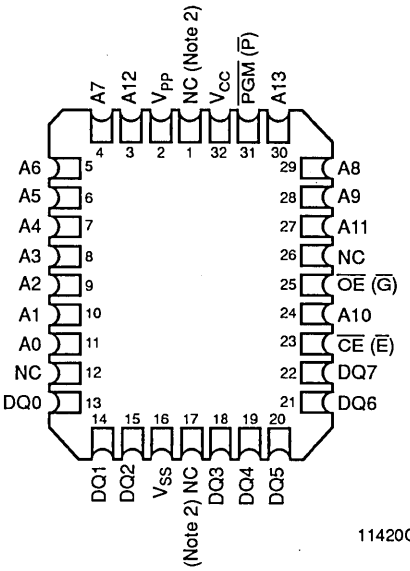
Top View

DIP



11420C-2

PLCC/LCC



11420C-3

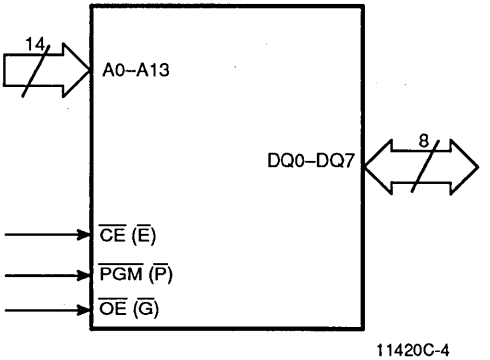
Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *Don't use (DU) for PLCC.*

PIN DESIGNATIONS

A0–A13	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable
DQ0–DQ7	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
Vcc	=	Vcc Supply Voltage
VPP	=	Program Supply Voltage
VSS	=	Ground

LOGIC SYMBOL

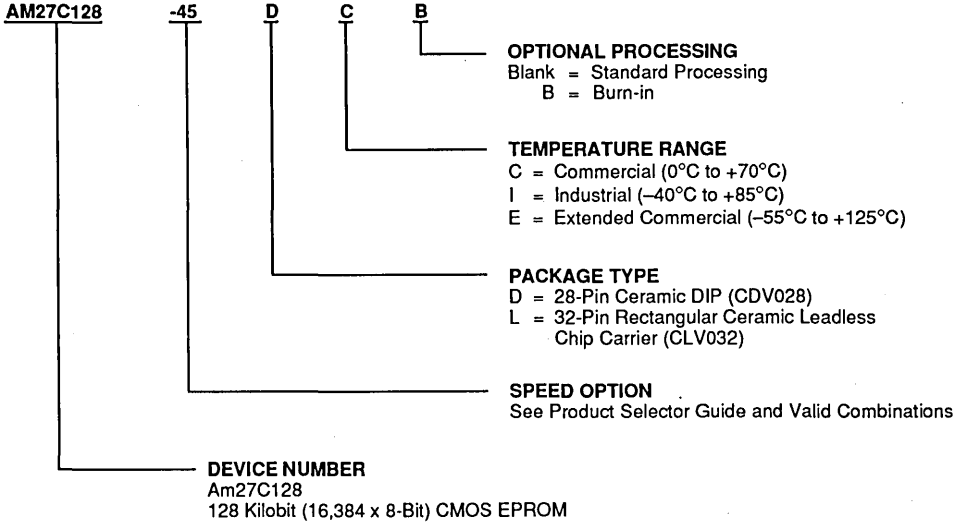


11420C-4

ORDERING INFORMATION

EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C128-45	DC, DCB, DI, DIB
AM27C128-55	LC, LCB, LI, LIB
AM27C128-70	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C128-90	
AM27C128-120	
AM27C128-150	
AM27C128-200	
AM27C128-255	

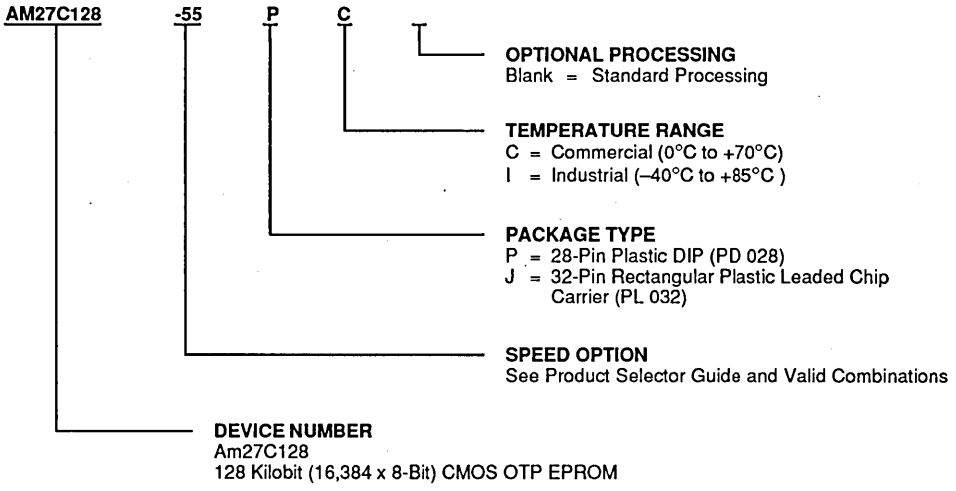
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C128-55	JC, PC, JI, PI
AM27C128-70	
AM27C128-90	
AM27C128-120	
AM27C128-150	
AM27C128-200	
AM27C128-255	

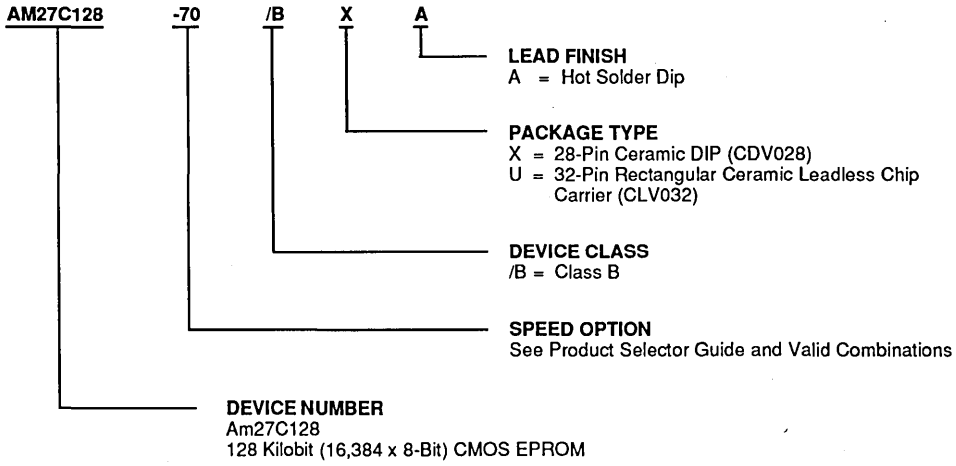
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C128-70	/BXA, /BUA
AM27C128-90	
AM27C128-120	
AM27C128-150	
AM27C128-200	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C128

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C128 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C128. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C128 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C128 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C128 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C128

Upon delivery or after each erasure the Am27C128 has all 131,072 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C128 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL}, and $\overline{PGM}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C128. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C128 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C128 may be common. A TTL low-level program pulse applied to an Am27C128 $\overline{PGM}$ input with V_{PP} = 12.75 V ± 0.25 V and $\overline{CE}$ Low will program that Am27C128. A high-level $\overline{CE}$ input inhibits the other Am27C128 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C128.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C128. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code, and byte 1 ($A0 = V_{IH}$), the device code. For the Am27C128, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C128 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C128 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C128 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{CC}	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	V_{CC}	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	V_{CC}	Hi-Z
Standby (CMOS)		V_{CC} ± 0.3 V	X	X	X	X	V_{CC}	Hi-Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{CC}	16H

Notes:

1. *V_H = 12.0 V ± 0.5 V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A10–A12 = V_{IL}, A13 = X*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Voltage with Respect To V_{SS}
- All pins except A9, V_{PP}, V_{CC} . −0.6 V to V_{CC} + 0.5 V
- A9 and V_{PP} ..... −0.6 V to +13.5 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C128-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27C128-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2, 3 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA			25	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C128 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

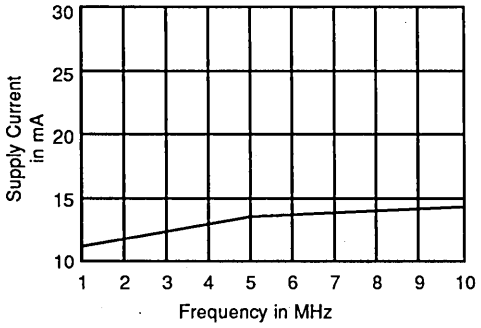


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

11420C-5

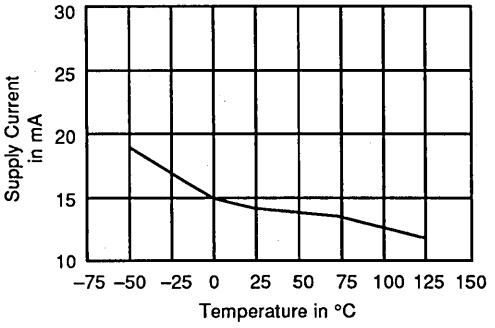


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

11420C-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CLV032		CDV028		PL 032		PD 028		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	7	10	8	10	6	10	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	11	14	8	12	8	10	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9,10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C128								Unit
JEDEC	Standard				-45	-55	-70	-90	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	–	
				Max	45	55	70	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	–	
				Max	45	55	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	–	–	–	
				Max	30	35	40	40	50	50	50	50	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	–	–	
				Max	25	25	25	25	30	30	30	30	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	0	0	
				Max	–	–	–	–	–	–	–	–	ns

Notes:

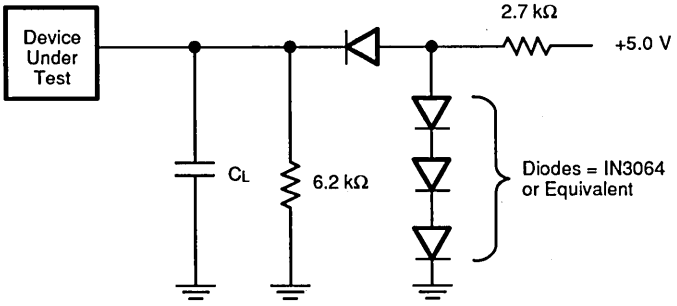
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C128 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *For the -45, -55 and -70:*

   Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

   For all other versions:

   Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V inputs and outputs

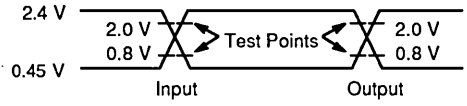
SWITCHING TEST CIRCUIT



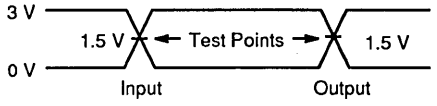
C_L = 100 pF including jig capacitance (30 pF for -45, -55, -70)

11420C-7

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



11420C-8

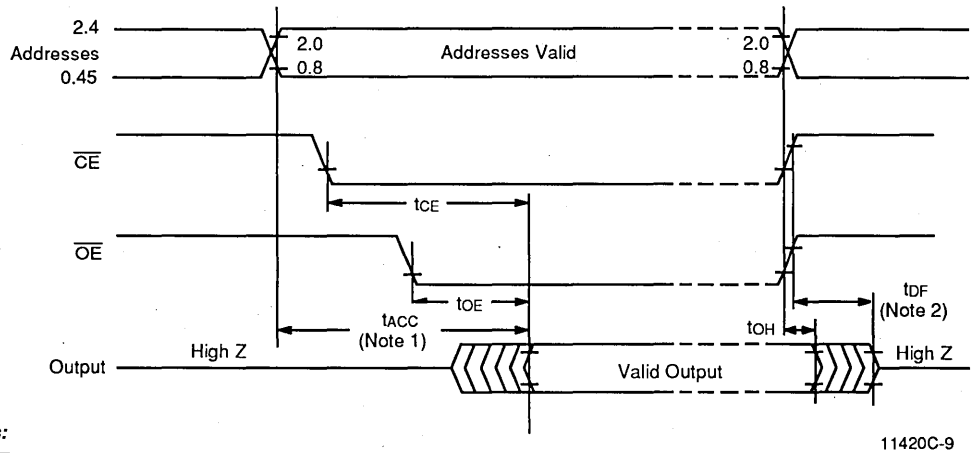
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -45, -55, and -70.

KEY TO SWITCHING TEST WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS



11420C-9

Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27C256

256 Kilobit (32,768 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 55 ns
- **Low power consumption**
  - — 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite™ programming**
  - — Typical programming time of 4 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions
- **Standard 28-pin DIP, PDIP, 32-pin TSOP, LCC and LCC packages**
- **DESC SMD No. 5962–86063**

GENERAL DESCRIPTION

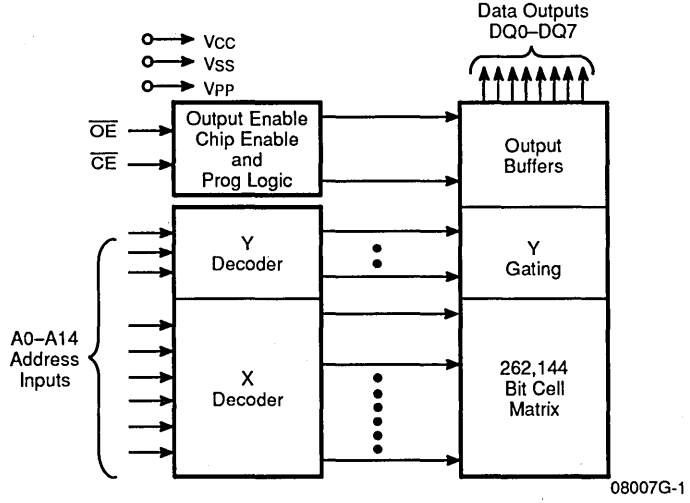
The Am27C256 is a 256K-bit ultraviolet erasable programmable read-only memory. It is organized as 32K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP, TSOP, and PLCC packages.

Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C256 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C256 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming time of 4 seconds.

BLOCK DIAGRAM



Publication# 08007 Rev. G Amendment/0
Issue Date: July 1993

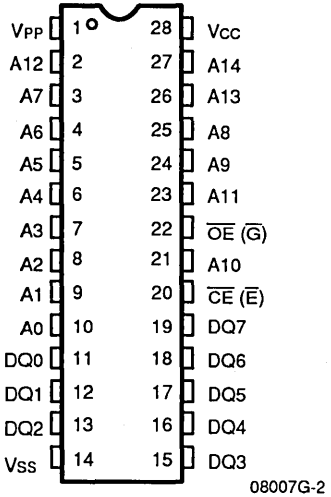
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C256						
Ordering Part No: $V_{CC} \pm 5\%$							-255
$V_{CC} \pm 10\%$	-55	-70	-90	-120	-150	-200	-250
Max Access Time (ns)	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	35	40	40	50	65	75	100

CONNECTION DIAGRAMS

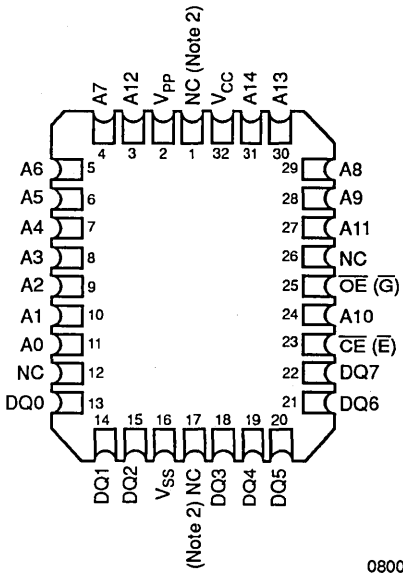
Top View

DIP



08007G-2

PLCC/LCC

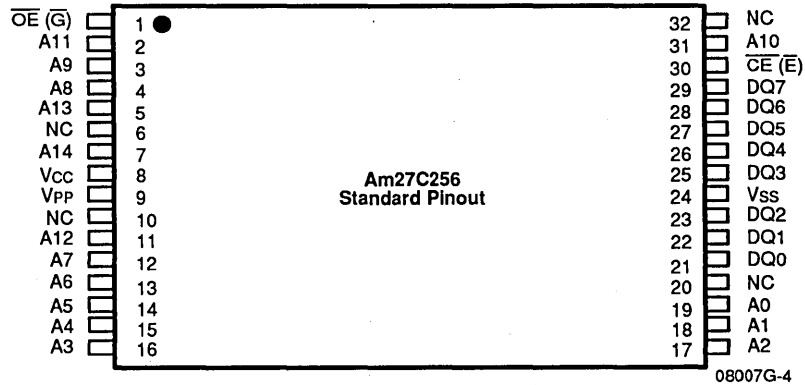


08007G-3

Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *Don't use (DU) for PLCC.*

TSOP*

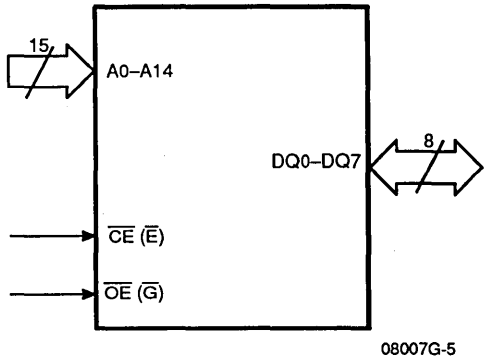


**Contact local AMD sales office for package availability*

PIN DESIGNATIONS

A0–A14	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable
DQ0–DQ7	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

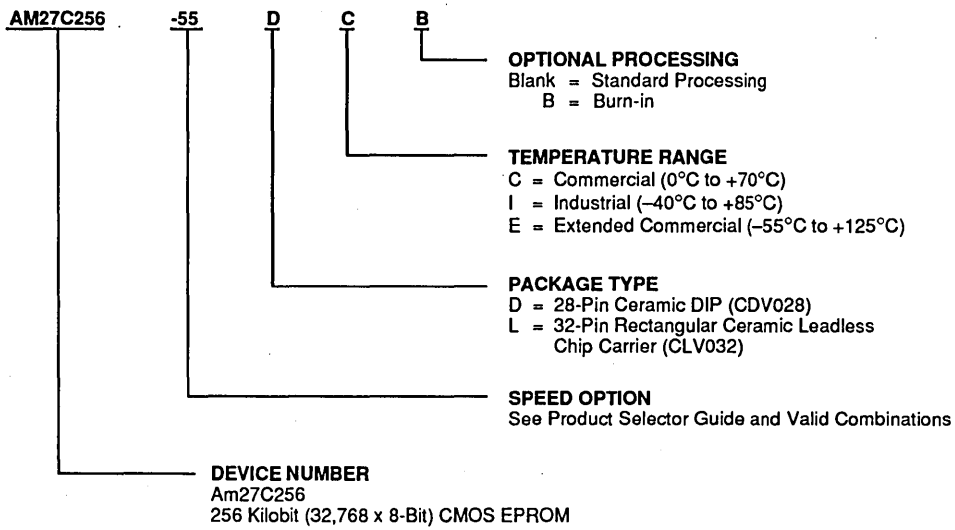
LOGIC SYMBOL



ORDERING INFORMATION

EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C256-55	DC, DCB, DI, DIB
AM27C256-70	LC, LCB, LI, LIB
AM27C256-90	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C256-120	
AM27C256-150	
AM27C256-200	
AM27C256-255	

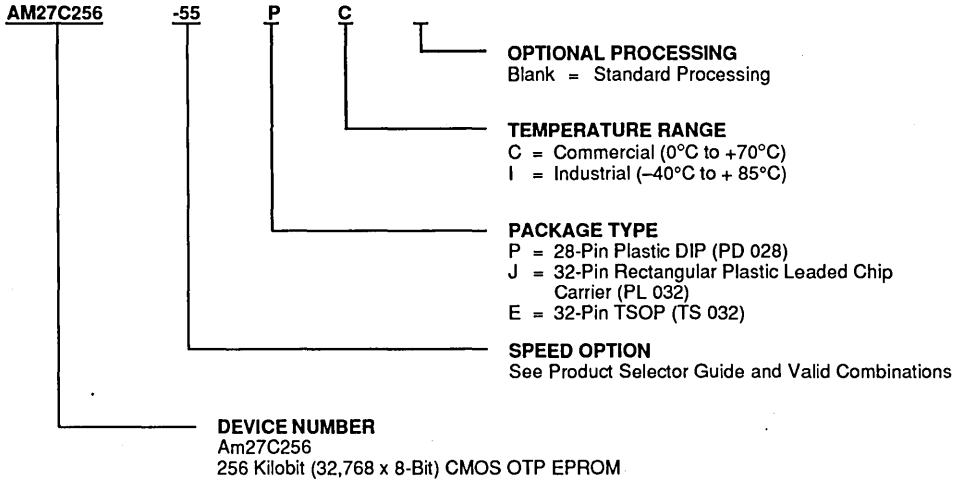
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C256-55	JC, PC, EC, JI, PI, EI
AM27C256-70	
AM27C256-90	
AM27C256-120	
AM27C256-150	
AM27C256-200	
AM27C256-255	

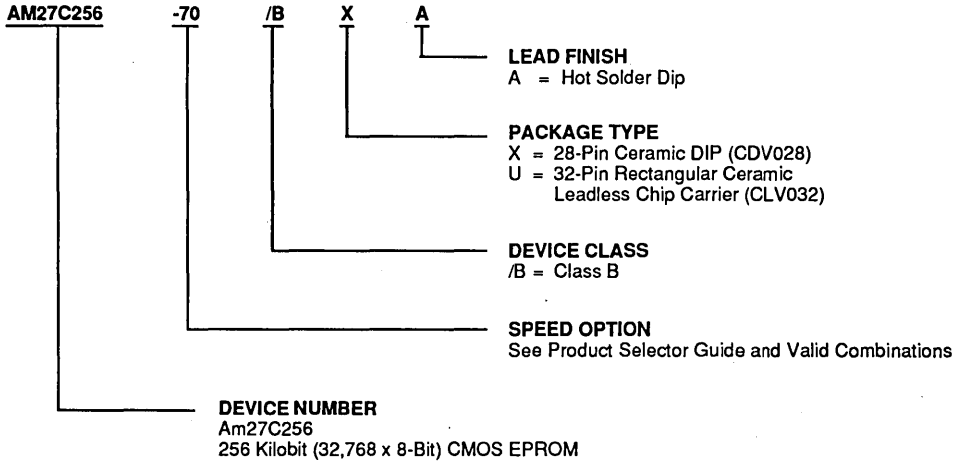
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C256-70	/BXA, /BUA
AM27C256-90	
AM27C256-120	
AM27C256-150	
AM27C256-200	
AM27C256-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C256

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C256 to an ultraviolet light source. A dosage of 15 W sec/cm^2 is required to completely erase an Am27C256. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C256 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C256 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C256 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C256

Upon delivery or after each erasure the Am27C256 has all 262,144 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C256 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{OE}$ is at V_{IH}, and $\overline{CE}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C256. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C256 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C256 may be common. A TTL low-level program pulse applied to an Am27C256 $\overline{CE}$ input with V_{PP} = 12.75 V ± 0.25 V, and $\overline{OE}$ High will program that Am27C256. A high-level $\overline{CE}$ input inhibits the other Am27C256 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH}, and V_{PP} between 12.5 V to 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C256.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address like A9 of the Am27C256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code, and byte 1 ($A0 = V_{IH}$), the device code. For the Am27C256, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C256 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C256 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable		X	V_{IH}	X	X	V_{CC}	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	V_{CC}	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	V_{CC}	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	10H

Notes:

1. *V_H = 12.0 V ± 0.5 V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1 – A8 = A10 – A14 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect To V_{SS}
- All pins except A9, V_{PP}, V_{CC} (Note 1) ..... −0.6 V to V_{CC} + 0.5 V
- A9 and V_{PP} (Note 2) ..... −0.6 V to +13.5 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:
1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C256-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27C256-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			−0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA			25	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

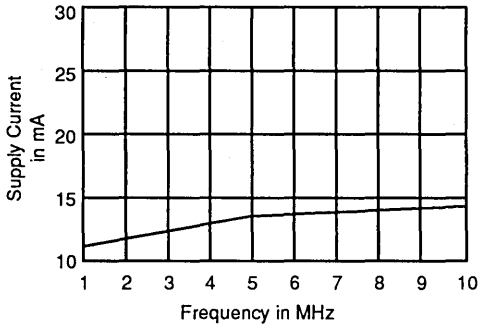


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

08007G-6

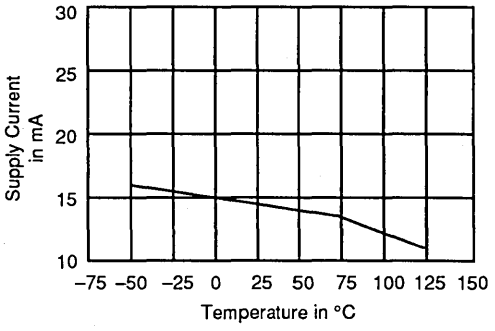


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

08007G-7

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CLV032		CDV028		PL 032		PD 028		TS 032		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	11	14	8	12	8	12	6	10	10	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	10	14	8	12	8	12	8	10	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9,10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C256							Unit
JEDEC	Standard				-55	-70	-90	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	
				Max	55	70	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	
				Max	55	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	–	–	
				Max	35	40	40	50	50	50	50	ns
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	–	
				Max	25	25	25	30	30	30	30	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	0	
				Max	–	–	–	–	–	–	–	ns

Notes:

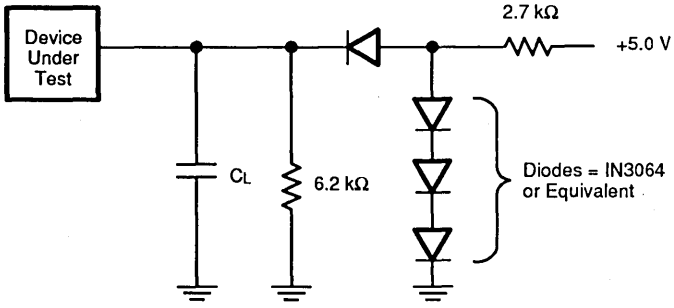
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C256 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *For the -55 and -70:*

   Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

   For all other versions:

   Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V inputs and outputs

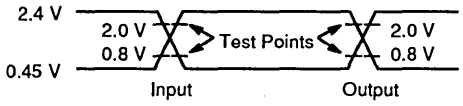
SWITCHING TEST CIRCUIT



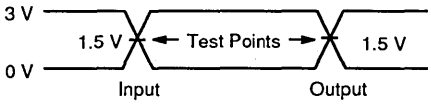
C_L = 100 pF including jig capacitance (30 pF for –55, –70)

08007G–8

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



08007G-9

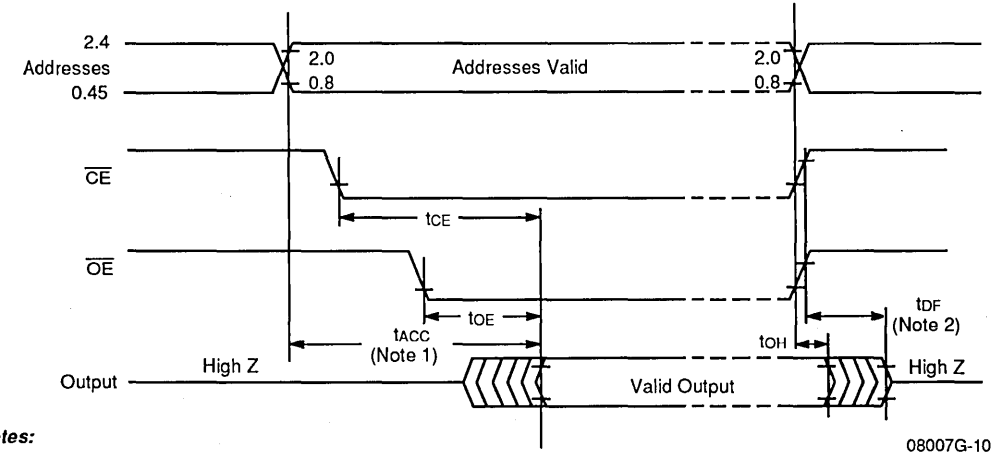
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -55 and -70.

KEY TO SWITCHING TEST WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS



08007G-10

Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27C512

512 Kilobit (65,536 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 70 ns
- **Low power consumption**
  - — 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite™ programming**
  - — Typical programming time of 8 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions
- **Standard 28-pin DIP, PDIP, 32-pin TSOP, LCC and PLCC packages**
- **DESC SMD No. 5962–87648**

GENERAL DESCRIPTION

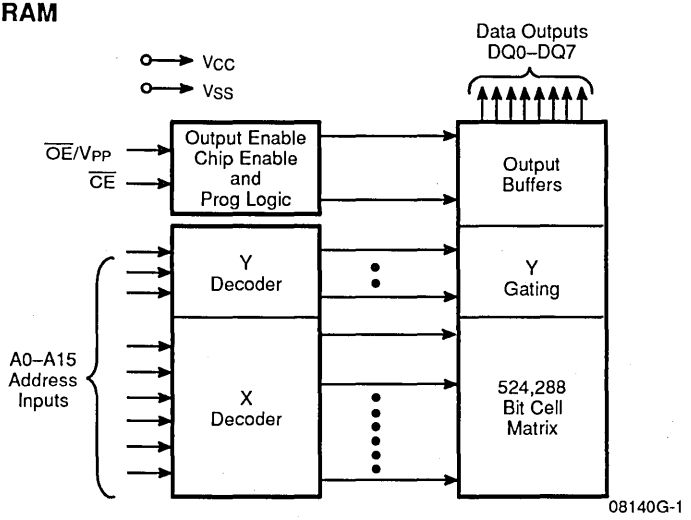
The Am27C512 is a 512 K-bit ultraviolet erasable programmable read-only memory. It is organized as 64K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP, TSOP and PLCC packages.

Typically, any byte can be accessed in less than 70 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C512 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C512 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in a typical programming time of 8 seconds.

BLOCK DIAGRAM



08140G-1

Publication# 08140 Rev. G Amendment/0
Issue Date: July 1993

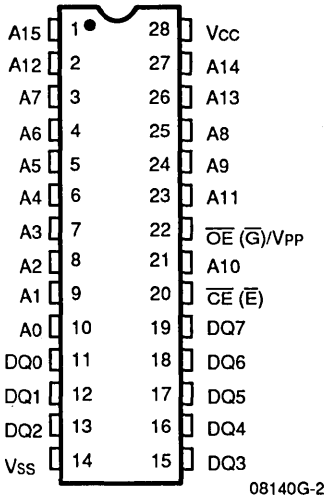
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C512					
Ordering Part No: $V_{CC} \pm 5\%$	-75					-255
$V_{CC} \pm 10\%$		-90	-120	-150	-200	-250
Max Access Time (ns)	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	40	40	50	50	75	100

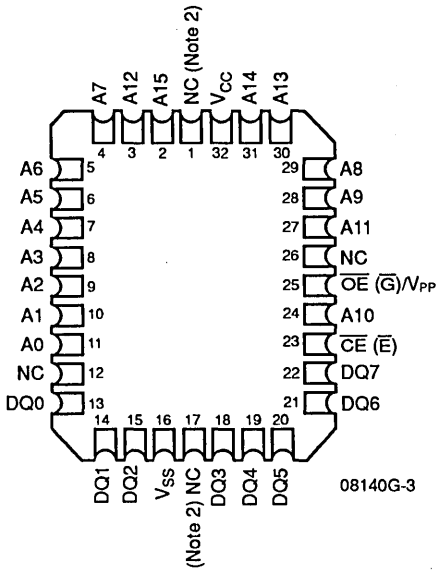
CONNECTION DIAGRAMS

Top View

DIP



PLCC/LCC



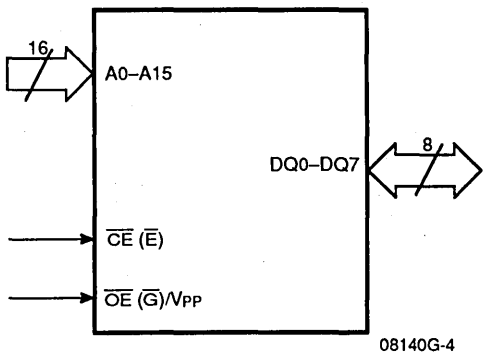
Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *Don't use (DU) for PLCC.*

PIN DESIGNATIONS

A0–A15	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0–DQ7	=	Data Inputs/Outputs
DU	=	No External Connection (Do Not Use)
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)/V_{PP}	=	Output Enable Input/ Program Supply Voltage
V_{CC}	=	V_{CC} Supply Voltage
V_{SS}	=	Ground

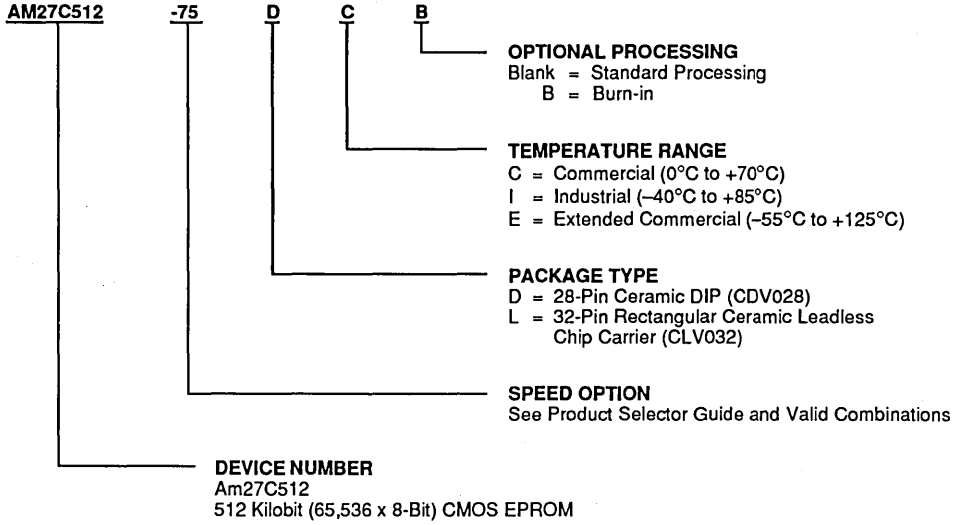
LOGIC SYMBOL



ORDERING INFORMATION

EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C512-75	DC, DCB, LC, LCB
AM27C512-90	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C512-120	
AM27C512-150	
AM27C512-200	
AM27C512-250	
AM27C512-255	

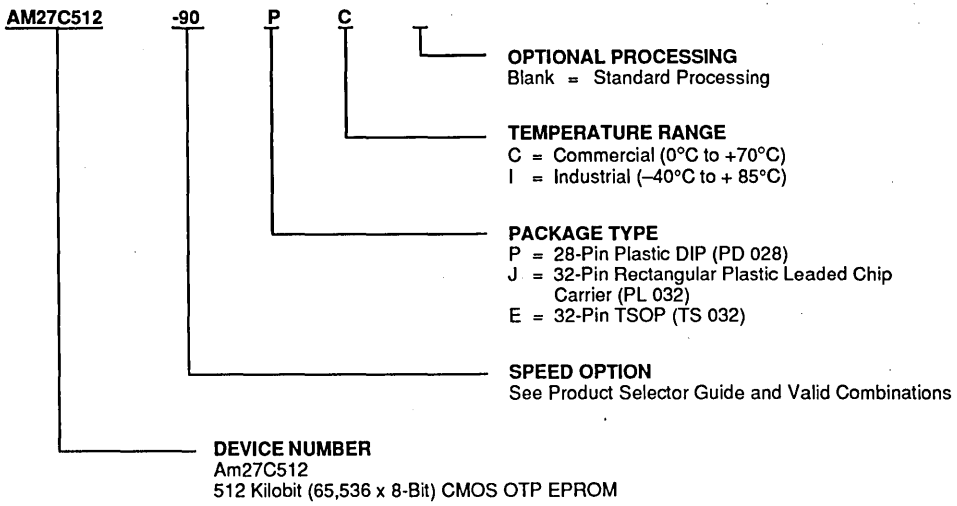
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C512-90	PC, JC, EC PI, JI, EI
AM27C512-120	
AM27C512-150	
AM27C512-200	
AM27C512-255	

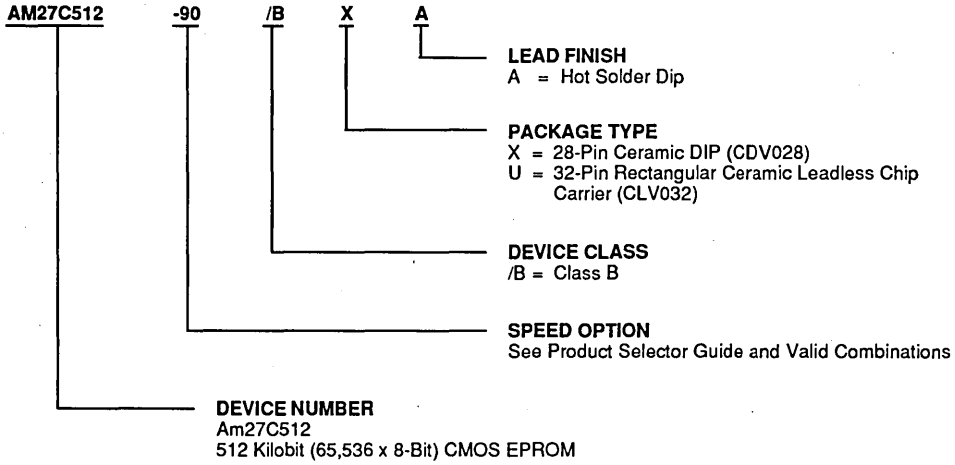
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C512-90	/BXA, /BUA
AM27C512-120	
AM27C512-150	
AM27C512-200	
AM27C512-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C512

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C512 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C512. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The Am27C512 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C512 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C512 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C512

Upon delivery or after each erasure the Am27C512 has all 524,288 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C512 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the $\overline{OE}/V_{PP}$ and $\overline{CE}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 μs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C512. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at V_{CC} = 5.25 V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C512 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C512 may be common. A TTL low-level program pulse applied to an Am27C512 $\overline{CE}$ input and $\overline{OE}/V_{PP}$ = 12.75 V ± 0.25 V, will program that Am27C512. A high-level $\overline{CE}$ input inhibits the other Am27C512 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{CE}$ at V_{IL} and $\overline{OE}/V_{PP}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C512.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the Am27C512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code, and byte 1 ($A0 = V_{IH}$), the device code. For the Am27C512, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C512 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 μA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C512 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}/V_{PP}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}/V_{PP}$	A0	A9	Outputs
Read		V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable		X	V_{IH}	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	Hi-Z
Standby (CMOS)		V_{CC} + 0.3 V	X	X	X	Hi-Z
Program		V_{IL}	V_{PP}	X	X	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	D_{OUT}
Program Inhibit		V_{IH}	V_{PP}	X	X	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	91H

Notes:

1. *V_H = 12.0 ± 0.5 V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A10–A15 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Voltage with Respect To V_{SS}
- All pins except A9, V_{PP}, V_{CC} ..... −0.6 V to V_{CC} + 0.5 V
- A9 and V_{PP} ..... −0.6 V to +13.5 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C512-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27C512-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA,			30	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

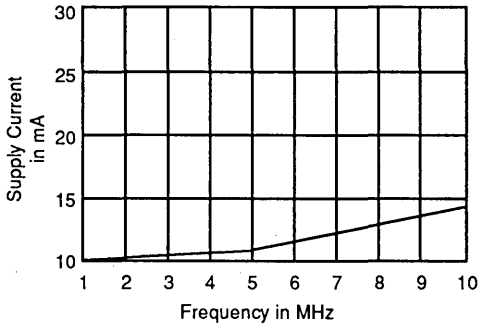


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

08140G-5

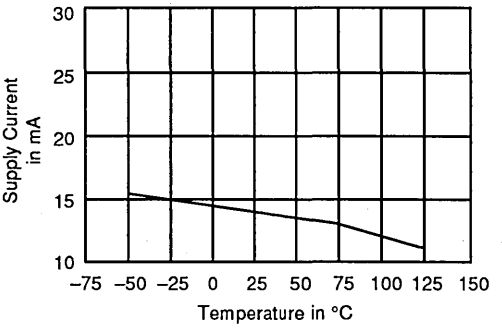


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

08140G-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CLV032		CDV028		PL 032		PD 028		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	9	12	10	12	9	12	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	10	12	10	13	9	12	6	10	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz*

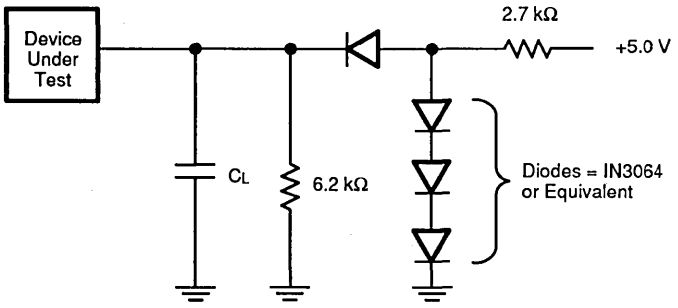
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, 4 and 5) (for APL Products, Group A, Subgroups 9,10, and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C512						Unit
JEDEC	Standard				-75	-90	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	
				Max	70	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	
				Max	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	–	
				Max	40	40	50	50	75	75	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	
				Max	25	30	30	30	30	30	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	
				Max	–	–	–	–	–	–	ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C512 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V inputs and outputs
5. *For the Am27C512-75:*
   Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

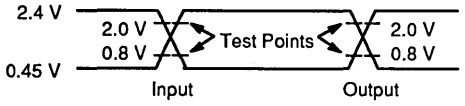
SWITCHING TEST CIRCUIT



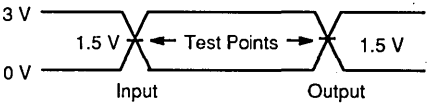
C_L = 100 pF including jig capacitance (30 pF for -75)

08140G-7

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



08140G-8

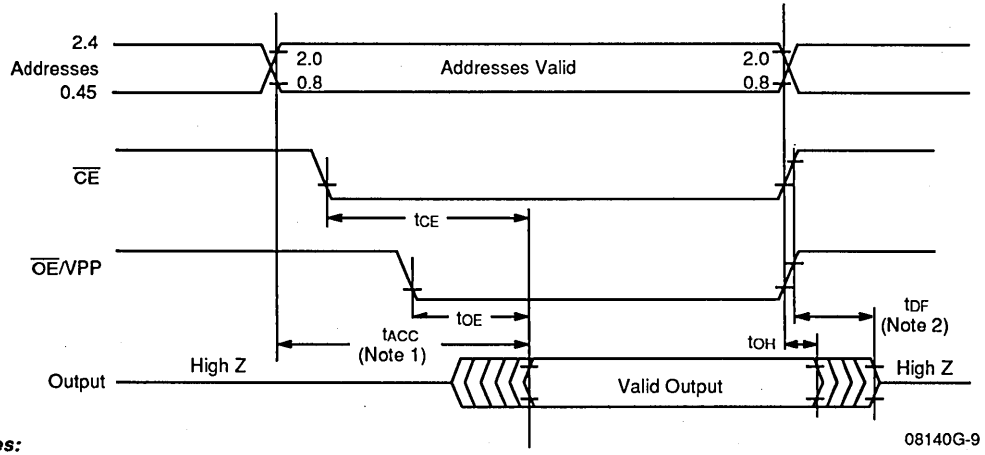
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -75 device.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27C010

1 Megabit (131,072 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 90 ns
- **Low power consumption**
  - — 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite™ programming**
  - — Typical programming time of 16 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions
- **Compact 32-pin DIP, PDIP, TSOP, LCC and PLCC packages**
- **DESC SMD No. 5962-89614**

GENERAL DESCRIPTION

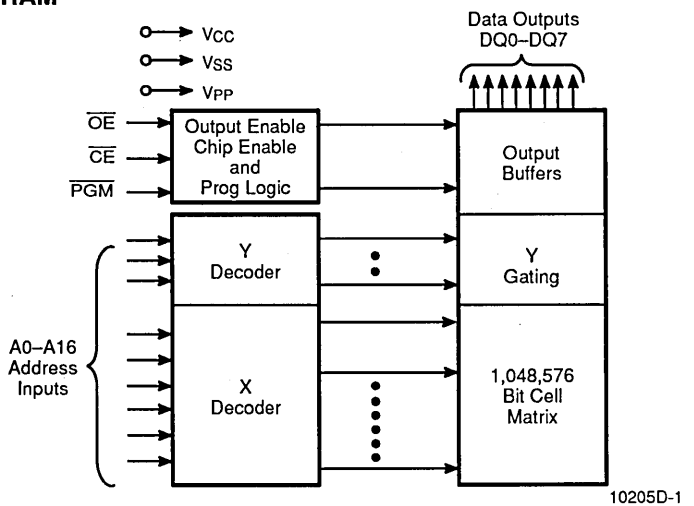
The Am27C010 is a 1 Megabit ultraviolet erasable programmable read-only memory. It is organized as 128K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP, TSOP, and PLCC packages.

Typically, any byte can be accessed in less than 90 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C010 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C010 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in a typical programming time of 16 seconds.

BLOCK DIAGRAM



10205D-1

Publication# 10205 Rev. D Amendment/0
Issue Date: July 1993

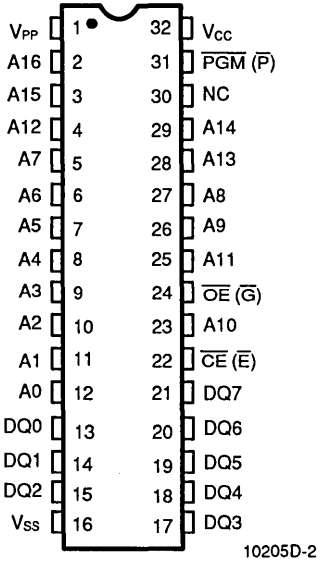
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C010					
Ordering Part No: $V_{CC} \pm 5\%$	-95	-105				-255
$V_{CC} \pm 10\%$	-90		-120	-150	-200	
Max Access Time (ns)	90	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	90	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	40	50	50	65	75	100

CONNECTION DIAGRAMS

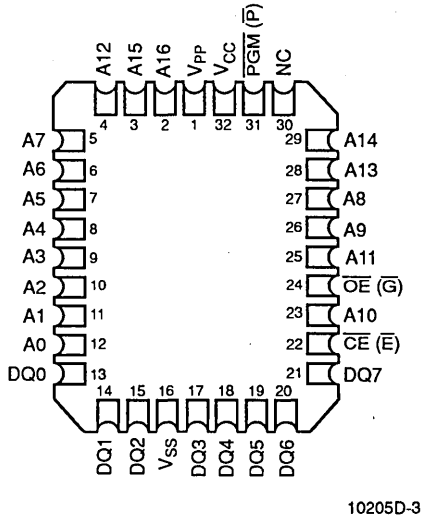
Top View

DIP



10205D-2

PLCC/LCC

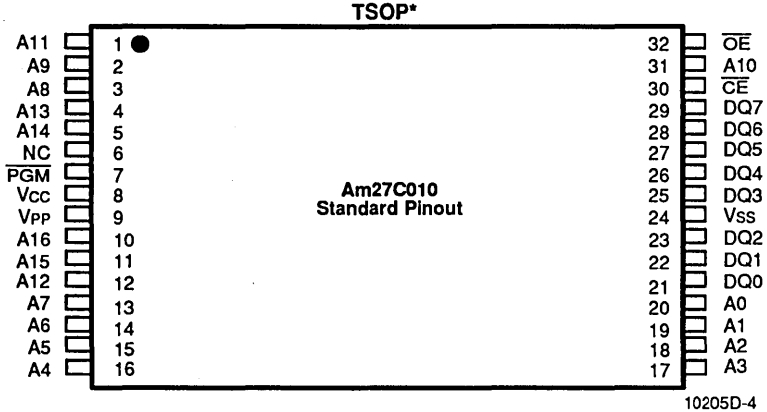


10205D-3

Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *The 32-pin DIP to 32-Pin LCC configuration varies from the JEDEC 28-pin DIP to 32-pin LCC configuration.*

TSOP*



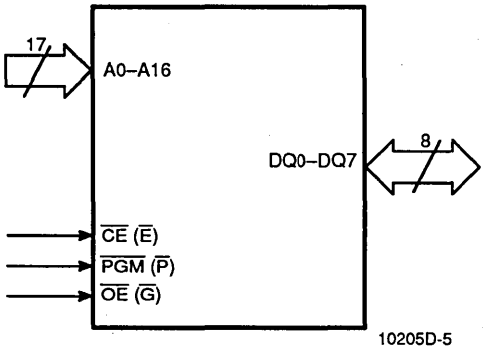
10205D-4

**Contact local AMD sales office for package availability*

PIN DESIGNATIONS

A0–A16	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable
DQ0–DQ7	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

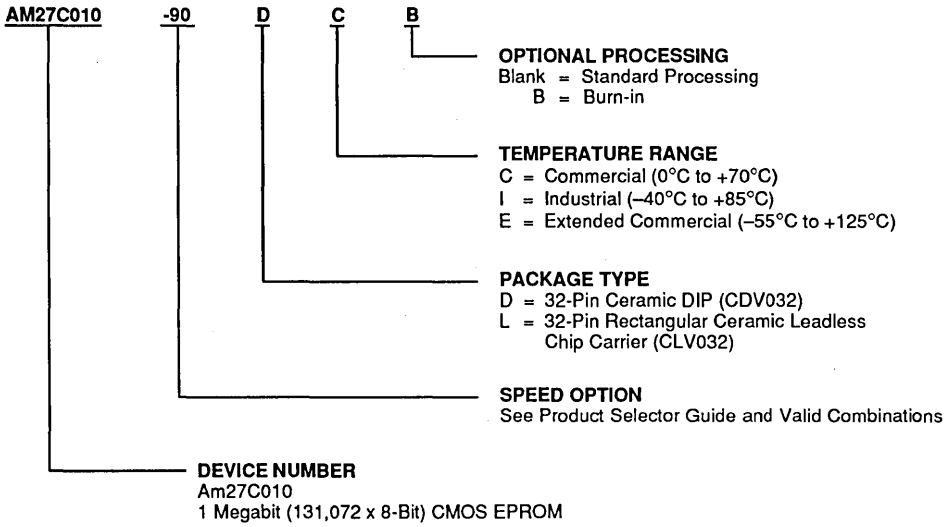
LOGIC SYMBOL



10205D-5

ORDERING INFORMATION
EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C010-90	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C010-95	
AM27C010-105	
AM27C010-120	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C010-150	
AM27C010-200	
AM27C010-255	

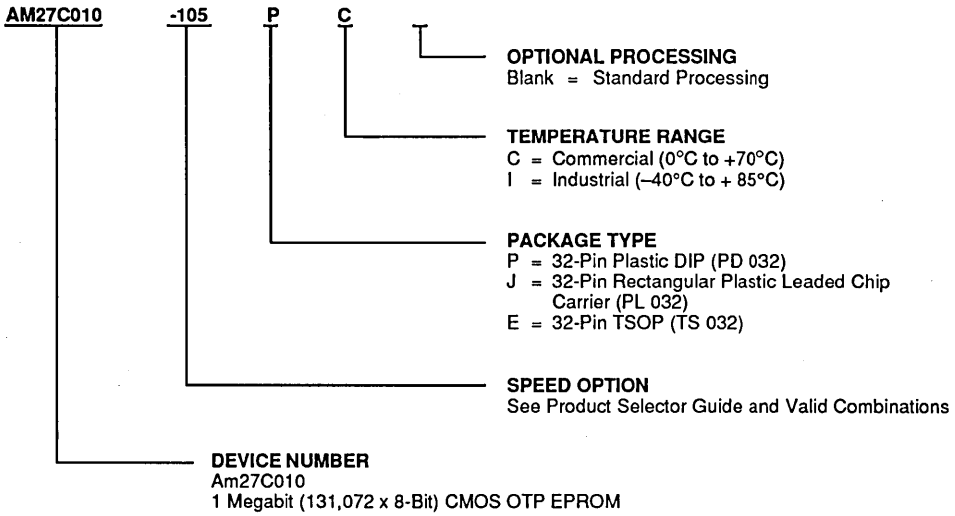
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C010-105	PC, JC, EC, PI, JI, EI
AM27C010-120	
AM27C010-150	
AM27C010-200	
AM27C010-255	

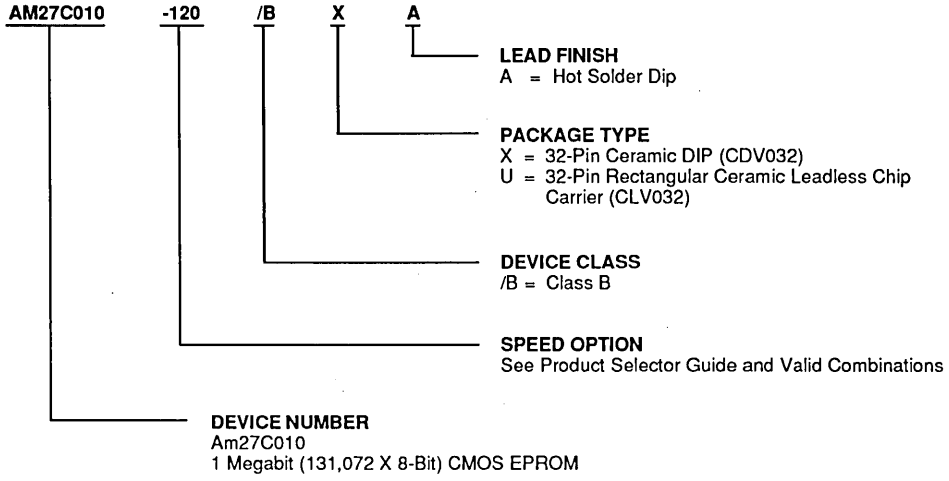
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C010-120	/BXA, /BUA
AM27C010-150	
AM27C010-200	
AM27C010-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C010

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C010 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C010. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C010 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C010 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C010 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C010

Upon delivery or after each erasure the Am27C010 has all 1,048,576 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C010 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}, and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C010. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C010 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C010 may be common. A TTL low-level program pulse applied to an Am27C010 $\overline{CE}$ input and V_{PP} = 12.75 V ± 0.25 V, $\overline{PGM}$ Low and $\overline{OE}$ High will program that Am27C010. A high-level $\overline{CE}$ input inhibits the other Am27C010 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C010.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C010. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$), the device code. For the Am27C010, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C010 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C010 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{CC}	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	V_{CC}	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	V_{CC}	Hi-Z
Standby (CMOS)		V_{CC} ± 0.3 V	X	X	X	X	V_{CC}	Hi-Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{CC}	0E

Notes:

1. *V_H = 12.0 V ± 0.5 V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A10–A16 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Voltage with Respect To V_{SS}
- All pins except A9, V_{PP}, V_{CC} . −0.6 V to V_{CC} + 0.5 V
- A9 and V_{PP} ..... −0.6 V to +13.5 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C010-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27C010-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}			10	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA	C/I Devices		30	mA
			E/M Devices		60	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$/V_{PP} = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

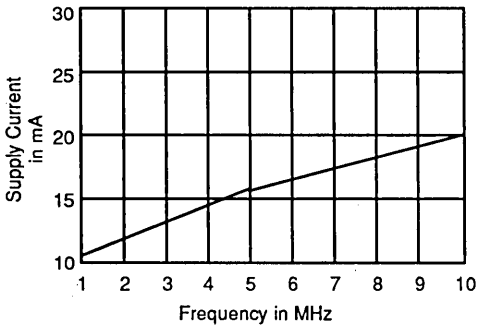


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

10205D-6

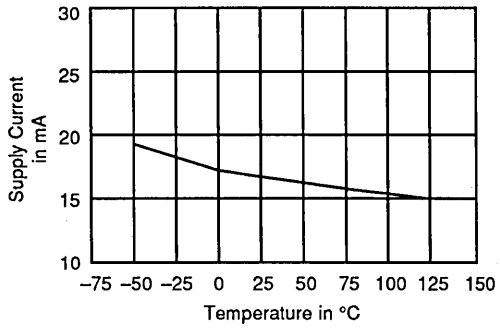


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

10205D-7

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CLV032		CDV032		PL 032		PD 032		TS 032		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	9	12	9	12	8	12	8	12	10	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	11	14	13	15	11	14	11	14	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz*

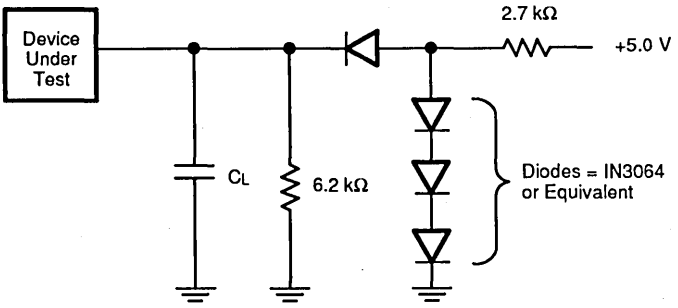
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9,10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C010						Unit
JEDEC	Standard				-95 -90	-105	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	
				Max	90	100	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	
				Max	90	100	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	–	
				Max	40	50	50	65	75	75	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	
				Max	25	25	35	35	40	40	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	
				Max	–	–	–	–	–	–	ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C010 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

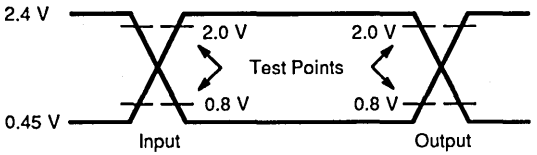
SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

10205D-8

SWITCHING TEST WAVEFORM



10205D-9

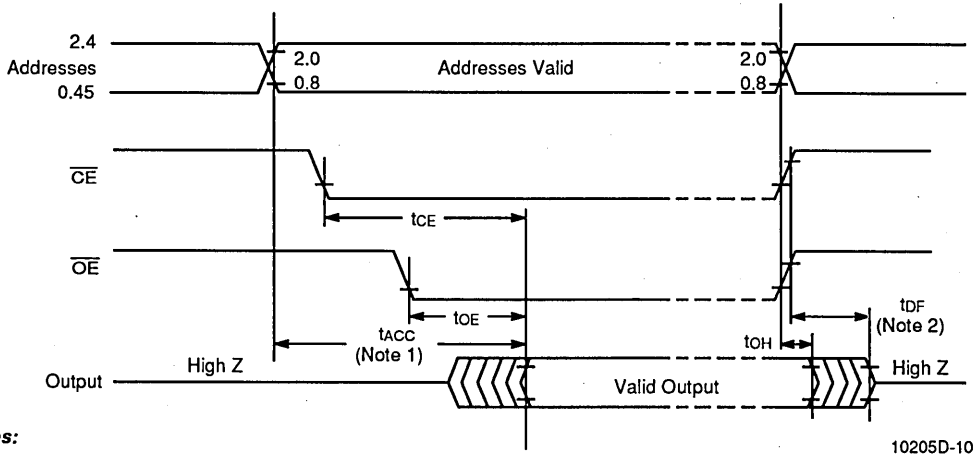
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS



10205D-10

Notes:

1. $\overline{OE}$ *may be delayed up to* $t_{ACC} - t_{OE}$ *after the falling edge of the addresses without impact on* t_{ACC}.
2. t_{DF} *is specified from* $\overline{OE}$ *or* $\overline{CE}$, *whichever occurs first.*

FINAL

Am27C1024

1 Megabit (65,536 x 16-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 85 ns
- **Low power consumption**
  - — 20 µA typical CMOS standby current
- **JEDEC-approved 40-Pin DIP and 44-Pin LCC pinouts**
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite™ programming**
  - — Typical programming time of 8 seconds
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions
- **DESC SMD No. 5962-86805**

GENERAL DESCRIPTION

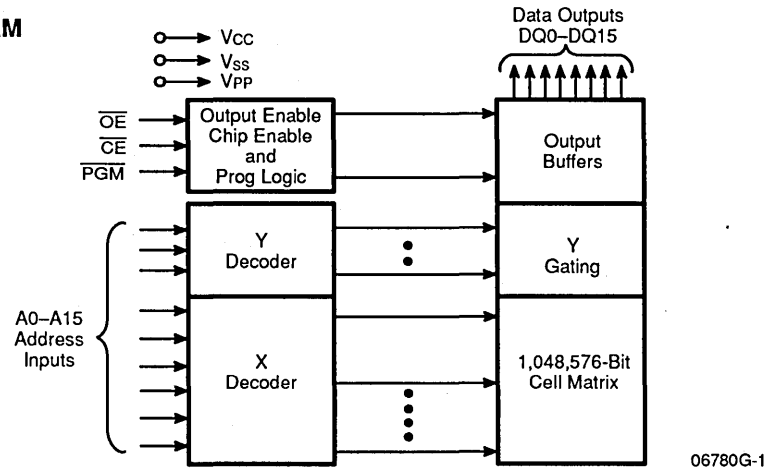
The Am27C1024 is a 1 Mbit ultraviolet erasable programmable read-only memory. It is organized as 64K words by 16 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 85 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C1024 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C1024 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in a typical programming time of 8 seconds.

BLOCK DIAGRAM



06780G-1

Publication# 06780 Rev. G Amendment/0
Issue Date: July 1993

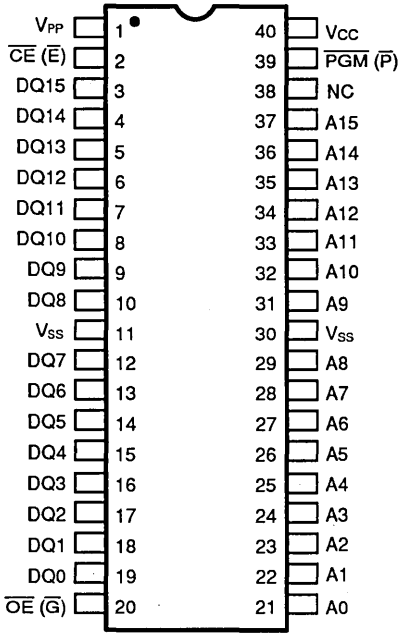
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C1024					
Ordering Part No: V_{CC} ± 5%	-85					-255
V_{CC} ± 10%		-90	-120	-150	-200	-250
Max Access Time (ns)	85	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	85	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	45	45	50	65	75	100

CONNECTIONS DIAGRAMS

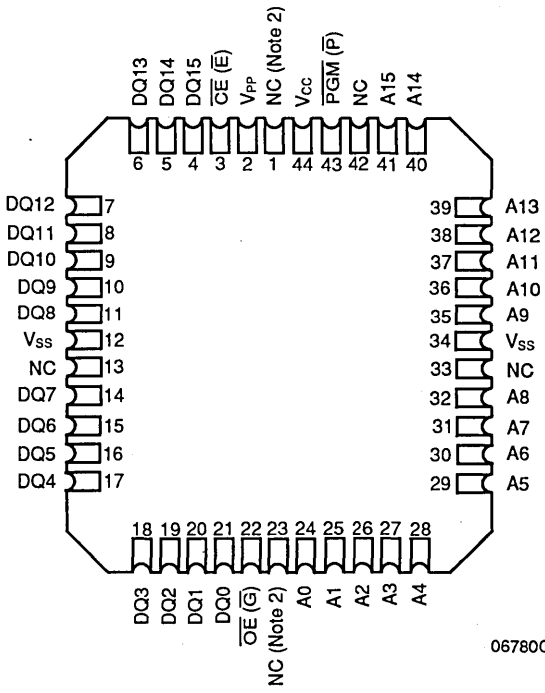
Top View

DIP



06780G-2

PLCC/LCC



06780G-3

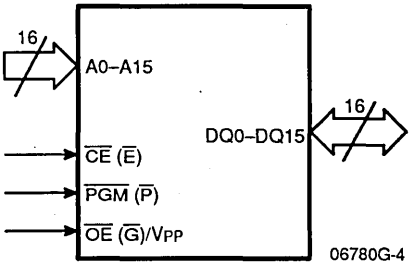
Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *Don't use (DU) for PLCC.*

PIN DESIGNATIONS

A0–A15	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable
DQ0–DQ15	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$	=	Program Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

LOGIC SYMBOL

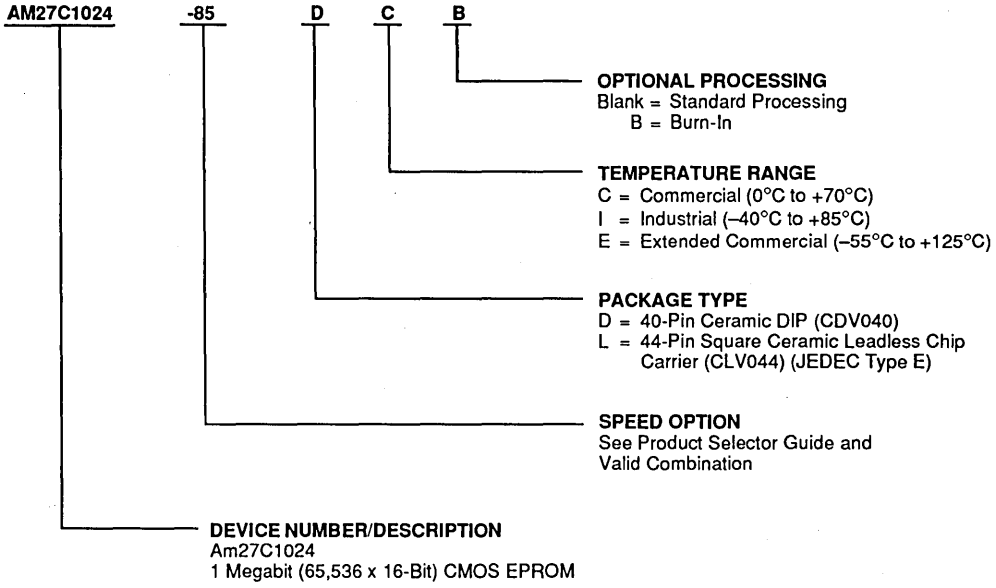


06780G-4

ORDERING INFORMATION

EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C1024-85	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C1024-90	
AM27C1024-120	DC, DCB, DI, DIB, DE, DEB, LCB, LIB, LE, LEB, LC, LI
AM27C1024-150	
AM27C1024-200	
AM27C1024-255	

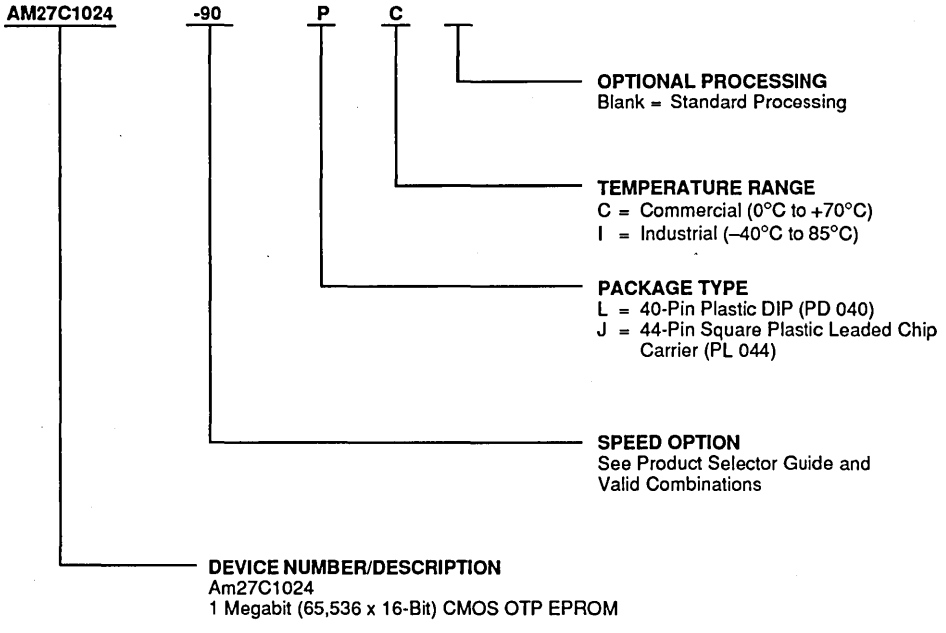
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C1024-90	PC, JC
AM27C1024-120	PC, JC, PI, JI
AM27C1024-150	
AM27C1024-200	
AM27C1024-255	

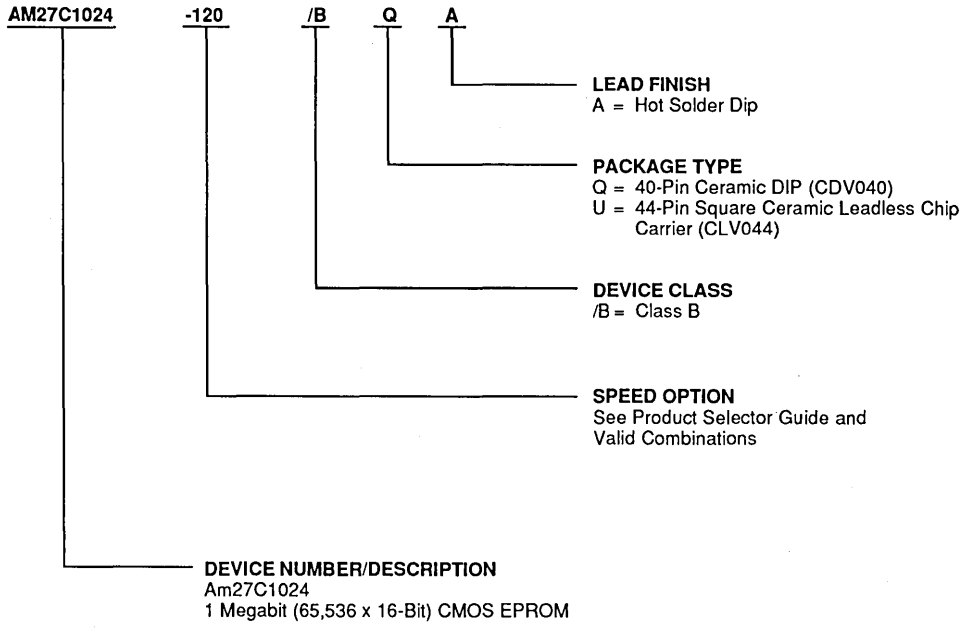
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C1024-120	/BQA, /BUA
AM27C1024-150	
AM27C1024-170	
AM27C1024-200	
AM27C1024-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C1024

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C1024 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C1024. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 (Å)—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C1024 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C1024 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C1024 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C1024

Upon delivery or after each erasure the Am27C1024 has all 1,048,576 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C1024 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin and $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}.

For programming, the data to be programmed is applied 16 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C1024. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C1024 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C1024 may be common. A TTL low-level program pulse applied to an Am27C1024 $\overline{CE}$ input with V_{PP} = 12.75 V ± 0.25 V, and $\overline{PGM}$ Low will program that Am27C1024. A high-level $\overline{CE}$ input inhibits the other Am27C1024 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} between 12.75 V ± 0.25 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C1024.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V open address the A9 of the Am27C1024. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device code. For the Am27C1024, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C1024 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C1024 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C1024 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{CC}	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	V_{CC}	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	V_{CC}	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	V_{CC}	Hi-Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H	V_{CC}	8CH

Notes:

1. *V_H = 12.0 V ± 0.5 V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A0–A15 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
- All pins except A9, V_{PP}, V_{CC} . −0.6 V to V_{CC} + 0.5 V
- A9 and V_{PP} ..... −0.6 V to +13.5 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C1024-XX5 .... +4.75 V to +5.25 V
- V_{CC} for Am27C1024-XX0 .... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA	C/I Devices		30	mA
			E/M Devices		50	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C1024 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

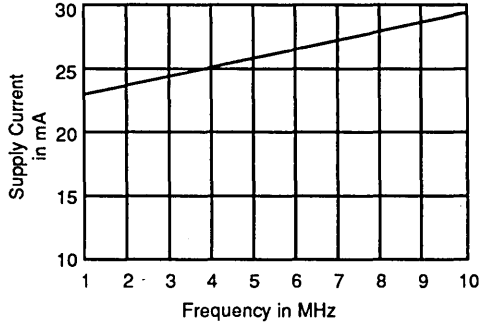
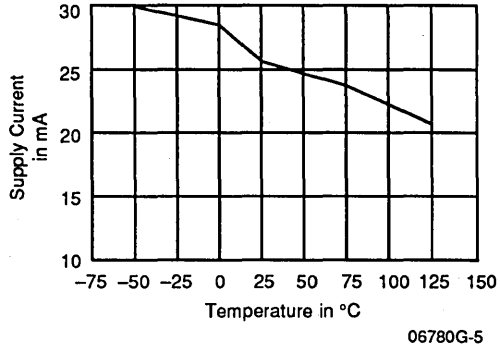


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C



06780G-5

Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5, f = 5 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV040		CLV044		PD 040		PL 044		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	9	12	8	12	7	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	14	11	14	11	14	11	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

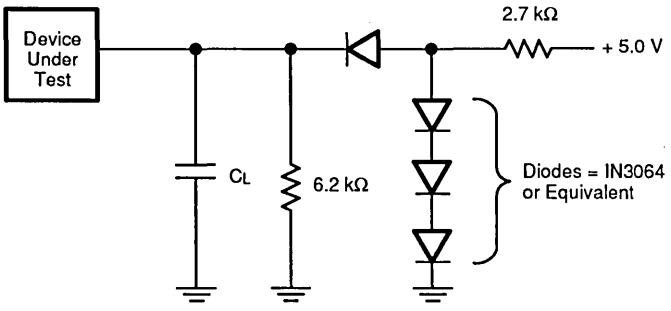
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C1024						Unit
JEDEC	Standard				-85	-90	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min							
				Max	85	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min							
				Max	85	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min							
				Max	45	45	50	65	75	75	ns
t_{EHQZ}	t_{DF}	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	ns
t_{GHQZ}	(Note 2)			Max	40	40	50	50	50	50	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, CE, or OE, whichever occurred first		Min	0	0	0	0	0	0	ns
				Max							

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C1024 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V inputs and outputs

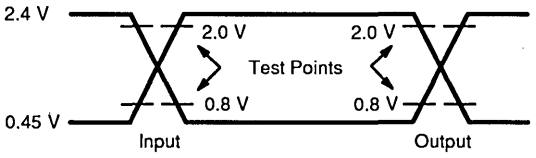
SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

06780G-6

SWITCHING TEST WAVEFORM



06780G-7

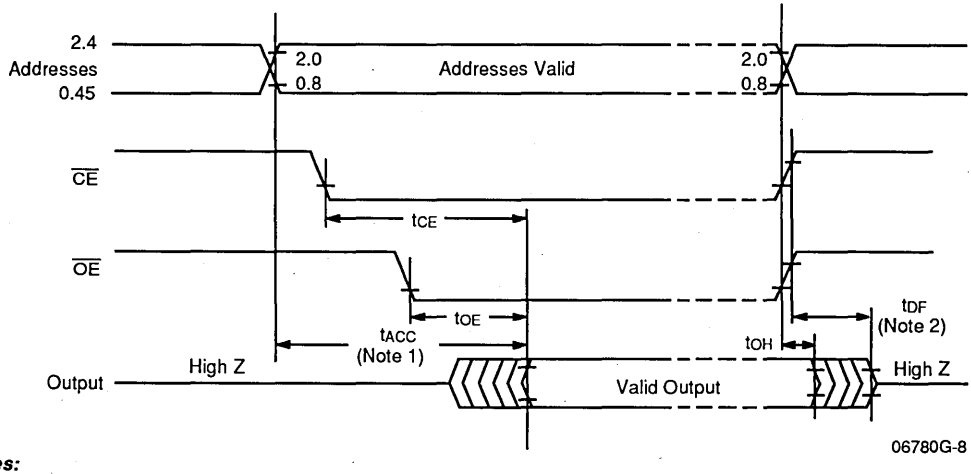
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Input pulse rise and fall times are < 20 ns.

KEY TO SWITCHING TEST WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27C020

2 Megabit (262,144 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 90 ns
- **Low power consumption**
  - — 100 µA maximum CMOS standby current
- **JEDEC-approved pinout**
  - — Plug in upgrade of 1 Mbit EPROM
  - — Easy upgrade from 28-pin JEDEC EPROMs
- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - — Typical programming time of 32 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Compact 32-pin DIP package requires no hardware change for upgrades to 8 Mbits**
- **DESC SMD No. 5962-90912**

GENERAL DESCRIPTION

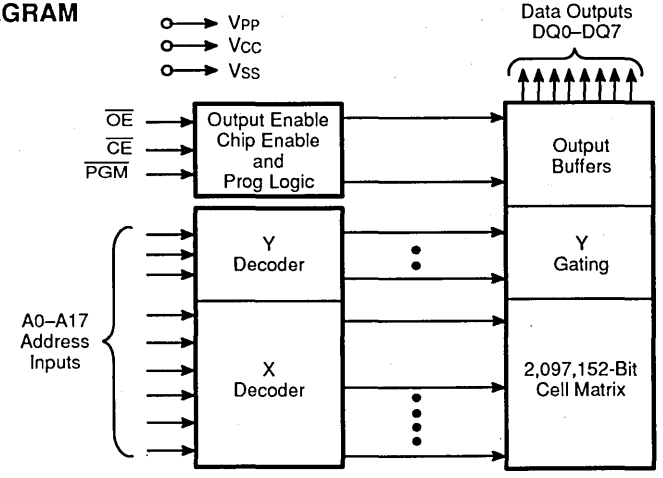
The Am27C020 is a 2 Mbit, ultraviolet erasable programmable read-only memory. It is organized as 256K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 90 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C020 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C020 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming times of 32 seconds.

BLOCK DIAGRAM



11507D-1

Publication# 11507 Rev. D Amendment/0
Issue Date: July 1993

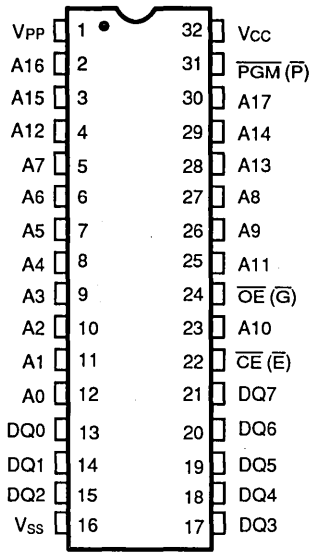
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C020					
Ordering Part No: VCC ±5%	-95	-105				-255
VCC ±10%	-90	-100	-120	-150	-200	-250
Max Access Time (ns)	90	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	50	65	75	100

CONNECTION DIAGRAMS

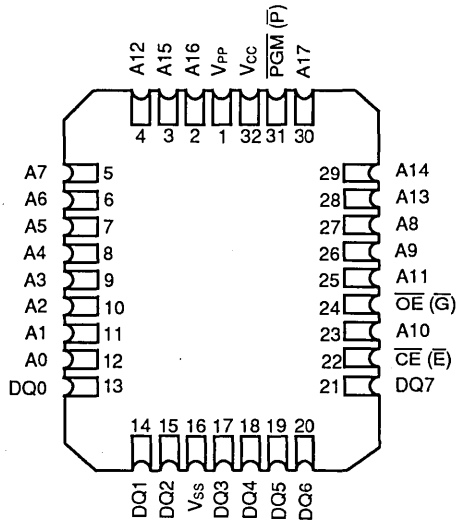
Top View

DIP



11507D-2

PLCC/LCC



11507D-3

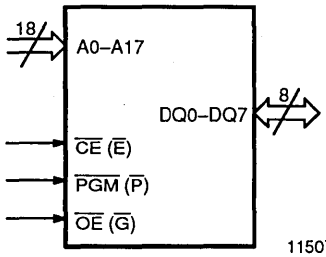
Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *The 32-pin DIP to 32-pin LCC configuration varies from the JEDEC 28-pin DIP to 32-pin LCC configuration.*

PIN DESIGNATIONS

A0–A17	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0–DQ7	=	Data Input/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
VCC	=	VCC Supply Voltage
VPP	=	Program Supply Voltage
VSS	=	Ground

LOGIC SYMBOL

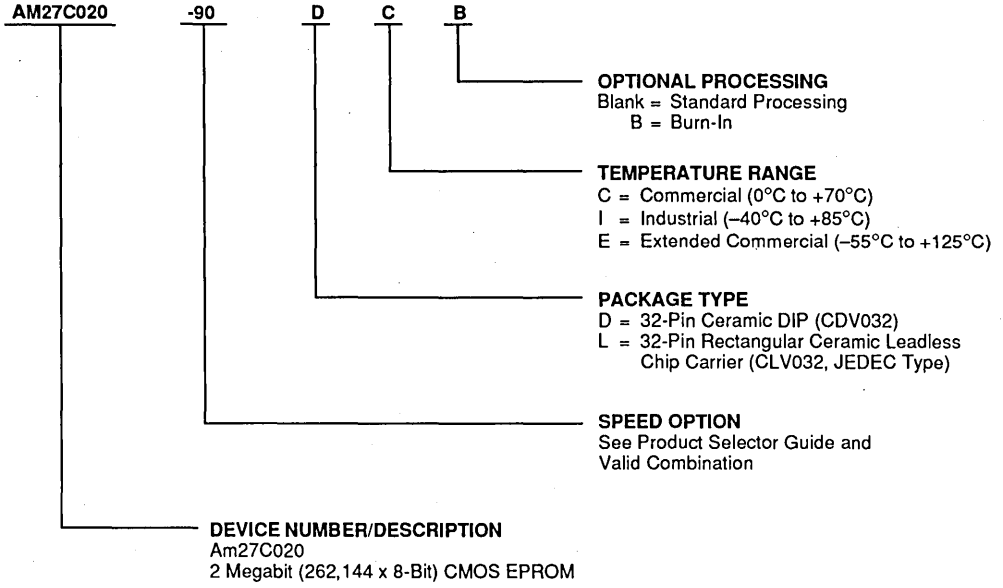


11507D-4

ORDERING INFORMATION

EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C020-90	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C020-95	
AM27C020-100	
AM27C020-105	
AM27C020-120	
AM27C020-150	DC, DCB, DI, DIB, DE, DEB, LCB, LIB, LE, LEB, LC, LI
AM27C020-200	
AM27C020-255	

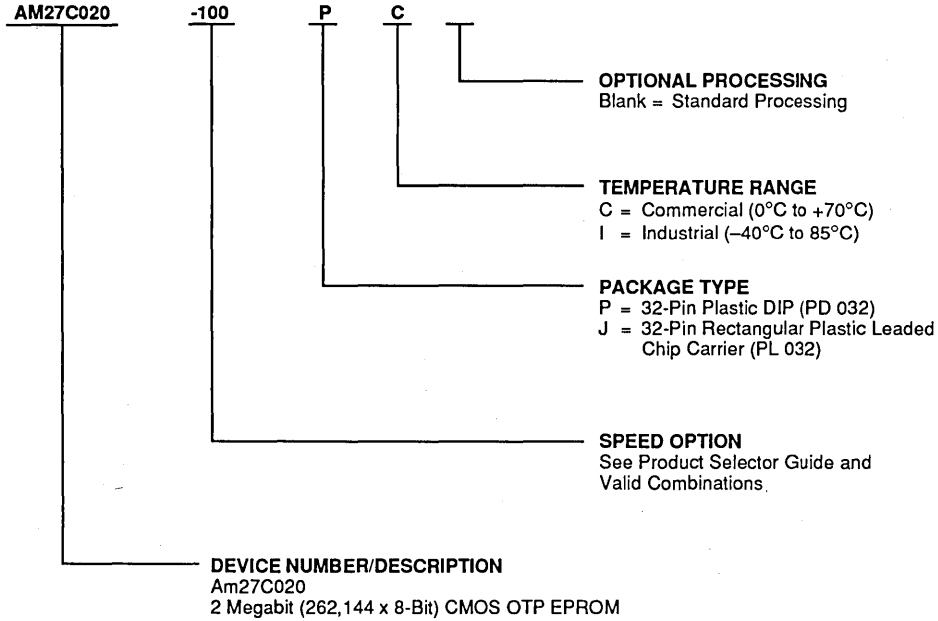
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C020-100	PC, JC, PI, JI
AM27C020-105	
AM27C020-120	
AM27C020-150	
AM27C020-200	
AM27C020-255	

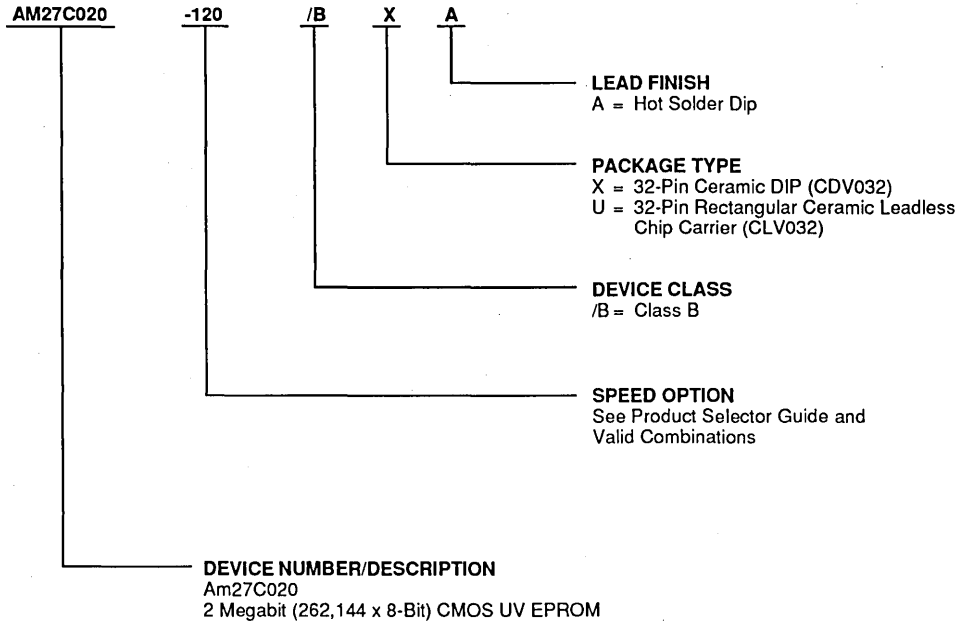
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C020-120	/BXA, /BUA
AM27C020-150	
AM27C020-200	
AM27C020-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C020

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C020 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C020. This dosage can be obtained by exposure to an ultraviolet lamp —wavelength of 2537 Å — with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C020 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C020, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C020 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C020

Upon delivery, or after each erasure, the Am27C020 has all 2,097,152 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C020 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ and $\overline{PGM}$ are at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulse and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C020. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Program Inhibit

Programming of multiple Am27C020s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C020 may be common. A TTL low-level program pulse applied to an Am27C020 $\overline{CE}$ input with V_{PP} = 12.75 V ± 0.25 V, $\overline{PGM}$ LOW, and $\overline{OE}$ HIGH will program that Am27C020.

A high-level $\overline{CE}$ input inhibits the other Am27C020s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C020.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C020. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and Byte 1 (A0 = V_{IH}), the device identifier code. For the Am27C020, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C020 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C020 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C020 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation, and
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the outut pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	97H

Notes:

1. *V_H = 12.0 V± 0.5 V*
2. *X can be either V_{IL} or V_{IH}*
3. *A1–A8 = A10–A17 = V_{IL}*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:
OTP Products ..... −65°C to +125°C
All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}:
All pins except A9, V_{PP}, and
V_{CC} (Note 1) ..... −0.6 V to V_{CC} + 0.6 V

A9 and V_{PP} (Note 2) ..... −0.6 V to 13.5 V

V_{CC} ..... −0.6 V to 7.0 V

Notes:

1. *During transitions, the input may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.*
2. *During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices

Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices

Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices

Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages:

V_{CC} for Am27C020-XX5 ..... +4.75 V to +5.25 V
V_{CC} for Am27C020-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 2 and 4) (for APL products, Group A, Subgroups 1, 2, 3, 6 and 7 are tested unless otherwise noted)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			−0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}			5.0	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA	C/I Devices		30	µA
			E/M Devices		60	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} + 0.3 V			100	µA
I_{PP1}	V_{PP} Supply Current (Read)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

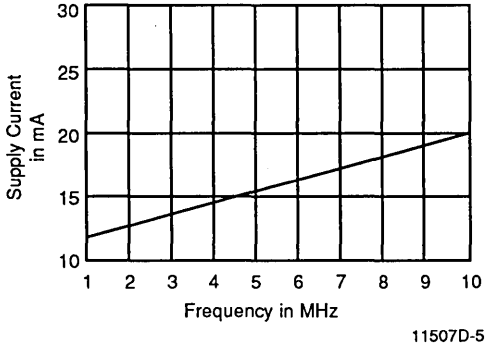


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

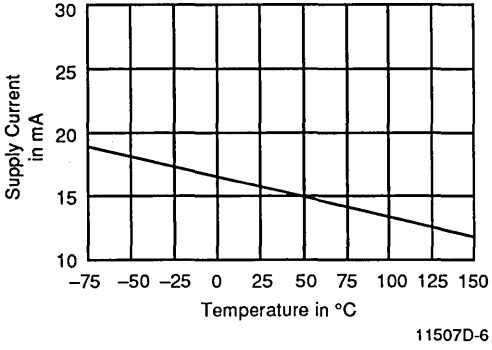


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		PD 032		PL 032		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	12	15	9	12	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

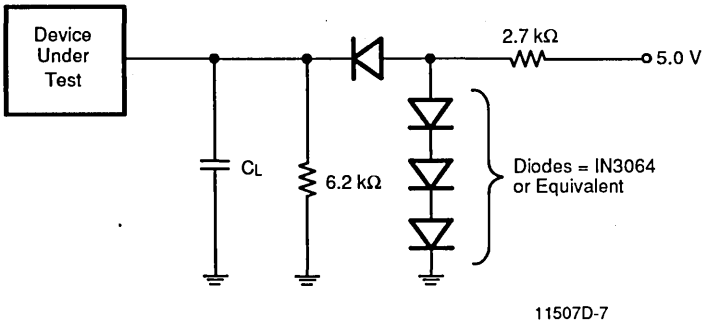
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C020						Unit
JEDEC	Standard				-95 -90	-105 -100	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min							ns
				Max	90	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min							ns
				Max	90	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min							ns
				Max	40	50	50	55	60	75	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	ns
				Max	25	30	30	30	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	ns
				Max							

Notes:

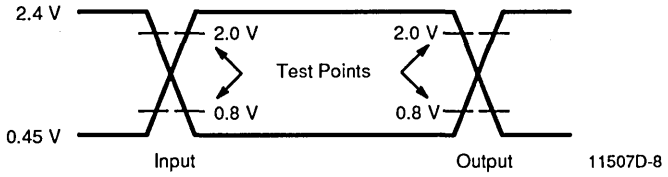
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C020 must not be removed from, or inserted into a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF,*
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.45 V to 2.4 V,
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V,
   Outputs: 0.8 V and 2 V

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



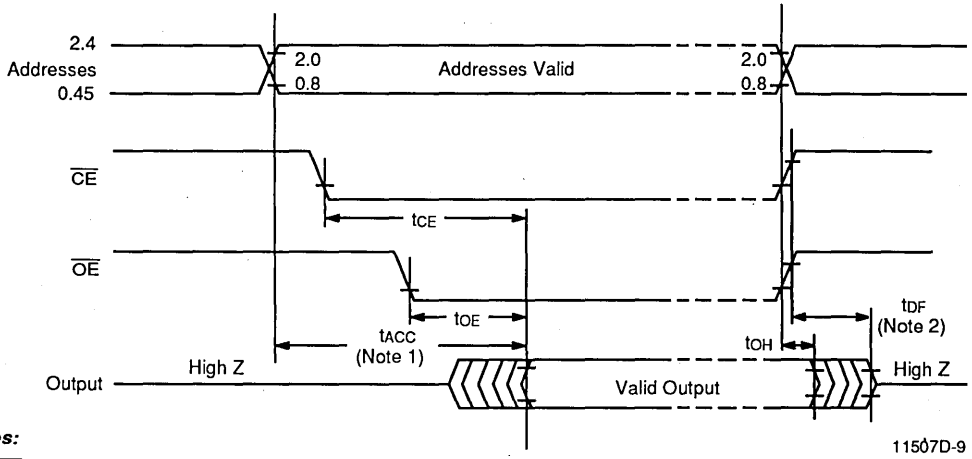
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0." Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORM



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27C2048

2 Megabit (131,072 x 16-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 90 ns
- **Low power consumption**
  - — 100 µA maximum CMOS standby current
- **JEDEC-approved pinout**
  - — Plug-in upgrade of 1 Mbit EPROM
  - — 40-pin DIP/PDIP
  - — 44-pin LCC/PLCC
- **Single +5 V power supply**
- **±10 V power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - — Typical programming time of 16 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **DESC SMD No. 5962-92140**

GENERAL DESCRIPTION

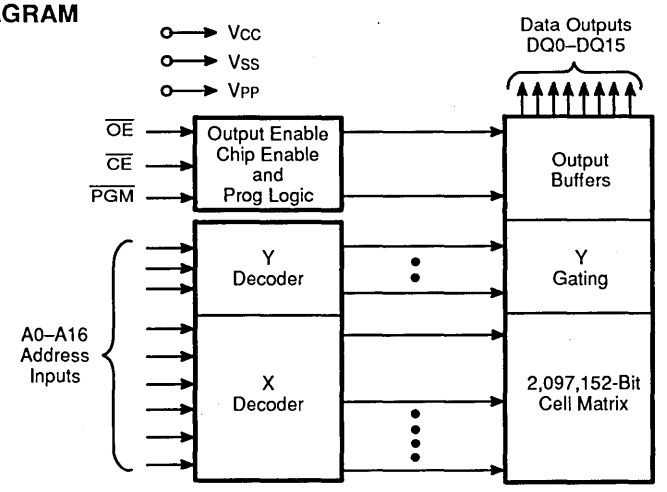
The Am27C2048 is a 2 Mbit, ultraviolet erasable programmable read-only memory. It is organized as 128K words by 16 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. The Am27C2048 is ideal for use in 16-bit microprocessor systems. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 90 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C2048 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C2048 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming time of 16 seconds.

BLOCK DIAGRAM



11407D-1

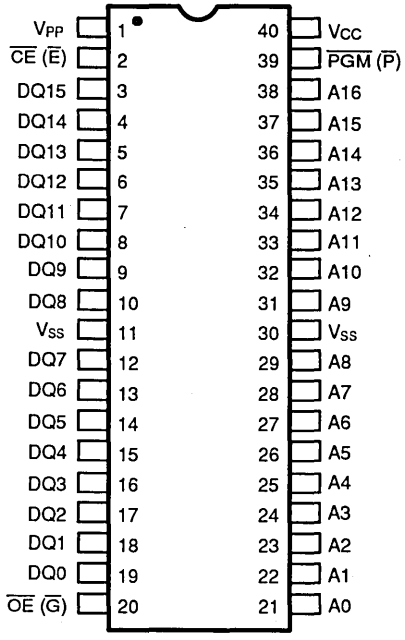
Publication# 11407 Rev. D Amendment/0
Issue Date: July 1993

PRODUCT SELECTOR GUIDE

Family Part No.	Am27C2048					
Ordering Part No:						
VCC ±5%	-95	-105	-125			-255
VCC ±10%	-90	-100	-120	-150	-200	-250
Max Access Time (ns)	90	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	50	65	75	100

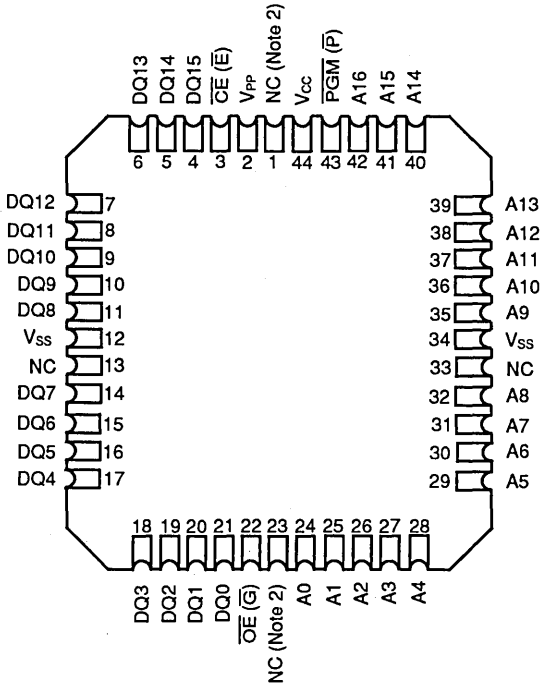
CONNECTION DIAGRAMS
Top View

DIP



11407D-2

LCC/PLCC



11407D-3

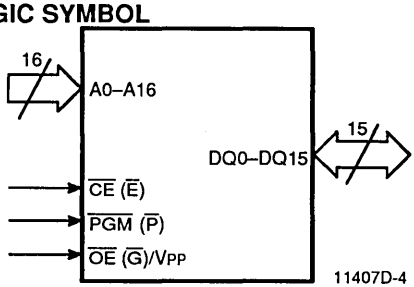
Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *Don't use (DU) for PLCC.*

PIN DESIGNATIONS

A0–A16	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0–DQ15	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
VCC	=	VCC Supply Voltage
VPP	=	Program Supply Voltage
VSS	=	Ground

LOGIC SYMBOL

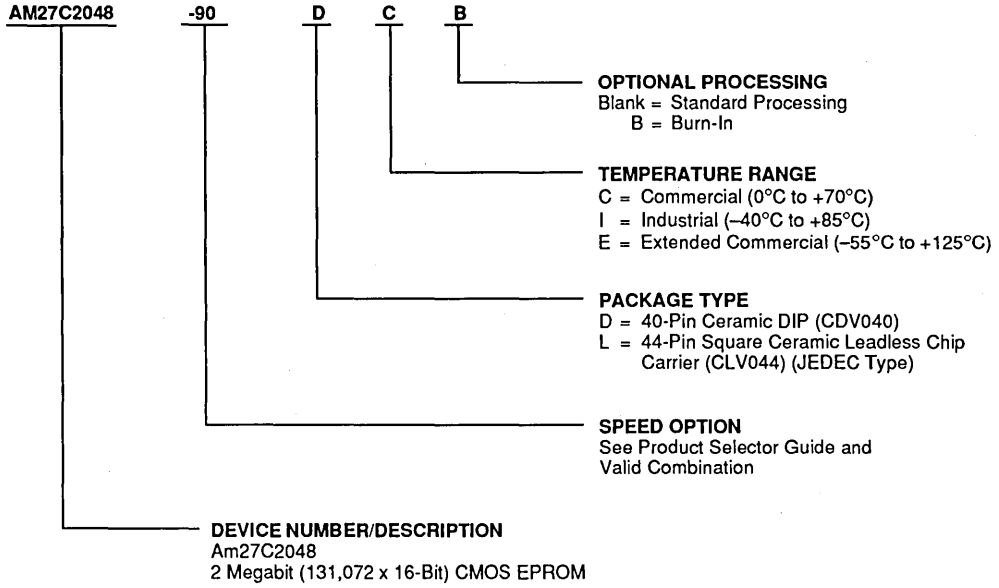


11407D-4

ORDERING INFORMATION

EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C2048-90	DC, DCB, DI, LC, LCB, LI
AM27C2048-95	
AM27C2048-105	
AM27C2048-120	
AM27C2048-125	DC, DCB, DI, DIB, DE, DEB, LCB, LIB, LE, LEB, LC, LI
AM27C2048-150	
AM27C2048-200	
AM27C2048-255	

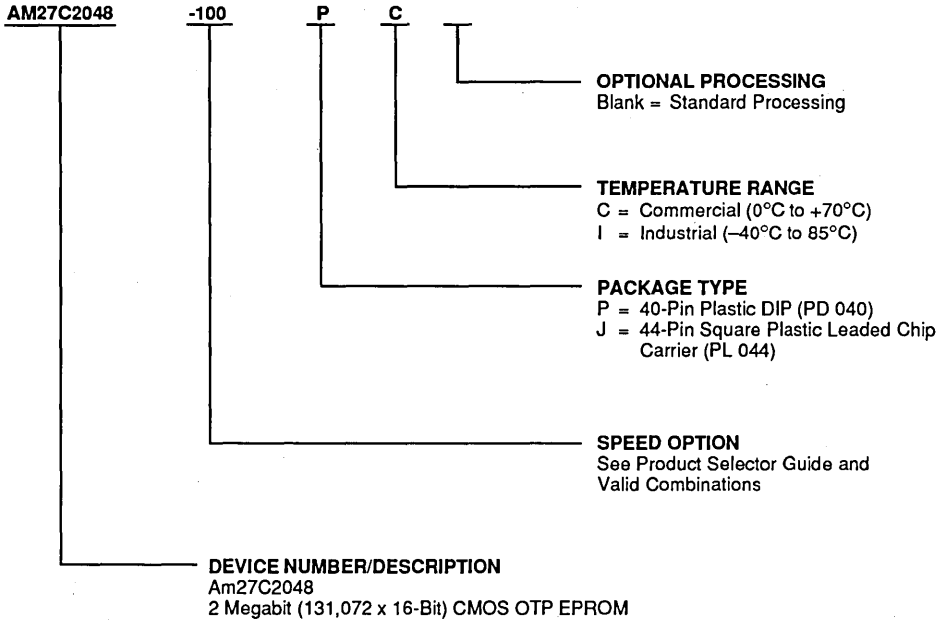
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C2048-100	PC, JC, PI, JI
AM27C2048-105	
AM27C2048-120	
AM27C2048-125	
AM27C2048-150	
AM27C2048-200	
AM27C2048-255	

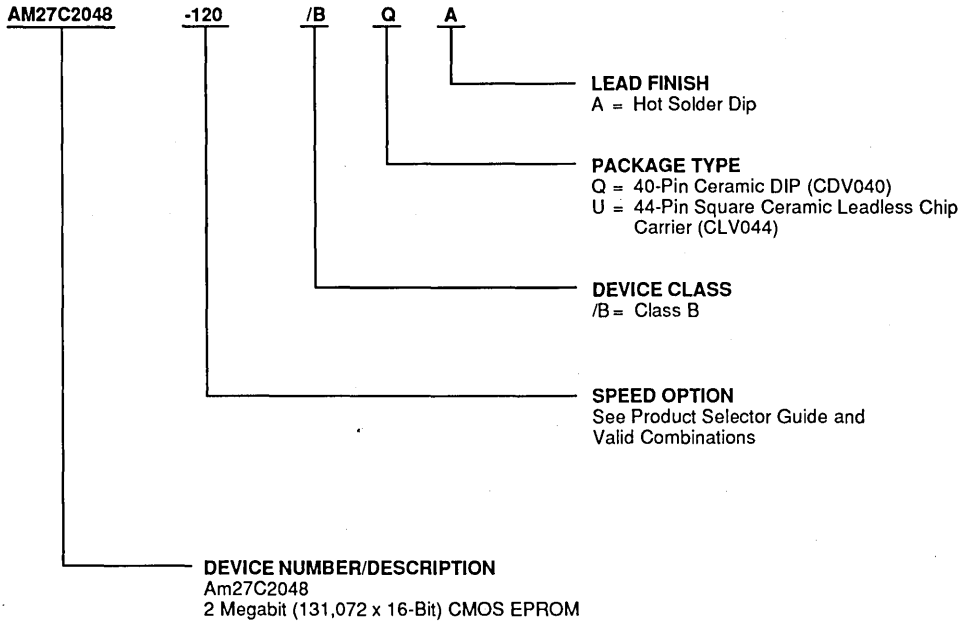
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C2048-120	/BQA, /BUA
AM27C2048-150	
AM27C2048-200	
AM27C2048-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C2048

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C2048 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C2048. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Å — with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C2048 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C2048, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C2048 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C2048

Upon delivery, or after each erasure, the Am27C2048 has all 2,097,152 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C2048 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, and $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}.

For programming, the data to be programmed is applied 16 bits in parallel to the data pins.

The flowchart (Figure 2) shows AMD's Flashrite algorithm. The Flashrite algorithm reduces programming time by using 100 µs programming pulse and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C2048. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP}$ = 5.25 V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C2048s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C2048 may be common. A TTL low-level program pulse applied to an Am27C2048 $\overline{CE}$ input with V_{PP} = 12.75 V ± 0.25 V and $\overline{PGM}$ LOW will program that Am27C2048. A high-level $\overline{CE}$ input inhibits the other Am27C2048 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$, at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C2048.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C2048. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and Byte 1 (A0 = V_{IH}), the device identifier code. For the Am27C2048, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C2048 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C2048 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C2048 also has a TTL-standby mode which re-

duce the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation, and
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the outut pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	X	High Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	98H

Notes:

1. *X can be either V_{IL} or V_{IH}.*
2. *V_H = 12.0 V ± 0.5 V*
3. *A1–A8 = A10–16 = V_{IL}.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:
OTP Products ..... −65°C to +125°C
All Other Products ..... −65°C to +150°C

Ambient Temperature:
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}:
All pins except A9, V_{PP}, and
V_{CC} (Note 1) ..... −0.6 V to V_{CC} + 0.6 V

A9 and V_{PP} (Note 2) ..... −0.6 V to 13.5 V

V_{CC} ..... −0.6 V to 7.0 V

Notes:

1. *During transitions, the input may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices

Case Temperature (Tc) ..... −40°C to +85°C

Extended Commercial (E) Devices

Case Temperature (Tc) ..... −55°C to +125°C

Military (M) Devices

Case Temperature (Tc) ..... −55°C to +125°C

Supply Read Voltages:

V_{CC} for Am27C2048-XX5 .... +4.75 V to +5.25 V
V_{CC} for Am27C2048-XX0 .... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 6 and 7 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}			5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA	C/I Devices		50	µA
			E/M Devices		60	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} + 0.3 V			100	µA
I_{PP1}	V_{PP} Supply Current (Read)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C2048 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

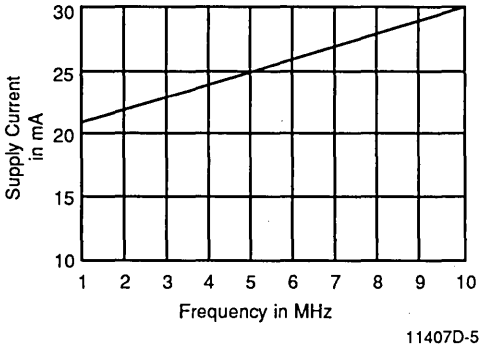


Figure 1. Typical Supply Current vs. Frequency V_{CC} = 5.5 V, T = 25°C

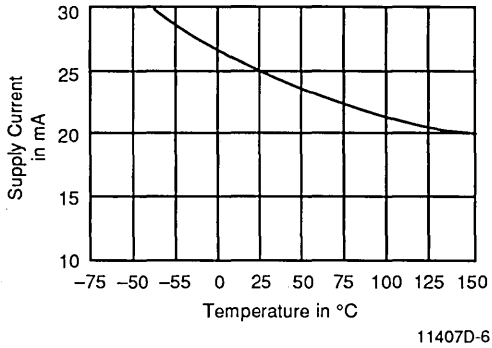


Figure 2. Typical Supply Current vs. Temperature V_{CC} = 5.5 V, f = 5 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV044		CLV044		PD 040		PL 044		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	10	12	8	10	10	12	7	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	15	10	12	12	15	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

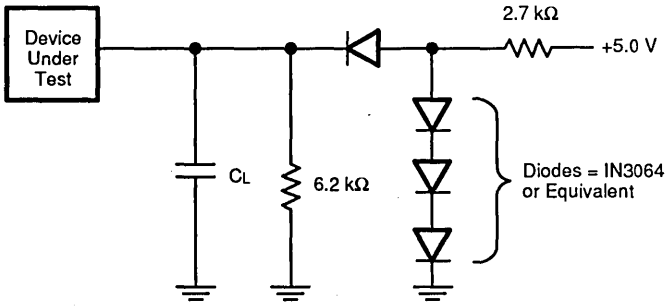
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9,10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C2048						Unit
JEDEC	Standard				-90 -95	-100 -105	-120 -125	-150	-200	-250 -255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min							ns
				Max	90	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min							ns
				Max	90	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min							ns
				Max	40	50	50	55	60	75	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	0	ns
				Max	25	30	30	30	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	ns
				Max							

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C2048 must not be removed from, or inserted into a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF,*
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.45 V to 2.4 V,
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V,
   Outputs: 0.8 V and 2 V

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

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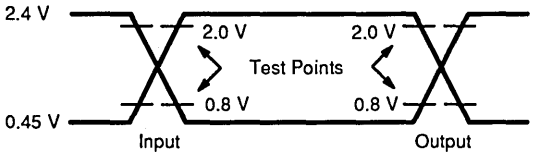
SWITCHING TEST WAVEFORM



11407D-8

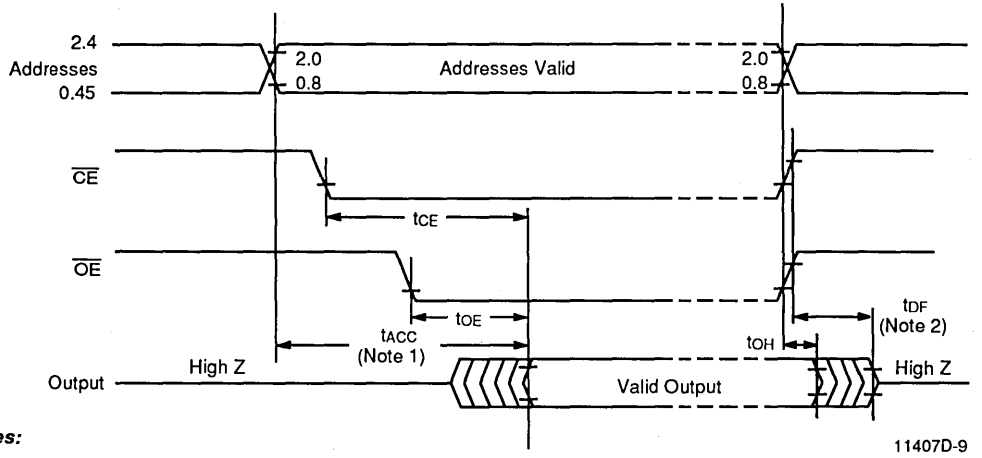
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Input pulse rise and fall times are < 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS



11407D-9

Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27C040

4 Megabit (524,288 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 100 ns
- **Low power consumption**
  - — 100 µA maximum CMOS standby current
- **JEDEC-approved pinout**
  - — Plug in upgrade of 1 Mbit EPROM and 2 Mbit EPROMs
  - — Easy upgrade from 28-pin JEDEC EPROMs
- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - — Typical programming time of 1 minute
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **High noise immunity**
- **Compact 32-pin DIP, PDIP, LCC and PLCC packages require no hardware change for upgrades to 8 Mbits**
- **DESC SMD No. 5962-91752**

GENERAL DESCRIPTION

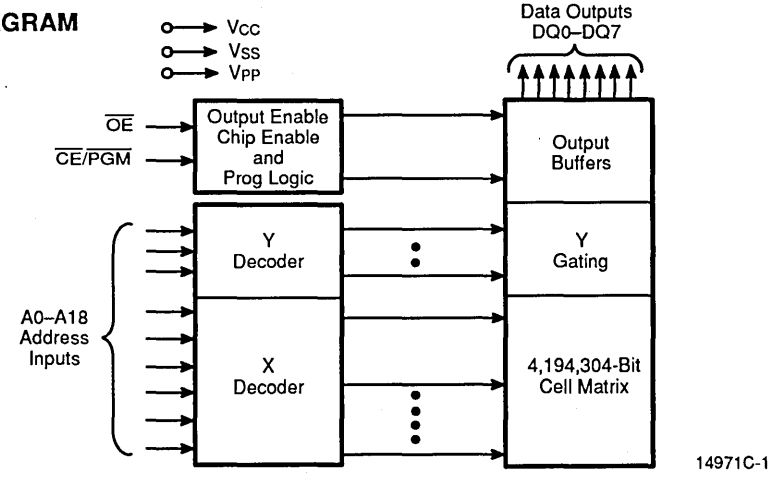
The Am27C040 is a 4 Mbit ultraviolet erasable programmable read-only memory. It is organized as 512K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C040 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C040 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming time of 1 minute.

BLOCK DIAGRAM



14971C-1

Publication# 14971 Rev. C Amendment/0
Issue Date: July 1993

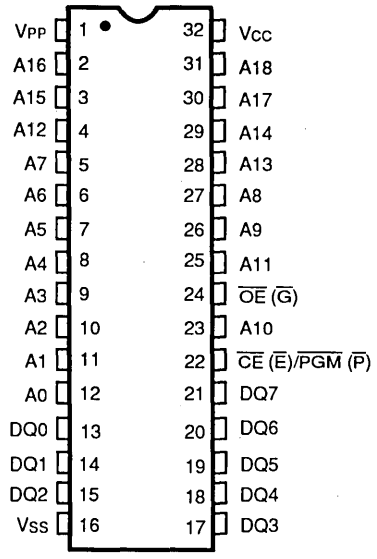
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C040			
Ordering Part No:				
V_{CC} ±5%	-105	-125		
V_{CC} ±10%	-100	-120	-150	-200
Max Access Time (ns)	100	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	65	75

CONNECTION DIAGRAMS

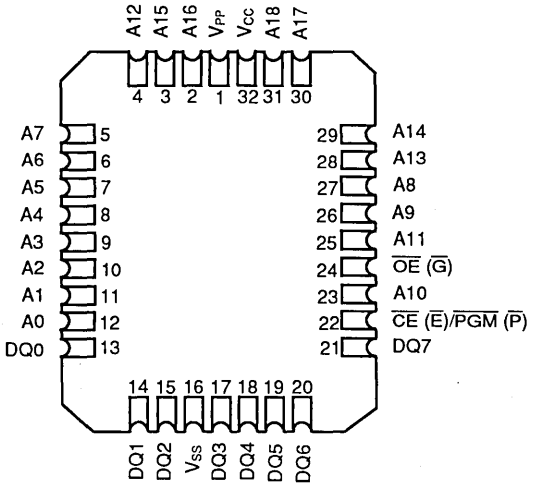
Top View

DIP



14971C-2

PLCC/LCC



14971C-3

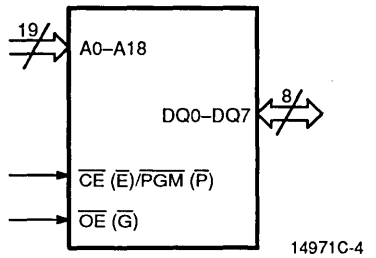
Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *The 32-pin DIP to 32-pin LCC configuration varies from the JEDEC 28-pin DIP to 32-pin LCC configuration.*

PIN DESIGNATIONS

A0–A18	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)/$\overline{PGM}$ ($\overline{P}$)	=	Chip Enable Input
DQ0–DQ7	=	Data Input/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

LOGIC SYMBOL

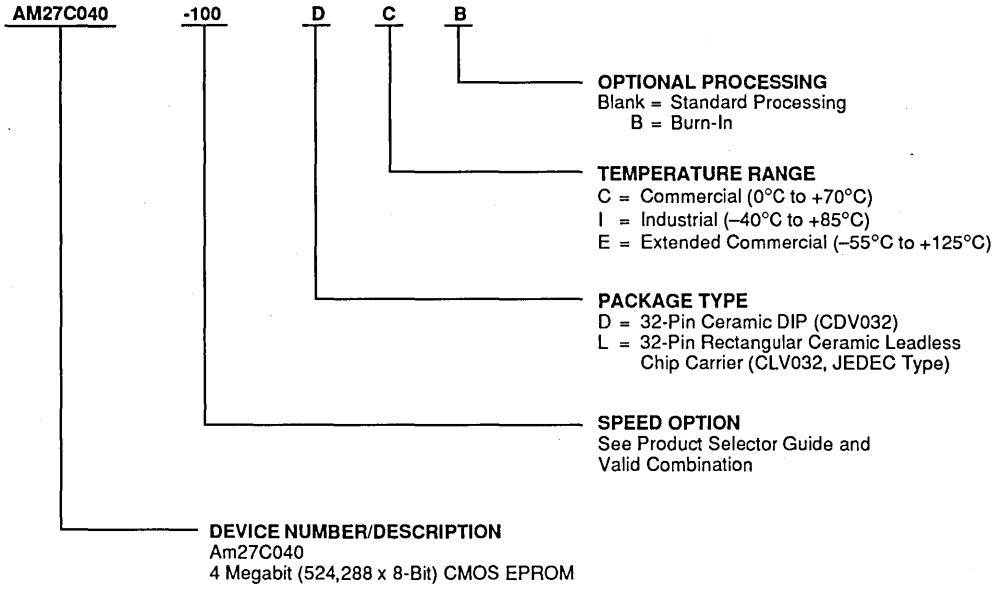


14971C-4

ORDERING INFORMATION

EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C040-100	DC, DCB, LC, LCB
AM27C040-105	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C040-120	
AM27C040-125	
AM27C040-150	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C040-200	

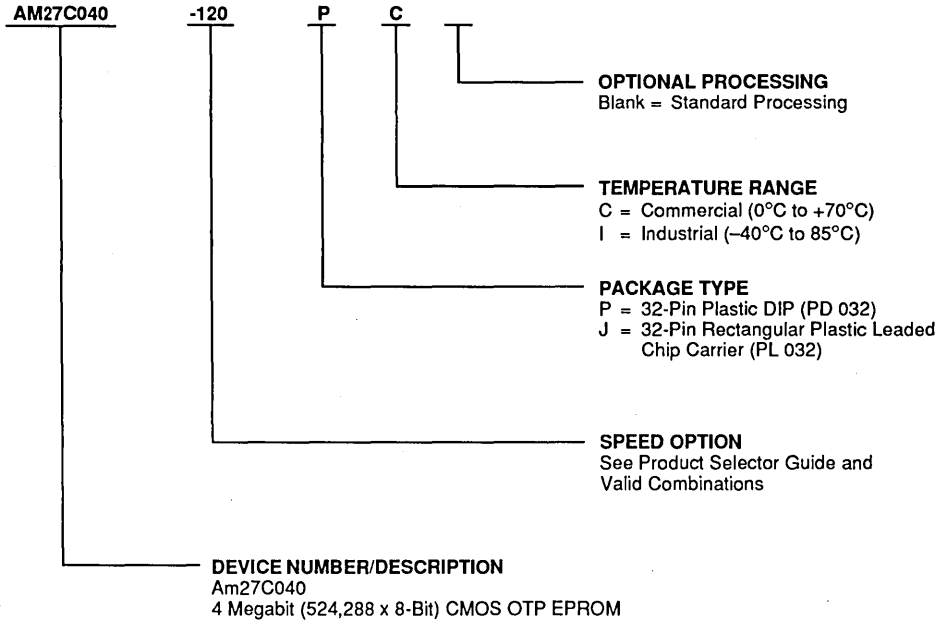
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products (Preliminary)

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C040-100	PC, JC, PI, JI
AM27C040-105	
AM27C040-120	
AM27C040-125	
AM27C040-150	
AM27C040-200	

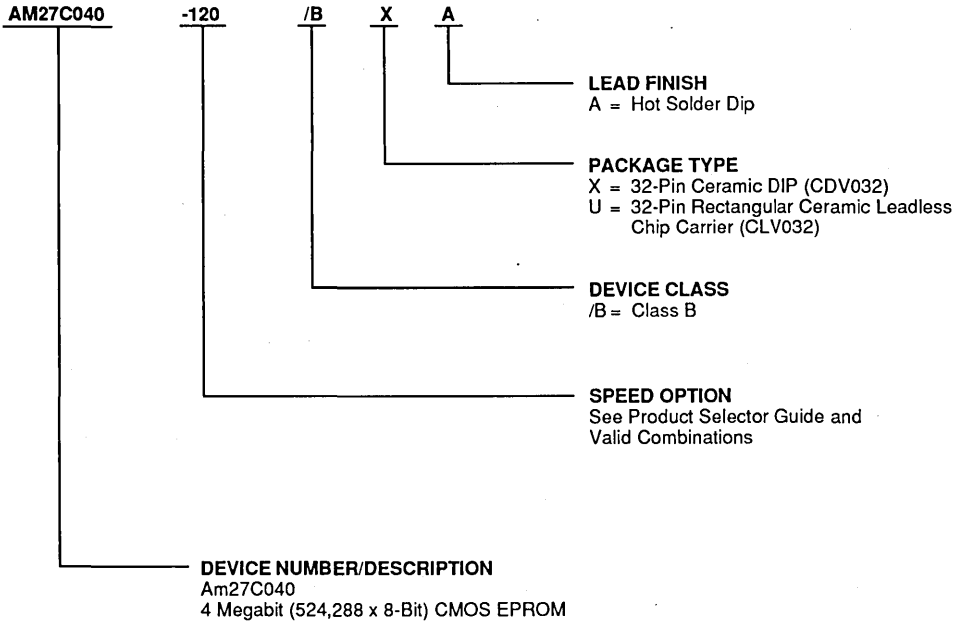
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C040-120	/BXA, /BUA
AM27C040-150	
AM27C040-200	
AM27C040-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C040

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C040 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C040. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Å — with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C040 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C040, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C040 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C040

Upon delivery, or after each erasure, the Am27C040 has all 4,194,304 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C040 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}/\overline{PGM}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulse and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C040. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C040s in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$, all like inputs of the parallel Am27C040 may be common. A TTL low-level program pulse applied to an Am27C040 $\overline{CE}/\overline{PGM}$ input with V_{PP} = 12.75 V ± 0.25 V, and $\overline{OE}$ HIGH will program that Am27C040. A high-level $\overline{CE}/\overline{PGM}$ input inhibits the other Am27C040s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}/\overline{PGM}$ at V_{IL}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C040.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C040. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and Byte 1 (A0 = V_{IH}), the device identifier code. For the Am27C040, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C040 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}/\overline{PGM}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}/\overline{PGM}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C040 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}/\overline{PGM}$ is at $V_{CC} \pm 0.3$ V. The Am27C040 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}/\overline{PGM}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state; independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}/\overline{PGM}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the outut pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	9BH

Notes:

1. *V_H = 12.0 V± 0.5 V*
2. *X can be either V_{IL} or V_{IH}*
3. *A1–A8 = A10–A18 = V_{IL}*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:
OTP Products ..... −65°C to +125°C
All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}:
All pins except A9, V_{PP}, and
V_{CC} (Note 1) ..... −0.6 V to V_{CC} + 0.6 V

A9 and V_{PP} (Note 2) ..... −0.6 V to 13.5 V

V_{CC} ..... −0.6 V to 7.0 V

Notes:

1. *During transitions, the input may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.*
2. *During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices

Case Temperature (Tc) ..... −40°C to +85°C

Extended Commercial (E) Devices

Case Temperature (Tc) ..... −55°C to +125°C

Military (M) Devices

Case Temperature (Tc) ..... −55°C to +125°C

Supply Read Voltages:

V_{CC} for Am27C040-XX5 ..... +4.75 V to +5.25 V
V_{CC} for Am27C040-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL products, Group A, Subgroups 1, 2, 3, 6 and 7 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5.0	µA
			E/M Devices		10.0	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA	C/I Devices		40	mA
			E/M Devices		60	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C040 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

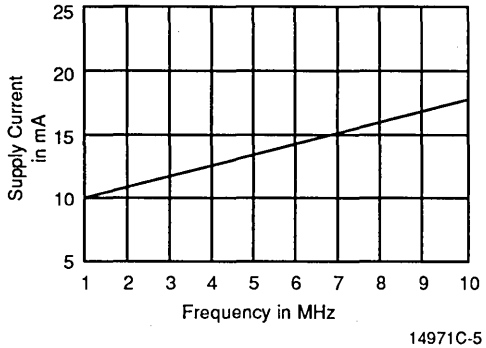


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.0 V, T = 25°C

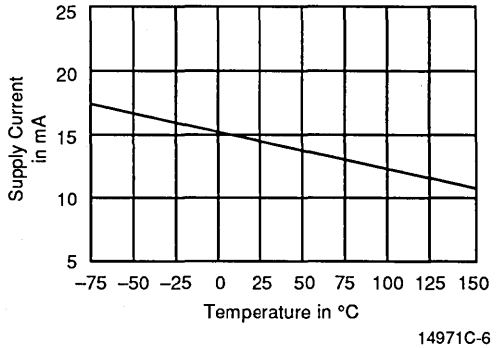


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		PD 032		PL 032		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	12	15	9	12	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

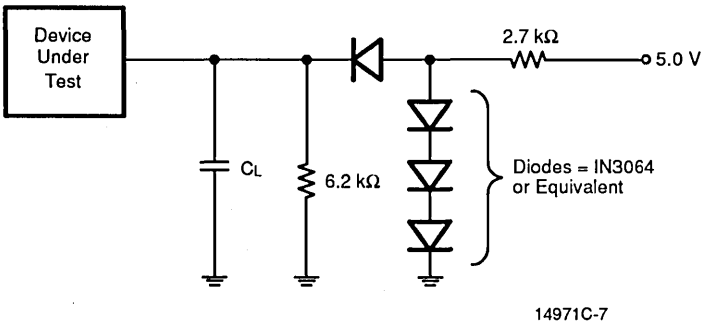
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C040					Unit
JEDEC	Standard				-105 -100	-125 -120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min						ns
				Max	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min						ns
				Max	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min						ns
				Max	40	50	55	60	60	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	ns
				Max	30	30	30	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	ns
				Max						

Notes:

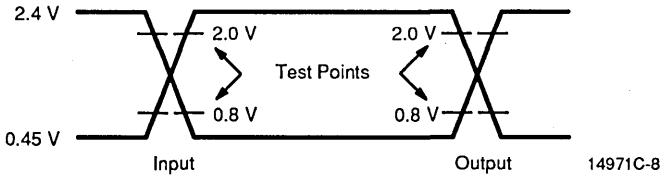
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C040 must not be removed from, or inserted into a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF,*
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.45 V to 2.4 V,
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V,
   Outputs: 0.8 V and 2 V

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0." Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

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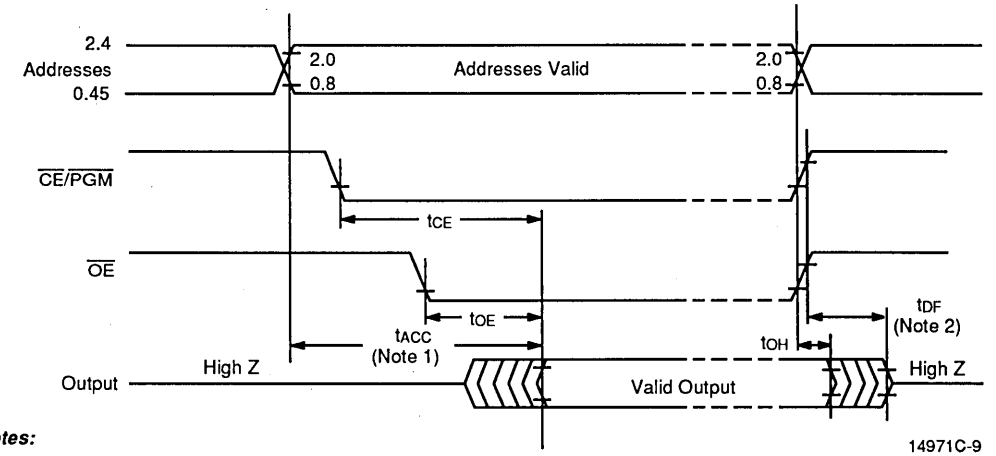
SWITCHING WAVEFORM



14971C-9

Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27C400

4 Megabit (524,288 x 8-Bit/262,144 x 16-Bit) ROM Compatible CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 100 ns
- **Low power consumption**
  - — 100 µA maximum CMOS standby current
- **Industry standard pinout:**
  - — ROM compatible
  - — 44-pin LCC, and PLCC packages provide easy upgrade to 8 Mbits, DIP upgrades require a 40- to 42-pin conversion
- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - — Typical programming time of 32 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**

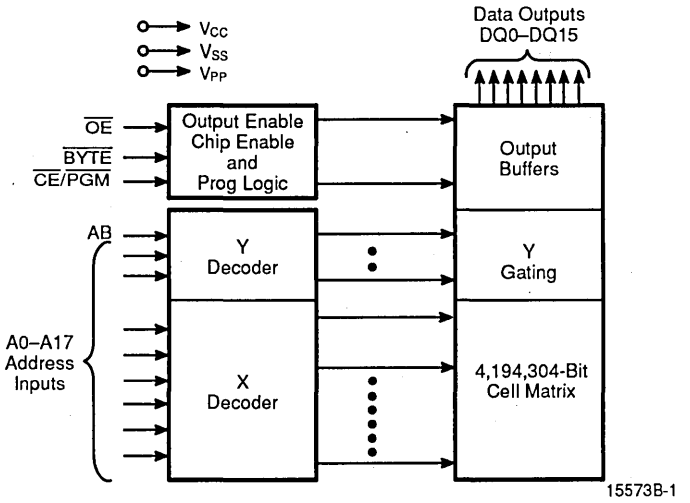
GENERAL DESCRIPTION

The Am27C400 is a 4 Mbit ultraviolet erasable programmable read-only memory that is functionally and pinout compatible with 4 Mbit masked ROMs. Under control of the $\overline{BYTE}$ input, the memory can be configured as either a 512K by 8-bit memory or a 256K by 16-bit memory. It operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic packages as well as plastic one time programmable (OTP) packages for both through hole and surface mount applications.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C400 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 150 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C400 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming times of 32 seconds.



15573B-1

Publication# 15573 Rev. B Amendment/0
Issue Date: July 1993

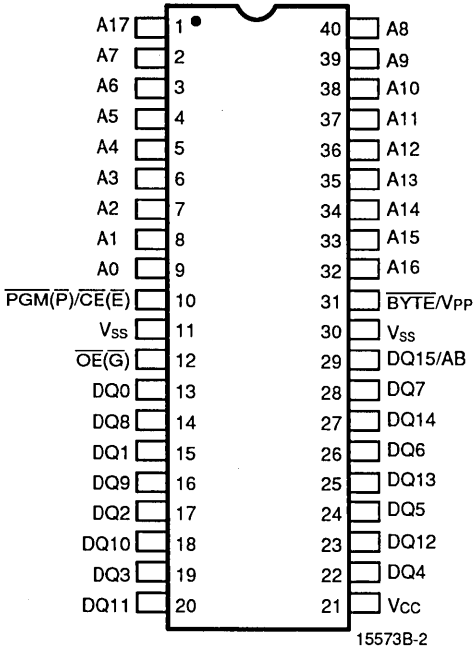
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C400				
Ordering Part No:					
V_{CC} ± 5%	-105	-125			-255
V_{CC} ± 10%	-100	-120	-150	-200	-250
Max Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	50	50	65	75	100

CONNECTION DIAGRAM

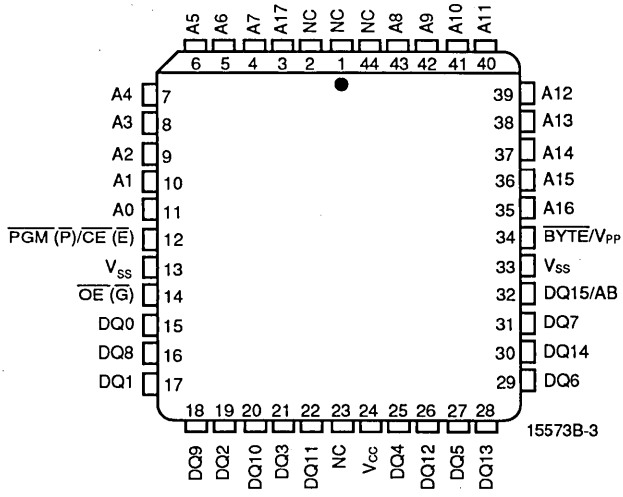
Top View

DIP



15573B-2

PLCC/LCC



15573B-3

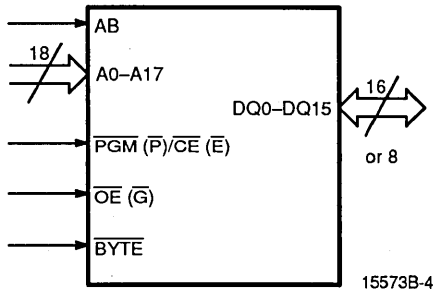
Notes:

1. *Inner ring of numbers correspond to the package pins*
2. *JEDEC nomenclature is in parenthesis*

PIN DESIGNATIONS

AB	=	Address Input ($\overline{BYTE}$ Mode)
A0–A17	=	Address Inputs
$\overline{BYTE}$	=	Byte/Word Switch
$\overline{CE}$ ($\overline{E}$)/$\overline{PGM}$ ($\overline{P}$)	=	Chip Enable and Program Enable Inputs
DQ0–DQ15	=	Data Inputs/Outputs
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

LOGIC SYMBOL

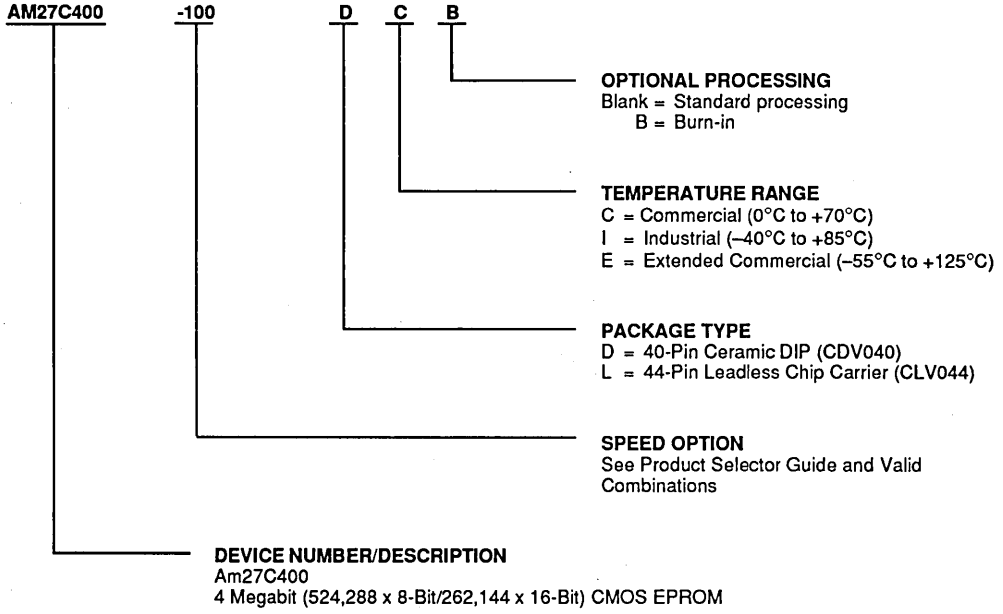


15573B-4

ORDERING INFORMATION

EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C400-100	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C400-105	
AM27C400-120	DC, DCB, DI, DIB, LC, LCB, LI, LIB DE, DEB, LE, LEB
AM27C400-125	
AM27C400-150	
AM27C400-200	
AM27C400-255	

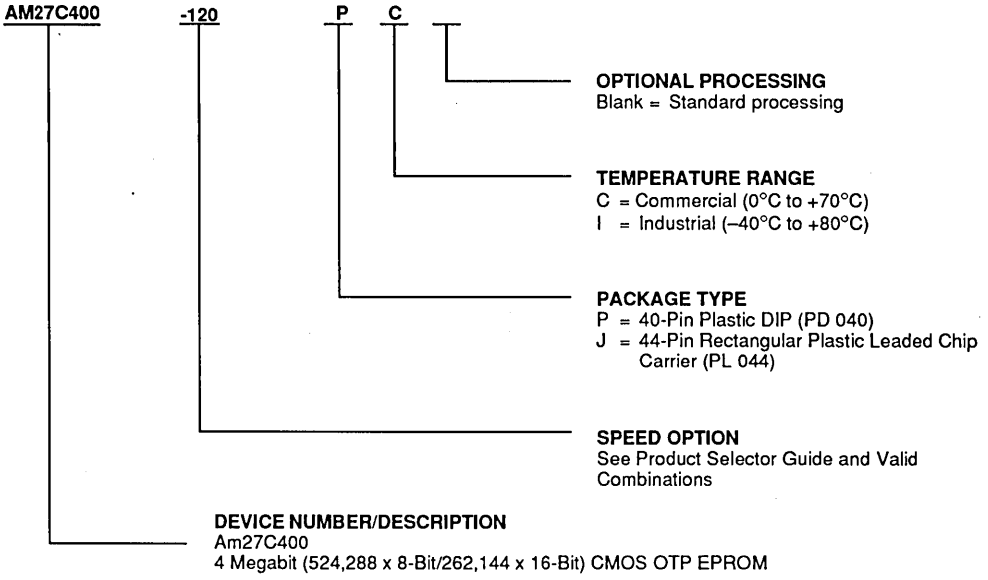
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C400-120	PC, JC, PI, JI
AM27C400-125	
AM27C400-150	
AM27C400-200	
AM27C400-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

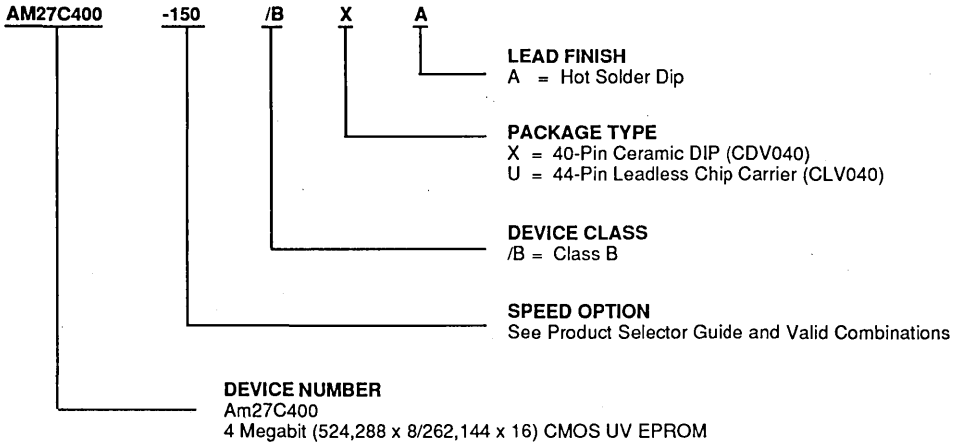
Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C400-120	/BUA, /BXA
AM27C400-150	
AM27C400-200	
AM27C400-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C400

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C400 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C400. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2,537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C400 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C400 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2,537Å, exposure to fluorescent light and sunlight will eventually erase the Am27C400 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C400

Upon delivery or after each erasure the Am27C400 has all 4,194,304 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C400 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}/\overline{PGM}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 16 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each addresss only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C400. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6.0 for programming and flow chart characteristics.

Program Inhibit

Programming of multiple Am27C400s in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$, all like inputs of the parallel Am27C400 may be common. A TTL low-level program pulse applied to an Am27C400 $\overline{CE}/\overline{PGM}$ input with V_{PP} = 12.75 V ± 0.25 V, and $\overline{OE}$ HIGH will program that Am27C400. A high-level $\overline{CE}/\overline{PGM}$ input inhibits the other Am27C400 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}/\overline{PGM}$ at V_{IH} and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C400.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C400. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and Byte 1 (A0 = V_{IH}), the device identifier code. For the Am27C400, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C400 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}/\overline{PGM}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}/\overline{PGM}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Byte Mode

The user has the option of reading data in either 16-bit words or 8-bit bytes under control of the $\overline{BYTE}$ input. With the $\overline{BYTE}$ input HIGH, inputs A0–A17 will address 256K words of 16-bit data. When the $\overline{BYTE}$ input is LOW, AB functions as the least significant address input and 512K bytes of data can be accessed. The 8 bits of data will appear on DQ0–DQ7.

Standby Mode

The Am27C400 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}/\overline{PGM}$ is at $V_{CC} \pm 0.3$ V. The Am27C400 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}/\overline{PGM}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}/\overline{PGM}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	9DH

Notes:

1. $V_H = 12.0 V \pm 0.5 V$
2. X = Either V_{IH} or V_{IL}
3. $A1–A8 = A0–A17 = V_{IL}$

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect To V_{SS}
- All pins except A9, V_{PP}, V_{CC} . −0.6 V to Vcc + 0.6 V
- A9 and V_{PP} ..... −0.6 V to +13.5 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:
1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C400-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27C400-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2, 3 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 6 and 7 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}			5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA	C/I Devices		40	mA
			E/M Devices		60	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C400 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$/V_{PP} = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

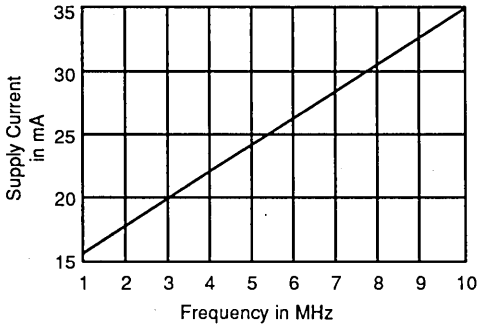


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

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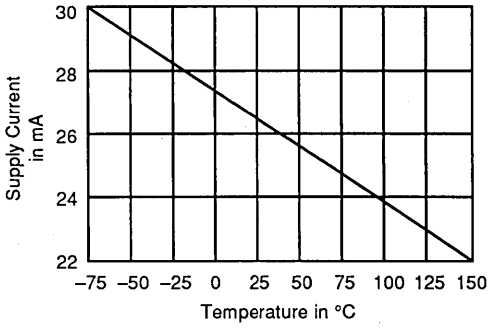

Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

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CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV040		CLV044		PD 040		PL 044		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	9	12	9	11	6	8	9	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	15	13	15	9	11	13	15	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

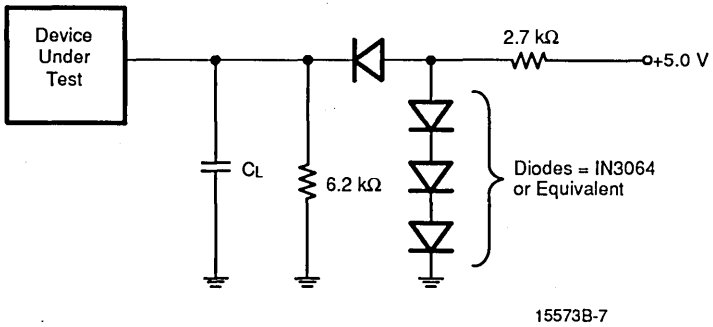
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C400					Unit
JEDEC	Standard				-105 -100	-125 -120	-155 -150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	
				Max	100	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	
				Max	100	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	
				Max	50	50	55	60	75	ns
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	
				Max	30	30	30	40	60	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	
				Max	–	–	–	–	–	ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C400 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs.

SWITCHING TEST CIRCUIT



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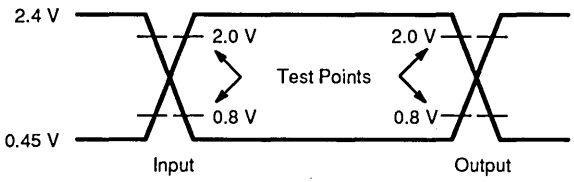
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



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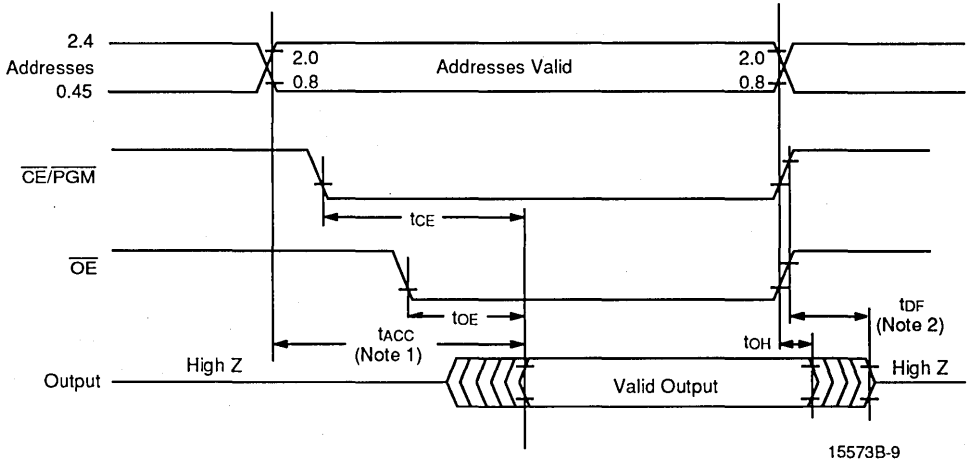
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 for a logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



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Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27C4096

4 Megabit (262,144 x 16-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 100 ns
- **Low power consumption**
  - — 100 µA maximum CMOS standby current
- **JEDEC-approved pinout**
  - — Plug in upgrade of 1 Mbit and 2 Mbit EPROMs
  - — 40-pin DIP/PDIP
  - — 44-pin LCC/PLCC
- **Single + 5 V power supply**
- **± 10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - — Typical programming time of 32 seconds
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **High noise immunity**

GENERAL DESCRIPTION

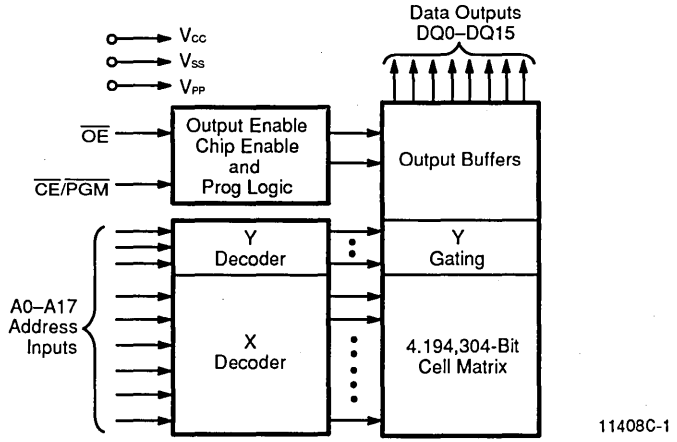
The Am27C4096 is a 4 Mbit ultraviolet erasable programmable read-only memory. It is organized as 256K words by 16 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. The Am27C4096 is ideal for use in 16-bit microprocessor systems. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C4096 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMDs CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 125 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C4096 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming times of 32 seconds.

BLOCK DIAGRAM



11408C-1

Publication# 11408 Rev. C Amendment/0
Issue Date: July 1993

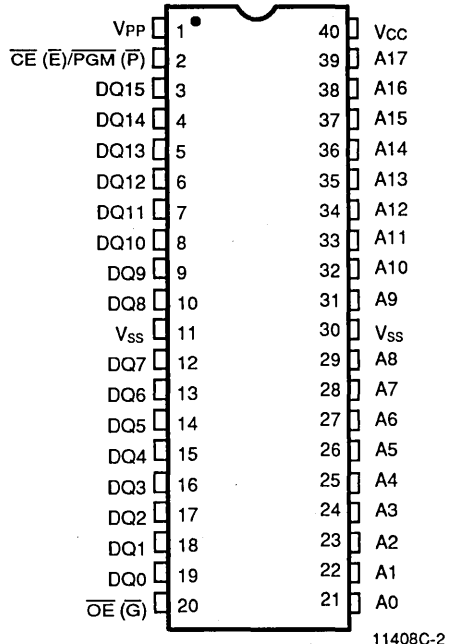
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C4096				
Ordering Part No:					
$V_{CC} \pm 5\%$	-105	-125			-255
$V_{CC} \pm 10\%$	-100	-120	-150	-200	-250
Max Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	50	50	65	75	100

CONNECTION DIAGRAMS

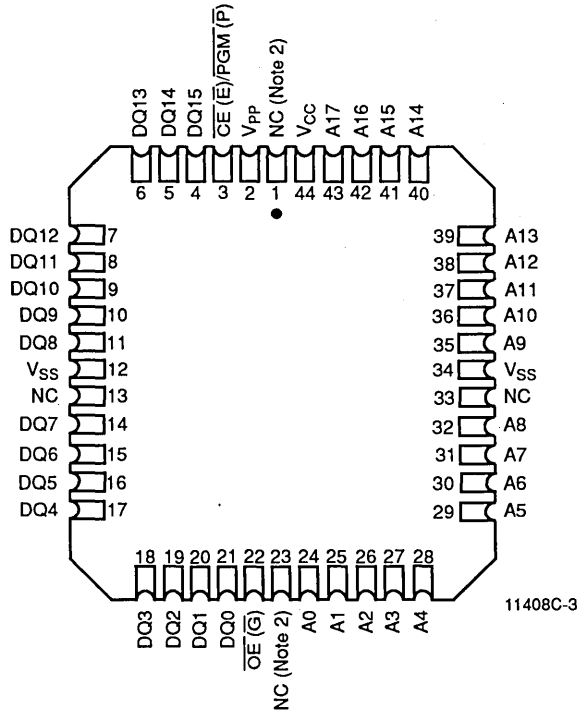
Top View

DIP



11408C-2

PLCC/LCC



11408C-3

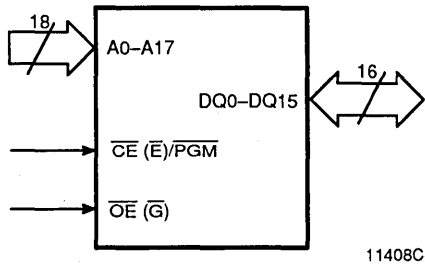
Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *Don't use (DU) for PLCC.*

PIN DESIGNATIONS

A0–A17	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)/$\overline{PGM}$ ($\overline{P}$)	=	Chip Enable Input
DQ0–DQ15	=	Data Input/Outputs
DU	=	No External Connection
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

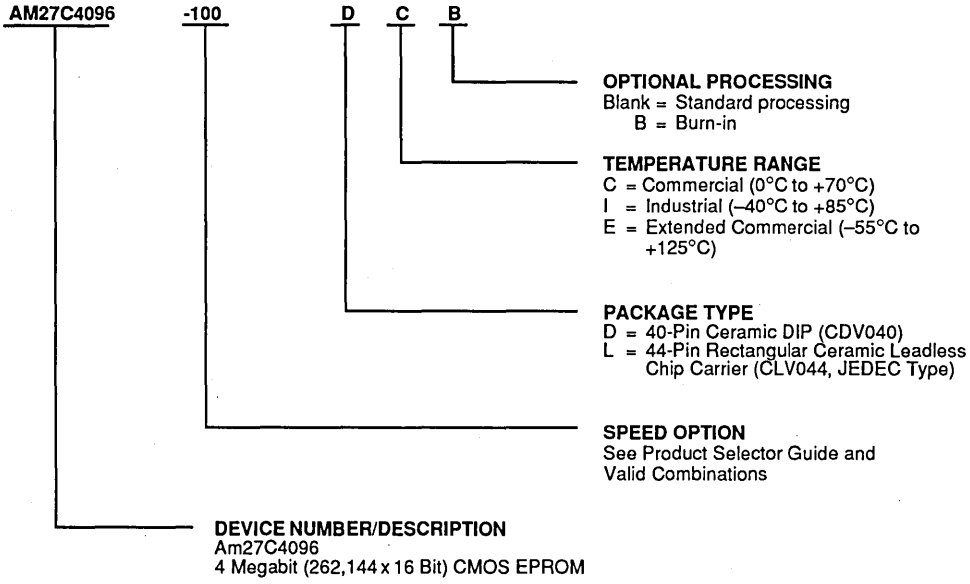
LOGIC SYMBOL



11408C-4

ORDERING INFORMATION
EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



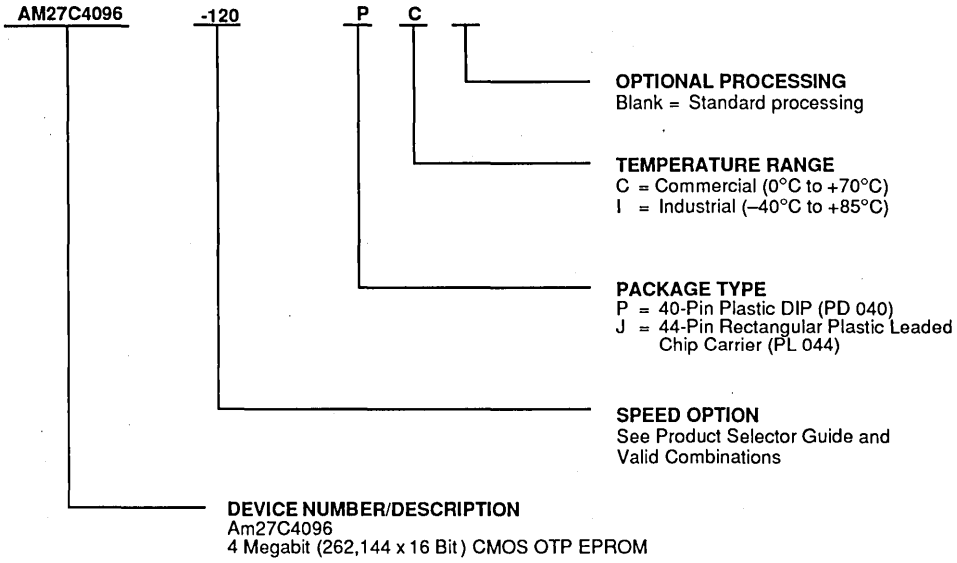
Valid Combinations	
AM27C4096-100	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C4096-105	
AM27C4096-120	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C4096-125	
AM27C4096-150	
AM27C4096-200	
AM27C4096-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C4096-120	PC, JC, PI, JI
AM27C4096-125	
AM27C4096-150	
AM27C4096-200	
AM27C4096-255	

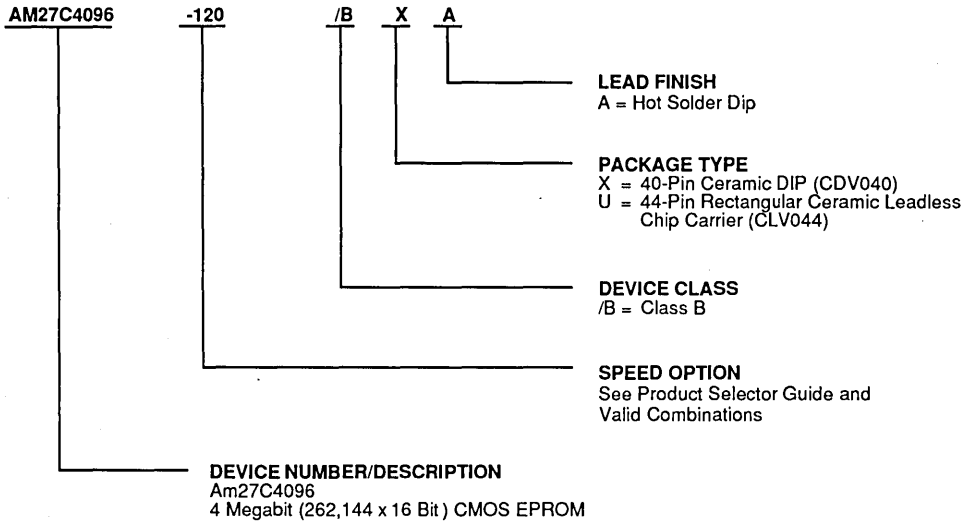
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C4096-120	/BXA, /BUA
AM27C4096-150	
AM27C4096-200	
AM27C4096-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing The Am27C4096

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C4096 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C4096. This dosage can be obtained by exposure to an ultraviolet lamp —wavelength of 2537 Å–with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C4096 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C4096 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C4096 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C4096

Upon delivery or after each erasure the Am27C4096 has all 4,194,304 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C4096 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}/\overline{PGM}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 16 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C4096. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6 for programming flow chart and characteristics

Program Inhibit

Programming of multiple Am27C4096 in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$, all like inputs of the parallel Am27C4096 may be common. A TTL low-level program pulse applied to an Am27C4096 $\overline{CE}/\overline{PGM}$ input with V_{PP} = 12.75 V ± 0.25 V and $\overline{OE}$ HIGH will program that Am27C4096. A high-level $\overline{CE}/\overline{PGM}$ input inhibits the other Am27C4096 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}/\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C4096.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C4096. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1(A0 = V_{IH}), the device identifier code. For the Am27C4096, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C4096 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}/\overline{PGM}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}/\overline{PGM}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C4096 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}/\overline{PGM}$ is at V_{CC} ± 0.3 V. The Am27C4096 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}/\overline{PGM}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}/\overline{PGM}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1–µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7–µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	Hi–Z
Standby (TTL)		V_{IH}	X	X	X	X	Hi–Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	Hi–Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi–Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	19H

Notes:

1. *X = Either V_{IH} or V_{IL}*
2. *V_H = 12.0 V ± 0.5 V*
3. *A1–A8 = A10–A17 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:
OTP Products ..... −65°C to +125°C
All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}:

All pins except A9, V_{PP},
and V_{CC} (Note 1) ..... −0.6 V to V_{CC} + 0.6 V

A9 and V_{PP} (Note 2) ..... −0.6 V to 13.5 V

V_{CC} ..... −0.6 V to 7.0 V

Notes:

1. *During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.*
2. *During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (Tc) ..... −40°C to +85°C

Extended Commercial (E) Devices
Case Temperature (Tc) ..... −55°C to +125°C

Military (M) Devices
Case Temperature (Tc) ..... −55°C to +125°C

Supply Read Voltages:
V_{CC} for Am27C4096-XX5 ..... +4.75 V to +5.25 V
V_{CC} for Am27C4096-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 6, and 7 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = 400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +0.5	V
V_{IL}	Input LOW Voltage			−0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1.0	µA
I_{LO}	Output Leakage Current				5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz OUT = 0 mA	C/I Devices		50	µA
			E/M Devices		60	
I_{CC2}	V_{CC} TTL Standby	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *Caution: The Am27C4096 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V during transitions, the inputs may overshoot −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods less than 20 ns.*

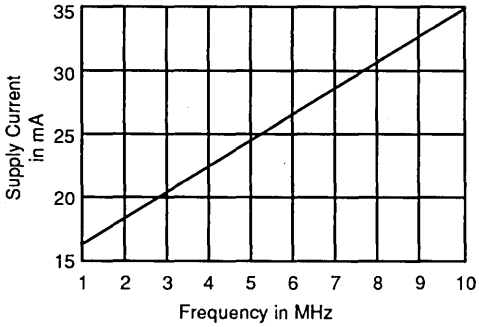


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

15573B-5

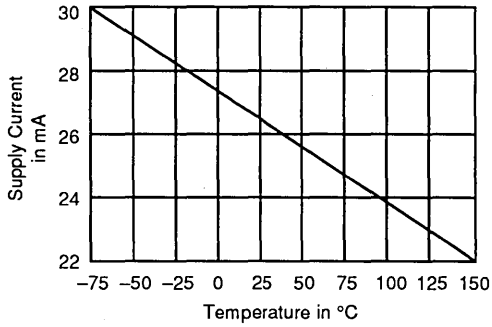


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

15573B-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV040		CLV044		PD040		PL044		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	13	10	13	6	8	10	13	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	10	13	13	15	8	10	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *TA = +25°C, f = 1 MHz*

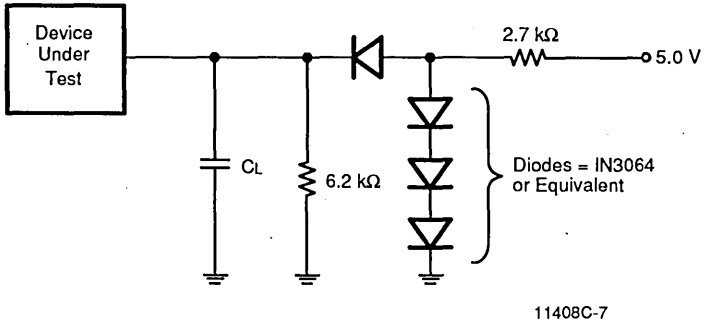
Switching CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

Parameter Symbols				Am27C4096						
JEDEC	Standard	Parameter Description	Test Conditions		-105, -100	-125, -120	-150	-200	-255, -250	Unit
A_{VQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	ns
				Max	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	ns
				Max	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	ns
				Max	50	50	55	60	60	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	ns
				Max	30	40	40	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, CE, or OE, whichever ocurred first		Min	0	0	0	0	0	ns
				Max	–	–	–	–	–	

Notes:

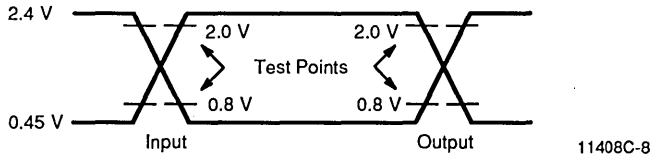
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C4096 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level — Inputs: 0.8 V to 2.0 V
   Outputs: 0.8 V to 2.0 V

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



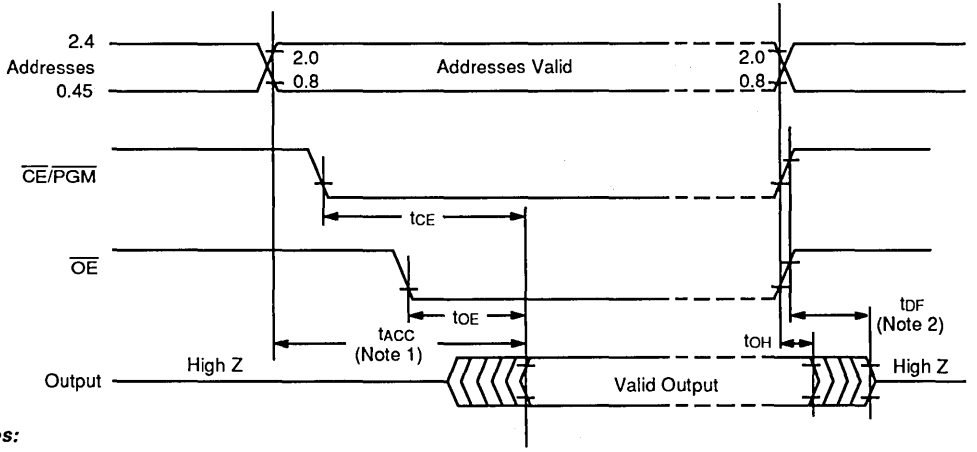
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORM



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

11408C-9

PRELIMINARY

Am27C080

8 Megabit (1,048,576 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 100 ns
- **Low power consumption**
  - — 100 µA maximum CMOS standby current
- **JEDEC-approved pinout**
  - — Plug in upgrade of 1-, 2-, 4-Mbit EPROMs
  - — Easy upgrade from 28-pin JEDEC EPROMs
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite™ programming**
  - — Typical programming time of less than 2 minutes
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Compact 32-pin DIP, PDIP, and PLCC packages**

GENERAL DESCRIPTION

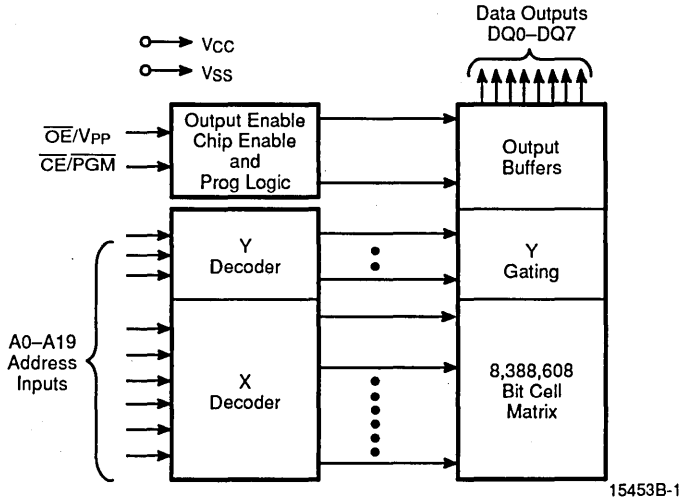
The Am27C080 is an 8 Mbit ultraviolet erasable programmable read-only memory. It is organized as 1,048K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C080 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C080 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming times of less than 2 minutes.

BLOCK DIAGRAM



15453B-1

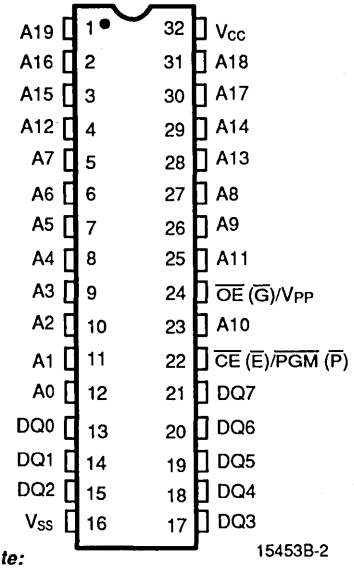
Publication# 15453 Rev. B Amendment/0
Issue Date: July 1993

PRODUCT SELECTOR GUIDE

Family Part No.	Am27C080				
Ordering Part No: $V_{CC} \pm 5\%$	-105				-255
$V_{CC} \pm 10\%$	-100	-120	-150	-200	-250
Max Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	50	50	65	75	100

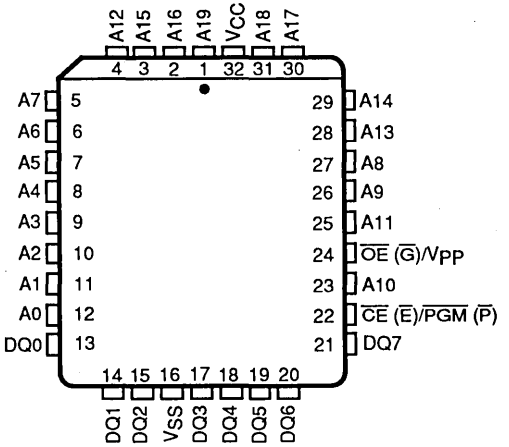
CONNECTION DIAGRAMS
Top View

DIP



15453B-2

PLCC



15453B-3

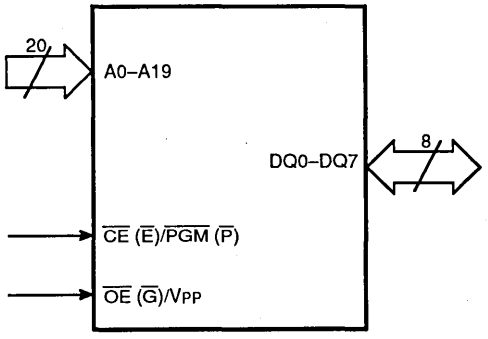
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A19 = Address Inputs
$\overline{CE}$ ($\overline{E}$)/$\overline{PGM}$ ($\overline{P}$) = Chip Enable
DQ0–DQ7 = Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)/V_{PP} = Output Enable Input/ Program Supply Voltage
V_{CC} = V_{CC} Supply Voltage
V_{SS} = Ground

LOGIC SYMBOL

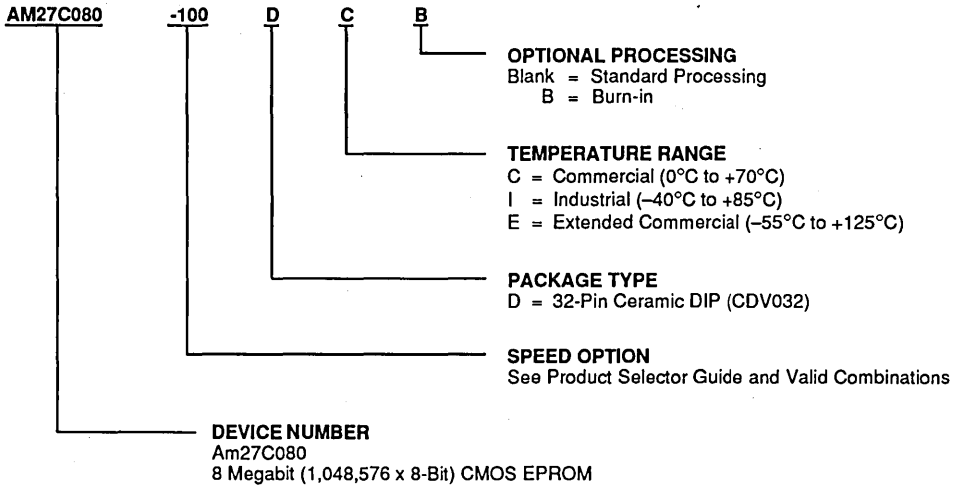


15453B-4

ORDERING INFORMATION

EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C080-100	DC, DI
AM27C080-105	
AM27C080-120	DC, DCB, DI, DIB
AM27C080-150	DC, DCB, DI, DIB, DE, DEB
AM27C080-200	
AM27C080-255	

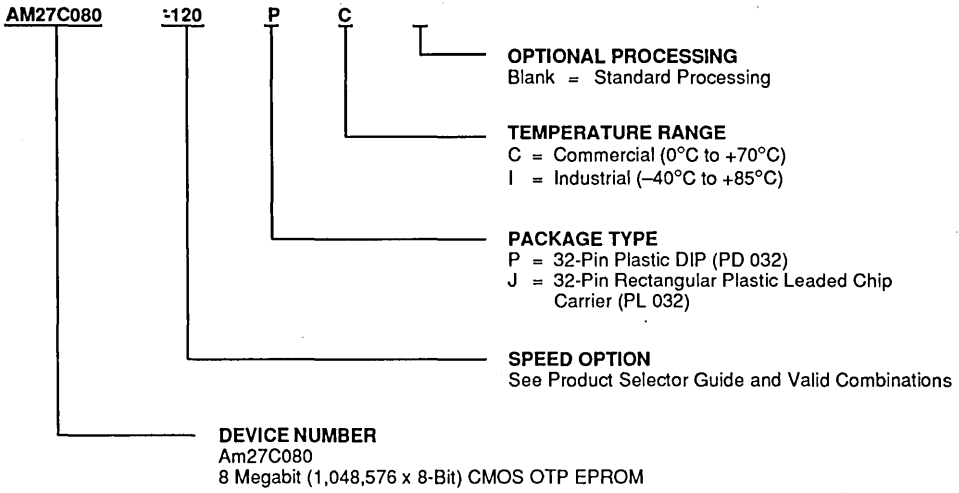
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C080-120	PC, JC, PI, JI
AM27C080-125	
AM27C080-150	
AM27C080-200	
AM27C080-255	

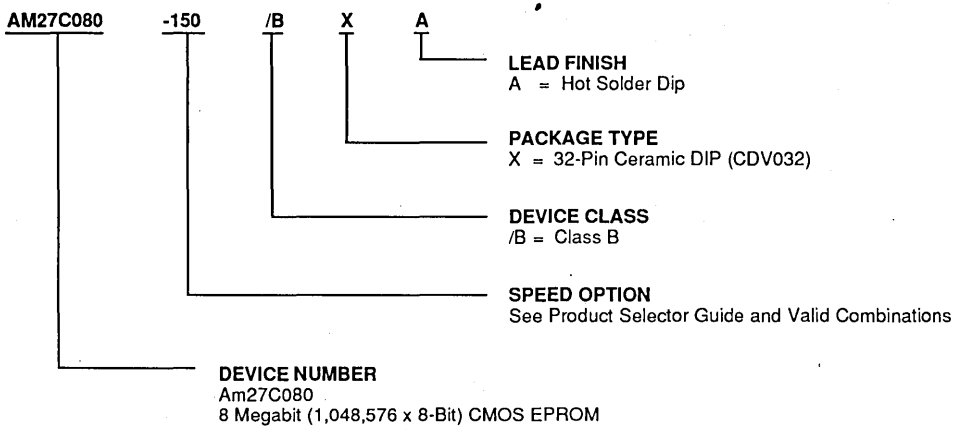
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C080-150	/BXA
AM27C080-200	
AM27C080-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C080

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C080 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C080. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C080 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C080 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C080 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C080

Upon delivery or after each erasure the Am27C080 has all 8,388,608 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C080 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the $\overline{OE}/V_{PP}$ and $\overline{CE}/\overline{PGM}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C080. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6.0 for programming flow charts and characteristics.

Program Inhibit

Programming of multiple Am27C080 in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$, all like inputs of the parallel Am27C080 may be common. A TTL low-level program pulse applied to an Am27C080 $\overline{CE}/\overline{PGM}$ input and $\overline{OE}/V_{PP}$ = 12.75 V ± 0.25 V, will program that Am27C080. A high-level $\overline{CE}/\overline{PGM}$ input inhibits the other Am27C080 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{CE}/\overline{PGM}$ at V_{IL} and $\overline{OE}/V_{PP}$ at V_{IL}.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C080.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V open address the A9 of the Am27C080. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device code. For the Am27C080, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C080 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}/\overline{PGM}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}/\overline{PGM}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C080 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}/\overline{PGM}$ is at V_{CC} ± 0.3 V. The Am27C080 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}/\overline{PGM}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}/V_{PP}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus connection will not occur

It is recommended that $\overline{CE}/\overline{PGM}$ be decoded and used as the primary device-selecting function, while $\overline{OE}/V_{PP}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}/\overline{PGM}$	$\overline{OE}/V_{PP}$	A0	A9	Outputs
Read		V_{IL}	V_{IL}	A0	A9	D_{OUT}
Output Disable		X	V_{IH}	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	Hi-Z
Standby (CMOS)		V_{CC} + 0.3 V	X	X	X	Hi-Z
Program		V_{IL}	V_{PP}	A0	A9	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	D_{OUT}
Program Inhibit		V_{IH}	V_{PP}	X	X	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	1CH

Notes:

1. *V_{IH} = 12.0 ± 0.5 V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A10–A19 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Voltage with Respect To V_{SS}
- All pins except A9, V_{PP}, V_{CC} ..... −0.6 V to V_{CC} + 0.6 V
- A9 and V_{PP} ..... −0.6 V to +13.5 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C080-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27C080-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 6 and 7 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}			5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA	C/I Devices		40	µA
			E/M Devices		50	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C080 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$/V_{PP} = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

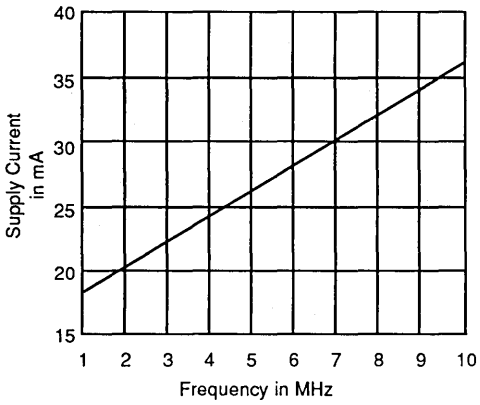


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

15453B-5

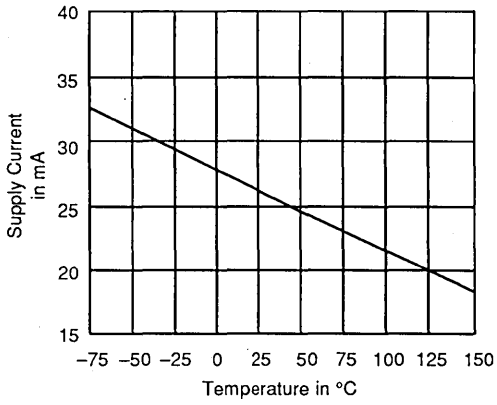


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

15453B-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV032		PL 032		PD 032		Unit
			Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	7	12	7	12	7	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	16	12	16	12	16	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz*

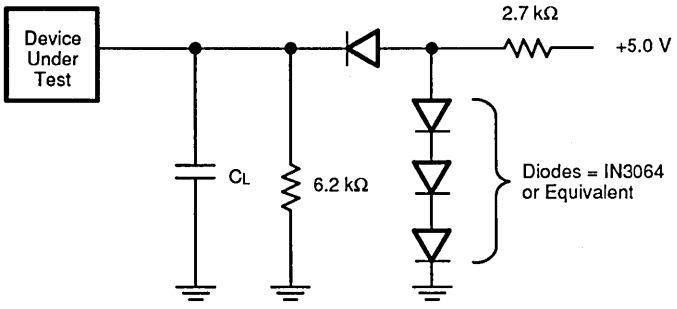
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9,10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C080					Unit
JEDEC	Standard				-105 -100	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	
				Max	100	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	
				Max	100	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	
				Max	50	50	55	60	60	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	
				Max	40	40	40	40	60	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	
				Max	–	–	–	–	–	ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C080 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V inputs and outputs

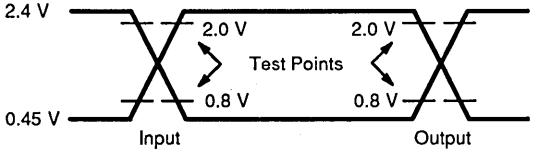
SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

15453B-7

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.

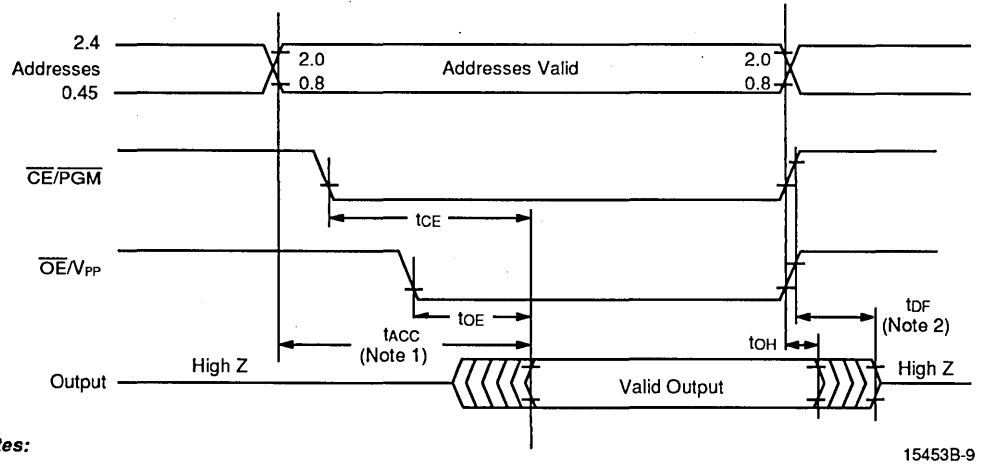
15453B-8

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS



15453B-9

Notes:

1. *$\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{OE} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

PRELIMINARY

Am27C800

8 Megabit (1,048,576 x 8-Bit/524,288 x 16-Bit) ROM Compatible CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 120 ns
- **Low power consumption**
  - — 100 µA maximum CMOS standby current
- **Industry standard pinout:**
  - — ROM compatible
  - — 42-pin DIP, PDIP and 44-pin LCC and PLCC packages provide easy upgrade to 16 Mbits
- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - — Typical programming time of less than 1 minute
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**

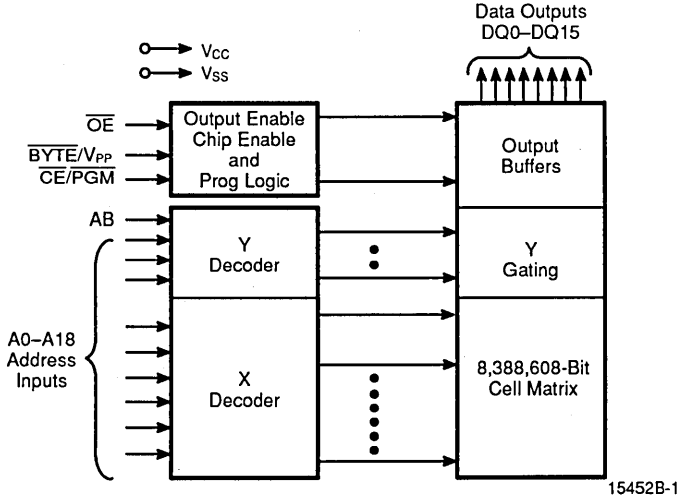
GENERAL DESCRIPTION

The Am27C800 is an 8 Mbit ultraviolet erasable programmable read-only memory that is functionally and pinout compatible with 8 Mbit masked ROMs. Under control of the $\overline{BYTE}$ input, the memory can be configured as either a 1 Mbit by 8-bit memory or a 512K by 16-bit memory. It operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic packages as well as plastic one time programmable (OTP) packages.

Typically, any byte can be accessed in less than 120 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C800 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 150 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C800 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming times of less than 1 minute.



Publication# 15452 Rev. B Amendment /0
Issue Date: July 1993

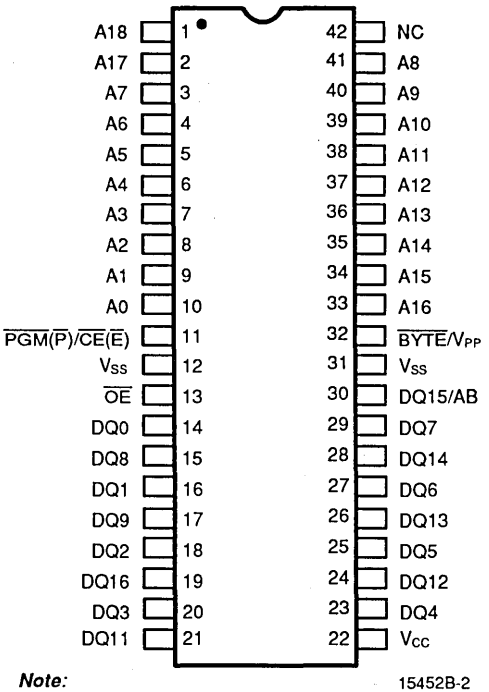
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C800			
Ordering Part No: V_{CC} ±5%	-125			-255
V_{CC} ±10%	-120	-150	-200	-250
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	50	65	75	100

CONNECTION DIAGRAM

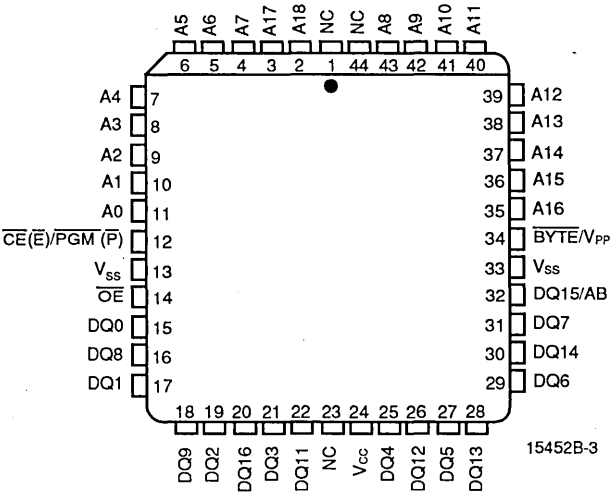
Top View

DIP



15452B-2

PLCC/LCC



15452B-3

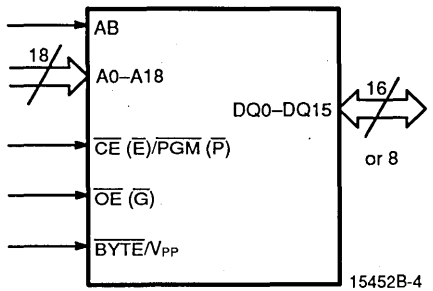
Note:

1. JEDEC nomenclature is in parenthesis.

PIN DESIGNATIONS

AB	=	Address Input ($\overline{BYTE}$ Mode)
A0–A18	=	Address Inputs
$\overline{BYTE}/V_{PP}$	=	Byte/Word Switch or Program Supply Voltage
$\overline{CE}$ ($\overline{E}$)/$\overline{PGM}$ ($\overline{P}$)	=	Chip Enable
DQ0–DQ15	=	Data Inputs/Outputs
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{SS}	=	Ground

LOGIC SYMBOL

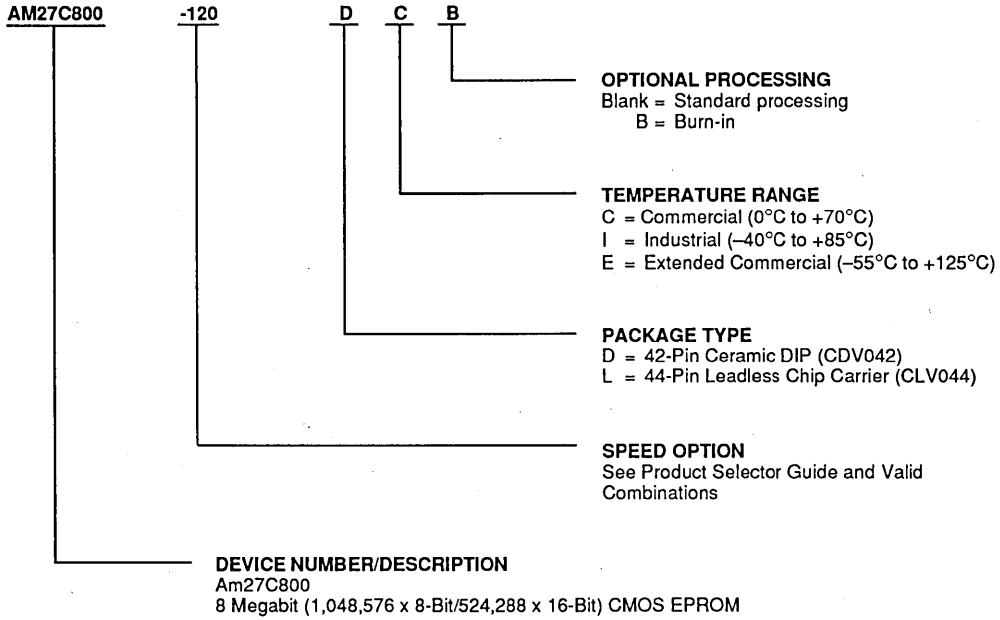


15452B-4

ORDERING INFORMATION

EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C800-120	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C800-125	
AM27C800-150	
AM27C800-200	
AM27C800-255	

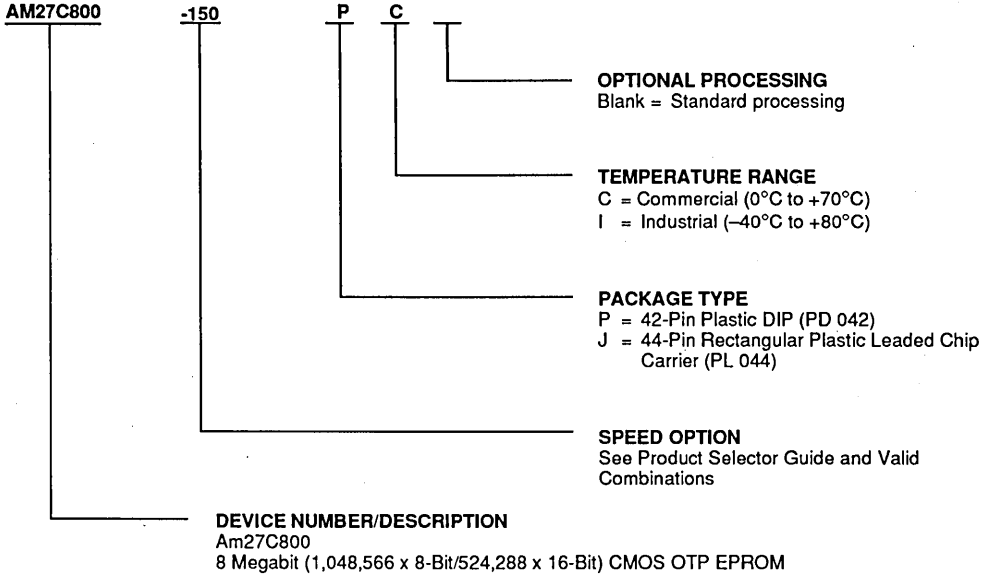
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C800-150	PC, JC, PI, JI
AM27C800-155	
AM27C800-200	
AM27C800-255	

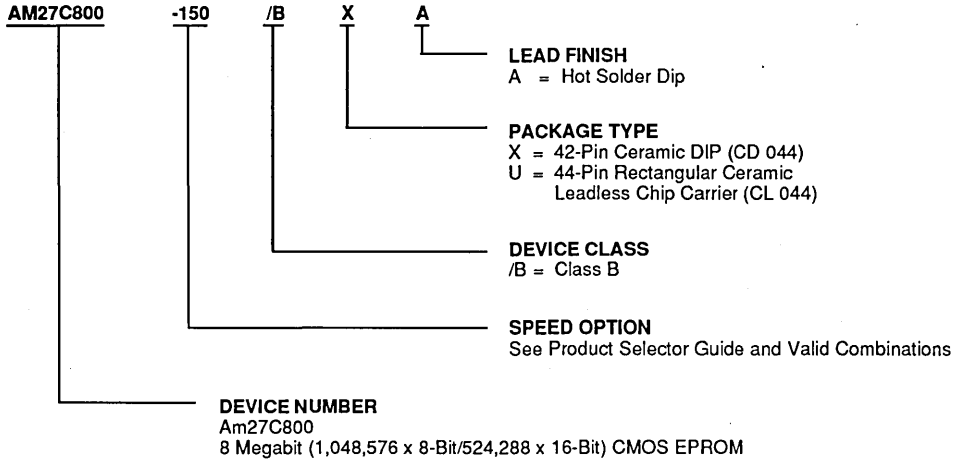
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C800-150	/BUA, /BXA
AM27C800-200	
AM27C800-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C800

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C800 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C800. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2,537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C800 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C800 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2,537Å, exposure to fluorescent light and sunlight will eventually erase the Am27C800 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C800

Upon delivery or after each erasure the Am27C800 has all 8,388,608 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C800 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}/\overline{PGM}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 16 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each addresss only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C800. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6.0 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C800s in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$, all like inputs of the parallel Am27C800 may be common. A TTL low-level program pulse applied to an Am27C800 $\overline{CE}/\overline{PGM}$ input with V_{PP} = 12.75 V ± 0.25 V, and $\overline{OE}$ HIGH will program that Am27C800. A high-level $\overline{CE}/\overline{PGM}$ input inhibits the other Am27C800 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}/\overline{PGM}$ at V_{IH} and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C800.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C800. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and Byte 1 (A0 = V_{IH}), the device identifier code. For the Am27C800, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C800 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}/\overline{PGM}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}/\overline{PGM}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Byte Mode

The user has the option of reading data in either 16-bit words or 8-bit bytes under control of the $\overline{BYTE}$ input. With the $\overline{BYTE}$ input HIGH, inputs A18–A0 will address 512K words of 16-bit data. When the $\overline{BYTE}$ input is LOW, AB functions as the least significant address input and 1 Mbyte of data can be accessed. The 8 bits of data will appear on DQ7–DQ0.

Standby Mode

The Am27C800 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}/\overline{PGM}$ is at $V_{CC} \pm 0.3$ V. The Am27C800 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}/\overline{PGM}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}/\overline{PGM}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A0	A9	$\overline{BYTE}/V_{PP}$	Outputs
Read		V_{IL}	V_{IL}	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	1AH

Notes:

1. *V_H = 12.0 V ± 0.5 V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A10–A18 = V_{IL}, AB = X*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect To V_{SS}
- All pins except A9, V_{PP}, V_{CC} (Note 1) ..... −0.6 V to V_{CC} + 0.6 V
- A9 and V_{PP} (Note 2) ..... −0.6 V to +13.5 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:
1. *During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.*
2. *During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C800-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27C800-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 6 and 7 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			−0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}			5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C800 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

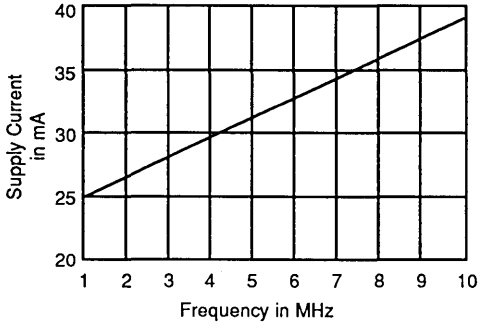


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

15452B-5

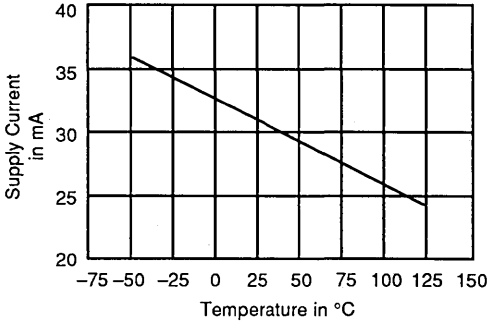


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

15452B-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV042		CLV044		PD 042		PL 044		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	10	18	10	18	10	18	10	18	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	10	18	10	18	10	18	10	18	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz*

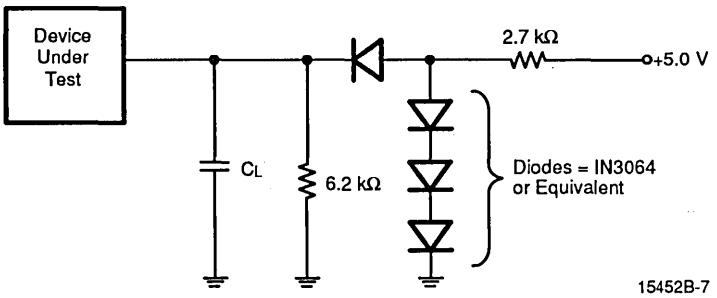
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

JEDEC	Standard	Parameter Description	Test Conditions		Am27C800 -125 -120	Am27C800 -150	Am27C800 -200	Am27C800 -255 -250	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	ns
				Max	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	ns
				Max	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	ns
				Max	50	55	60	60	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	ns
				Max	40	40	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	ns
				Max	–	–	–	–	

Notes:

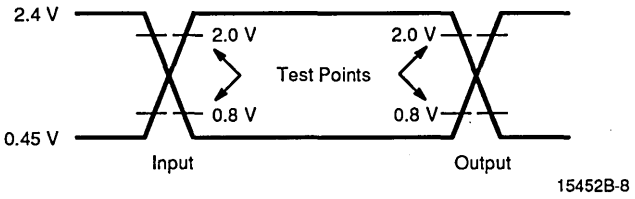
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C800 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V
   Outputs: 0.8 V and 2.0 V

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



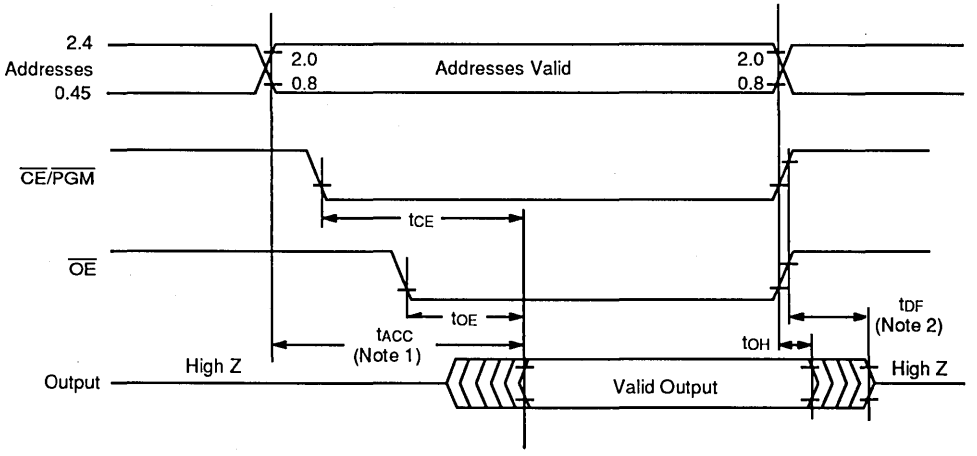
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 for a logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



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Notes:

1. *$\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

SECTION

3 HIGH-SPEED CMOS ERASABLE PROGRAMMABLE READ ONLY MEMORIES (EPROMs)

AN INTRODUCTION TO HIGH-SPEED EPROMs

Advanced Micro Devices has consistently improved the CMOS process to manufacture EPROMs in order to remain the technology leader in the marketplace. In addition to providing lower cost and higher density EPROM solutions, AMD's advanced CMOS process and superior design techniques create the highest performance devices in the industry. The devices that achieve high speed through process technology are identified by the "Am27C" nomenclature. This family provides the designer with a broad range of speeds and densities for most designs.

AMD has also introduced a family of CMOS EPROMs that have been specifically designed for speed. This "Am27H" family supports 35 ns and 45 ns access speeds at the 256K and 1 Mbit densities, respectively.

These high speed "commodity" and high performance "27H" series of EPROMs allow system designers to maximize microprocessor efficiency by matching clock speed with access time. This performance edge also benefits digital signal processor (DSP) and other designers by doing away with the need for expensive shadow RAM or external glue logic in the case of bank interleaving.

HIGH SPEED EPROMs AND MICROPROCESSORS

With the advent of the current generation of high speed microprocessors and their increasing use in embedded control systems it is becoming more and more important to match clock speed with memory access time. The impact of a slow memory can have a drastic effect on system performance. Until recently the designer's only choices have been to use PROMs or copy the contents of slow EPROMs into faster DRAMs or SRAMs. Both of these solutions are expensive in terms of both device cost and board area. Advanced Micro Devices manufactures a full line of high speed EPROMs that enable the designer to produce systems that allow microprocessors to achieve maximum performance.

The standard method of interfacing to slow EPROMs is by adding wait states to the memory access cycle. At first this may not seem to be a problem. However, with a typical memory cycle requiring 3 CPU cycles, each additional cycle is a 30% reduction in speed! This magnitude of performance degradation is not acceptable in the competitive market of today.

In general, the number of cycles available for "0 wait state" operation for popular microprocessors such as the Am386/286 are two cycles. Based on the above fact, the typical EPROM access time can be calculated using the following formula:

EPROM Access Time = Total Time Available –
(Address Ready Delay + Address Buffer Delay +
Data Buffer Delay + µproc Set-Up Time)

The table below lists CPU clock speed and the required EPROM access time for the given wait states.

Table 3-1

CPU Clock Frequency	Wait States	EPROM Access Time	Memory Access Cycle Time
40 MHz	1	45 ns	75 ns
33 MHz	0	30 ns	60 ns
33 MHz	1	60 ns	90 ns
33 MHz	2	90 ns	120 ns
25 MHz	0	45 ns	80 ns
25 MHz	1	85 ns	120 ns
25 MHz	2	120 ns	160 ns
20 MHz	0	60 ns	100 ns
20 MHz	1	100 ns	150 ns
20 MHz	2	150 ns	200 ns
16 MHz	0	75 ns	125 ns
16 MHz	1	120 ns	187 ns

It should be noted that by inserting just one wait state (see Memory Access Cycle Time above) the performance of the CPU is degraded to that of the slower clock speed with zero wait states. Considering the cost premium for the faster CPU, the simple insertion of a wait state can undermine the cost/performance ratio of the final system.

There have been two traditional engineering solutions to this problem:

- utilize a combination of slow EPROM and faster DRAM and/or SRAM, or
- utilize interleaving banks of memory

Both of the above solutions do work but at the expense of increasing cost to achieve the desired performance. The increased cost comes in the form of:

- duplication of memory components when pursuing a shadow memory implementation
- increase of real estate and decreased reliability due to higher component count

Advanced Micro Devices offers a better solution to eliminating wait states. High speed (35 ns – 120 ns) EPROMs are available, and designing a system using them is very easy. Don't add wait states! Most EPROM manufacturers have a formula listed in their design manuals that is used to calculate the EPROM access time required. They suggest that you vary the number of wait states in the formula until you hit on the access time of an EPROM that they manufacture. May we suggest that you use zero wait states in their formula and choose one of AMD's High Speed EPROMs.

BOARD LAYOUT METHODS FOR HIGH-SPEED EPROMs

Now that you have made the decision to get maximum performance from your microprocessor here are a few tips to make sure that your design goes to production smoothly. These tips are general system tips and are not unique to EPROMs. They can be used in any high-speed design.

As system speed increases so does the power supply noise, which can disrupt the system if left unchecked. There are some simple methods for reducing noise that can be used as guidelines when designing and laying out systems. The extent to which these tips are used in your design will depend on PC board size, total power supply capacity, length of feed lines from the power supply, presence of a ground plane in the PC board, clock speed, etc. There is no way to come up with an exact formula to minimize noise, so it is best to start with a standard setup and then modify it to fit the current design.

Rule of thumb 1:

- Place a 0.1 µF capacitor as close as possible to *every* IC between V_{CC} and GND.
- Place a 1.0 µF capacitor between V_{CC} and GND for every four ICs on a power trace.

Rule of thumb 2:

- Use power planes if you can.

This generally requires a multi-layer PC board that uses one or two of the internal layers to carry the power to each IC with very large traces. Don't forget to provide heat relief on the holes.

Figure 3-1 Typical Noise Isolation Between V_{CC} and GND

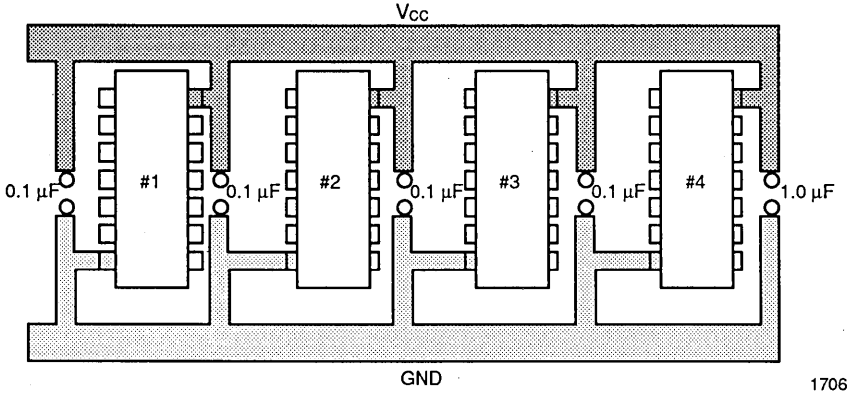
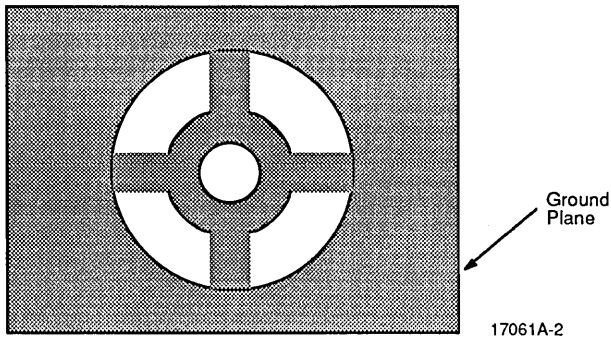


Figure 3-2 Typical Ground Plane Heat Relief Pattern



- If power planes cannot be used, then do not snake the trace.

Use a comb pattern to distribute the power to the ICs. Run heavy buses down the side of the board with smaller traces taking the power between the ICs and smaller traces, yet taking the power to the individual ICs.

Rule of thumb 3:

If you must wire wrap the prototype design place the bypass capacitors on the wire side of the board and solder them directly to the socket. Save yourself a lot of time and trouble and do this before you wire the board.

Rule of thumb 4:

When wiring a prototype do not channel the wires. This looks nice but you will spend a lot of time looking for cross talk problems where the signal is coupled from one wire to another. Use direct point-to-point wiring.

Rule of thumb 5:

Use a crow foot wiring pattern and not a daisy chain pattern. Have the heel of the crow foot at the signal source to drive the entire foot.

Figure 3-3 Example of a Crow Foot Pattern

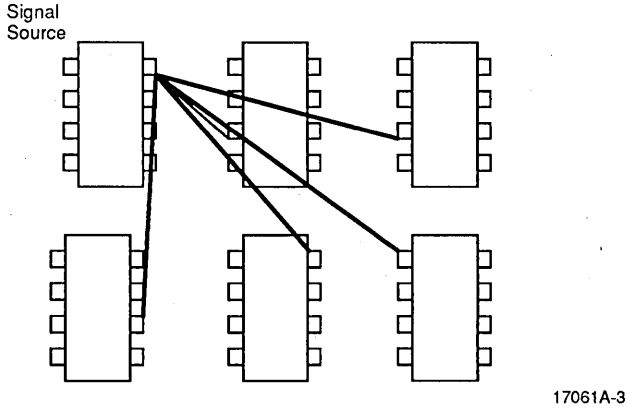
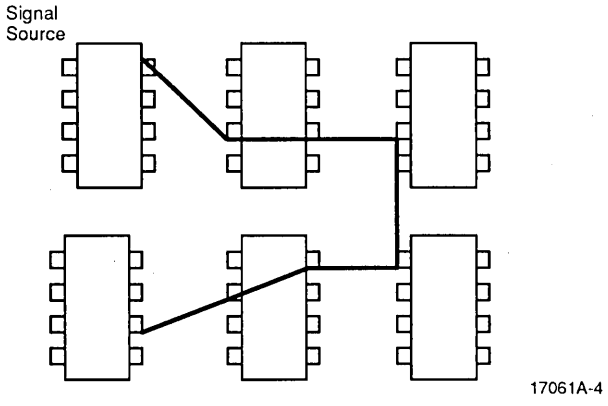
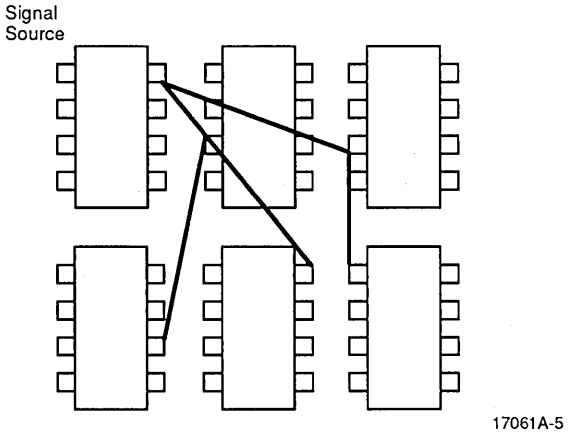


Figure 3-4 Example of a Daisy Chain Pattern



If there are too many destinations for the signal to be supplied from a single pin, use a modified crow foot.

Figure 3-5 Example of a Modified Crow Foot Pattern



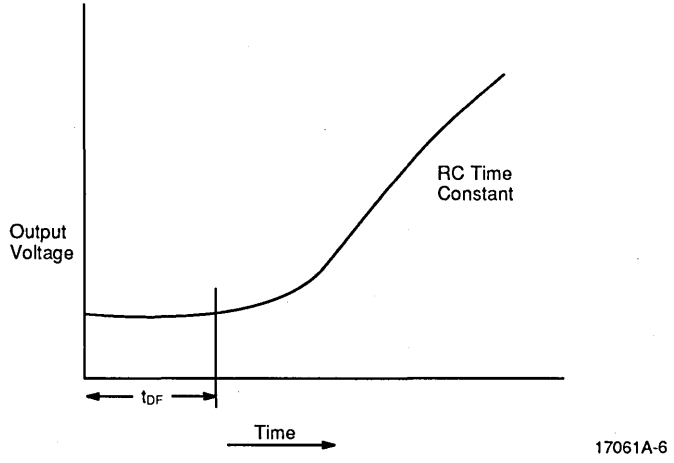
t_{DF} SPECIFICATIONS AND SYSTEM DESIGN CONSIDERATIONS

There are two specifications listed in data sheets—Output Enable to Output Delay (t_{OE}) and Output Enable to Output Float (t_{DF})—that are not always taken into account when designing a system. These two parameters respectively specify how much time the device takes to provide valid data on the bus when $\overline{OE}$ is asserted and when data is no longer available when $\overline{OE}$ is deasserted. This information is very important to avoid a bus contention problem in the final design.

The t_{OE} parameter is easy to test, but is very dependent on the output drive capacity of the device and the capacitive loading of the bus that the device is driving. The device must drive the bus to valid logic levels within this time limit.

The t_{DF} specification, which stands for Time to Data Float, is the maximum time it takes for a device to no longer be driving a bus. The device does not necessarily have to drive the bus to any voltage level, but only to a level that does not prevent another device from driving the bus. This definition is very critical when testing a part and consequently also affects the decisions made by the system designer. The above definition is not tied to the voltage level of the output and consequently, the loading capacitance has no effect on this parameter from the system point of view. This at first may seem inaccurate, but if the node is no longer being driven, then the voltage on the node resulting from the loading capacitance has an R-C time constant that is independent of the device.

Figure 3-6 Device Output dV/dT Curves



The capacitive loading is a test issue and is of considerable importance. To test t_{DF}, the test engineer must look for a voltage change in order to detect when the device is no longer driving the bus. With the voltage change being the only way to test this, the external R-C time constant must be minimized to give the most accurate measurements.

The systems designer must take the bus loading capacitance into account when dealing with t_{ACC}, t_{CE} and t_{OE} but not for t_{DF}.

FINAL

Am27H256

256 Kilobit (32,768 x 8-Bit) High Speed CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 35 ns
- **JEDEC-approved pinout**
  - — Pin compatible with Am27C256
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite™ programming**
  - — Typical programming time of 4 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Standard 28-pin DIP, PDIP, 32-pin LCC and PLCC packages**
- **DESC SMD No. 5962-86063**

GENERAL DESCRIPTION

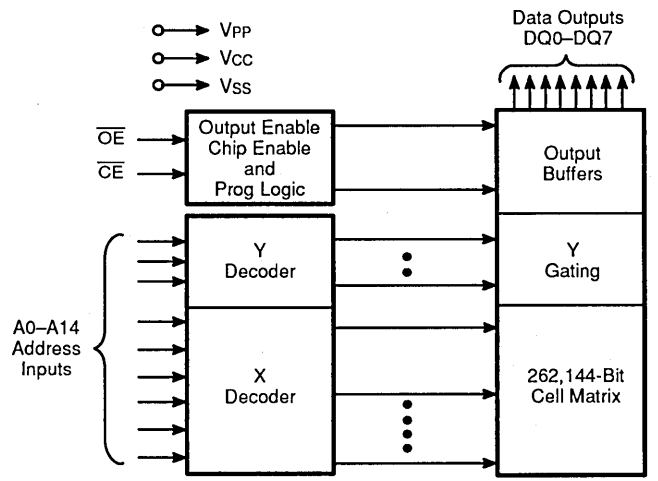
The Am27H256 is an 256 Kbit ultraviolet erasable programmable read-only memory. It is organized as 32K words by 8 bits per word, operates from a single +5 V supply, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 35 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27H256 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 220 mW in active mode, and 50 mW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27H256 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming time of 4 seconds.

BLOCK DIAGRAM



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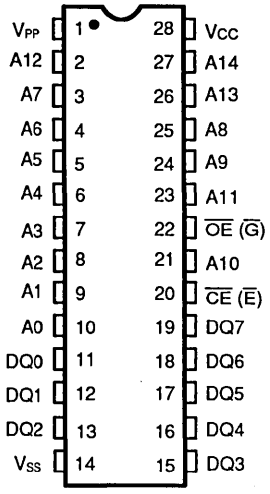
PRODUCT SELECTOR GUIDE

Family Part No.	Am27H256	
Ordering Part Number Vcc ± 5%	-35V05	
Vcc ± 10%	-35	-45
Max Access Time (ns)	35	-45
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	35	-45
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	20	20

CONNECTION DIAGRAMS

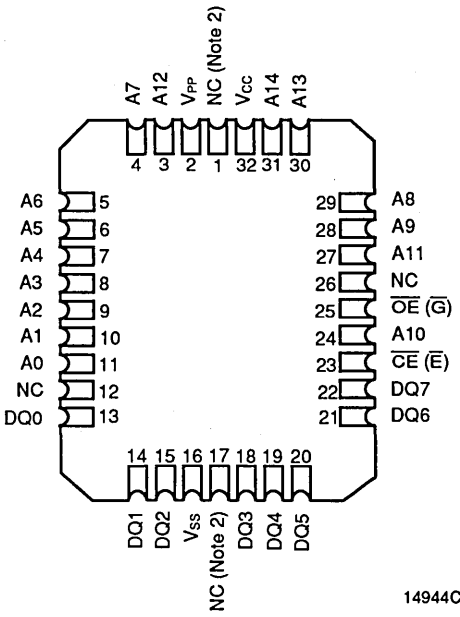
Top View

DIP



14944C-2

PLCC/LCC



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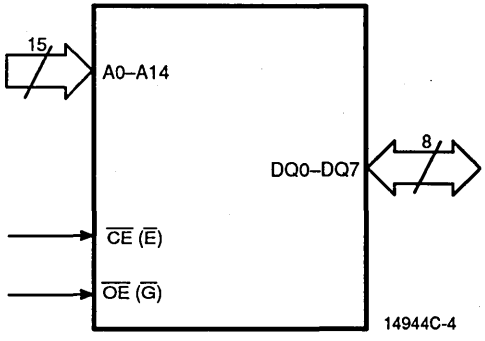
Notes:

1. *JEDEC nomenclature is in parentheses.*
2. *Don't use (DU) for PLCC.*

PIN DESIGNATIONS

A0–A14	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable
DQ0–DQ7	=	Data Inputs/Outputs
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
Vcc	=	Vcc Supply Voltage
VPP	=	Program Supply Voltage
VSS	=	Ground

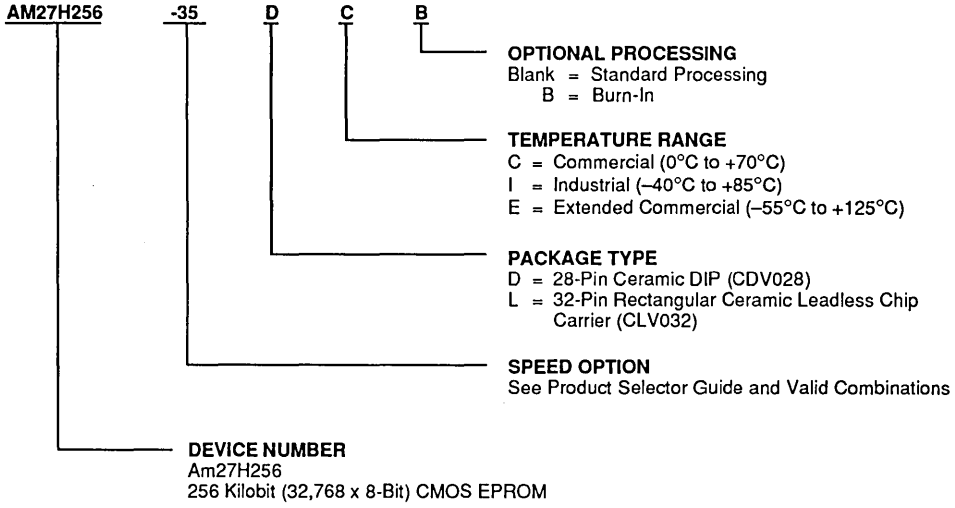
LOGIC SYMBOL



14944C-4

ORDERING INFORMATION
EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27H256-35	DC, DCB, DI, DIB, LC, LI, LCB, LIB
AM27H256-35V05	
AM27H256-45	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB

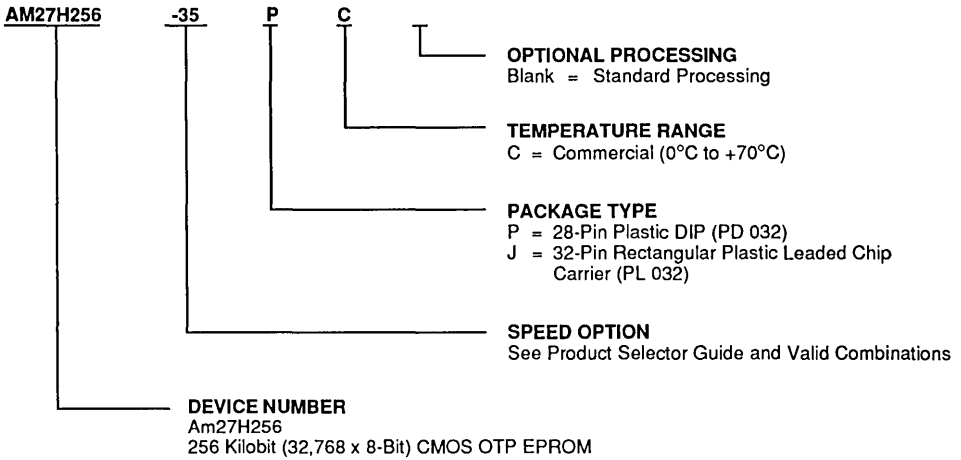
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27H256-35V05	PC, JC
AM27H256-45	

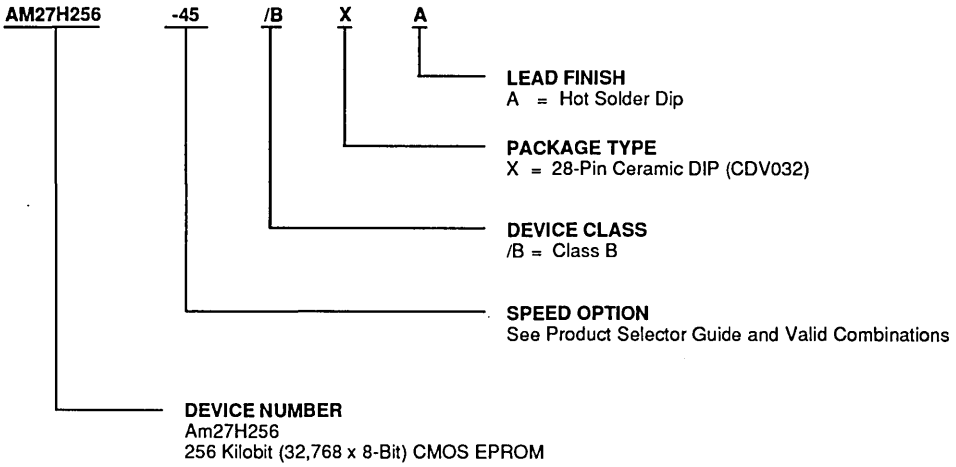
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27H256-45	/BXA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27H256

In order to clear all locations of their programmed contents, it is necessary to expose the Am27H256 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27H256. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27H256 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27H256 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27H256 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27H256

Upon delivery or after each erasure the Am27H256 has all 262,144 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27H256 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27H256. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27H256 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27H256 may be common. A TTL low-level program pulse applied to an Am27H256 $\overline{CE}$ input with V_{PP} = 12.75 V ± 0.25 V and $\overline{OE}$ high, will program that Am27H256. A high-level $\overline{CE}$ input inhibits the other Am27H256 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27H256.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27H256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device code. For the Am27H256, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27H256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27H256 has a standby mode which reduces the maximum V_{CC} current to 50% of the active current. It is placed in standby mode when $\overline{CE}$ is at V_{IH}. The amount of current drawn in standby mode depends on the frequency and the number of address pins switching. The Am27H256 is specified with 50% of the address lines toggling at 10 MHz. A reduction of the frequency or quantity of address lines toggling will significantly reduce actual standby current.

Output OR-Tieing

To accommodate multiple memory connection, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	A0	A9	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	V_{CC}	Hi-Z
Standby		V_{IH}	X	X	X	V_{CC}	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	10H

Notes:

1. *V_H = 12.0 V ± 0.5 V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A10–A14 = V_{IL}*
4. *The Am27H256 uses the same Flashrite algorithm during programming as the Am27C256.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products ..... −65°C to +125°C
All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
All pins except A9, V_{PP}, V_{CC} .... −0.6 V to V_{CC} +0.5 V (Note 1)

A9 and V_{PP} (Note 2) ..... −0.6 V to +13.5 V

V_{CC} ..... −0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (Tc) ..... −40°C to +85°C

Extended Commercial (E) Devices
Case Temperature (Tc) ..... −55°C to +125°C

Military (M) Devices
Case Temperature (Tc) ..... −55°C to +125°C

Supply Read Voltages
V_{CC} for Am27H256-XXV05 ... +4.75 V to +5.25 V
V_{CC} for Am27H256-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2, 3 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.3	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +Vcc	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +Vcc	C/I Devices		10.0	µA
			E/M Devices		10.0	
I_{CC1}	Vcc Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	Vcc Standby Current	$\overline{CE}$ = V_{IH}	C/I Devices		25	mA
			E/M Devices		35	
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = Vcc			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27H256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

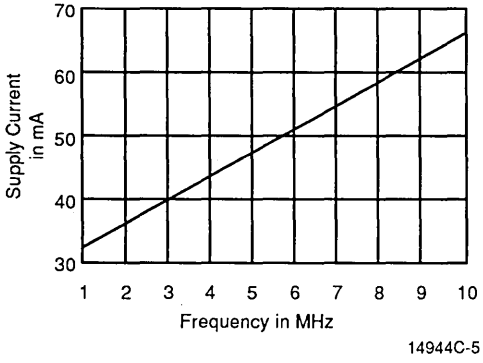


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.0 V, T = 25°C

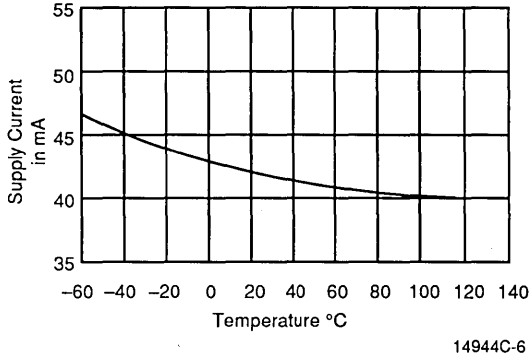


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.0 V, f = 10 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV028		CLV032		PD 028		PL 032		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	6	12	6	12	8	12	8	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	15	6	15	10	15	10	15	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

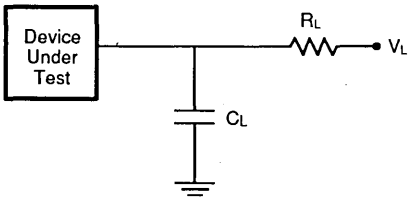
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9,10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27H256	
JEDEC	Standard				-35V05 -35	-45
t_{AVQV}	t_{RCC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min		
			C_L = C_{L1}	Max	35	45
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min		
			C_L = C_{L1}	Max	35	45
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min		
			C_L = C_{L1}	Max	20	20
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float	C_L = C_{L2}	Min	0	0
				Max	20	20
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0
				Max		

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27H256 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C = C_L*
   Input Rise and Fall Times: 5 ns
   Input Pulse Levels: 0 V to 3 V.
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

SWITCHING TEST CIRCUIT



R_L = 121 Ω
V_L = 1.9 V
C_{L1} = 30 pF
C_{L2} = 5 pF

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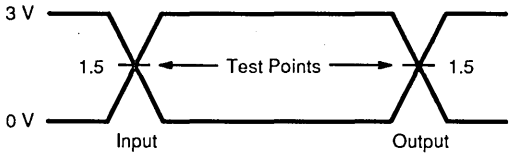
SWITCHING TEST WAVEFORM



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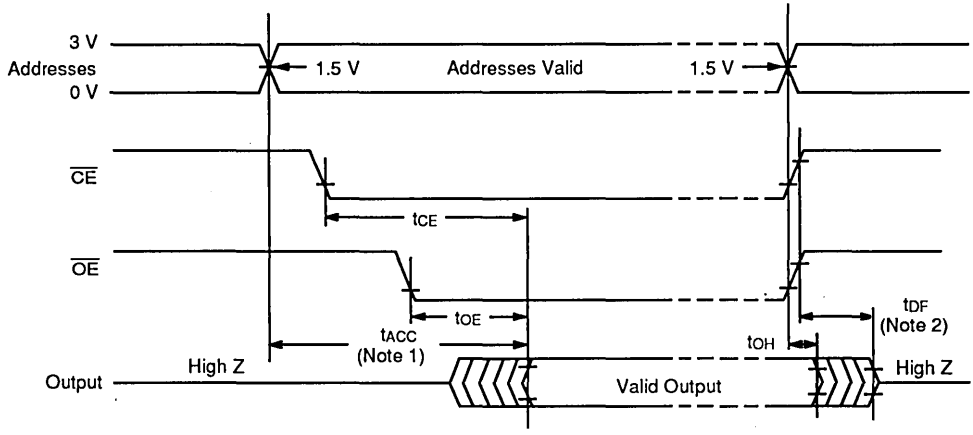
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0." Input pulse rise and fall times are ≤ 5 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS



14944C-9

Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27H010

1 Megabit (131,072 x 8-Bit) High Speed CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 45 ns
- **JEDEC-approved pinout**
  - — Plug in upgrade of standard 1 Mbit EPROMs
  - — Easy upgrade from 28-pin JEDEC EPROMs
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite™ programming**
  - — Typical programming time of 16 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Compact 32-pin DIP, PDIP, LCC and PLCC packages**
- **DESC SMD No. 5962-89614**

GENERAL DESCRIPTION

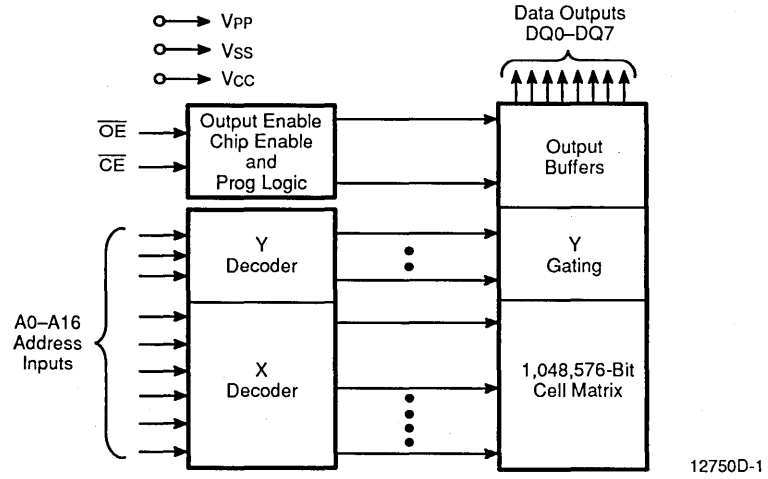
The Am27H010 is a 1 Mbit ultraviolet erasable programmable read-only memory. It is organized as 131,072 words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 45 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27H010 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 220 mW in active mode, and 50 mW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27H010 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming time of 16 seconds.

BLOCK DIAGRAM



Publication# 12750 Rev. D Amendment/0
Issue Date: July 1993

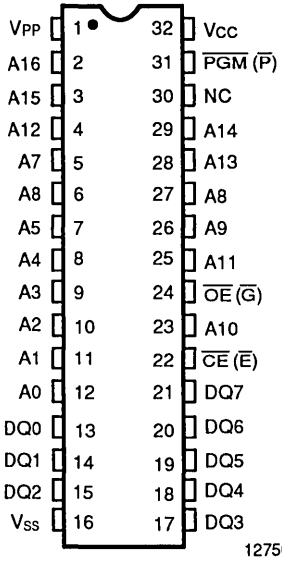
PRODUCT SELECTOR GUIDE

Family Part No.	Am27H010			
Ordering Part No: Vcc ±5%	-45V05			-90V05
Vcc ±10%	-45	-55	-70	-90
Max Access Time (ns)	45	55	70	90
$\overline{CE}$ ($\overline{E}$) Access (ns)	45	55	70	90
$\overline{OE}$ ($\overline{G}$) Access (ns)	20	25	35	40

CONNECTION DIAGRAMS

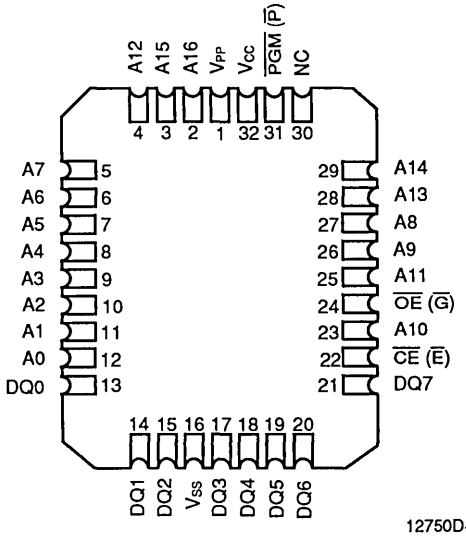
Top View

DIP



12750D-2

PLCC/LCC



12750D-3

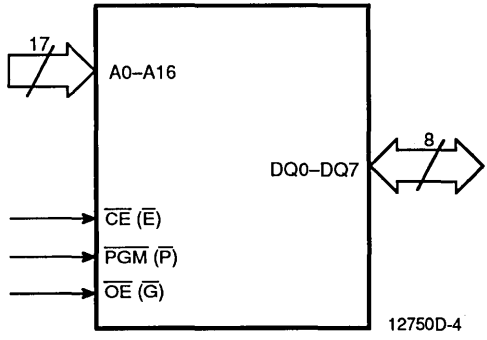
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A16	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip
DQ0–DQ7	=	Data Inputs/Outputs
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
Vcc	=	Vcc Supply Voltage
VPP	=	Program Supply Voltage
VSS	=	Ground

LOGIC SYMBOL

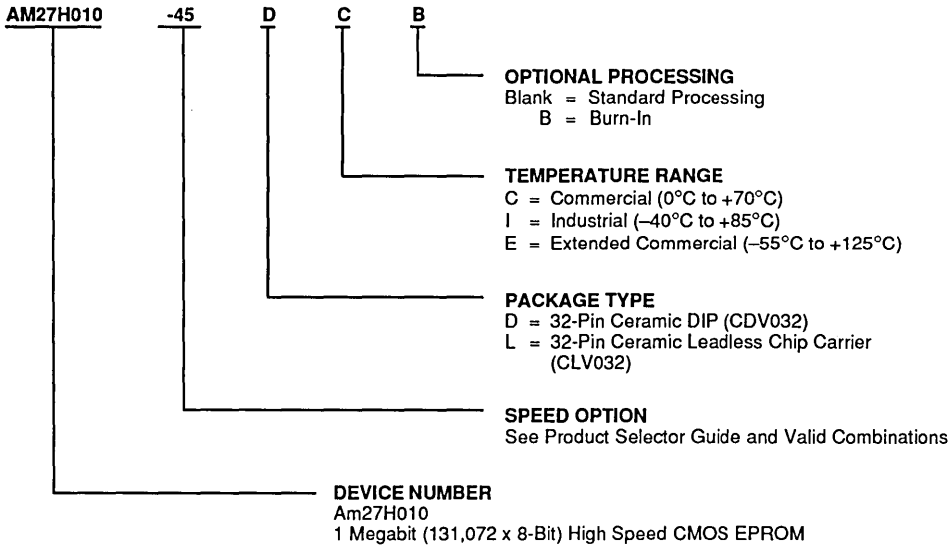


12750D-4

ORDERING INFORMATION

EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27H010-45	DC, DCB, DI, DIB, LC, LI, LCB, LIB
AM27H010-45V05	
AM27H010-55	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27H010-70	
AM27H010-90	

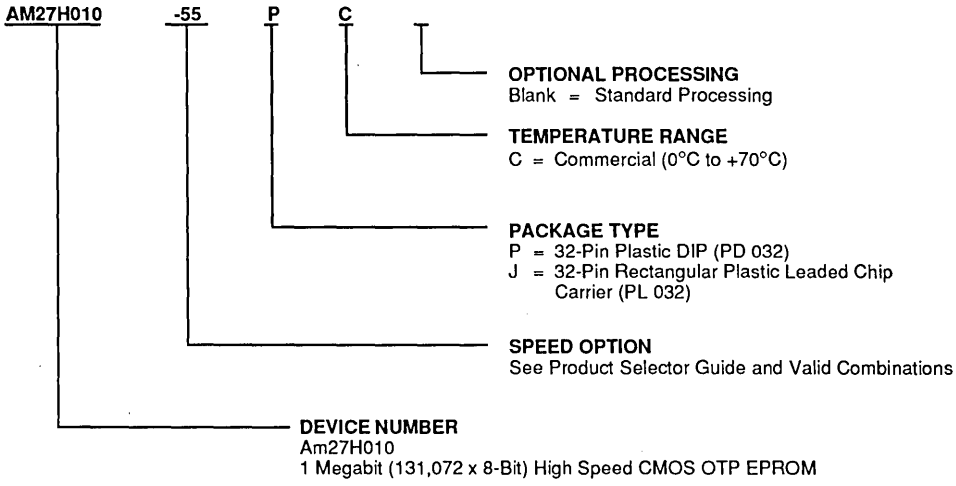
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27H010-55	PC, JC
AM27H010-70	
AM27H010-90	
AM27H010-90V05	

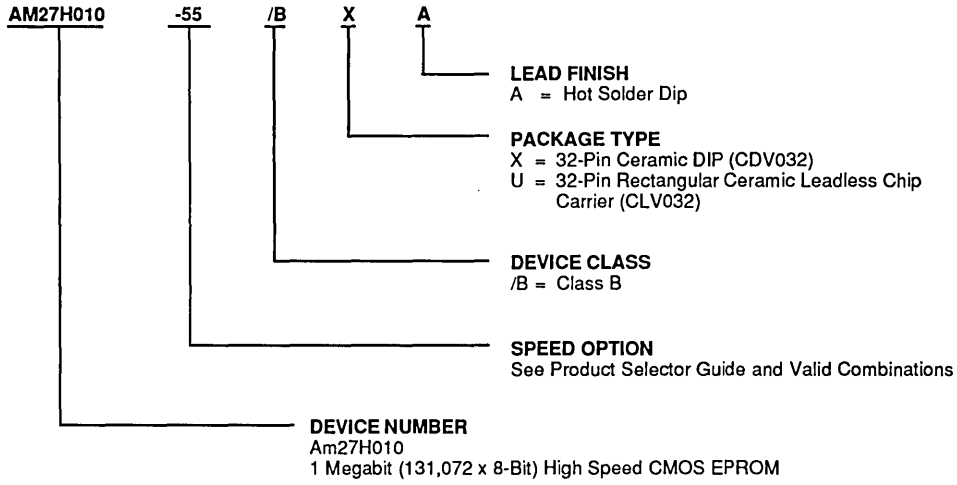
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27H010-55	/BXA, /BUA
AM27H010-70	
AM27H010-90	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27H010

In order to clear all locations of their programmed contents, it is necessary to expose the Am27H010 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27H010. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27H010 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27H010 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27H010 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27H010

Upon delivery or after each erasure the Am27H010 has all 1,048,576 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27H010 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP}, $\overline{CE}$ and $\overline{PGM}$ is at V_{IL} and $\overline{OE} = V_{IH}$.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27H010. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27H010 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27H010 may be common. A TTL low-level program pulse applied to an Am27H010 $\overline{CE}$ input and with V_{PP} = 12.75 V ± 0.25 V, $\overline{PGM}$ Low and $\overline{OE}$ High will program that Am27H010. A high-level $\overline{CE}$ input inhibits the other Am27H010 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27H010.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27H010. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device code. For the Am27H010, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27H010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{OE}). Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27H010 has a standby mode which reduces the maximum V_{CC} current to 50% of the active current. It is placed in standby mode when $\overline{CE}$ is at V_{IH}. The amount of current drawn in standby mode depends on the frequency and the number of address pins switching. The Am27H010 is specified with 50% of the address lines

toggling at 10 MHz. A reduction of the frequency or quantity of address lines toggling will significantly reduce the actual standby current.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}/V_{PP}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	A0	A9	V_{IH}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	V_{IH}	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	V_{IH}	Hi-Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{CC}	0EH

Notes:

1. *V_H = 12.0 V± 0.5 V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A10–A18 = V_{IL}*
4. *The Am27H010 uses the same Flashrite algorithm as the Am27C010.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products ..... −65°C to +125°C
All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
All pins except A9, V_{PP}, V_{CC} ... −0.6 V to V_{CC} + 0.5 V (Note 1)

A9 and V_{PP} (Note 2) ..... −0.6 V to +13.5 V

V_{CC} ..... −0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices

Case Temperature (Tc) ..... −40°C to +85°C

Extended Commercial (E) Devices

Case Temperature (Tc) ..... −55°C to +125°C

Military (M) Devices

Case Temperature (Tc) ..... −55°C to +125°C

Supply Read Voltages

V_{CC} for Am27H010-XXV05 ... +4.75 V to +5.25 V

V_{CC} for Am27H010-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2, 3 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	Vcc Active Current	$\overline{CE}$ = V_{IL}, f = 10 MHz	C/I Devices		50	mA
	(Note 3)	I_{OUT} = 0 mA	E/M Devices		60	
I_{CC2}	Vcc Standby Current	$\overline{CE}$ = V_{IH}	C/I Devices		25	mA
			E/M Devices		35	
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27H010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

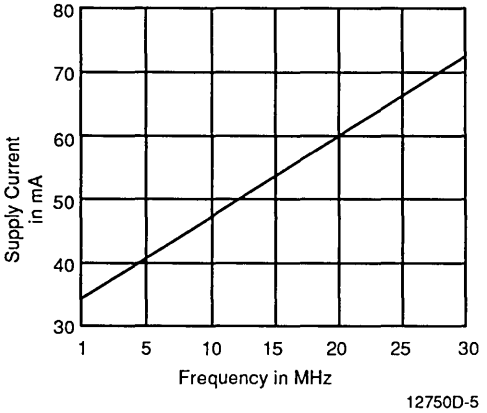


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.0 V, T = 25°C

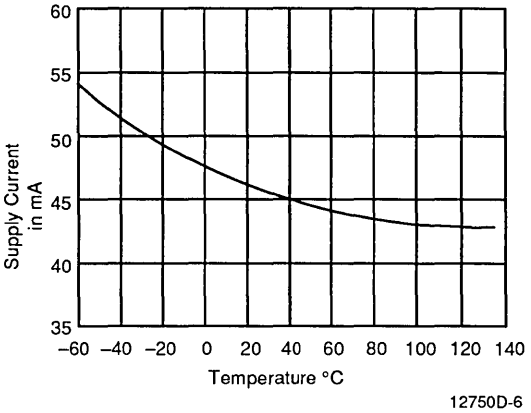


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.0 V, f = 10 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		PD 032		PL 032		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	6	12	6	12	8	12	8	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	15	6	15	10	15	10	15	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

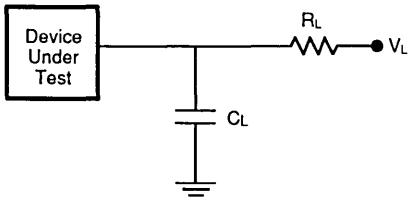
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9,10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27H010				Unit
JEDEC	Standard				-45V05 -45	-55	-70	-90V05 -90	
t_{AVQV}	t_{RCC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, C_L = C_{L1}	Min					ns
				Max	45	55	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}, C_L = C_{L1}	Min					ns
				Max	45	55	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}, C_L = C_{L1}	Min					ns
				Max	20	25	35	40	ns
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float	C_L = C_{L2}	Min	0	0	0	0	ns
				Max	20	25	35	40	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	ns
				Max					ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27H010 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C = C_L*
   Input Rise and Fall Times: 5 ns
   Input Pulse Levels: 0 V to 3 V.
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

SWITCHING TEST CIRCUIT



R_L = 121 Ω
V_L = 1.9 V
C_{L1} = 30 pF
C_{L2} = 5 pF

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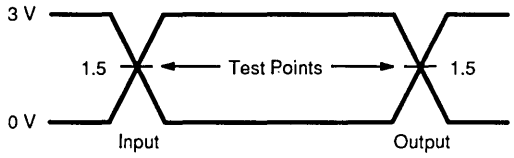
SWITCHING TEST WAVEFORM



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AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0." Input pulse rise and fall times are ≤ 5 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

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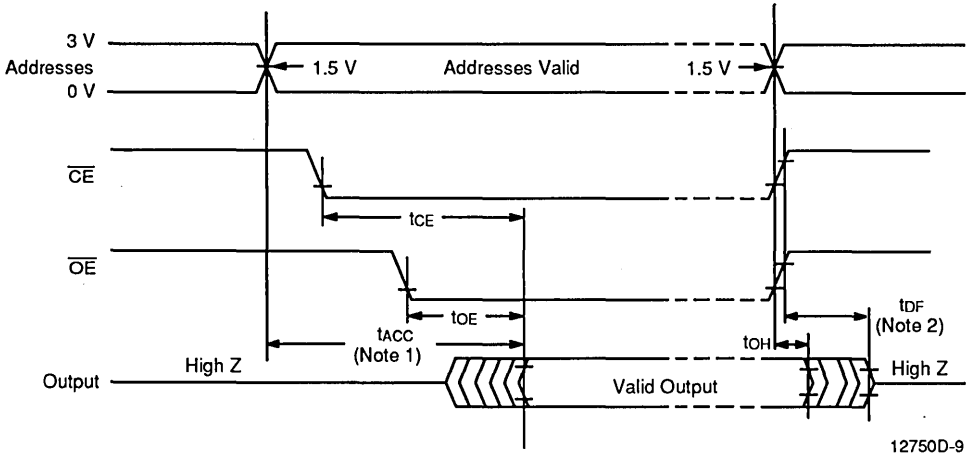
SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

SECTION

4 LOW VOLTAGE CMOS ERASABLE PROGRAMMABLE READ ONLY MEMORIES (EPROMs)

AN INTRODUCTION TO LOW VOLTAGE EPROMs

Advanced Micro Devices is committed to being the technology leader in Non-Volatile memories and therefore, continues to focus on developing superior memory products that serve the needs of our customers. Our technology leadership is evidenced by our offering of a complete line of EPROMs, the highest performance and density EPROM products in the marketplace as well as the industry's smallest die sizes. We are now proud to announce a family of Low Voltage (3.3 V) EPROMs to complement our product offering.

In the recent past, momentum for the need of Low Voltage ICs has been exponentially growing. The Electronics industry has demonstrated a well established trend of product improvements and enhancements while simultaneously decreasing the size and cost of the equipment. Typical examples of this phenomenon is the notebook and sub-notebook class of personal computers and the cellular phones of today. This trend towards "miniaturization" is expected to continue with the market demanding even smaller formfactors and increasing portability—in the form of handheld instrumentation—but with the same capability and performance levels that is available from their larger counterparts.

This trend of smaller formfactors and increasing portability forces manufacturers to constantly reduce the size and weight of their equipment. As batteries consume an increasingly larger share of the size and weight of the portable equipment, many manufacturers are now looking to reduce the number of batteries and/or lowering the power consumption i.e., the battery drain. This has led to the migration towards Low Voltage ICs. For example, a portable computer that utilizes 5.0 V components commonly needs five 1.2 V secondary (rechargeable) Nickel Cadmium or five 1.5 V primary (throw-away) alkaline batteries. By switching to 3.0 V components the required number of batteries now becomes three, thereby effectively reducing the weight of the heaviest component in the system by 40%. Switching to a 3.0 V operation from a 5.0 V operation also cuts down the power consumption significantly. As power is proportional to the square of the voltage, reducing the operating voltage from 5.0 V to 3.0 V results in power savings of at least 57%. This power consumption can further be reduced if the current level of the individual devices is lowered.

In keeping with our philosophy of offering memories that solve customers' needs, AMD is proud to announce a family of 3.3 V EPROMs. This Low Voltage family, designated as "Am27LV", is offered with two voltage ranges. The first has a V_{CC} tolerance level of 3.3 V ± 10% — 3.0 V to 3.6 V— making it suitable for use in systems that have regulated power supplies, and second, a voltage range of 2.7 V to 3.6 V making it ideally suited for battery operated systems.

This family complies with the recently approved JEDEC standards on Low Voltage. These devices typically have lower active and standby current levels than their 5.0 V counterparts thereby reducing the power consumption by as much as 83%. These products are also pin-compatible with their 5.0 V counterparts and are being offered in the traditional EPROM packages.

PRELIMINARY

Am27LV010/Am27LV010B

1 Megabit (131,072 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Single +3.3 V power supply**
  - — Regulated power supply 3.0 V–3.6 V
  - — Unregulated power supply 2.7 V–3.6 V (for battery operated systems)
- **Low power consumption:**
  - — 10 µA typical CMOS standby current
  - — 90 µW maximium standby power
  - — 54 mW maximum power at 5 MHz
- **Fast access time—120 ns**
- **JEDEC-approved pinout**
  - — Pin compatible with 5.0 V 1 Mbit EPROM
  - — Easy upgrade from 28-pin EPROMs
- **Fast Flashrite™ programming**
  - — Typical programming time of 16 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **High noise immunity**
- **Compact 32-pin DIP package requires no hardware change for upgrades to 8 Mbit**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

GENERAL DESCRIPTION

The Am27LV010 is a low voltage, low power 1 Mbit, ultraviolet erasable, progammable read-only memory, organized as 128K words by 8 bits per word.

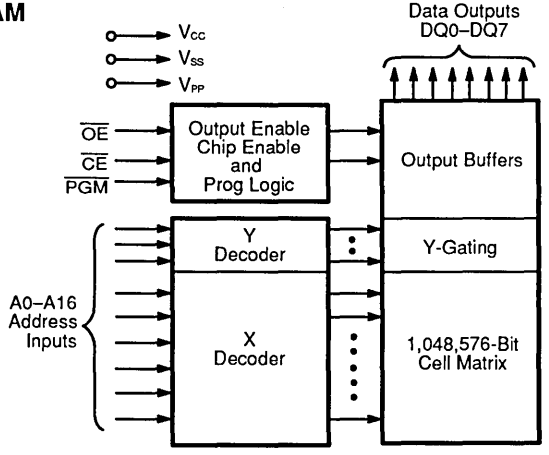
The Am27LV010 operates from a single power supply of 3.3 V and is offered with two power supply tolerances. The Am27LV010 has a Vcc tolerance range of 3.3 V ± 0.3 V making it suitable for use in systems that have regulated power supplies. The Am27LV010B has a voltage supply range of 2.7 V–3.6 V making it an ideal part for battery operated systems.

Maximum power consumption of the Am27LV010 in standby mode is only 90 µW. If the device is constantly accessed at 5 MHz, then the maximum power consumption increases to 54 mW. These power ratings are significantly lower than typical EPROMs. Also, as power consumption is proportional to voltage squared, 3.3 V devices consume at least 57% less power than their 5.0 V counterparts. Due to its lower current and voltage, the Am27LV010 is well-suited for battery operated and portable systems as it extends the battery life in these systems. Typical applications are notebook and hand-held computers as well as cellular phones.

The Am27LV010 is packaged in the industry standard 32-pin windowed ceramic DIP and LCC packages, as well as one-time programmable (OTP) packages. This device is pin-compatible with the 5.0 V devices.

The Am27LV010 uses AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming time of 16 seconds. This device is manufactured on AMD's sub-micron process technology which provides high speed, low power and high noise immunity.

BLOCK DIAGRAM



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Issue Date: July 1993

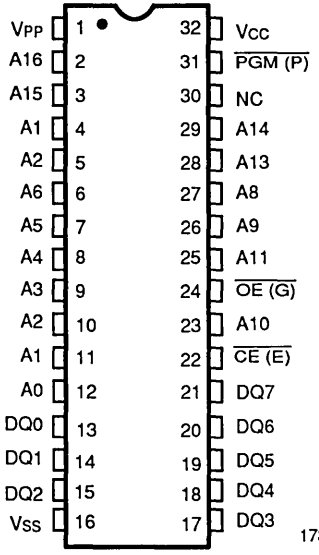
PRODUCT SELECTOR GUIDE

Family Part No	Am27LV010/Am27LV010B				
Ordering Part No:					
Am27LV010 (3.0 V – 3.6 V)	**-120**	**-150**	**-200**	**-250**	**-300**
Am27LV010B (2.7 V – 3.6 V)	**-150**	**-150**	**-200**	**-250**	**-300**
Max Access Time (ns)	120	150	200	250	300
$\overline{CE}$ ($\overline{E}$) Access (ns)	120	150	200	250	300
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	65	75	100	120

CONNECTION DIAGRAMS

Top View

DIP



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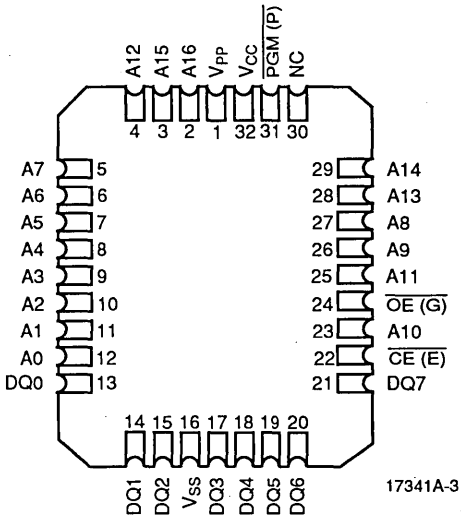
PLCC/LCC



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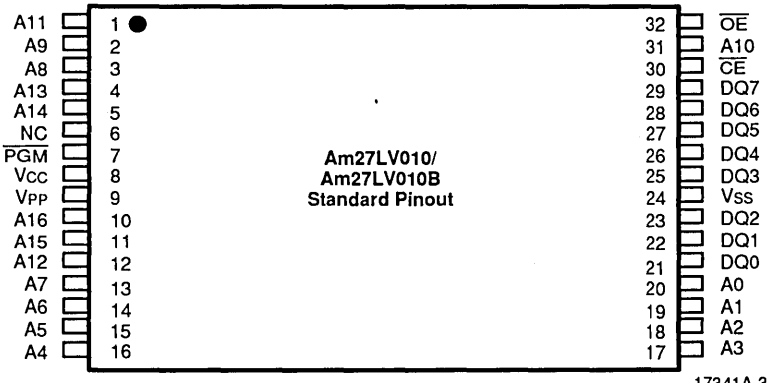
Notes:

1. *JEDEC nomenclature is in parenthesis.*
2. *The 32-pin DIP to 32-pin LCC configuration varies from the JEDEC 28-pin DIP to 32-pin LCC configuration.*

TSOP*



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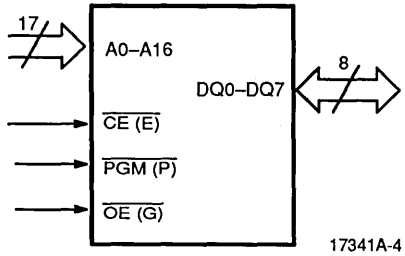
**Contact local AMD sales office for package availability.*

PIN DESCRIPTION

A0–A16 = Address Inputs
$\overline{CE\ (E)}$ = Chip Enable Input
DQ0–DQ7 = Data Input/Outputs
NC = No Internal Connect
$\overline{OE\ (G)}$ = Output Enable Input
$\overline{PGM\ (P)}$ = Program Enable Input
V_{CC} = V_{CC} Supply Voltage
V_{PP} = Program Supply Voltage
V_{SS} = Ground

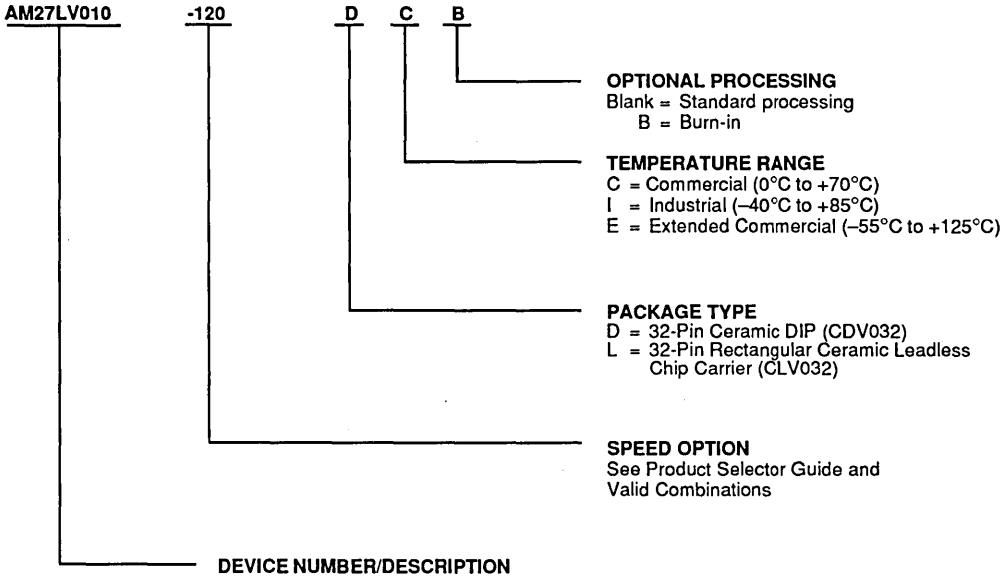
LOGIC SYMBOL



17341A-4

ORDERING INFORMATION
EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



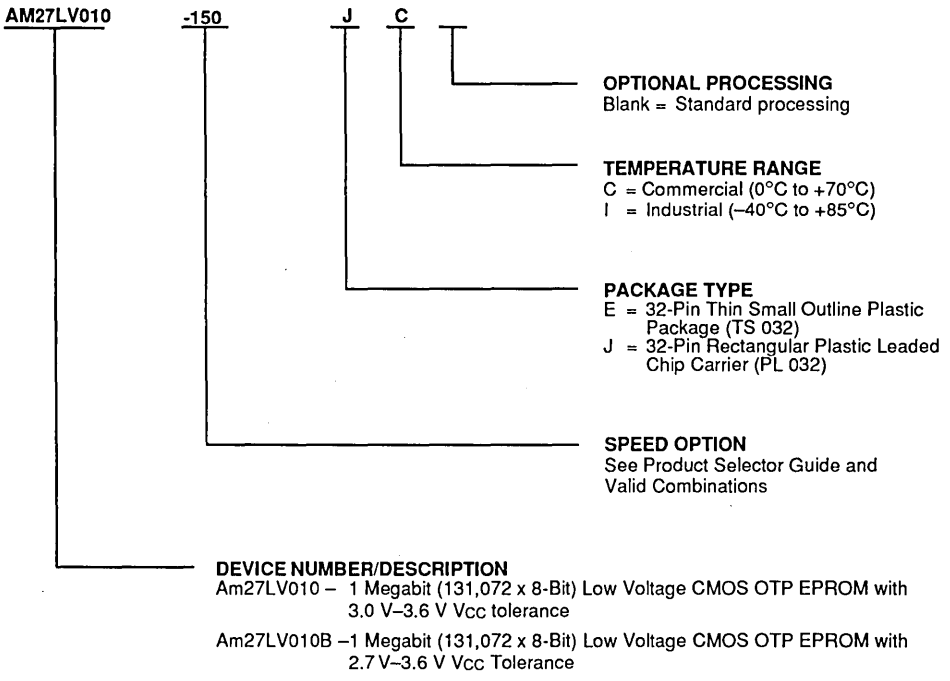
Valid Combinations	
AM27LV010-120	DC, DCB, LC, LCB
AM27LV010-150	DC, DCB, DE, DEB, DI, DIB, LC, LI, LE, LEB
AM27LV010-200	
AM27LV010-250	
AM27LV010-300	
AM27LV010B-150	
AM27LV010B-200	
AM27LV010B-250	
AM27LV010B-300	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



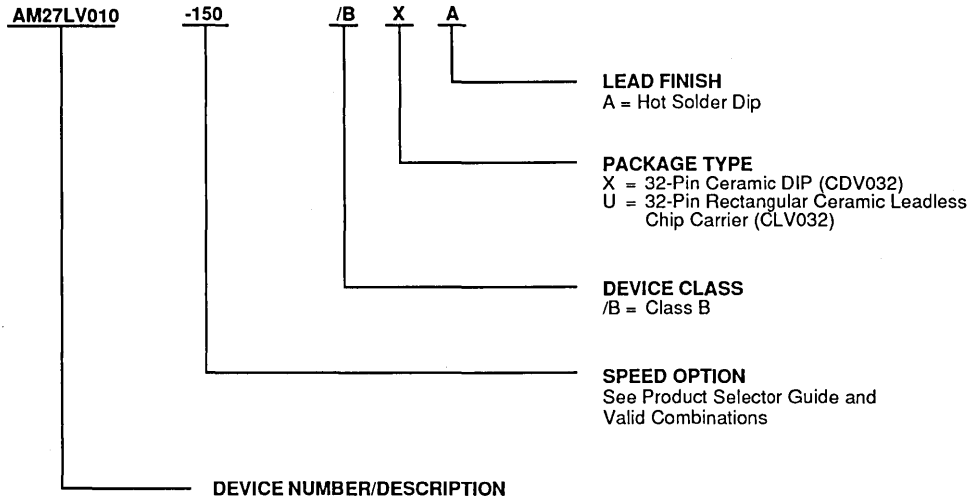
Valid Combinations	
AM27LV010-150	JC, EC, JI, EI
AM27LV010-200	
AM27LV010-250	
AM27LV010-300	
AM27LV010B-200	
AM27LV010B-250	
AM27LV010B-300	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27LV010-150	/BXA, /BUA
AM27LV010-200	
AM27LV010-250	
AM27LV010-300	
AM27LV010B-250	
AM27LV010B-300	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27LV010

In order to clear all locations of their programmed contents, it is necessary to expose the Am27LV010 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27LV010. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Å — with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27LV010 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27LV010, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27LV010 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27LV010

Upon delivery, or after each erasure, the Am27LV010 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27LV010 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ and $\overline{PGM}$ are at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP}$ = 5.25 V. Am27LV010 can be programmed using the same algorithm as the 5 V counterpart 27C010.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27LV010s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27LV010 may be common. A TTL low-level program pulse applied to an Am27LV010 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, $\overline{PGM}$ LOW, and $\overline{OE}$ HIGH will program that Am27LV010. A high-level $\overline{CE}$ input inhibits the other Am27LV010s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27LV010.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the Am27LV010. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and Byte 1 (A0 = V_{IH}), the device identifier code. For the Am27LV010, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27LV010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27LV010 has a CMOS standby mode which reduces the maximum V_{CC} current to 25 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27LV010 also has a TTL-standby mode which reduces the maximum V_{CC} current to 0.6 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Mixed Power Supply System

Am27LV020 (in 3.0 V to 3.6 V regulated power supply) can be intefaced with 5 V system only when the I/O pins (DQ0–DQ7) are not driven by the 5 V system. V_{IHmax} = V_{CCLV} + 2.2 V for address and clock pins and V_{IHmax} = V_{CCLV} + 0.5 V for I/O pins should be followed to avoid CMOS latch-up condition

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-sele cting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		V_{CC} ± 0.3 V	X	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	0EH

Notes:

1. *X can be either V_{IL} or V_{IH}*
2. *V_H = 12.0 V± 0.5 V*
3. *A1–A8 = A10–A16 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}:
- All pins except A9, V_{PP}, and V_{CC} (Note 1) ..... −0.6 V to V_{CC} + 0.6 V
- A9 and V_{PP} (Note 2) ..... −0.6 V to 13.5 V
- V_{CC} ..... −0.6 V to 7.0 V

Notes:

1. *During transitions, the input may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *During transitions, A9 and V_{CC} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. This is a stress rating only; functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (Tc) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (Tc) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (Tc) ..... −55°C to +125°C

Supply Read Voltages:
- V_{CC} for Am27LV010 ..... +3.0 V to +3.6 V
- V_{CC} for Am27LV010B ..... +2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 2, 3 and 4) (for APL products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
TTL and CMOS Inputs for V_{CC} = 3.0 V to 3.6 V						
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5	µA
			E/M Devices		5	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		15	mA
			E/M Devices		20	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}	TTL		0.6	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	CMOS		25	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
CMOS Inputs for V_{CC} = 2.7 V to 3.6 V						
V_{OH}	Output HIGH Voltage	I_{OH} = –20 µA		V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 20 µA			0.1	V
V_{IH}	Input HIGH Voltage			0.7 V_{CC}	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	0.2 V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		5	µA
			E/M Devices		5	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		15	mA
			E/M Devices		20	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}	TTL		0.6	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} + 0.3 V			25	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27LV010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

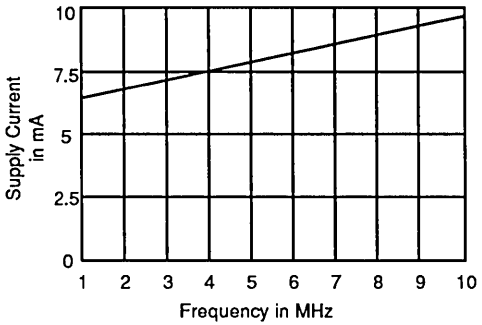


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 3.6 V, T = 25°C

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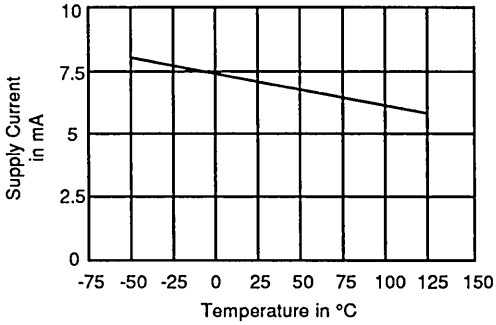

Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 3.6 V, f = 5 MHz

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CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		TS 032		Unit
			Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	10	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

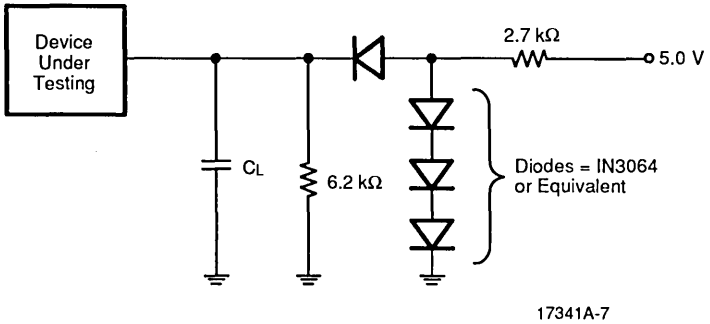
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

JEDEC	Standard	Parameter Description	Test Conditions		Am27LV010/Am27LV010B -120	-150	-200	-250	-300	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min						ns
				Max	120	150	200	250	300	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min						ns
				Max	120	150	200	250	300	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min	–	–	–	–	–	ns
				Max	50	65	75	100	120	
t_{EHQZ} t_{GHQZ}	t_{DF}	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float (Note 2)		Min	0	0	0	0	0	ns
				Max	40	50	60	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	ns
				Max	–	–	–	–	–	

Notes:

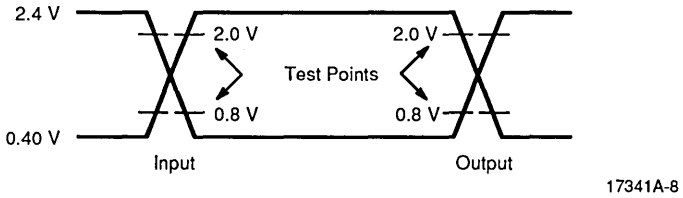
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27LV010 must not be removed from, or inserted into, a socket when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.40 V to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2.0 V
   Outputs: 0.8 V and 2.0 V

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



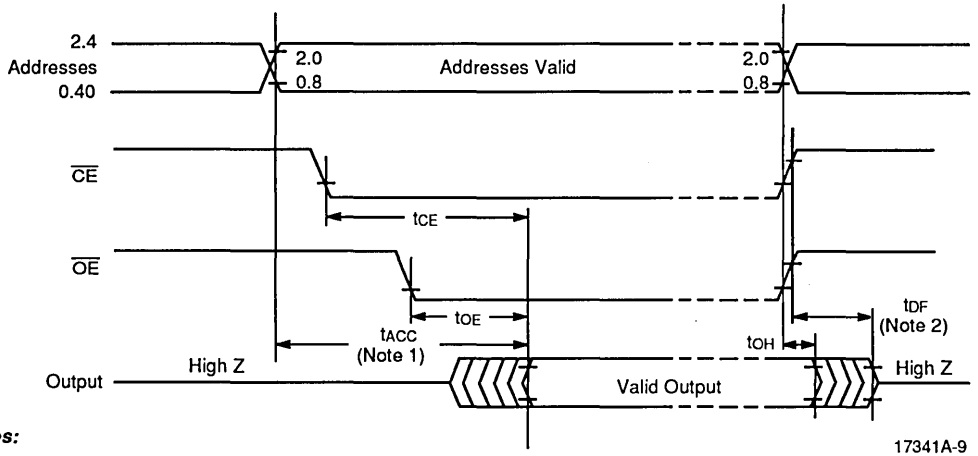
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.40 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORM



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Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

PROGRAMMING FLOW CHART

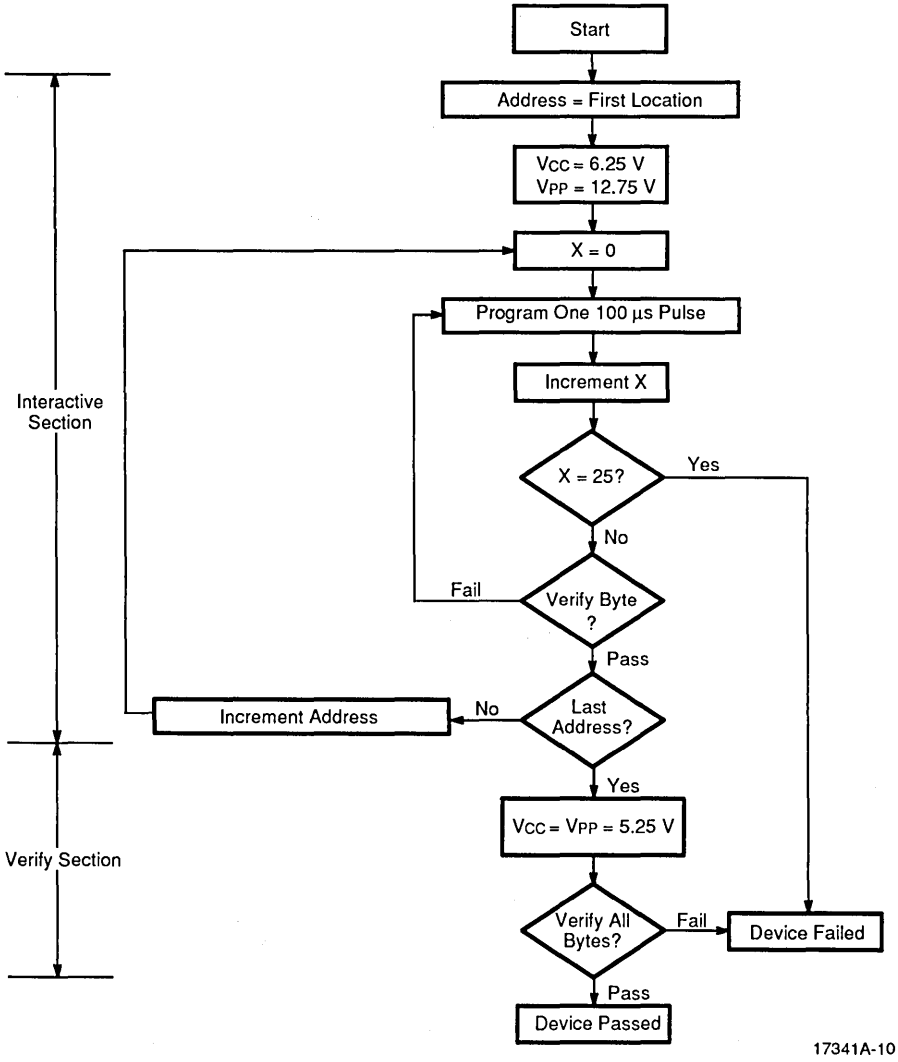


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2 and 3)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		3.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

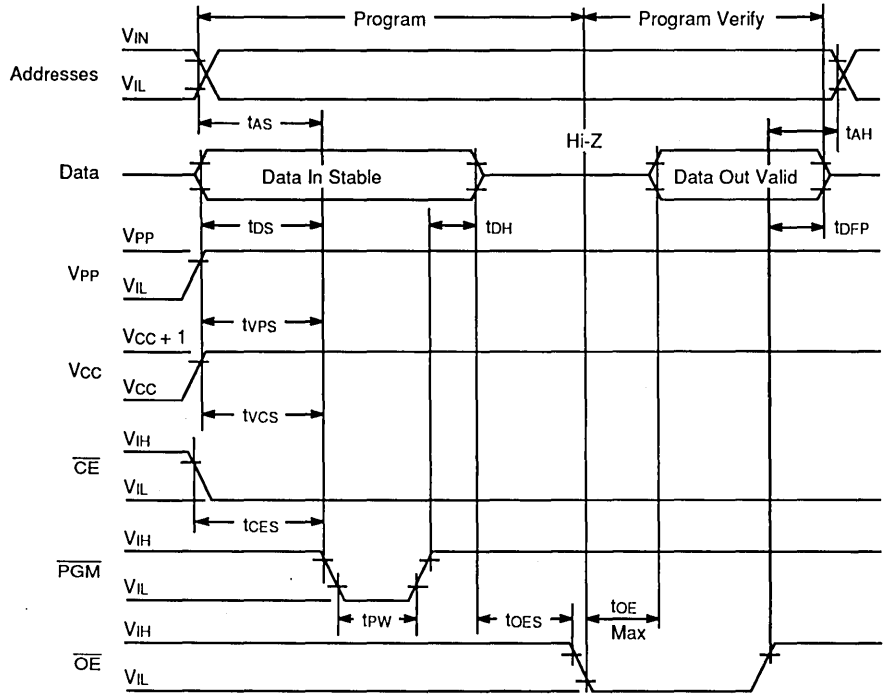
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2 and 3)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *When programming the Am27LV010, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.*
3. *Programming characteristics are sampled but not 100% tested at worst-case conditions.*

INTERACTIVE AND FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 and 2)



17341A-11

Notes:

1. *The input timing reference level is 0.8 V for V_{IL} and 3 V for V_{IH}.*
2. *t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.*

PRELIMINARY

Am27LV020/Am27LV020B

2 Megabit (262,144 x 8-Bit) Low Voltage CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Single 3.3 V power supply**
  - — Regulated power supply 3.0 V–3.6 V
  - — Unregulated power supply 2.7 V–3.6 V (battery-operated systems)
- **Low power consumption:**
  - — 10 µA typical CMOS standby current
  - — 90 µW maximum standby power
  - — 54 mW power at 5 MHz maximum
- **Fast access time**
  - — 150 ns
- **JEDEC-approved pinout**
  - — Pin compatible with 5.0 V 2 Mbit EPROM
  - — Easy upgrade from 28-pin JEDEC EPROMs
- **100% Flashrite™ programming**
  - — Typical programming time of 32 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **High noise immunity**
- **Compact 32-pin DIP package requires no hardware change for upgrades to 8 Mbit**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

GENERAL DESCRIPTION

The Am27LV020 is a low voltage, low power 2 Mbit, ultraviolet erasable, progammable read-only memory organized as 256K words by 8 bits per word.

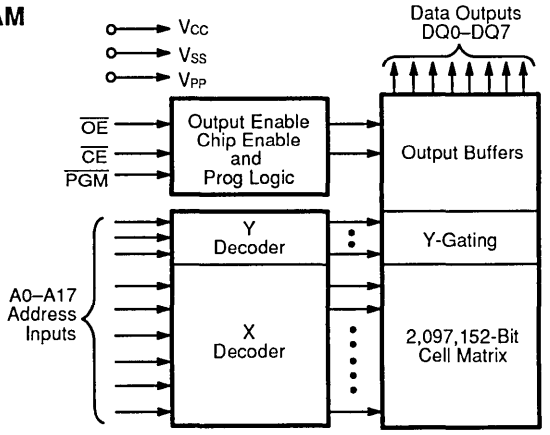
The Am27LV020 operates from a single power supply of 3.3 V and is offered with two power supply tolerances. The Am27LV020 has a Vcc tolerance range of 3.3 V ±0.3 V making it suitable for use in systems that have regulated power supplies. The Am27LV020B has a voltage supply range of 2.7 V–3.6 V making it an ideal part for battery operated systems.

Maximum power consumption of the Am27LV020 in standby mode is only 90 µW. If the device is constantly accessed at 5 MHz, then the maximum power consumption increases to 54 mW. These power ratings are significantly lower than typical EPROMs. Also, as power consumption is proportional to voltage squared, 3.3 V devices consume at least 57% less power than their 5.0 V counterparts. Due to its lower current and voltage, the Am27LV020 is well-suited for battery operated and portable systems as it extends the battery life in these systems. Typical applications are notebook and handheld computers as well as cellular phones.

The Am27LV020 is packaged in the industry standard 32-pin windowed ceramic DIP and LCC packages, as well as one-time programmable (OTP) packages. This device is pin-compatible with the 5.0 V devices.

The Am27LV020 uses AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming times of 32 seconds. This device is manufactured on AMD's sub-micron process technology which provides high speed, low power and high noise immunity.

BLOCK DIAGRAM



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Publication# 17342 Rev. A Amendment/0
Issue Date: July 1993

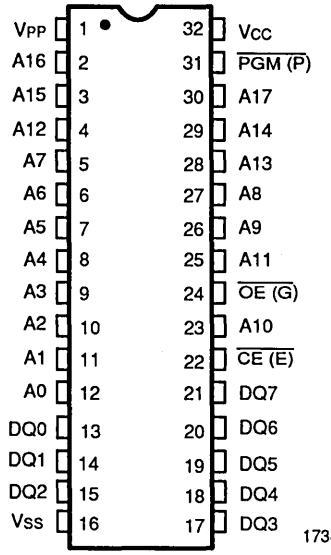
PRODUCT SELECTOR GUIDE

Family Part No	Am27LV020/Am27LV020B			
Ordering Part No:				
Am27LV020 (3.0 V–3.6 V)	-150	-200	-250	-300
Am27LV020B (2.7 V–3.6 V)		-200	-250	-300
Max Access Time (ns)	150	200	250	300
$\overline{CE}$ ($\overline{E}$) Access (ns)	150	200	250	300
$\overline{OE}$ ($\overline{G}$) Access (ns)	65	75	100	120

CONNECTION DIAGRAMS

Top View

DIP



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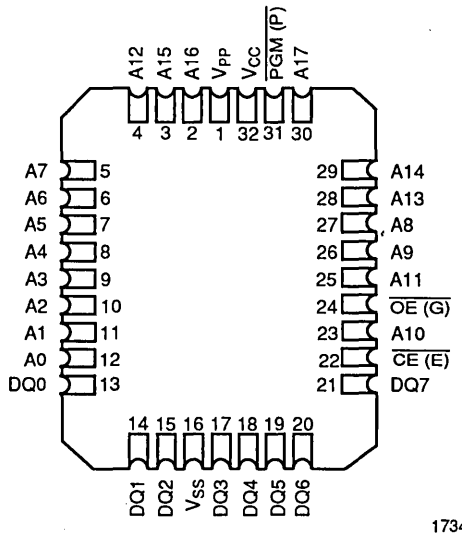
PLCC/LCC



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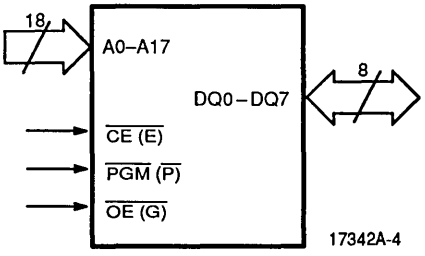
Notes:

1. *JEDEC nomenclature is in parenthesis.*
2. *The 32-pin DIP to 32-pin LCC configuration varies from the JEDEC 28-pin DIP to 32-pin LCC configuration.*

PIN DESCRIPTION

A0–A17	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0–DQ7	=	Data Input/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
VCC	=	VCC Supply Voltage
VPP	=	Program Supply Voltage
VSS	=	Ground

LOGIC SYMBOL



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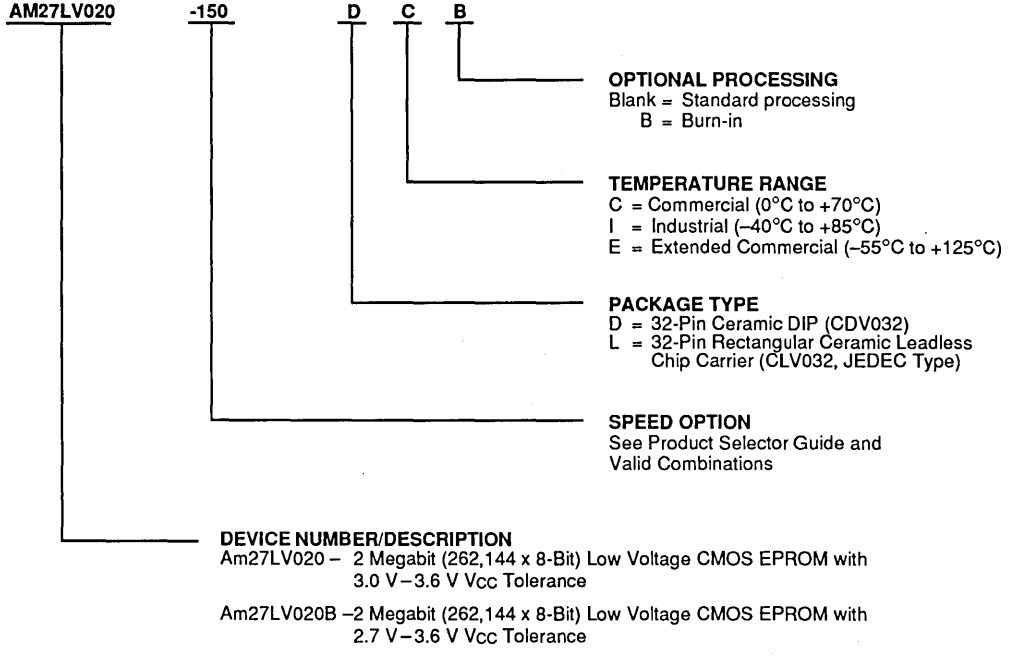
ORDERING INFORMATION
EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



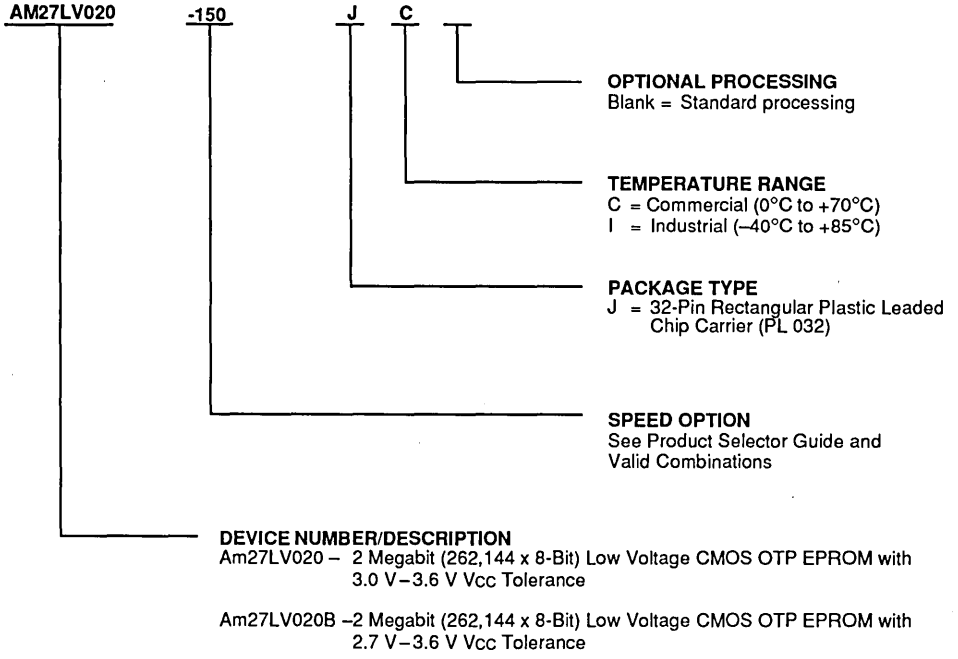
Valid Combinations	
AM27LV020-150	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27LV020-200	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27LV020-250	
AM27LV020-300	
AM27LV020B-200	
AM27LV020B-250	
AM27LV020B-300	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27LV020-150	JC, JI
AM27LV020-200	
AM27LV020-250	
AM27LV020-300	
AM27LV020B-200	
AM27LV020B-250	
AM27LV020B-300	

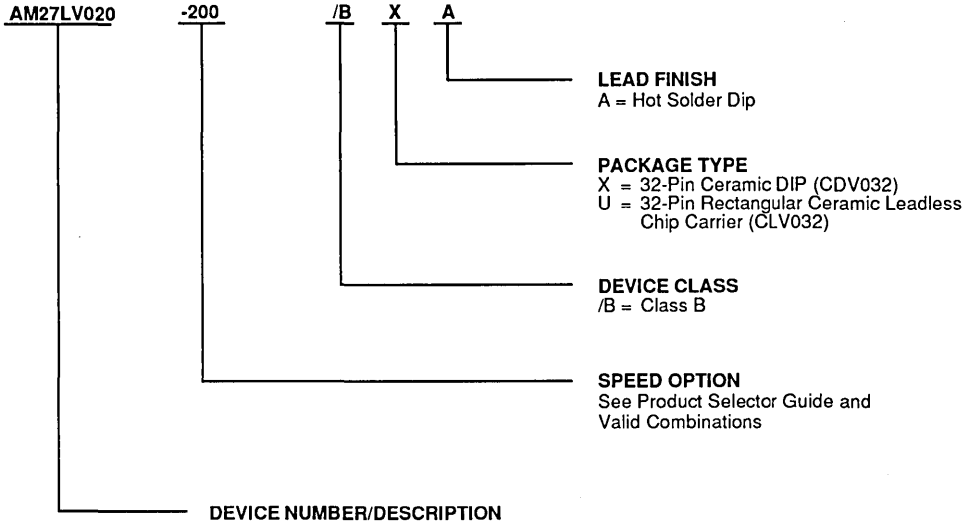
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27LV020-200	/BXA, /BUA
AM27LV020-250	
AM27LV020-300	
AM27LV020B-250	
AM27LV020B-300	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27LV020

In order to clear all locations of their programmed contents, it is necessary to expose the Am27LV020 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27LV020. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Å — with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27LV020 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27LV020, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27LV020 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27LV020

Upon delivery, or after each erasure, the Am27LV020 has all 2,097,152 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27LV020 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ and $\overline{PGM}$ are at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulse and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27LV020. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at V_{CC} = V_{PP} = 5.25 V. Am27LV020 can be programmed using the same algorithm as the 5 V counterpart 27C020.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27LV020s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27LV020 may be common. A TTL low-level program pulse applied to an Am27LV020 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, $\overline{PGM}$ LOW, and $\overline{OE}$ HIGH will program that Am27LV020. A high-level $\overline{CE}$ input inhibits the other Am27LV020s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27LV020.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the Am27LV020. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code, and Byte 1 ($A0 = V_{IH}$), the device identifier code. For the Am27LV020, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27LV020 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27LV020 has a CMOS standby mode which reduces the maximum V_{CC} current to 25 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27LV020 also has a TTL-standby mode which reduces the maximum V_{CC} current to 0.6 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Mixed Power Supply System

Am27LV020 (in 3.0 V to 3.6 V regulated power supply) can be intefaced with 5 V system only when the I/O pins (DQ0–DQ7) are not driven by the 5 V system. V_{IHmax} = V_{CCLV} +2.2 V for address and clock pins and V_{IHmax} =

V_{CCLV} +0.5 V for I/O pins should be followed to avoid CMOS latch-up condition.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		V_{CC} ± 0.3 V	X	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	97H

Notes:

1. *V_H = 12.0 V± 0.5 V*
2. *X can be either V_{IL} or V_{IH}*
3. *A1–A8 = A10–A17 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}:
- All pins except A9, V_{PP}, and V_{CC} (Note 1) ..... −0.6 V to V_{CC} + 0.6 V
- A9 and V_{PP} (Note 2) ..... −0.6 V to 13.5 V
- V_{CC} ..... −0.6 V to 7.0 V

Notes:

1. *During transitions, the input may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.*
2. *During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
- Case Temperature (T_C) ..... −55°C to +125°C

Supply Read Voltages:
- V_{CC} for Am27LV020 ..... +3.0 V to +3.6 V
- V_{CC} for Am27LV020B ..... +2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 2, 3 and 4) (for APL products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
TTL and CMOS Inputs for V_{CC} = 3.0 V to 3.6 V						
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz I_{OUT} = 0 mA (Open Outputs)	C/I Devices		15	mA
			E/M Devices		20	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	TTL		0.6	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	CMOS		25	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
CMOS for V_{CC} = 2.7 V to 3.6 V						
V_{OH}	Output HIGH Voltage	I_{OH} = –20 µA		V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 20 µA			0.1	V
V_{IH}	Input HIGH Voltage			0.7 V_{CC}	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	0.2 V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		5.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		15	mA
			E/M Devices		20	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	TTL		0.6	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			25	µA
I_{PP1}	V_{PP} Supply Current (Read)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27LV020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods less than 20 ns.*

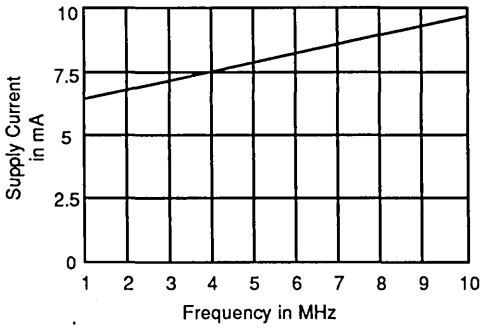


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 3.6 V, T = 25°C

17342A-5

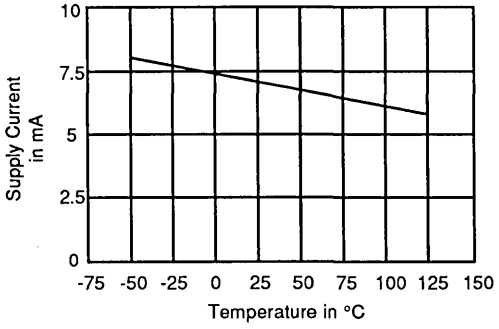


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 3.6 V, f = 5 MHz

17342A-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		PL032		Unit
			Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	9	12	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

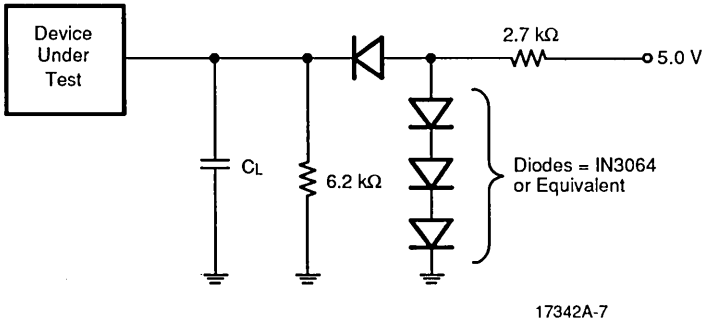
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

PRELIMINARY									
Parameter Symbols		Parameter Description	Test Conditions		Am27LV020/Am27LV020B				
JEDEC	Standard				-150	-200	-250	-300	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min					ns
				Max	150	200	250	300	
t_{ELQV}	t_{CE}	Chip Enable Output Delay	$\overline{OE} = V_{IL}$	Min					ns
				Max	150	200	250	300	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min					ns
				Max	65	75	100	120	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	ns
				Max	50	60	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	ns
				Max					

Notes:

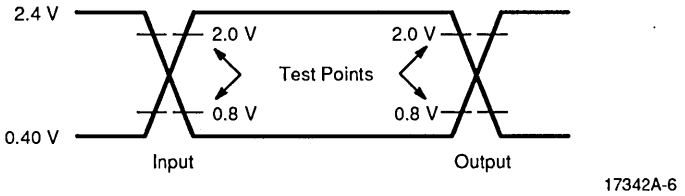
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution**: The Am27LV020 must not be removed from, or inserted into a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF,*
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.40 V to 2.4 V,
   Timing Measurement Reference Level—Inputs: 0.8 V and 2.0 V,
   Outputs: 0.8 V and 2.0 V

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



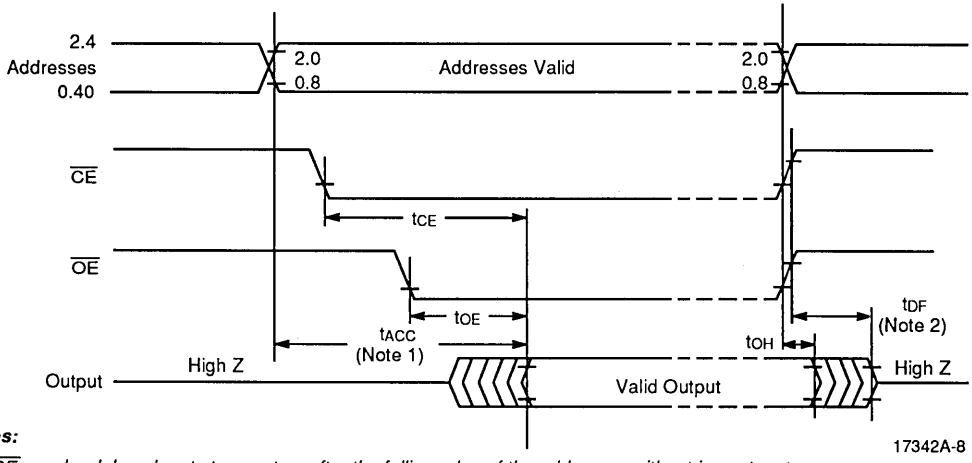
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.40 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORM



17342A-8

Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

PROGRAMMING FLOW CHART

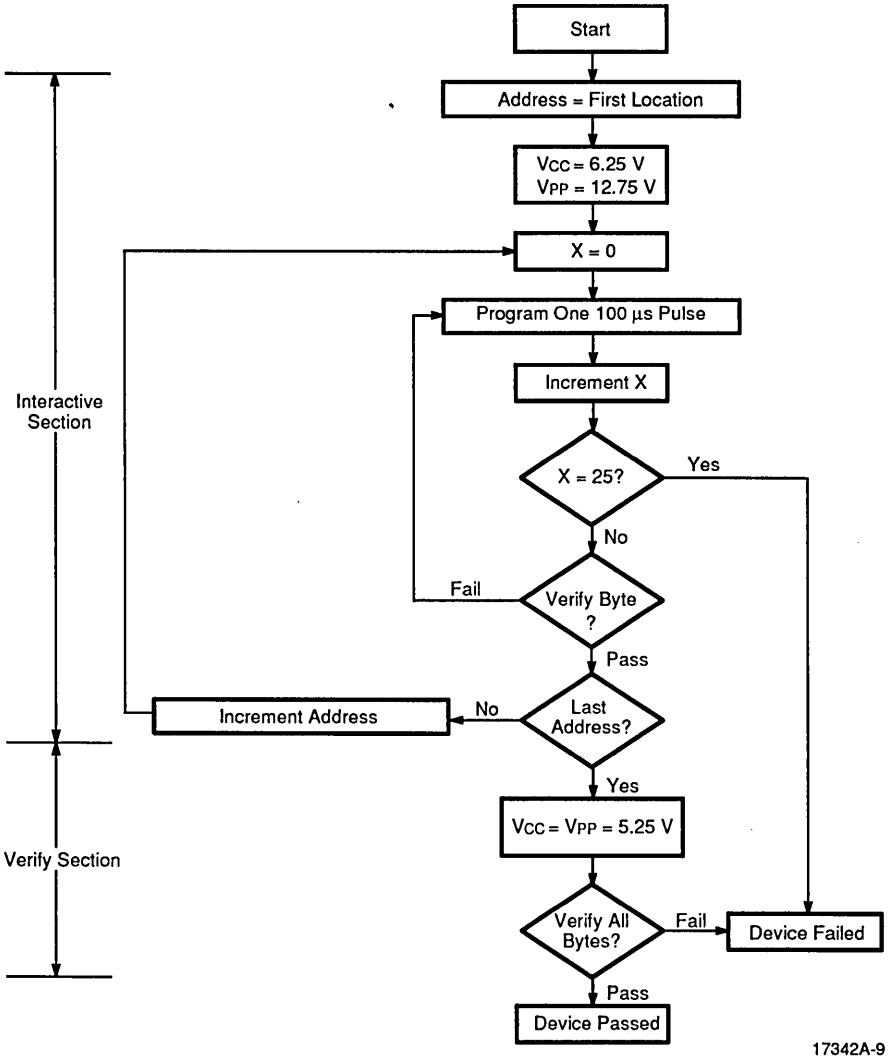


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2 and 3)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		3.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

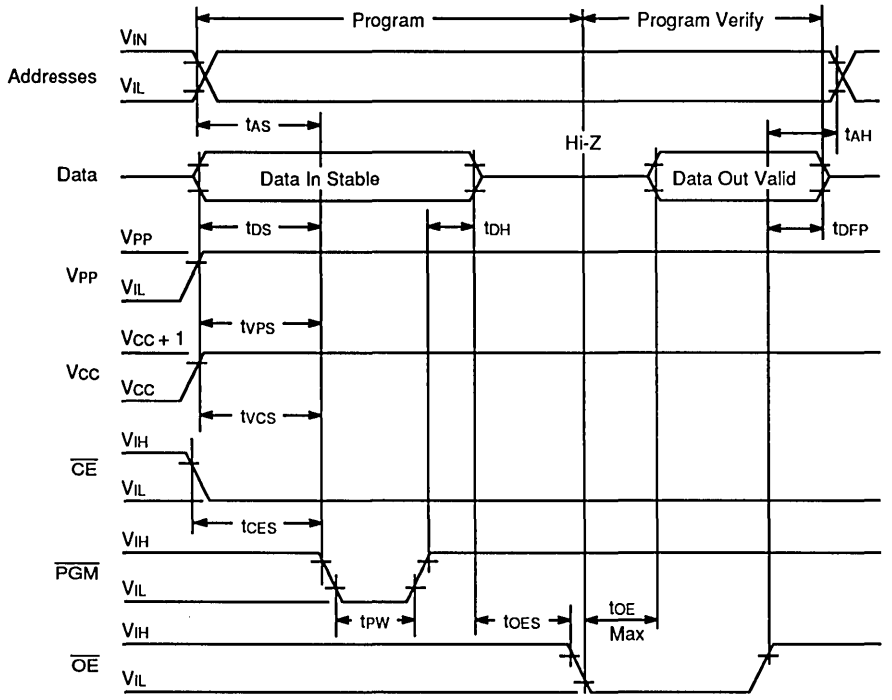
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2 and 3)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *When programming the Am27LV020, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.*
3. *Programming characteristics are sampled but not 100% tested at worst-case conditions.*

INTERACTIVE AND FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 and 2)



17342A-10

Notes:

1. *The input timing reference level is 0.8 V for V_{IL} and 3 V for V_{IH}.*
2. *t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.*

SECTION

5 ExpressROM™ MEMORIES

AN INTRODUCTION TO ExpressROM™ MEMORIES

ExpressROM memories are an exciting product family created by Advanced Micro Devices to offer the system manufacturer lower cost in the manufacturing process. ExpressROM devices are delivered pre-programmed with your stable code in a low cost plastic package and are 100% compatible with the EPROMs they replace. An ExpressROM device is manufactured with the same process as AMD's standard U.V. EPROM equivalent, with the topside passivation layer for plastic encapsulation. Since a standard EPROM die is used, you are assured that the ExpressROM family is identical in architecture, density, and pinout to both AMD's current and future generations of high performance CMOS EPROMs.

ExpressROM devices are inventoried unprogrammed. Upon verification of your code, every device is rigorously tested under both AC and DC operating conditions prior to shipment. Also, because ExpressROM memories are shipped board-ready with factory guaranteed quality, your ship-to-stock or Just-In-Time programs can be easily implemented. At Advanced Micro Devices, we ship them the way you want them—ready for your system. And there are none of the delays, costs or risks normally associated with custom ROMs.

Table 5-1 Non-Volatile Memory Alternatives

	UV EPROM	OTP	ExpressROM Device	ROM
Leadtime	Manufacturer's Leadtime	Manufacturer's Leadtime	2 Weeks	6–10 Weeks
Set-up Charge	No	No	No	Yes
Minimum Quantity	0	0	5K	15–20K
Fully Tested Custom Pattern	No	No	Yes	Yes
User Programming Required	Yes	Yes	No	No
Auto Insertion	No	Yes	Yes	Yes
Flexibility	Reprogrammable	Cannot Reprogram	Fixed 2 Weeks Prior to Use	Fixed 6–10 Weeks Prior to Use

Plastic packaging inherently provides a cost savings over standard EPROMs packaged in expensive windowed ceramic DIPs. However, component price is only a small part of your true in-system cost. ExpressROM devices allow you to eliminate or reduce costs in several other areas: programming, testing, labeling and production. Since ExpressROM memories are delivered with your code, you will reap savings by eliminating programming costs and associated yield losses. Incoming inspection may often be eliminated since your ExpressROM devices have been thoroughly tested and are guaranteed to operate to full specifications with your code! Additional in-house cost savings can be attained by using automatic insertion equipment in lieu of manual placement into sockets.

ExpressROM devices were designed to provide a low cost alternative for EPROM users without the liabilities of other non-volatile memory alternatives. Although ROMs have a

lower component cost, they are economically feasible only at high volume and have the risks of long leadtimes and limited manufacturing flexibility. While OTP EPROMs offer the systems manufacturer the ability to respond to varying codes during production, they force the user to incur additional and hidden costs.

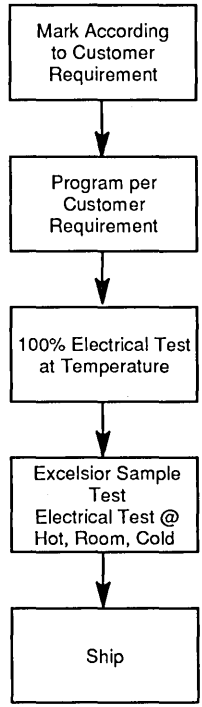
ExpressROM Memories Lower Cost

ExpressROM memories eliminate or reduce costs in several areas. These include programming, testing, marking and labeling. Standard programming of blank devices may reveal other hidden expenses such as costs associated with possible programming yield losses, capacity constraints, labels and other supplies, rework, inventory and associated queue time, handling, maintenance, labor and personnel, transit costs, inspections, floor space and other overhead. AMD's ExpressROM memories add value by eliminating or reducing all these costs in your system manufacturing environment.

Our mission at AMD is to deliver you the services and products you demand to build the cost competitive systems you need to win in your markets. The ExpressROM memory provides this opportunity. As one of the world's five largest IC manufacturers and the first to market with a 1 Mbit EPROM, we appreciate the value of efficient manufacturing. Compressing time-to-market cycles, improving yields and providing high levels of quality are invaluable strategies for today's manufacturer. At Advanced Micro Devices we are proud to offer another tool to give our customers this strategic advantage, the ExpressROM Memory: the ROM without the wait!

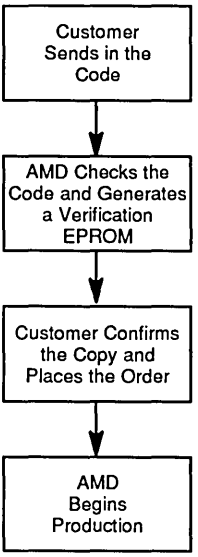
ExpressROM Memory Flow

AMD's OTP EPROM devices are taken from inventory in our off-shore testing facility and processed as shown.



ORDERING ExpressROM DEVICES

The following procedure outlines the method for ordering an ExpressROM device. For more information, contact your local AMD sales representative.



1) Send in the Code

Please have your field sales representative provide you with the latest version of the ExpressROM Code Approval Form (see Page 5-7). This form will provide all the necessary information required for processing your order. After receiving this form, fill out the Code Transmittal and Ordering Information sections. Then send the form with two (2) master copies of each code being ordered to your field sales representative. To minimize the verification turn-around process, supply two master copies of each code using standard EPROMs identical in architecture and density as the ExpressROM device being ordered. Two master copies per code are required in order to guarantee proper code transmission. Please be sure the checksum is clearly identified on each master EPROM.

2) AMD Checks the Code and Generates a Verification EPROM

We check that both EPROMs contain the same code to make certain there was not a mix-up in shipping your codes to the factory as well as ensuring that the integrity of your code has been preserved. After confirming this, a unique 5-digit code designation is assigned. The AMD part number is formed by adding the 5-digit code designation as a suffix to the ExpressROM Device number. See below:

Am27X010–105JC X X X X X

DEVICE NUMBER — CODE DESIGNATION

AMD then logs in your code with the 5-digit code designation and generates a verification EPROM. The verification EPROM along with one of your master EPROMs and the ExpressROM Code Approval Form should be back in your hand for final approval within 2-3 days. The other master EPROM remains at AMD for our records. Please note: the verification EPROM is simply a means of transferring the code and is not necessarily indicative of the ExpressROM product being ordered.

3) Confirm the Copy and Place the Order

Once the verification EPROM is approved, sign the Approval Section of the ExpressROM Code Approval Form and return it to AMD with your purchase order. Upon receipt of the signed form and a purchase order, AMD enters the order and begins production. Logged codes are maintained for 60 days and then deleted if there is no purchase order placed.

TERMS AND CONDITIONS

You should be aware of the following when ordering ExpressROM devices.

1) AMD will maintain customer code confidentiality.
2) AMD will absorb all initial set-up costs.
3) All orders are subject to minimum quantities. The minimum quantity for initial orders is 5,000 pieces.
4) AMD may begin production 14 days in advance of the AMD scheduled ship date covered by a purchase order and requires 14 days minimum notification from the AMD scheduled ship date for code changes. The customer is liable for all work-in-process covered by the same purchase order.
5) No schedule changes may be made within 14 days of AMD scheduled ship date.
6) All unpackaged die product procured by the customer is for use exclusively in the customer's end products. Any other use of die product must be approved in writing by AMD.
7) Code changes with Work-In-Process will require additional charges and may affect delivery schedules.
8) All other terms and conditions which normally apply to AMD's EPROMs (if any) also apply with AMD's ExpressROM memories.

ExpressROM™ Code Approval Form

CODE TRANSMITTAL AND ORDERING INFORMATION SECTION Rev. 7 11/05/92

Please complete items 1 thru 9. To minimize the verification turn-around process, supply 2 master copies of each code using EPROMs of the same architecture and density as the ExpressROM™ Device being ordered. Also, be sure the checksum is clearly identified on each master EPROM.

CODE TRANSMITTAL SECTION

1. Company Name: _____ 2. Date: _____

3. Incoming Master's Part #: _____ 4. Master's Checksum: _____

ORDERING INFORMATION SECTION

Please check the appropriate ExpressROM™ Memory data sheet for valid combinations and mark appropriate boxes below:

5. Part #:

❑ Am27X64	❑ -55	❑ -70	❑ -90	❑ -120	❑ -150	❑ -200	❑ -255
❑ Am27X128	❑ -55	❑ -70	❑ -90	❑ -120	❑ -150	❑ -200	❑ -255
❑ Am27X256	❑ -55	❑ -70	❑ -90	❑ -120	❑ -150	❑ -200	❑ -255
❑ Am27X512		❑ -75	❑ -90	❑ -120	❑ -150	❑ -200	❑ -255
❑ Am27X010			❑ -105	❑ -120	❑ -150	❑ -200	❑ -255
❑ Am27X1024			❑ -90	❑ -120	❑ -150	❑ -200	❑ -255
❑ Am27X020				❑ -120	❑ -150	❑ -200	❑ -255
❑ Am27X048				❑ -120	❑ -150	❑ -200	❑ -255
❑ Am27X040				❑ -120	❑ -150	❑ -200	❑ -255
❑ Am27X400				❑ -120	❑ -150	❑ -200	❑ -255
❑ Am27X4096				❑ -120	❑ -150	❑ -200	❑ -255

6. Package and Temperature:

❑ Plastic DIP ❑ Commercial (0°C to +70°C)
❑ PLCC ❑ Industrial (–40°C to +85°C)
❑ TSOP Standard Pinout
❑ TSOP Reverse Pinout
❑ Other _____

7. AMD Standard Part Number: _____

8. Customer Ordering Part Number: _____

9. Please indicate the exact marking and complete the blank sections (11 characters per line including spaces, © = 2 spaces if required).

AMD Logo
ExpressROM™

_____

_____

_____

Date Code

APPROVAL SECTION TERMS AND CONDITIONS

AMD will maintain customer code confidentiality. AMD will absorb all initial set-up costs.
AMD may begin production 14 days in advance of the AMD scheduled ship date covered by a purchase order and requires 14 days minimum notification from the AMD scheduled ship date for code changes.
The customer is liable for all work-in-process covered by the same purchase order.
No schedule changes may be made within 14 days of AMD scheduled ship date.
All unpackaged die product procured by the customer is for use exclusively in the customer's end products.
Any other use of die product must be approved in writing by AMD.
All orders are subject to minimum quantities.
Code changes with Work In Process will require additional charges and may affect delivery schedules.

AMD Standard Part #: Am27X _____ Approved Checksum: _____

Customer Signature: _____ Date: _____

Name (Print): _____ Title: _____

FINAL

Am27X64

64 Kilobit (8,192 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 55 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP), and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

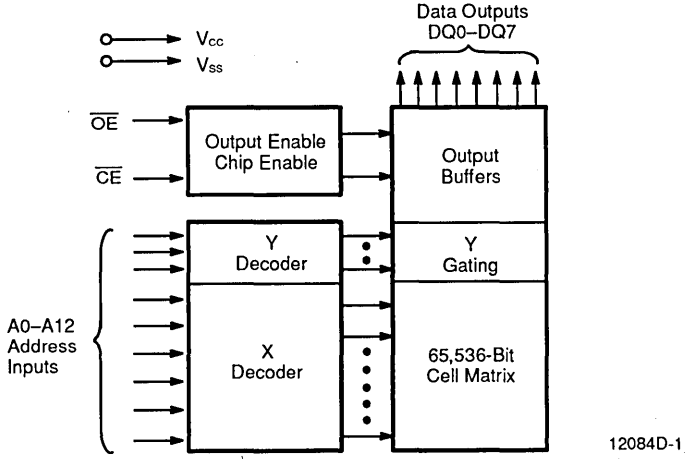
GENERAL DESCRIPTION

The Am27X64 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 8,192 by 8 bits and is available in plastic dual in-line (PDIP) as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 55 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X64 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



12084D-1

Publication# 12084 Rev. D Amendment/0
Issue Date: July 1993

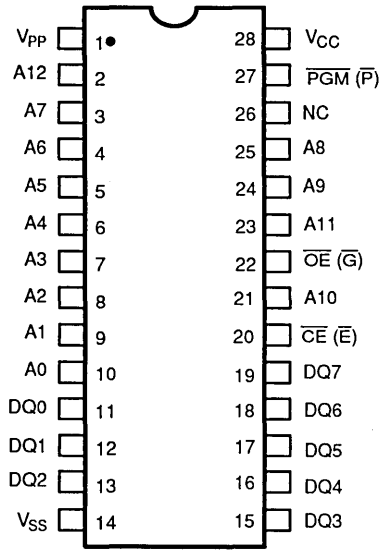
PRODUCT SELECTOR GUIDE

Family Part No	Am27X64						
Ordering Part No: V_{CC} ±5%							-255
V_{CC} ±10%	-55	-70	-90	-120	-150	-200	
Max Access Time (ns)	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	40	40	50	65	75	100

CONNECTION DIAGRAMS

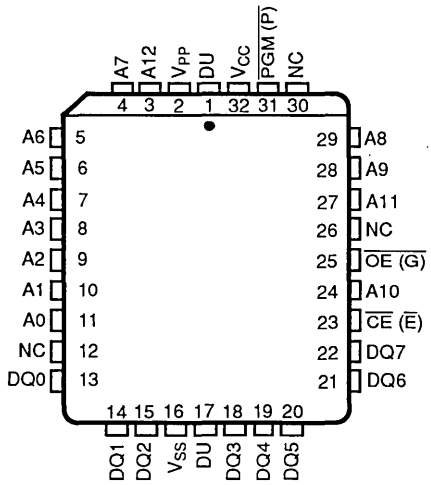
Top View

PDIP



12084D-2

PLCC



12084D-3

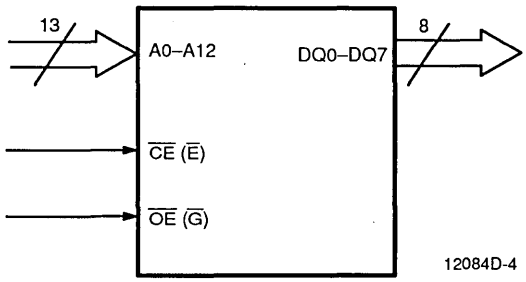
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A12 = Address Inputs
$\overline{CE}$ ($\overline{E}$) = Chip Enable Input
DQ0–DQ7 = Data Inputs/Outputs
DU = No External Connection (Do Not Use)
NC = No Internal Connection
$\overline{OE}$ ($\overline{G}$) = Output Enable Input
$\overline{PGM}$ ($\overline{P}$) = Program Enable Input
V_{CC} = V_{CC} Supply Voltage
V_{PP} = Program Supply Voltage
V_{SS} = Ground

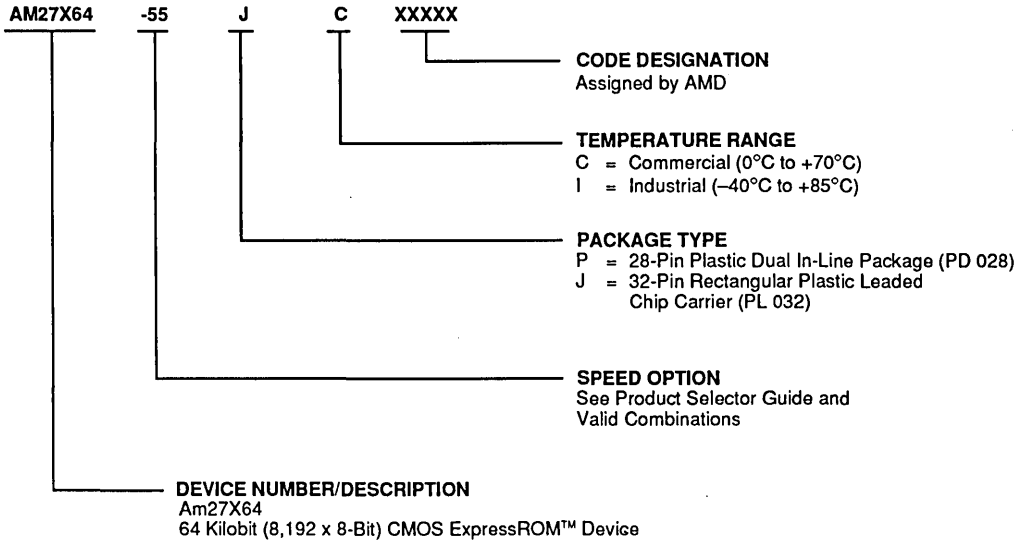
LOGIC SYMBOL



12084D-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X64-55	PC, JC, PI, JI
AM27X64-70	
AM27X64-90	
AM27X64-120	
AM27X64-150	
AM27X64-200	
AM27X64-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X64 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}–t_{OE}.

Standby Mode

The Am27X64 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X64 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	DOUT
Output Disable	X	V_{IH}	X	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	X	Hi-Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to Vss
All pins except Vcc ..... −0.6 V to Vcc + 0.6 V

Vcc ..... −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (Tc) ..... −40°C to +85°C

Supply Read Voltages
Vcc for Am27X64-255 ..... +4.75 V to +5.25 V

Vcc for all other valid ..... +4.50 V to +5.50 V
combinations

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC}+0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		1.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 10 MHz, $I_{OUT} = 0$ mA		25	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27X64 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V during transactions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods less than 20 ns.*

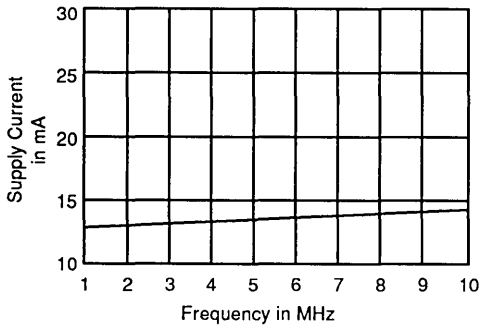


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

12084D-5

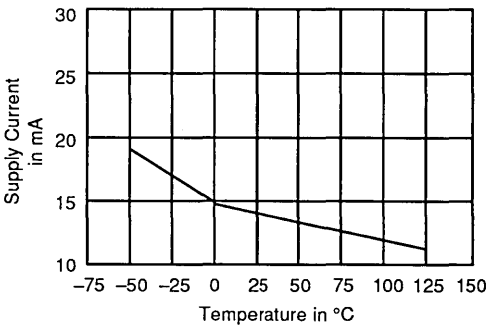


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

12084D-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 028		PL 032		Unit
			Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	5	10	10	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	10	11	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X64							Unit
JEDEC	Standard				-55	-70	-90	-120	-150	-200	-255	
t_{AVQV}	t_{RCC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	ns
				Max	55	70	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	ns
				Max	55	70	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	–	–	ns
				Max	35	40	40	50	50	50	50	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	0	0	ns
				Max	25	25	25	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	0	ns
				Max	–	–	–	–	–	–	–	

Notes:

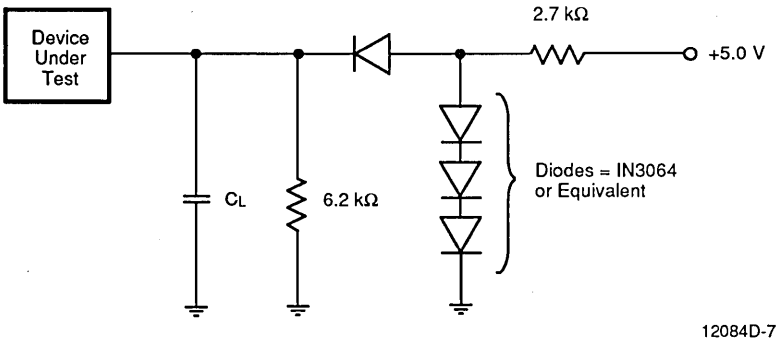
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X64 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *For the -55 and -70*

   Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

   For all other versions

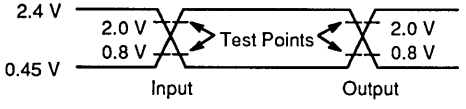
   Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT

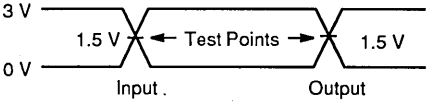


C_L = 100 pF including jig capacitance (30 pF for -55 and -70)

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



12084D-8

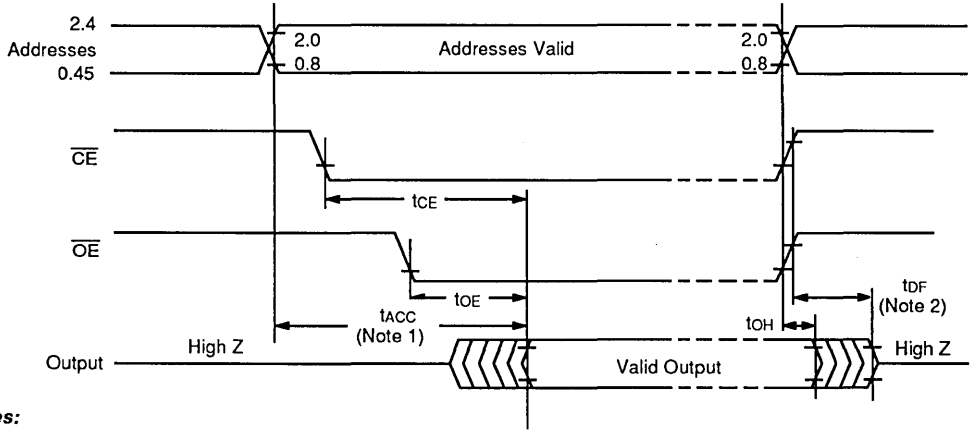
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -55 and -70.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

12084D-9

FINAL

Am27X128

128 Kilobit (16,384 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 55 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

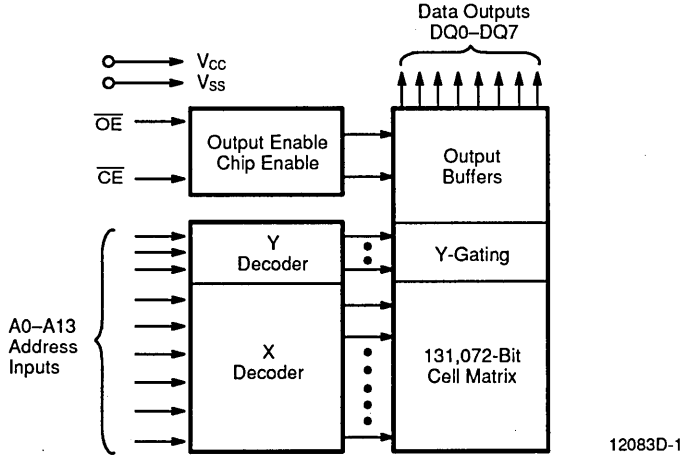
GENERAL DESCRIPTION

The Am27X128 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 16,384 by 8 bits and is available in plastic dual in-line (PDIP) as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 55 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X128 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



12083D-1

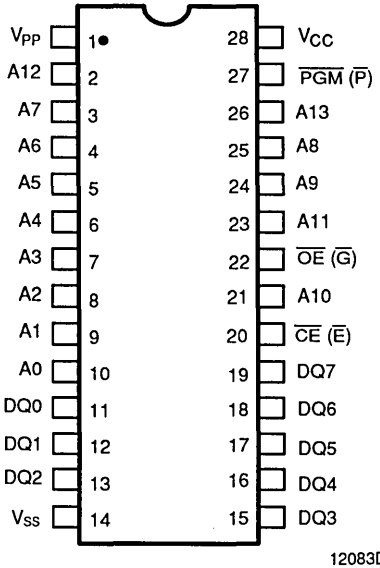
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X128						
Ordering Part No: Vcc ±5%							-255
Vcc ±10%	-55	-70	-90	-120	-150	-200	
Max Access Time (ns)	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	40	40	50	65	75	100

CONNECTION DIAGRAMS

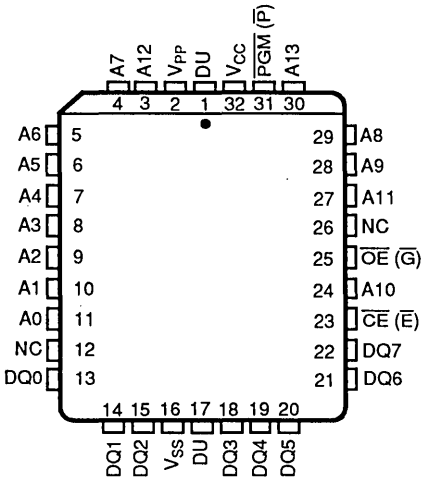
Top View

PDIP



12083D-2

PLCC



12083D-3

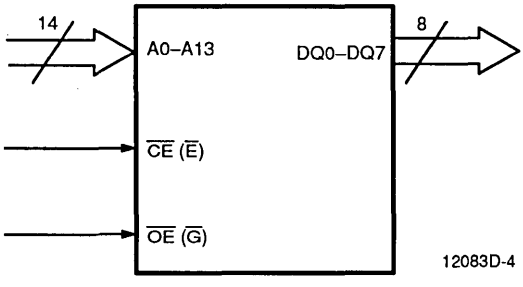
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A13 = Address Inputs
$\overline{CE}$ ($\overline{E}$) = Chip Enable Input
DQ0–DQ7 = Data Inputs/Outputs
DU = No External Connection (Do Not Use)
NC = No Internal Connection
$\overline{OE}$ ($\overline{G}$) = Output Enable Input
$\overline{PGM}$ ($\overline{P}$) = Program Enable Input
Vcc = Vcc Supply Voltage
VPP = Program Supply Voltage
VSS = Ground

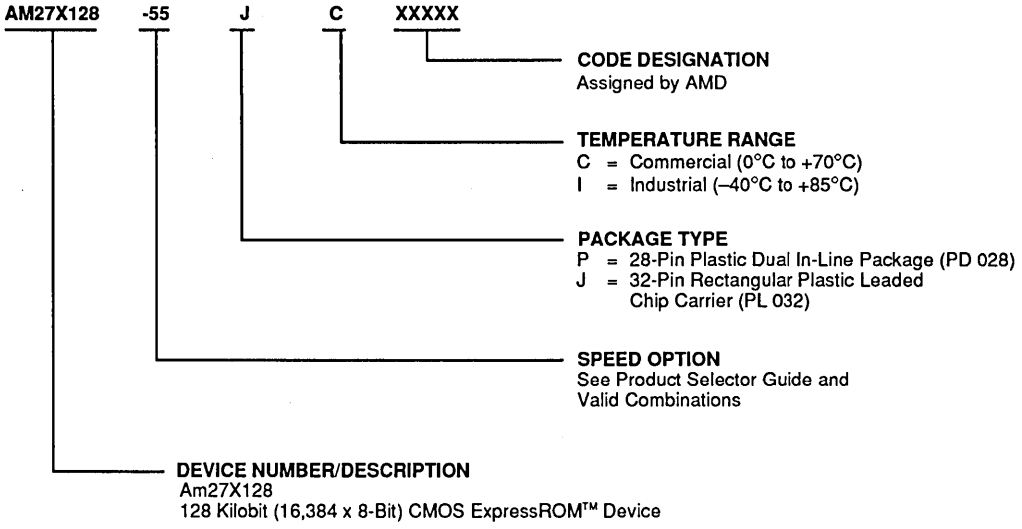
LOGIC SYMBOL



12083D-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X128-55	PC, JC, PI, JI
AM27X128-70	
AM27X128-90	
AM27X128-120	
AM27X128-150	
AM27X128-200	
AM27X128-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X128 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable $\overline{OE}$ is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}–t_{OE}.

Standby Mode

The Am27X128 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X128 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	DOUT
Output Disable	X	V_{IH}	X	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	X	Hi-Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
All pins except V_{CC} ..... −0.6 V to V_{CC} + 0.6 V

V_{CC} ..... −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (Tc) ..... −40°C to +85°C

Supply Read Voltages
V_{CC} for Am27X128-255 ..... +4.75 V to +5.25 V

V_{CC} for all other
valid combinations ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC}+0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		1.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 10 MHz, $I_{OUT} = 0$ mA		25	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27X128 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

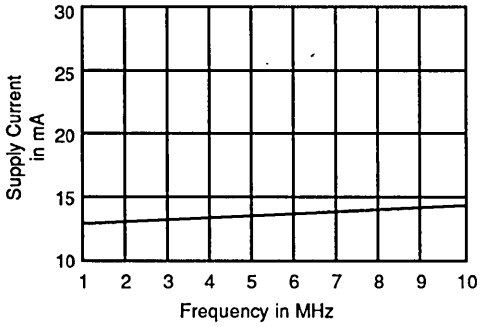


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

12083D-5

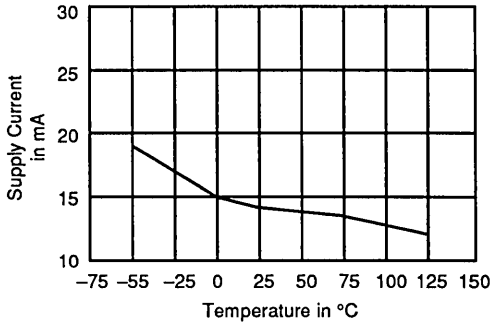


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

12083D-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 028		PL 032		Unit
			Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	5	10	10	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	10	11	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X128							Unit
JEDEC	Standard				-55	-70	-90	-120	-150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	ns
				Max	55	70	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	ns
				Max	55	70	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	–	–	ns
				Max	35	40	40	50	50	50	50	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	0	0	ns
				Max	25	25	25	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	0	ns
				Max	–	–	–	–	–	–	–	

Notes:

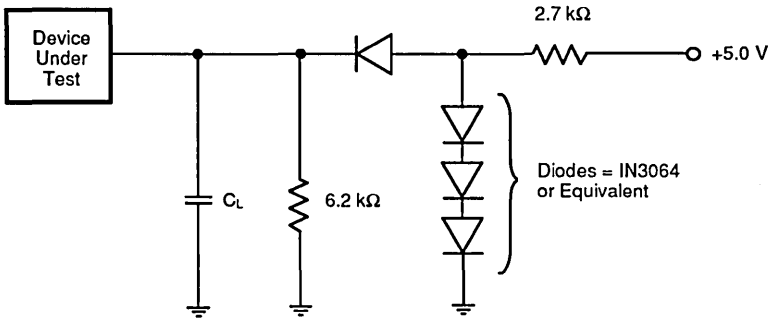
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X128 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *For the -55 and -70:*

   Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

   For all other versions:

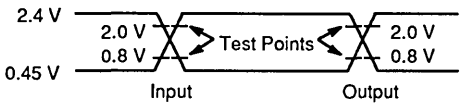
   Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT

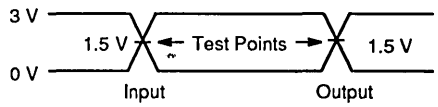


C_L = 100 pF including jig capacitance (30 pF for -55 and -70)

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



12083D-8

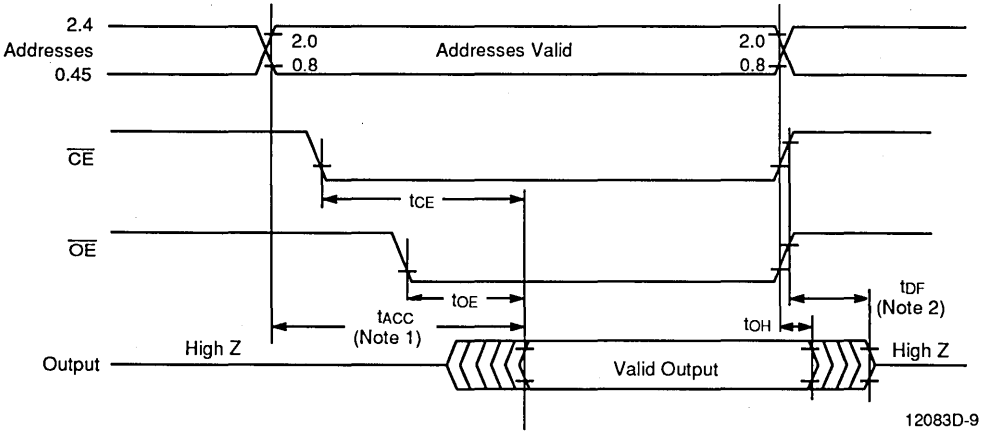
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -55 and -70.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



12083D-9

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.

2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

FINAL

Am27X256

256 Kilobit (32,768 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 55 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP), Plastic Leaded Chip Carrier (PLCC), and Thin Small Outline Package (TSOP)**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

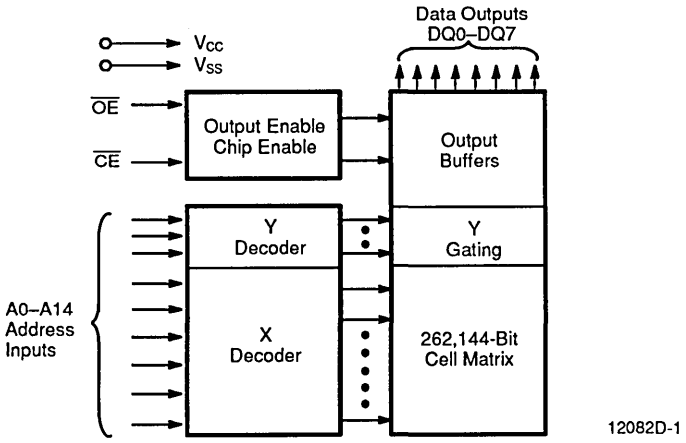
GENERAL DESCRIPTION

The Am27X256 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 32,768 by 8 bits and is available in plastic dual in-line (PDIP), plastic leaded chip carrier (PLCC), and thin small outline (TSOP) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 55 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X256 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



12082D-1

Publication# 12082 Rev. D Amendment/0
Issue Date: July 1993

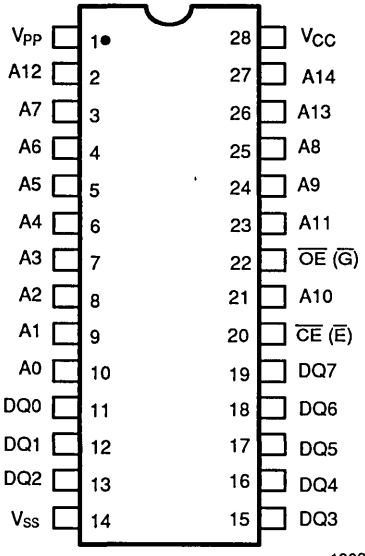
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X256						
Ordering Part No: V_{CC} ±5%							-255
V_{CC} ±10%	-55	-70	-90	-120	-150	-200	
Max Access Time (ns)	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	40	40	50	65	75	100

CONNECTION DIAGRAMS

Top View

PDIP



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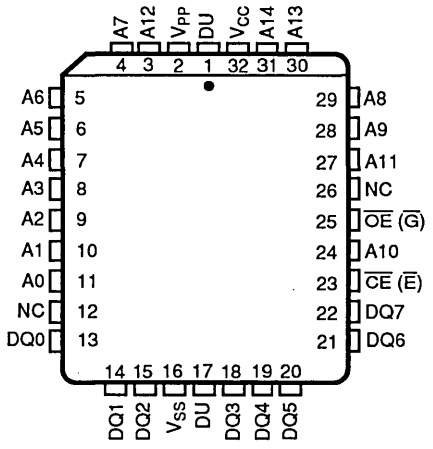
PLCC

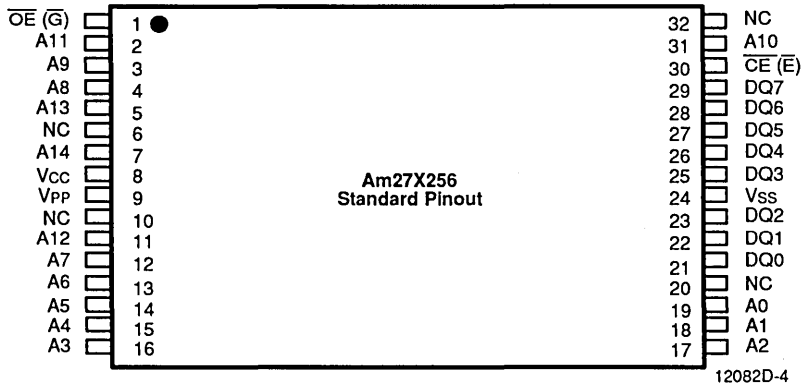


12082D-3

Notes:

1. JEDEC nomenclature is in parentheses.

TSOP*

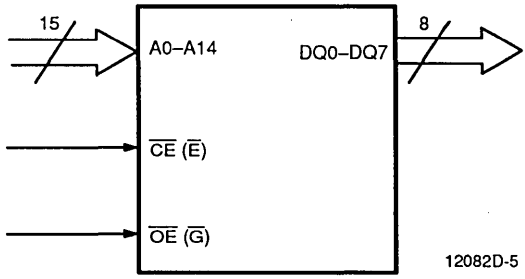


Contact local AMD sales office for package availability

PIN DESIGNATIONS

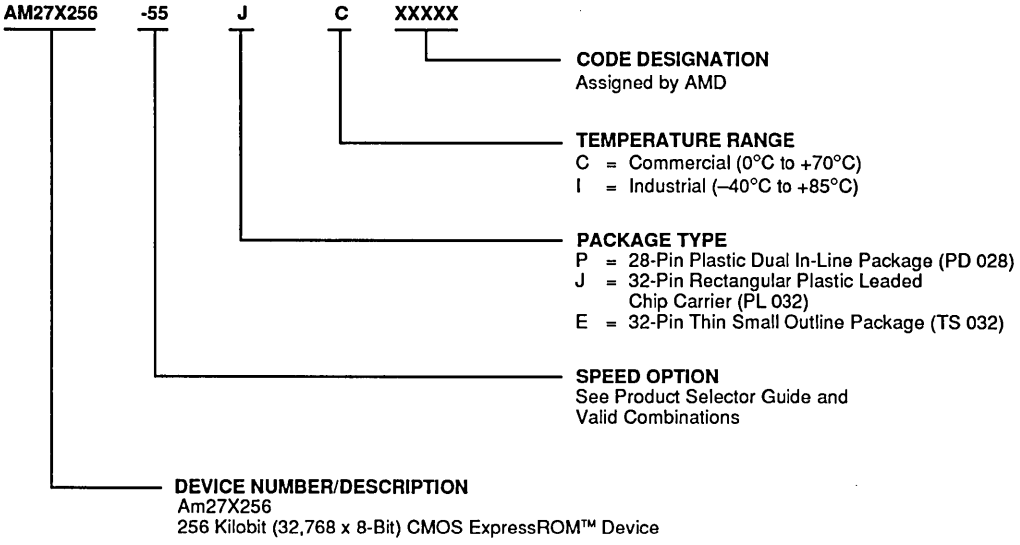
A0–A14	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0–DQ7	=	Data Inputs/Outputs
DU	=	No External Connection (Do Not Use)
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

LOGIC SYMBOL



ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X256-55	PC, JC, PI, JI, EC, EI
AM27X256-70	
AM27X256-90	
AM27X256-120	
AM27X256-150	
AM27X256-200	
AM27X256-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X256 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X256 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	DOUT
Output Disable	X	V_{IH}	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	Hi-Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
All pins except V_{CC} ..... −0.6 V to V_{CC} + 0.6 V

V_{CC} ..... −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) ..... −40°C to +85°C

Supply Read Voltages
V_{CC} for Am27X256-255 ..... +4.75 V to +5.25 V

V_{CC} for all other
valid combinations ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC}+0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		1.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 10 MHz, $I_{OUT} = 0$ mA		25	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** the Am27X256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

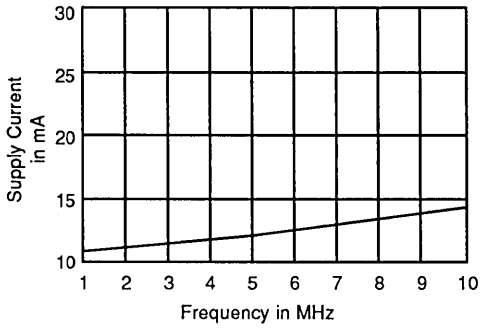


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

12082D-6

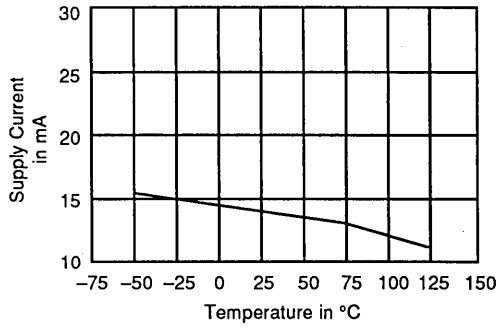


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

12082D-7

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 028		PL 032		TS 032		Unit
			Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	6	10	8	12	10	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	10	8	12	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X256							Unit
JEDEC	Standard				-55	-70	-90	-120	-150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	ns
				Max	55	70	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	ns
				Max	55	70	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	–	–	ns
				Max	35	40	40	50	50	50	50	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	0	0	ns
				Max	25	25	25	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	0	ns
				Max	–	–	–	–	–	–	–	

Notes:

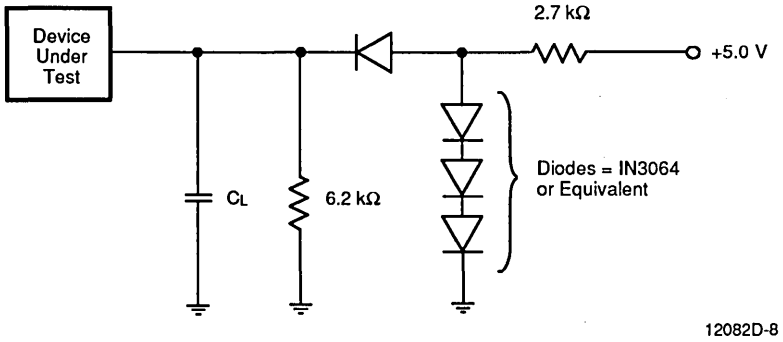
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X256 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *For the -55 and -70:*

   Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

   For all other versions:

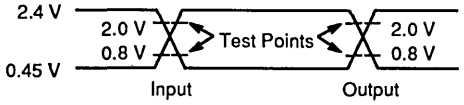
   Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT

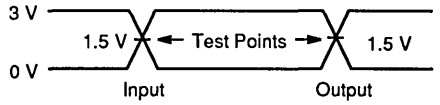


C_L = 100 pF including jig capacitance (30 pF for -55 and -70)

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



12082D-9

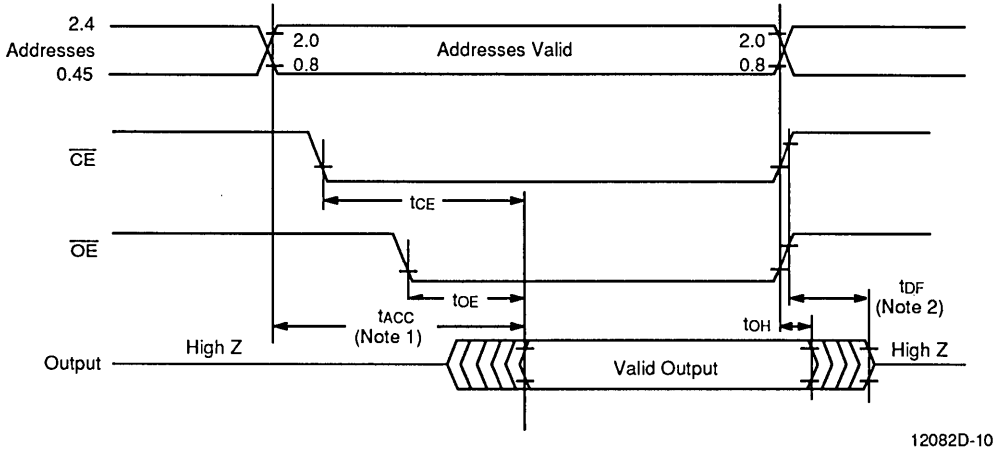
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -55 and -70.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



12082D-10

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.

2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

FINAL

Am27X512

512 Kilobit (65,536 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 90 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

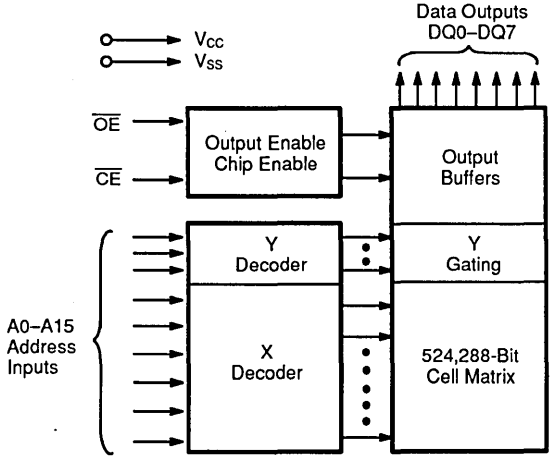
GENERAL DESCRIPTION

The Am27X512 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 65,536 by 8 bits and is available in plastic dual in-line (PDIP), plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 90 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X512 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



12081D-1

Publication# 12081 Rev. D Amendment/0
Issue Date: July 1993

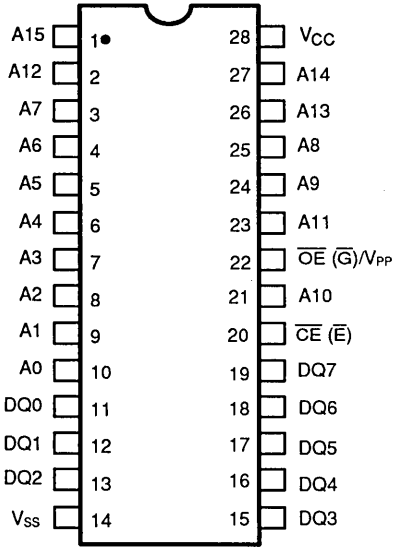
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X512				
Ordering Part No: $V_{CC} \pm 5\%$					-255
$V_{CC} \pm 10\%$	-90	-120	-150	-200	
Max Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	65	75	100

CONNECTION DIAGRAMS

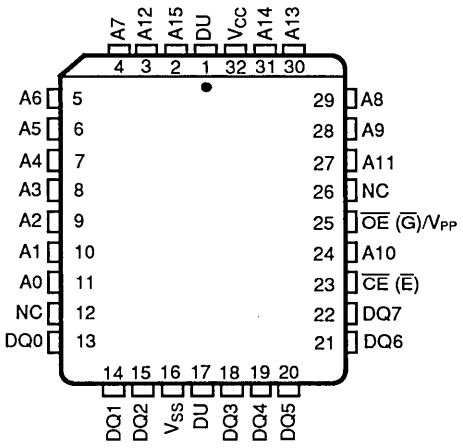
Top View

PDIP



12081D-2

PLCC



12081D-3

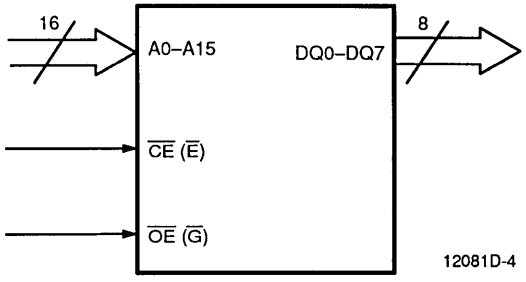
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A15 = Address Inputs
$\overline{CE}$ ($\overline{E}$) = Chip Enable Input
DQ0–DQ7 = Data Inputs/Outputs
DU = No External Connection (Do Not Use)
NC = No Internal Connection
$\overline{OE}$ ($\overline{G}$) = Output Enable Input
V_{CC} = Vcc Supply Voltage
V_{PP} = Program Supply Voltage
V_{SS} = Ground

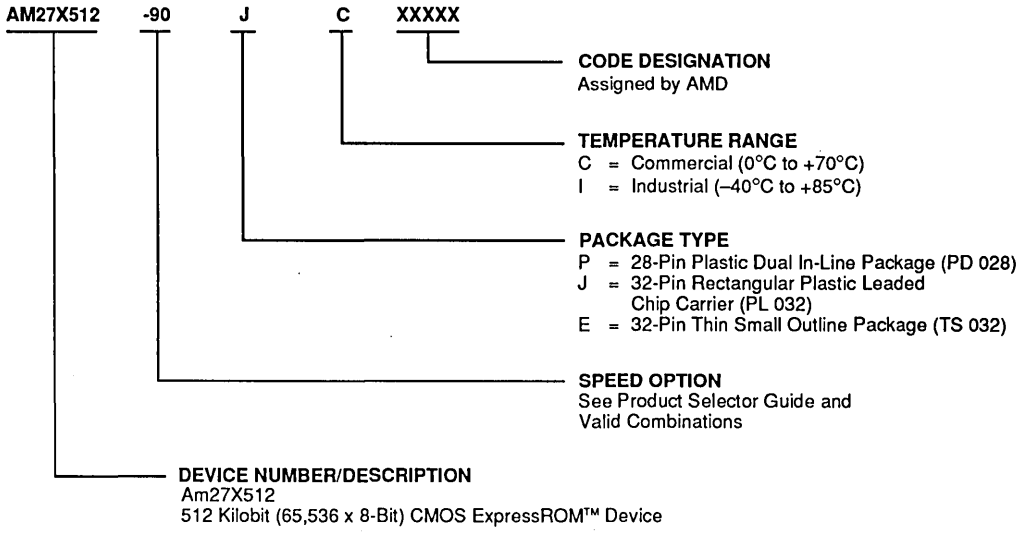
LOGIC SYMBOL



12081D-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X512-90	PC, JC, PI, JI, EC, EI
AM27X512-120	
AM27X512-150	
AM27X512-200	
AM27X512-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable $\overline{OE}$ is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X512 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X512 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}/V_{PP}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}/V_{PP}$	Outputs
Read	V_{IL}	V_{IL}	DOUT
Output Disable	X	V_{IH}	Hi-Z
Standby (TTL)	V_{IH}	X	Hi-Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
All pins except V_{CC} ..... −0.6 V to V_{CC} + 0.6 V

V_{CC} ..... −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) ..... −40°C to +85°C

Supply Read Voltages
V_{CC} for Am27X512-255 ..... +4.75 V to +5.25 V

V_{CC} for all other
valid combinations ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC}+0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		1.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 10 MHz, $I_{OUT} = 0$ mA		30	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** the Am27X512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

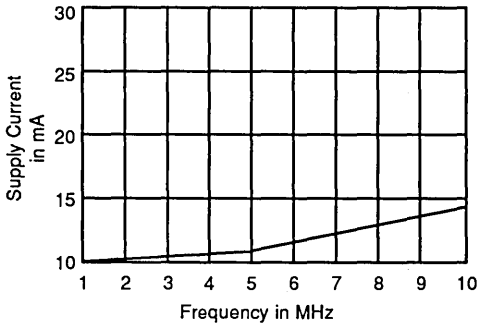


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

12081D-5

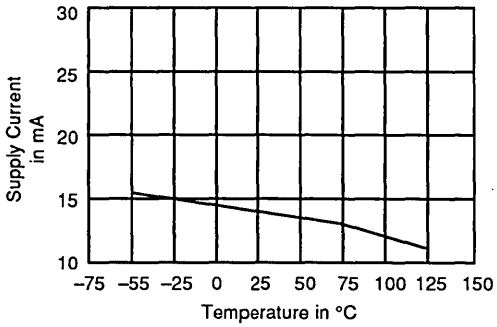


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

12081D-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 028		PL 032		TS 032		Unit
			Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	6	10	9	12	10	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	10	9	12	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

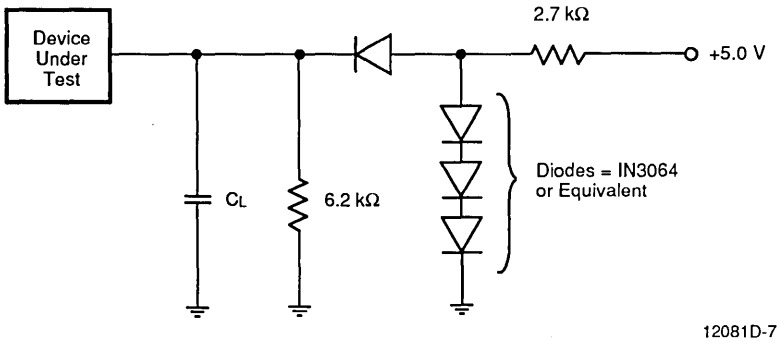
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X512					Unit
JEDEC	Standard				-90	-120	-150	-200	-255	
t_{AVQV}	t_{RCC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	ns
				Max	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	ns
				Max	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	ns
				Max	40	50	50	50	50	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	ns
				Max	30	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	ns
				Max	–	–	–	–	–	

Notes:

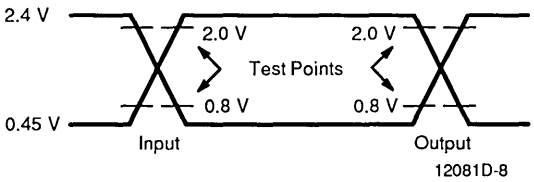
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X512 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



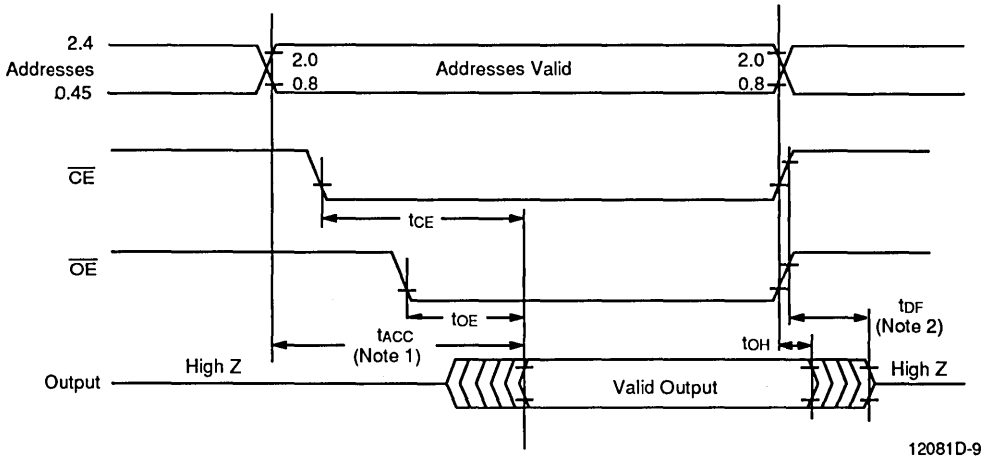
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are < 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



12081D-9

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.

2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

FINAL

Am27X010

1 Megabit (131,072 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 105 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **± 10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP), Plastic Leaded Chip Carrier (PLCC), and Thin Small Outline Package (TSOP)**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

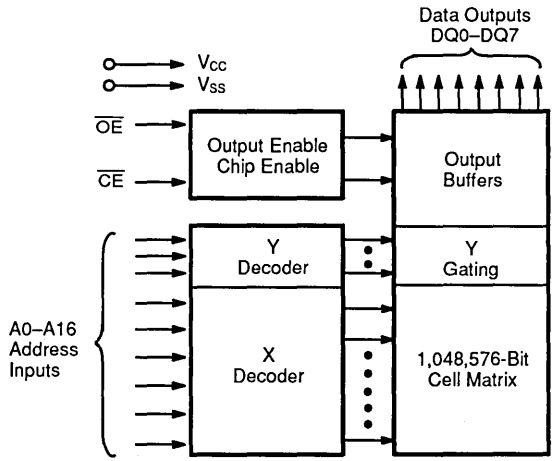
GENERAL DESCRIPTION

The Am27X010 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 131,072 by 8 bits and is available in plastic dual in-line (PDIP), plastic leaded chip carrier (PLCC) and thin small outline (TSOP) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 105 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X010 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



12080D-1

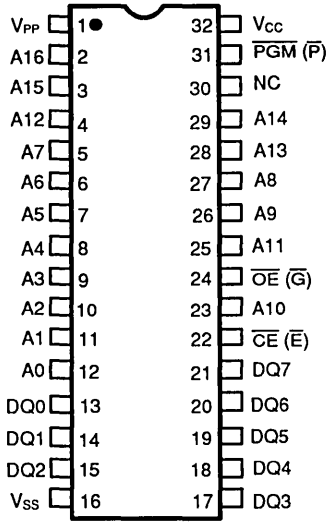
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X010				
Ordering Part No: V_{CC} ±5%	-105				-255
V_{CC} ±10%		-120	-150	-200	
Max Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	50	65	75	100

CONNECTION DIAGRAMS

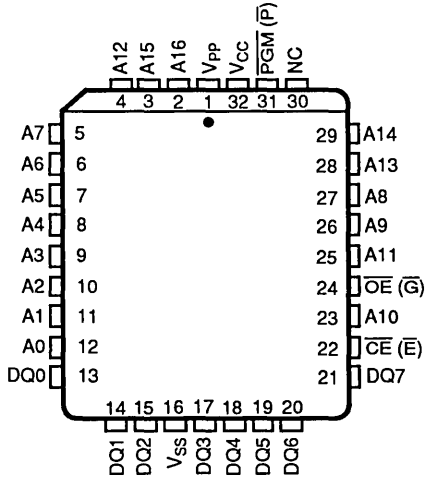
Top View

PDIP



12080D-2

PLCC

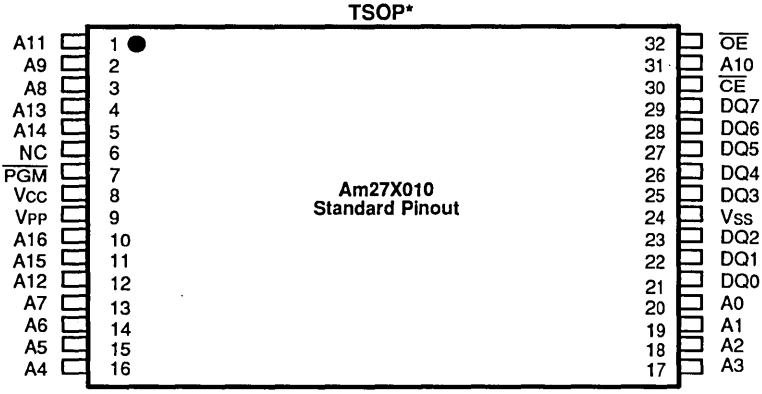


12080D-3

Notes:

1. JEDEC nomenclature is in parentheses.

TSOP*



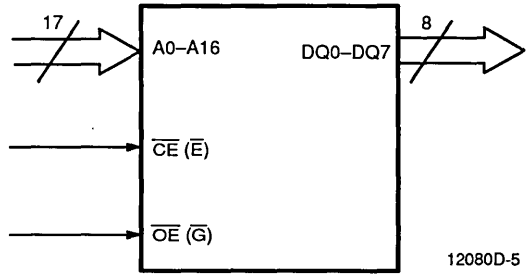
Contact local AMD sales office for package availability

12080D-4

PIN DESIGNATIONS

A0–A16	= Address Inputs
$\overline{CE}$ ($\overline{E}$)	= Chip Enable Input
DQ0–DQ7	= Data Inputs/Outputs
DU	= No External Connection (Do Not Use)
NC	= No Internal Connection
$\overline{OE}$ ($\overline{G}$)	= Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	= Enable Input
Vcc	= Vcc Supply Voltage
VPP	= Program Supply Voltage
Vss	= Ground

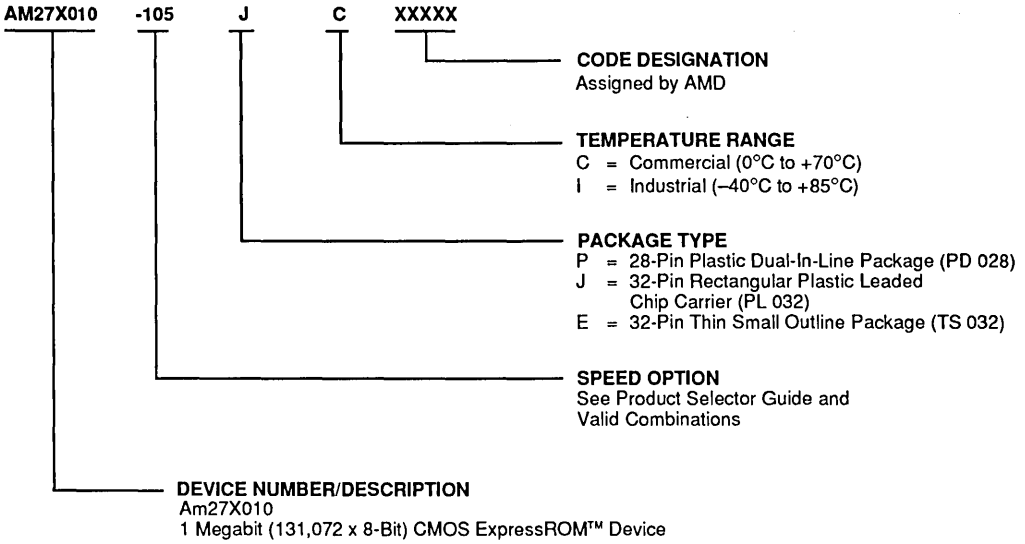
LOGIC SYMBOL



12080D-5

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X010-105	PC, JC, PI, JI, EC, EI
AM27X010-120	
AM27X010-150	
AM27X010-200	
AM27X010-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{CE}$.

Standby Mode

The Am27X010 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X010 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on Express-ROM device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	DOUT
Output Disable	X	V_{IH}	X	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	X	Hi-Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
All pins except V_{CC} ..... −0.6 V to V_{CC} + 0.6 V

V_{CC} ..... −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices

Case Temperature (Tc) ..... −40°C to +85°C

Supply Read Voltages

V_{CC} for Am27X010-XX5 ..... +4.75 V to +5.25 V

V_{CC} for Am27X010-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC}+0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		10	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA		30	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27X010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

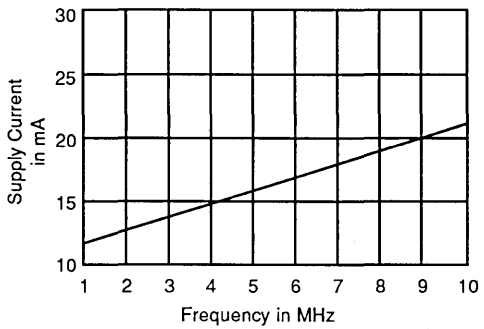


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

12080D-6

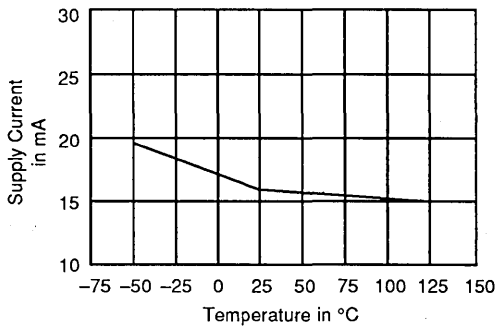


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

12080D-7

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 032		PL 032		TS 032		Unit
			Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	8	12	8	10	10	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	11	14	11	12	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

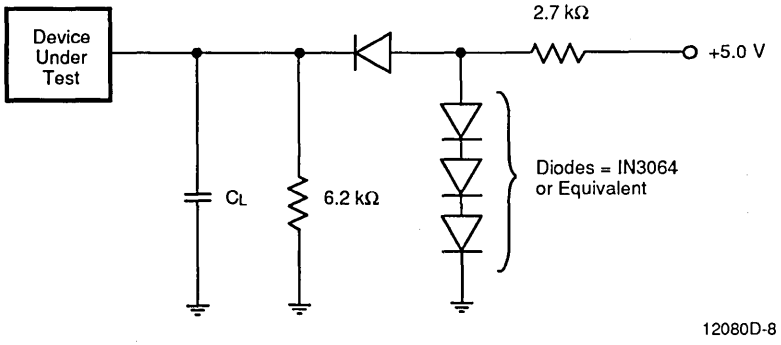
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X010					Unit
JEDEC	Standard				-105	-120	-150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	ns
				Max	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	ns
				Max	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	ns
				Max	50	50	65	75	75	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	ns
				Max	25	35	35	40	40	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	ns
				Max	–	–	–	–	–	

Notes:

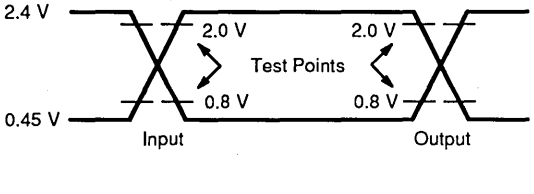
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X010 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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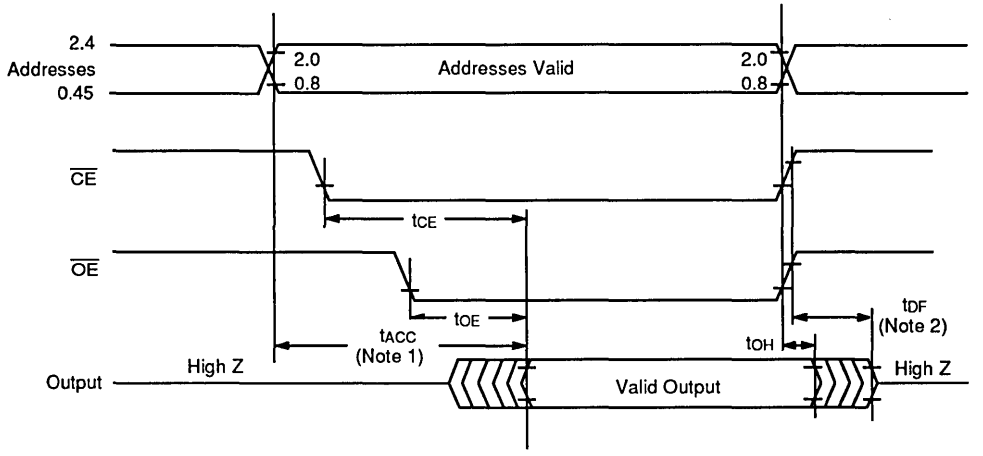
SWITCHING WAVEFORMS



12080D-10

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.

2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

FINAL

Am27X1024

1 Megabit (65,536 x 16-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 90 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

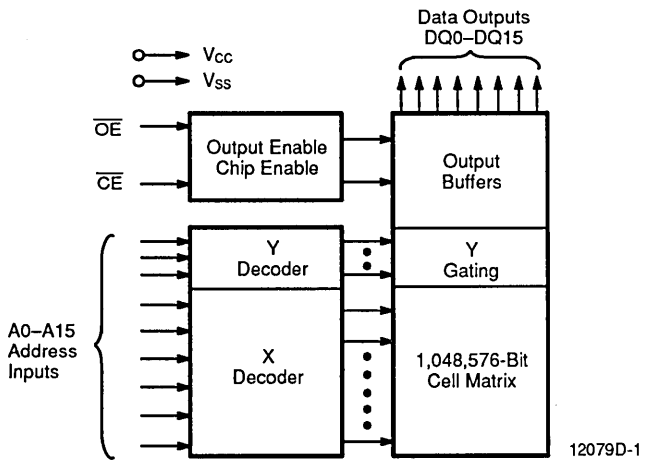
GENERAL DESCRIPTION

The Am27X1024 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 65,536 by 16 bits and is available in plastic dual in-line (PDIP) as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 90 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X1024 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



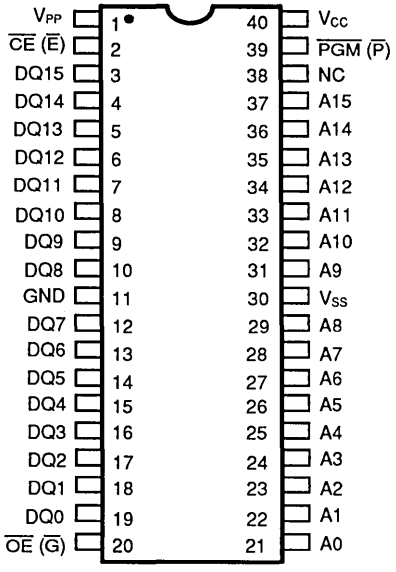
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X1024				
Ordering Part No:					
V_{CC} ±5%					-255
V_{CC} ±10%	-90	-120	-150	-200	
Max Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	45	50	65	75	100

CONNECTION DIAGRAMS

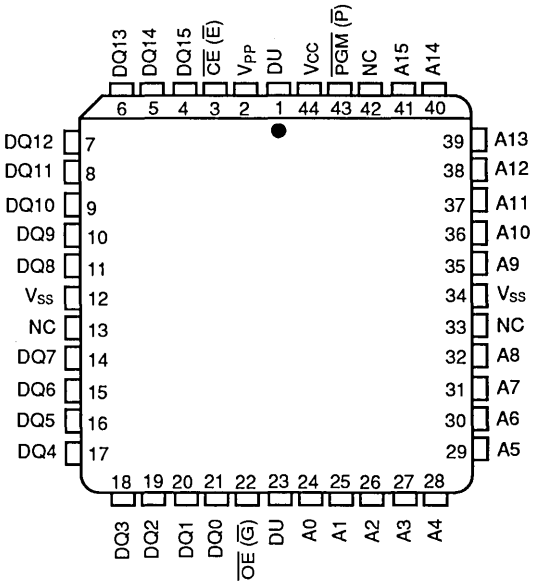
Top View

PDIP



12079D-2

PLCC



12079D-3

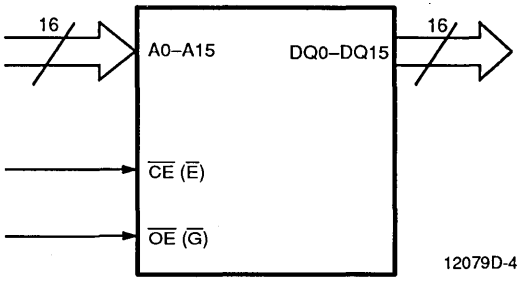
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A15	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0–DQ15	=	Data Inputs/Outputs
DU	=	No External Connection (Do Not Use)
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

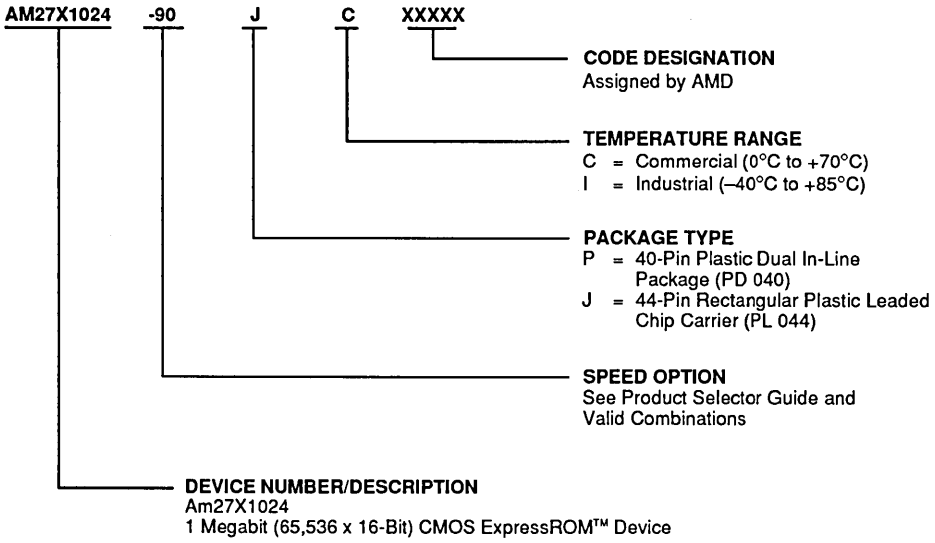
LOGIC SYMBOL



12079D-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X1024-90	PC, JC
AM27X1024-120	PC, JC, PI, JI
AM27X1024-150	
AM27X1024-200	
AM27X1024-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X1024 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X1024 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X1024 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	DOUT
Output Disable	X	V_{IH}	X	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	X	Hi-Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
All pins except V_{CC} ..... −0.6 V to V_{CC} + 0.6 V

V_{CC} ..... −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (Tc) ..... −40°C to +85°C

Supply Read Voltages
V_{CC} for Am27X1024-255 ..... +4.75 V to +5.25 V

V_{CC} for all other
valid combinations ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC}+0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		1.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 10 MHz, $I_{OUT} = 0$ mA		50	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27X1024 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

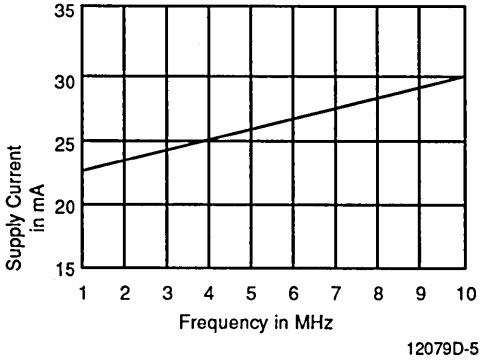


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

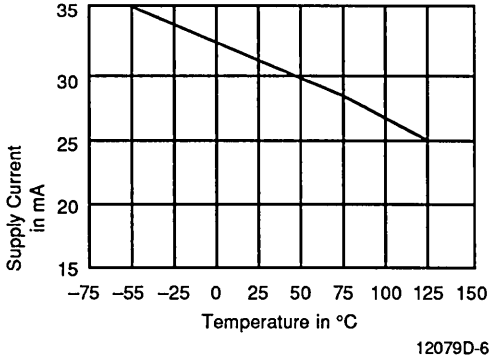


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 040		PL 044		Unit
			Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	7	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	11	14	11	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

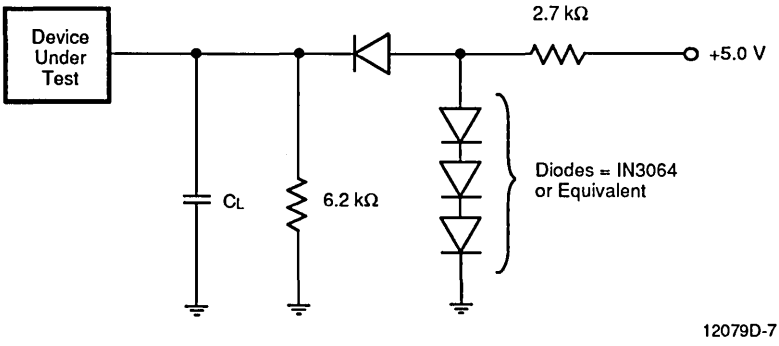
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X1024					Unit
JEDEC	Standard				-90	-120	-150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	—	—	—	—	—	ns
				Max	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	—	—	—	—	—	ns
				Max	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	—	—	—	—	—	ns
				Max	45	50	65	75	75	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	ns
				Max	40	50	50	50	50	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	ns
				Max	—	—	—	—	—	

Notes:

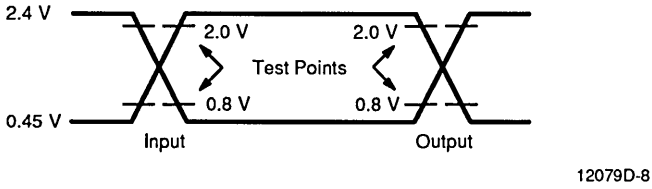
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X1024 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0." Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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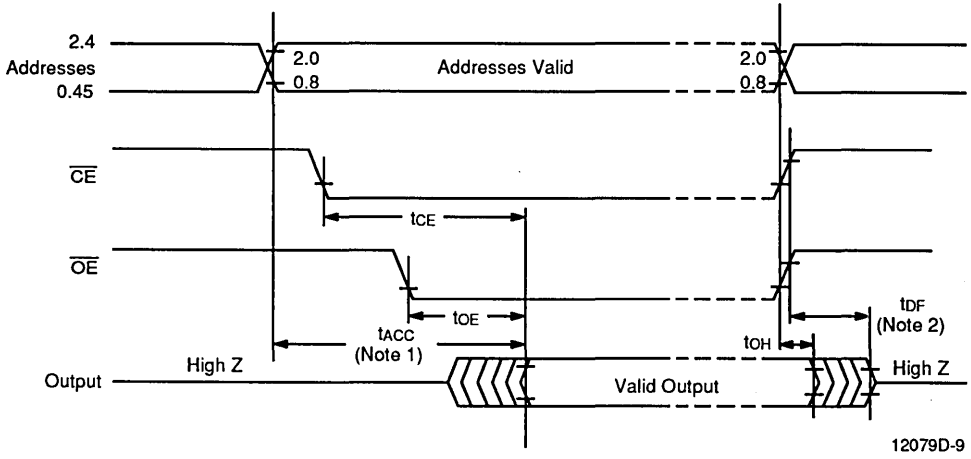
SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27X020

2 Megabit (262,144 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 100 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

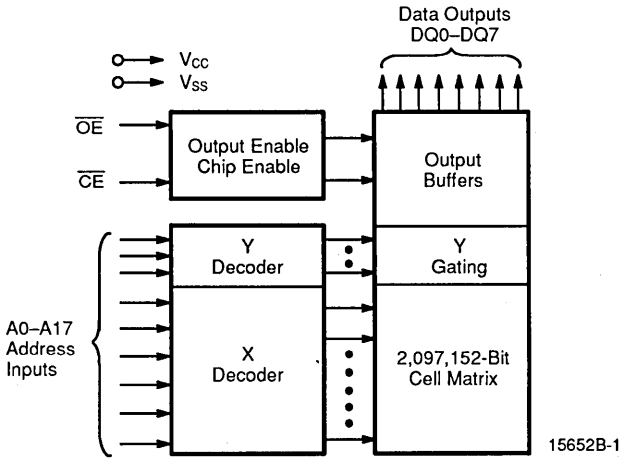
GENERAL DESCRIPTION

The Am27X020 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 262,144 by 8 bits and is available in plastic dual in-line (PDIP), plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 100 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X020 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



Publication# 15652 Rev. B Amendment/0
Issue Date: July 1993

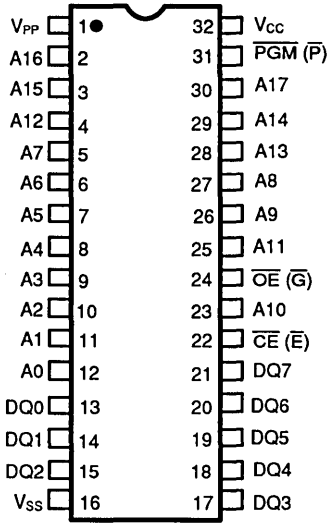
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X020				
Ordering Part No:					
V_{CC} ±5%	-105				-255
V_{CC} ±10%	-100	-120	-150	-200	
Max Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	50	65	75	100

CONNECTION DIAGRAMS

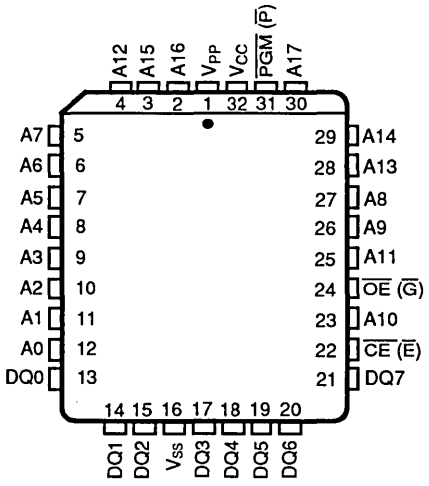
Top View

PDIP



15652B-2

PLCC



15652B-3

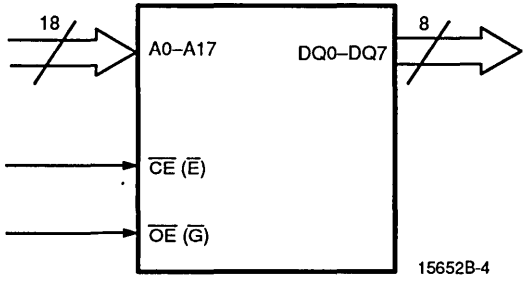
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A17 = Address Inputs
$\overline{CE}$ ($\overline{E}$) = Chip Enable Input
DQ0–DQ7 = Data Inputs/Outputs
DU = No External Connection (Do Not Use)
NC = No Internal Connection
$\overline{OE}$ ($\overline{G}$) = Output Enable Input
$\overline{PGM}$ ($\overline{P}$) = Program Enable Input
V_{CC} = V_{CC} Supply Voltage
V_{PP} = Program Supply Voltage
V_{SS} = Ground

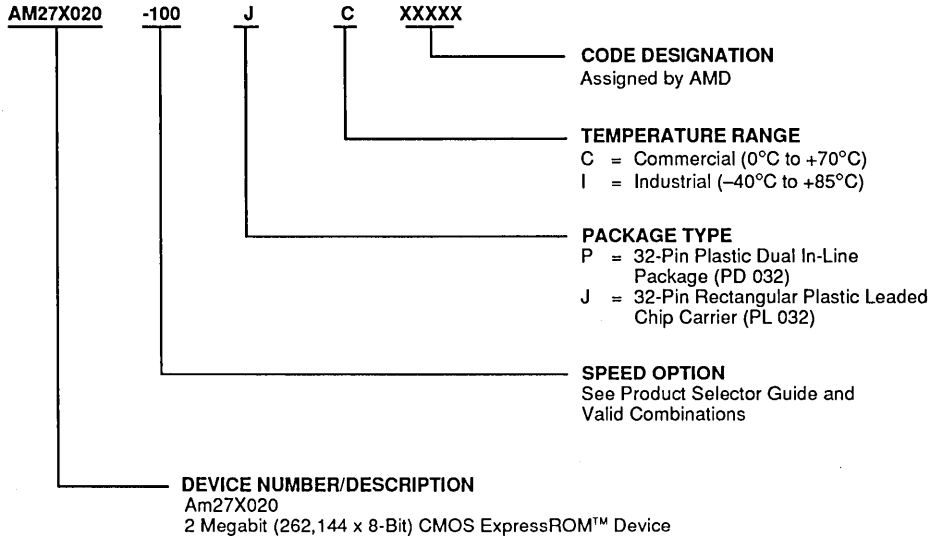
LOGIC SYMBOL



15652B-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X020-100	PC, JC, PI, JI
AM27X020-105	
AM27X020-120	
AM27X020-150	
AM27X020-200	
AM27X020-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X020 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X020 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X020 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	DOUT
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	X	Hi-Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
- All pins except V_{CC} ..... −0.6 V to V_{CC} + 0.6 V
- V_{CC} ..... −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) ..... −40°C to +85°C

Supply Read Voltages
- V_{CC} for Am27X020-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27X020-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA		30	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27X020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

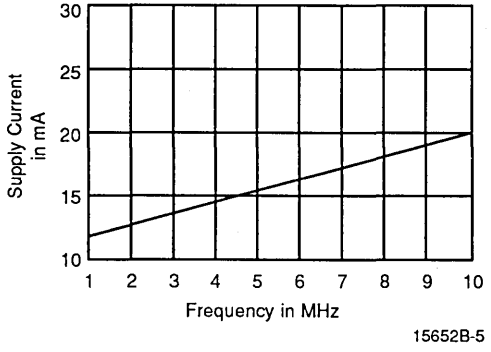


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

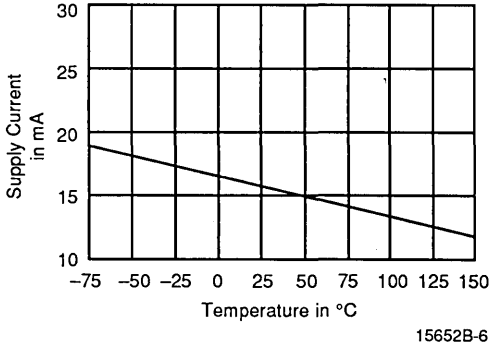


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 032		PL 032		Unit
			Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

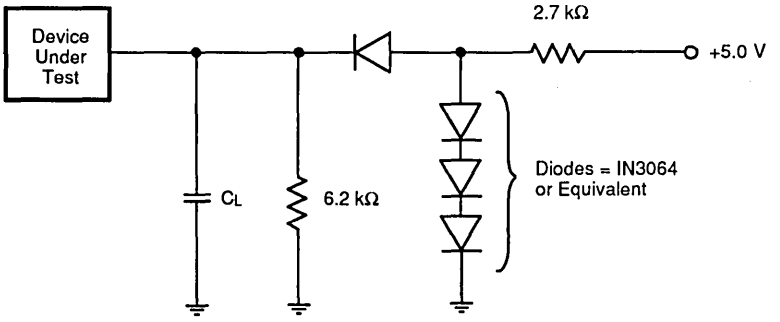
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X020					Unit
JEDEC	Standard				-105 -100	-120	-150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	—	—	—	—	—	ns
				Max	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	—	—	—	—	—	ns
				Max	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	—	—	—	—	—	ns
				Max	50	50	55	60	75	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	ns
				Max	30	30	30	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	ns
				Max	—	—	—	—	—	

Notes:

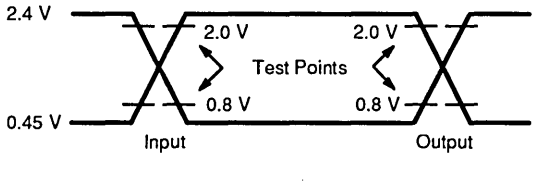
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X020 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



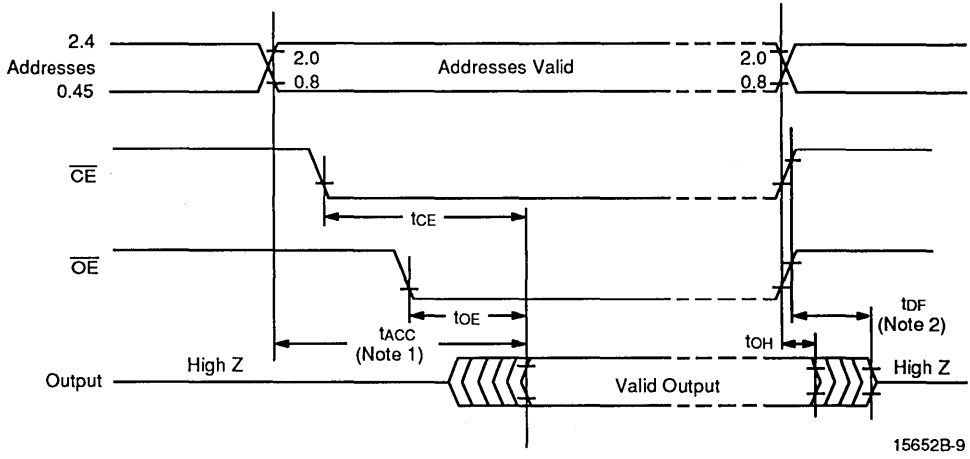
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0." Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27X2048

2 Megabit (131,072 x 16-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 100 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

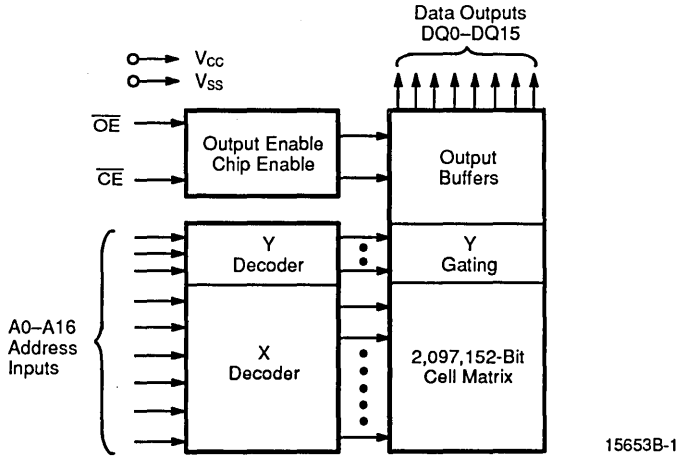
GENERAL DESCRIPTION

The Am27X2048 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 131,072 by 16 bits and is available in plastic dual in-line (PDIP) as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 100 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X2048 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



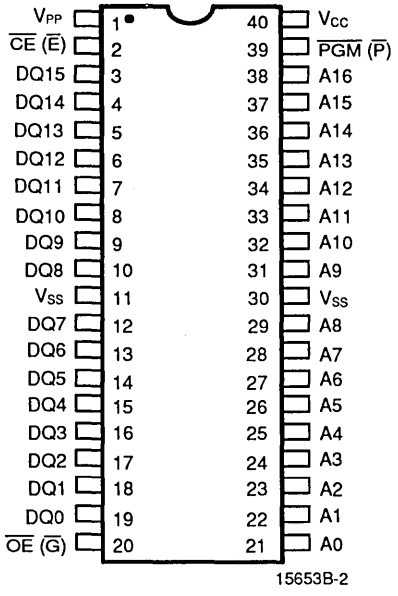
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X2048				
Ordering Part No:					
V_{CC} ±5%	-105	-125			-255
V_{CC} ±10%	-100	-120	-150	-200	
Max Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	50	65	75	100

CONNECTION DIAGRAMS

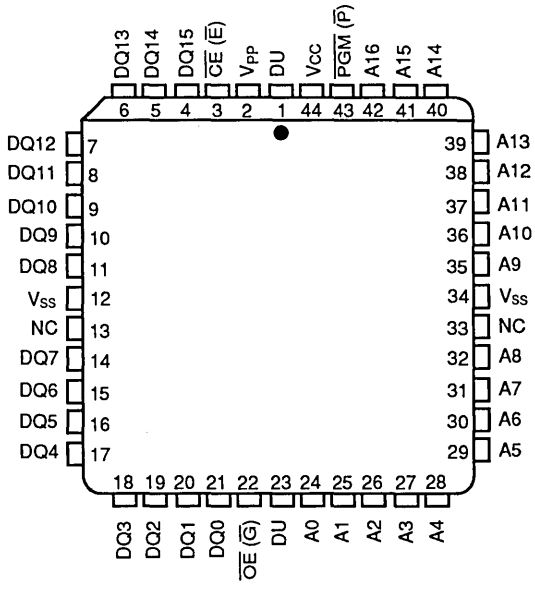
Top View

PDIP



15653B-2

PLCC



15653B-3

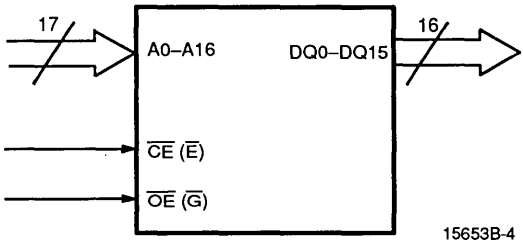
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A16 = Address Inputs
$\overline{CE}$ ($\overline{E}$) = Chip Enable Input
DQ0–DQ15 = Data Inputs/Outputs
DU = No External Connection (Do Not Use)
NC = No Internal Connection
$\overline{OE}$ ($\overline{G}$) = Output Enable Input
$\overline{PGM}$ ($\overline{P}$) = Program Enable Input
V_{CC} = V_{CC} Supply Voltage
V_{PP} = Program Supply Voltage
V_{SS} = Ground

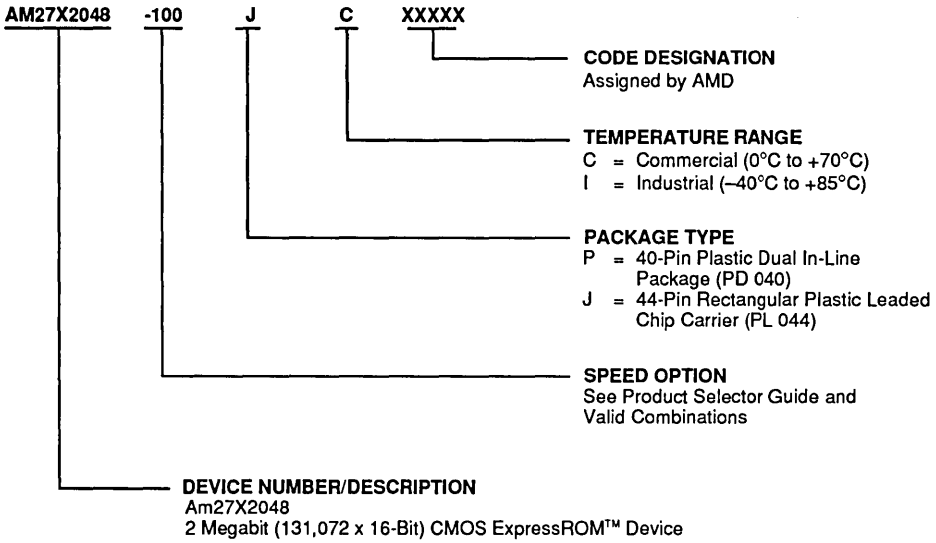
LOGIC SYMBOL



15653B-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X2048-100	PC, JC, PI, JI
AM27X2048-105	
AM27X2048-120	
AM27X2048-125	
AM27X2048-150	
AM27X2048-200	
AM27X2048-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X2048 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X2048 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X2048 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	DOUT
Output Disable	X	V_{IH}	X	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	X	Hi-Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products . . . . . –65°C to +125°C
- All Other Products . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Voltage with Respect to V_{SS}
- All pins except V_{CC} . . . . . –0.6 V to V_{CC} + 0.6 V
- V_{CC} . . . . . –0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During transitions, the inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (Tc) . . . . . 0°C to +70°C

Industrial (I) Devices
- Case Temperature (Tc) . . . . . –40°C to +85°C

Supply Read Voltages
- V_{CC} for Am27X2048-XX5 . . . . +4.75 V to +5.25 V
- V_{CC} for Am27X2048-XX0 . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA		50	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution**: The Am27X2048 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

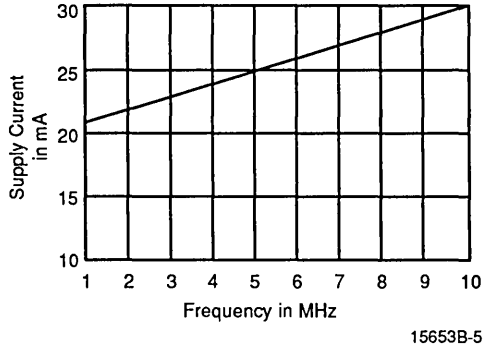


Figure 1. Typical Supply Current vs. Frequency V_{CC} = 5.5 V, T = 25°C

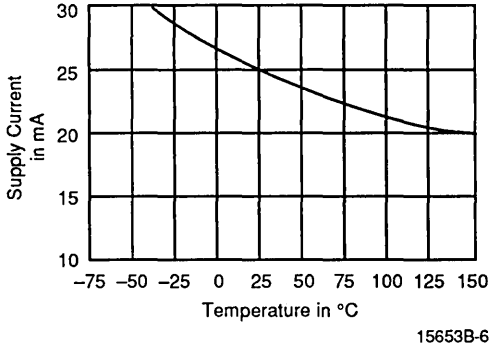


Figure 2. Typical Supply Current vs. Temperature V_{CC} = 5.5 V, f = 5 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 040		PL 044		Unit
			Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	7	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

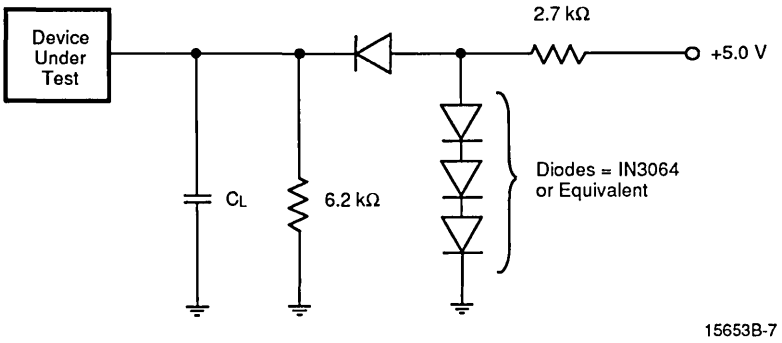
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X2048					Unit
JEDEC	Standard				-100 -105	-120 -125	-150	-200	-255	
tAVQV	tACC	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	—	—	—	—	—	ns
				Max	100	120	150	200	250	
tELQV	tCE	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	—	—	—	—	—	ns
				Max	100	120	150	200	250	
tGLQV	tOE	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	—	—	—	—	—	ns
				Max	50	50	55	60	75	
tEHQZ tGHQZ	tDF (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	ns
				Max	30	30	30	40	60	
tAXQX	tOH	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	ns
				Max	—	—	—	—	—	

Notes:

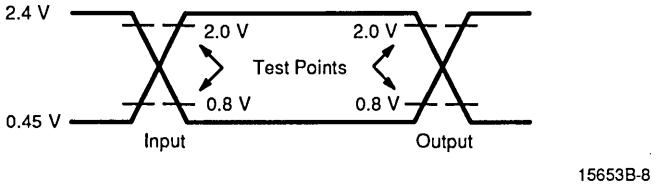
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X2048 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0." Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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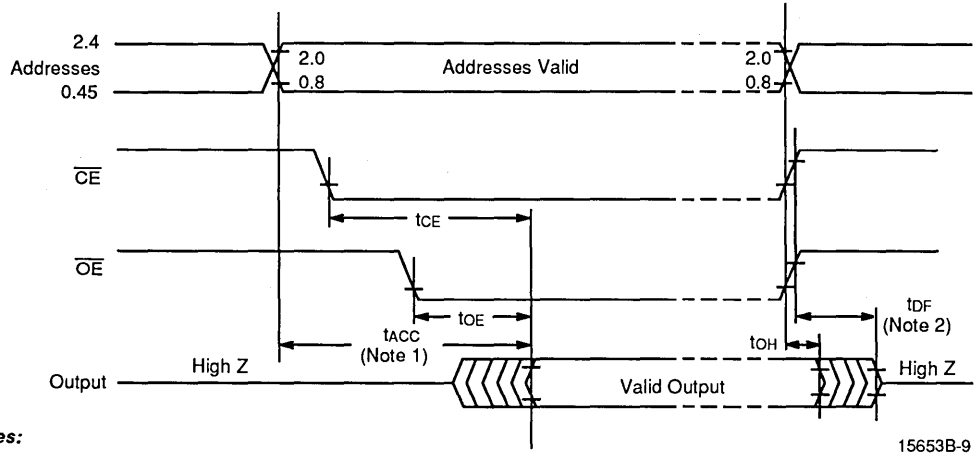
SWITCHING WAVEFORMS



15653B-9

Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27X040

4 Megabit (524,288 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 120 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

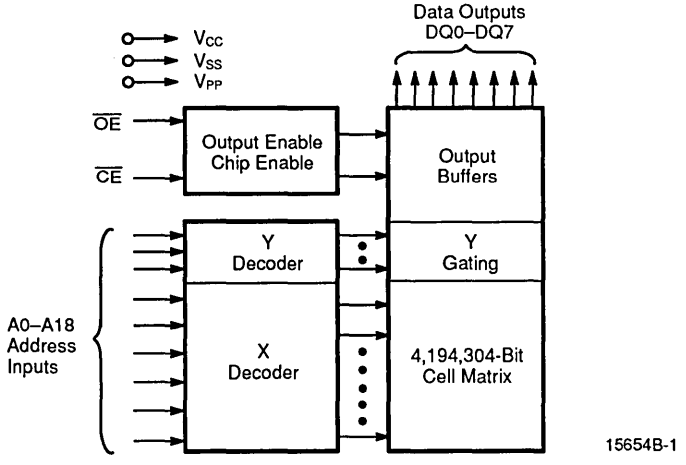
GENERAL DESCRIPTION

The Am27X040 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 524,288 by 8 bits and is available in plastic dual in-line (PDIP) as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 120 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X040 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



15654B-1

Publication# 15654 Rev. B Amendment/0
Issue Date: July 1993

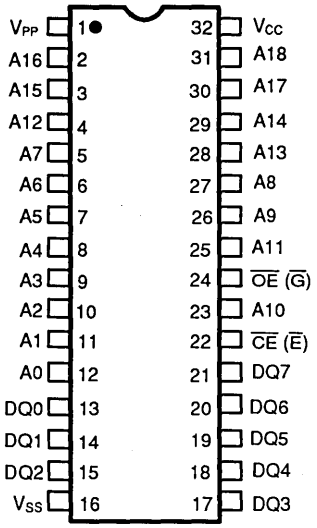
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X040			
Ordering Part No:				
V_{CC} ±5%	-125			
V_{CC} ±10%	-120	-150	-200	-250
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	65	75	100

CONNECTION DIAGRAMS

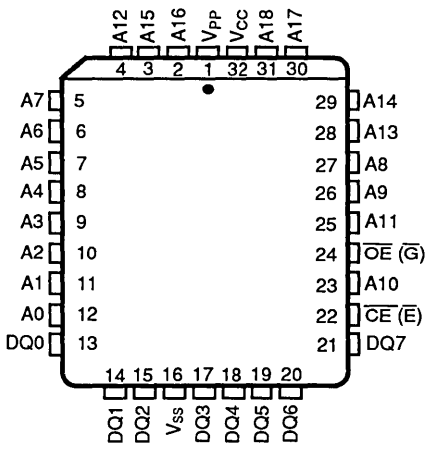
Top View

PDIP



15654B-2

PLCC



15654B-3

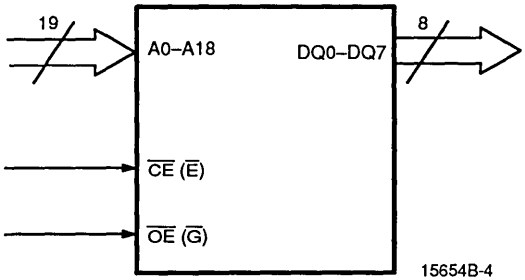
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A18	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0–DQ7	=	Data Inputs/Outputs
DU	=	No External Connection (Do Not Use)
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

LOGIC SYMBOL

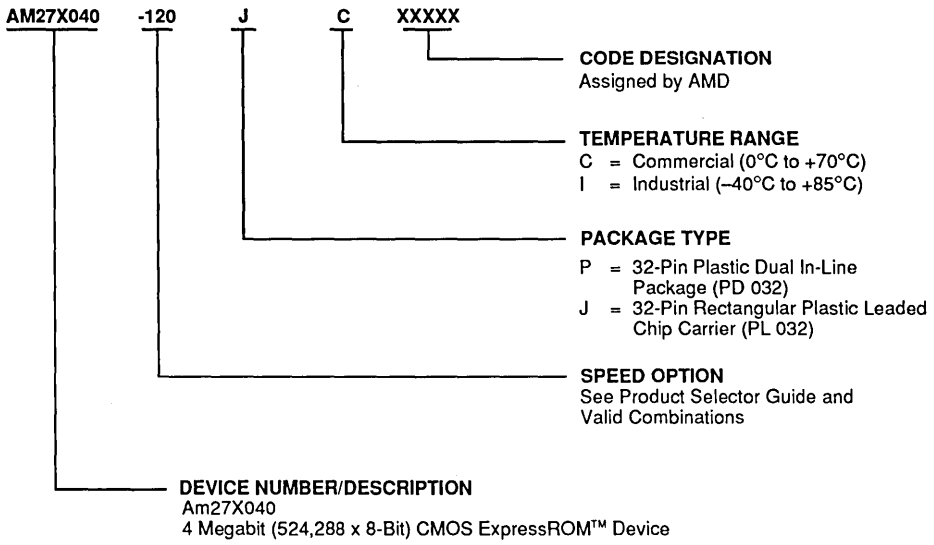


15654B-4

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X040-120	PC, JC, PI, JI
AM27X040-125	
AM27X040-150	
AM27X040-200	
AM27X040-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X040 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X040 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X040 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	DOUT
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	Hi-Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products . . . . . −65°C to +125°C
- All Other Products . . . . . −65°C to +150°C

Ambient Temperature
with Power Applied . . . . . −55°C to +125°C

Voltage with Respect to V_{SS}
- All pins except V_{CC} . . . . . −0.6 V to V_{CC} + 0.6 V
- V_{CC} . . . . . −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C) . . . . . 0°C to +70°C

Industrial (I) Devices
- Case Temperature (T_C) . . . . . −40°C to +85°C

Supply Read Voltages
- V_{CC} for Am27X040-XX5 . . . . . +4.75 V to +5.25 V
- V_{CC} for Am27X040-XX0 . . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		0.7 V_{CC}	$V_{CC}+0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA		40	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27X040 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

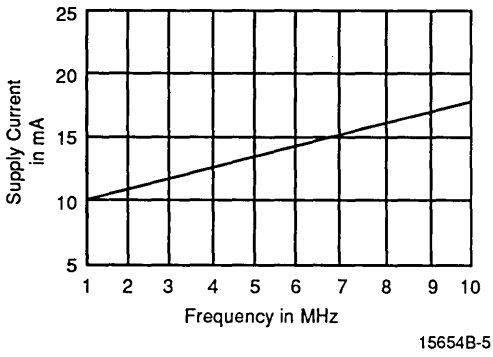


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

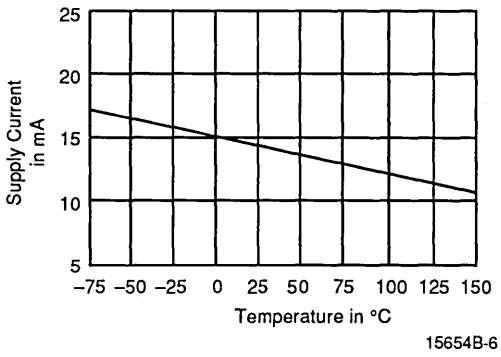


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 032		PL 032		Unit
			Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

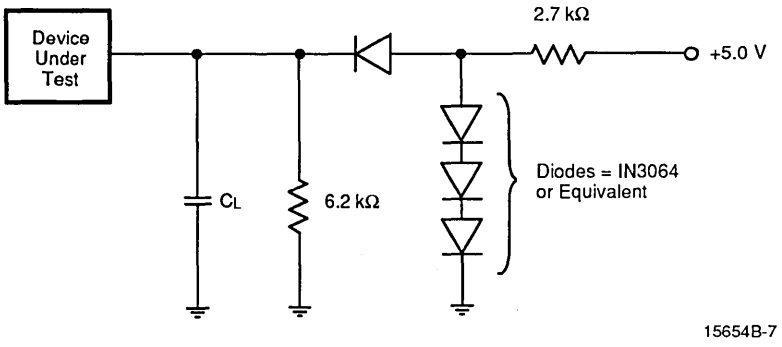
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X040				Unit
JEDEC	Standard				-125 -120	-150	-200	-250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	—	—	—	—	ns
				Max	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	—	—	—	—	ns
				Max	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	—	—	—	—	ns
				Max	50	55	60	60	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	ns
				Max	30	30	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	ns
				Max	—	—	—	—	

Notes:

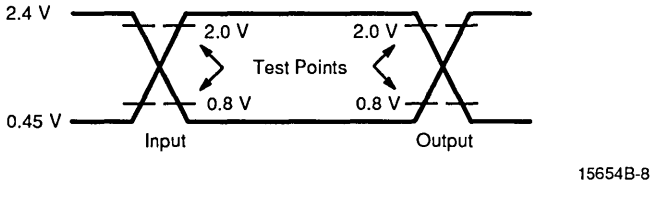
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X040 must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0." Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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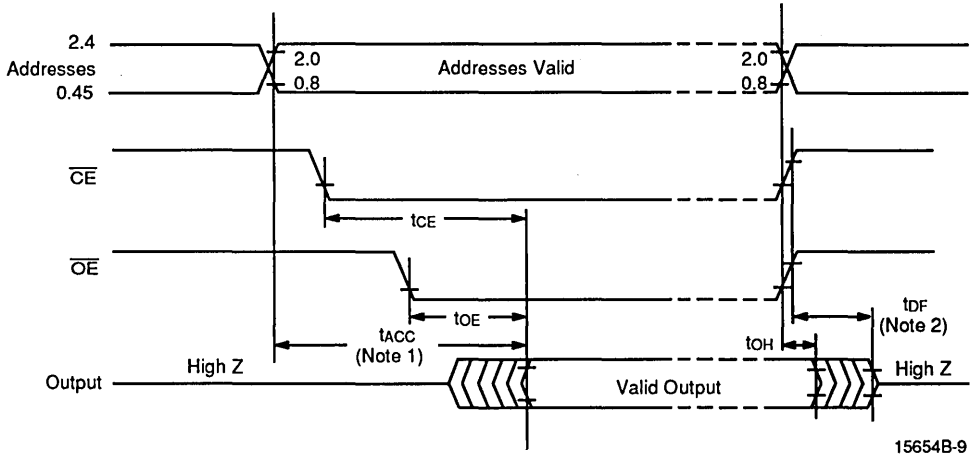
SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27X400

4 Megabit (524,288 x 8-Bit/262,144 x 16-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 120 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

GENERAL DESCRIPTION

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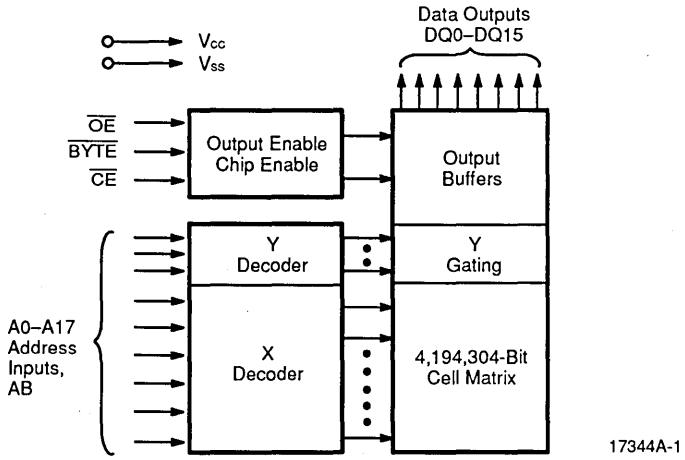
AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 150 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



17344A-1

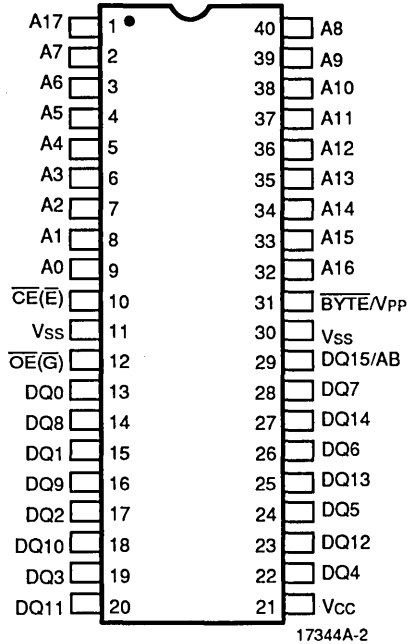
PRODUCT SELECTOR GUIDE

Family Part No	Am27X400			
Ordering Part No:				
V_{CC} ±5%	-125			-255
V_{CC} ±10%	-120	-150	-200	
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	65	75	100

CONNECTION DIAGRAMS

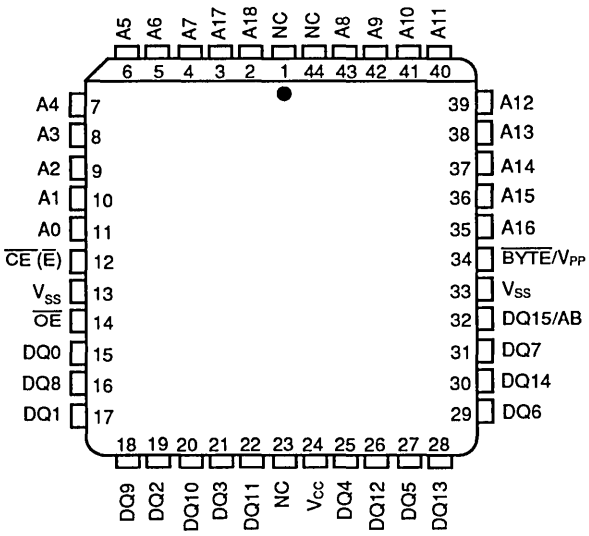
Top View

PDIP



17344A-2

PLCC



17344A-3

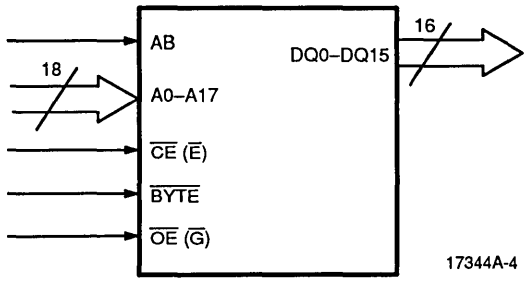
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

AB	=	Address Input ($\overline{BYTE}$ Mode)
A0–A17	=	Address Inputs
$\overline{BYTE}$	=	Byte/Word Switch
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0–DQ15	=	Data Inputs/Outputs
DU	=	No External Connection (Do Not Use)
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

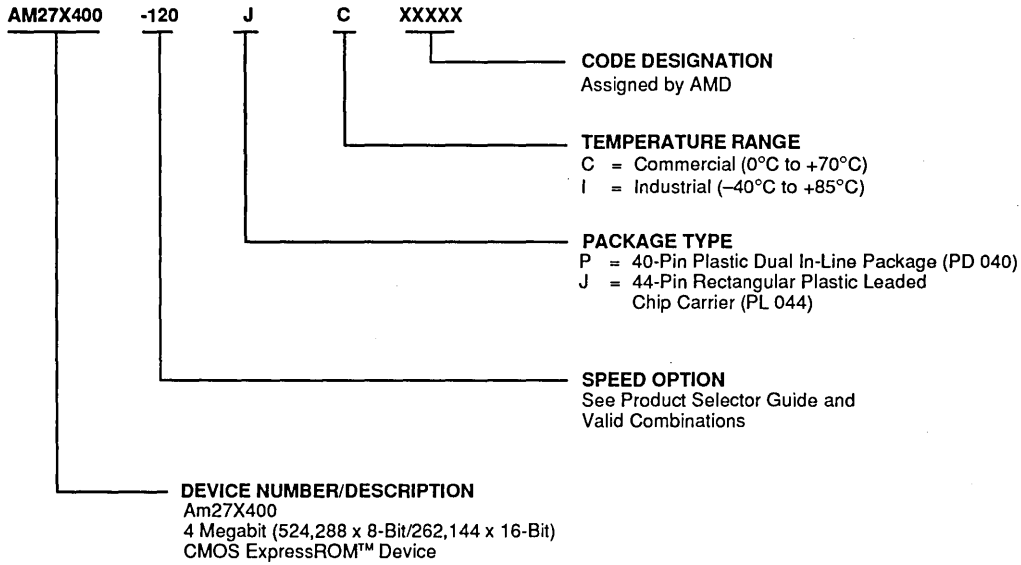
LOGIC SYMBOL



17344A-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X400-120	PC, JC, PI, JI
AM27X400-125	
AM27X400-150	
AM27X400-200	
AM27X400-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X400 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}–t_{OE}.

Byte Mode

The user has the option of reading data in either 16-bit words or 8-bit bytes under control of the $\overline{BYTE}$ input. With the $\overline{BYTE}$ input HIGH, inputs A0–A17 will address 256K words of 16-bit data. When the $\overline{BYTE}$ input is LOW, AB functions as the least significant address input and 512K bytes of data can be accessed. The 8 bits of data will appear on DQ0–DQ7.

Standby Mode

The Am27X400 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X400 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	DOUT
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	Hi-Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products . . . . . −65°C to +125°C
- All Other Products . . . . . −65°C to +150°C

Ambient Temperature
with Power Applied . . . . . −55°C to +125°C

Voltage with Respect to V_{SS}
- All pins except V_{CC} . . . . . −0.6 V to V_{CC} + 0.6 V
- V_{CC} . . . . . −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (Tc) . . . . . 0°C to +70°C

Industrial (I) Devices
- Case Temperature (Tc) . . . . . −40°C to +85°C

Supply Read Voltages
- V_{CC} for Am27X400-XX5 . . . . . +4.75 V to +5.25 V
- V_{CC} for Am27X400-XX0 . . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}		5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA		50	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27X400 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V during transactions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods less than 20 ns.*

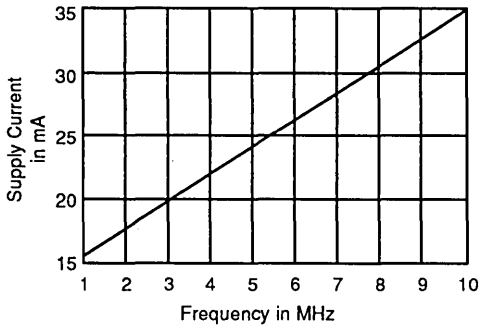


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

17344A-5

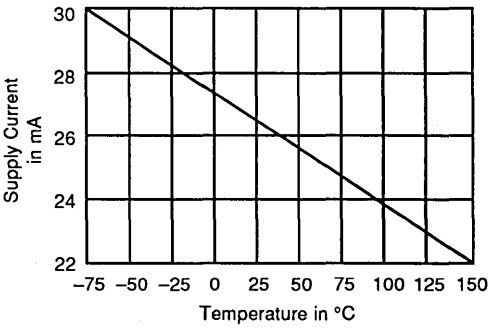


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

17344A-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 040		PL 044		Unit
			Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	6	8	9	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	9	11	13	15	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

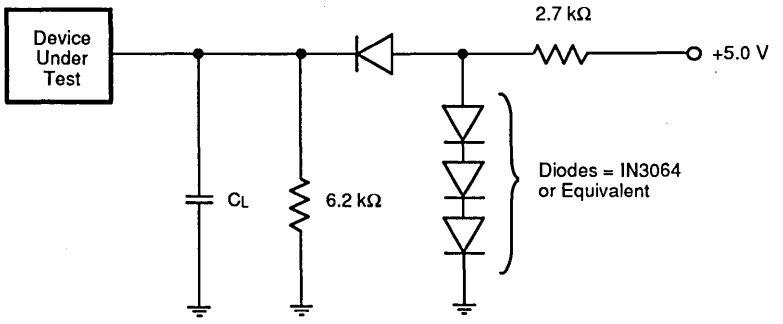
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X400				Unit
JEDEC	Standard				-125 -120	-150	-200	-255	
t_{AVQV}	t_{RCC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	ns
				Max	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	ns
				Max	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	ns
				Max	50	55	60	75	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	ns
				Max	30	30	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	ns
				Max	–	–	–	–	

Notes:

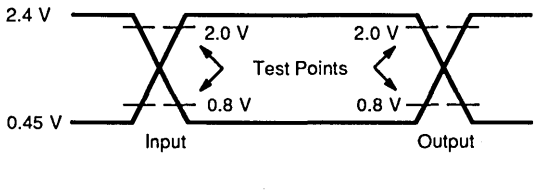
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X400 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



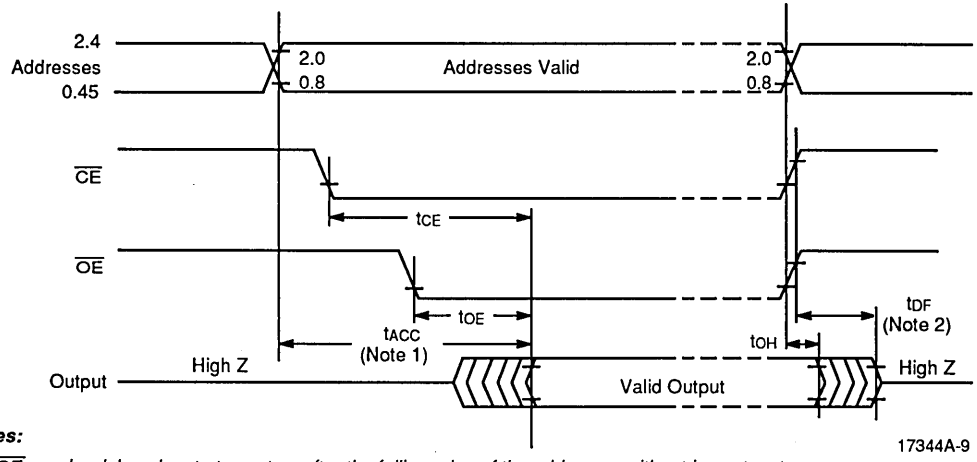
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



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Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

FINAL

Am27X4096

4 Megabit (262,144 x 16-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 120 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

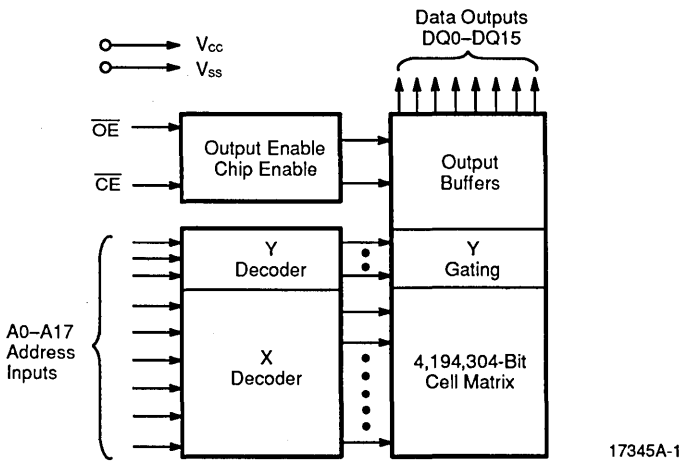
GENERAL DESCRIPTION

The Am27X4096 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 262,144 by 16 bits and is available in plastic dual in-line (PDIP) as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 120 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X4096 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 150 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



17345A-1

Publication# 17345 Rev. A Amendment/0
Issue Date: July 1993

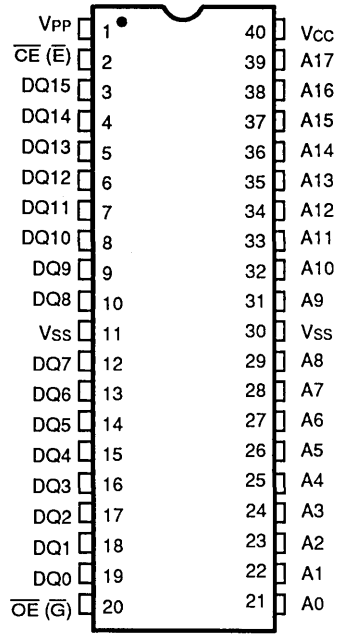
PRODUCT SELECTOR GUIDE

Family Part No	Am27X4096			
Ordering Part No:				
V_{CC} ±5%	-125			-255
V_{CC} ±10%	-120	-150	-200	
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	65	75	100

CONNECTION DIAGRAMS

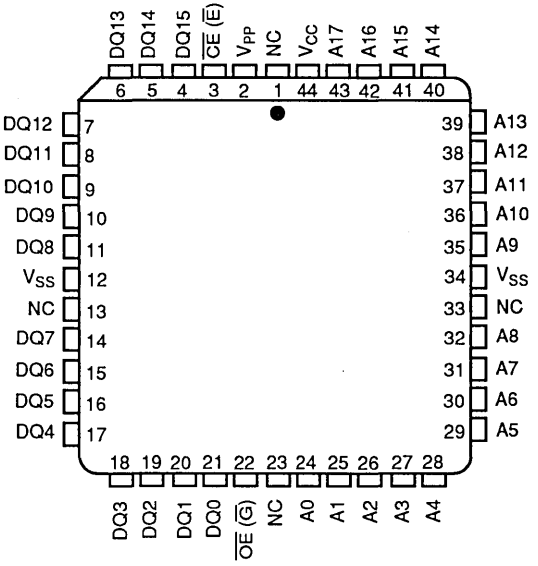
Top View

PDIP



17345A-2

PLCC



17345A-3

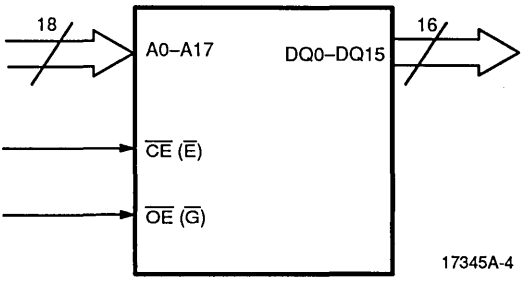
Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A17 = Address Inputs
$\overline{CE}$ ($\overline{E}$) = Chip Enable Input
DQ0–DQ15 = Data Inputs/Outputs
DU = No External Connection (Do Not Use)
NC = No Internal Connection
$\overline{OE}$ ($\overline{G}$) = Output Enable Input
V_{CC} = V_{CC} Supply Voltage
V_{PP} = Program Supply Voltage
V_{SS} = Ground

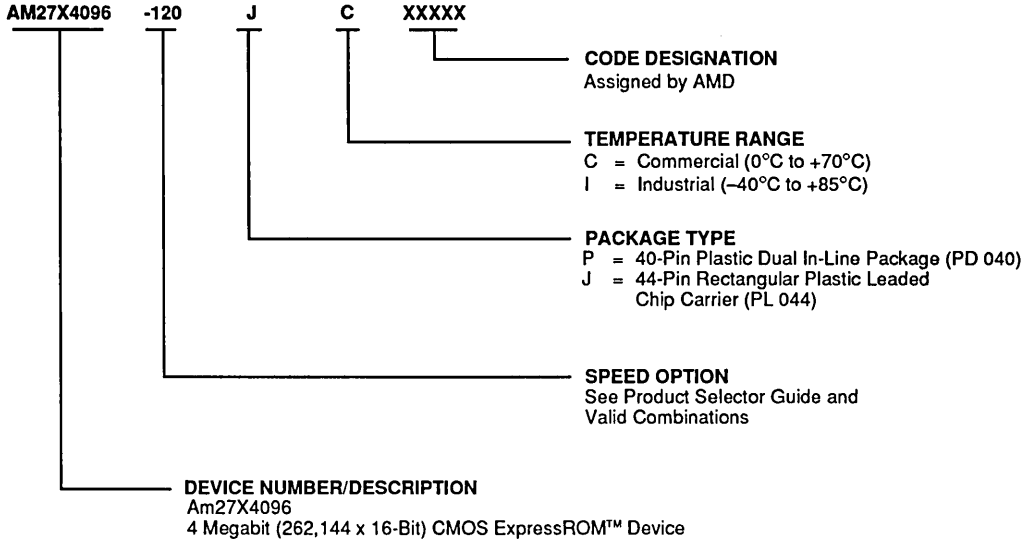
LOGIC SYMBOL



17345A-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X4096-120	PC, JC, PI, JI
AM27X4096-125	
AM27X4096-150	
AM27X4096-200	
AM27X4096-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X4096 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The Am27X4096 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X4096 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	DOUT
Output Disable	X	V_{IH}	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	Hi-Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
- All pins except V_{CC} ..... −0.6 V to V_{CC} + 0.6 V
- V_{CC} ..... −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (Tc) ..... −40°C to +85°C

Supply Read Voltages
- V_{CC} for Am27X4096-XX5 .... +4.75 V to +5.25 V
- V_{CC} for Am27X4096-XX0 .... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = – 400 µA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}		5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA		50	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27X4096 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V during transactions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods less than 20 ns.*

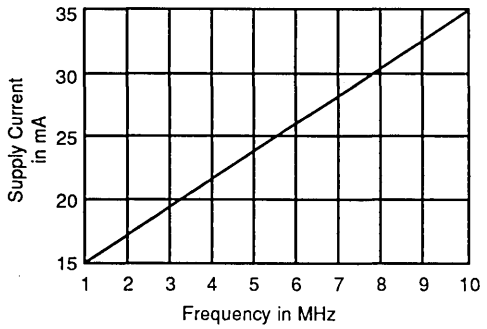


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

17345A-5

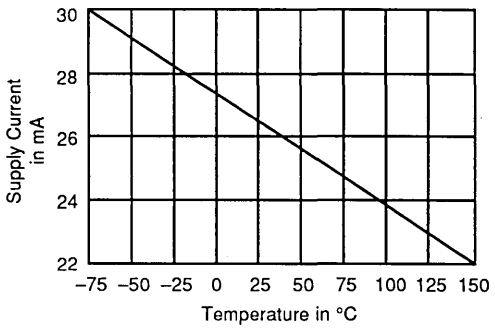


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

17345A-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 040		PL 044		Unit
			Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	6	8	10	13	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	10	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

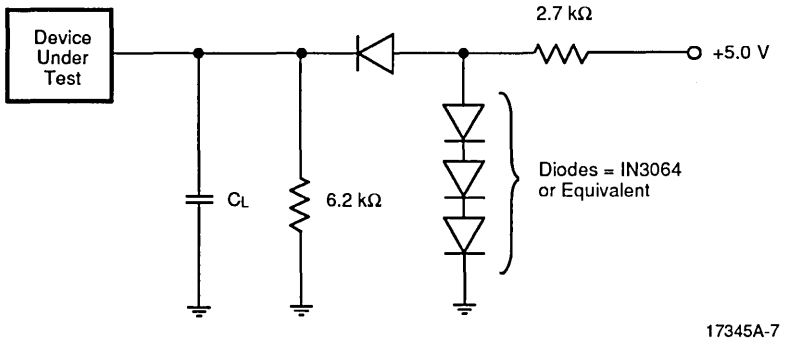
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X4096				Unit
JEDEC	Standard				-125 -120	-150	-200	-255	
t_{AVQV}	t_{RCC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	ns
				Max	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	ns
				Max	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	ns
				Max	50	55	60	60	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	ns
				Max	40	40	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	ns
				Max	–	–	–	–	

Notes:

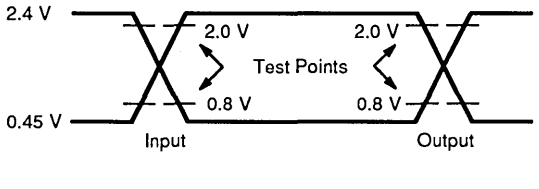
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27X4096 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



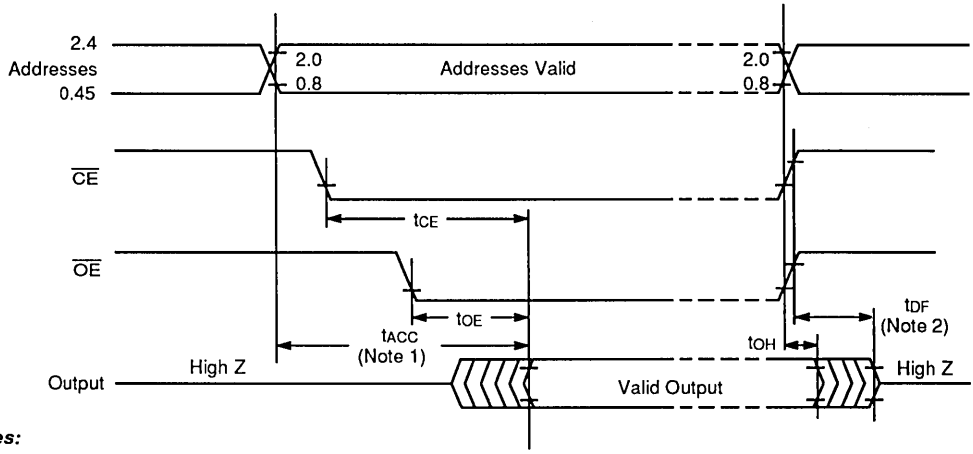
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

17345A-9

PRELIMINARY

Am27X080

8 Megabit (1,048,576 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 120 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control function

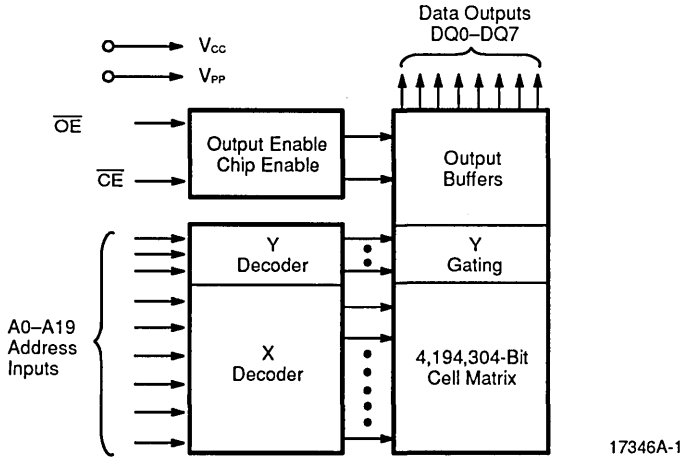
GENERAL DESCRIPTION

The Am27X080 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 1,048 K words by 8 bits per word and is available in plastic dual in-line (PDIP) as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 120 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X080 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



17346A-1

Publication# 17346 Rev. A Amendment/0
Issue Date: July 1993

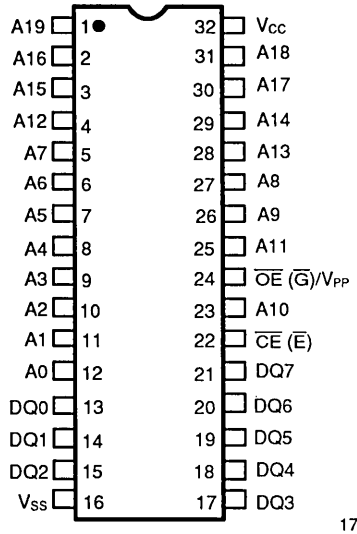
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X080			
Ordering Part No				
V_{CC} ±5%	-125			-255
V_{CC} ±10%	-120	-150	-200	
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	65	75	100

CONNECTION DIAGRAMS

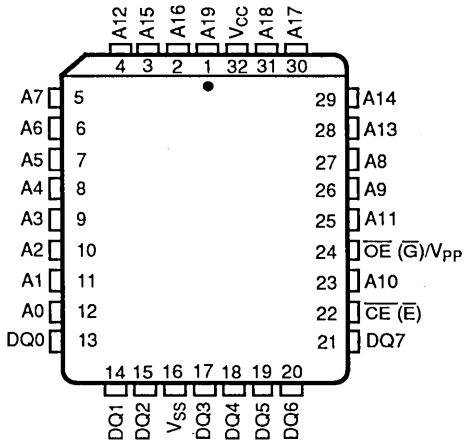
Top View

PDIP



17346A-2

PLCC



17346A-3

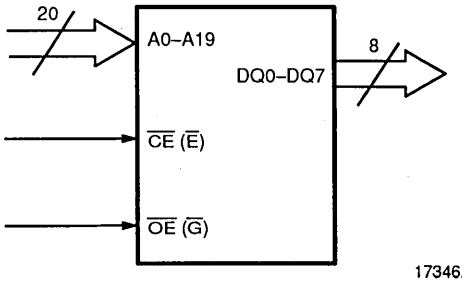
Notes:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A19	= Address Inputs
$\overline{CE}$ ($\overline{E}$)	= Chip Enable Input
DQ0–DQ17	= Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	= Output Enable Input
V_{CC}	= V_{CC} Supply Voltage
V_{PP}	= Program Supply Voltage
V_{SS}	= Ground

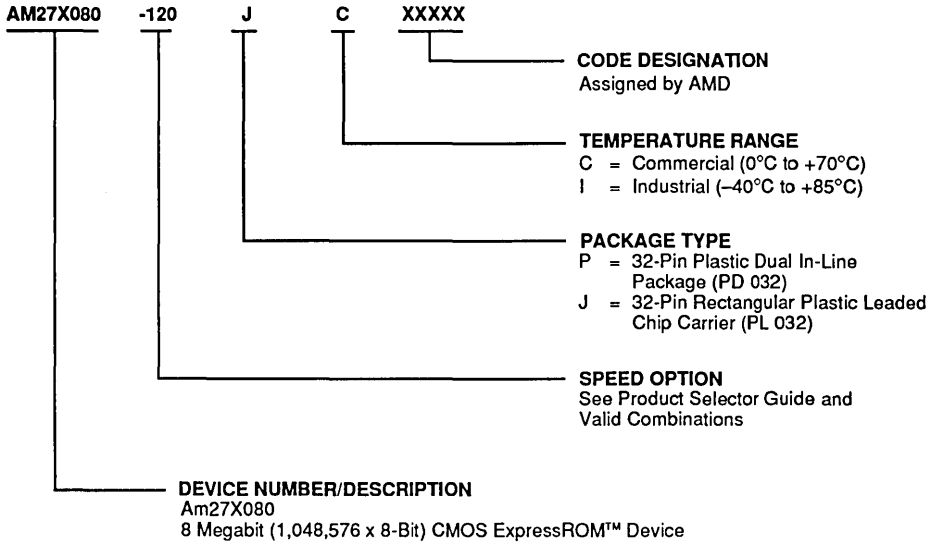
LOGIC SYMBOL



17346A-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X080-120	PC, JC, PI, JI
AM27X080-125	
AM27X080-150	
AM27X080-200	
AM27X080-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X080 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$/V_{PP}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}–t_{OE}.

Standby Mode

The Am27X080 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X080 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$/V_{PP} be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$/V_{PP}	Outputs
Read	V_{IL}	V_{IL}	DOUT
Output Disable	X	V_{IH}	Hi-Z
Standby (TTL)	V_{IH}	X	Hi-Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
- All pins except A9, V_{PP}, V_{CC} . −0.6 V to V_{CC} + 0.6 V
- V_{CC} ..... −0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
- Case Temperature (Tc) ..... −40°C to +85°C

Supply Read Voltages
- V_{CC} for Am27X080-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27X080-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	$V_{CC}-0.8$		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		0.7 V_{CC}	$V_{CC}+0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA		40	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *Caution: The Am27X080 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V during transitions, the inputs may overshoot −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods less than 20 ns.*

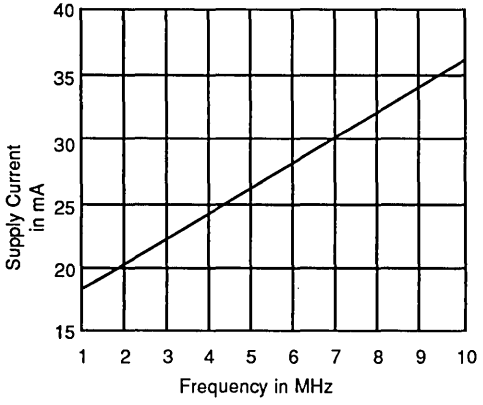


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

15453B-5

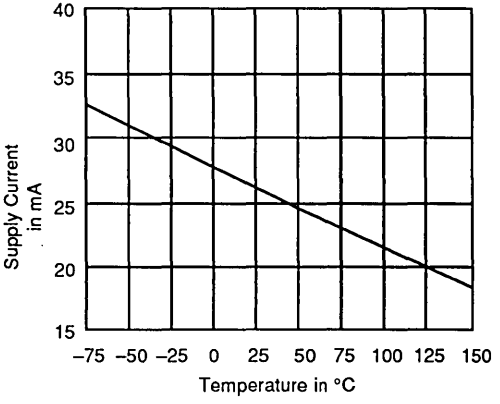


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

15453B-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 032		PL 032		Unit
			Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0 V	7	12	7	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	16	12	16	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

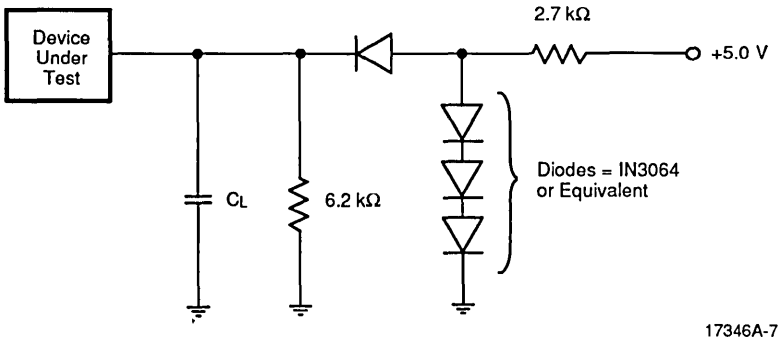
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27X080				Unit
JEDEC	Standard				-125 -120	-150	-200	-255	
t_{AVQV}	t_{RCC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	
				Max	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	
				Max	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	
				Max	50	55	60	60	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	
				Max	40	40	40	60	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	
				Max	–	–	–	–	ns

Notes:

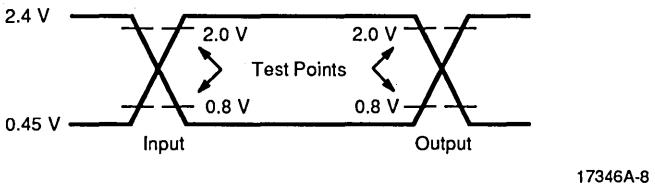
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sample and not 100% tested.*
3. ***Caution:** The Am27X080 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



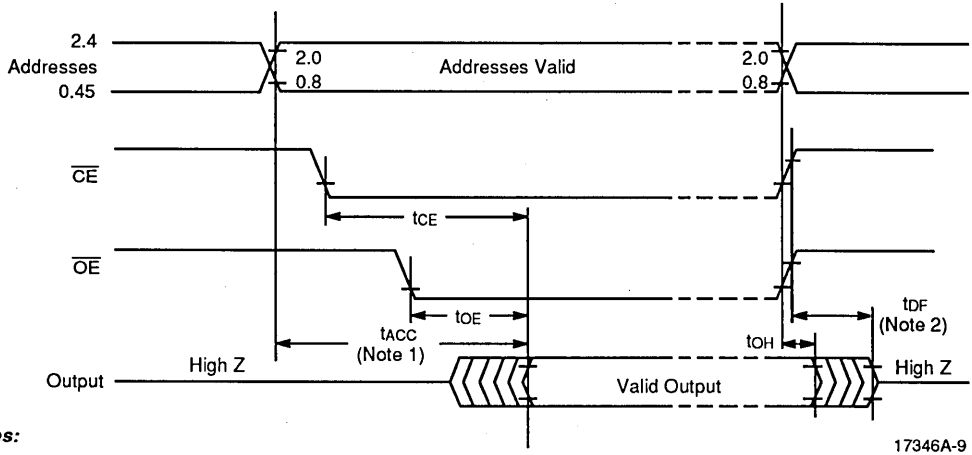
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

PRELIMINARY

Am27X800

8 Megabit (1,048,576 x 8-Bit/524,288 x 16-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 150 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 100 µA maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

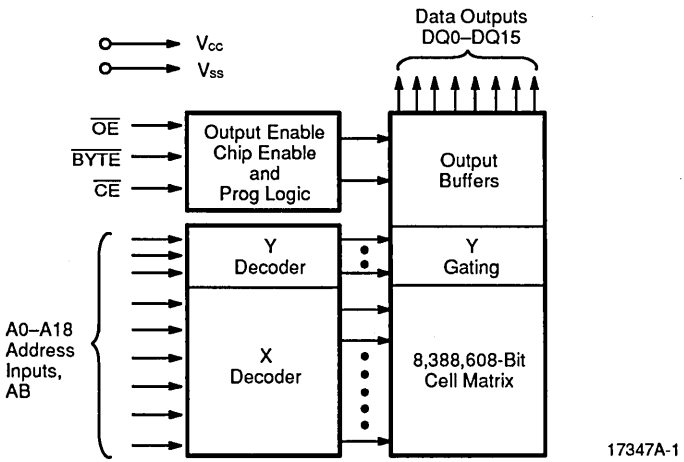
GENERAL DESCRIPTION

The Am27X800 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 1,048,576 by 8 bits/524,288 x 16 bits and is available in plastic dual in-line (PDIP) as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 150 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X800 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 150 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



17347A-1

Publication# 17347 Rev. A Amendment/0
Issue Date: July 1993

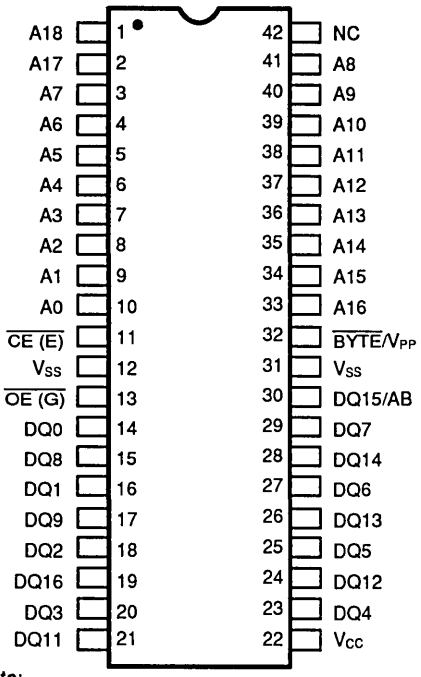
PRODUCT SELECTOR GUIDE

Family Part No	Am27X800		
Ordering Part No:			
V_{CC} ±5%	-155		-255
V_{CC} ±10%	-150	-200	
Max Access Time (ns)	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	65	75	100

CONNECTION DIAGRAMS

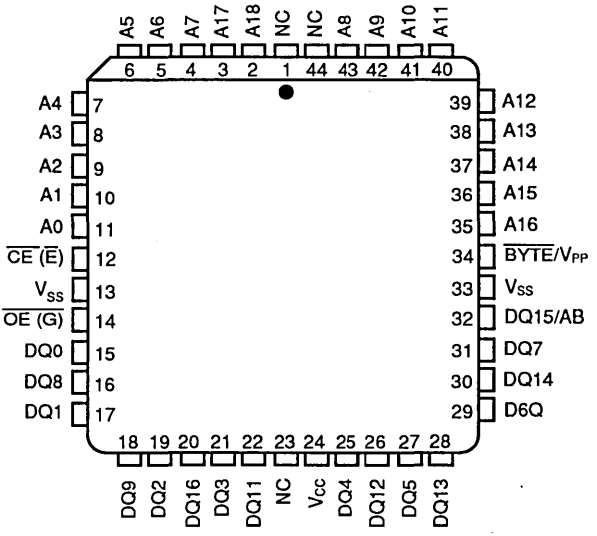
Top View

PDIP



17347A-2

PLCC



17347A-3

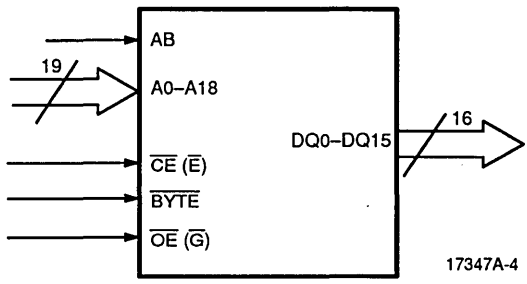
Note:

1. JEDEC nomenclature is in parenthesis.

PIN DESIGNATIONS

AB	=	Address Inputs ($\overline{BYTE}$ Mode)
A0–A18	=	Address Inputs
$\overline{BYTE}$	=	Byte/Word Switch
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0–DQ15	=	Data Inputs/Outputs
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
V_{SS}	=	Ground

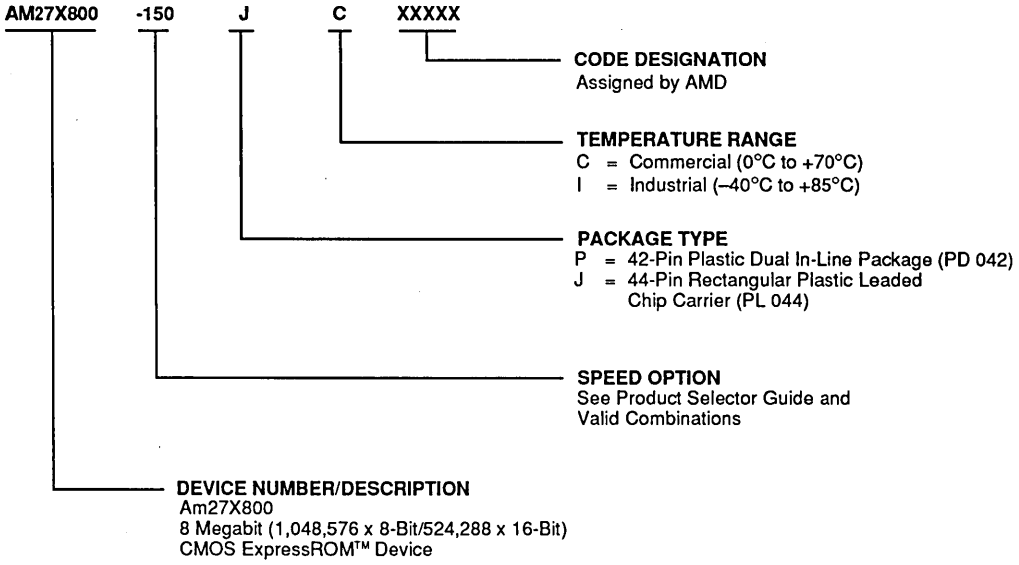
LOGIC SYMBOL



17347A-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
Am27X800-150	PC, JC, PI, JI
Am27X800-155	
Am27X800-200	
Am27X800-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X800 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Byte Mode

The user has the option of reading data in either 16-bit words or 8-bit bytes under control of the $\overline{BYTE}$ input. With the $\overline{BYTE}$ input HIGH, input A0–A18 will address 512K words of 16-bit data. When the $\overline{BYTE}$ input is LOW, AB functions as the least significant address input and 1 Mbyte of data can be accessed. The 8 bits of data will appear on DQ0–DQ7.

Standby Mode

The Am27X800 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X800 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	DOUT
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Standby (TTL)	V_{IH}	X	X	Hi-Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	Hi-Z

Note:

1. X = Either V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... −65°C to +125°C
- All Other Products ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Voltage with Respect to V_{SS}
- All pins except V_{CC} ..... −0.6 V to V_{CC} + 0.6 V
- V_{CC} ..... −0.6 V to +7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} +0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices

Case Temperature (T_C) ..... −40°C to +85°C

Supply Read Voltages

V_{CC} for Am27X800-XX5 ..... +4.75 V to +5.25 V

V_{CC} for Am27X800-XX0 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC}+0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5.0	µA
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA		50	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27X800 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
4. *Minimum DC Input Voltage is −0.5 V during transactions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

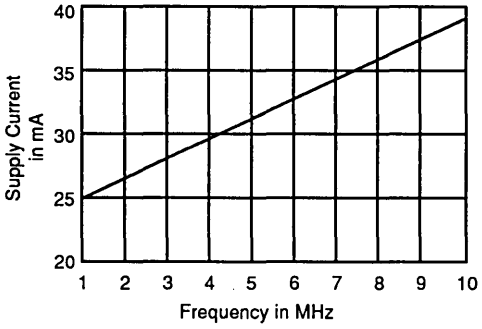


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

17344A-5

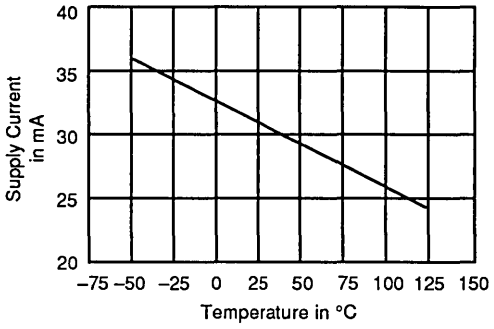


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 5 MHz

17344A-6

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	PD 042 Typ	PD 042 Max	PL 044 Typ	PL 044 Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	18	10	18	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	10	18	10	18	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

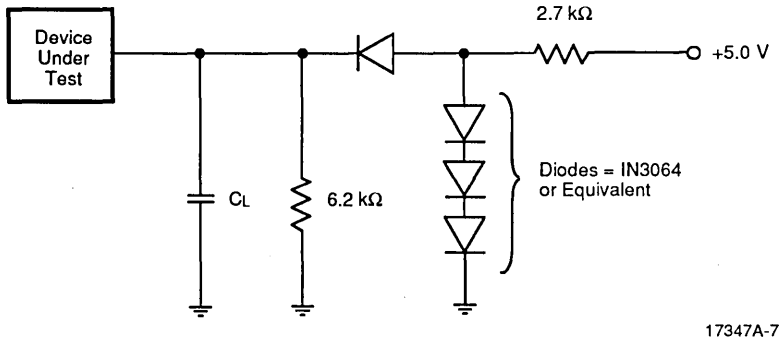
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, and 4)

Parameter Symbols JEDEC	Parameter Symbols Standard	Parameter Description	Test Conditions		Am27X800 -155 -150	Am27X800 -200	Am27X800 -255	Unit
t_{AVQV}	t_{RCC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	ns
				Max	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	ns
				Max	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	ns
				Max	55	60	60	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	ns
				Max	40	40	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	ns
				Max	–	–	–	

Notes:

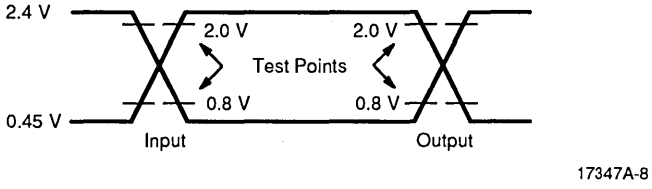
1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sample and not 100% tested.*
3. ***Caution:** The Am27X800 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



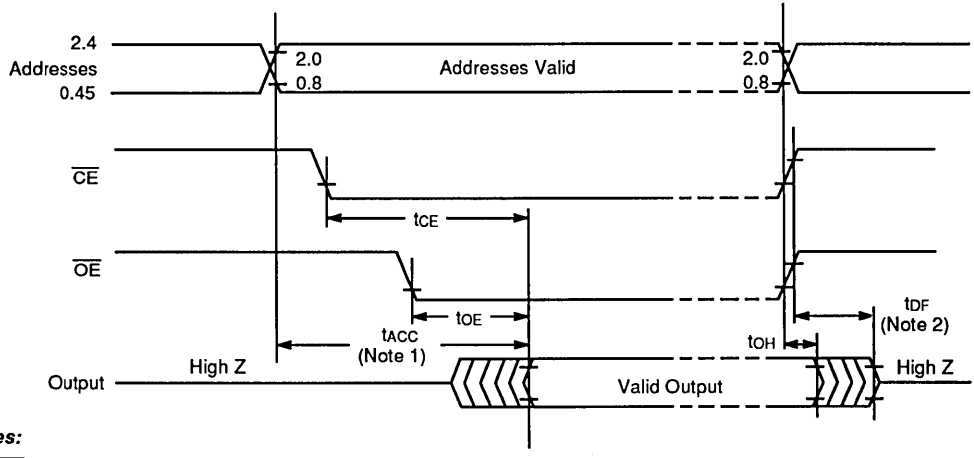
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



Notes:

1. *$\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

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SECTION

6 PROGRAMMING

PROGRAMMING

All of AMD's CMOS EPROMs now utilize the fast Flashrite™ programming algorithm. Programming the 256K EPROM typically takes 4 seconds, the 1 Mbit EPROM 16 seconds, and the 4 Mbit 1 minute. Bit locations may be programmed singly, in blocks or at random.

PROGRAMMING METHODOLOGY

Upon delivery or after each erasure, AMD's CMOS EPROM has all bits in the "ONE" or HIGH state. "ZEROs" are loaded into the device through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ and $\overline{PGM}$* are at V_{IL}, and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8- or 16-bits in parallel (depending upon the device organization) to the data output pins.

The flowchart on the next page shows AMD's Flashrite programming algorithm. The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum pulse count is reached. This process is repeated while sequencing through each address of the device. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage.

Program Verify

A program verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$* at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Read Verify

After the final address is programmed, a read verify on the entire EPROM is performed at $V_{CC} = V_{PP} = 5.25$ V.

**Not all devices have the $\overline{PGM}$ pin.*

Figure 6-1 Flashrite Programming Flowchart

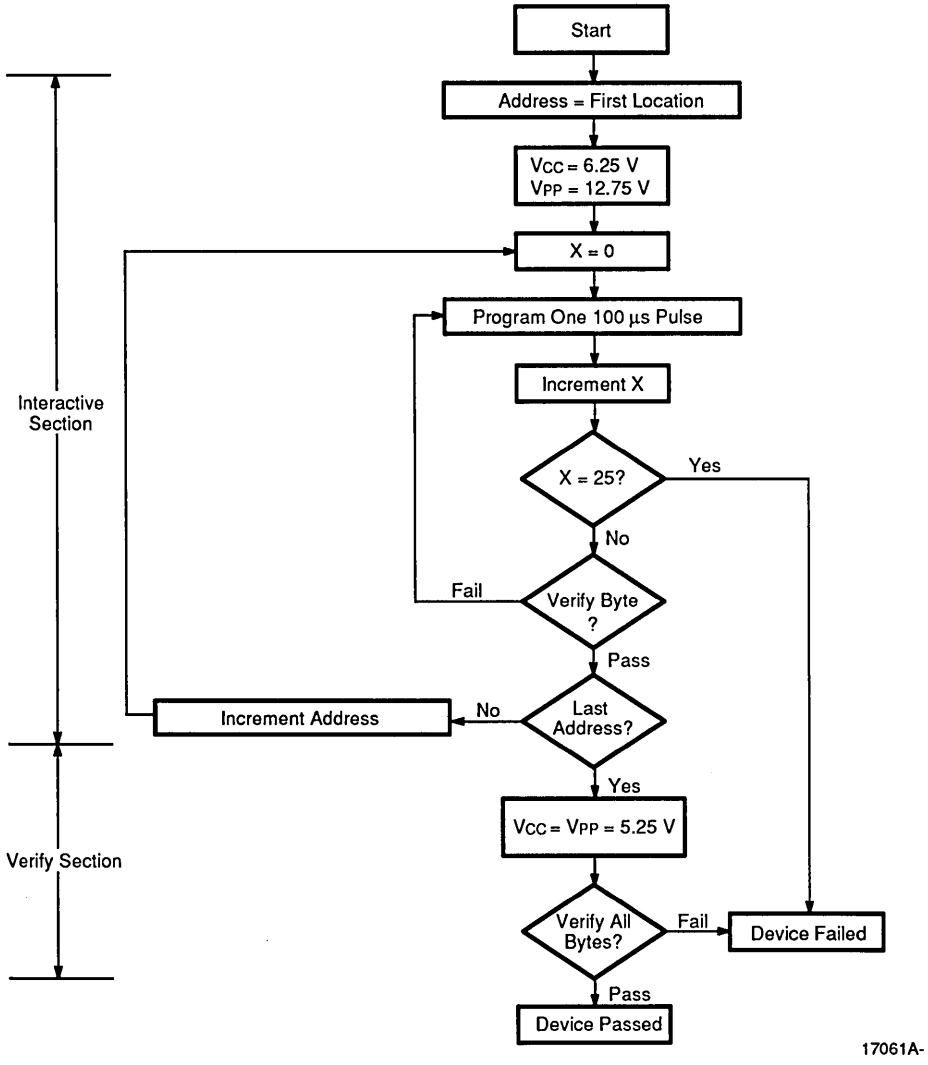


Table 6-1 **DC Programming Characteristics (T_A = +25°C ±5°C) (Notes 1, 2 and 3)**

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input LOW Level		–0.5	0.8	V
V_{IH}	Input HIGH Level		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A9 Auto Select Voltage		11.5	12.5	V
I_{CC3}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		30	mA
V_{CC1}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP1}	Flashrite Programming Voltage		12.5	13.0	V

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *When programming an AMD CMOS EPROM, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.*
3. *Programming characteristics are sampled but not 100% tested at worst-case conditions.*

Switching Characteristics and Waveforms

These programming switching characteristics and waveforms apply to the following AMD EPROM devices: Am27C64, Am27C128, Am27C010, Am27H010, Am27LV010, Am27C1024, Am27C020, Am27LV020 and Am27C2048.

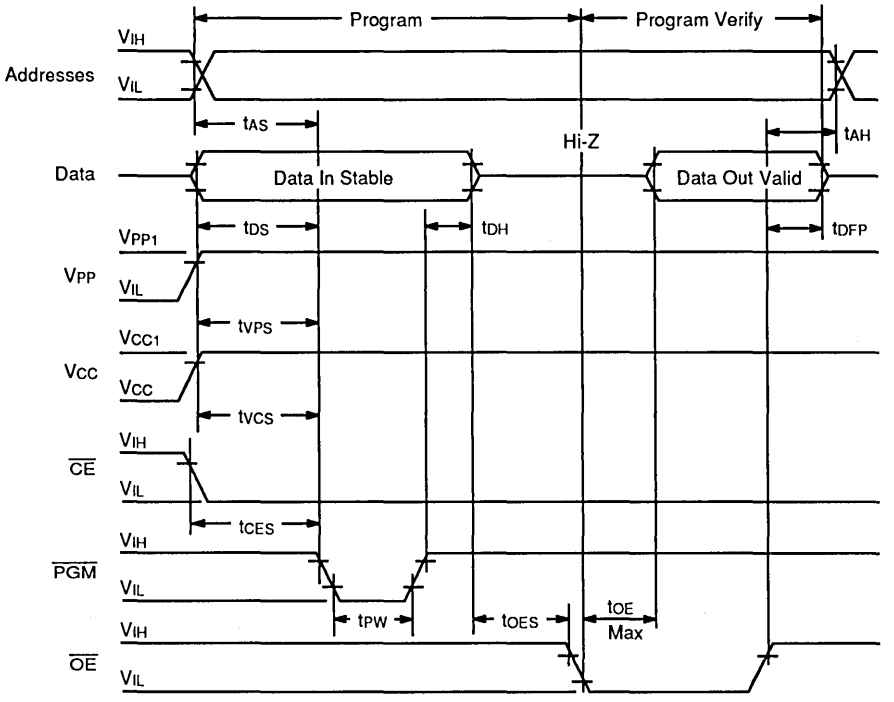
Table 6-2 **Switching Programming Characteristics (T_A = +25°C ±5°C) (Notes 1, 2 and 3)**

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *When programming the above devices, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.*
3. *Programming characteristics are sampled but not 100% tested at worst-case conditions.*

Figure 6-2 Flashrite Programming Algorithm Waveform (Notes 1 and 2)



Notes:

1. *The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.*
2. *t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.*

These programming switching characteristics and waveforms apply to the following EPROM devices: Am27C256, Am27H256, Am27C040, Am27C400, Am27C4096 and Am27C800.

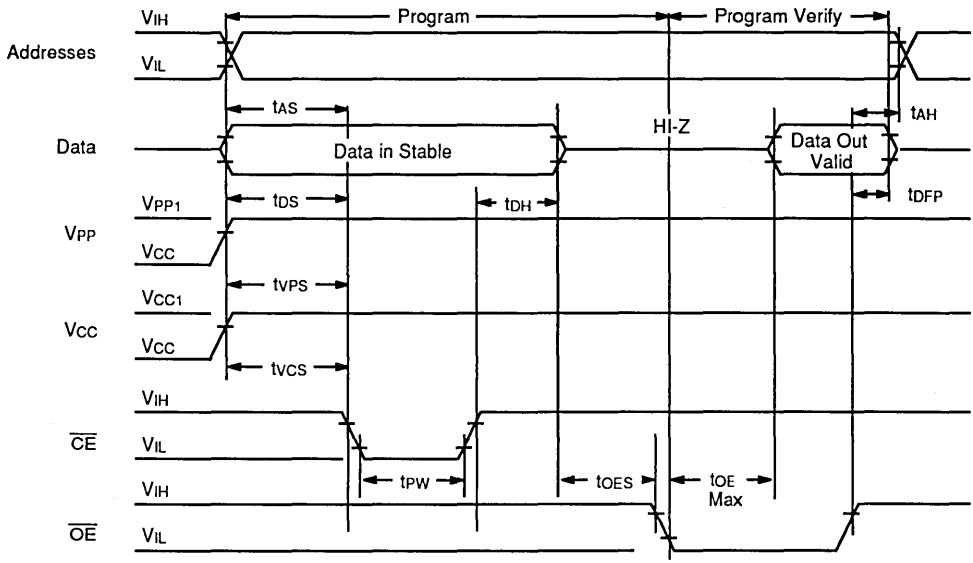
Table 6-3 Switching Programming Characteristics (T_A = +25°C ±5°C) (Notes 1, 2 and 3)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min	Max	Unit
tAVEL	tAS	Address Setup Time	2		µs
tDZGL	tOES	$\overline{OE}$ Setup Time	2		µs
tDVEL	tDS	Data Setup Time	2		µs
tGHAX	tAH	Address Hold Time	0		µs
tEHDX	tDH	Data Hold Time	2		µs
tGHQZ	tDFP	Output Enable to Output Float Delay	0	130	ns
tVPS	tVPS	VPP Setup Time	2		µs
tELEH1	tPW	$\overline{PGM}$ Program Pulse Width	95	105	µs
tVCS	tVCS	VCC Setup Time	2		µs
tGLQV	tOE	Data Valid from $\overline{OE}$		150	ns

Notes:

1. *VCC must be applied simultaneously or before VPP, and removed simultaneously or after VPP.*
2. *When programming the above devices, a 0.1 µF capacitor is required across VPP and ground to suppress spurious voltage transients which may damage the device.*
3. *Programming characteristics are sampled but not 100% tested at worst-case conditions.*

Figure 6-3 Flashrite Programming Algorithm Waveform (Notes 1 and 2)



Notes:

1. *The input timing reference level is 0.8 V for VIL and 2 V for VIH.*
2. *tOE and tDFP are characteristics of the device, but must be accommodated by the programmer.*

17061A-

These programming switching characteristics and waveforms apply to the Am27C512 and Am27C080 devices.

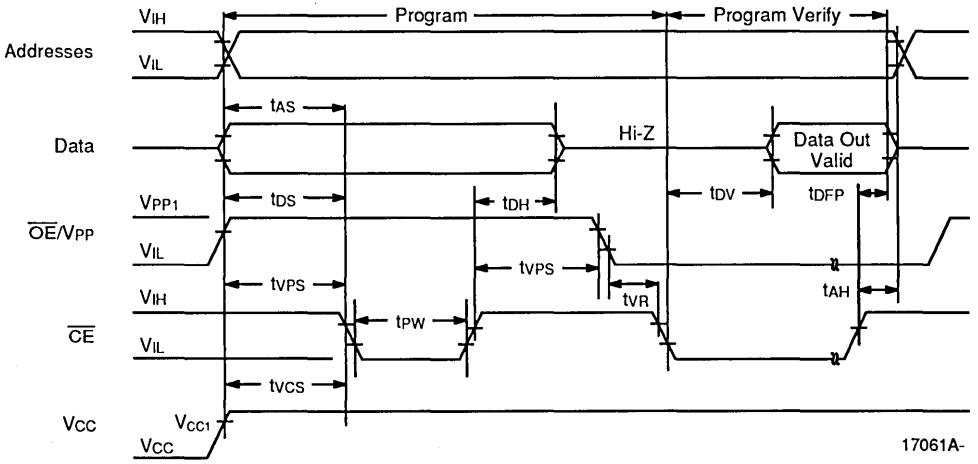
Table 6-4 Switching Programming Characteristics (T_A = +25°C ±5°C) (Notes 1, 2 and 3)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min	Max	Unit
tAVEL	tAS	Address Setup Time	2		µs
tDVEL	tDS	Data Setup Time	2		µs
tGHAX	tAH	Address Hold Time	0		µs
tEHDX	tDH	Data Hold Time	2		µs
tEHQZ	tDFP	Chip Enable to Output Float Delay	0	130	ns
tVPS	tVPS	V_{PP} Setup Time	2		µs
tELEH	tPW	$\overline{CE}$ Program Pulse Width	95	105	µs
tVCS	tVCS	V_{CC} Setup Time	2		µs
tELQV	tDV	Data Valid from $\overline{OE}$		150	ns
tEHGL	tOEH	$\overline{OE}/V_{PP}$ Hold Time	2		ns
tGLEL	tVR	$\overline{OE}/V_{PP}$ Recovery Time	2		ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *When programming the above devices, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.*
3. *Programming characteristics are sampled but not 100% tested at worst-case conditions.*

Figure 6-4 Flashrite Programming Algorithm Waveform (Notes 1 and 2)



Notes:

1. *The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.*
2. *t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.*

THIRD-PARTY PROGRAMMING SUPPORT

Recommended Vendors

Advin Systems

- PILOT-U84 Programmer
- PILOT-U40 Programmer
- PILOT-145 Programmer
- PILOT-GCE Programmer
- PILOT-832D Programmer

BP Microsystems

- BP-1200 Programmer
- CP-1128 Programmer
- EP-1132 Programmer
- EP-1140 Programmer
- EP-1 Programmer

Data I/O Corporation

- 2900 Programmer
- UniPak 2B Programmer
- BoardSite Programmer
- HandlerSite Programmer
- UniSite 40 Programmer
- S1000 Programmer
- 3900 Programmer

Elan Digital Systems Ltd

- 132 Programmer
- 142 Programmer
- 232 Programmer
- 532 Programmer
- 832 Programmer
- 840 Programmer
- 928 Programmer
- 932 Programmer
- 940 Programmer

Logical Devices

- ALLPRO 88/XR Programmer
- Husky Programmer
- GangPro-8+ Programmer
- GangPro-S Model II Programmer

Stag Microsystems

- 39M101 Programmer
- 41M101 Programmer
- 41M102 Programmer
- 41M111 Programmer
- 41M121 Programmer
- 42M101 Programmer
- ZM3000 Programmer
- Orbit Programmer
- Solar Programmer
- Stratus-2 Programmer
- System 1040/84 Programmer

PROGRAMMING UPDATE

The following charts provide the latest information on programming support for AMD's CMOS EPROMs from the following vendors:

Advin Systems, Inc.
BP Microsystems
Data I/O Corporation
Elan Digital Systems Ltd.
Logical Devices
Stag Microsystems

These charts indicate the Versions as well as the Family code (where appropriate) that incorporates the **FLASHRITE™ Programming Algorithm** for all of their "popular" models.

Table 6-6 Advin Systems

Part Number Package	Version				
	PILOT -U84	PILOT -U40	PILOT -145	PILOT -GCE	PILOT -832D
Am27C64					
DIP	V10.42	V10.42	V10.42	V10.42	V10.43
PLCC	V10.42*	V10.42*	V10.42*	V10.42*	V10.43
Am27C128					
DIP	V10.42	V10.42	V10.42	V10.42	V10.43
PLCC	V10.42*	V10.42*	V10.42*	V10.42*	V10.43
Am27C256					
DIP	V10.42	V10.42	V10.42	V10.42	V10.43
PLCC	V10.42*	V10.42*	V10.42*	V10.42*	V10.43
Am27H256					
DIP	V10.42	V10.42	V10.42	V10.42	V10.43
PLCC	V10.42*	V10.42*	V10.42*	V10.42*	V10.43
Am27C512					
DIP	V10.42	V10.42	V10.42	V10.42	V10.43
PLCC	V10.42*	V10.42*	V10.42*	V10.42*	V10.43
Am27C010					
DIP	V10.42	V10.42	V10.42	V10.42	V10.43
PLCC	V10.42*	V10.42*	V10.42*	V10.42*	V10.43
Am27H010					
DIP	V10.42	V10.42	V10.42	V10.42	V10.43
PLCC	V10.42*	V10.42*	V10.42*	V10.42*	V10.43
Am27C100					
DIP	V10.42	V10.42	V10.42	V10.42	V10.43
PLCC	V10.42*	V10.42*	V10.42*	V10.42*	V10.43
Am27C1024					
DIP	V10.42	V10.42	V10.42		V10.43
PLCC	V10.42*	V10.42*	V10.42*		V10.43

Table 6-6 Advin Systems (continued)

Part Number Package	Version				
	PILOT -U84	PILOT -U40	PILOT -145	PILOT -GCE	PILOT -832D
Am27C020					
DIP	V10.42	V10.42	V10.42	V10.42	V10.43
PLCC	V10.42*	V10.42*	V10.42*	V10.42*	V10.43
Am27C2048					
DIP	V10.42	V10.42	V10.42		V10.43
PLCC	V10.42*	V10.42*	V10.42*		V10.43
Am27C040					
DIP	V10.42	V10.42	V10.42	V10.42	V10.43
PLCC	V10.42*	V10.42*	V10.42*	V10.42*	V10.43
Am27C400					
DIP	V10.42	V10.42	V10.42		V10.43
PLCC					
Am27C4096					
DIP	V10.42	V10.42	V10.42		V10.43
PLCC	V10.42*	V10.42*	V10.42*		V10.43

Notes:

1. *Information listed above applies for all speed grades of that particular device/package.*
2. *Programmer models PILOT-U84, PILOT-U40, PILOT-145 and PILOT-GCE are single socket programmers whereas PILOT-832D is a gang programmer.*
3. *Programmer model PILOT-GCE does not support the X16 organizations.*
4. *PLCC packages for all devices (marked with an *) for the following programmers: PILOT-U84, PILOT-U40, PILOT-145 and PILOT-GCE require separate modules. These modules are listed below:*

   PX-32 32-pin PLCC (X8 organizations)

   PX-44 44-pin PLCC (X16 organizations)
5. *For further information please contact Advin Systems directly at (408) 243-7000.*

Table 6-7 BP Microsystems

	Version (DIP Packages only)				
Part Number	BP-1200	CP-1128	EP-1140	EP-1132	EP-1
Am27C64	V2.05	V2.05	V2.05	V2.05	V2.05
Am27C128	V2.05	V2.05	V2.05	V2.05	V2.05
Am27C256	V2.05	V2.05	V2.05	V2.05	V2.05
Am27H256	V2.05	V2.05	V2.05	V2.05	V2.05
Am27C512	V2.05	V2.05	V2.05	V2.05	V2.05
Am27C010	V2.05		V2.05	V2.05	
Am27H010	V2.05		V2.05	V2.05	
Am27C100	V2.05		V2.05	V2.05	
Am27C1024	V2.05		V2.05		
Am27C020	V2.05		V2.05	V2.05	
Am27C2048	V2.05		V2.05		
Am27C040	V2.05		V2.05	V2.05	
Am27C400	V2.05				
Am27C4096					

Notes:

1. *Information listed above applies for all speed grades of that particular device/package.*
2. *There is a reason for the "blanks" above due to the fact that each module serves a specific DIP Package Pin-count(s):*

Model	***Package Pin-Count***
BP-1200	*28, 32 and 40 pins*
CP-1128	*28 pin*
EP-1140	*28, 32 and 40 pins*
EP-1132	*28 and 32 pins*
EP-1	*28 pin*

3. *All LCC/PLCC packages require adapters. These adapters are common for all programmers. Please contact BP Microsystems directly for availability of these adapters.*
4. *For further information please contact BP Microsystems directly at (713) 461-9430.*

Table 6-8 Data I/O

Part Number Package	Version (Family Code)		
	2900	UNIPAK 2B	AutoSite
Am27C64			
DIP	V1.0 (D6)	V23 (5C)	V3.6 (D6)
PLCC	V1.4 (D6)	V24 (5C)	V3.6 (D6)
Am27C128			
DIP	V1.0 (11D)	V23 (5C)	V3.6 (D6)
PLCC	V1.5 (D6)	V25 (5C)	V3.6 (D6)
Am27C256			
DIP	V1.0 (5C)	V23 (5C)	V3.6 (5C)
PLCC	V1.4 (5C)	V24 (5C)	V3.6 (5C)
Am27H256			
DIP	V1.7 (1DF)	V27 (D6)	V3.6 (1DF)
PLCC			
Am27C512			
DIP	V1.0 (5E)	V23 (5E)	V3.6 (5E)
PLCC	V1.4 (5E)	V24 (5E)	V3.6 (5E)
Am27C010			
DIP	V1.0 (D6)	V24 (5C)	V3.6 (D6)
PLCC	V1.2 (D6)	V24 (5C)	V3.6 (D6)
Am27H010			
DIP	V1.4 (D6)	V24 (5C)	V3.6 (D6)
PLCC			
Am27C100			
DIP	V1.0 (D6)	V20 (D6)	3.6 (D6)
Am27C1024			
DIP	V1.0 (5F)	V18 (5F)	V3.6 (5F)
PLCC	V1.5 (5F)	V25 (5F)	V3.6 (5F)

Table 6-8 Data I/O (continued)

Part Number Package	Version (Family Code) 2900	UNIPAK 2B	AutoSite
Am27C020			
DIP PLCC	V1.0 (D6)	V19 (D6)	V3.6 (D6)
Am27C2048			
DIP PLCC	V1.1 (5F) V1.9 (5F)	V21 (5F)	V3.6 (5F)
Am27C040			
DIP PLCC	V1.3 (D6)	V23 (5C)	V3.6 (D6)
Am27C400			
DIP PLCC	V2.0 (5F)		3.9
Am27C4096			
DIP PLCC	V2.0 (5F) V2.1 (5F)		1.1 1.5

Notes:

1. *Information listed above applies for all speed grades of that particular device/package.*
2. *The Am27H010 can be programmed by manually entering the pinout code for the Am27C010, as the silicon signature for these devices are the same.*
3. *The Am27H256 can be programmed by manually entering the pinout code for the Am27C256, as the silicon signature for these devices are the same.*
4. *All AMD EPROMs not specifically supported by Data I/O can be programmed using Intel's Quick-Pulse™ Programming algorithm. Intel's pin-out code must be manually entered as "Autoselect" will not work.*

Table 6-8 Data I/O (continued)

Part Number Package	Version (Family Code) UniSite 40	S1000	3900
Am27C64			
DIP	V3.2 (D6)	V19 (B5C)	V1.0 (D6)
PLCC	V3.3 (D6)*	V19 (B5C)	V1.0 (D6)
Am27C128			
DIP	V3.2 (D6)	V19 (B5C)	V1.0 (D6)
PLCC	V3.4 (D6)*	V20 (B5C)	V1.0 (D6)
Am27C256			
DIP	V3.2 (5C)	V18 (B5C)	V1.0 (5C)
PLCC	V3.3 (5C)*	V20 (B5C)	V1.0 (5C)
Am27H256			
DIP	V3.6 (1DF)	V23 (B5C)	V1.0 (1DF)
PLCC			V1.0 (D6)
Am27C512			
DIP	V3.2 (5E)	V19 (B5E)	V1.0 (5E)
PLCC	V3.3 (5E)*	V22 (B5E)	V1.0 (5E)
Am27C010			
DIP	V2.7 (D6)	V15 (D5C)	V1.0 (D6)
PLCC	V3.1 (D6)*	V20 (D5C)	V1.0 (D6)
Am27H010			
DIP	V3.3 (D6)	V19 (D5C)	V1.0 (D6)
PLCC			
Am27C100			
DIP	V2.7 (D6)	V14 (C5C)	V1.0 (D6)
Am27C1024			
DIP	V2.5 (5F)	V17 (5F)	V1.0 (5F)
PLCC	V3.4 (5F)*	V20 (5F)	V1.0 (5F)

Table 6-8 Data I/O (continued)

Part Number Package	Version (Family Code)		
	UniSite 40	S1000	3900
Am27C020			
DIP	V2.6 (D6)	V13 (D5C)	V1.0 (D6)
PLCC			
Am27C2048			
DIP	V3.0 (5F)	V16 (E5F)	V1.0 (5F)
PLCC	V3.8 (5F)*	V24 (E5F)	
Am27C040			
DIP	V3.2 (D6)	V19 (FD6)	V1.0 (D6)
PLCC			
Am27C400			
DIP	V3.9 (5F)	V26 (F5F)	V1.4 (5F)
PLCC			
Am27C4096			
DIP	V3.9 (5F)	V26 (F5F)	V1.4 (5F)
PLCC	V4.0 (5F)	V26 (F5F)	V1.5 (5F)

Notes:

1. *Information listed above applies for all speed grades of that particular device/package.*
2. *UNISITE 40 requires an optional PinSite Programming Module for PLCC Packages (marked with an *).*
3. *The 3900 programmer model requires an optional PLCC Package Base as it uses the Universal Package System™.*
4. *The Am27H010 can be programmed by manually entering the pinout code for the Am27C010, as the silicon signature for these devices are the same.*
5. *The Am27H256 can be programmed by manually entering the pinout code for the Am27C256, as the silicon signature for these devices are the same.*
6. *All AMD EPROMs not specifically supported by Data I/O can be programmed using Intel's Quick-Pulse™ Programming algorithm. Intel's pin-out code must be manually entered as "Autoselect" will not work.*

Table 6-9 ELAN

Part Number	Version 142	928	132 232 532 832 932	840 940	Adapter LCC	PLCC
Am27C64	E 5.00	E 5.00	E 5.00		A86A	A86
Am27C128	E 5.00	E 5.00	E 5.00		A86A	A86
Am27C256	E 5.00	E 5.00	E 5.00		A86A	A86
Am27H256						
Am27C512	E 5.00	E 5.00	E 5.00		A86A	A86
Am27C010	E 5.00		E 5.00		A104	A104
Am27H010						
Am27C1024	E 5.00			E 5.00	A94A	A94
Am27C020	E 5.01		E 5.01		A104	A104
Am27C2048	E 5.01			E 5.01	A94A	A94
Am27C040	E 5.01		E 5.01		A104	A104
Am27C400						
Am27C4096						

Notes:

1. *Information listed above applies for all speed grades of that particular device/package.*
2. *There is a reason for the "blanks" above due to the fact that each ZIFPAK model serves a specific DIP Package Pin-count (s) :*

Model	***DIP Package Pin-Count***
142	*28, 32 and 40 pins*
928	*28 pin*
132, 232, 532, 832 and 932	*28 and 32 pins*
840 and 940	*40 pin*

3. *All LCC and PLCC Packages require the specific adapter listed. Each adapter supports all ZIFPAK models listed for a specific device.*
4. *The Am27H010 can be programmed by manually entering the pinout code for the Am27C010, as the silicon signature for these devices are the same.*
5. *The Am27H256 can be programmed by manually entering the pinout code for the Am27C256, as the silicon signature for these devices are the same.*

Table 6-10 Logical Devices

Part Number Package	Version ALLPro 88/XR	Husky	GangPro -8+	GangPro-S Model II
Am27C64				
DIP	V2.1		V1.0	V1.0
PLCC	V2.1		V1.0*	V1.0*
Am27C128				
DIP	V2.1		V1.0	V1.0
PLCC	V2.1		V1.0*	V1.0*
Am27C256				
DIP	V2.2		V1.0	V1.0
PLCC	V2.2		V1.0*	V1.0*
Am27H256				
DIP	V2.2			
PLCC	V2.2			
Am27C512				
DIP	V2.2		V1.0	V1.0
PLCC	V2.2		V1.0*	V1.0*
Am27C010				
DIP	V2.2			
PLCC	V2.2			
Am27H010				
DIP	V2.2			
PLCC	V2.2			
Am27C100				
DIP				
Am27C1024				
DIP	V2.2			V1.0
PLCC	V2.2			

Table 6-10 Logical Devices (continued)

Part Number Package	Version			
	ALLPro 88/XR	Husky	GangPro -8+	GangPro-S Model II
Am27C020				
DIP	V1.5C	V2.10	V1.0	V1.0
PLCC	V1.5C	V2.10*	V1.0*	V1.0*
Am27C2048				
DIP	V2.2			V1.0-3
PLCC	V2.2			
Am27C040				
DIP	V2.2	V2.4R1	V1.1	V1.0
PLCC	V2.2	V2.4R1*	V1.1*	V1.0*
Am27C400				
DIP				
PLCC				
Am27C4096				
DIP	V2.2			V1.0-3
PLCC	V2.2			

Notes:

1. *Information listed above applies for all speed grades of that particular device/package.*
2. *The ALLPRO programmer model has PLCC Package programming capability.*
3. *The programmer models HUSKY and GANGPRO-8+ need separate adapters for PLCC Packages. These adapters are not currently offered by Logical Devices and need to be procured from third-party vendors. Please contact Logical Devices for additional information on these adapters.*
4. *The programmer model GANGPRO-S MODEL II needs a separate adapter – OPTGP2-E32 – for 32-pin PLCC Packages and is currently offered directly by Logical Devices. 44-pin PLCC Packages are currently not supported on this programmer.*
5. *The Am27H010 can be programmed by manually entering the pinout code for the Am27C010, as the silicon signature for these devices are the same.*
6. *The Am27H256 can be programmed by manually entering the pinout code for the Am27C256, as the silicon signature for these devices are the same.*
7. *For further information please contact Logical Devices directly at (305) 974-0967.*

Table 6-11 Stag Microsystems

Part Number Package	Pin-Out Code	Software Revision						
		39M101	41M101	41M102	41M111	41M121	42M101	ZM300
Am27C64	9FDA							
DIP		9.0	6.0				6.0	11.1
PLCC					6.0			11.1[1]
Am27C128	9FDB							
DIP		9.0	6.0				6.0	9.0
PLCC					6.0			9.0[1]
Am27C256	9FDC							
DIP		4.0	4.3				4.3	9.0
PLCC					4.3			9.0[1]
Am27H256								
DIP								
PLCC								
Am27C512	9FDD							
DIP		4.0	4.0				4.0	9.0
PLCC					4.0			9.0[1]
Am27C010	9FE1							
DIP		4.0	4.0				4.0	9.0
PLCC						4.0		9.0[1]
Am27H010								
DIP								
PLCC								
Am27C100	9FE3							
DIP		9.0	6.0			6.0	6.0	11.1
Am27C1024	9FF1							
DIP		4.0		5.0				10.0
PLCC								10.0[2]
Am27C020	9FE2							
DIP		7.0	6.0				6.0	8.0
PLCC						6.0		8.0[1]

Table 6-11 Stag Microsystems (continued)

Part Number Package	Pin-Out Code	Software Revision						
		39M101	41M101	41M102	41M111	41M121	42M101	ZM300
Am27C2048	9FF2							
DIP		7.0		6.0				11.1
PLCC								11.1[2]
Am27C040	9FE4							
DIP		10.0	7.0				7.0	
PLCC								
Am27C400								
DIP								
PLCC								
Am27C4096	9FF4							
DIP		9.0		6.0				11.3
PLCC								11.3[2]

Notes:

1. *Information listed above applies for all speed grades of that particular device/package.*
2. *There is a reason for the "blanks" above as each module serves a specific package and pin-count(s):*

Model	***Package***	***Pin-Count***
39M101	*DIP*	*28, 32 and 40 pins*
41M101	*DIP*	*28 and 32 pins*
41M102	*DIP*	*40 pin*
41M111	*LCC/PLCC*	*32 pin*
41M121	*LCC/PLCC*	*32 pin*
42M101	*DIP*	*28 and 32 pins*
ZM3000 (UNIVERSAL)	*All*	*All*

3. *PLCC Packages require separate adapters. The Legend for these adapters is as follows: [1] requires Zs3001 Adapter, [2] requires Zs3009 Adapter.*
4. *The Am27H010 can be programmed by manually entering the pinout code for the Am27C010, as the silicon signature for these devices are the same.*
5. *The Am27H256 can be programmed by manually entering the pinout code for the Am27C256, as the silicon signature for these devices are the same.*
6. *For further information please contact Stag Microsystems directly at (408) 988-1118 in the U.S. and 707-332148 in the U.K.*

Table 6-11 Stag Microsystems (continued)

Part Number	Software Revision			
	Orbit	Solar	Stratos 2	System 1040/84
Am27C64	3.7	1.0	1.2	10.41
Am27C128	3.7	1.0	1.2	10.41
Am27C256	3.7	1.0	1.2	10.41
Am27H256		1.0		
Am27C512	3.7	1.0	1.2	10.41
Am27C010	3.7	1.0	1.2	10.41
Am27H010		1.0		10.41
Am27C1024	3.7	2.0		10.41
Am27C020	3.7	1.0		10.41
Am27C2048		2.0		10.41
Am27C040		1.0	1.2	10.41
Am27C400				
Am27C4096		2.0		10.41

Notes:

1. *Information listed above applies for all speed grades of that particular device.*
2. *The Am27H010 can be programmed by manually entering the pinout code for the Am27C010, as the silicon signature for these devices are the same.*
3. *The Am27H256 can be programmed by manually entering the pinout code for the Am27C256, as the silicon signature for these devices are the same.*
4. *For further information please contact Stag Microsystems directly at (408) 988-1188 in the U.S. and 707-332148 in the U.K.*

SECTION

7 ARTICLE REPRINT

SEMICONDUCTOR MEMORIES

Making EPROM/flash trade-offs

By Datar Lalvani
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The non-volatile memory market, long the bastion of the UV EPROM, has been fissured with the recent emergence of in-system reprogrammable flash memories as a viable technology. Today, both EPROMs and flash memories coexist and they will continue to run parallel paths, with the choice of technology influenced by the requirements of the end product.

Flash memories were born of the marriage between EPROM and E²PROM devices. Flash incorporates the same programming capability as an EPROM with the added benefit of E²PROM-like electrical erasability, so it can be reprogrammed without removing it from the circuit board. This makes flash an ideal choice for applications that require in-system reprogrammability. While the same benefit can be obtained from either E²PROM or battery-backed SRAM, flash memories are less expensive than both.

In light of the projected rapid growth in demand for flash, the product-development plans announced by the ever-increasing number of vendors, and the recent public announcements by some large vendors—who have stated that their strategy is to "de-emphasize" EPROMs in favor of flash memories—the future of EPROMs has become unclear. This has caused some confusion in the memory marketplace. Technical factors such as scalability, die cost, erasure and package considerations—as well as market-based factors such as demand, applications and features—factor into the decisions to build and use either EPROM or flash products.

EPROMs and flash memories will coexist with the choice of technology influenced by the requirements of the end product as used by the customer. While some vendors have stated that flash memories are more scalable than EPROMs with the addition of double-layer metal,even down at 0.5-micron geometries, Advanced Micro Devices Inc. sees no need for multilayer metal for EPROMs. AMD's single-layer metal process for EPROMs using 0.5-micron technology not only will provide the high density—up to the 16-Mbit level—but is also capable of generating the smallest die size and highest performance in the industry.

It is a fact that, at the same density, the flash-memory die is more expensive than an EPROM because it has the slightly larger cell size required to support high endurance. Also, the flash process complexity is greater due to additional masking steps, and it requires longer test times to perform electrical erasure in the tester, as opposed to UV-erase in an oven.

Flash pricing today remains at a multiple of EPROM. However, flash pricing will continue to drop until it settles at around a 20 percent to 30 percent premium over a comparable EPROM. Memory designers are not going to increase the cost of their systems by using flash when there is no need for future reprogramming. In these designs, reprogrammability does not represent value to the customer. Consequently, flash technology will not ubiquitously replace OTP EPROM designs.

The market's demand for various price/performance products supports the coexistence of both EPROM and flash technology.

There is no question that flash technology has already reserved a bright spot in the history of non-volatile memories. In some designs, however, EPROM and flash memories can coexist comfortably. Laser-printer designs are becoming commodity-oriented items. Memory-design requirements are dictated by the pages-per-minute output of the printer. Memory designers can make a trade-off between designing interleaved systems with slower/less expensive devices or non-interleaved systems using faster/higher-cost devices. The software requirements for these systems are also fairly straightforward. Firmware that typically does not change in this system are the PCL-5 and/or Postscript engine-control codes.

In addition, the code for font types does not typically change. The density requirements for this code range from 2 to 4 Mbytes of storage, depending on the font types available and the number of scaling options. EPROMs instead of ROMs are used to provide manufacturing flexibility. The EPROMs are programmed just-in-time, depending on the printer engine and font options

Datar Lalvani holds a BSEE from the University of Madras, India, and an MBA from the Wharton Graduate School of Business, University of Pennsylvania. Kurt Wolf holds a BSEE from the University of Michigan.

16611A

Choosing flash or EPROM

Continued

required for that day's manufacturing run. Flash memory is then incorporated as an option that allows end users to store customized fonts or screen images in the printer. This eliminates the repetitive delay associated with transferring the bit-map-generated images between the computer and printer. This decrease in productivity is eliminated when the code is resident on the printer in flash memory, a clear example of a very high-volume product that requires both high-density EPROM and flash-memory devices.

Each technology is employed to take advantage of its strengths. OTP EPROMs are used in the most cost-sensitive portion of the memory system where the code typically does not change once the system is shipped. OTP EPROMs also allow for smooth transitions between manufacturing runs that incorporate different printer engines and/or font type options.

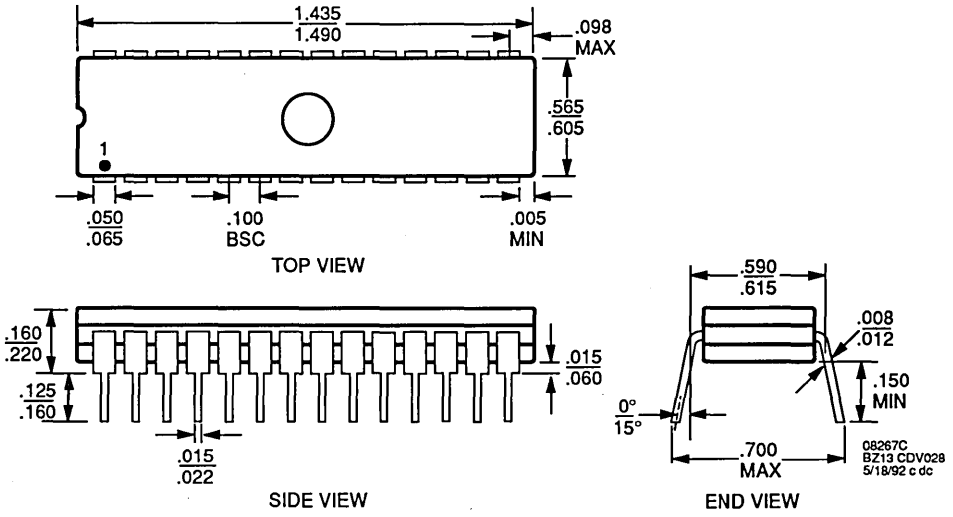
The higher-priced flash devices provide customers with the ability to personalize their systems. The value of this functionality more than offsets the incremental cost of the devices.

SECTION

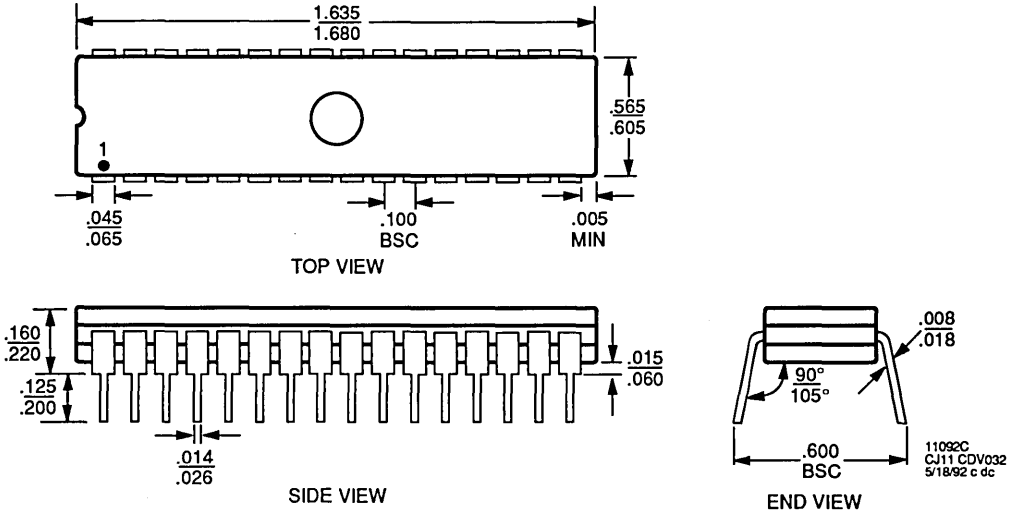
8 PHYSICAL DIMENSIONS*

**For reference only. BSC is an ANSI standard for Basic Space Centering.*

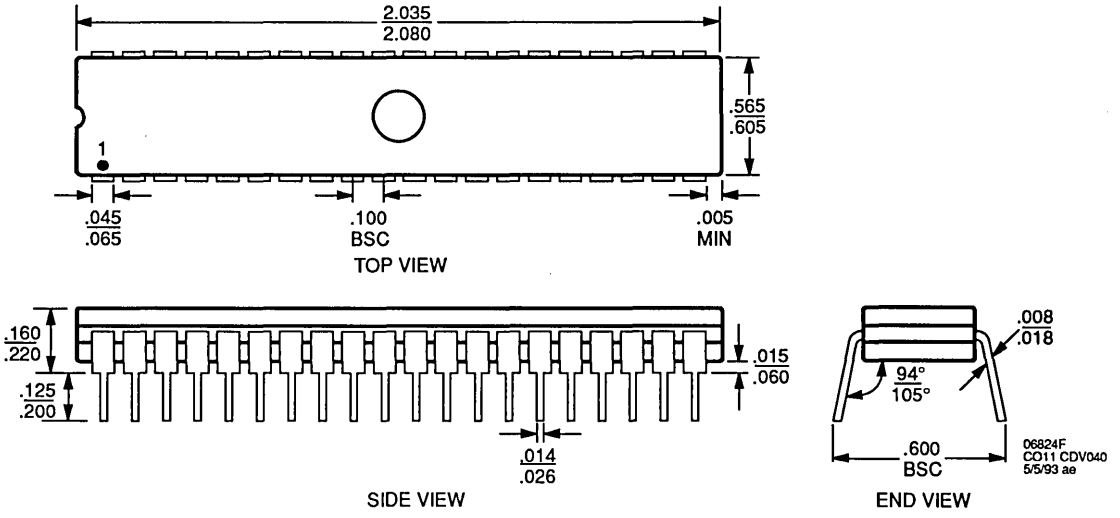
CDV028
28-Pin Ceramic DIP (measured in inches)



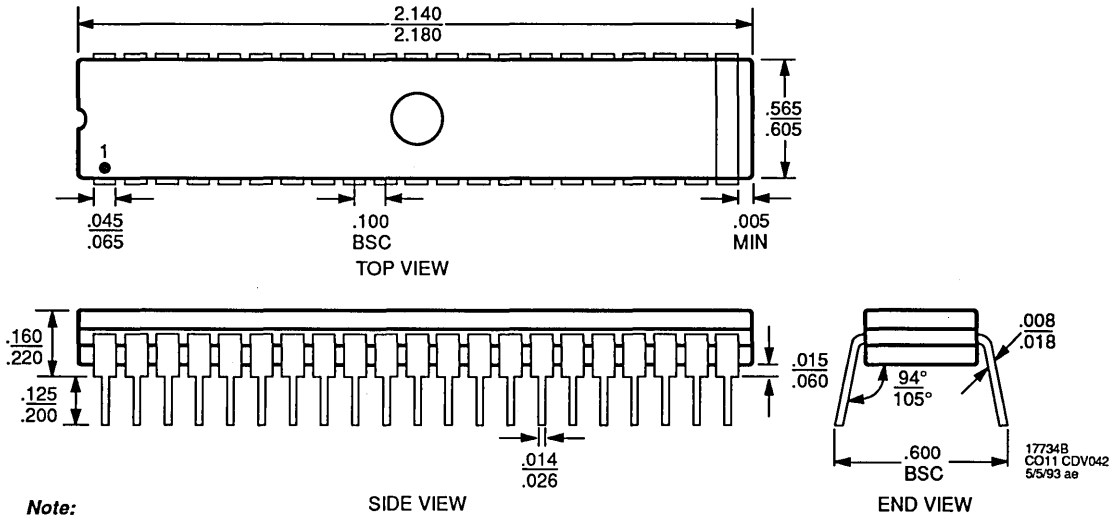
CDV032
32-Pin Ceramic DIP (measured in inches)



CDV040
40-Pin Ceramic DIP (measured in inches)

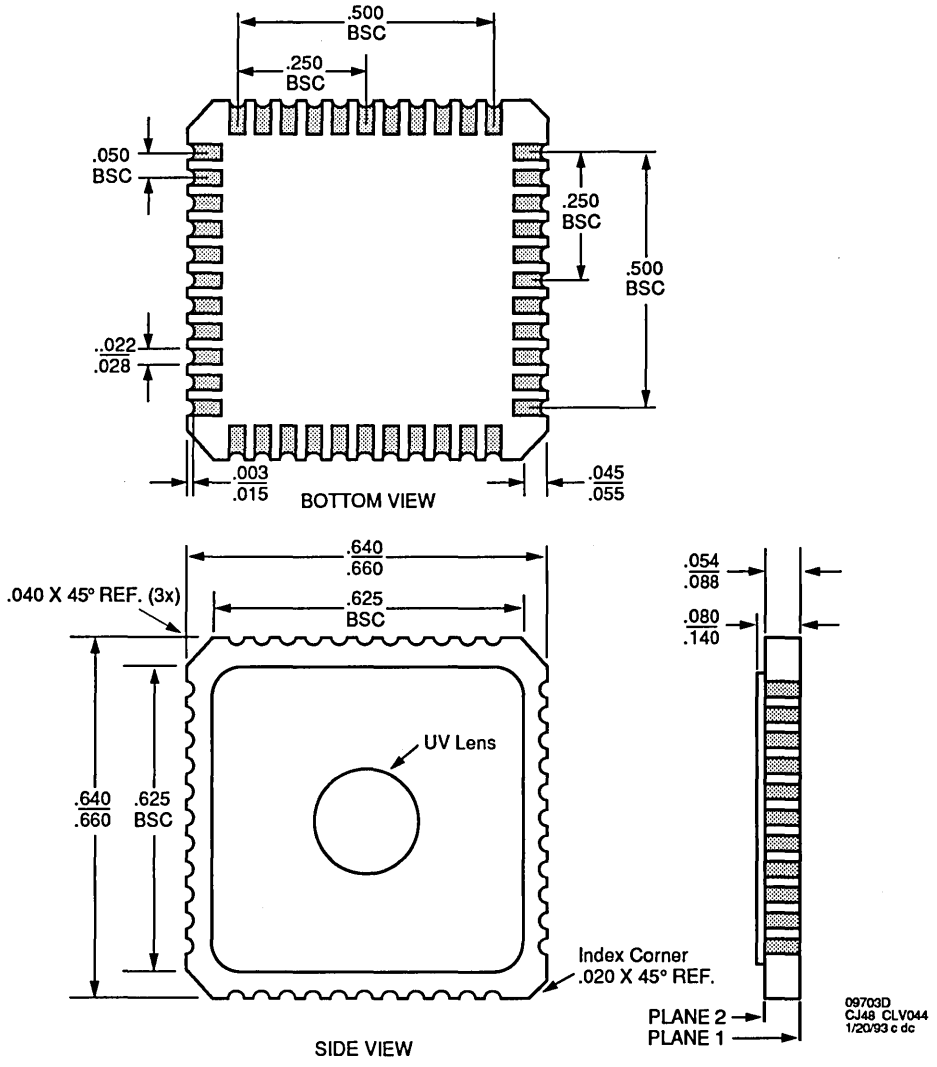


CDV042
42-Pin Ceramic DIP (measured in inches)

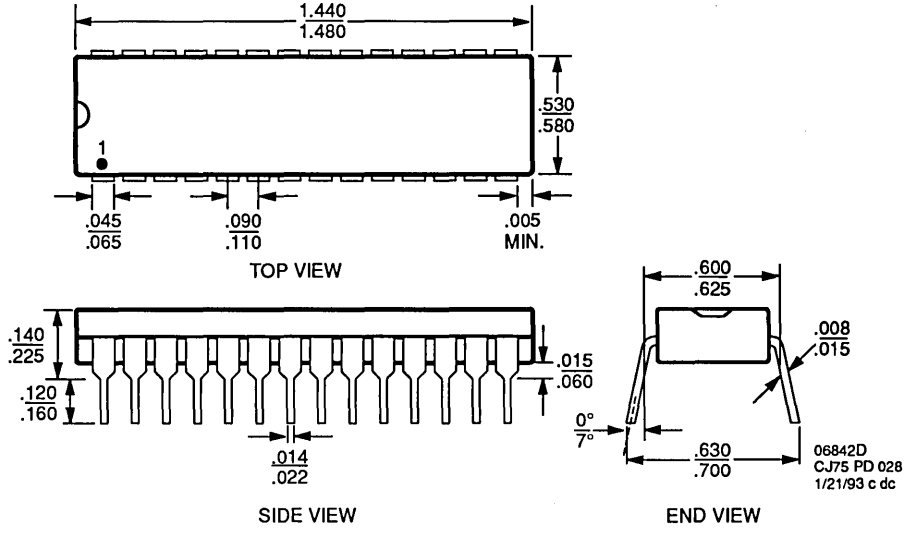


Note:
Package in development.

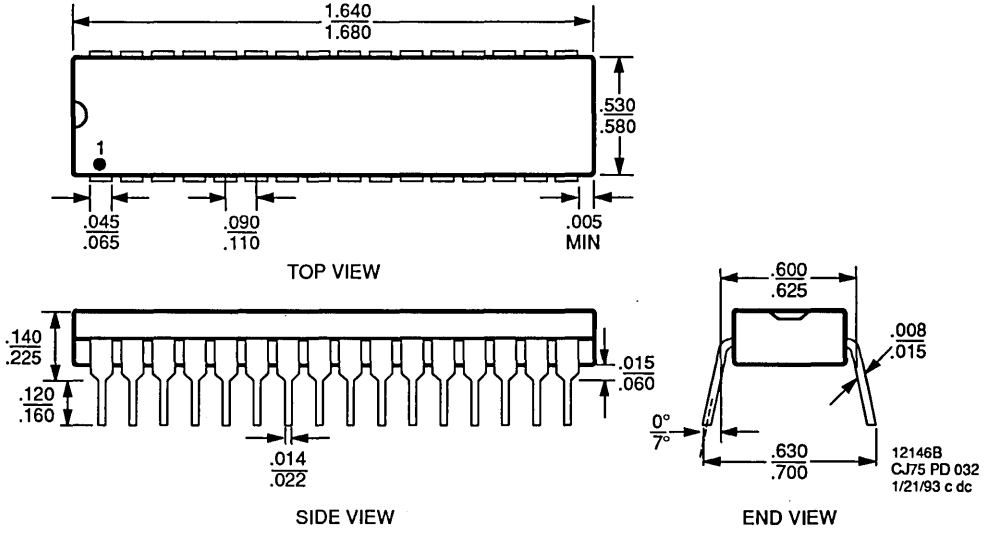
CLV044
44-Pin Square Ceramic Leadless Chip Carrier
(measured in inches)



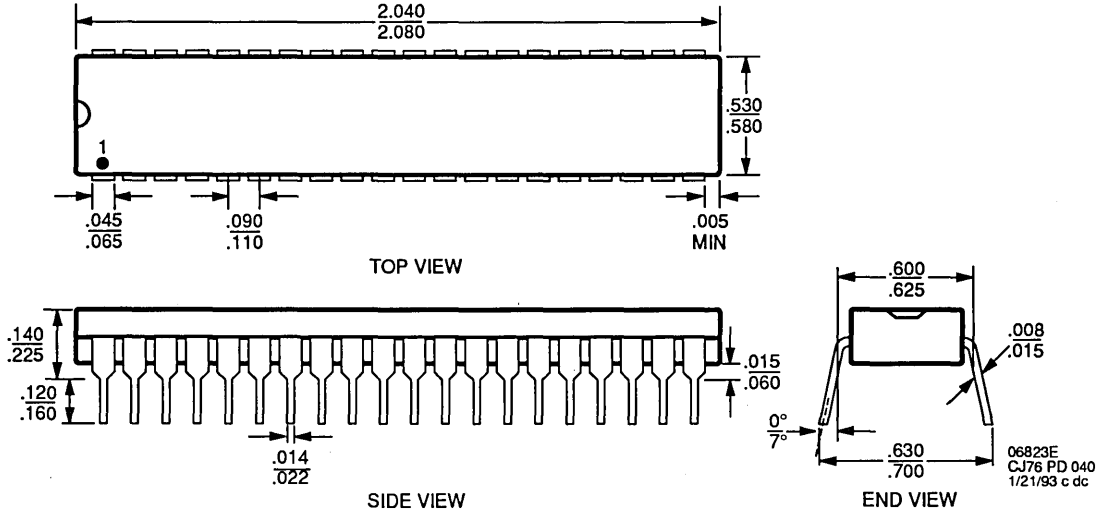
PD 028
28-Pin Plastic Dual In-Line Package (measured in inches)



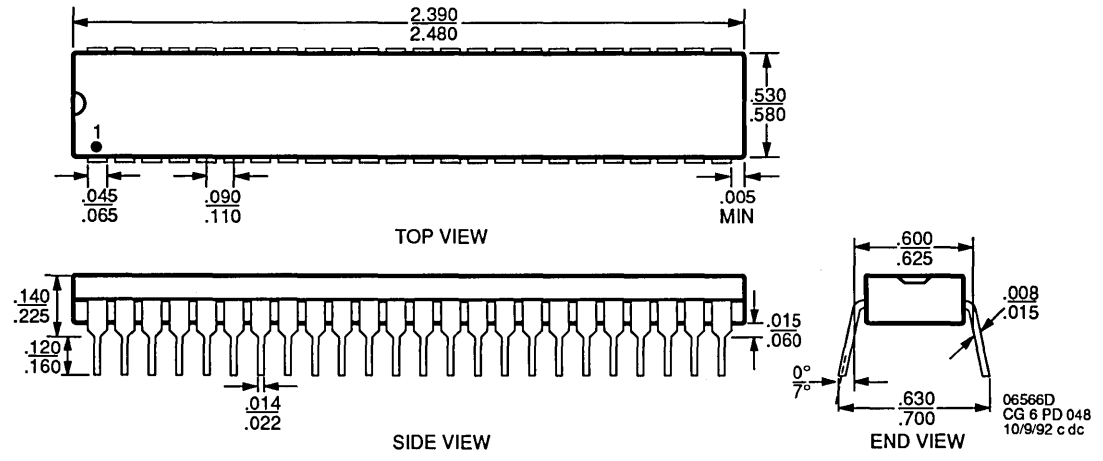
PD 032
32-Pin Plastic Dual In-Line Package



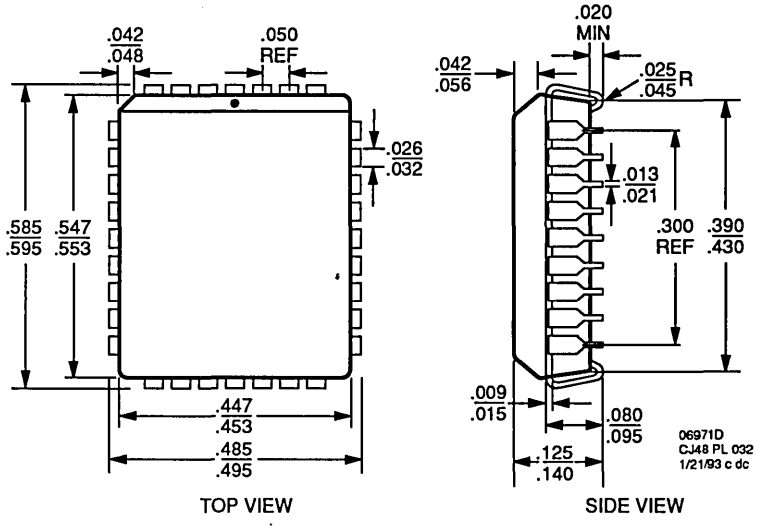
PD 040
40-Pin Plastic Dual In-Line Package (measured in inches)



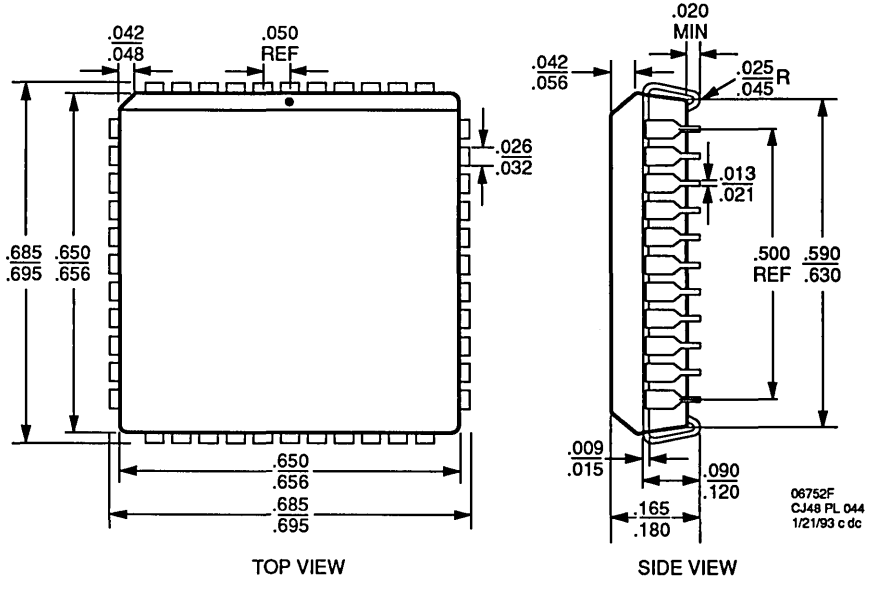
PD 048
48-Pin Plastic Dual In-Line Package (measured in inches)



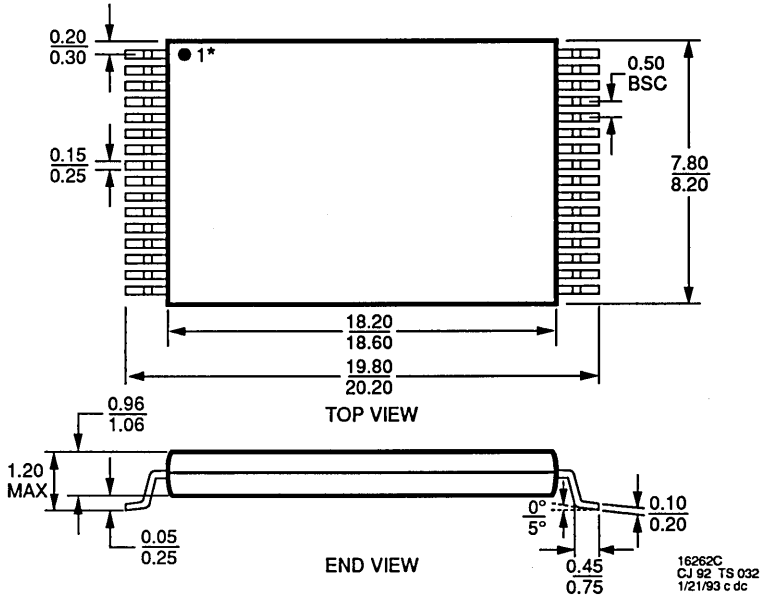
PL 032
32-Pin Rectangular Plastic Leaded Chip Carrier (measured in inches)



PL 044
44-Pin Square Plastic Leaded Chip Carrier (measured in inches)



TS 032
32-Pin Thin Small Outline (measured in inches)



**For the standard form/pin-out, the pin one is a round dimple. For the reverse form/pin-out, an inverted triangle will be marked here indicating pin one.*

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