Am9590

Hard Disk Controller (HDC)

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Supports ESDI, ST506/412, SMD, and IBM double-density floppy-disk drives
- Supports hard- and soft-sector formats
- Controls up to four drives, in any interface combinations
- Two on-chip sector buffers, up to 512 bytes, support zero-sector interleaving
- Error checking algorithms supported include:
  - CRC/CCITT
  - Single-Burst Reed-Solomon
  - Double-Burst Reed-Solomon
  - External ECC (Error Correction Code)
- Linked-list command and data structure
- On-chip DMA controller supports 32-bit addressing and 8/16-bit data
- Data rate up to 15 Mbits/second

GENERAL DESCRIPTION

The Am9590 Hard Disk Controller (HDC) is a single-chip solution to problems encountered in designing Data Formatters and Disk System Controllers. With its companion part, the Am9582 Disk Data Separator (DDS), the Am9590 provides all the functions which have been found only on sophisticated board-level products.

The Am9590 is flexible enough to cope with the differing requirements in today's broad marketplace while using the advanced technology and innovative features that tomorrow's market will demand.

The Am9590 supports both rigid- and flexible-disk drives and their data formats. The Am9590 can control up to four drives, allowing any combination of rigid and flexible drives. The characteristics of each drive are independently user-programmable.

A sophisticated on-chip DMA Controller fetches commands, writes status information, fetches data to be written on disk, and writes data that has been read from disk. DMA operation is programmable to adjust the bus occupancy, data bus width (8-bit or 16-bit), and Wait State insertions. Two sector buffers allow zero-sector interleaving to access data on physically adjacent sectors, improving both file access time and system throughput. Sector size is programmable for 128, 256, or 512 bytes.

The Am9590 insures data integrity by selecting either an error detecting code (CRC-CCITT), or one of two error correcting codes (Single- or Double- Burst Reed-Solomon). Additionally, the HDC provides handshake signals to control external ECC circuitry to implement any user-definable ECC algorithm.

The HDC disk interface directly supports ESDI hard- and soft- sectored disk drives. For ST506/412 and standard double-density floppy- disk interfaces, the HDC provides all the signals used by the Disk Data Separator (Am9582). By partitioning the disk control system into Hard Disk Controller and Disk Data Separator, future developments in the field of data encoding (e.g., RLL codes) will be able to take advantage of the HDC's advanced data formatting and control capabilities. Track format and interface timing are independently switchable, keeping the disk interface adaptable to other standards (e.g., SMD).

The Am9590 provides a comprehensive and high-level command set for multi-sector disk I/O, marginal data recovery, diagnostics, and error recovery. Commands may be linked together to be executed sequentially by the Am9590 without host intervention. This linked-list command structure also simplifies command insertion, deletion, or rearrangement.

Advanced Micro Devices

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08467	A	/0

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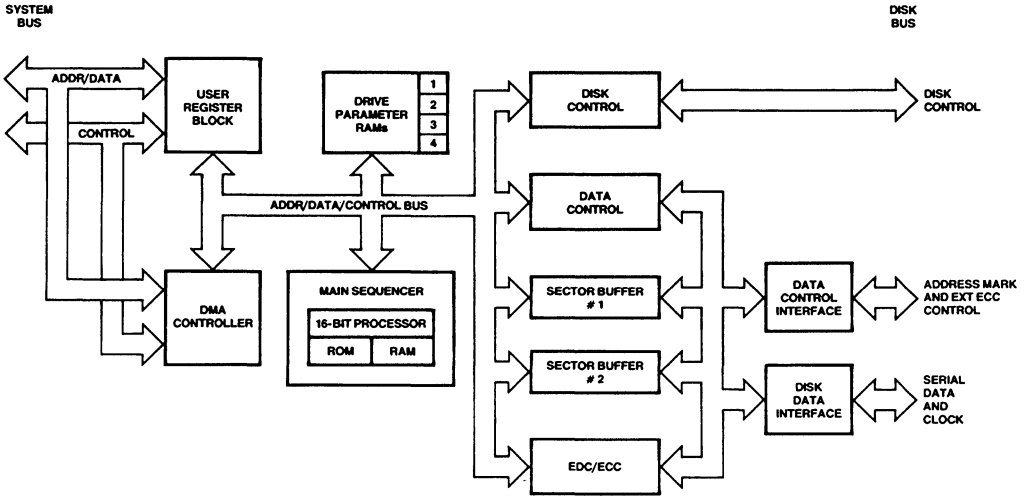
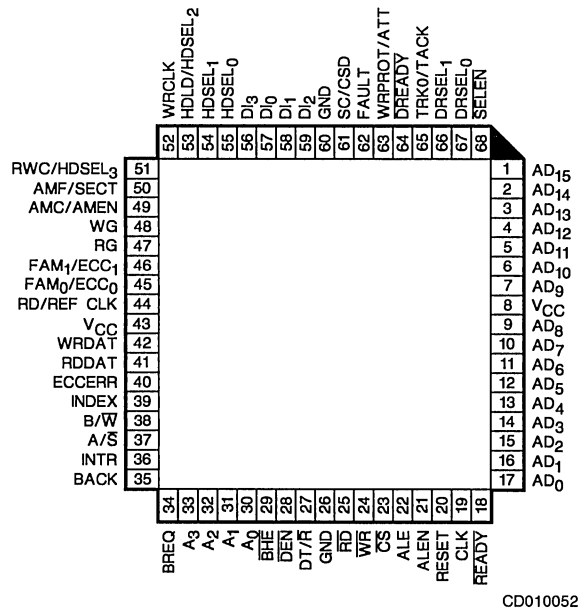
BLOCK DIAGRAM



BD004030

CONNECTION DIAGRAM
Top View



CD010052

Note: Pin 1 is marked for orientation.

Drive Interface Pin Cross References

Name	Pin #	Floppy	ST-506	ESDI (Serial)	Special
$\overline{SELEN}$	68	$\overline{SELEN}$	$\overline{SELEN}$	$\overline{SELEN}$	$\overline{SELEN}$
$DRSEL_1$	66	$DRSEL_1$	$DRSEL_1$	$DRSEL_1$	$DRSEL_1$
$DRSEL_0$	67	$DRSEL_0$	$DRSEL_0$	$DRSEL_0$	$DRSEL_0$
$\overline{DREADY}$	64	$\overline{DREADY}$	$\overline{DREADY}$	$\overline{DREADY}$	$\overline{DREADY}$
WRPROT/ATT	63	WRPROT	WRPROT	ATTENTION	—
FAULT	62	FAULT	FAULT	FAULT	FAULT
SC/CSD	61	SEEKCOMP	SEEKCOMP	CONFIGURATION/ STATUS DATA	SEEKCOMP
TRK0/TACK	65	TRK0	TRK0	TRANSFER ACKNOWLEDGE	—
DI3	56	PCEN	PCEN	—	TCLK
DI2	59	STEP	STEP	TRANSFER REQUEST	TDATA
DI1	58	DIRIN	DIRIN	COMMAND DATA	$HDSEL_5$
DI0	57	MOTOR ON	RTZ	COMMAND COMPLETE	$HDSEL_4$
$HDSEL_3$/RWC	51	RWC	$HDSEL_3$/RWC	$HDSEL_3$	$HDSEL_3$
HDLD/$HDSEL_2$	53	HDLD	$HDSEL_2$	$HDSEL_2$	$HDSEL_2$
$HDSEL_1$	54	—	$HDSEL_1$	$HDSEL_1$	$HDSEL_1$
$HDSEL_0$	55	SIDE	$HDSEL_0$	$HDSEL_0$	$HDSEL_0$
INDEX	39	INDEX	INDEX	INDEX	INDEX
AMC/AMEN	49	AMC	AMC	AMEN	AMC/AMEN
AMF/SECT	50	AMF	AMF	AMF/SECTOR	AMF/SECTOR
RG	47	RG	RG	RG	RG
WG	48	WG	WG	WG	WG
RD/REF CLK	44	RD/REF CLK	RD/REF CLK	RD/REF CLK	RD/REF CLK
WRCLK	52	—	—	WRCLK	WRCLK
WRDAT	42	WRDAT	WRDAT	WRDAT	WRDAT
RDDAT	41	RDDAT	RDDAT	RDDAT	RDDAT
ECC ERR	40	—	ECC ERR	ECC ERR	ECC ERR
ECC_1	46	IAMWR	ECC_1	ECC_1	ECC_1
ECC_0	45	—	ECC_0	ECC_0	ECC_0

PIN DESCRIPTION

V_{CC1}, V_{CC2} +5-V Power Supply
Both lines must be connected.

GND_1, GND_2 Ground
Both lines must be connected

System Interface Lines

CLK System Clock (Input)
CLK is a TTL-compatible clock input to time DMA transfers and disk- control operations (e.g., seeks). The system clock drives all except the Disk Data Section of the HDC.

$\overline{RD}$ Read (Input/Output; Active LOW, Three State)
A LOW on this line indicates that the CPU or HDC is performing an I/O or memory read cycle. When the HDC is in Slave Mode, this is an input signal used by the CPU to read the internal registers of the HDC (slave access). When the HDC is the bus master, this signal is an HDC output to access data from memory.

In Slave Mode, the transfer control signals, $\overline{RD}$ and $\overline{WR}$, must not be active simultaneously, but may be asynchronous to the clock. In Master Mode, the HDC drives this line synchronously by using a 4- clock-cycle transfer.

$\overline{WR}$ Write (Input/Output; Active LOW, Three State)
A LOW indicates that the CPU or HDC is performing an I/O, or memory write cycle. When the HDC is in Slave Mode, it is an input signal used by the CPU to load the internal registers of the HDC. When the HDC is the bus master, this signal is a HDC output to write data to the system memory. In Slave Mode, $\overline{RD}$ and $\overline{WR}$ must not be active simultaneously.

$\overline{BHE}$ Byte High Enable (Input/Output; Active LOW, Three State)
$\overline{BHE}$ enables data on the most significant byte of the data bus ($AD_{15}-AD_8$). The data bus is allocated as the following:

$\overline{BHE}$	A_0	Data Lines	Type
0	0	$AD_{15}-AD_0$	Word Transfer
0	1	$AD_{15}-AD_8$	Byte Transfer on Upper Byte
1	0	AD_7-AD_0	Byte Transfer on Lower Byte
1	1	–	None (Reserved)

When the HDC is the bus master, this pin is an output. When the HDC is the bus slave, it is an input and must be stable for the entire cycle. $\overline{BHE}$ is disabled and ignored when the HDC is strapped to a byte interface.

$\overline{READY}$ Ready (Input/Output; Active LOW, Open Drain)
When the HDC is in control of the system bus, this is an input to allow slow memories and peripheral devices to extend the bus cycle. When the HDC is in Slave Mode, this is an output indicating that the HDC is ready to complete the current bus transfer. The CPU $\overline{READY}/\overline{WAIT}$ input must be connected to the $\overline{READY}$ output of the Am9590 (in Slave Mode), because slave cycle length varies between 1 and 16 system clocks.

AD_0-AD_{15} Address/Data Bus (Input/Output; Active HIGH, Three State)
The Address/Data Bus is a time-multiplexed, bi-directional, three-state, 16-bit bus used for all system transactions. A HIGH represents a "1" on the bus and a LOW represents a "0". AD_0 is the least significant bit. The presence of an address is indicated by either ALE or ALEN. When ALE is HIGH, the bus contains lower address bits (A_0-A_{15}). When ALEN is HIGH, the bus contains upper address bits ($A_{16}-A_{31}$). The 32-bit address allows the HDC to directly access a linear (non-segmented) memory address space of up to 4 Gbytes.

The presence of data is indicated by the $\overline{RD}$, $\overline{WR}$, and $\overline{READY}$ signals. The HDC drives data out onto the AD-bus (lines are configured as outputs) when $\overline{RD}$ is asserted in Slave Mode, or when $\overline{WR}$ is asserted in Master Mode. The HDC reads data in from the AD- bus (lines are configured as inputs) when $\overline{WR}$ is asserted in Slave Mode, or when $\overline{RD}$ is asserted in Master Mode.

Mode	$\overline{RD}$	$\overline{WR}$	$AD_{15}-AD_0$
Slave	L	H	Output
Slave	H	L	Input
Master	L	H	Input
Master	H	L	Output

A_0 Address Line 0 (Input; Active HIGH)
When the HDC is in Slave Mode, a HIGH on this address line selects the upper byte of internal registers, a LOW selects the lower byte of internal registers. For word accesses, this line must be LOW. A_0-A_3 must be valid through the Read or Write cycle. In Master Mode, this line is ignored.

A_1-A_3 Address Lines 1-3 (Inputs; Active HIGH)
When the HDC is in Slave Mode, these lines select one of the internal registers (see Figure 4). In Master Mode, these lines are ignored.

ALE Address Latch Enable (Output; Active HIGH)
ALE latches the lower address word (A_0-A_{15}) onto the external address latch. This output is never floating.

ALEN Upper Address Latch Enable (Output; Active HIGH)
ALEN latches the upper address word ($A_{16}-A_{31}$) onto the external address latch. This signal is active whenever the upper address is to be updated. The upper address is not updated at the begin of each DMA burst; therefore, the upper address latch must not be shared with the CPU or other DMA devices. This output is never floating. (See also "System Interface" Section)

DT/$\overline{R}$ Data Transmit/$\overline{Receive}$ (Output; Three State)
In Master Mode, this output indicates the direction of data flow. A HIGH indicates that the data is being transmitted from the HDC to memory (master write cycle). A LOW indicates that the data is being transferred from memory to the HDC (master read cycle). This output is floating when the HDC is not in control of the system bus.

$\overline{DEN}$ Data Enable (Output; Active LOW, Three State)
When the HDC is bus master, a LOW on this output enables an external data bus transceiver (DT/$\overline{R}$ specifies the direction). $\overline{DEN}$ is active when data is driven onto the Address/Data bus (master write cycle), or the bus is three-stated when receiving the data (master read cycle). This output is three-stated when the HDC is not in control of the system bus.

BREQ Bus Request (Output; Active HIGH)
The HDC activates BREQ to request for control of the system bus. BREQ timing is specified by the DMA Burst Length and DMA Dwell Time parameters in the Mode Register.

BACK Bus Acknowledge (Input; Active HIGH)
BACK acknowledges the HDC bus request, indicating that the CPU has relinquished the system bus to the HDC. Since BACK is internally synchronized, transitions on BACK do not have to be synchronous with the system clock (CLK). BACK may be removed, at any time, to make the HDC release the

bus (bus preemption). If the HDC DMA is preempted by removing BACK, HDC completes the current bus transaction and releases BREQ for the programmed dwell time so that external devices may gain system bus mastership.

INTR Interrupt Request (Output; Active HIGH)
INTR is activated when the HDC requires CPU service. Interrupt Request is reset whenever the upper byte (Status Byte) of the Status/Command Register (SCR) is accessed. The HDC asserts INTR after a hardware or software reset to indicate that the internal reset process has been completed. This interrupt cannot be disabled. Further interrupts are issued whenever the HDC enters the IDLE state (e.g., terminating a command chain). These interrupts may be disabled by resetting the Interrupt Mask in the Mode Register. The INTR output is never floating.

$\overline{CS}$ Chip Select (Input; Active LOW)
The host processor activates $\overline{CS}$ to enable a Slave Mode access to read or write HDC internal registers. $\overline{CS}$ may be asynchronous to the system clock (CLK). This pin is ignored when the HDC is in Master Mode.

B/$\overline{W}$ Byte/$\overline{Word}$ Strap (Input)
This pin selects either a byte (8-bit) (B/$\overline{W}$ HIGH) or word (16- bit) (B/$\overline{W}$ LOW) interface. When a byte interface is selected, only $AD_0 - AD_7$ are used for data transfers, making all operations byte operations. When word interface is selected, $AD_{15} - AD_0$ are used for data transfers. This input may be altered only while the HDC is in IDLE state.

HIGH = Byte interface
LOW = Word interface

A/$\overline{S}$ Asynchronous/$\overline{Synchronous}$ (Input)
This input selects whether the $\overline{READY}$ input is synchronous or asynchronous to the system clock (CLK). When A/$\overline{S}$ is HIGH, the HDC internally synchronizes the $\overline{READY}$ input. When A/$\overline{S}$ is LOW, $\overline{READY}$ must be synchronized externally. This input may only change state while the HDC is in IDLE state.

RESET Reset (Input; Active HIGH)
When RESET is active, all outputs lines are inactive, all three- state outputs are floating, and all inputs other then RESET are ignored. With the falling edge of RESET, the chip enters the initialization procedure. A RESET pulse is required after power-up. Upon completion of initialization, an interrupt request will be issued and INTR will go HIGH. If the user attempts to read from, or write to, the HDC prior to completion of reset, the $\overline{READY}$ output will remain inactive until the reset has been completed; this causes the CPU to wait. After an initial hardware reset, a software reset (loading the Command Status field of the Status/Command Register with RESET) is equivalent to a hardware reset (pulse on the RESET input).

Power-up reset must be active after V_{CC} has been stable for a certain period (see AC specification). This can be achieved by a long reset pulse generated by a RC circuit during power-up, or by a short pulse after power-up. The HDC must capture the Reset input being LOW for two rising edges of the system clock (2 plus system clocks pulse width).

Disk Interface Lines

$\overline{SELEN}$ $\overline{Select\ Enable}$ (Output; Active LOW)
$\overline{SELEN}$ = LOW enables the drive specified by $DRIVE_{0,1}$. When $\overline{SELEN}$ = HIGH, no drive is selected. The disk drive must respond to $\overline{SELEN}$ LOW by bringing $\overline{DREADY}$ LOW. See $\overline{DREADY}$ and MON descriptions below.

$DRSEL_{0,1}$ Drive Select (Outputs; Active HIGH)
$DRSEL_{0,1}$ designates which of the four possible drives is expected to respond to the assertion of $\overline{SELEN}$.

$DRIVE_1$	$DRIVE_0$	Drive Selected
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

$DRSEL_0$ and $DRSEL_1$ are the two least-significant bits of the drive number specified in the IOPB.

DI_3 Disk Interface Control 3 (Output; Active HIGH)
(PCEN) Precompensation Enable — This output indicates whether the data write encoder should initiate pre-compensation on the encoded disk-write data pulse stream. PCEN will be valid for at least four system clocks prior to any disk-write operation ($\overline{WG}$ LOW), and will remain valid for at least four system clocks after the disk-write operation ($\overline{WG}$ HIGH). PCEN is asserted if the current track number is greater than, or equal to, the Pre-compensation Track Parameter specified in the Drive Parameter Block for the selected drive. No other internal processing takes place.

HIGH = Pre-compensation enabled
LOW = Pre-compensation disabled

PCEN should be connected to PCEN/S($\overline{D}$) of the Am9582, even if pre-compensation is not used. When $\overline{SELEN}$ is asserted, this output is pulsed LOW to select Double-Density Floppy Mode.

TCLK) Track # Clock — In Restricted Seek Mode, and Special Mode, this output provides the shift clock for the serial track information provided on TDATA. See the following description on DI_2.

$\overline{DREADY}$ $\overline{Drive\ Ready}$ (Input; Active LOW)
Drive Ready indicates that the currently selected drive is ready to Read, Write, or Seek. It must become LOW within 10 ms (100,000 system clocks) after $\overline{SELEN}$ is asserted by the HDC (see Motor-on Description for Floppy Mode). Once asserted by the selected drive, any negation of this line causes the current IOPB to be aborted. $\overline{DREADY}$ is ignored while $\overline{SELEN}$ is HIGH. $\overline{DREADY}$ must be deasserted within 100,000 system clocks after $\overline{SELEN}$ is deactivated. This input is not used if SMD interface is selected.

FAULT Fault (Input; Active HIGH)
For ST506, floppy, and SMD operation, this indicates a fault in the selection of the current drive, or a fault within the selected drive. For normal operations, FAULT must be inactive (LOW) as long as $\overline{DREADY}$ is active (LOW). FAULT is considered valid after $\overline{DREADY}$ is asserted. If it is asserted by the selected drive, the HDC will immediately abort the current IOPB and de-selects the drive.

For ESDI interface, this pin has to be inactive during a read, write, or seek operation. If it is asserted during a read, write, or seek, the HDC will immediately abort the current IOPB and de-selects the drive. It is disregarded during a serial communication.

WRPROT/ATT Write Protected/Attention (Input; Active HIGH)
(WRPROT) Write Protected — Before the HDC attempts to write data to the currently selected drive, the HDC samples WRPROT to determine whether the drive is write protected (WRPROT HIGH). If it is, the current IOPB is immediately aborted. Typically, in Hard-disk Mode, this input should be tied LOW (inactive), and is considered valid after $\overline{DREADY}$ is asserted. It is ignored during "Ready Only"-type commands. When $\overline{SELEN}$ is inactive (HIGH), this input is also ignored.

(ATT) Attention — For ESDI interface, this line has to be valid after $\overline{\text{DREADY}}$ becomes active. With this signal, an ESDI drive indicates to the controller that status information can be read from the drive (usually this is an error condition). If Attention becomes active when the HDC attempts a read or write operation, the HDC will abort immediately and de-selects the drive.

SC/CSD Seek Complete/Configuration Status Data (Input; Active HIGH)

(SC) Seek Complete — The drive asserts SC to indicate to the HDC that the head is loaded (only for Floppy Mode) and the drive is ready for another Seek operation. This line is sampled and verified HIGH before starting any seek operation.

(CSD) Configuration Status Data — If the ESDI interface (Serial Mode) is selected, this line is the serial data input for configuration/status information from the drive.

DI_2 Disk Interface Control 2 (Output; Active HIGH)

Step — The HDC pulses the STEP line to move the head from one track to the next. The width and spacing of pulses are programmable, allowing an easy upgrade path to higher performance drives. The disk drive should initiate the head movement with the rising edge of STEP. SC (Seek Complete) must go inactive after the HDC has issued the first step-pulse.

Transfer Request — For ESDI interface, the HDC uses this pin to request a data transfer (one bit at a time) to or from the drive. If data are transferred to the drive, the pin is activated when a command bit is present on the Command/Data line. It is deasserted after the ESDI disk drive responds with TACK (Transfer Acknowledge). If data are received from the drive, TRQ indicates that the HDC is ready to receive a bit from the drive. Again, REQ is deasserted with the reception of TACK.

(TDATA) Track Data — In Restricted Seek Mode, and Special Mode, TDATA provides the current track number (16-bit) each time the track number needs to be updated. A shift clock is available on the DI3 output.

DI_1 Disk Interface Control 1 (Output; Active HIGH)

(DIRIN) Direction In — DIRIN indicates the direction the head should move on STEP pulses. When HIGH, the head should move towards higher track numbers (in, or towards the disk spindle). When LOW, it should move towards lower track numbers (Out). DIRIN will be asserted at least four clock cycles before any seek pulses are issued. It remains stable during the entire stepping operation until at least four clock cycles after the last step-pulse.

Command Data — For the ESDI interface, the Am9590 uses this pin to send serial ESDI command words, plus parity, to the disk drive.

($HDSEL_5$) Head Select 5 — For the Special interface, this is the most-significant bit of the head number.

DI_0 Disk Interface Control 0 (Input/Output; Active HIGH)

(RTZ) Return To Zero — In Hard-disk Mode, a pulse on the RTZ output should re-calibrate the head to Track 0. The HDC may also re-calibrate the drive by issuing STEP pulses until Track 0 is reached (TRK0 becomes active). The RTZ pulse has the same width as the STEP pulse. The drive should assert SC (Seek Complete) as an indication of the completion of the requested re-calibration. If the drive asserts SC (LOW), and TRK0 is LOW, the Am9590 will assume that re-calibration has failed. In this case, the HDC continues to re-calibrate the drive by issuing STEP pulses until Track 0 is reached (TRK0 becomes HIGH).

Motor On — In Floppy Mode, this output provides Motor-On signal for the floppy-disk drive. Whenever a floppy-disk drive is selected and MON is asserted HIGH, this turns on the spindle motor of the selected drive(s). The HDC waits for a programmed period before attempting any read or write access to the drive (see Drive Parameter Block description).

Command Complete — In ESDI Mode, this input indicates to the HDC whether the drive has completed a command or if a new command may be issued. Command Complete goes inactive upon the reception of the first Command Data bit. It stays inactive until the command has been executed. Command Complete is also monitored after a head change during disk- data transfers. This allows the drive to have any head-settle time that is required.

($HDSEL_4$) Head Select 4 — For Special interface this is the second-most significant bit of the head number.

TRK_0/TACK Track 0/Transfer Acknowledge (Input; Active HIGH)

(TRK_0) Track 0 — The selected drive must assert TRK0 whenever the head is positioned over the outer-most track (Track 0). This is the only hardware indicator that the head is positioned over a specific track. This input is sampled only when the HDC is performing a drive restore operation. Here, the HDC provides single step-pulses (DIRIN LOW), waits for SC to go inactive (LOW), returns to active (HIGH), and then samples TRK_0. Whenever TRK_0 is asserted, the HDC assumes that the heads have restored to Track 0.

(TACK) Transfer Acknowledge — For the ESDI interface, this pin, with TREQ (Transfer Request), handles the asynchronous handshake for the serial command transfer between Am9590 and ESDI hard-disk drive.

RWC/$HDSEL_3$ Reduced Write Current/Head Select 3 (Output; Active HIGH)

(RWC) Reduced Write Current — RWC indicates that the head is over an inner track where the write current should be reduced. RWC is activated whenever the current track number is greater than, or equal to, the RWC track parameter, specified in the Drive Parameter Block for each drive. No internal processing of RWC takes place in the HDC. RWC operation is similar to that of Pre-compensation Enable (PCEN). If RWC is used to control the write current, the write current should be reduced when RWC goes active (HIGH). A programmable option bit within the Drive Parameter Block configures this output.

($HDSEL_3$) Head Select 3 — This pin provides Bit 3 of the head number.

HLD/$HDSEL_2$ Head Load/Head Select 2 (Output; Active HIGH)

(HLD) Head Load — For floppy drives, this pin provides the Head Load signal. SC (Seek Complete) is sampled eight clocks after the assertion of HLD. If SC is LOW the HDC waits for it to go HIGH. If SC is HIGH the HDC assumes that the heads are already loaded.

($HDSEL/_2$) Head Select 2 — For hard-disk drives, this pin provides Bit 2 of the head number.

$HDSEL_{1,\ 0}$ Head Select (Output,Active HIGH)

These are the two lower-order bits of the head number selected.

INDEX Index (Input; Active HIGH)

INDEX marks each revolution of the disk. INDEX should be valid as long as $\overline{\text{DREADY}}$ is asserted. The HDC uses INDEX to keep track of the number of complete disk revolutions encountered during disk I/O operations and/or to indicate the physical beginning of the track. Only the leading (rising) edge of INDEX is significant. Depending on the drive

parameters programmed, the first sector might begin before INDEX has gone inactive (LOW).

AMC/AMEN Address Mark Control/Address Mark Enable (Output; Active HIGH)

(AMC) Address Mark Control — The HDC asserts AMC in conjunction with RG or WG, to command the external data separator to generate address marks (write operation), or to search for address marks (read operation). In either operation the data separator acknowledges the completion of the requested operation by asserting AMF. In write cycles, this signal indicates that the address mark has been generated. The type and length of the address mark is completely transparent to the HDC. The data separator may, therefore, generate any address mark. In read cycles, AMF indicates that an address mark has been found.

(AMEN) Address Mark Enable — For the ESDI interface, this pin causes the ESDI drive to either write an address mark (in conjunction with WG) or to search for an address mark (no RG activated).

AMF/SECT Address Mark Found/Sector (Input; Active HIGH)

(AMF) Address Mark Found — In ST506 mode the data separator asserts AMF, in response to AMC, to acknowledge that an address mark has been generated (write cycle) or found (read cycle). In ESDI mode (soft-sectored) the disk drive generates AMF. The AMF signal must be asserted in the RD/REF CLK cycle after the data separator has put out the last address mark bit (write cycle), or in the RD/REF CLK cycle when the data separator provides the first data bit after the address mark (read cycle).

(SECT) Sector — For hard-sectored ESDI drives this signal indicates to the Am9590 the start of a new sector.

RG Read Gate (Output; Active HIGH)

RG indicates that a disk-read operation is in progress. It commands the Phase Locked Loop (PLL) of the data separator to lock the RD/REF CLK to the serial read data from disk. This output changes synchronously with RD/REF CLK.

WG Write Gate (Output; Active HIGH)

WG indicates that a disk-write operation is in progress. It commands the data separator to lock the RD/REF CLK to a constant frequency source (e.g., crystal oscillator) to provide a stable reference clock for the write operation. This output changes synchronously with RD/REF CLK.

RD/REF CLK Read/Reference Clock (Input)

RD/REF CLK is a TTL-compatible clock input which controls the operation of the data section of the HDC. This clock samples the read data (read clock) and strobes out write data (reference clock). It is assumed to be valid 16 system clocks (CLK) after drive selection acknowledge (DREADY) is received, and must remain valid until $\overline{\text{SELEN}}$ is deasserted. While valid, this clock should be free from any glitches (the specified clock HIGH and LOW widths must not be violated).

WRCLK Write Clock (Output)

This is the reference clock output for ESDI write operations. It is inverted from, and synchronous to, the reference clock input (RD/REF CLK). WRCLK must not be connected to the Am9582 write clock input.

RDDAT Read Data (Input; Active HIGH)

RDDAT is the NRZ (Not Return to Zero) disk data input. The HDC samples RDDAT with the rising edges of RD/REF CLK.

WRDAT Write Data (Output; Active HIGH)

WRDAT is the NRZ disk data output. Transitions occur on the rising edge of RD/REF CLK.

ECCERR External ECC Error (Input; Active HIGH)

When using the external ECC option, this input is asserted when the external ECC logic finds an error. During a read operation, the Am9590 samples ECCERR at the end of Postamble 2 to determine if an error has been detected by the external ECC logic. This input is ignored for write operations and when external ECC is disabled (see Drive Parameter Block description).

FAM_0/ECC_0 Floppy Address Mark 0/External ECC Control 0 (Output; Active HIGH)

FAM_1/ECC_1 Floppy Address Mark 1/External ECC Control 1 (Output; Active HIGH)

When using the external ECC option, the outputs ECC_0 and ECC_1, in conjunction, provide status control for the external ECC logic. These dual-function lines either control external ECC (hard-disk format, external ECC enabled) or indicate the type of address mark to be used (double-density floppy format, AMC HIGH). The four states are encoded as follows:

ECC Controls

ECC_1, ECC_0	State	Comment
00_B	Idle	No operation in the external ECC.
01_B	Reset	External ECC should reset and prepares itself for an operation.
11_B	Generate	Whether reading or writing, the external ECC should strobe data in and generates a check-sum.
10_B	Check	When reading, this state indicates that the ECC should accept the check-sum from the disk. When writing, it should gate the check-sum to the disk.

These states always proceed in the Gray code progression shown above; i.e., 00-01-11-10-00, which can be decoded without glitches. The nominal state of the HDC is 00 (Idle).

In Double-Density Floppy Mode, the Floppy Address Mark outputs (FAM_0, FAM_1), in conjunction, tell the data separator to generate an Index Address Mark (IXAM) rather than a normal address mark. The two states that can be encoded are as follows:

00 = Index Address Mark (IXAM)
XX = Data Field or Header Address Mark (DAM, IDAM)

FUNCTIONAL DESCRIPTION

Enhancements to the Am9580A

The Am9590 Hard Disk Controller is an enhanced version of the Am9580A, Hard Disk Controller. It provides the same CPU interface, the same DMA structure, and the same high-level command set as the Am9580A.

Similar to the Am9580A, the disk interface of the Am9590 supports the IBM double-density floppy interface as well as the ST506 hard-disk drive interface. In addition to these interfaces, the Am9590 connects directly to ESDI (Enhanced Small Device Interface) hard-disk drives. Because the controller implements the ESDI data format as well as the serial command interface to the disk drive, the Am9590 is transparent to the CPU.

The ESDI Interface

The ESDI (Enhanced Small Device Interface) standard allows a flexible and high performance interface between hard-disk controller and drive. It is specifically designed to interface high-capacity, small, hard-disk drives.

ESDI provides two major enhancements over ST506:

ESDI specifies the data transferred, between the controller and the hard-disk drive, to be NRZ data. Thus, implementing the data separator on the drive, data encoding and decoding is handled by the drive. The typical encoding scheme for an ESDI drive is a form of run-length limited code. The very close coupling between DDS logic and drive electronic also increases reliability because additional cables and line drivers are not required. The ESDI drive determines the disk data rate by providing Reference and Read Clocks for the disk controller.

The ESDI interface defines a serial command/status link between the controller and disk drive. The ST506 step pulse scheme is replaced by SEEK and RESTORE commands which allow fast head positioning. The Am9590 issues these commands automatically for all disk operations. These commands are 17-bit serial data words which are transferred asynchronously with a bit-by-bit handshake.

The ESDI command/status interface provides added functionality over the ST506. There is a drive self-test function implemented and Status information can be requested from the disk drive to get details on error conditions. ESDI can also get the drive configuration from the disk drive. In other words, the drive provides all parameters, such as the number of cylinders, heads, etc. to initialize the controller. The CPU must initiate the necessary steps to call the required features up, and the Am9590 provides the hardware interface.

There are two methods to achieve higher storage capacity in disk drives. The first is to increase the number of surfaces. The second is to increase the storage density on each surface. The second method requires either an increase in data rate or a reduction in rotation speed.

ESDI achieves higher storage capacity by supporting both methods. It has a high number of heads per drive (64) and a high data rate (up to 15 Mbits/sec).

Overview

The Am9590 HDC supports the two interfaces shown in the block diagram. The system interface (see Figure 1) communicates with the host CPU and system memory. The disk interface controls the data separator and the disk drives.

System Interface

The HDC is designed for easy interfacing to most 8-bit or 16-bit, multiplexed or demultiplexed, synchronous or asynchronous, microprocessor buses. A strap pin programs the system interface for either byte (8-bit) or word (16-bit) mode. In Slave Mode, the on-chip DMA controller controls the system bus.

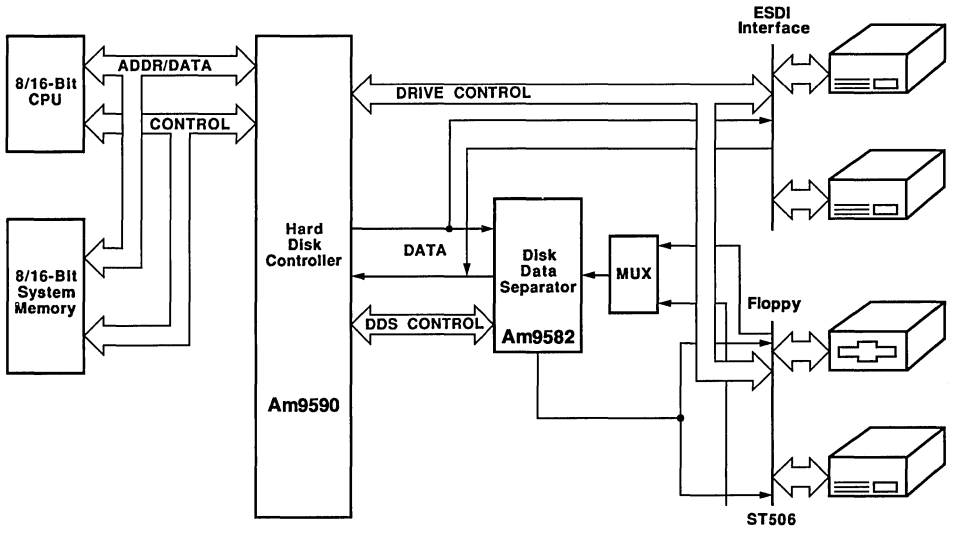


Figure 1. Disk Controller System

DMA Controller

The on-chip DMA controller enables the HDC to execute complex disk I/O operations without host CPU intervention. The DMA controller scans the command chain stored in system memory, updates the Status Result Area when errors occur, and transfers the data between the internal sector buffers and system memory. Data may be stored in non-contiguous memory, for example, to support linked-list data storage in word- processing systems.

The DMA controller generates 32-bit linear addresses to access up to 4 GBytes of system memory directly. For multiple bus-master systems, DMA transfers can be throttled to dedicate only a certain share of the system bus bandwidth to the HDC. The Mode Register (Figure 2) specifies DMA burst length and dwell time. DMA bursts can be preempted by removing Bus Acknowledge (BACK). The HDC can insert a programmable number of software Wait States into the DMA bus cycles. Additionally, hardware Wait States can be added via the $\overline{\text{READY}}$ input. The HDC updates the upper address word ($A_{16} - A_{31}$) when there is a carry-out off the lower 16 address bits.

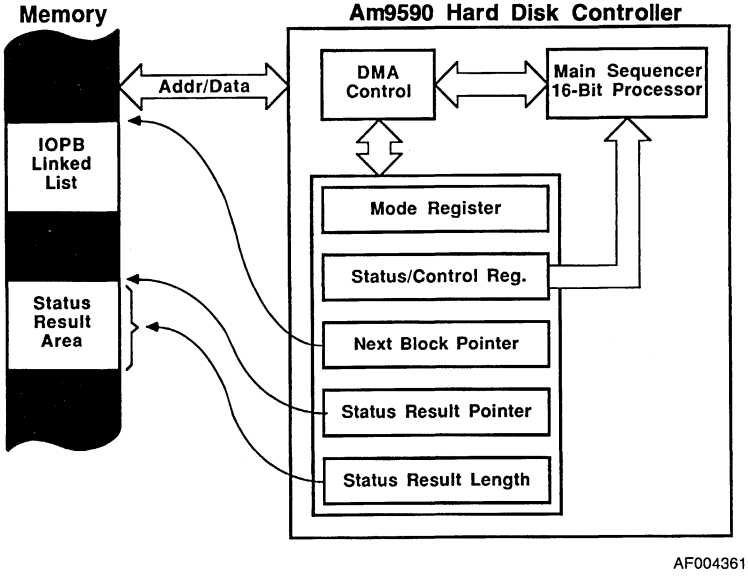


Figure 2. Software Interface

User Registers

The Mode Register defines the operation of the DMA controller. The Status/Command Register controls the basic operation of the HDC itself. The Next Block Pointer (NBP) Register links to the first Input/Output Parameter Block (IOPB) of the command chain. The Status Result Pointer Register and the Status Result Length Register define the Status Result Area where the HDC stores the status for each IOPB (See Figures 2 – 6).

$\overline{CS}$	A_3	A_2	A_1	Register Accessed
L	L	L	L	Status/Command Register
L	L	L	H	Mode Register
L	L	H	L	Next Block Pointer (low word)
L	L	H	H	Next Block Pointer (high word)
L	H	L	L	Status Result Pointer (low word)
L	H	L	H	Status Result Pointer (high word)
L	H	H	L	Status Result Length
L	H	H	H	Reserved
H	X	X	X	No Register Accessed

Figure 3. Register Addresses

MODE	B/$\overline{W}$	$\overline{BHE}$	A_0	AD<15 : 8>	AD<7 : 0>
Word Access	L	L	L	HIGH	LOW
	L	H	L	—	LOW
	L	L	H	HIGH	—
Word Access	H	X	L	—	LOW
	H	X	H	—	HIGH

Figure 4. Data Bus Assignment for Byte/Word Transfers

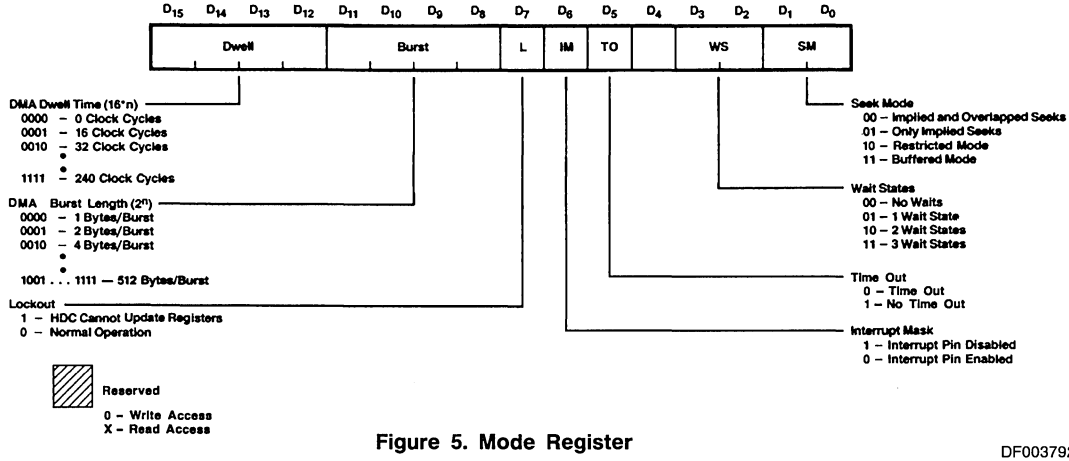
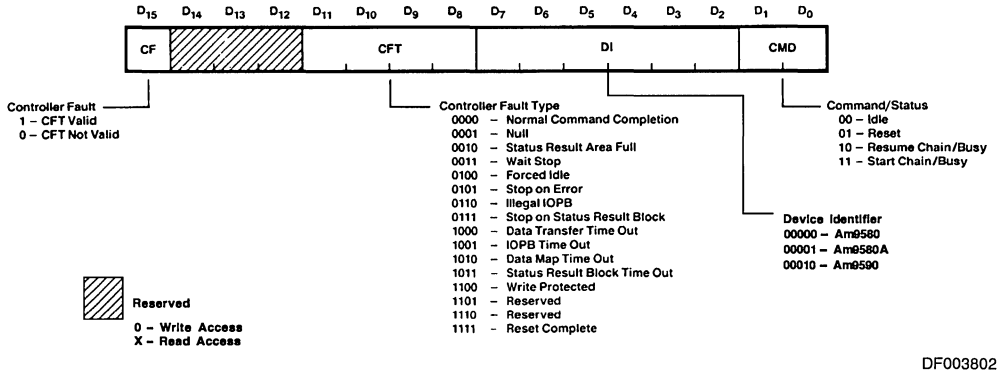


Figure 5. Mode Register

DF003792



DF003802

Figure 6. Status/Command Register

Main Sequencer

The main sequencer translates the high-level system commands into control signals for the various functional sections of the HDC. This 16- bit processor relieves the system CPU of complex data manipulations.

Drive Parameter RAMs

The Drive Parameter RAMs store the specification parameters for drives that adapt the HDC to any combination of disk recording schemes (Figures 7 – 10). The contents can be altered any time with a single IOPB. Once loaded, these parameters allow disk commands to be independent of the drive type or track format. For example, the write command is the same whether it is for a double-density floppy-disk drive or a Winchester hard-disk drive.

$BYTE_D$	$BYTE_H$	D_7 D_0
0	0	General Select Byte
1	1	Data Select Byte
2	2	Tracks/Surface <7:0>
3	3	Tracks/Surface <15:8>
4	4	HEADS/DRIVE
5	5	Sectors/Track
6	6	RWC Track <7:0>
7	7	RWC Track <15:8>
8	8	Seek Dwell <7:0>
9	9	Seek Dwell <15:8>
10	A	STEP WIDTH
11	B	HEAD SETTLE
12	C	PRE-COMPENSATION TRACK <7:0>
13	D	PRE-COMPENSATION TRACK <15:8>
14	E	Retry Policy Byte
15	F	Motor On Delay
16	10	Delay Length
17	11	Preamble 1 Length
18	12	Postamble 1 Length
19	13	Pad Length
20	14	Preamble 2 Length
21	15	ECC Length
22	16	Postamble 2 Length
23	17	GAP Length

$WORD_D$	$WORD_H$	D_{15} D_8 D_7 D_0
0	0	Data Select Byte | General Select Byte
2	2	Tracks/Surface
4	4	Sector/Track | HEADs/Drive
6	6	RWC Track
8	8	Seek Dwell
10	A	HEAD SETTLE | STEP WIDTH
12	C	PRE-COMPENSATION TRACK
14	E	Motor On Delay | Retry Policy Byte
16	10	Preamble 1 Length | Delay Length
18	12	Pad Length | Postamble 1 Length
20	14	ECC Length | Preamble 2 Length
22	16	GAP Length | Postamble 2 Length

Figure 7. Drive Parameter Block

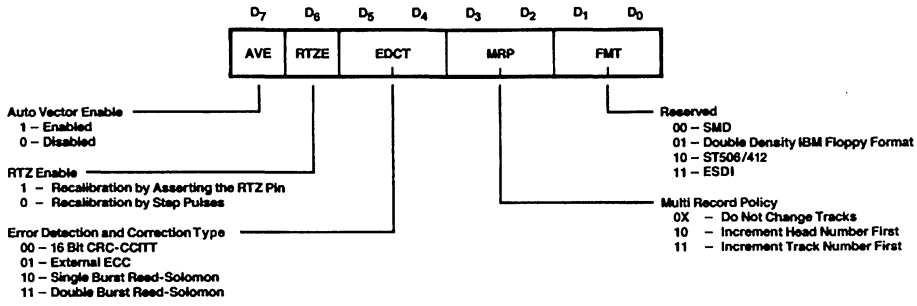


Figure 8. General Select Byte

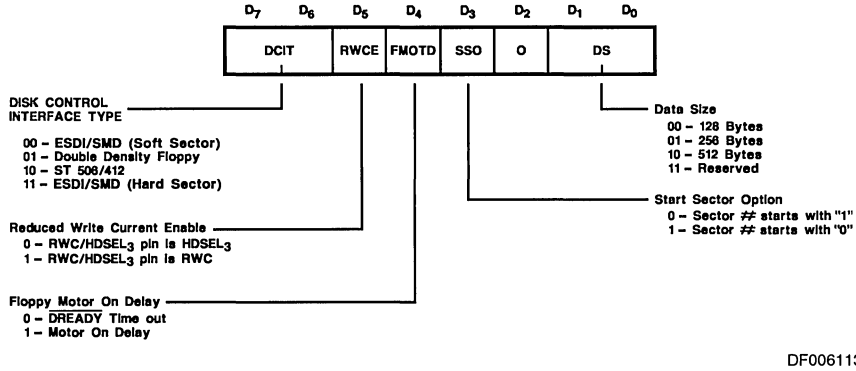


Figure 9. Data Select Byte

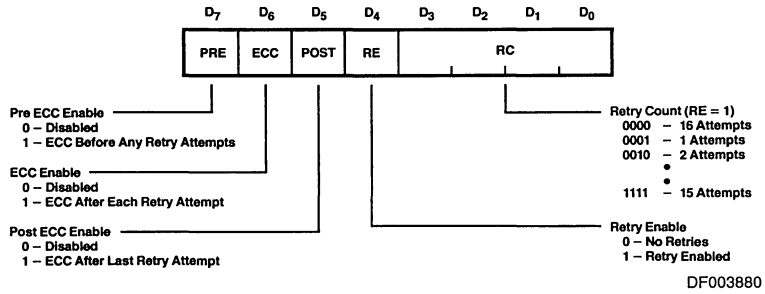


Figure 10. Retry Policy Byte

Error Checking

The HDC features two powerful Reed-Solomon error correcting codes as well as the industry standard error detection code CRC-CCITT. It also supports a user-definable, external error correction scheme. Along with programmble retry and correction attempt policy, the HDC allows maximum control of data integrity.

Sector Buffers

The HDC transfers data to or from disk without adding time constraints on the system bus bandwidth. The two internal sector buffers can be filled or emptied, at any speed, without interfering with data transfers between sector buffers and the disk. The two internal sector buffers can be toggled for zero-sector interleave disk data operations (Figure 11).

While one sector buffer is filled with data from disk, the other buffer is emptied by the DMA controller. Physically, contiguous sectors on a track can be read or written on-the-fly (during one revolution of the disk).

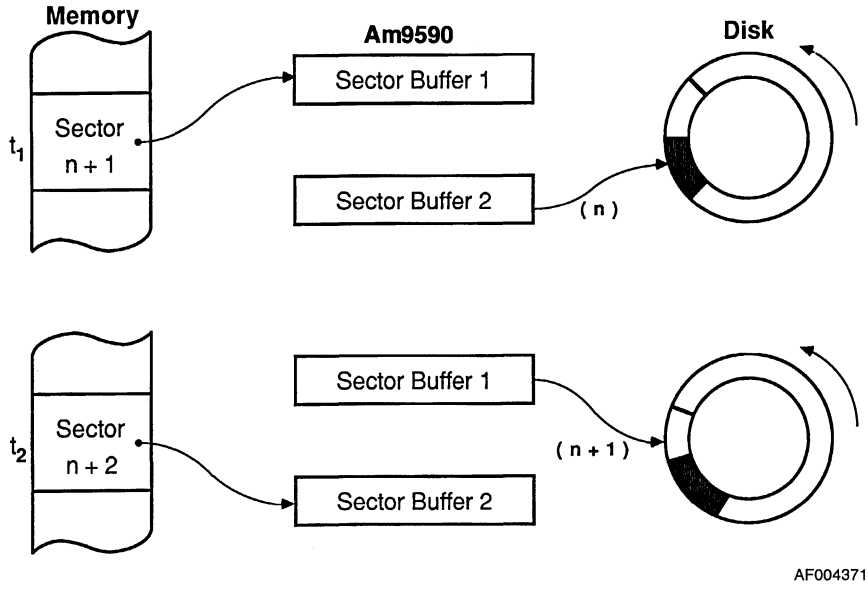


Figure 11. Dual On-Chip Sector Buffers

Disk Control Interface

The Disk Control Interface of the Am9590 can be configured for four different types of drive interfaces: ST506/412, Floppy Disk, ESDI (Serial) and SMD; each drive can be individually set up. Other drives can be connected with external logic.

By using the ST506/412 and Floppy option, the Am9590 issues step pulses to position the heads to the desired cylinder. Step width and dwell times, as well as head settling times, are programmable.

If the ESDI interface is selected, the HDC will automatically generate SEEK and RESTORE commands to the ESDI drive using the serial communication link (Figure 12).

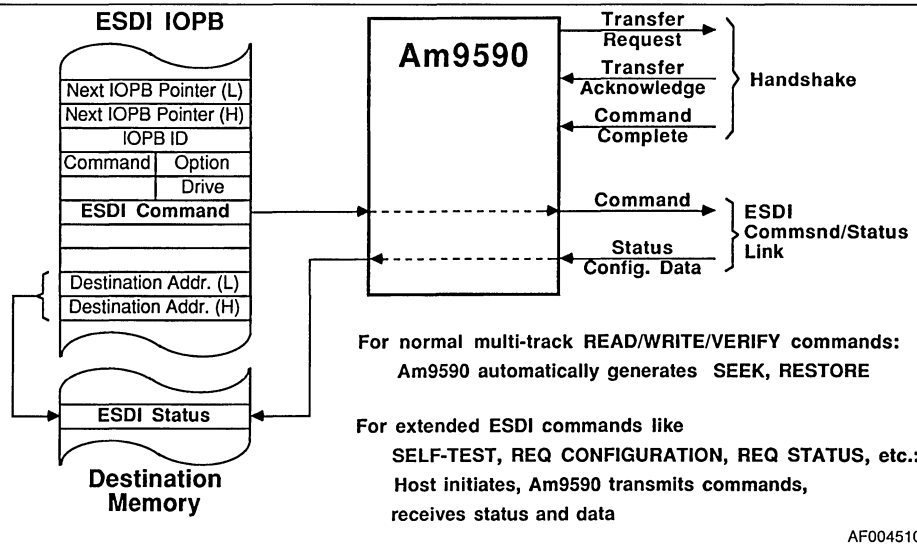


Figure 12. ESDI Serial Command/Status Communications

In SMD mode, the Am9590 provides a serialized track number (16 bits) whenever a track needs to be changed. This track number can be used by external logic to generate the appropriate disk commands.

All seek modes have two options in common, they can be either IMPLIED or OVERLAPPED seeks (Figure 13). In Implied Mode, the HDC performs only one seek operation at a time and waits for the selected disk drive to finish the operation before any data transfer is attempted. In Overlapped Mode, the Am9590 looks ahead in the IOPB command chain to search for future commands which require seek operations on different drives. It then starts seeking, up to four drives simultaneously, and performs data transfer operations on one drive while others are still seeking. This scheme reduces seek overhead substantially.

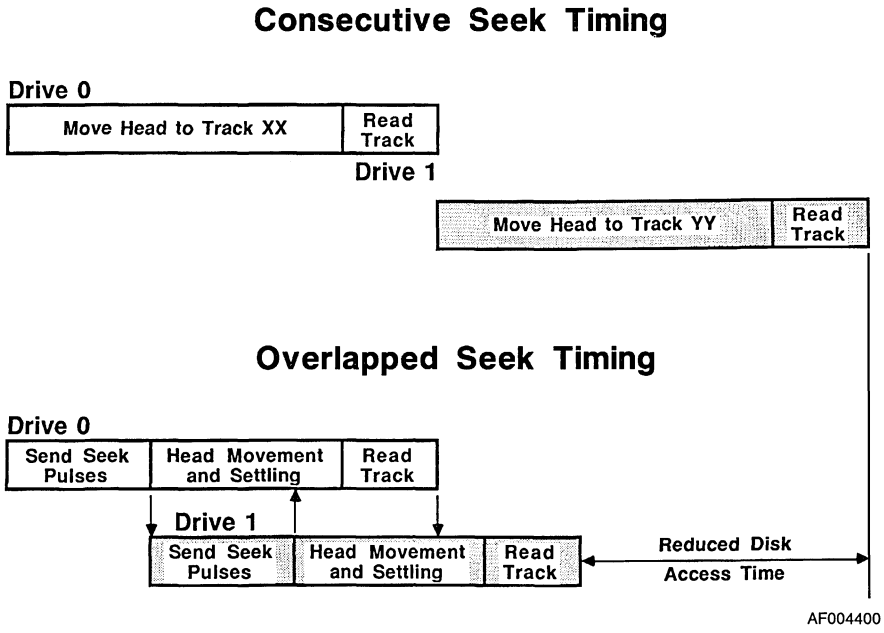


Figure 13. Consecutive and Overlapped Seek Timing

Disk Data Interface

The Am9590 can be configured for the following types of disk data formats: ESDI/SMD Soft Sector, ESDI/SMD Hard Sector, Double-Density Floppy and ST506/412 Soft Sector. Depending on the interface chosen, the HDC either provides data and handshake signals which connect directly to the disk drive (ESDI), or signals which interface to the Am9582 Data Separator (ST506/412, Double-Density Floppy).

Operating asynchronously to the other blocks of the device, the Disk Data Interface is driven by the Read/Reference Clock (RD/REF CLK). The Disk Data Interface converts the data stored in the sector buffer into a serial bit-stream for the disk, or it de-serializes the incoming bit-stream to be loaded into one of the sector buffers. Non-data information, such as the header (sector ID field), pads, gaps, preambles, and postambles, are conditioned according to the parameters stored in the Drive Parameter RAMs, to meet the defined recording standard.

IOPB Command Structure

The Am9590 HDC features a high-level data and command structure. The basic unit of this command structure is the Input/Output Parameter Block (IOPB). The host CPU creates IOPBs in system memory to pass control and status information to the HDC. The HDC fetches these IOPBs by using the on-chip DMA controller. Each IOPB specifies one disk command and contains all parameters needed for execution (Figures 14 – 16). To start the execution of an IOPB, the host CPU loads the address of the IOPB into the Next Block Pointer Register and writes the "Start Chain" command by programming the Status/Command Register. After the IOPB is executed, the HDC reports the status information and waits for further instructions. The host CPU can examine the Status/Command Register on how the commands were terminated. The CPU can also get status from the Status Result Block in memory, if an error occurs.

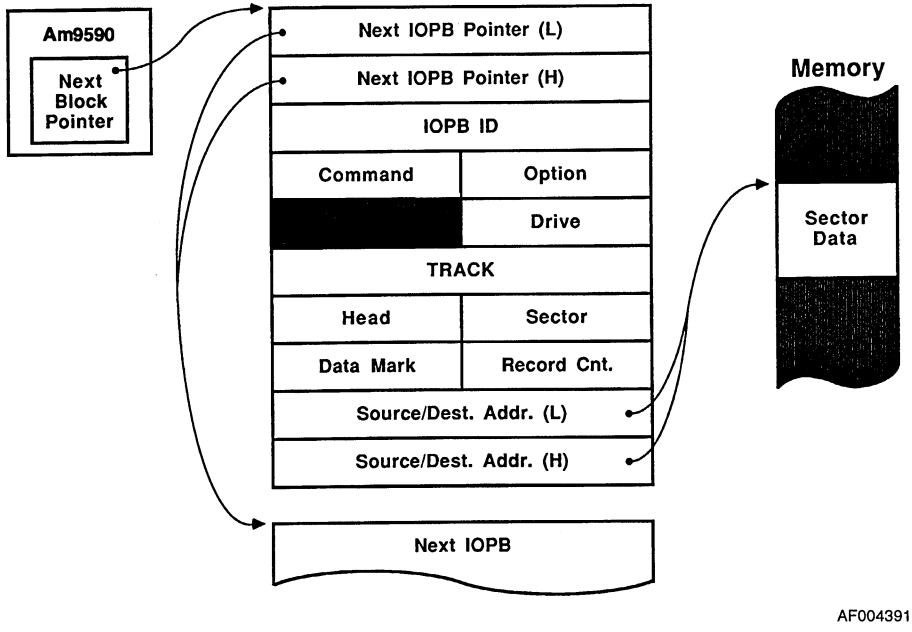


Figure 14. IOPB Address Sequence

$BYTE_D$	$BYTE_H$	
0	0	NEXT IOPB P. <7:07>
1	1	NEXT IOPB P. <15:1>
2	2	NEXT IOPB P. <23:16>
3	3	NEXT IOPB P. <31:24>
4	4	ID <7:0>
5	5	ID <15:8>
6	6	OPTIONS
7	7	COMMAND CODE (1)
8	8	BYTE 8
9	9	BYTE 9
10	A	BYTE 10
11	B	BYTE 11
12	C	BYTE 12
13	D	BYTE 13
14	E	BYTE 14
15	F	BYTE 15
16	10	BYTE 16
1	11	BYTE 17
18	12	BYTE 18
19	13	BYTE 19

$WORD_D$	$WORD_H$	D_{15}	D_0
0	0	NEXT IOPB POINTER <15:0>	
2	2	NEXT IOPB POINTER <31:16>	
4	4	ID	
6	6	COMMAND CODE(1)	OPTIONS
8	8	BYTE 9	BYTE 8
10	A	BYTE 11	BYTE 10
12	C	BYTE 13	BYTE 12
14	E	BYTE 15	BYTE 14
16	10	BYTE 17	BYTE 16
18	12	BYTE 19	BYTE 18

(1) see IOPB Parameter Table

Figure 15. IOPB Structure

Command	Code	Options 7	6	5	4	3	2	1	0	Byte 9	Byte 8	Byte 11	Byte 10	Byte 13	Byte 12	Byte 15	Byte 14	Byte 17	Byte 16	Byte 19	Byte 18
Read	0C	W	SE	SSRB	0	DME	DM	0	0	00	Drive	Track		Head	Sector	Data Mark	Record Count	Destination <15 : 0>		Destination <31 : 16>	
Write	0D	W	SE	SSRB	0	DME	DM	0	0	00	Drive	Track		Head	Sector	Data Mark	Record Count	Source <15 : 0>		Destination <31 : 16>	
Verify	0F	W	SE	SSRB	0	DME	DM	0	0	00	Drive	Track		Head	Sector	Data Mark	Record Count	Source <15 : 0>		Destination <31 : 16>	
Format	07	W	SE	SSRB	0	0	0	0	0	00	Drive	Track		Head	Pattern	Track Count		Map Pointer <15 : 0>		Map Pointer <31 : 16>	
Relocate Track	0B	W	SE	SSRB	0	0	0	0	0	00	Drive	Track		Head	00	Alternate Track		Alternate Head	00	0000	
Load Drive Parameter Block	00	W	SE	SSRB	0	0	0	0	0	00	Drive	0000		00	00	00	00	Source <15 : 0>		Source <31 : 16>	
Dump Drive Parameter Block	03	W	SE	SSRB	0	0	0	0	0	00	Drive	0000		00	00	00	00	Destination <15 : 0>		Destination <31 : 16>	
Read Physical Sector	0A	W	SE	SSRB	0	TV	DM	0	0	00	Drive	Track		Head	Physical Sector	00	00	Destination <15 : 0>		Destination <31 : 16>	
Read ID	09	W	SE	SSRB	0	AS	0	0	0	00	Drive	Track		Head	Physical Sector	00	00	Destination <15 : 0>		Destination <31 : 16>	
Load Buffer	01	W	SE	SSRB	0	DME	0	0	TB	00	Drive	0000		00	00	00	00	Source <15 : 0>		Source <31 : 16>	
Dump Buffer	02	W	SE	SSRB	0	DME	0	0	TB	00	Drive	0000		00	00	00	00	Destination <15 : 0>		Destination <31 : 16>	
Load Syndrome	04	W	SE	SSRB	0	0	0	0	0	00	Drive	0000		00	00	00	00	Source <15 : 0>		Source <31 : 16>	
Dump Syndrome	05	W	SE	SSRB	0	0	0	0	0	00	Drive	0000		00	00	00	00	Destination <15 : 0>		Destination <31 : 16>	
Correct Buffer	06	W	SE	SSRB	0	LD	0	0	0	00	Drive	0000		00	00	00	00	Destination <15 : 0>		Destination <31 : 16>	
Seek	0E	W	SE	SSRB	0	TV	0	0	0	00	Drive	Track		Head	00	00	00	0000		0000	
Restore	08	W	SE	SSRB	0	TV	0	0	0	00	Drive	0000		00	00	00	00	0000		0000	
ESDI Channel	10	W	SE	SSRB	0	0	0	0	SR	WCC	Drive	0000		00	00	00	00	Destination <15:0>		Destination <31:16>	

Figure 16. IOPB Parameters

The Am9590 supports five different types of commands: Normal Disk I/O Commands, Initialization Commands, Marginal Data Recovery Commands, Head Movement Commands, and ESDI Command

Normal Disk I/O Commands:
- READ multiple sectors
- WRITE multiple sectors
- VERIFY multiple sectors

Initialization Commands:
- FORMAT TRACK(s)
- RELOCATE TRACK
- LOAD DRIVE PARAMETER BLOCK
- DUMP DRIVE PARAMETER BLOCK

Marginal Data Recovery Commands:
- READ PHYSICAL SECTOR (Read data field only)
- READ ID (Read header only)
- LOAD BUFFER (Load internal sector buffer)
- DUMP BUFFER (Dump internal sector buffer)
- LOAD ECC SYNDROMES
- DUMP ECC SYNDROMES
- CORRECT BUFFER (Correct internal sector buffer)

Head Movement Commands:
- SEEK
- RESTORE

ESDI Command:
- ESDI CHANNEL (Send user-definable command to ESDI drive).

As an option, IOPBs may be chained together in a linked-list format which the HDC can interpret sequentially. With this structure, a complex list of disk commands can be set up and then executed by the HDC without CPU intervention. The CPU is then totally free from any disk controlling. For example, the host CPU might set up a list of commands for the HDC to copy an entire floppy-disk to a hard-disk and verifies that the data has been copied correctly. Upon verification, the HDC reformats the floppy-disk, all without host CPU intervention. This is shown in Figure 17.

An IOPB command chain is basically a queue of jobs waiting for HDC execution. This offers a pre-defined and efficient structure for the operating system to handle its disk I/O. The ID field of the IOPB provides the linkage between a particular disk command and the user's program that generated the disk request. Jobs can be placed in the HDC job queue and be ignored by the operating system, unless an error occurs. All the information required to retrace an error is provided by the HDC Status Result Block.

Data Mapping

Sector data to be transferred to or from the disk may be stored in non-contiguous system memory using the data mapping option (Figures 17 & 18). Definable portions of a disk file can be written to, or read from, separate areas of memory on a byte-by-byte basis. Word processing systems can employ this feature to save text, arranged in a linked-list directly on disk, and eliminates the time-consuming task of converting the linked-list into a linear list. The Data Map defines the linked-list data structure. The Data Map option is processed by the HDC, while the disk is in operation, so that data maps can be handled without affecting data transfer rate.

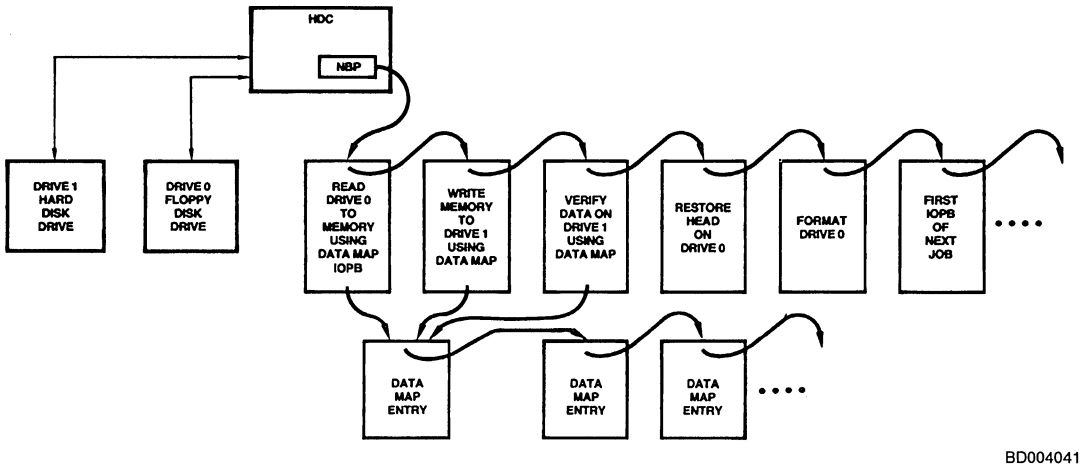


Figure 17. Command Chaining Example

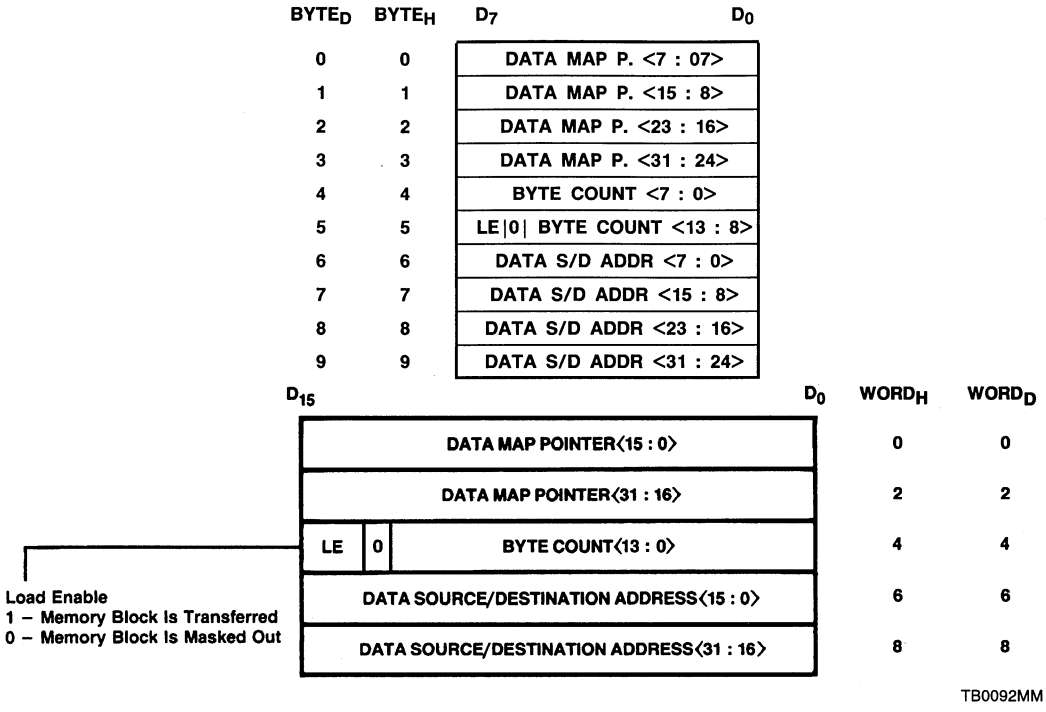


Figure 18. Data Map Entry

Status Result Blocks

When the HDC finds that an IOPB has caused an error, it writes to the Status Result Block (SRB) (Figure 19). Errors may be caused by invalid command codes, disk read and write errors, seek errors, or memory time-outs. Since the SRB contains the ID number for the IOPB which caused the error, the operating system can determine which disk I/O job caused the error and reports this to the user. Depending upon the type of error, and what policy has been selected, the HDC may continue with the IOPB chain automatically, or waits for the host processor to tell it whether to start over or continue. The SRBs contain all the specific information required to find the exact location of the error and to make recovery as complete as possible.

BYTE	D_7	D_0
0	BYTE 0	
1	BYTE 1	
2	BYTE 2	
3	BYTE 3	
4	BYTE 4	
5	BYTE 5	
6	BYTE 6	
7	BYTE 7	
8	BYTE 8	
9	BYTE 9	

WORD	D_{15}	D_0
0	Byte 1	Byte 0
2	Byte 3	Byte 2
4	Byte 5	Byte 4
6	Byte 7	Byte 6
8	Byte 9	Byte 8

Figure 19. Layout of Status Result Blocks

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) .....+4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

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