Am29117

A High-Performance 16-Bit Bipolar Microprocessor

DISTINCTIVE CHARACTERISTICS

- **Optimized for High-Performance Controllers**
  Architecture and instruction set optimized for high-performance, intelligent controllers
- **Flow-Through Architecture**
  Separate input and output ports avoid bus turn-around for higher throughput

- **Fast**
  Supports 100 ns microcycle time/10 MHz data rate for all instructions
- **16-Bit Barrel Shifter**
- **32 Working Registers**
- **68-Pin Pin Grid Array Package**

GENERAL DESCRIPTION

The Am29117 is a microprogrammable 16-bit bipolar microprocessor whose architecture and instruction set are identical to the Am29116's except for the I/O bus structure. Since the device has separate input and output ports, designers can avoid quick bus turnaround requirements.

The architecture and instruction set are not only optimized for high-performance peripheral controllers, but also suitable for microprogrammed processor applications when combined with the Am29517A 16 x 16 Multiplier.

The instruction set contains unique functions besides ordinary logic and arithmetic functions: bit manipulation instructions (set, reset and test), rotate merge/compare instructions, prioritize instruction and CRC instruction.

BLOCK DIAGRAM
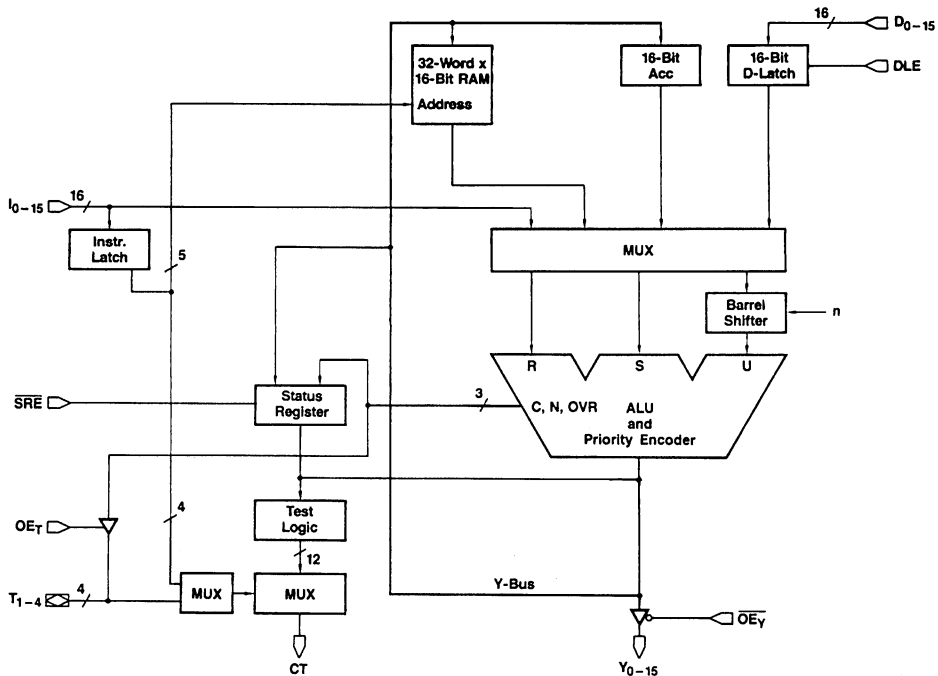
BD001972

RELATED AMD PRODUCTS

Part No.	Description
Am29112	High-Performance 8-Bit Slice Microprogram Sequencer
Am29114	Eight-Level Real-Time Interrupt Controller
Am29116	High-Performance Single-Port Bipolar Microprocessor
Am29116A	Speed-Enhanced Version of the Am29116 (Supports up to 76-ns Microcycle Times)
Am29L116A	Low-Power Version of the Am29116 (25% Lower Power Dissipation)
Am29C117	CMOS Version of the Am29117
Am29118	8-Bit Am29116 I/O Support
Am29130	16-Bit Barrel Shifter
Am29PL141	Fuse-Programmable Controller
Am29516/Am29517 Family	16 x 16-Bit Parallel Multipliers (High-Speed Bipolar, Low-Power Bipolar, and CMOS Versions)

The following diagram is a summary of devices within the Am29116 Family showing performance versus power:
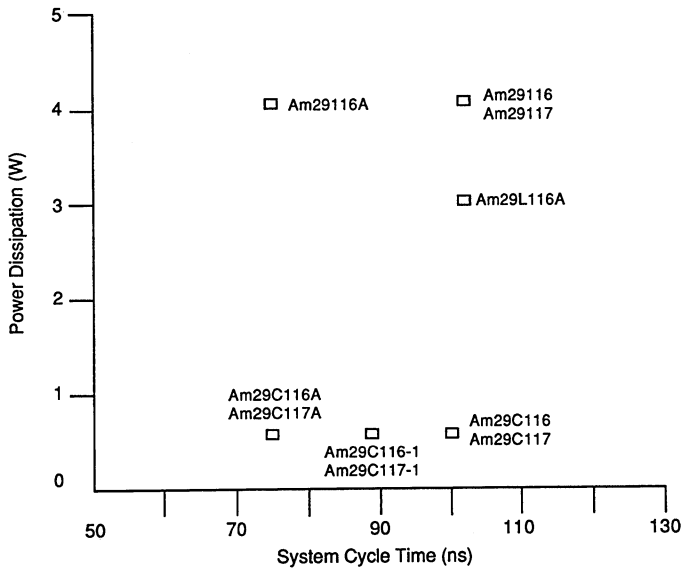

**Am29116 Family
(Performance vs. Power)**

OP002300

CONNECTION DIAGRAM
PIN GRID ARRAY
Bottom View

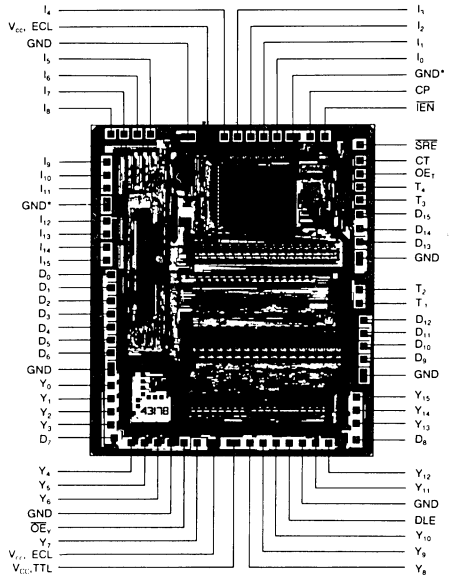|	A	B	C	D	E	F	G	H	J	K	L
1		Y1	GND	D5	D3	D1	D0	I14	I12	I10	
2	Y3	Y2	Y0	D6	D4	D2	I15	I13	I11	I9	I8
3	Y4	D7								I7	I6
4	Y6	Y5								I5	GND
5	OEY	GND								I4	VCCE
6	VCCE	Y7								I3	I2
7	VCCT	Y8								I0	I1
8	Y9	Y10								IEN	CP
9	DLE	GND								CT	SRE
10	Y11	Y12	Y13	Y15	D9	D12	T2	D13	D15	T4	OET
11		D8	Y14	GND	D10	D11	T1	GND	D14	T3	

CD010610

Note: Notch indicates orientation.

LOGIC SYMBOL
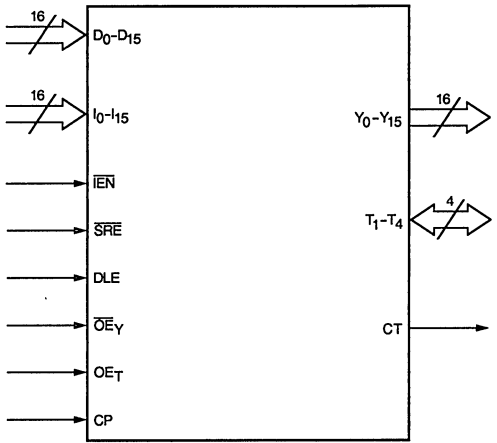
LS002610

METALLIZATION AND PAD LAYOUT

Die Size: 0.285″ x 0.334″
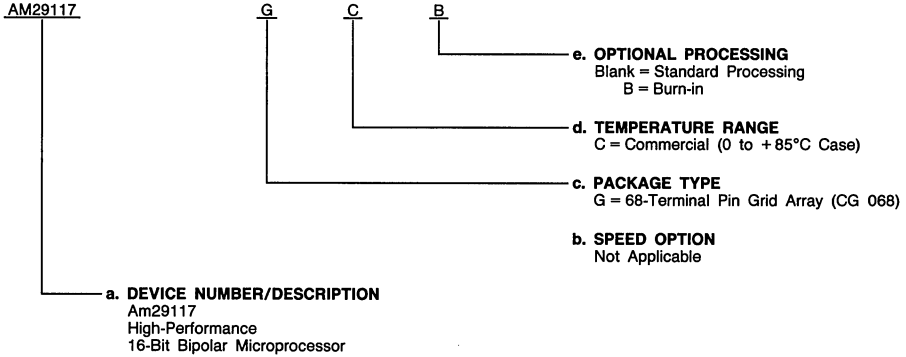Gate Count: 2500 Equivalent Gates

*These GND pads are internally connected inside the package, therefore they do not have external pin numbers.

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
- **a. Device Number**
- **b. Speed Option** (if applicable)
- **c. Package Type**
- **d. Temperature Range**
- **e. Optional Processing**

AM29117   G   C   B

e. OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +85°C Case)

c. PACKAGE TYPE
G = 68-Terminal Pin Grid Array (CG 068)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29117
High-Performance
16-Bit Bipolar Microprocessor

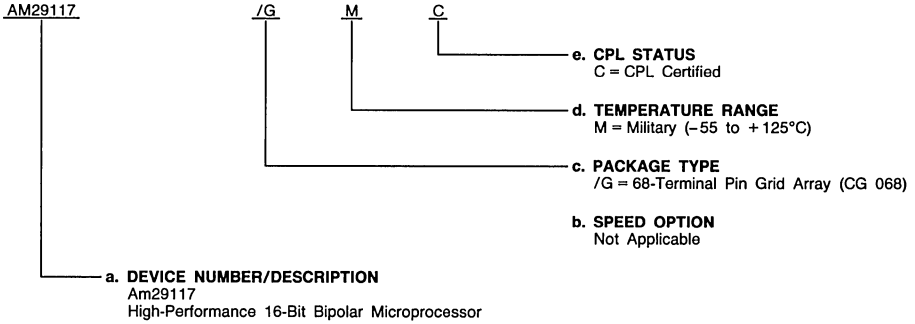| Valid Combinations	
AM29117	GC, GCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)
CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

    a. Device Number
    b. Speed Option (if applicable)
    c. Device Class
    d. Package Type
    e. Lead Finish

AM29117   /G   M   C

e. CPL STATUS
C = CPL Certified

d. TEMPERATURE RANGE
M = Military (–55 to +125°C)

c. PACKAGE TYPE
/G = 68-Terminal Pin Grid Array (CG 068)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29117
High-Performance 16-Bit Bipolar Microprocessor

Valid Combinations

Valid Combinations	
AM29117	/GMC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests
Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

CP   Clock Pulse (Input)

The clock input to the Am29117. The RAM latch is transparent when the clock is HIGH. When the clock goes LOW, the RAM output is latched. Data is written into the RAM during the LOW period of the clock, provided $\overline{IEN}$ is LOW, and if the instruction being executed designates the RAM as the destination of operation. The Accumulator and Status Register will accept data on the LOW-to-HIGH transition of the clock if $\overline{IEN}$ is also LOW. The instruction latch becomes transparent when it exits an immediate instruction mode during a LOW-to-HIGH transition of the clock.

CT   Conditional Test (Output)

The condition code multiplexer selects one of the twelve condition code signals and places it on the CT output. A HIGH on the CT output indicates a passed condition and a LOW indicates a failed condition.

$D_0 - D_{15}$ Data Input Lines (Input)

Data Input Lines, $D_0 - D_{15}$, are used as external data inputs which allow data to be directly loaded into the 16-bit data latch.

DLE   Data Latch Enable (Input)

When DLE is HIGH, the 16-bit data latch is transparent and is latched when DLE is LOW.

$I_0 - I_{15}$ Instruction Inputs (Input)

Sixteen Instruction Inputs, used to select the operation to be performed in the Am29117. Also used as data inputs while performing immediate instructions.

$\overline{IEN}$ Instruction Enable (Input)

When $\overline{IEN}$ is LOW, data can be written into RAM when the clock is LOW. The Accumulator can accept data during the LOW-to-HIGH transition of the clock. Having $\overline{IEN}$ LOW, the Status Register can be updated when $\overline{SRE}$ is LOW. When $\overline{IEN}$ is HIGH, the conditional test output, CT, is disabled as a function of the instruction inputs.

OE_T Output Enable (Output)

When OE_T is LOW, 4-bit T outputs are disabled (high impedance); when OE_T is HIGH, the 4-bit T outputs are enabled (HIGH or LOW).

$\overline{OE}_Y$ Output Enable (Input)

When $\overline{OE}_Y$ is HIGH, the 16-bit Y outputs are disabled (high impedance); when $\overline{OE}_Y$ is LOW, the 16-bit Y outputs are enabled (HIGH or LOW).

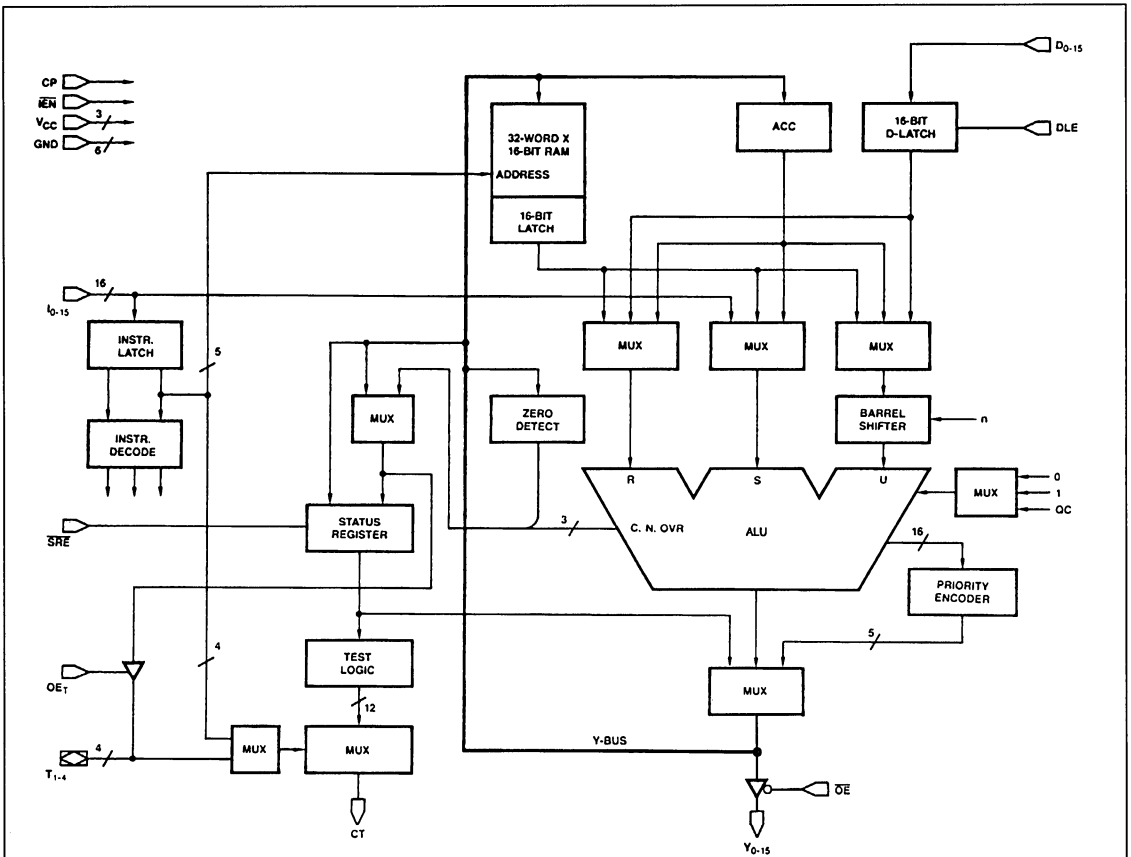**$\overline{SRE}$ Status Register Enable (Input)**

When $\overline{SRE}$ and $\overline{IEN}$ are both LOW, the Status Register is updated at the end of all instructions with the exception of NO-OP, Save Status and Test Status. Having either $\overline{SRE}$ or $\overline{IEN}$ HIGH will inhibit the Status Register from changing.

$T_1 - T_4$ Test I/O Pins (Input/Output)

Under the control of OE_T, the four lower status bits, Z, C, N and OVR, become outputs on $T_1 - T_4$, respectively, when OE_T goes HIGH. When OE_T is LOW, $T_1 - T_4$ are used as inputs to generate the CT output.

$Y_0 - Y_{15}$ Data Output Lines (Output)

Data Output lines. When $\overline{OE}_Y$ is HIGH, the 16-bit Y outputs are disabled (high impedance); having $\overline{OE}_Y$ LOW allows the ALU data to be output on $Y_0 - Y_{15}$.

Figure 1. Detailed Block Diagram

BD001965

FUNCTIONAL DESCRIPTION

Architecture of the Am29117

The Am29117 is a high-performance, microprogrammable 16-bit bipolar microprocessor.

As shown in the Detailed Block Diagram (Figure 1), the device consists of the following elements interconnected with 16-bit data paths.

- 32-Word by 16-Bit RAM
- Accumulator
- Data Latch
- Barrel Shifter
- Arithmetic Logic Unit (ALU)
- Priority Encoder
- Status Register
- Condition-Code Generator/Multiplexer
- Three-State Output Buffers
- Instruction Latch and Decoder

32-Word by 16-Bit RAM

The 32-word by 16-bit RAM is a single-port RAM with a 16-bit latch at its output. The latches are transparent when the clock input (CP) is HIGH and latched when the clock input is LOW. Data is written into the RAM while the clock is LOW if the $\overline{IEN}$ input is also LOW and if the instruction being executed defines the RAM as the destination of the operation. For byte instructions, only the lower eight RAM bits are written into; for word instructions, all 16 bits are written into. With the use of an external multiplexer on five of the instruction inputs, it is possible to select separate read and write addresses for the same instruction.

Accumulator

The 16-bit Accumulator is an edge-triggered register. The Accumulator accepts data on the LOW-to-HIGH transition of the clock input if the $\overline{IEN}$ input is LOW and if the instruction being executed defines the Accumulator as the destination of the operation. For byte instructions, only the lower eight bits of the Accumulator are written into; for word instructions, all 16 bits are written into.

Data Latch

The 16-bit Data Latch holds the data input to the Am29117 on the D bus. The latch is transparent when the DLE input is HIGH and latched when the DLE input is LOW.

Barrel Shifter

A 16-bit Barrel Shifter is used as one of the ALU inputs. This permits rotating data from either the RAM, the Accumulator or the Data Latch up to 15 positions. In the word mode, the Barrel Shifter rotates a 16-bit word; in the byte mode, it rotates only the lower eight bits.

Arithmetic Logic Unit

The Am29117 contains a 16-bit ALU with full carry lookahead across all 16 bits in the arithmetic mode. The ALU is capable of operating on either one, two or three operands, depending upon the instruction being executed. It has the ability to execute all conventional one and two operand operations, such as pass, complement, two's complement, add, subtract, AND, NAND, OR, NOR, EXOR, and EX-NOR. In addition, the ALU can also execute three-operand instructions such as rotate and merge, and rotate and compare with mask. All ALU operations can be performed on either a word or byte basis, with byte operations being performed on the lower eight bits only.

The ALU produces three status outputs, C (carry), N (negative) and OVR (overflow). The appropriate flags are generated at the byte or word level, depending upon whether the device is executing in the byte or word mode. The Z (zero) flag, although not generated by the ALU, detects zero at both the byte and word level.

The carry input to the ALU is generated by the Carry Multiplexer which can select an input of zero, one, or the stored carry bit from the Status Register, QC. Using QC as the carry input allows execution of multiprecision addition and subtractions.

Priority Encoder

The Priority Encoder produces a binary-weighted code to indicate the locations of the highest order ONE at its input. The input to the Priority Encoder is generated by the ALU which performs an AND operation on the operand to be prioritized and a mask. The mask determines which bit locations to eliminate from prioritization. In the word mode, if no bit is HIGH, the output is a binary zero. If bit 15 is HIGH, the output is a binary one. Bit 14 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 16 is produced.

In the byte mode, bits 8 through 15 do not participate. If none of bits 7 through 0 are HIGH, the output is a binary zero. If bit 7 is HIGH a binary one is produced. Bit 6 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 8 is produced.

Status Register

The Status Register holds the 8-bit status word. With the Status-Register Enable ($\overline{SRE}$) input LOW and the $\overline{IEN}$ input LOW, the Status Register is updated at the end of all instructions except NO-OP, Save-Status and Test-Status instructions. $\overline{SRE}$ going HIGH or $\overline{IEN}$ going HIGH inhibits the Status Register from changing.

The lower four bits of the Status Register contain the ALU status bits of Zero (Z), Carry (C), Negative (N), and Overflow (OVR). The upper four bits contain a Link bit and three user-definable status bits (Flag 1, Flag 2, Flag 3).

With $\overline{SRE}$ LOW and $\overline{IEN}$ LOW, the lower four status bits are updated after each instruction except those mentioned above, NO-OP, Save Status, Status Test and the Status Set/Reset instruction for the upper four bits. Under the same conditions, the upper four status bits are changed only during their respective Status Set/Reset instructions and during Status Load instructions in the word mode. The Link-Status bit is also updated after each shift instruction.

The Status Register can be loaded from the internal Y-bus, and can also be selected as a source for the internal Y-bus. When the Status Register is loaded in the word mode, all 8-bits are updated; in the byte mode, only the lower 4 bits (Z, C, N, OVR) are updated.

When the Status Register is selected as a source in the word mode, all eight bits are loaded into the lower byte of the destination; the upper byte of the destination is loaded with all zeros. In the byte mode, the Status Register again loads into the lower byte of the destination, but the upper byte remains unchanged. This Store and Load combination allows saving and restoring the Status Register for interrupt and subroutine processing. The four lower status bits (Z, C, N, OVR) can be read directly via the bidirectional T bus. These four bits are available as outputs on the T_{1-4} outputs whenever OE_T is HIGH.

Condition-Code Generator/Multiplexer

The Condition-Code Generator/Multiplexer contains the logic necessary to develop the 12 condition-code test signals. The multiplexer portion can select one of these test signals and place it on the CT output for use by the microprogram sequence. The multiplexer may be addressed in two different

ways. One way is through the Test Instruction. This instruction specifies the test condition to be placed in the CT output, but does not allow an ALU operation at the same time. The second method uses the bidirectional T bus as an input. This requires extra bits in the microword, but provides the ability to simultaneously test and execute. The test instruction lines, I_{0-4}, have priority over T_{1-4}, for testing status.

Three-State Output Buffers

There are two sets of Three-State Output Buffers in the Am29117. One set controls the 16-bit Y bus. These outputs are enabled by placing a LOW on the $\overline{OE}_Y$ input. A HIGH puts the Y outputs in the high-impedance state.

The second set of Three-State Output Buffers controls the bidirectional 4-bit T bus and is enabled by placing a HIGH on the OE_T input. This allows storing the four internal ALU status bits (Z, C, N, OVR) externally. A LOW OE_T input forces the T outputs into the high-impedance state. External devices can then drive the T bus to select a test condition for the CT output.

Instruction Latch and Decoder

The 16-bit Instruction Latch is normally transparent to allow decoding of the Instruction Inputs by the Instruction Decoder into the internal control signals for the Am29117. All instructions except Immediate Instructions are executed in a single clock cycle.

Immediate instructions require two clock cycles for execution. During the first clock cycle, the Instruction Decoder recognizes that an Immediate Instruction is being specified and captures the data on the Instruction Inputs in the Instruction Latch. During the second clock cycle, the data on the Instruction Inputs is used as one of the operands for the function specified during the first clock cycle. At the end of the second clock cycle, the Instruction Latch is returned to its transparent state.

Instruction Set

The instruction set of the Am29117 is very powerful. In addition to the single and two operand logical and arithmetic instructions, the Am29117 instruction set contains functions particularly useful in controller applications: bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundancy-check (CRC) generation.

Three data types are supported by the Am29117.

- Bit
- Byte
- Word (16-bit)

In the byte mode data is written into the lower half of the word and the upper half is unchanged. The special case is when the status register is specified as the destination. In the byte mode the LSH (OVR, N, C, Z) of the status register is updated and in the word mode all eight bits of the status register are updated. The status register does not change for save status and test status instructions. In the test status instructions the CT output has the result and the Y-bus is undefined.

The Am29117 Instruction Set can be divided into eleven types of instructions. These are:

- Single Operand
- Two Operand
- Single Bit Shift
- Rotate and Merge
- Bit Oriented
- Rotate by n Bits
- Rotate and Compare
- Prioritize
- Cyclic-Redundancy-Check
- Status
- No-Op

Each instruction type is arbitrarily divided into quadrants. Two of the sixteen instruction lines decode to four quadrants labelled from 0 to 3. The quadrants were defined mainly for convenience in classification of the instruction set and addressing modes and can be used together with the OP CODES to distinguish the instructions.

The following pages describe each of the instruction types in detail. Table 1 illustrates Operand Source-Destination Combinations for each instruction type.

TABLE 1. OPERAND SOURCE-DESTINATION COMBINATIONS

Single Operand

Source (R/S)	Destination
RAM (Note 2)	RAM
ACC	ACC
D	Y Bus
D(0E)	Status
D(SE)	ACC and Status
I	
0	

Two Operand

Source (R)	Source (S)	Destination
RAM	ACC	RAM
RAM	I	ACC
D	RAM	Y Bus
D	ACC	Status
ACC	I	ACC and Status
D	I	

Single Bit Shift

Source (U)	Destination
RAM	RAM
ACC	ACC
ACC	Y Bus
D	RAM
D	ACC
D	Y Bus

Rotate n Bits

Source (U)	Destination
RAM	RAM
ACC	ACC
D	Y Bus

Bit Oriented

Source (R/S)	Destination
RAM	RAM
ACC	ACC
D	Y Bus

Rotate and Merge

Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
D	I	ACC
D	RAM	ACC
D	I	RAM
D	ACC	RAM
ACC	I	RAM
RAM	I	ACC

Rotate and Compare

Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
D	I	
D	I	RAM
D	ACC	RAM
RAM	I	ACC

Prioritize (Note 3)

Source (R)	Mask (S)	Destination
RAM	RAM	RAM
ACC	ACC	ACC
D	I	Y Bus
	0	

Cyclic Redundancy Check

Data In	Destination	Polynomial
QLINK	RAM	ACC

No Operation

–

Set Reset Status

Bits Affected
OVR, N, C, Z
LINK
Flag1
Flag2
Flag3

Store Status

Source	Destination
Status	RAM
	ACC
	Y Bus

Status Load

Source (R)	Source (S)	Destination
D	ACC	Status
ACC	I	Status and ACC
D	I	

Test Status

Test Condition (CT)
$(N \oplus OVR) + Z$
$N \oplus OVR$
Z
OVR
Low
C
$Z + \overline{C}$
N
LINK
Flag 1
Flag 2
Flag 3

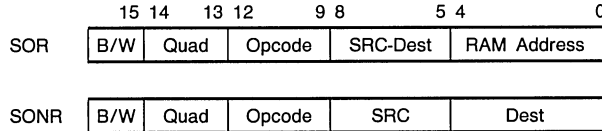Notes: 1. When there is no dividing line between the R&S OPERAND or SOURCE and DESTINATION, the two must be used as a given pair. But where there exists such a separation, any combination of them is possible.
2. In the SINGLE OPERAND INSTRUCTION, RAM cannot be used when both ACC and STATUS are designated as a DESTINATION.
3. In the PRIORITIZE INSTRUCTION, OPERAND and MASK must be different sources.

Single Operand Instructions

The Single Operand Instructions contain four indicators: byte or word mode, opcode, source and destination. They are further subdivided into two types. The first type uses RAM as a source or destination or both, and the second type does not use RAM as a source or destination. Both types have different instruction formats as shown below. Under the control of instruction inputs, the desired function is performed on the source and the result is either stored in the specified destination or placed on the Y-bus or both. For a special case where

8-bit to 16-bit conversion is needed, the Am29117 is capable of extending sign bit (D(SE)) or binary zero (D(0E)) over 16-bits in the word mode. The least significant four bits of the Status Register (OVR, N, C, Z) are affected by the function performed in this category. The most significant bits of status register (FLAG1, FLAG2, FLAG3, LINK) are not affected. The only limitation in this type is that the RAM cannot be used as a source when both ACC and the Status Register are specified as a destination.

SINGLE OPERAND FIELD DEFINITIONS

	15 14	13 12	9 8	5 4	0
SOR	B/W	Quad	Opcode	SRC-Dest	RAM Address

	15 14	13 12	9 8	5 4	0
SONR	B/W	Quad	Opcode	SRC	Dest

SINGLE OPERAND INSTRUCTION

Instruction[1]	B/W[2]	Quad[3]	Opcode			R/S[4] Dest[4]			RAM Address		
SOR	0 = B 1 = W	10	1100 1101 1110 1111	MOVE COMP INC NEG	SRC→Dest $\overline{SRC}$→Dest SRC + 1→Dest $\overline{SRC}$ + 1→Dest	0000 0010 0011 0100 0110 0111 1000 1001 1010 1011	SORA SORY SORS SOAR SODR SOIR SOZR SOZER SOSER SORR	RAM ACC RAM Y Bus RAM Status ACC RAM D RAM I RAM 0 RAM D(0E) RAM D(SE) RAM RAM RAM	00000 11111	R00 ·· R31	RAM Reg 00 ···· RAM Reg 31

Instruction	B/W	Quad	Opcode			R/S[4]		Destination		
SONR	0 = B 1 = W	11	1100 1101 1110 1111	MOVE COMP INC NEG	SRC→Dest $\overline{SRC}$→Dest SRC + 1→Dest $\overline{SRC}$ + 1→Dest	0100 0110 0111 1000 1001 1010	SOA ACC SOD D SOI I SOZ 0 SOZE D(0E) SOSE D(SE)	00000 00001 00100 00101	NRY NRA NRS NRAS	Y Bus ACC Status[5] ACC, Status[5]

Notes: 1. The instruction mnemonic designates different instruction formats used in the Am29117. They are useful in microcode assembly.
2. B = Byte Mode, W = Word Mode.
3. See Instruction Set description.
4. R = Source; S = Source; Dest = Destination.
5. When status is destination,
 Status i ← Yi i = 0 to 3 (Byte mode)
 i = 0 to 7 (Word mode)

Y BUS AND STATUS – SINGLE OPERAND INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y — Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SOR SONR	MOVE	SRC→Dest	0 = B	Y ← SRC	NC	NC	NC	NC	0	U	0	U
	COMP	$\overline{SRC}$ →Dest	1 = W	Y ← $\overline{SRC}$	NC	NC	NC	NC	0	U	0	U
	INC	SRC +1 → Dest		Y ← SRC +1	NC	NC	NC	NC	U	U	U	U
	NEG	$\overline{SRC}$ +1→Dest		Y ← $\overline{SRC}$ +1	NC	NC	NC	NC	U	U	U	U

SRC = Source
U = Update
NC = No Change

0 = Reset
1 = Set
i = 0 to 15 when not specified

Two Operand Instructions

The Two Operand Instructions contain five indicators: byte or word mode, opcode, R source, S source, and destination. They are further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. The first type has two formats; the only difference is in the quadrant. Under the control of instruction inputs, the desired function is performed on the specified sources and the result is stored in the specified destination or placed on the Y-bus or both. The least significant four bits of the status register (OVR, N, C, Z) are affected by the arithmetic functions performed and only the N and Z bits are affected by the logical functions performed. The OVR and C bits of the status register are forced to ZERO for logical functions. Add with carry and Subtract with carry instructions are useful for Multiprecision Add or Subtract.

TWO OPERAND FIELD DEFINITIONS

```
        15 14 13 12      9 8      5 4           0
       +-----+-----+--------+--------+------------+
TOR1   | B/W | Quad|SRC-SRC | Opcode |RAM Address |
       |     |     | -Dest  |        |            |
       +-----+-----+--------+--------+------------+

       +-----+-----+--------+--------+------------+
TOR2   | B/W | Quad|SRC-SRC | Opcode |RAM Address |
       |     |     | -Dest  |        |            |
       +-----+-----+--------+--------+------------+

       +-----+-----+--------+--------+------------+
TONR   | B/W | Quad|SRC-SRC | Opcode |   Dest     |
       +-----+-----+--------+--------+------------+
```

TWO OPERAND INSTRUCTIONS

Instruction	B/W	Quad			R^1	S^1	$Dest^1$		Opcode			RAM Address		
	0 = B	00	0000	TORAA	RAM	ACC	ACC	0000	SUBR	S minus R	00000	R00	RAM Reg 00
	1 = W		0010	TORIA	RAM	I	ACC	0001	SUBRC[2]	S minus R with carry	. .	. .	. . . .
			0011	TODRA	D	RAM	ACC				11111	R31	RAM Reg 31
			1000	TORAY	RAM	ACC	Y Bus	0010	SUBS	R minus S			
			1010	TORIY	RAM	I	Y Bus	0011	SUBSC[2]	R minus S with carry			
			1011	TODRY	D	RAM	Y Bus						
TOR1			1100	TORAR	RAM	ACC	RAM	0100	ADD	R plus S			
			1110	TORIR	RAM	I	RAM	0101	ADDC	R plus S with carry			
			1111	TODRR	D	RAM	RAM						
								0110	AND	$\underline{R \cdot S}$			
								0111	NAND	$R \cdot S$			
								1000	EXOR	$\underline{R \oplus S}$			
								1001	NOR	$\overline{R + S}$			
								1010	OR	$\underline{R + S}$			
								1011	EXNOR	$R \oplus S$			

Instruction	B/W	Quad			R^1	S^1	$Dest^1$		Opcode			RAM Address		
	0 = B	10	0001	TODAR	D	ACC	RAM	0000	SUBR	S minus R	00000	R00	RAM Reg 00
	1 = W		0010	TOAIR	ACC	I	RAM	0001	SUBRC[2]	S minus R with carry	. .	. .	. . . .
			0101	TODIR	D	I	RAM				11111	R31	RAM Reg 31
								0010	SUBS	R minus S			
								0011	SUBSC[2]	R minus S with carry			
TOR2								0100	ADD	R plus S			
								0101	ADDC	R plus S with carry			
								0110	AND	$\underline{R \cdot S}$			
								0111	NAND	$R \cdot S$			
								1000	EXOR	$\underline{R \oplus S}$			
								1001	NOR	$\overline{R + S}$			
								1010	OR	$\underline{R + S}$			
								1011	EXNOR	$R \oplus S$			

Notes: 1. R = Source
S = Source
Dest = Destination
2. During subtraction the carry is interpreted as $\overline{borrow}$.

TWO OPERAND INSTRUCTIONS

Instruction	B/W	Quad	R^1 S^1			Opcode			Destination	
TONR	0 = B 1 = W	11	0001 TODA D ACC 0010 TOAI ACC I 0101 TODI D I		0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011	SUBR SUBRC[3] SUBS SUBSC[3] ADD ADDC AND NAND EXOR NOR OR EXNOR	S minus R S minus R with carry R minus S R minus S with carry R plus S R plus S with carry $\overline{R \cdot S}$ $\overline{R \cdot S}$ $\overline{R \oplus S}$ $\overline{R + S}$ $R + S$ $\overline{R \oplus S}$	00000 NRY Y Bus 00001 NRA ACC 00100 NRS Status[2] 00101 NRAS ACC, Status[2]	

Notes: 1. R = Source
S = Source
2. When status is destination,
Status i←Y_i i = 0 to 3 (Byte mode)
i = 0 to 7 (Word mode)
3. During subtraction the carry is interpreted as $\overline{borrow}$.
4. OVR = $C_8 \oplus C_7$ (Byte mode)
OVR = $C_{16} \oplus C_{15}$ (Word mode)

Y BUS AND STATUS CONTENTS – TWO OPERAND INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag 1	LINK	OVR	N	C	Z
TOR1 TOR2 TONR	SUBR	S minus R	0 = B	$Y \leftarrow S + \overline{R} + 1$	NC	NC	NC	NC	U	U	U	U
	SUBRC	S minus R with carry	1 = w	$Y \leftarrow S + \overline{R} + QC$	NC	NC	NC	NC	U	U	U	U
	SUBS	R minus S		$Y \leftarrow R + \overline{S} + 1$	NC	NC	NC	NC	U	U	U	U
	SUBSC	R minus S with carry		$Y \leftarrow R + \overline{S} + QC$	NC	NC	NC	NC	U	U	U	U
	ADD	R plus S		$Y \leftarrow R + S$	NC	NC	NC	NC	U	U	U	U
	ADDC	R plus S with carry		$Y \leftarrow R + S + QC$	NC	NC	NC	NC	U	U	U	U
	AND	$R \cdot S$		$Y \leftarrow R_i$ AND S_i	NC	NC	NC	NC	0	U	0	U
	NAND	$\overline{R \cdot S}$		$Y_i \leftarrow R_i$ NAND S_i	NC	NC	NC	NC	0	U	0	U
	EXOR	$R \oplus S$		$Y_i \leftarrow R_i$ EXOR S_i	NC	NC	NC	NC	0	U	0	U
	NOR	$\overline{R + S}$		$Y_i \leftarrow R_i$ NOR S_i	NC	NC	NC	NC	0	U	0	U
	OR	$R + S$		$Y_i \leftarrow R_i$ OR S_i	NC	NC	NC	NC	0	U	0	U
	EXNOR	$\overline{R \oplus S}$		$Y_i \leftarrow R_i$ EXNOR S_i	NC	NC	NC	NC	0	0	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

Single Bit Shift Instructions

The Single Bit Shift Instructions contain four indicators: byte or word mode, direction and shift linkage, source and destination. They are further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. Under the control of the instruction inputs, the desired shift function is performed on the specified source and the result is stored in the specified destination or placed on the Y-bus or both. The direction and shift linkage indicator defines the direction of the shift (up or down) as well as what will be shifted into the vacant bit. On a shift-up instruction, the LSB may be loaded with ZERO, ONE, or the Link-Status bit (QLINK). The MSB is loaded into the Link-Status bit as shown in Figure 2. On a shift-down instruction, the MSB may be loaded with ZERO, ONE, the contents of the Status Carry flip-flop, (QC), the Exclusive-OR of the Negative-Status bit and the Overflow-Status bit (QN ⊕ QOVR) or the Link-Status bit. The LSB is loaded into the Link-Status bit as shown in Figure 3. The N and Z bits of the Status register are affected but the OVR and C bits are forced to ZERO. The Shift-Down with QN ⊕ QOVR is useful for Two's Complement multiplication.
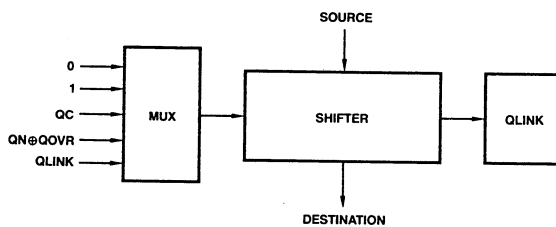
SINGLE BIT SHIFT FIELD DEFINITIONS:

	15 14	13 12	9 8	5 4	0
SHFTR	B/W	Quad	SRC-Dest	Opcode	RAM Address

	15 14	13 12	9 8	5 4	0
SHFTNR	B/W	Quad	SRC	Opcode	Dest
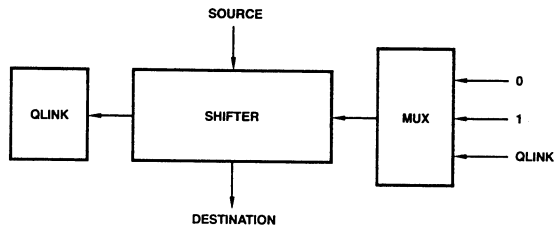
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Figure 2. Shift Up Function

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Figure 3. Shift Down Function

SINGLE BIT SHIFT INSTRUCTIONS

SINGLE BIT SHIFT

Instruction	B/W	Quad			U^1	$Dest^1$		Opcode			RAM Address		
SHFTR	0 = B 1 = W	10	0110 0111	SHRR SHDR	RAM D	RAM RAM	0000 0001 0010 0100 0101 0110 0111 1000	SHUPZ SHUP1 SHUPL SHDNZ SHDN1 SHDNL SHDNC SHDNOV	Up Up Up Down Down Down Down Down	0 1 QLINK 0 1 QLINK QC QN⊕QOVR	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31

Instruction	B/W	Quad			U^1		Opcode			Destination		
SHFTNR	0 = B 1 = W	11	0110 0111	SHA SHD	ACC D	0000 0001 0010 0100 0101 0110 0111 1000	SHUPZ SHUP1 SHUPL SHDNZ SHDN1 SHDNL SHDNC SHDNOV	Up Up Up Down Down Down Down Down	0 1 QLINK 0 1 QLINK QC QN⊕QOVR	00000 00001	NRY NRA	Y Bus ACC

Note 1. U = Source
Dest = Destination

Y BUS AND STATUS – SINGLE BIT SHIFT INSTRUCTIONS

Instruction	Opcode	Description		B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SHR SHNR	SHUPZ SHUP1 SHUPL	Up Up Up	0 1 QLINK	1 = W	$Y_i \leftarrow SRC_{i-1}$, i = 1 to 15; $Y_0 \leftarrow$ Shift Input	NC	NC	NC	SRC_{15}*	0	SRC_{14}	0	U
				0 = B	$Y_i \leftarrow SRC_{i-1}$, i = 1 to 7; $Y_0 \leftarrow$ Shift Input; $Y_8 \leftarrow SRC_7$, $Y_i \leftarrow SRC_{i-9}$ for i = 9 to 15	NC	NC	NC	SRC_7*	0	SRC_6	0	U
	SHDNZ SHDN1 SHDNL SHDNC SHCNOV	Down Down Down Down Down	0 1 QLINK QC QN⊕QOVR	1 = W	$Y_i \leftarrow SRC_{i+1}$, i = 0 to 14; $Y_{15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U
				0 = B	$Y_i \leftarrow SRC_{i+1}$, i = 0 to 6; $Y_i \leftarrow SRC_{i-7}$, i = 8 to 14; $Y_{7,15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U

*Shifted Output is loaded into the QLINK.

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified
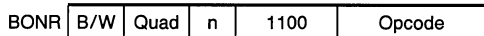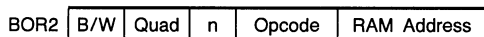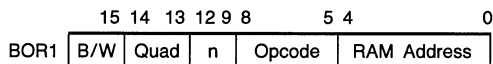
Bit Oriented Instructions

The Bit Oriented Instructions contain four indicators: byte or word mode, operation, source/destination, and the bit position of the bit to be operated on (Bit 0 is the least significant bit). They are further subdivided into two types. The first type uses the RAM as both source and destination and has two kinds of formats which differ only by quadrant. The second type does not use the RAM as a source or a destination. Under the control of the instruction inputs, the desired function is performed on the specified source and the result is stored in the specified destination or placed on the Y-bus or both. The operations which can be performed are: Set Bit n which forces the nth bit to a ONE leaving other bits unchanged; Reset Bit n which forces the nth bit to ZERO leaving the other bits unchanged; Test Bit n, which sets the ZERO Status Bit depending on the state of bit n leaving all the bits unchanged; Load 2^n, which loads ONE in Bit position n and ZERO in all other bit positions; Load $\overline{2^n}$ which loads ZERO in bit position n and ONE in all other bit positions; increment by 2^n, which adds 2^n to the operand; and decrement by 2^n which subtracts 2^n from the operand. For all the Load, Set, Reset and Test instructions, the N and Z bits are affected and OVR and C bit of the Status register are forced to ZERO. For all arithmetic instructions the LSH (OVR, C, N, Z bits) of the Status register is affected.

BIT ORIENTED FIELD DEFINITIONS

```
        15 14  13 12 9 8      5 4           0
BOR1  | B/W | Quad | n | Opcode | RAM Address |


BOR2  | B/W | Quad | n | Opcode | RAM Address |


BONR  | B/W | Quad | n |  1100  |   Opcode    |
```

BIT ORIENTED INSTRUCTIONS

Instruction	B/W	Quad	n	Opcode			RAM Address		
BOR1	0 = B 1 = W	11	0 to 15	1101 1110 1111	SETNR RSTNR TSTNR	Set RAM, bit n Reset RAM, bit n Test RAM, bit n	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Instruction	B/W	Quad	n	Opcode			RAM Address		
BOR2	0 = B 1 = W	10	0 to 15	1100 1101 1110 1111	LD2NR LDC2NR A2NR S2NR	$2^n \to$ RAM $\overline{2^n} \to$ RAM RAM plus $2^n \to$ RAM RAM minus $2^n \to$ RAM	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Instruction	B/W	Quad	n	Opcode		
BONR	0 = B 1 = W	11	0 to 15	1100	00000 00001 00010 00011 00100 00101 00110 00111 10000 10001 10010 10100 10101 10110 10111	TSTNA RSTNA SETNA A2NA S2NA LD2NA LDC2NA TSTND RSTND SETND A2NDY S2NDY LS2NY LDC2NY	Test ACC, bit n Reset ACC, bit n Set ACC, bit n ACC plus $2^n \to$ ACC ACC minus $2^n \to$ ACC $2^n \to$ ACC $\overline{2^n} \to$ ACC Test D, bit n Reset D, bit n Set D, bit n D plus $2^n \to$ Y BUS D minus $2^n \to$ Y Bus $2^n \to$ Y Bus $\overline{2^n} \to$ Y Bus

BIT ORIENTED INSTRUCTIONS
Y BUS AND STATUS – BIT ORIENTED INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
BOR1	SETNR	Set RAM Bit n	0 = B	$Y_i \leftarrow RAM_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	RSTNR	Reset RAM, Bit n	1 = W	$Y_i \leftarrow RAM_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	TSTNR	Test RAM, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow SRC_n$	NC	NC	NC	NC	0	U	0	U
BOR2	LD2NR	$2^n \rightarrow RAM$		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NR	$\overline{2^n} \rightarrow RAM$		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0
	A2NR	$RAM + 2^n \rightarrow RAM$		$Y \leftarrow RAM + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NR	$RAM - 2^n \rightarrow RAM$		$Y \leftarrow RAM - 2^n$	NC	NC	NC	NC	U	U	U	U
BONR	TSTNA	Test ACC, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow ACC_n$	NC	NC	NC	NC	0	U	0	U
	RSTNA	Reset ACC, Bit n		$Y_i \leftarrow ACC_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	SETNA	Set ACC, Bit n		$Y_i \leftarrow ACC_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	A2NA	$ACC + 2^n \rightarrow ACC$		$Y \leftarrow ACC + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NA	$ACC - 2^n \rightarrow ACC$		$Y \leftarrow ACC - 2^n$	NC	NC	NC	NC	U	U	U	U
	LD2NA	$2^n \rightarrow ACC$		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NA	$\overline{2^n} \rightarrow ACC$		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0
	TSTND	Test D, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow D_n$	NC	NC	NC	NC	0	U	0	U
	RSTND	Reset D, Bit n*		$Y_i \leftarrow D_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	SETND	Set D, Bit n*		$Y_i \leftarrow D_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	A2NDY	$D + 2^n \rightarrow Y$ Bus		$Y \leftarrow D + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NDY	$D - 2^n \rightarrow Y$ Bus		$Y \leftarrow D - 2^n$	NC	NC	NC	NC	U	U	U	U
	LD2NY	$2^n \rightarrow Y$ Bus		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NY	$\overline{2^n} \rightarrow Y$ Bus		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*Destination is not D Latch but Y Bus.

Rotate by n Bits Instructions

The Rotate by n Bits Instructions contain four indicators: byte or word mode, source, destination and the number of places the source is to be rotated. They are further subdivided into two types. The first type uses RAM as a source and/or a destination and the second type does not use RAM as a source or destination. The first type has two different formats and the only difference is in the quadrant. The second type has only one format as shown in the table. Under the control of instruction inputs, the n indicator specifies the number of bit positions the source is to be rotated up (0 to 15), and the result is either stored in the specified destination or placed on the Y-bus or both. An example of this instruction is given in Figure 4. In the Word mode, all 16 bits are rotated up; while in the Byte mode, only the lower 8 bits (0-7) are rotated up. In the Word mode, a rotate up by n bits is equivalent to a rotate down by (16-n) bits. Similarly, in the Byte mode a rotate up by n bits is equivalent to a rotate down by (8-n) bits. The N and Z bits of the Status Register are affected and OVR and C bits are forced to ZERO.

EXAMPLE: n = 4, Word Mode

Source	0001	0011	0111	1111
Destination	0011	0111	1111	0001

EXAMPLE: n = 4, Byte Mode

Source	0001	0011	0111	1111
Destination	0001	0011	1111	0111

Figure 4. Rotate by n Example

ROTATE BY n BITS FIELD DEFINITIONS

	15 14	13 12	9 8	5 4	0
ROTR1	B/W	Quad	n	SRC-Dest	RAM Address
ROTR2	B/W	Quad	n	SRC-Dest	RAM Address
ROTNR	B/W	Quad	n	1100	SRC-Dest

ROTATE BY n BITS INSTRUCTIONS

Instruction	B/W	Quad	n		U^1	$Dest^1$	RAM Address		
ROTR1	0 = B 1 = W	00	0 to 15	1100 1110 1111	RTRA RTRY RTRR	RAM RAM RAM	ACC Y Bus RAM	00000 . . 11111	R00 RAM Reg 00 . . . . . . R31 RAM Reg 31

Instruction	B/W	Quad	n		U^1	$Dest^1$	RAM Address		
ROTR2	0 = B 1 = W	01	0 to 15	0000 0001	RTAR RTDR	ACC D	RAM RAM	00000 11111	R00 RAM Reg 00 . . . . . . R31 RAM Reg 31

Instruction	B/W	Quad	n					U^1	$Dest^1$
ROTNR	0 = B 1 = W	11	0 to 15	1100			11000 11001 11100 11101	RTDY D RTDA D RTAY ACC RTAA ACC	Y Bus ACC Y Bus ACC

Note: 1. U = Source
Dest = Destination

Y BUS AND STATUS – ROTATE BY n BITS INSTRUCTIONS

Instruction	Op-code	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTR1 ROTR2 ROTNR		1 = W	$Y_i \leftarrow SRC_{(i-n)mod16}$	NC	NC	NC	NC	0	SRC_{15-n}	0	U
		0 = B	$Y_i \leftarrow SRC_{i+8} = SRC_{(i-n)mod8}$ for i = 0 to 7	NC	NC	NC	NC	0	SRC_{8-n}	0	U

SRC = Source
U = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

Rotate and Merge Instruction

The Rotate and Merge Instructions contain five indicators: byte or word mode, rotated source, non-rotated source/destination, mask and the number of bit positions a source is to be rotated. The function performed by the Rotate and Merge instruction is illustrated in Figure 5. The rotated source, U, is rotated up by the Barrel Shifter n places. The mask input then selects, on a bit by bit basis, the rotated U input or R input. A ZERO in bit i of the mask will select the ith bit of the R input as the ith output bit, while ONE in bit i will select the ith rotated U input as the output bit. The output word is stored in the non-rotated operand location. The N and Z bits are affected. The OVR and C bits of the Status register are forced to ZERO. An example of this instruction is given in Figure 6.
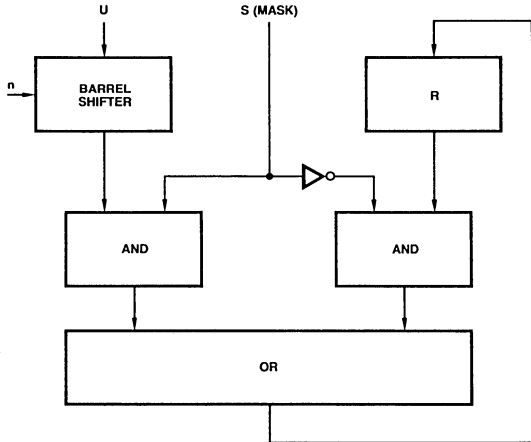
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Figure 5. Rotate and Merge Function

ROTATE AND MERGE FIELD DEFINITIONS:

	15 14	13 12 9	8	5 4	0
ROTM	B/W	Quad	n	ROT SRC- Non ROT SRC- Mask	RAM Address

EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	1010	1010	1010	1010
Mask (S)	0000	1111	0000	1111
Destination	1010	0101	1010	0011

Figure 6. Rotate and Merge Example

ROTATE AND MERGE INSTRUCTION

Instruction	B/W	Quad	n			U	R/Dest	S	RAM Address		
ROTM	0 = B 1 = W	01	0 to 15	0111 1000 1001 1010 1100 1110	MDAI MDAR MDRI MDRA MARI MRAI	D D D D ACC RAM	ACC ACC RAM RAM RAM ACC	I RAM I ACC I I	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31

U = Rotated Source
R/Dest = Non-Rotated Source and Destination
S = Mask

Y BUS AND STATUS – ROTATE AND MERGE INSTRUCTIONS

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTM		1=W	$Y_i \leftarrow$ (Non Rot Op)$_i \cdot \overline{(mask)}_i$ + (Rot Op)$_{(i-n) \bmod 16} \cdot (mask)_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow$ (Non Rot Op)$_i \cdot \overline{(mask)}_i$ + (Rot Op)$_{(i-n) \bmod 8} \cdot (mask)_i$	NC	NC	NC	NC	0	U	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

Rotate and Compare Instructions

The Rotate and Compare Instructions contain five indicators: byte or word mode, rotated source, non-rotated source, mask, and the number of bit positions the rotated source is to be rotated up. Under the control of instruction inputs, the function performed by the Rotate and Compare instruction is illustrated in Figure 7. The rotated operand is rotated by the Barrel Shifter n places. The mask is inverted and ANDed on a bit-by-bit basis with the output of the Barrel Shifter and R input. Thus, a ONE in the mask input eliminates that bit from the comparison. A ZERO allows the comparison. If the comparison passes, the Zero flag is set. If it fails, the Zero flag is reset. The N and Z bit are affected. The OVR and C bits of the Status register are forced to ZERO. An example of this instruction is given in Figure 8.
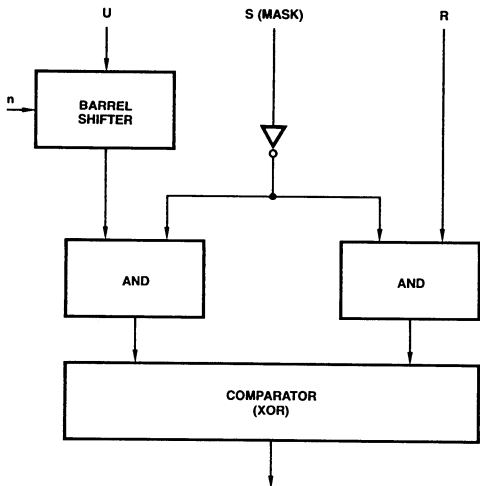

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Figure 7. Rotate and Compare Function

ROTATE AND COMPARE FIELD DEFINITIONS

	15 14	13 12 9	8	5 4	0
ROTC	B/W	Quad	n	Rot Src- Non Rot Src- Mask	RAM Address

EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
U Rotated	0001	0101	0110	0011
R	0001	0101	1111	0000
Mask (S)	0000	0000	1111	1111
Z (status) = 1				

Figure 8. Rotate and Compare Examples

ROTATE AND COMPARE INSTRUCTIONS

Instruction	B/W	Quad	n			U	R	S	RAM Address		
ROTC	0 = B 1 = W	01	0 to 15	0010 0011 0100 0101	CDAI CDRI CDRA CRAI	D D D RAM	ACC RAM RAM ACC	I I ACC I	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . RAM Reg 31

U = Rotated Source
R = Non-Rotated Source
S = Mask

Y BUS AND STATUS – ROTATE AND COMPARE INSTRUCTIONS

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTC		1 = W	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})}_i \oplus$ $(\text{Rot Op})_{(i-n)\bmod 16} \cdot \overline{(\text{mask})}_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})}_i \oplus$ $(\text{Rot Op})_{(i-n)\bmod 8} \cdot \overline{(\text{mask})}_i$	NC	NC	NC	NC	0	U	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

Prioritize Instruction

The Prioritize Instructions contain four indicators: byte or word mode, operand source (R), mask source (S) and destination. They are further subdivided into two types. The function performed by the Prioritize instruction is shown in Figure 9. The R operand is ANDed with the complement of the Mask operand. A ZERO in the Mask operand allows the corresponding bit in the R operand to participate in the priority encoding function. A ONE in the Mask operand forces the corresponding bit in the R operand to a ZERO, eliminating it from participation in the priority encoding function.

The priority encoder accepts a 16-bit input and produces a 5-bit binary-weighted code indicating the bit position of the highest priority active bit. If none of the inputs are active, the output is ZERO. In the Word mode, if input bit 15 is active, the output is 1, etc. Figure 10 lists the output as a function of the highest-priority active-bit position in both the Word and Byte mode. The N and Z bits are affected and the OVR and C bits of the status register are forced to ZERO. The only limitation in this instruction is that the operand and the mask must be different sources.

Figure 9. Prioritize Function

PRIORITIZE FIELD DEFINITIONS

15	14 13	12 9	8 5	4 0
B/W	Quad	Destination	Source (R)	RAM Address/Mask (S)

B/W	Quad	Mask (S)	Destination	RAM Address/Source (R)

B/W	Quad	Mask (S)	Source (R)	RAM Address/Destination

B/W	Quad	Mask (S)	Source (R)	Destination

WORD MODE		BYTE MODE*	
Highest Priority Active Bit	**Encoder Output**	**Highest Priority Active Bit**	**Encoder Output**
None	0	None	0
15	1	7	1
14	2	6	2
•	•	•	•
•	•	•	•
1	15	1	7
0	16	0	8

*Bits 8 through 15 do not participate

Figure 10.

PRIORITIZE INSTRUCTION

Instruction	B/W	Quad	Destination			Source (R)			RAM Address/Mask (S)		
PRT1	0 = B 1 = W	10	1000 1010 1011	PRIA PR1Y PR1R	ACC Y Bus RAM	0111 1001	RPT1A PR1D	ACC D	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Instruction	B/W	Quad	Mask (S)			Destination			RAM Address/Source (R)		
PRT2	0 = B 1 = W	10	1000 1010 1011	PRA PRZ PRI	Acc 0 I	0000 0010	PR2A PR2Y	ACC Y Bus	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Instruction	B/W	Quad	Mask (S)			Source (R)			RAM Address/Dest		
PRT3	0 = B 1 = W	10	1000 1010 1011	PRA PRZ PRI	ACC 0 I	0011 0100 0110	PR3R PR3A PR3D	RAM ACC D	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Instruction	B/W	Quad	Mask (S)			Source (R)			Destination		
PRTNR	0 = B 1 = W	11	1000 1010 1011	PRA PRZ PRI	ACC 0 I	0100 0110	PRTA PRTD	ACC D	00000 00001	NRY NRA	Y Bus ACC

Y BUS AND STATUS - PRIORITIZE INSTRUCTIONS

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
PRT1 PRT2		1 = W	$Y_i \leftarrow$ CODE $(SCR_n \cdot \overline{mask_n})$; $Y_m \leftarrow 0$; i = 0 to 4 and n = 0 to 15 m = 5 to 15	NC	NC	NC	NC	0	U	0	U
PRT3 PRTNR		0 = B	$Y_i \leftarrow$ CODE $(SCR_n \cdot \overline{mask_n})$; $Y_m \leftarrow 0$; i = 0 to 3 and n = 0 to 7 m = 4 to 15	NC	NC	NC	NC	0	U	0	U

SRC = Source   NC = No Change   1 = Set
U = Update   0 = Reset   i = 0 to 15 when not specified

Cyclic-Redundancy-Check Instruction

The Cyclic-Redundancy-Check (CRC) Instructions contain one indicator: address of a RAM register to use as the check sum register. The CRC instruction provides a method for generation of the check bits in a CRC calculation. Two CRC instructions are provided – CRC Forward and CRC Reverse. The reason for providing two instructions is that CRC standards do not specify which data bit is to be transmitted first, the LSB or the MSB, but they do specify which check bit must be transmitted first. Figure 11 illustrates the method used to generate these check bits for the CRC Forward function and Figure 12 illustrates method used for the CRC Reverse function. The ACC serves as a polynomial mask to define the generating polynomial while the RAM register holds the partial result and eventually the calculated check sum. The LINK-bit is used as the serial input. The serial input combines with the MSB of the check-sum register, according to the polynomial defined by the polynomial mask register. When the last input bit has been processed, the check-sum register contains the CRC check bits. The LINK, N and Z bits are affected and the OVR and C bits of the Status register are forced to ZERO.
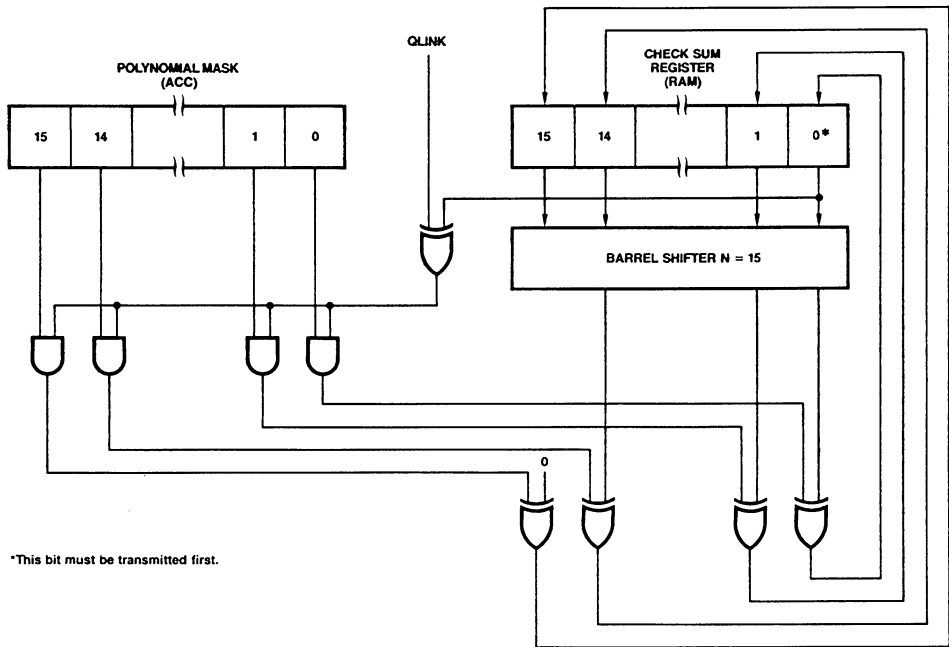
CYCLIC-REDUNDANCY-CHECK FIELD DEFINITIONS:

	15	14 13 12	9 8	5 4	0
CRCF	1	Quad	0110	0011	RAM Address

	15	14 13 12	9 8	5 4	0
CRCR	1	Quad	0110	1001	RAM Address
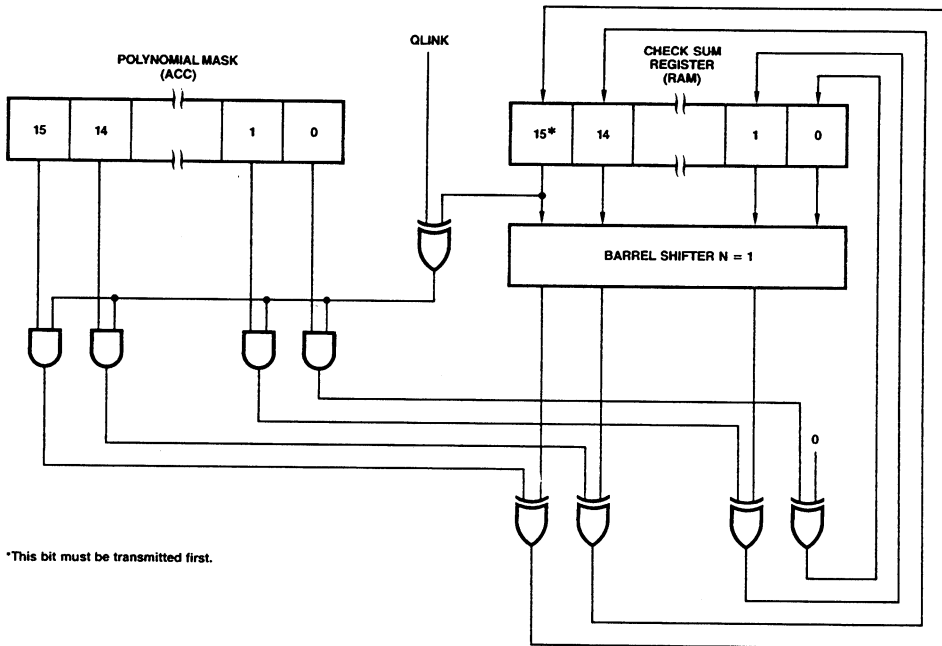
Figure 11. CRC Forward Function

PF000330

Figure 12. CRC Reverse Function

*This bit must be transmitted first.

PF000320

CYCLIC-REDUNDANCY-CHECK

Instruction	B/W	Quad			RAM Address		
CRCF	1	10	0110	0011	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**			**RAM Address**		
CRCR	1	10	0110	1001	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Y BUS AND STATUS – CYCLIC-REDUNDANCY-CHECK INSTRUCTION

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
CRCF		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_i]$ $\oplus RAM_{i-1}$ for i = 15 to 1 $Y_0 \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_0] \oplus 0$	NC	NC	NC	RAM_{15}*	0	U	0	U
CRCR		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_i]$ $\oplus RAM_{i+1}$ for i = 14 to 0 $Y_{15} \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_{15}] \oplus 0$	NC	NC	NC	RAM_0*	0	U	0	U

*QLINK is loaded with the shifted out bit from the checksum register.

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

Status Instructions

Status Instructions

The Set Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register (Figure 13), are to be set (forced to a ONE).

7	6	5	4	3	2	1	0
Flag3	Flag2	Flag1	LINK	OVR	N	C	Z

MPR-775

Figure 13. Status Byte

The Reset Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register, are to be reset (forced to ZERO).

The Store Status Instruction contains two indicators; byte/word and a second indicator that specifies the destination of the status register. The Store Status Instruction allows the status of the processor to be saved and restored later, which is an especially useful function for interrupt handling.

The status register is always stored in the lower byte of the RAM or the ACC register. Depending upon byte or word mode the upper byte is unchanged or loaded with all ZEROs respectively.

The Load Status instructions are included in the single operand and two operand instruction types.

The Test Status Instructions contain a single indicator which specifies which one of the 12 possible test conditions are to be placed on the Conditional-Test output. Besides the eight bits in the Status register (QZ, QC, QN, QOVR, QLINK, QFlag1, QFlag 2, and QFlag3), four logical functions (QN ⊕ QOVR), (QN ⊕ QOVR) + QZ, QZ + $\overline{QC}$ and LOW may also be selected. These functions are useful in testing results of Two's Complement and unsigned number arithmetic operations. The status register may also be tested via the bidirectional T bus. The code to test the status register via T bus is similar to the code used by instruction lines I_1 to I_4 as shown below. Instruction lines I_{0-4} have priority over T bus for testing the status register on CT output. See the discussion on the status register for a full description.

T_4 I_4	T_3 I_3	T_2 I_2	T_1 I_1	CT
0	0	0	0	(N ⊕ OVR) + Z
0	0	0	1	N ⊕ OVR
0	0	1	0	Z
0	0	1	1	OVR
0	1	0	0	LOW*
0	1	0	1	C
0	1	1	0	Z + $\overline{C}$
0	1	1	1	N
1	0	0	0	LINK
1	0	0	1	Flag1
1	0	1	0	Flag2
1	0	1	1	Flag3

*LOW means CT is forced LOW

STATUS FIELD DEFINITIONS

15 14 13 12 9 8 5 4 0

SETST	0	Quad	1011	1010	Opcode
RSTST	0	Quad	1010	1010	Opcode
SVSTR	B/W	Quad	0111	1010	RAM Address/Dest
SVSTNR	B/W	Quad	0111	1010	Destination

STATUS INSTRUCTIONS

Instruction	B/W	Quad			Opcode		
SETST	0	11	1011	1010	00011 00101 00110 01001 01010	SONCZ SL SF1 SF2 SF3	Set OVR, N, C, Z Set LINK Set Flag1 Set Flag2 Set Flag3
Instruction	**B/W**	**Quad**			**Opcode**		
RSTST	0	11	1010	1010	00011 00101 00110 01001 01010	RONCZ RL RF1 RF2 RF3	Reset OVR, N, C, Z Reset LINK Reset Flag1 Reset Flag2 Reset Flag3
Instruction	**B/W**	**Quad**			**RAM Address/Dest**		
SVSTR	0 = B 1 = W	10	0111	1010	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
					Destination		
SVSTNR	0 = B 1 = W	11	0111	1010	00000 00001	NRY NRA	Y Bus ACC

STATUS INSTRUCTIONS

Instruction	B/W	Quad			Opcode (CT)		
Test	0	11	1001	1010	00000 00010 00100 00110 01000 01010 01100 01110 10000 10010 10100 10110	TNOZ TNO TZ TOVR TLOW TC TZC TN TL TF1 TF2 TF3	Test $(N \oplus OVR) + Z$ Test $N \oplus OVR$ Test Z Test OVR Test LOW Test C Test $Z + \overline{C}$ Test N Test LINK Test Flag1 Test Flag2 Test Flag3

Note:

Y BUS AND STATUS – STATUS INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SETST	SONCZ	Set OVR, N, C, Z	0 = B	$Y_i \leftarrow 1$ for i = 0 to 15	NC	NC	NC	NC	1	1	1	1
	SL	Set LINK			NC	NC	NC	1	NC	NC	NC	NC
	SF1	Set Flag1			NC	NC	1	NC	NC	NC	NC	NC
	SF2	Set Flag2			NC	1	NC	NC	NC	NC	NC	NC
	SF3	Set Flag3			1	NC	NC	NC	NC	NC	NC	NC
RSTST	RONCZ	Reset OVR, N, C, Z	0 = B	$Y_i \leftarrow 0$ for i = 0 to 15	NC	NC	NC	NC	0	0	0	0
	RL	Reset LINK			NC	NC	NC	0	NC	NC	NC	NC
	RF1	Reset Flag1			NC	NC	0	NC	NC	NC	NC	NC
	RF2	Reset Flag2			NC	0	NC	NC	NC	NC	NC	NC
	RF3	Reset Flag3			0	NC	NC	NC	NC	NC	NC	NC
SVSTR SVSTNR		Save Status*	0 = B 1 = W	$Y_i \leftarrow$ Status for i – 0 to 7; $Y_i \leftarrow 0$ for i = 8 to 15	NC	NC	NC	NC	NC	NC	NC	NC
Test	TNOZ	Test $(N \oplus OVR) + Z$	0 = B	**	NC	NC	NC	NC	NC	NC	NC	NC
	TNO	Test $N \oplus OVR$			NC	NC	NC	NC	NC	NC	NC	NC
	TZ	Test Z			NC	NC	NC	NC	NC	NC	NC	NC
	TOVR	Test OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TLOW	Test LOW			NC	NC	NC	NC	NC	NC	NC	NC
	TC	Test C			NC	NC	NC	NC	NC	NC	NC	NC
	TZC	Test $Z + \overline{C}$			NC	NC	NC	NC	NC	NC	NC	NC
	TN	Test N			NC	NC	NC	NC	NC	NC	NC	NC
	TL	Test LINK			NC	NC	NC	NC	NC	NC	NC	NC
	TF1	Test Flag1			NC	NC	NC	NC	NC	NC	NC	NC
	TF2	Test Flag2			NC	NC	NC	NC	NC	NC	NC	NC
	TF3	Test Flag3			NC	NC	NC	NC	NC	NC	NC	NC

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*In byte mode only the lower byte from the Y bus is loaded into the RAM or ACC and in word mode all 16-bits from the Y bus are loaded into the RAM or ACC.

**Y-Bus is Undefined.

NO-OP Instruction

The NO-OP Instruction has a fixed 16-bit code. This instruction does not change any internal registers in the Am29117. It preserves the status register, RAM register and the ACC register.

NO OPERATION FIELD DEFINITION

	15	14 13 12		9 8	5 4		0
NOOP	0	11	1000	1010	00000		

NO-OP INSTRUCTION

Instruction	B/W	Quad			
NOOP	0	11	1000	1010	00000

Y BUS AND STATUS – NO-OP INSTRUCTION

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
NOOP		0 = B	*	NC	NC	NC	NC	NC	NC	NC	NC

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified
  *Y-Bus is undefined.

SUMMARY OF MNEMONICS

INSTRUCTION TYPE

SOR	Single Operand RAM
SONR	Single Operand Non-RAM
TOR1	Two Operand RAM (Quad 0)
TOR2	Two Operand RAM (Quad 2)
TONR	Two Operand Non-RAM
SHFTR	Single Bit Shift RAM
SHFTNR	Single Bit Shift Non-RAM
ROTR1	Rotate n Bits RAM (Quad 0)
ROTR2	Rotate n Bits RAM (Quad 1)
ROTNR	Rotate n Bits Non-RAM
BOR1	Bit Oriented RAM (Quad 3)
BOR2	Bit Oriented RAM (Quad 2)
BONR	Bit Oriented Non-RAM
ROTM	Rotate and Merge
ROTC	Rotate and Compare
PRT1	Prioritize RAM; Type 1
PRT2	Prioritize RAM; Type 2
PRT3	Prioritize RAM; Type 3
PRTNR	Prioritize Non-RAM
CRCF	Cyclic Redundancy Check Forward
CRCR	Cyclic Redundancy Check Reverse
NOOP	No Operation
SETST	Set Status
RSTST	Reset Status
SVSTR	Save Status RAM
SVSTNR	Save Status Non-RAM
TEST	Test Status

SOURCE AND DESTINATION

Single Operand

SORA	Single Operand RAM to ACC
SORY	Single Operand RAM to Y Bus
SORS	Single Operand RAM to Status
SOAR	Single Operand ACC to RAM
SODR	Single Operand D to RAM
SOIR	Single Operand I to RAM
SOZR	Single Operand 0 to RAM
SOZER	Single Operand D(0E) to RAM
SOSER	Single Operand D(SE) to RAM
SORR	Single Operand RAM to RAM
SOA	Single Operand ACC
SOD	Single Operand D
SOI	Single Operand I
SOZ	Single Operand 0
SOZE	Single Operand D(0E)
SOSE	Single Operand D(SE)
NRY	Non-RAM Y Bus
NRA	Non-RAM ACC
NRS	Non-RAM Status
NRAS	Non-RAM ACC, Status

Two Operand

TORAA	Two Operand RAM, ACC to ACC
TORIA	Two Operand RAM, I to ACC
TODRA	Two Operand D, RAM to ACC
TORAY	Two Operand RAM, ACC to Y Bus
TORIY	Two Operand RAM, I to Y Bus
TODRY	Two Operand D, RAM to Y Bus
TORAR	Two Operand RAM, ACC to RAM
TORIR	Two Operand RAM, I to RAM
TODRR	Two Operand D, RAM to RAM
TODAR	Two Operand D, ACC to RAM
TOAIR	Two Operand ACC, I to RAM
TODIR	Two Operand D, I to RAM
TODA	Two Operand D, ACC
TOAI	Two Operand ACC, I
TODI	Two Operand D, I

Single Bit Shift

SHRR	Shift RAM, Store in RAM
SHDR	Shift D, Store in RAM
SHA	Shift ACC
SHD	Shift D

Rotate n Bits

RTRA	Rotate RAM, Store in ACC
RTRY	Rotate RAM, Place on Y Bus
RTRR	Rotate RAM, Store in RAM
RTAR	Rotate ACC, Store in RAM
RTDR	Rotate D, Store in RAM
RTDY	Rotate D, Place on Y Bus
RTDA	Rotate D, Store in ACC
RTAY	Rotate ACC, Place on Y Bus
RTAA	Rotate ACC, Store in ACC

Rotate and Merge

MDAI	Merge Disjoint Bits of D and ACC Using I as Mask and Store in ACC
MDAR	Merge Disjoint Bits of D and ACC Using RAM as Mask and Store in ACC
MDRI	Merge Disjoint Bits of D and RAM Using I as Mask and Store in RAM
MDRA	Merge Disjoint Bits of D and RAM Using ACC as Mask and Store in RAM
MARI	Merge Disjoint Bits of ACC and RAM Using I as Mask and Store in RAM
MRAI	Merge Disjoint Bits of RAM and ACC Using I as Mask and Store in ACC

Rotate and Compare

CDAI	Compare Unmasked Bits of D and ACC Using I as Mask

CDRI	Compare Unmasked Bits of D and RAM Using I as Mask
CDRA	Compare Unmasked Bits of D and RAM Using ACC as Mask
CRAI	Compare Unmasked Bits of RAM and ACC Using I as Mask

Prioritize

PR1A	ACC as Destination for Prioritize Type 1
PR1Y	Y Bus as Destination for Prioritize Type 1
PR1R	RAM as Destination for Prioritize Type 1
PRT1A	ACC as Source for Prioritize Type 1
PR1D	D as Source for Prioritize Type 1
PR2A	ACC as Destination for Prioritize Type 2
PR2Y	Y Bus as Destination for Prioritize Type 2
PR3R	RAM as Source for Prioritize Type 3
PR3A	ACC as Source for Prioritize Type 3
PR3D	D as Source for Prioritize Type 3
PRTA	ACC as source for Prioritize Type Non-RAM
PRTD	D as Source for Prioritize Type Non-RAM
PRA	ACC as Mask for Prioritize Type 2, 3, and Non-RAM
PRZ	Mask Equal to Zero for Prioritize Type 2, 3, and Non-RAM
PRI	I as Mask for Prioritize Type 2, 3, and Non-RAM

OPCODE

Addition

ADD	Add without Carry
ADDC	Add with Carry
A2NA	Add 2^n to ACC
A2NR	Add 2^n to RAM
A2NDY	Add 2^n to D, Place on Y Bus

Subtraction

SUBR	Subtract R from S without Carry
SUBRC	Subtract R from S with Carry
SUBS	Subtract S from R without Carry
SUBSC	Subtract S from R with Carry
S2NR	Subtract 2^n from RAM
S2NA	Subtract 2^n from ACC
S2NDY	Subtract 2^n from D, Place on Y Bus

Logical Operations

AND	Boolean AND
NAND	Boolean NAND
EXOR	Boolean EXOR
NOR	Boolean NOR
OR	Boolean OR
EXNOR	Boolean EXNOR

SHIFTS

SHUPZ	Shift Up Towards MSB with 0 Insert
SHUP1	Shift Up Towards MSB with 1 Insert
SHUPL	Shift Up Towards MSB with LINK Insert

SHDNZ	Shift Down Towards LSB with 0 Insert
SHDN1	Shift Down Towards LSB with 1 Insert
SHDNL	Shift Down Towards LSB with LINK Insert
SHDNC	Shift Down Towards LSB with Carry Insert
SHDNOV	Shift Down Towards LSB with Sign EXOR Overflow Insert

Loads

LD2NR	Load 2^n into RAM
LDC2NR	Load $\overline{2^n}$ into RAM
LD2NA	Load 2^n into ACC
LDC2NA	Load $\overline{2^n}$ into ACC
LD2NY	Place 2^n on Y Bus
LDC2NY	Place $\overline{2^n}$ on Y Bus

Bit Oriented

SETNR	Set RAM, Bit n
SETNA	Set ACC, Bit n
SETND	Set D, Bit n
SONCZ	Set OVR, N, C, Z, in Status Register
SL	Set LINK Bit in Status Register
SF1	Set Flag1 Bit in Status Register
SF2	Set Flag2 Bit in Status Register
SF3	Set Flag3 Bit in Status Register
RSTNR	Reset RAM, Bit n
RSTNA	Reset ACC, Bit n
RSTND	Reset D, Bit n
RONCZ	Reset OVR, N, C, Z, in Status Register
RL	Reset LINK Bit in Status Register
RF1	Reset Flag1 Bit in Status Register
RF2	Reset Flag2 Bit in Status Register
RF3	Reset Flag3 Bit in Status Register
TSTNR	Test RAM, Bit n
TSTNA	Test ACC, Bit n
TSTND	Test D, Bit n

Arithmetic Operations

MOVE	Move and Update Status
COMP	Complement (1's Complement)
INC	Increment
NEG	Two's Complement

Conditional Test

TNOZ	Test $(N \oplus OVR) + Z$
TNO	Test $N \oplus OVR$
TZ	Test Zero Bit
TOVR	Test Overflow Bit
TLOW	Test for LOW
TC	Test Carry Bit
TZC	Test $Z + \overline{C}$
TN	Test Negative Bit
TL	Test LINK Bit
TF1	Test Flag1 Bit
TF2	Test Flag2 Bit
TF3	Test Flag3 Bit

APPLICATIONS

System Cycle Time Calculations

BD005952
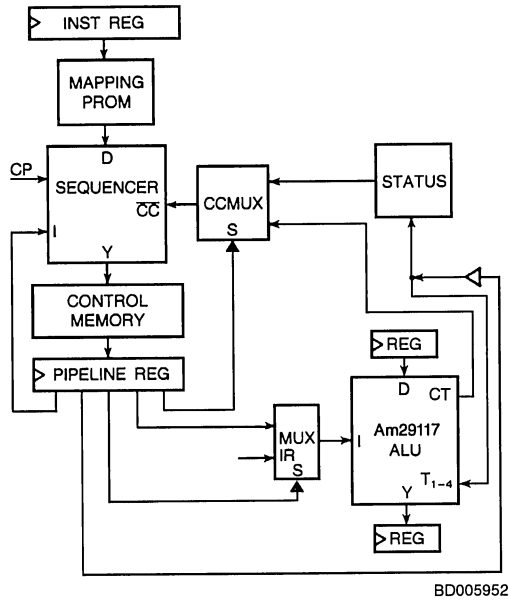
Figure 14. System Block Diagram

DATA PATH TIMING ANALYSIS

I. Without Any External Logic

a.
Pipeline Register	(29821)	CP–Q	12 ns
RALU	(29117)	$I–T_{1-4}$	68
Status Register	(29821)	Setup	4
		Cycle Time:	**84 ns**

b.
Pipeline Register	(29821)	CP–Q	12 ns
RALU	(29117)	I–Y	65
Data Register	(29821)	Setup	4
		Cycle Time:	**81 ns**

II. With Multiplexers for Address, N–Count, etc.

a.
Pipeline Register	(29821)	CP–Q	12 ns
Multiplexer	(F157)	Sel–Y	15
RALU	(29117)	$I–T_{1-4}$	68
Status Register	(29821)	Setup	4
		Cycle Time:	**99 ns**

b.
Pipeline Register	(29821)	CP–Q	12 ns
Multiplexer	(F157)	Sel–Y	15
RALU	(29117)	I–Y	65
Data Register	(29821)	Setup	4
		Cycle Time:	**96 ns**

III. Input/Output in One Cycle

a.
Pipeline Register	(29821)	CP–Q	12 ns
Decoder	(2924)	Sel–Y	12
Source Select	(29821)	OE–Y	15
RALU	(29117)	D–Y	41
Destination	(29821)	Setup	4
		Cycle Time:	**84 ns**

CONTROL PATH TIMING ANALYSIS

				Am2910A	Am29112 (est.)	Am29331 (est.)	Type
I.	**Pipeline Register**	(29821)					Branch Map
	Mapping PROM	(27S190A)					
	Register	(29821)	CP–Q	12 ns	12	12	
	Sequencer		D–Y	20	23*	19	
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
	Cycle Time:			76	79	75	
II.	**Pipeline Register**	(29821)	CP–Q	12	12	12	Branch
	Buffer Enable	(2959)	OE–Y	20	20	NA	
	Sequencer		I, D–Y	20	23**	20	
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
	Cycle Time:			96	99	76	
III.	**Pipeline Register**	(29821)	CP–Q	12	12	12	Conditional
	RALU	(29117)	I, T–CT	40	40	40	Branch
	CC–MUX	(2923)	D–W	7	7	NA	
	Polarity	(74S86)	D–Y	11	NA	NA	
	Sequencer		CC–Y	30	26	23	
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
	Cycle Time:			144	129	119	
IV.	**Pipeline Register**	(29821)	CP–Q	12	12	12	Conditional
	CC–MUX	(2923)	Sel–W	15	15	NA	Branch Using
	Polarity	(74S86)	D–Y	11	NA	NA	External Status
	Sequencer		CC–Y	30	26	23	Register
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
	Cycle Time:			112	97	79	
V.	**Pipeline Register**	(29821)	CP–Q	12	12	12	Instruction to
	Sequencer		I–Y	35	35*	20	Output Path
	Control Memory		t_{AA}	40	40	40	
	Pipeline Register	(29821)	Setup	4	4	4	
	Cycle Time:			91	91	76	
VI.	**Sequencer**		CP–Y	40	31	24	Clock to
	Control Memory		t_{AA}	40	40	40	Output Path
	Pipeline Register	(29821)	Setup	4	4	4	
	Cycle Time:			84	75	68	

* For the Am29112 Instruction 18 (Test SP with D (TSTSP.P)) is not used. If Instruction 18 is used D–Y is 35 ns and I–Y is 47 ns.
**For the Am29112 Relative Branch Instructions are not used. If the Relative Branch Instructions are used D–Y is 43 ns.

The Use of an External Status Register in Reducing Microcycle Length

The standard connection of the CT pin of the Am29117 and microcycle length calculation arising from that connection are shown below:

Critical Path Timing (Figure 15)

Part Number	Path	Maximum Commercial Delay (ns)
Pipeline Register	CP–Q	12
Am29117	I, T–CT	40
Am2923 CC–MUX	D–W	7
74S86 Polarity	D–Y	11
Am2910A	CC–Y	30
Control Memory	t_{AA}	40
Pipeline Register	Setup	4
		144

While 144 ns cycle time is quite fast, it can be improved by using an external register for status testing.

Critical Path Timing (Figure 16)

Part Number	Path	Maximum Commercial Delay (ns)
Am29821 Status Reg	CP–Y	12
Am2923 CC–MUX	Sel–W	15
74S86 Polarity	D–Y	11
Am2910A	CC–Y	30
Control Memory	t_{AA}	40
Pipeline Register	Setup	4
		112

The cycle time has been reduced from 144 ns to 112 ns.

BD005962

Figure 15.

BD005972
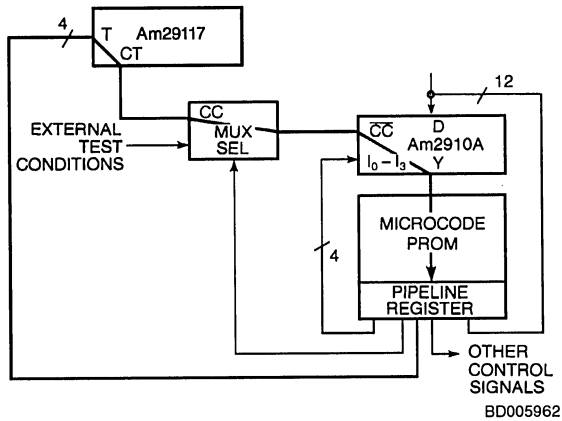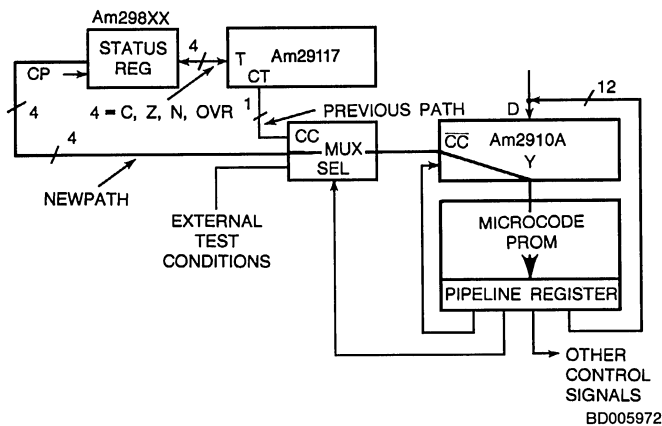
Figure 16.

Suggestions for Power and Ground Pin Connections

The Am29117 operates in an environment of fast signal rise times and substantial switching currents. Therefore, care must be exercised during circuit board design and layout, as with any high-performance component. The following is a suggested layout, but since systems vary widely in electrical configuration, an empirical evaluation of the intended layout is recommended.

The V_T pin, which carries output driver switching currents, tends to be electrically noisy. The V_E pins, which supply the ECL core of the device, tend to produce less noise, and the circuits they supply may be adversely affected by noise spikes on the V_{CC} plane. For this reason, it is best to provide isolation between the V_T and V_E pins, as well as independent decoupling for each; isolating the GND pins is not required.

Printed Circuit Board Layout Suggestions

1. Use of a multilayer PC board with separate V_{CC}, GND, and signal planes is highly recommended.

2. The V_T and V_E pins should be connected to the V_{CC} plane. The V_T pin should be isolated from the V_E pins by means of a slot cut in the V_{CC} plane (see suggested layout diagram that follows). By physically separating the V_T and V_E pins, coupled noise will be reduced.

3. All GND pins should be connected directly to the ground plane.

4. The V_T pin should be decoupled to ground with a 0.1-μF ceramic capacitor and a 10-μF electrolytic capacitor, placed as closely to the Am29117 as is practical. The V_E pins should be decoupled to ground in a similar manner.

A suggested layout is shown in Figure 17:

Bottom View

= V_{CC} Plane Connection

= Through Hole

$C_1 = C_3 = 0.1\,\mu F$

$C_2 = C_4 = 10\,\mu F$
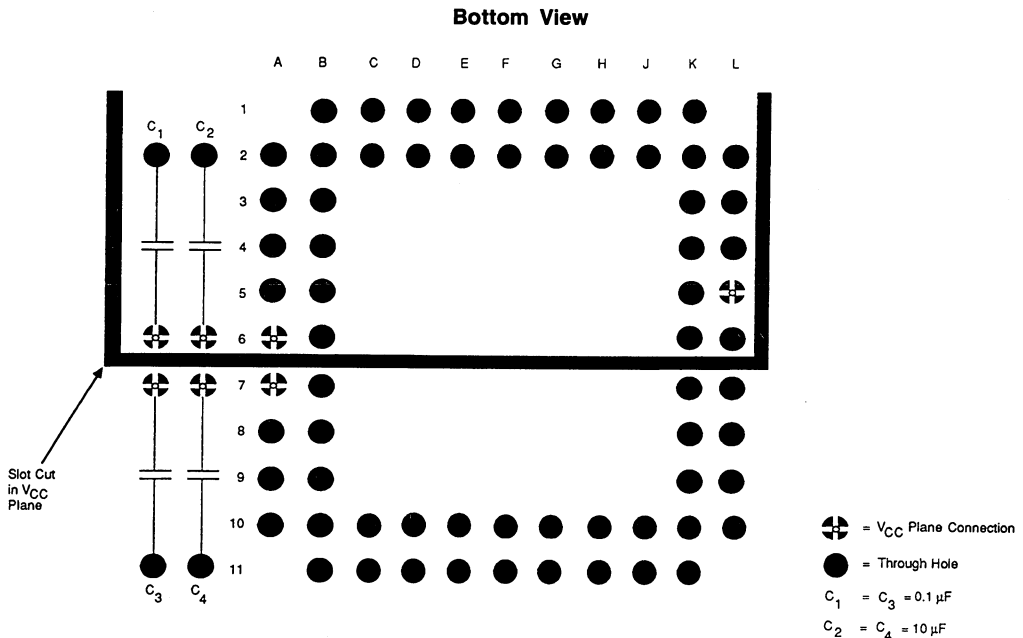
CD010600

Figure 17. Suggested PC Board Layout

Parameters, θ_{JA}	°C/W
No Airflow	23
200 LFM	8.5
600 LFM	7.0

Y-axis: THERMAL RESISTANCE, θ_{JA} (°C/W)

X-axis: AIR VELOCITY (LINEAR FEET PER MINUTE)
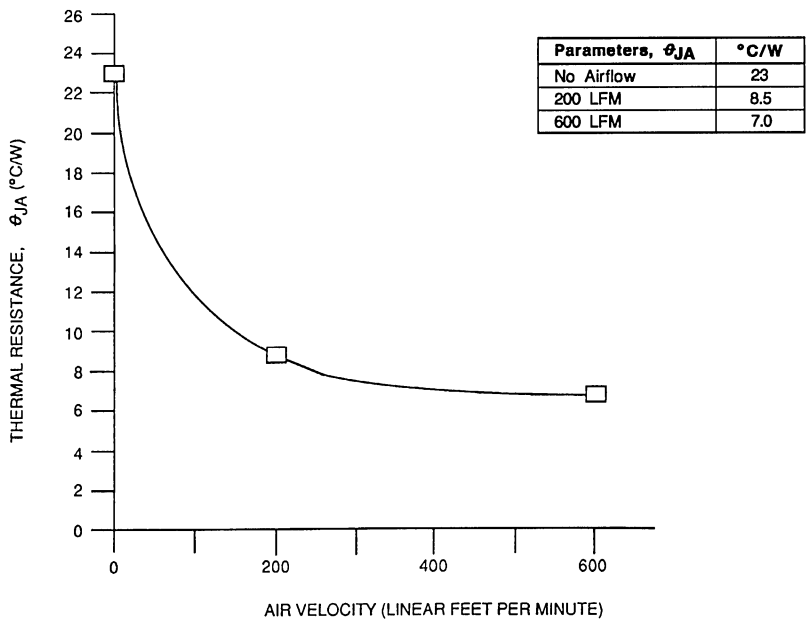
OP002271

Figure 18. Thermal Characteristics (Typical)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Case Temperature Under Bias (T_C) ..... −55 to +125°C
Supply Voltage to Ground Potential .. −0.5 V to +7.0 V
DC Voltage Applied to Outputs For
  High Output State .... −0.5 V to +V_{CC} Max.
DC Input Voltage .... −0.5 V to +5.5 V
DC Output Current, Into Outputs .... 30 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Temperature (T_C) .... 0 to +85°C
  Supply Voltage (V_{CC}) .... +4.75 V to +5.25 V

Military (M) Devices
  Temperature (T_C) .... −55 to +125°C
  Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for CPL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameters	Description	Test Conditions (Note 1)			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	Y_{0-15} T_{1-4} CT	$I_{OH} = -1.6$ mA (COM'L) $I_{OH} = -1.2$ mA (MIL)	2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	Y_{0-15} T_{1-4} CT	$I_{OL} = 16$ mA (COM'L) $I_{OL} = 12$ mA (MIL)		0.5	Volts
V_{IH}	Guaranteed Input Logical HIGH Voltage (Note 5)		All Inputs		2.0		Volts
V_{IL}	Guaranteed Input Logical LOW Voltage (Note 5)		All Inputs			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min.	All Inputs	$I_{IN} = -18$ mA		−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = Max. $V_{IN} = 0.5$ Volts (Note 3)	IEN SRE DLE I_{0-4} I_{5-15} OE_T $\overline{OE}_Y$ CP T_{1-4} D_{0-15}			−0.50 −0.50 −1.00 −1.00 −0.50 −0.50 −0.50 −1.50 −0.55 −0.50	mA
I_{IH}	Input HIGH Current	V_{CC} = Max. $V_{IN} = 2.4$ Volts (Note 3)	IEN SRE DLE I_{0-4} I_{5-15} OE_T $\overline{OE}_Y$ CP T_{1-4} D_{0-15}			50 50 100 100 50 50 50 150 100 50	µA
I_I	Input HIGH Current	V_{CC} = Max. $V_{IN} = 5.5$ Volts	All Inputs			1.0	mA
I_{OZH}	Off State (HIGH Impedance) Output Current	V_{CC} = Max. V_O = 2.4 Volts (Note 3)	T_{1-4} (Note 3) Y_{0-15}			100 50	µA
I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = Max. V_O = 0.5 Volts (Note 4)	T_{1-4} (Note 3) Y_{0-15}			−550 −50	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max. + 0.5 Volts V_O = 0.5 Volts (Note 2)			−30	−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = Max.	COM'L	T_C = 0 to +85°C (Note 6)		735	mA
				T_C = +85°C		605	
			MIL	T_C = −55 to +125°C (Note 6)		745	
				T_C = +125°C		525	

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
3. Y_{0-15}, T_{1-4} are three-state outputs internally connected to TTL inputs. Input characteristics are measured under conditions such that the outputs are in the OFF state.
4. Worst case I_{CC} is at minimum temperature.
5. These input levels provide zero noise immunity and should be tested only in a static, noise-free environment.
6. Cold start.
7. It is the responsibility of the user to maintain a case temperature of +85°C or less. AMD recommends an airflow of at least 200 linear feet per minute over the heatsink.

SWITCHING CHARACTERISTICS over Commercial Operating Range unless otherwise specified

($T_C = 0$ to $+85°C$ Case, $V_{CC} = 4.75$ to 5.25 V, $C_L = 50$ pF)

A. Combinational Delays (nsec)

Input		Outputs		
		Y_{0-15}	T_{1-4}	CT
	I_{0-4} (ADDR)	65	68	–
	I_{0-15} (DATA)	65	68	–
	I_{0-15} (INSTR)	65	68	40
Input	DLE	44	46	–
	T_{1-4}	–	–	25
	CP	43	42	23
	D_{0-15}	41	41	–
	$\overline{IEN}$	–	–	30

B. Enable/Disable Times (nsec)
(Disable: $C_L = 5$ pF, 0.5-V Change on Outputs)

From Input	To Output	Enable		Disable	
		t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	20	20	20	20
OE_T	T_{1-4}	25	25	25	25

C. Clock and Pulse Requirements (nsec)

Input	Min LOW Time	Min HIGH Time
CP	16	18
DLE	–	15
$\overline{IEN}$	20	–

D. Setup and Hold Times (nsec)

Input	With Respect to	HIGH-to-LOW Transition Setup	HIGH-to-LOW Transition Hold	LOW-to-HIGH Transition Setup	LOW-to-HIGH Transition Hold	Comment
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 14	(t_{h1}) 0	–	–	Single ADDR (Source)
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 5	Do Not Change		(t_{h7}) 1	Two ADDR (Destination)
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 54	(t_{h8}) 1	
I_{0-15} (INSTR)	CP	(t_{s3}) 32*	(t_{h3}) 13*	(t_{s9}) 54	(t_{h9}) 4	
I_{0-15} (INSTR)	$\overline{IEN}$ ⌐	(t_{s16}) 0	(t_{h16}) 20	–	–	Two ADDR Immediate First Cycle
$\overline{IEN}$ ⌠	CP ⌐	–	–	(t_{s15}) 20	(t_{h15}) 0	Disable Immediate
$\overline{IEN}$ HIGH	CP	(t_{s4}) 4	–	–	(t_{h10}) 1	Disable Write
$\overline{IEN}$ LOW	CP	–	–	–	–	(t_{s11}) 22	(t_{s5}) 18	(t_{h11}) 0**	(t_{h5}) 8*	Enable Write	Immediate First Cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 13	(t_{h12}) 0	
D	CP	–	–	(t_{s13}) 34	(t_{h13}) 0	
D	DLE	(t_{s6}) 11	(t_{h6}) 5	–	–	
DLE	CP	–	–	(t_{s14}) 38	(t_{h14}) 0	

*Timing for immediate instruction for first cycle.
**Status register and accumulator destination only.

SWITCHING CHARACTERISTICS over Military Operating Range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

($T_C = -55$ to $+125°C$, $V_{CC} = 4.5$ to 5.5 V, $C_L = 50$ pF)

A. Combinational Delays (nsec)

		Outputs		
		Y_{0-15}	T_{1-4}	CT
Input	I_{0-4} (ADDR)	76	78	–
	I_{0-15} (DATA)	76	78	–
	I_{0-15} (INSTR)	76	78	44
	DLE	47	49	–
	T_{1-4}	–	–	29
	CP	52	48	27
	D_{0-15}	47	46	–
	$\overline{IEN}$	–	–	34

B. Enable/Disable Times (nsec)
(Disable: $C_L = 5$ pF, 0.5-V Change on Outputs)

		Enable		Disable	
From Input	To Output	t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	25	25	25	25
OE_T	T_{1-4}	30	30	30	30

C. Clock and Pulse Requirements (nsec)

Input	Min LOW Time	Min HIGH Time
CP	21	19
DLE	–	15
$\overline{IEN}$	23	–

D. Setup and Hold Times (nsec)

Input	With Respect to	HIGH-to-LOW Transition Setup	Hold	LOW-to-HIGH Transition Setup	Hold	Comment	
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 16	(t_{h1}) 0	–	–	Single ADDR (Source)	
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 7	–	–	(t_{h7}) 2	Two ADDR (Destination)	
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 61	(t_{h8}) 2		
I_{0-15} (INSTR)	CP	(t_{s3}) 35*	(t_{h3}) 15*	(t_{s9}) 61	(t_{h9}) 5		
I_{0-15} (INSTR)	$\overline{IEN}$	(t_{s16}) 2	(t_{h16}) 22	–	–	Two ADDR Immediate First Cycle	
$\overline{IEN}$ HIGH	CP	–	–	(t_{s15}) 22	(t_{h15}) 1	Disable Immediate	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 6	–	–	(t_{h10}) 1	Disable	
$\overline{IEN}$ LOW	CP	–	(t_{s5}) 19	–	(t_{h5}) 1*	(t_{s11}) 24	–	(t_{h11}) 1**	–	Enable	Immediate First Cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 15	(t_{h12}) 0		
D	CP	–	–	(t_{s13}) 36	(t_{h13}) 1		
D	DLE	(t_{s6}) 12	(t_{h6}) 6	–	–		
DLE	CP	–	–	(t_{s14}) 39	(t_{h14}) 0		

*Timing for immediate instruction for first cycle.
**Status register and accumulator destination only.

Test Philosophy and Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic testing environment. The specifics of what philosophies are applied to which test are shown in the data sheet and the data-sheet reconciliation that follow.

Capacitive Loading for AC Testing

Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters that call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" that measure the propagation delays in to and out of the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench setup are used to determine the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impractical to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is determined from engineering correlations based on data taken with a bench setup and the knowledge that certain DC tests are performed in order to facilitate this correlation.

AC loads specified in the data sheet are used for bench testing. Automatic tester loads, which simulate the data-sheet loads, may be used during production testing.

Threshold Testing

The noise associated with automatic testing, the long inductive cables, and the high gain of bipolar devices frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels.

AC Testing

AC parameters are specified that cannot be measured accurately on automatic testers because of tester limitations. Data-input hold times fall into this category. In these cases, the parameter in question is tested by correlating the tester to bench data or oscilloscope measurements made on the tester by engineering (supporting data on file).

Certain AC tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.

### Output Short-Circuit Current Testing

When performing I_{OS} tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{output}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the $V_{OUT} = 0$, $V_{CC} = $ Max. case.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

| WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▧	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
◇	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010
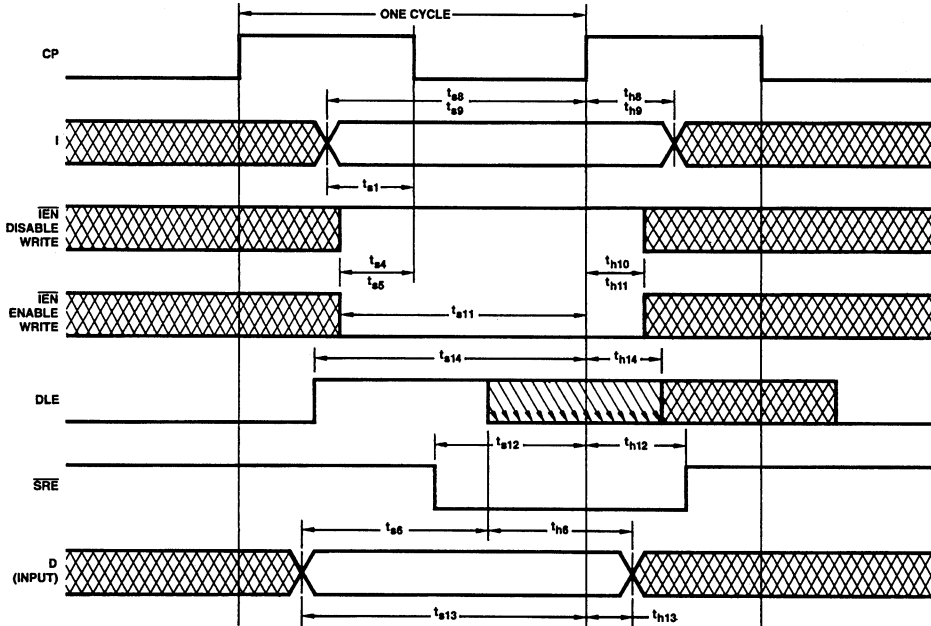
WF002561

Single Address Access Timing

If t_{h6} is satisfied, t_{h13} need not be satisfied.

SWITCHING WAVEFORMS (Cont'd.)
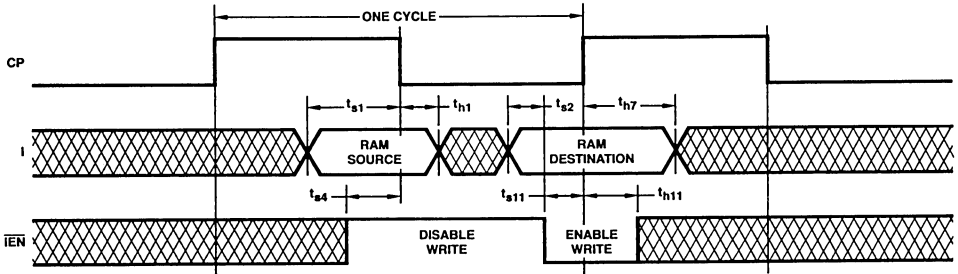
Double Address Access Timing
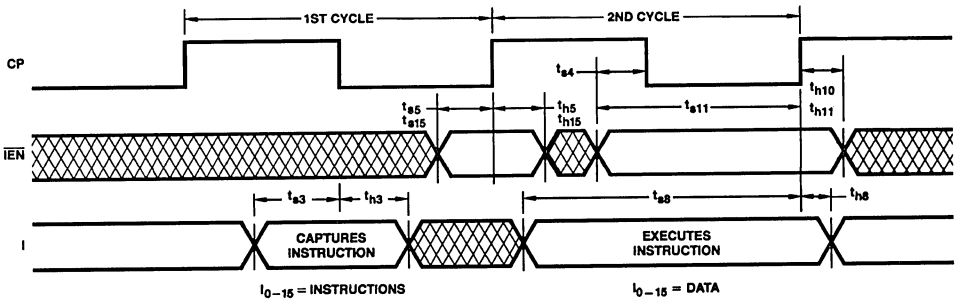
WF002540

One-Address Immediate Instruction Cycle Timing
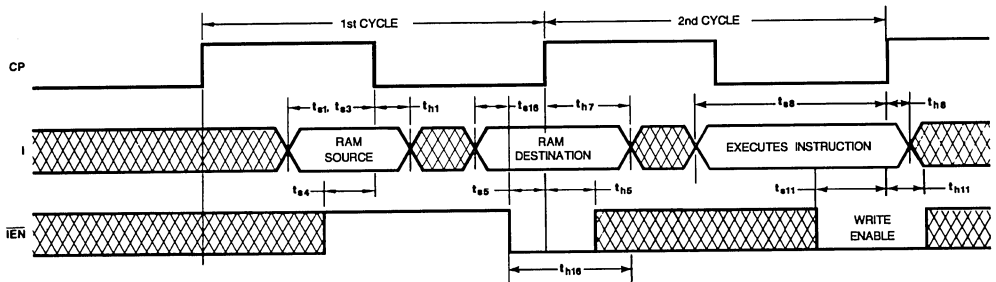
WF002552

Two-Address Immediate Instruction Timing

WF002544

SWITCHING TEST CIRCUITS
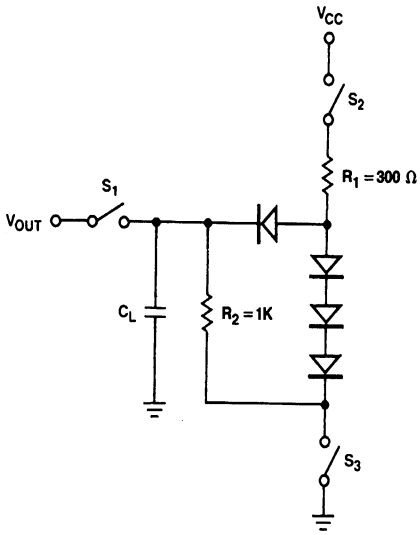
TCR01331

A. Three-State Outputs

$R_1 = 300 \ \Omega$

TCR01341

B. Normal Outputs

$R_1 = 300 \ \Omega$
$R_2 = 3.0 \ k\Omega$

Notes: 1. $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. $C_L = 5.0$ pF for output disable tests.
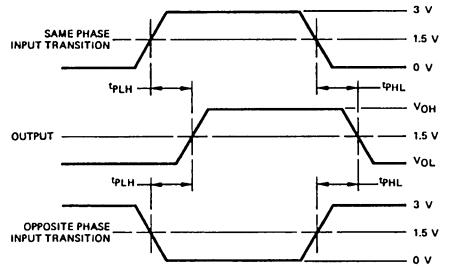
SWITCHING TEST WAVEFORMS

WFR02970
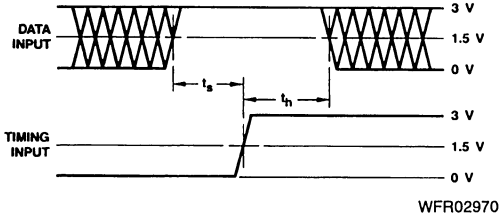
Set-up, Hold, and Release Times

Notes: 1. Diagram shown for HIGH data only.
Output transition may be opposite sense.
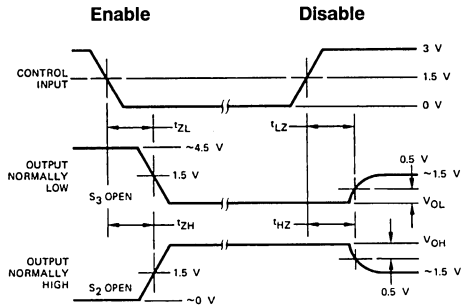2. Cross hatched area is don't care condition.

WFR02790
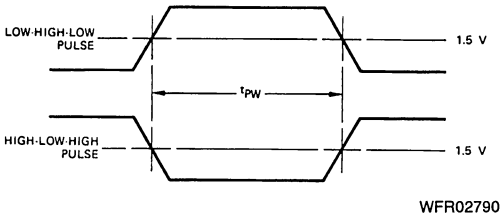
Pulse Width

Note: 1. Pulse generator for all pulses Rate ⩽ 1.0 MHz;
$Z_O = 50$ Ω; t_r ⩽ 2.5 ns; t_f ⩽ 2.5 ns.

WFR02980

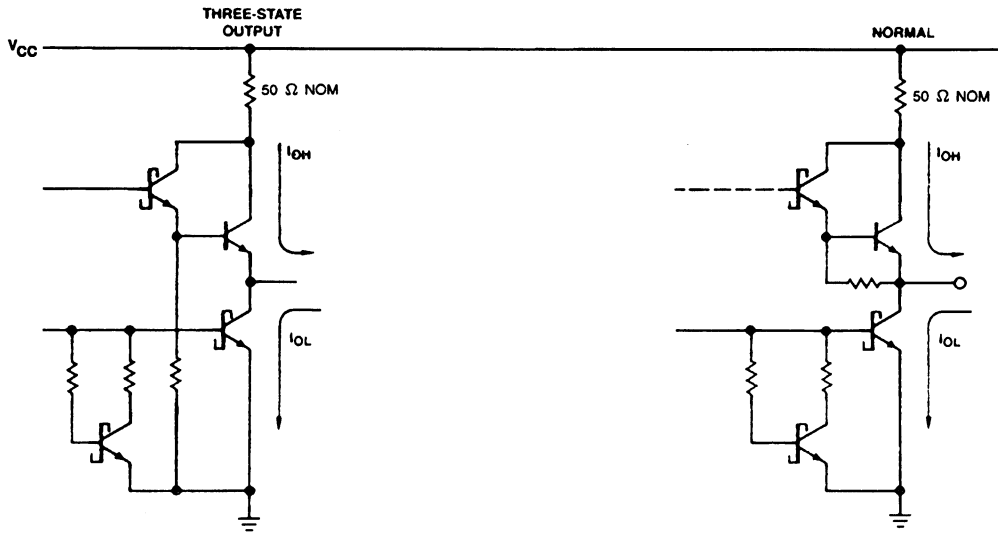## Propagation Delay

WFR02660

Enable and Disable Times

Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH
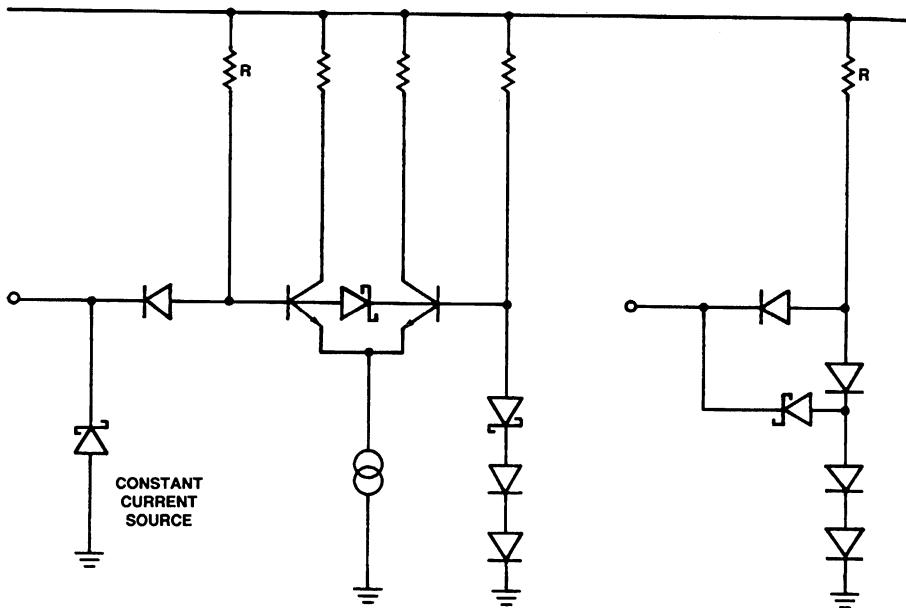2. S_1, S_2 and S_3 of Load Circuit are closed except where shown.

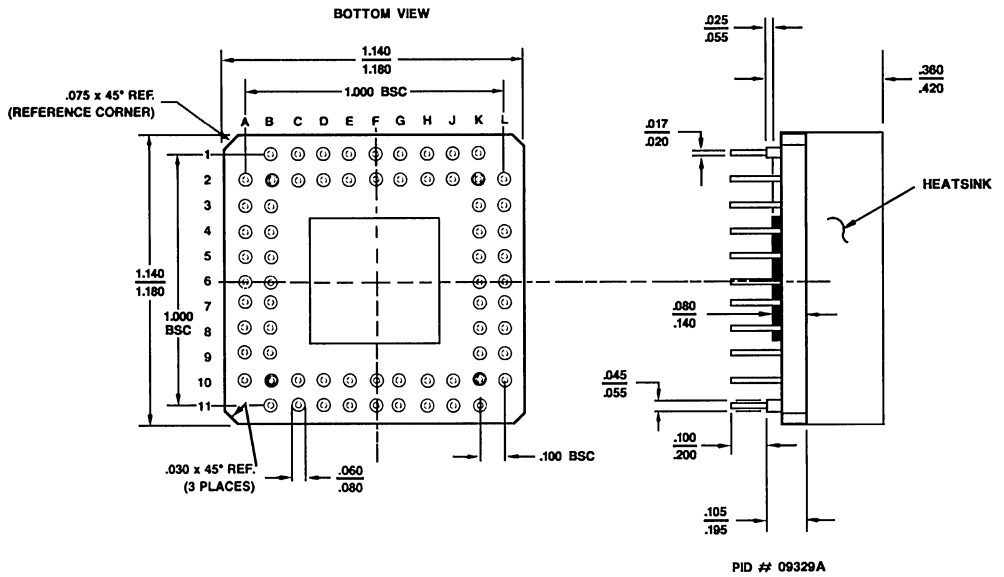# INPUT/OUTPUT CURRENT INTERFACE

TTL

ICR00523

$C_O \cong 5.0$ pF, all outputs

ICR00531

PHYSICAL DIMENSIONS*

CG 068

BOTTOM VIEW

.075 x 45° REF.
(REFERENCE CORNER)

1.140
1.180

1.000 BSC

A B C D E F G H J K L

1.140
1.180

1.000
BSC

.030 x 45° REF.
(3 PLACES)

.060
.080

.100 BSC

.025
.055

.360
.420

.017
.020

HEATSINK

.080
.140

.045
.055

.100
.200

.105
.195

PID # 09329A

*For reference only.

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