Am29C516A/Am29C517A

16 x 16-Bit CMOS Parallel Multipliers

DISTINCTIVE CHARACTERISTICS

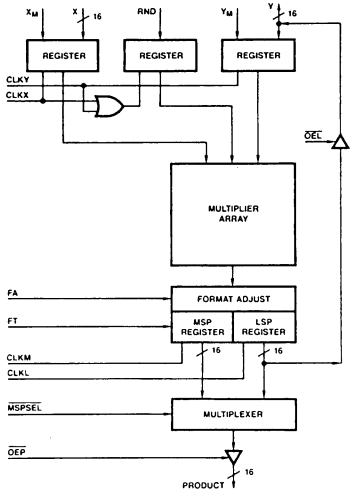
- 45-ns Clocked Multiply (Am29C516A/Am29C517A)
- 35-ns Clocked Mulitply (Am29C516A-1/Am29C517A-1)
- Low-power 1.2 micron CMOS technology
- 16 x 16-Bit Parallel Multiplier with 32-Bit output
- Full product multiplexed at output
- Two's-complement, unsigned, or mixed operands
- Output register may be made transparent
- Am29C516A pin and functionally compatible with CY7C516, WTL1516, IDT7216, MPY016, and Am29516
- TTL I/O and single +5-V supply
- Available in 64-pin plastic or ceramic DIPs, and 68-pin ceramic leadless or plastic leaded chip carriers

GENERAL DESCRIPTION

The Am29C516A/Am29C517A are high-speed, low-power, industry-standard 16 x 16-bit parallel multipliers. They are widely used in array-processing and DSP applications. The 35-ns speed and 150-mW power dissipation provide fast multiplication and power savings. The Am29C516A has independent register clocks (CLKX, CLKY, CLKM, CLKL), whereas the Am29C517A has a single clock and three register enables for use with microprogrammed systems. Applications for the Am29C516A/Am29C517A include digital filtering, graphics, speech recognition, radar, accelerators, FFT, and floating-point processors.

BLOCK DIAGRAMS

Am29C516A



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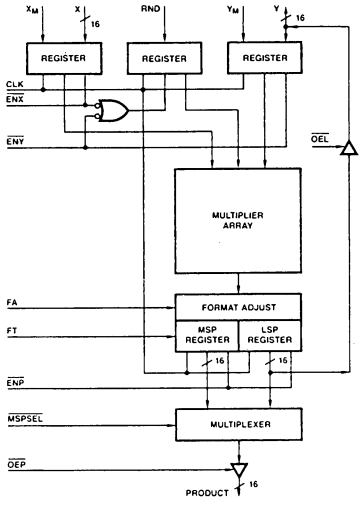
Am29C517A



BD002850

Publication # 09130 | Rev. B | Amendment /0
Issue Date: February 1988

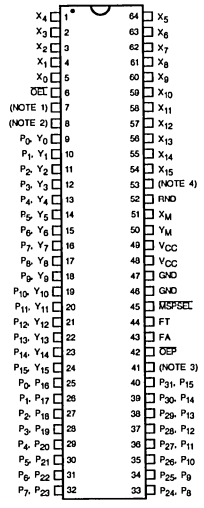
RELATED AMD PRODUCTS

Part No.	Description
Am29C10A	CMOS Microprogram Sequencer
Am29C101	16-Bit CMOS Microprocessor Slice
Am29C116/C116-2	16-Bit CMOS Microprocessor
Am29PL141	Fuse-Programmable Controller
Am29325	32-Bit Floating-Point Processor
Am29C325	32-Bit CMOS Floating-Point Processor
Am29501A	Multiport 8-Bit Expandable Pipelined Processor
Am29C509	12 x 12 CMOS Multiplier Accumulator
Am29C520/C521	4 x 8 CMOS Pipeline Registers
Am29525	Dual 8-Deep Pipeline Register (All 16 Registers Available at Output)
Am29526	IMOX* Sine Generator (MSB)
Am29527	IMOX Sine Generator (LSB)
Am29528	IMOX Cosine Generator (MSB)
Am29529	IMOX Cosine Generator (LSB)
Am29540	FFT Address Generator

IMOX is a trademark of Advanced Micro Devices, Inc.

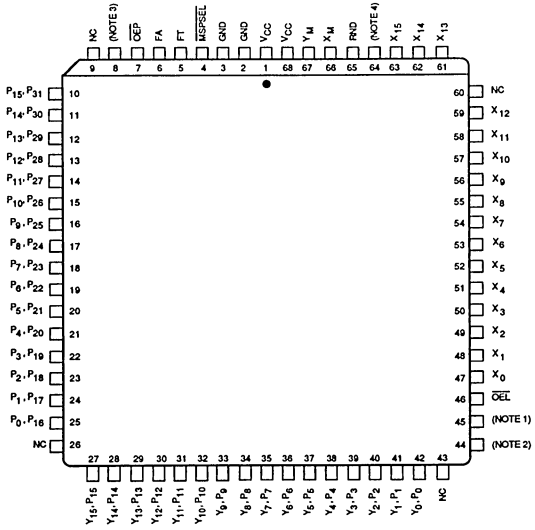
CONNECTION DIAGRAMS
Top View

DIPs



CD010620

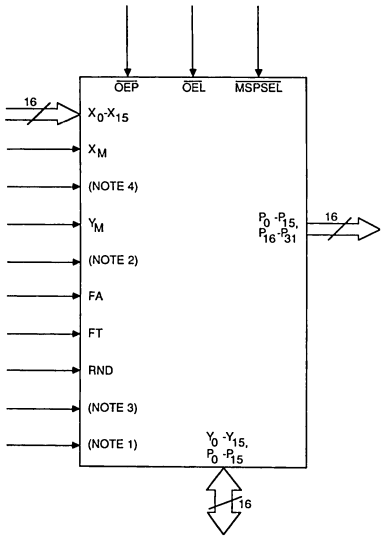
PLCC



CD011220

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



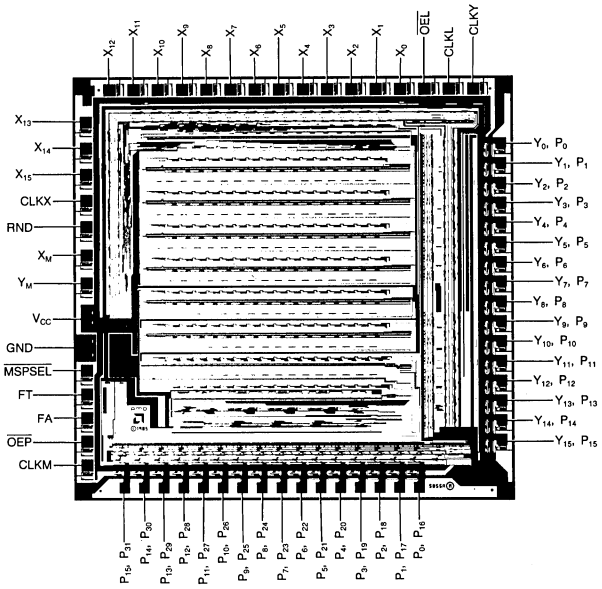
LS003000

Notes:

	Am29C516A	Am29C517A
1	CLKL	CLK
2	CLKY	$\overline{ENY}$
3	CLKM	$\overline{ENP}$
4	CLKX	$\overline{ENX}$

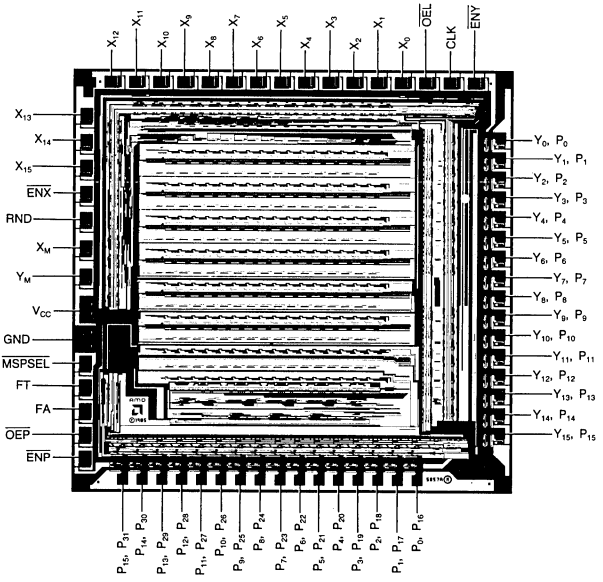
METALLIZATION AND PAD LAYOUT

Am29C516A



Die Size: 256 x 253 Mils
Approx. Gate Count: 7300

Am29C517A

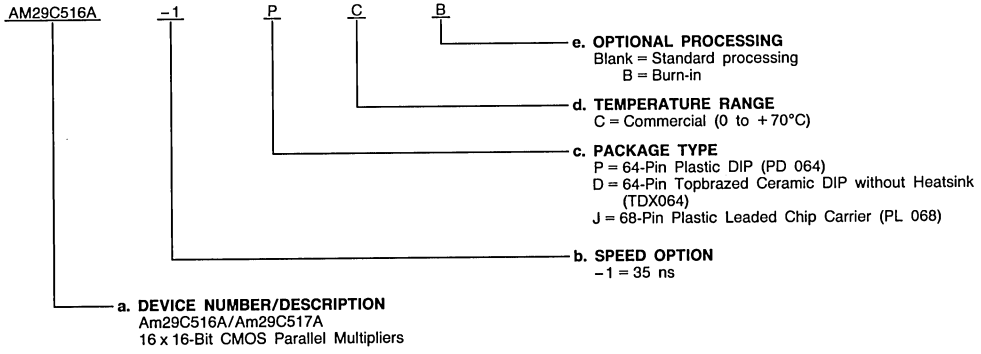


Die Size: 256 x 253 Mils
Approx. Gate Count: 7300

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C516A	PC, PCB, DC, DCB, JC
AM29C517A	
AM29C516A-1	PC, DC, JC
AM29C517A-1	

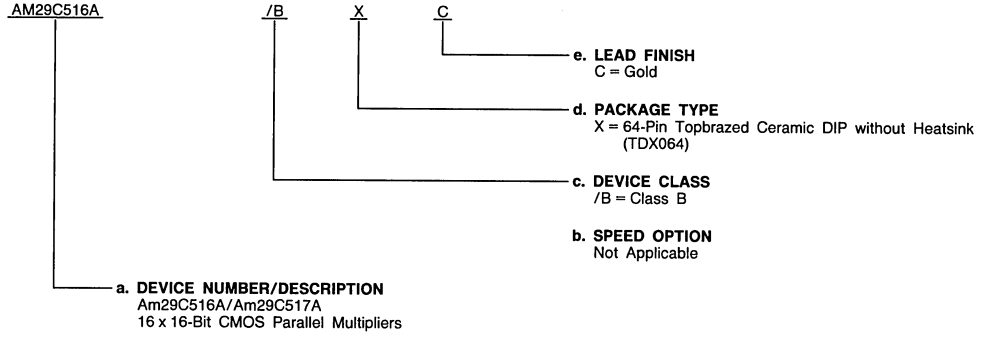
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C516A	BXC
AM29C517A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

FA (RS*) Format Adjust (Input; Active HIGH)
Format Adjust control selects either a full 32-bit product (HIGH) or a left-shifted 31-bit product with the sign bit replicated in the Least Significant Product (LSP) (LOW). This control is normally HIGH, except for certain fractional two's-complement applications (see Multiplier output formats table).

FT Feedthrough (Input; Active HIGH)
Feedthrough control (HIGH) makes both MSP and LSP registers transparent.

$\overline{\text{MSPSEL}}$ Product Select (Input; Active LOW)
Selects either MSP (LOW) or LSP (HIGH) to be available at the product output port.

$\overline{\text{OEL}}$ (TRIL*) Output Enable LSP (Input; Active LOW)
Three-state enable for routing LSP through Y input/output port.

$\overline{\text{OEP}}$ (TRIM*) Output Enable Product (Input; Active LOW)
Three-state enable for product output port.

$P_0 - P_{15}$ Data (Output)
LSP product port when $\overline{\text{MSPSEL}}$ is HIGH.

$P_{16} - P_{31}$ Data (Output)
MSP product port when $\overline{\text{MSPSEL}}$ is LOW.

RND Round Control (Input; Active HIGH)
Control for rounding the MSP. Adds a binary one to the most-significant bit of the LSP for two's-complement and unsigned numbers. Format adjust occurs before rounding.

$X_0 - X_{15}$ Data (Input)
Multiplicand data inputs.

X_M, Y_M, (TCX, TCY*) Mode Control (Input)
Mode control inputs for each data word; LOW for unsigned data and HIGH for two's-complement data.

$Y_0 - Y_{15}$ Data (Input/Output)
Multiplier data inputs or LSP output.

Am29C516A Only

CLKL LSP Register Clock (Input)

CLKM MSP Register Clock (Input)

CLKX Register Clock, $X_0 - X_{15}$, RND (Input)

CLKY Register Clock, $Y_0 - Y_{15}$, RND (Input)

Am29C517A Only

CLK Clock, All Registers (Input)

$\overline{\text{ENP}}$ Data (Input; Active LOW)
Register Enable MSP, LSP.

$\overline{\text{ENX}}$ Data (Input; Active LOW)
Register Enable $X_0 - X_{15}$, X_M, RND.

$\overline{\text{ENY}}$ Data (Input; Active LOW)
Register Enable, $Y_0 - Y_{15}$, Y_M, RND.

*TRW MPY 16HJ pin designation.

FUNCTIONAL DESCRIPTION

The Am29C516A and Am29C517A are high-speed parallel 16 x 16-bit CMOS multipliers that generate a 32-bit product. Two 17-bit input registers are provided for the X and Y operands and their associated mode controls, X_M and Y_M. These mode controls are used to specify each operand as either two's-complement or unsigned numbers. When one operand is two's complement and the other is unsigned, the product will be two's complement.

Two 16-bit output registers are provided to hold the most- and least-significant halves of the product (MSP and LSP). For asynchronous operation, these registers may be made transparent by taking the Feedthrough (FT) control HIGH.

The two halves of the product may be routed to a 16-bit output port (P) via a multiplexer. The multiplexer control ($\overline{MSPSEL}$) uses a pin which is a supply ground in the TRW MPY16HJ. When this control is LOW, the MSP appears on the P port, thus allowing full compatibility with the MPY16HJ. When this control is HIGH, the LSP appears on the P port. In addition, the LSP is connected to the bidirectional Y port through a separate three-state buffer controlled by $\overline{OEL}$.

In two's-complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. In fractional notation, however, a problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude; however, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit. The Am29C516A/Am29C517A has a Format Adjust (FA) control that permits shifting of the result to provide a correct answer for every two's-complement multiplication. When FA is LOW, the value of the MSP is doubled (i.e., shifted left one bit), which provides the capability of representing the largest possible product. The effects of this control are illustrated in the Format tables. Note that for unsigned-magnitude operation, the FA control must be HIGH.

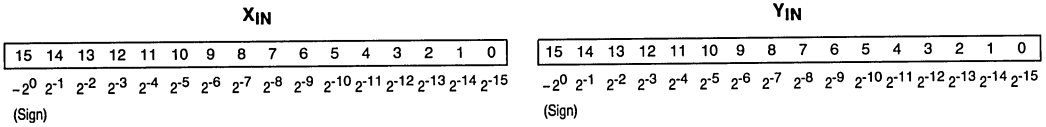
A Round control (RND) allows rounding of the MSP by adding a 1 to the MSB of the LSP. This control is registered, and is entered whenever either input register is clocked. Format Adjust takes place on a product before it is rounded.

The Am29C516A X, Y, MSP, and LSP registers have independent clocks (CLKX, CLKY, CLKM, CLKL). The Am29C517A differs in that it has a single clock input (CLK) and three register enables ($\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$) for the two input registers and the entire product, respectively. This facilitates the use of the part in microprogrammed systems. In both parts, data is entered into the registers on the positive edge of the clock.

INPUT FORMATS (All Devices)

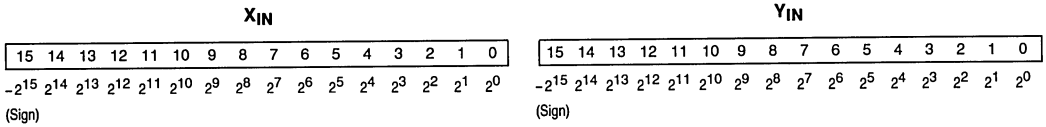
Fractional Two's-Complement Input Format

X_M, $Y_M = 1$



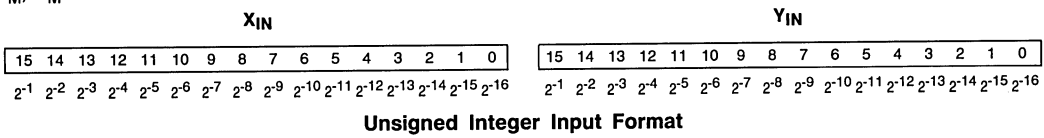
Integer Two's-Complement Input Format

X_M, $Y_M = 1$



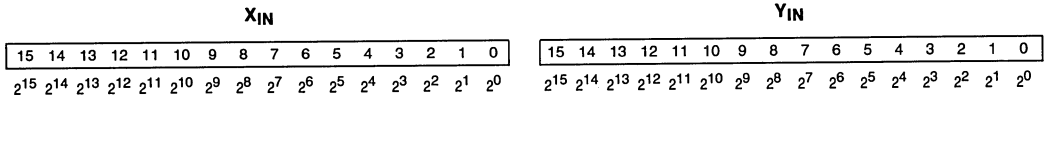
Unsigned Fractional Input Format

X_M, $Y_M = 0$



Unsigned Integer Input Format

X_M, $Y_M = 0$



OUTPUT FORMATS
(All Devices)

Fractional Two's-Complement (Shifted)* Output

FA = 0

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
(Sign)															

Fractional Two's-Complement Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}
(Sign)															

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

Integer Two's-Complement Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
(Sign)															

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

*In this format an overflow occurs in the attemped multiplication of the two's complement number 1.000...(−1) with itself, yielding a product of 1.000... or −1.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature under Bias (T_C) ..... −55 to +125°C
Supply Voltage to Ground Potential Continuous ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs For High Output State ..... −0.3 to +V_{CC} +0.3 V
DC Input Voltage ..... −0.3 to +V_{CC} +0.3 V
DC Output Current, Into LOW Outputs ..... 30 mA
DC Input Current ..... −10 to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Military* (M) Devices
Ambient Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_A = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −0.4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4 mA		0.5	V
V_{IH}	Guaranteed Input Logical-HIGH Voltage (Note 2)			2.0		V
V_{IL}	Guaranteed Input Logical-LOW Voltage (Note 2)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5 V			−10	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.4 V			10	μA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.4 V		10	μA
I_{OZL}			V_O = 0.5 V		−10	
I_{CC}	Static Power-Supply Current	V_{CC} = Max., V_{IN} = V_{CC} or GND, I_O = 0 μA	TTL V_{IN} = V_{OL} or V_{OH}		30	mA
			CMOS V_{IN} = V_{CC} or GND		15	
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = 5.0 V, T_A = +25°C, No Load		950 pF Typical		

Notes:
1. V_{CC} conditions shown as Min. or Max. refer to the commercial (±10%) V_{CC} limits.
2. These input levels provide zero noise immunity and should only be statically tested in a noise-free environment (not functionally tested).
3. C_{PD} determines the no-load dynamic current consumption: I_{CC} (Total) = I_{CC} (Static) + C_{PD} V_{CC} f, where f is the switching frequency of the majority of the internal nodes, normally one-half of the clock frequency.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 1)

Parameter Symbol	Parameter Description		Test Conditions	COM'L				MIL		Unit
				29C516A/ 29C517A		29C516A-1/ 29C517A-1		29C516A/ 29C517A		
				Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time		Load 1		55		49		70	ns
t_{MC}	Clocked Multiply Time				45		35		50	ns
t_S	X_i, Y_i, RND Setup Time			12		12		15		ns
t_H	X_i, Y_i, Hold Time			0		0		0		ns
	RND Hold Time			0		0		0		
t_{PWH}	Clock Pulse Width HIGH			15		15		15		ns
t_{PWL}	Clock Pulse Width LOW			15		15		15		ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out				18		17		25	ns
t_{PDP}	Output Clock to P				20		19		25	ns
t_{PDY}	Output Clock to Y				22		21		25	ns
t_{PHZ}	$\overline{OEP}$ Disable Time	HIGH to Z	Load 2		20		20		25	ns
t_{PLZ}		LOW to Z			20		20		25	ns
t_{PZH}	$\overline{OEP}$ Enable Time	Z to HIGH			21		21		25	ns
t_{PZL}		Z to LOW			21		21		25	ns
t_{PHZ}	$\overline{OEL}$ Disable Time	HIGH to Z			20		20		25	ns
t_{PLZ}		LOW to Z			20		20		25	ns
t_{PZH}	$\overline{OEL}$ Enable Time	Z to HIGH			25		25		27	ns
t_{PZL}		Z to LOW			25		25		27	ns
t_S	Clock Enable Setup Time (Am29C517A Only)		Load 1	15		15		20		ns
t_H	Clock Enable Hold Time (Am29C517A Only)			0		0		0		ns
t_{HCL}	Clock LOW Hold Time CLKXY Relative to CLKML (Am29C516A Only)			0		0		0		ns

Notes: 1. To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

Test Philosophy and Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic environment. The specifics of what philosophies applied to which test are shown in the data sheet.

1. Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily. Current level may vary from product to product.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins that may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3.0$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Capacitive Loading for AC Testing

   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another but is generally around 50 pF. This makes it impossible to make direct measurements of parameters that call for a smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench set up are used to predict the result at the lower capacitance.

   Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench setup and the knowledge that certain DC measurements (I_{OH}, I_{OL}, for example) have already been taken and are within specification. In some cases, special DC tests are performed in order to facilitate this correlation.
7. Threshold Testing

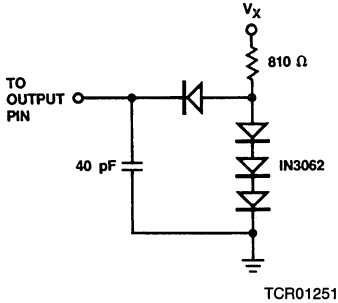
   The noise associated with automatic testing (due to the long inductive cables), and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.
8. AC Testing

   Occasionally parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer using data from precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

   In some cases, certain AC tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.
9. Output Short-Circuit Current Testing

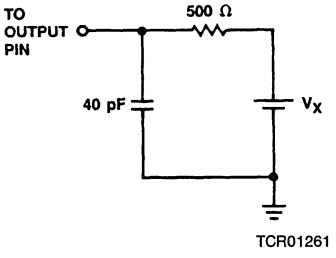
   When performing I_{OS} tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. To avoid this effect, it is common to make the measurement at a voltage (V_{output}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the $V_{OUT} = 0$, V_{CC} = Max. case.

SWITCHING TEST CIRCUITS



TCR01251

A. Normal Load (Load 1)



TCR01261

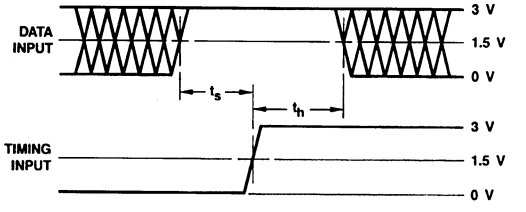
B. Three-State Delay Load (Load 2)

SWITCHING TEST WAVEFORMS

(All Devices)

Test	V_X	Output Waveform – Measurement Level
All t_{PD}s	V_{CC}	V_{OH}, V_{OL}, 1.5 V
t_{PHZ}	0.0 V	V_{OH}, 0.5 V, 0.0 V
t_{PLZ}	2.6 V	2.6 V, 0.5 V, V_{OL}
t_{PZH}	0.0 V	V_{OH}, 1.5 V, 0.0 V
t_{PZL}	2.6 V	2.6 V, 1.5 V, V_{OL}

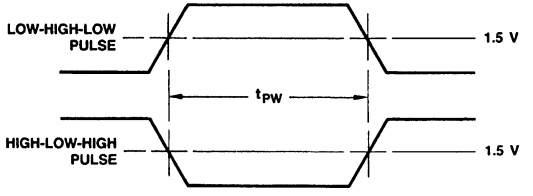
WFR02781



WFR02971

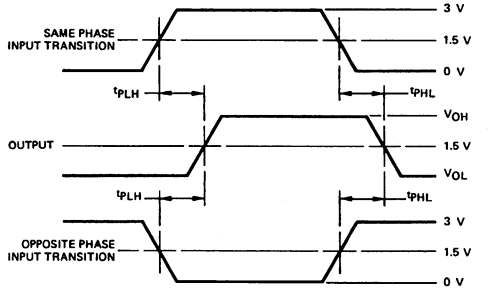
Notes: 1. Diagram shown for HIGH data only.
Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

Setup, Hold, and Release Times



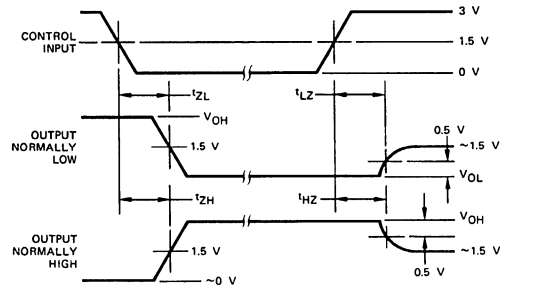
WFR02851

Pulse Width



WFR02980

Propagation Delay



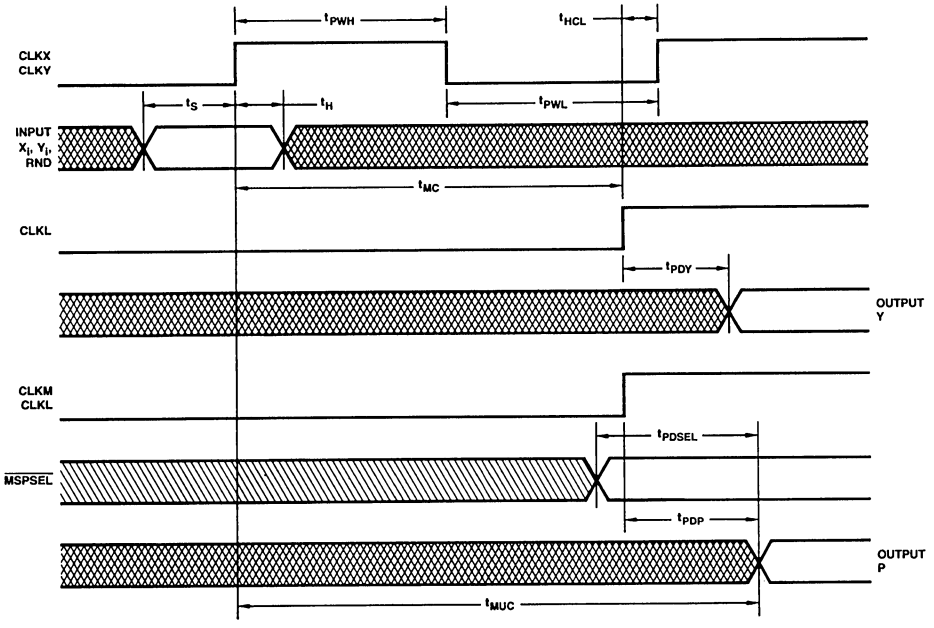
WFR02662

Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.

Enable and Disable Times

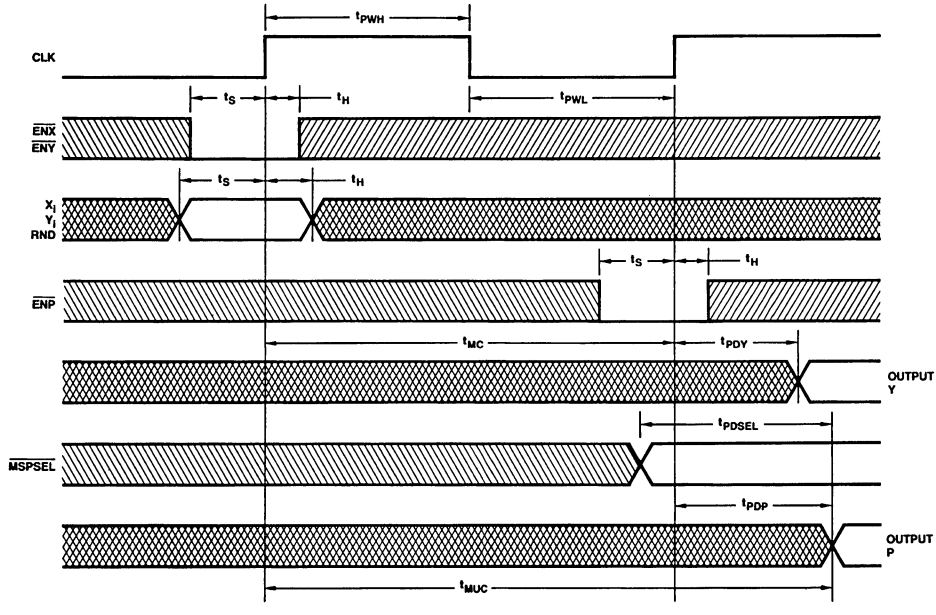
SWITCHING WAVEFORMS

Am29C516A/Am29C516A-1



WFR02741

Am29C517A/Am29C517A-1



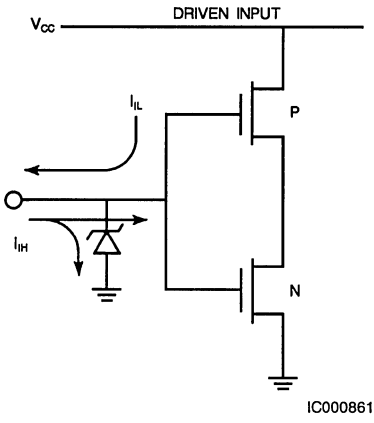
WFR02751

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

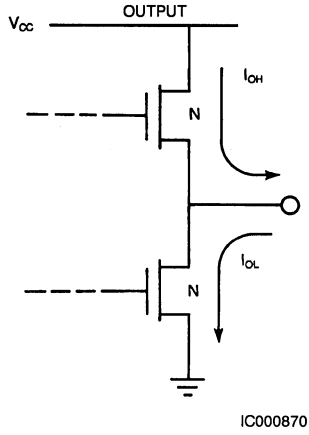
KS000010

INPUT/OUPUT CIRCUIT DIAGRAMS



IC000861

$C_I \approx 5.0$ pF, all inputs

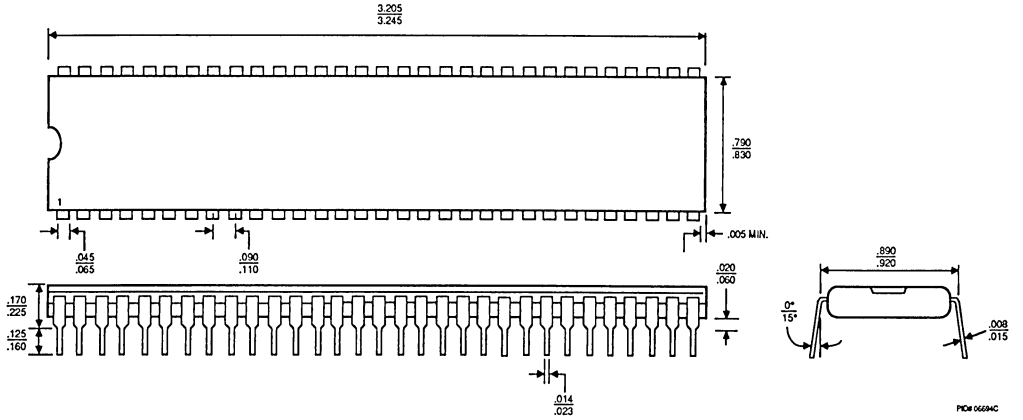


IC000870

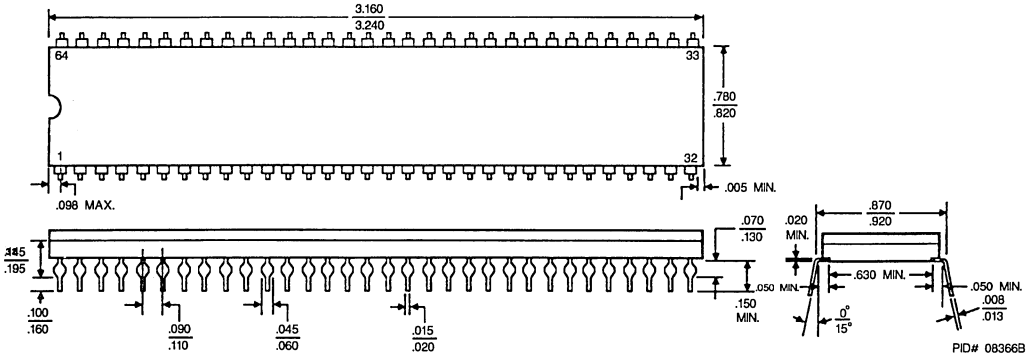
$C_O \approx 5.0$ pF, all outputs

PHYSICAL DIMENSIONS*

PD 064



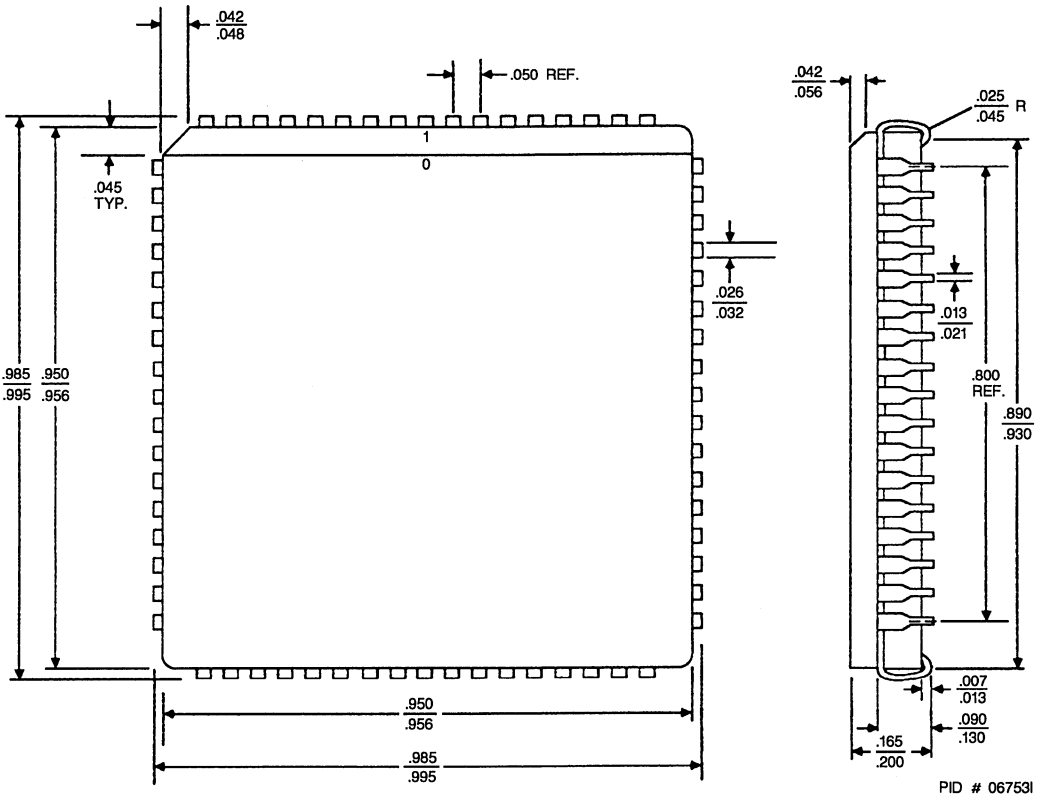
TDX064



*For reference only.

PHYSICAL DIMENSIONS (Cont'd.)

PL 068



ADVANCED MICRO DEVICES 901 Thompson Pl., P.O. Box 3453, Sunnyvale, CA 94088, USA
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