MACH® 1, 2, 3, and 4 Family Data Book

High Density EE CMOS Programmable Logic

1995

Advanced
Micro
Devices

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MACH® 1, 2, 3, and 4 Data Book and Design Guide

1995

ADVANCED MICRO DEVICES

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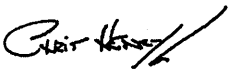
First introduced in the Fall of 1990, MACH (Macro Array CMOS High-density) devices have set the industry standard for high-speed, predictable worst-case pin-to-pin delays for devices ranging from 900 to 3,600 PLD gates. For the first time, higher-density electrically-erasable (EE) CMOS PAL®-like devices with truly predictable speeds were widely available. The MACH family's already-familiar architecture aided its rapid acceptance. Today, the MACH family has been designed into thousands of systems around the world and several million MACH devices have been shipped.

Based on customer feedback on the MACH 1 and 2 family, Advanced Micro Devices (AMD) created the MACH 3 and 4 family. Like the first generation MACH 1 and 2 devices, the newer MACH 3 and 4 devices offer the same, truly predictable pin-to-pin delays, but with greater density, flexibility and higher pin-count packages. The MACH 3 and 4 family feature synchronous and asynchronous operation, 5-volt on-board programming and JTAG in packages greater than 84 pins, densities from 3,500 to 10,000 PLD gates, and 84 to 208 pins in PLCC and PQFP packages.

However, the evolution of the MACH family did not stop here. As a growing number of customer designs migrated from PAL to MACH devices, they required solutions offering even higher density, greater flexibility and higher value. Through leading-edge process technology and design innovation, AMD introduced Performance Plus devices, enhanced versions of popular MACH 1 and 2 devices. The Performance Plus devices build upon the same densities and solid benefits of the original MACH 1 and 2 family, adding improved routing, power management, Bus-Friendly I/Os, and PCI compliance.

An early pioneer and leader in the programmable logic world, AMD invented the industry-standard PAL devices and 22V10. AMD continued that tradition with the MACH family. Enabled by advanced process technology, which began with bipolar and today is state-of-the-art EE CMOS, AMD is committed to innovation in programmable logic. At AMD, we believe: "If it's a good idea. If it makes a difference to our customers. Run with it." The result: designers leverage the rapid design with and advanced features of MACH devices to speed their own value-added products to market.



Chris Henry
Director of Marketing
Programmable Logic

INTRODUCTION

This book is a guide to the MACH 1, 2, 3, and 4 families of programmable logic from Advanced Micro Devices. These devices provide programmable logic capabilities from 900 PLD gates to 10,000 PLD gates. Included in this book is an overview of and data sheets for the MACH 1, 2, 3, and 4 family members.

The overview covers details affecting the entire MACH 1 and 2, and MACH 3 and 4 device families including a brief discussion of design software used in configuring the devices. Because of the common architecture, understanding the whole family yields knowledge about much of the individual members.

The data sheets discuss items that are specific to each device. They contain the basic DC and switching specifications. Other general specifications, such as switching waveforms and endurance information, follow the data sheets since they are consistent for all devices.

Rounding out this book are application notes. The application notes range in topic from the general methodology of designing with MACH devices, to the theory and use of advanced MACH features such as on-board programming and test via JTAG pins, to specific MACH design examples.

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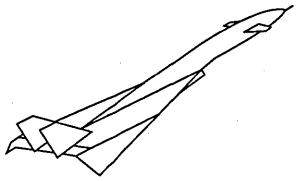
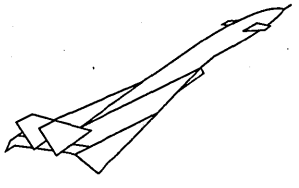


CHAPTER

1 MACH 1 AND 2 DEVICE FAMILIES DESCRIPTION



MACH 1 and 2 Device Families

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-performance, high-density, electrically-erasable CMOS PLD families**
- **900 to 3600 PLD gates**
- **44 to 84 pins in cost-effective PLCC and TQFP packages**
- **32 to 128 macrocells**
- **State-of-the art EE CMOS provides predictable design-independent high speeds**
  - — Commercial 7/10/12/15/20-ns t_{PD}, 133/100/76.9/66.6/50-MHz f_{CNT}
  - — Industrial 12/14/18/24, 80/61.5/53/38-MHz f_{CNT}
- **Synchronous and asynchronous devices**
- **PAL blocks connected by switch matrix**
  - — Provides optimized global connectivity
  - — Switch matrix integrates blocks into uniform device
- **Configurable macrocells**
  - — Programmable polarity
  - — Registered or combinatorial
  - — Internal and I/O feedback
  - — D-type or T-type flip-flops
  - — Choice of clocks for each flip-flop
  - — Input registers for MACH 2 family
- **Performance Plus devices such as the MACH111, MACH131, MACH211, MACH221, and MACH231 have a programmable power-down mode resulting in power savings of up to 75%**
- **The MACH111, MACH211, and MACH231 have improved routing over the MACH110, MACH210, and MACH230**
- **Extensive third-party software and programmer support through FusionPLD^{SM} partners**
  - — Schematic capture and text entry
  - — Compilation and JEDEC file generation
  - — Design simulation
  - — Logic and timing models
  - — Standard PLD programmers
- **Each MACH product has a factory programming option available for high-volume applications**

PRODUCT SELECTOR GUIDE

Device	Pins	Macrocells	PLD Gates	Max Inputs	Max Outputs	Max Flip-Flops	Speed (ns)
MACH 1 Family							
MACH110	44	32	900	38	32	32	12, 15, 20
MACH111	44	32	900	38	32	32	7, 10, 12, 15, 20
MACH120	68	48	1200	56	48	48	12, 15, 20
MACH130	84	64	1800	70	64	64	15, 20
MACH131	84	64	1800	70	64	64	7, 10, 12, 15, 20
MACH 2 Family							
MACH210	44	64	1800	38	32	64	7, 10, 12, 15, 20
MACH211	44	64	1800	38	32	64	7, 10, 12, 15, 20
MACH220	68	96	2400	56	48	96	12, 15, 20
MACH221	68	96	2400	56	48	96	7, 10, 12, 15, 20
MACH230	84	128	3600	70	64	128	15, 20
MACH231	84	128	3600	70	64	128	7, 10, 12, 15, 20
Asynchronous MACH Device							
MACH215	44	64	1500	38	32	64	12, 15, 20

GENERAL DESCRIPTION

The MACH (Macro Array CMOS High-density) family provides a new way to implement large logic designs in a programmable logic device. AMD has combined an innovative architecture with advanced electrically-erasable CMOS technology to offer a device with several times the logic capability of the industry's most popular existing PAL device solutions at comparable speed and cost.

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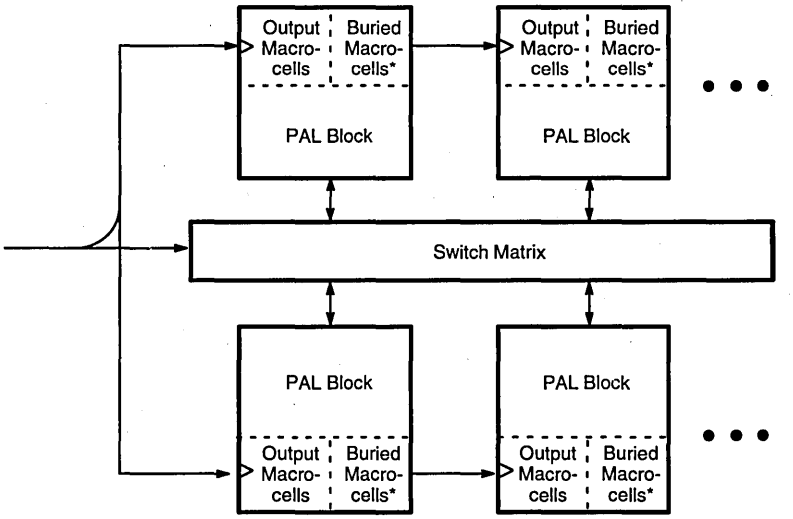
Their unique architecture makes these devices ideal for replacing large amounts of TTL, PAL-device, glue, and gate-array logic. They are the first devices to provide such increased functionality with completely predictable, deterministic speed.

The MACH devices consist of PAL blocks interconnected by a programmable switch matrix (Figure 1). Designs that consist of several interconnected functional modules can be efficiently implemented by placing the modules into PAL blocks. Designs that are not as modular can also be readily implemented since the switch matrix provides a high level of connectivity between PAL blocks. The internal arrangement of resources is managed automatically by the design software, so that the designer does not have to be concerned with the logic implementation details.

The MACH family consists of the MACH 1 and MACH 2 series of synchronous devices and the MACH215, an asynchronous device. The MACH 1 and 2 series are ideal for synchronous subsystems like memory controllers and peripheral controllers. The MACH215 is appropriate for applications having asynchronous inputs and for collecting random glue logic.

AMD's FusionPLD program allows MACH device designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide timely, accurate, quality support. This ensures that a designer does not have to buy a complete new set of tools for each new device, but rather can use the tools with which he or she is already familiar. The MACH devices can be programmed on conventional PAL device programmers with appropriate personality and socket adapter modules.

MACH devices are manufactured using AMD's state-of-the-art advanced CMOS electrically-erasable process for high performance and logic density. CMOS EE technology provides 100% testability, reducing both prototype development costs and production costs.



** Buried macrocell available on MACH 2 devices only.*

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Figure 1. MACH 1 and 2 Block Diagram

Design Methodology

Design tools for MACH devices are widely available both from AMD and from third-party software vendors. AMD supplies MACHXL® software as a low-cost baseline tool set and works with tools vendors to ensure broad MACH device support. This allows designers to do MACH device designs using the same tools that they would use to do PAL device designs, whether MACHXL software or any of the other popular PLD device design packages.

Design entry is the same as that used for PAL devices. The basic logic processing steps are the same steps that are needed to process and minimize logic for any PAL device. Simulation is available for verifying the correct behavior of the device. Functional (unit-delay) simulation of MACH devices is supported in all approved software packages, and other options for simulating the timing and board-level behavior of the MACH devices are available. The end result is a JEDEC file that can be downloaded to a programmer for device configuration.

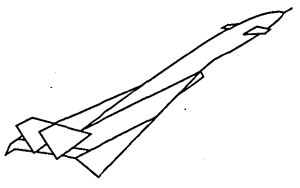
MACH device design methodology differs somewhat from that of a PAL device due to the automatic design fitting procedure that the software performs. Designs written by logic designers—whether by schematic capture, state machine equations, or Boolean equations—are partitioned and placed into the PAL blocks of the MACH device. While this procedure is handled

automatically by the software, the software can also accept manual direction based upon the user's working knowledge of the design. MACH device connectivity is 100% with the exception of the MACH230. This facilitates automatic place and route.

AMD recommends allowing the software to decide the best fit and pin placement automatically for the first design iteration to provide the best chance of fitting. With this approach, large designs can be implemented incrementally, starting with low device utilization and building up by adding logic until the device is full. This generally means that designs are done without any specific pinout assignments, with the final pinout decided by the software. While it is possible to pre-place signals, it is not recommended in most cases. If done carefully, pre-placement can help the software fit difficult designs; if not done carefully, it may make it harder for the design to fit.

The design is partitioned and placed into the MACH device by the software so as not to affect the performance of the design. With designs that do not fit, it is possible to make some performance tradeoffs to aid in fitting (for example, by optimizing the flip-flop type or passing through the device more than once), while any additional delays are entirely predictable, tradeoffs must be specifically requested.

Once an initial design fits, there may be subsequent changes to the design. This is important if board layout has already started based on the original pinout. Design changes make it necessary to refit the design, which may result in a different pinout. Some design changes may not make it possible to refit the design, regardless of the pinout. The stability of the design and the expected extent of any changes should therefore be considered before committing the design to layout. Hints on designing for change can be found in the *MACH Device Design Planning Guide* near the end of this book.



SYNCHRONOUS MACH DEVICES

The MACH 1 and MACH 2 families of synchronous devices each consist of several members. The items that differentiate the members of the family are the number of pins, the number of macrocells, the amount of interconnect, and the number of clocks. The MACH 1 family has output macrocells; the MACH 2 family has output and buried macrocells. In all other respects, the two families are the same.

This provides a convenient way of migrating designs up or down with little difficulty. Because there is a choice of I/O-pin-to-macrocell ratio, the designer can choose a device that suits both internal logic needs and I/O needs.

The devices range in pin count from 44 to 84, and in number of macrocells from 32 to 128. All devices are provided in cost-effective PLCC packages; some are available in TQFP packages.

Functional Description

The fundamental architecture of the MACH devices consists of multiple, optimized PAL blocks interconnected by a switch matrix. The switch matrix allows communication between PAL blocks, and routes inputs to the PAL blocks. Together, the PAL blocks and switch matrix allow the logic designer to create large designs in a single device instead of multiple devices.

Most pins are I/O pins that can be used as inputs, outputs, or bidirectional pins. There are some dedicated input pins, but all macrocells have internal feedback, allowing the pin to be used as an input if the macrocell signal is not needed externally.

The key to being able to make effective use of these devices lies in the interconnect schemes. Because of the programmable interconnections, the product-term arrays have been decoupled from the switch matrix, the macrocells, and the I/O pins. This provides the needed flexibility to place and route designs efficiently.

In a MACH device, all signals incur the same delays, regardless of routing. Performance is design-independent, and is therefore known before the design is begun.

The PAL Blocks

The PAL blocks can be viewed as independent PAL devices on the chip. This provides for logic functions that need the complete interconnect that a PAL device provides. PAL blocks communicate with each other only through the switch matrix.

Each PAL block consists of a product-term array, a logic allocator, macrocells, and I/O cells. The product-term array generates the basic logic, although the number of product terms per macrocell is variable. The logic allocator distributes the product terms to the macrocells as required by the design. The macrocell configures the signal, and the I/O cell delivers the final signal to the output pin.

Each PAL block additionally contains an asynchronous reset product term and an asynchronous preset product term. This allows the flip-flops within a single PAL block to be initialized as a bank. There are also several three-state product terms that provide three-state control to the I/O cells.

The Switch Matrix

The switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that only return to the same PAL block still must go through the switch matrix. This mechanism ensures that PAL blocks in MACH devices communicate with each other with consistent, predictable delays.

The switch matrix makes a MACH device more than just several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

The Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the switch matrix (Table 1), and are provided in both true and complement forms for efficient logic implementation.

Because the number of product terms available for a given function is not fixed, the full sum of products is not realized in the array. The product terms drive the logic allocator, which allocates the appropriate number of product terms to generate the function.

Table 1. PAL Block Inputs

Device	Number of Inputs to PAL Block
MACH110	22
MACH111	26
MACH120	26
MACH130	26
MACH131	26
MACH210	22
MACH211	26
MACH220	26
MACH221	26
MACH230	26
MACH231	32

The Logic Allocator

The logic allocator (Figure 2) is a block within which different product terms are allocated to the appropriate macrocells in groups of four product terms called "product term clusters". The availability and distribution of product term clusters is automatically considered by the software as it places and routes functions within the PAL block. The size of the product term clusters has been designed to provide high utilization of product terms. Complex functions using many product terms are possible. When few product terms are used, there will be a minimal number of unused–or wasted–product terms left over.

The product term clusters do not "wrap" around the logic block. This means that the macrocells at the ends of the block have fewer product terms available. Refer to the individual device data sheets for details.

The Macrocell

There are two fundamental types of macrocell: the output macrocell and the buried macrocell. The buried macrocell is only found in MACH 2 devices. The use of buried macrocells effectively doubles the number of macrocells available without increasing the pin count.

Both macrocell types can generate registered or combinatorial outputs. For the MACH 2 series, a transparent-low latched configuration is provided. If used, the register can be configured as a T-type or a D-type flip-flop. Register and latch functionality is defined in Table 2. Programmable polarity (for output macrocells) and the T-type flip-flop both give the software a way to minimize the number of product terms needed. These choices can be made automatically by the software when it fits the design into the device.

Table 2. Register/Latch Operation

Configuration	D/T	CLK/LE	Q+
D-Register	X	0, 1, ↓	Q
	0	↑	0
	1	↑	1
T-Register	X	0,1, ↓	Q
	0	↑	Q
	1	↑	$\overline{Q}$
Latch	X	1	Q
	0	0	0
	1	0	1

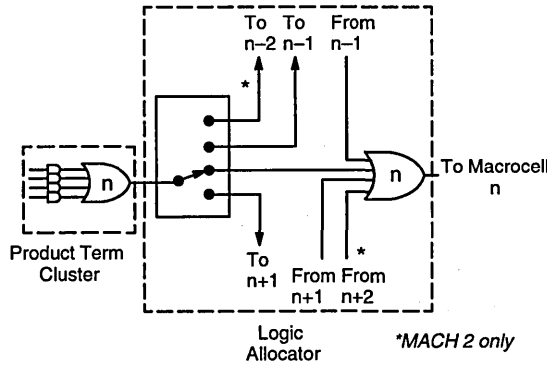
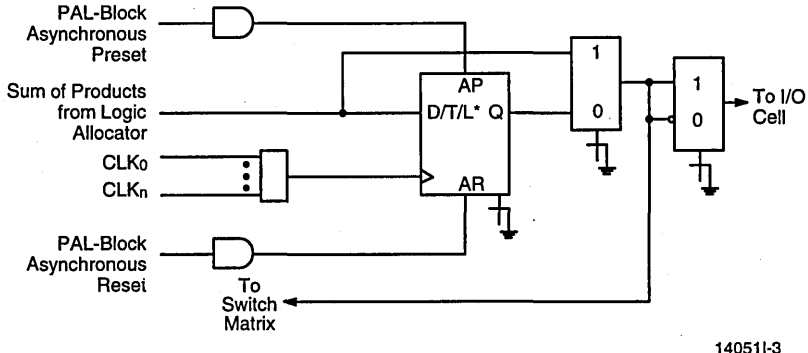
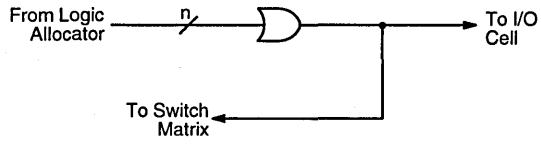


Figure 2. Product Term Clusters and the Logic Allocator

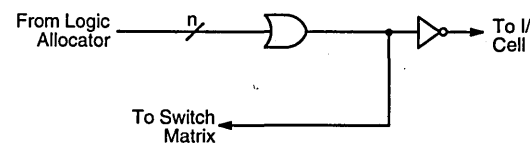


** Latch option available on MACH 2 devices only.*

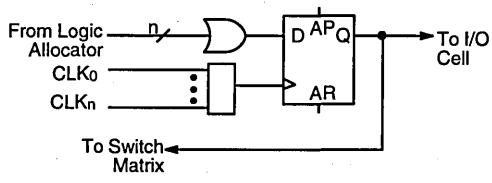
Figure 3. Output Macrocell



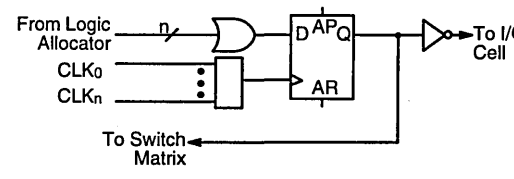
a. Combinatorial, Active High



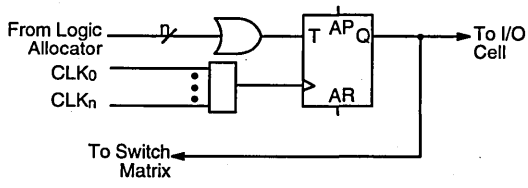
b. Combinatorial, Active Low



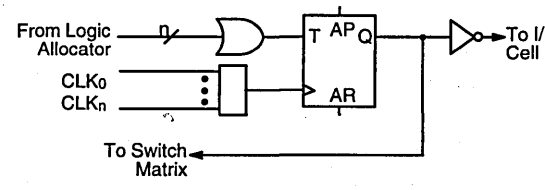
c. D-type Register, Active High



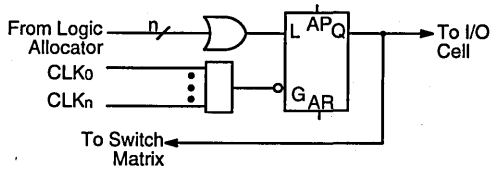
d. D-type Register, Active Low



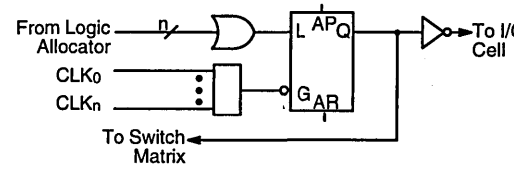
e. T-type Register, Active High



f. T-type Register, Active Low



g. Latch, Active High (MACH 2 only)



h. Latch, Active Low (MACH 2 only)

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Figure 4. Output Macrocell Configurations

The output macrocell (Figure 3) sends its output back to the switch matrix, via internal feedback, and to the I/O cell. The feedback is always available regardless of the configuration of the I/O cell. This allows for buried combinatorial or registered functions, freeing up the I/O pins for use as inputs if not needed as outputs. The basic output macrocell configurations are shown in Figure 4.

The buried macrocell (Figure 5) does not send its output to an I/O cell. The output of a buried macrocell is provided only as an internal feedback signal which feeds the switch matrix. This allows the designer to generate additional logic without requiring additional pins.

In addition to the capabilities of the output macrocell, the buried macrocell allows the use of registered or latched inputs. The input register is a D-type flip-flop; the input latch is a transparent-low D-type latch. Once configured as a registered or latched input, the buried macrocell cannot generate logic from the product-term array. The basic buried macrocell configurations are shown in Figure 6.

The flip-flops in either macrocell type can be clocked by one of several clock pins (Table 3). Registers are clocked on the rising edge of the clock input. Latches hold their data when the gate input is HIGH. Clock pins are also available as inputs, although care must be taken when a signal acts as both clock and input to the same device.

Table 3. Macrocell Clocks

Device	Number of Clocks Available
MACH110	2
MACH111	4
MACH120	4
MACH130	4
MACH131	4
MACH210	2
MACH211	4
MACH220	4
MACH221	4
MACH230	4
MACH231	4

All flip-flops have asynchronous reset and preset. This is controlled by the common product terms that control all flip-flops within a PAL block. For a single PAL block, all flip-flops, whether in an output or a buried macrocell, are initialized together. The initialization functionality of the flip-flops is illustrated in Table 4.

Table 4. Asynchronous Reset/Preset Operation

Configuration	AR	AP	CLK/LE	Q+
Register	0	0	X	See Table 2
	0	1	X	1
	1	0	X	0
	1	1	X	0
Latch	0	0	X	See Table 2
	0	1	0	Illegal
	0	1	1	1
	1	0	0	Illegal
	1	0	1	0
	1	1	0	Illegal
	1	1	1	0

The I/O Cell

The I/O cell (Figure 7) provides a three-state output buffer. The three-state buffer can be left permanently enabled, for use only as an output; permanently disabled, for use as an input; or it can be controlled by one of two product terms, for bidirectional signals and bus connections. The two product terms provided are common to a bank of I/O cells.

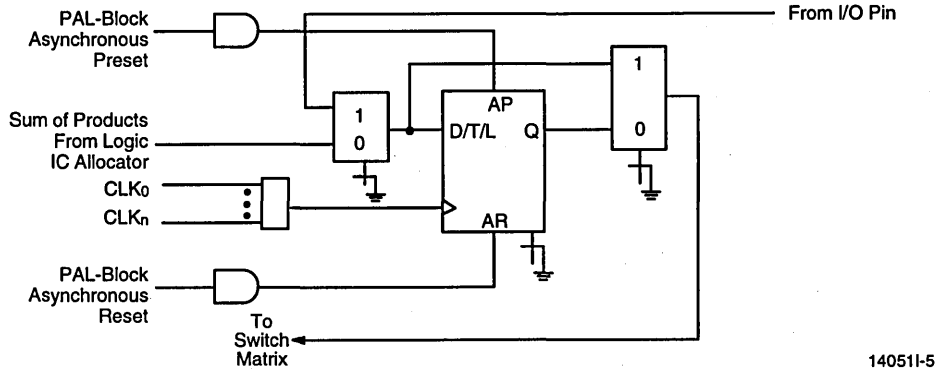


Figure 5. Buried Macrocell (MACH 2 only)

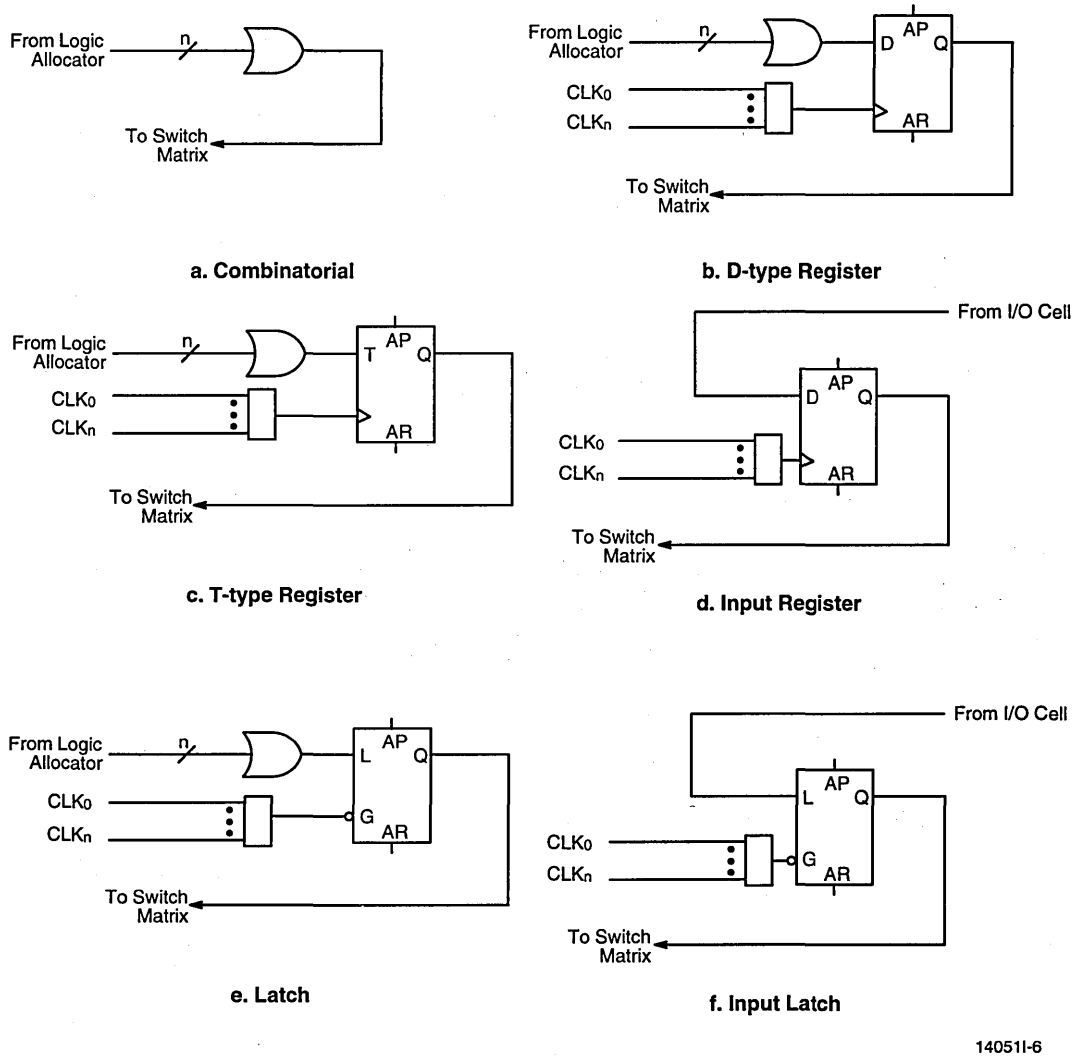


Figure 6. Buried Macrocell Configurations (MACH 2 only)

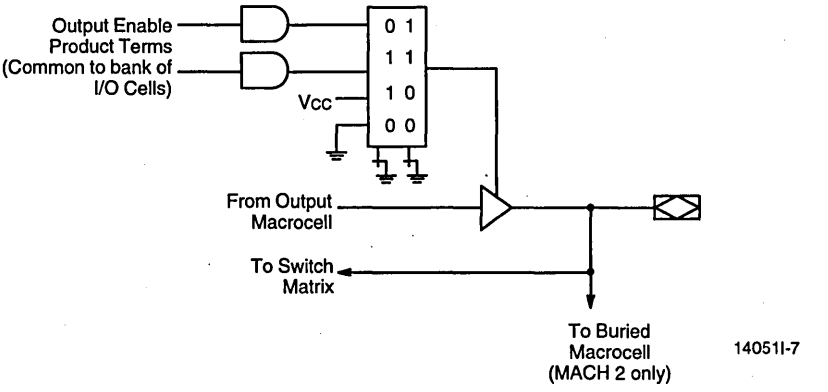


Figure 7. I/O Cell

Register Preload

All registers on the MACH devices can be preloaded from the I/O pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Observability

In addition to the control offered by preload, testing requires observability of the internal state of the device following a sequence of vectors. The MACH devices offer an observability feature that allows the user to send hidden buried register values to observable output pins.

For macrocells that are configured as combinatorial, the observability function suppresses the selection of the combinatorial output by forcing the macrocell output multiplexer into registered output mode. The observability function allows observation of the associated registers by overriding the output enable control and enabling the output buffer.

Power-up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. The actual values of the outputs of the MACH devices will depend on the configuration of the macrocell. The V_{CC} rise must be monotonic and the reset delay time is 10 µs maximum.

Security Bit

A security bit is provided on the MACH devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit, but test vectors containing preload can be used independently of the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Programming and Erasing

The MACH devices can be programmed on standard logic programmers. They may also be erased to reprogram a previously configured device with a new program. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The MACH devices offer a very high level of built-in quality. The fact that the device is erasable allows direct verification of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The MACH devices are fabricated with AMD's advanced electrically-erasable floating-gate 0.8-µm, 0.65-µm, and 0.50-µm CMOS technology. This provides the devices with performance and power consumption that are unmatched in the industry. The floating gate cells rely on Fowler-Nordheim tunneling to charge the gate, and have long proven their endurance and reliability. 20-year data retention is provided over operating conditions when devices are programmed on approved programmers.

The substrate of these devices is grounded, providing for a more efficient circuit. In addition, this provides substrate clamp diodes at all inputs, making them more immune to noisy input signals.

FINAL | COM'L: -12/15/20 | IND: -14/18/24

MACH110-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 32 Macrocells
- 12 ns t_{PD} Commercial
  14 ns t_{PD} Industrial
- 77 MHz f_{CNT}
- 38 Inputs
- 32 Outputs
- 32 Flip-flops; 2 clock choices
- 2 "PAL22V16" Blocks
- Pin-compatible with MACH111, MACH210, MACH211, MACH215

GENERAL DESCRIPTION

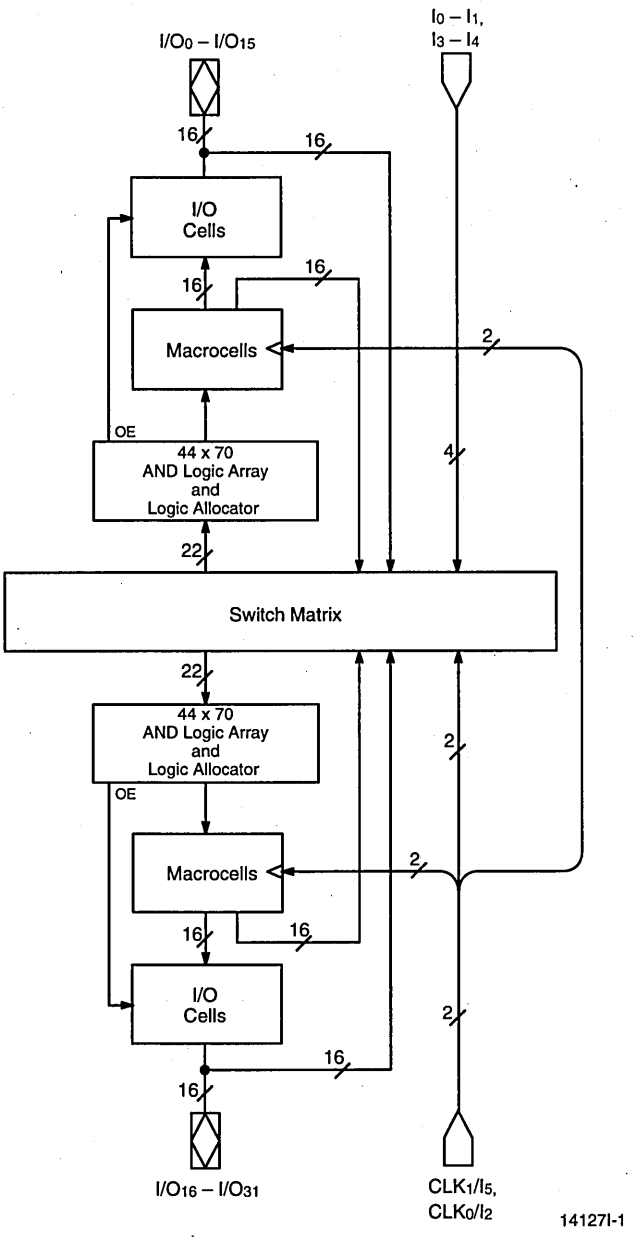
The MACH110 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately three times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH110 consists of two PAL blocks interconnected by a programmable switch matrix. The two PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH110 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

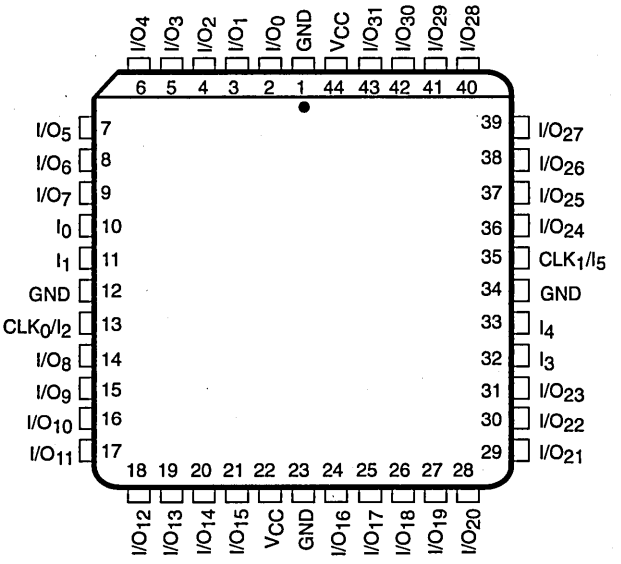
Publication# 14127 Rev. I Amendment/0
Issue Date: May 1995

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View

PLCC



14127I-2

Note:
Pin-compatible with MACH111, MACH210, MACH211, and MACH215.

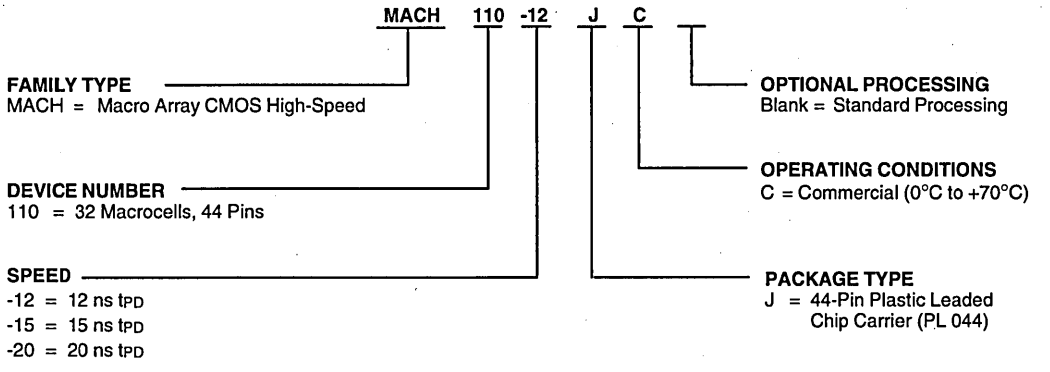
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH110-12	JC
MACH110-15	
MACH110-20	

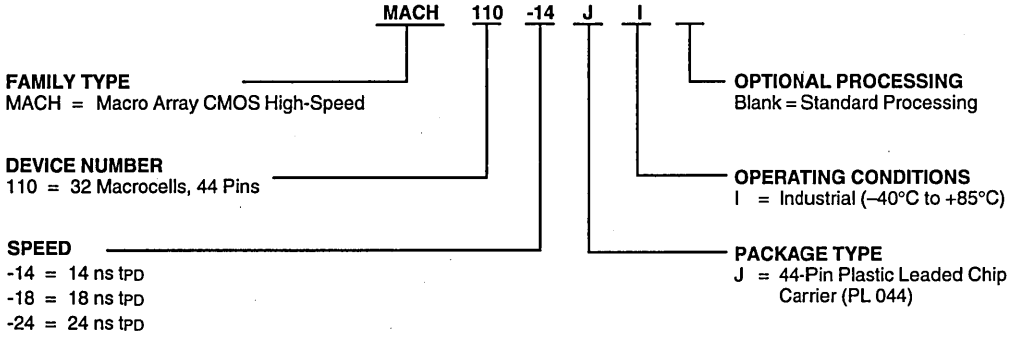
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for Industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH110-14	JI
MACH110-18	
MACH110-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH110 consists of two PAL blocks connected by a switch matrix. There are 32 I/O pins and 6 dedicated input pins feeding the switch matrix. These signals are distributed to the two PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH110 (Figure 1) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the output enable product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH110 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH110 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides a synchronous preset. Two of the output enable product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH110 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7
M_8	C_8, C_9
M_9	C_8, C_9, C_{10}
M_{10}	C_9, C_{10}, C_{11}
M_{11}	C_{10}, C_{11}, C_{12}
M_{12}	C_{11}, C_{12}, C_{13}
M_{13}	C_{12}, C_{13}, C_{14}
M_{14}	C_{13}, C_{14}, C_{15}
M_{15}	C_{14}, C_{15}

The Macrocell

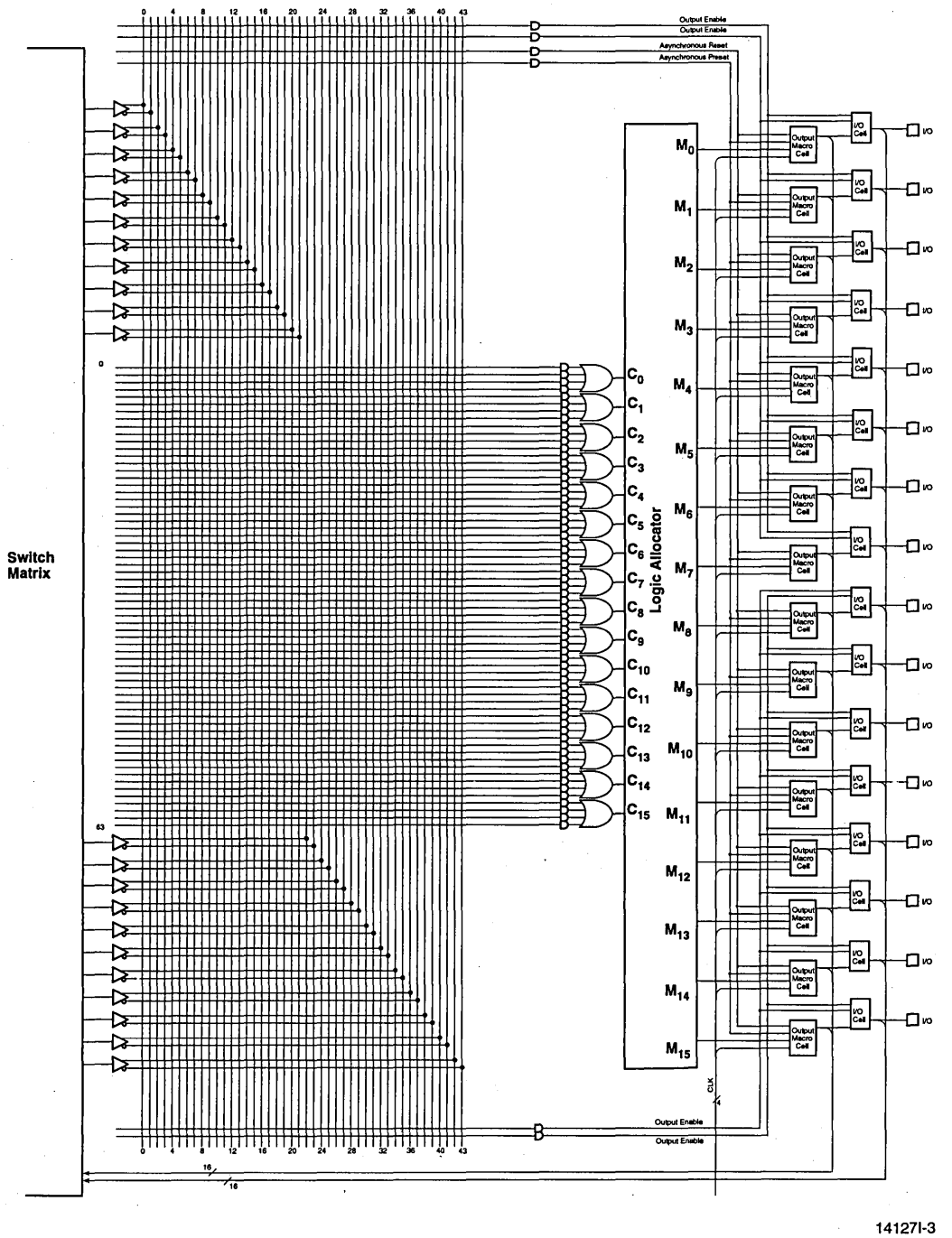
The MACH110 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH110 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells. Within each PAL block, two product terms are available for selection by the first eight three-state outputs; two other product terms are available for selection by the last eight three-state outputs.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.



14127I-3

Figure 1. MACH110 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A=25°C, f = 25 MHz (Note 4)		95		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter program. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-15		-20		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	76.9		66.6		47.6		MHz
				T-type	71.4		55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				8		10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)				12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)					12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)					12		15		20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 16 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = –40°C to +85°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		95		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

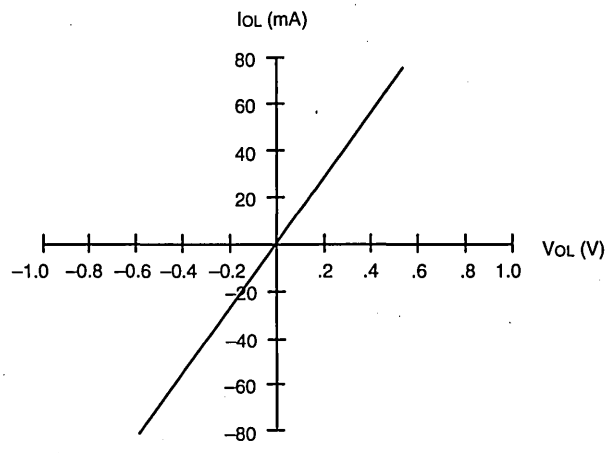
Parameter Symbol	Parameter Description				-14		-18		-24		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					14.5		18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	8.5		12		16		ns
				T-type	10		13.5		17		ns
t_H	Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12		14.5	ns
t_{WL}	Clock Width			LOW	7.5		7.5		10		ns
t_{WH}				HIGH	7.5		7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	53.5		40		32		MHz
				T-type	50		38		30		MHz
		Internal Feedback (f_{CNT})		D-type	61.5		53		38		MHz
				T-type	57		44		34.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		66.5		66.5		50		MHz
t_{AR}	Asynchronous Reset to Registered Output					19.5		24		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				14.5		18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				10		12		18		ns
t_{AP}	Asynchronous Preset to Registered Output					19.5		24		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)				14.5		18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				10		12		18		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)					14.5		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)					14.5		18		24	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 16 outputs switching.*

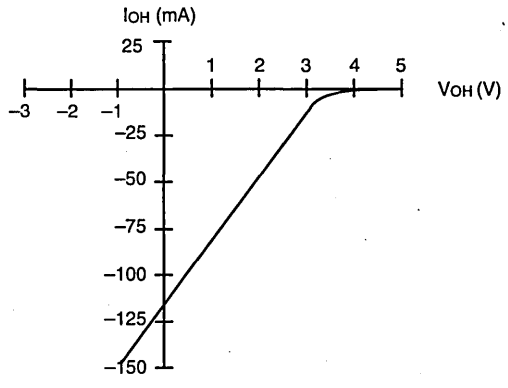
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



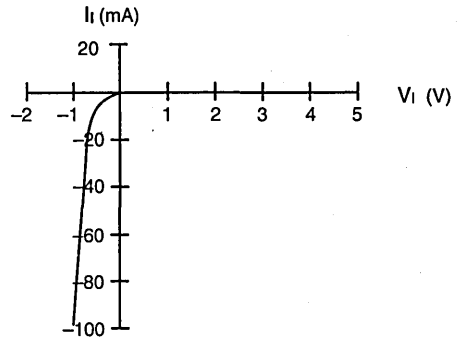
Output, LOW

14127I-4



14127I-5

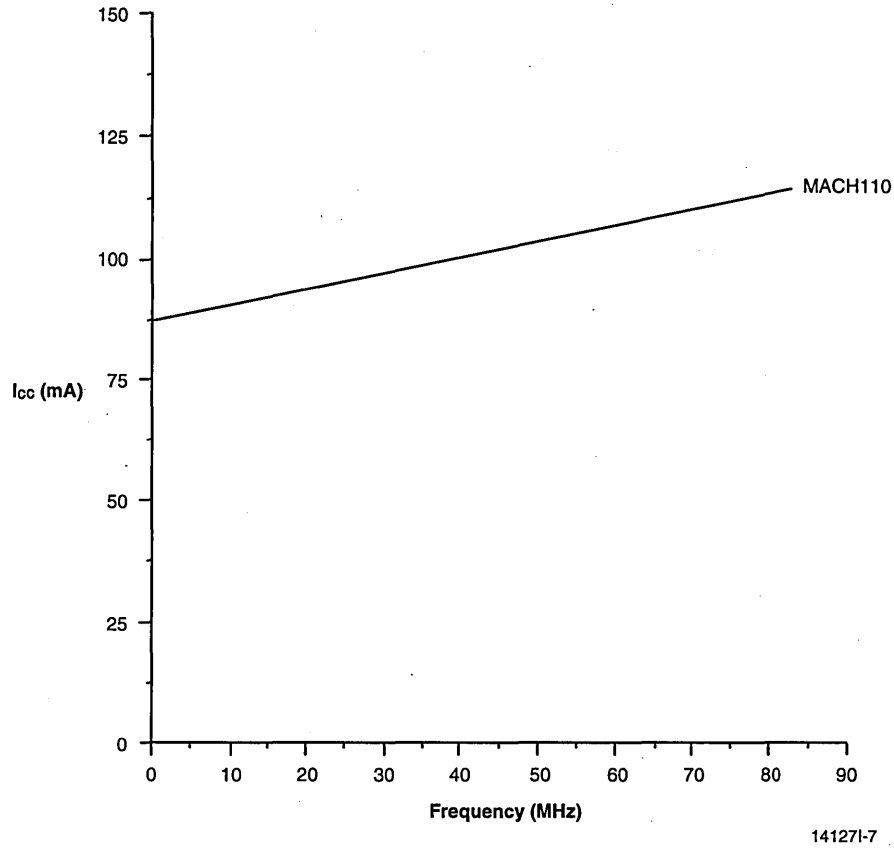
Output, HIGH



14127I-6

Input

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		14	°C/W
θ_{ja}	Thermal impedance, junction to ambient		39	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	33	°C/W
		400 lfpm air	30	°C/W
		600 lfpm air	27	°C/W
		800 lfpm air	25	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

FINAL COM'L: -5/7.5/10/12/15/20

MACH111-5/7/10/12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 32 Macrocells
- 5 ns t_{PD}
- 167 MHz f_{CNT}
- 38 Bus-Friendly Inputs
- Peripheral Component Interconnect (PCI) compliant
- Programmable power-down mode
- 32 Outputs
- 32 Flip-flops; 4 clock choices
- 2 "PAL26V16" Blocks
- Pin-compatible with MACH110, MACH210, MACH211, MACH215
- Improved routing over the MACH110

GENERAL DESCRIPTION

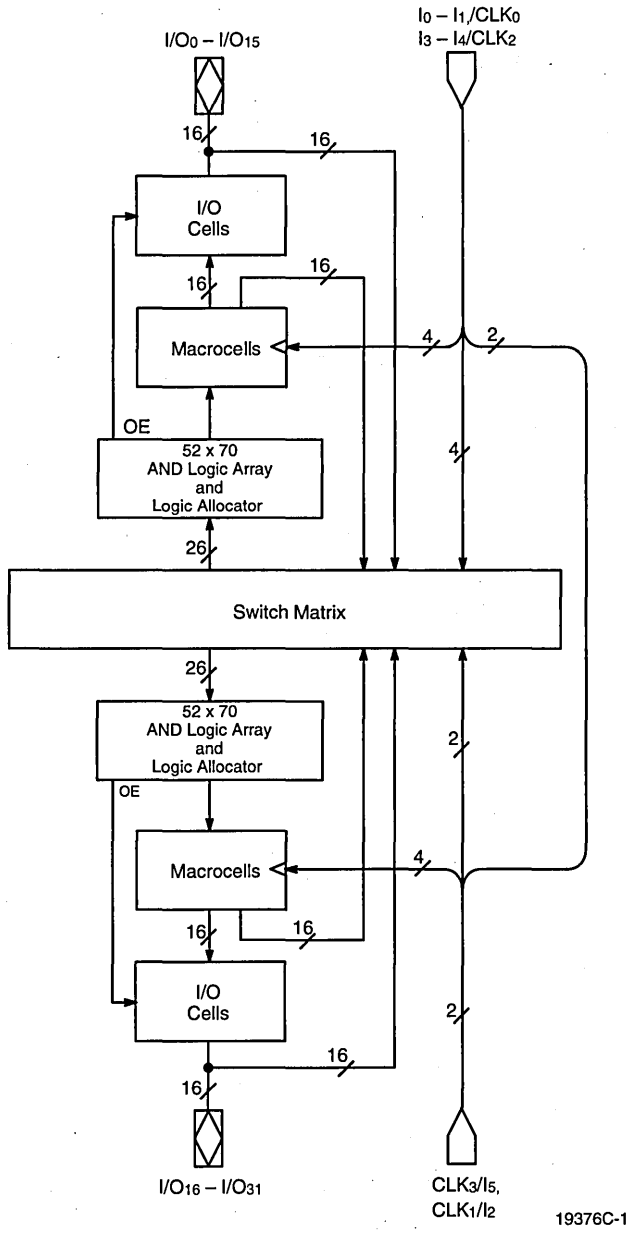
The MACH111 is a member of AMD's EE CMOS Performance Plus MACH 1 family. This device has approximately three times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH111 consists of two PAL blocks interconnected by a programmable switch matrix. The two PAL blocks are essentially "PAL26V16" structures complete with product-term arrays and programmable macrocells, which can be programmed as high speed or low power. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH111 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

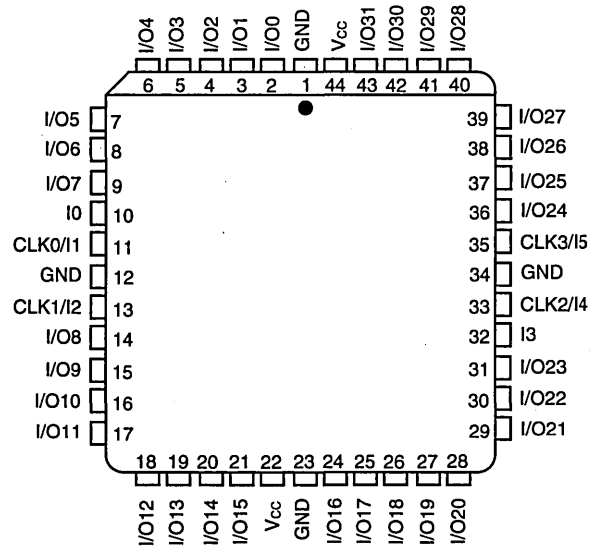
Publication# 19376 Rev. C Amendment/0
Issue Date: May 1995

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View

PLCC

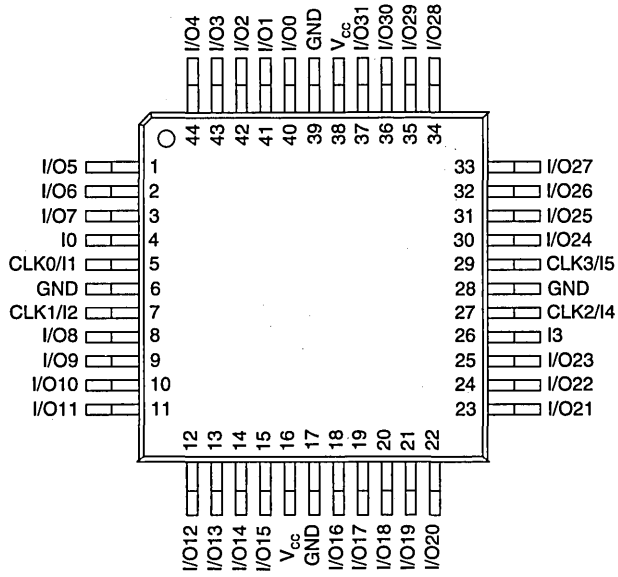


19376C-2

Note:
Pin-compatible with MACH110, MACH210, MACH211, and MACH215.

CONNECTION DIAGRAM
Top View

TQFP



Note:
Pin-compatible with MACH211 and MACH210A.

19376C-3

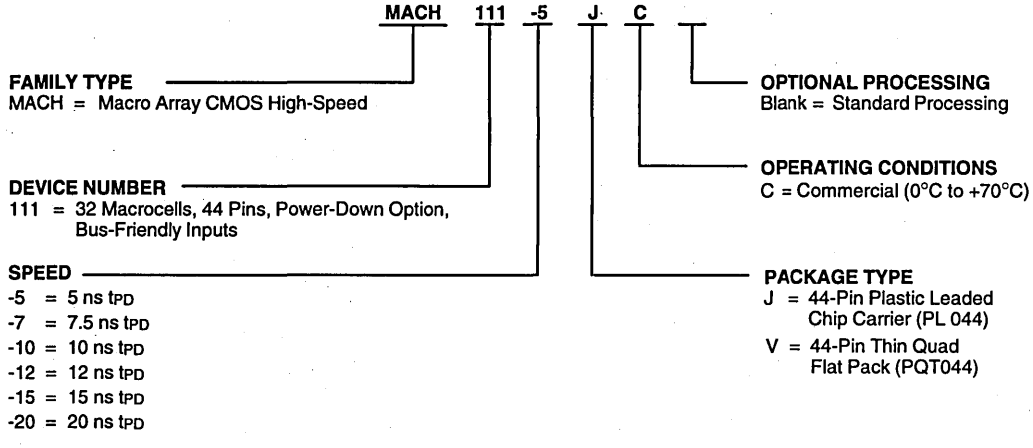
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH111-5	JC
MACH111-7	JC, VC
MACH111-10	
MACH111-12	
MACH111-15	
MACH111-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH111 consists of two PAL blocks connected by a switch matrix. There are 32 I/O pins and 6 dedicated input pins feeding the switch matrix. These signals are distributed to the two PAL blocks for efficient design implementation. There are four clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH111 (Figure 1) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the output enable product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH111 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH111 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the output enable product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH111 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7
M_8	C_8, C_9
M_9	C_8, C_9, C_{10}
M_{10}	C_9, C_{10}, C_{11}
M_{11}	C_{10}, C_{11}, C_{12}
M_{12}	C_{11}, C_{12}, C_{13}
M_{13}	C_{12}, C_{13}, C_{14}
M_{14}	C_{13}, C_{14}, C_{15}
M_{15}	C_{14}, C_{15}

The Macrocell

The MACH111 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four clock pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

Power-Down Mode

The MACH111 features a programmable low-power mode in which individual signal paths can be programmed as low power. These low-power speed paths will be slightly slower than the non-low-power paths. This feature allows speed critical paths to run at maximum frequency while the rest of the paths operate in the low-power mode, resulting in power savings of up to 50%.

The I/O Cell

The I/O cell in the MACH111 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells. Within each PAL block, two product terms are available for selection by the first eight three-state outputs; two other product terms are available for selection by the last eight three-state outputs.

Bus-Friendly Inputs and I/Os

The MACH111 inputs and I/Os include two inverters in series which loop back to the input. This double inversion reinforces the state of the input and pulls the voltage away from the input threshold voltage. Unlike a pull-up, this configuration cannot cause contention on a bus. For an illustration of this configuration, please turn to the input and output equivalent schematics at the end of this data book.

PCI Compliance

The MACH111-7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH111-7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without predictable timing, PCI compliance is dependent upon routing and product term distribution.

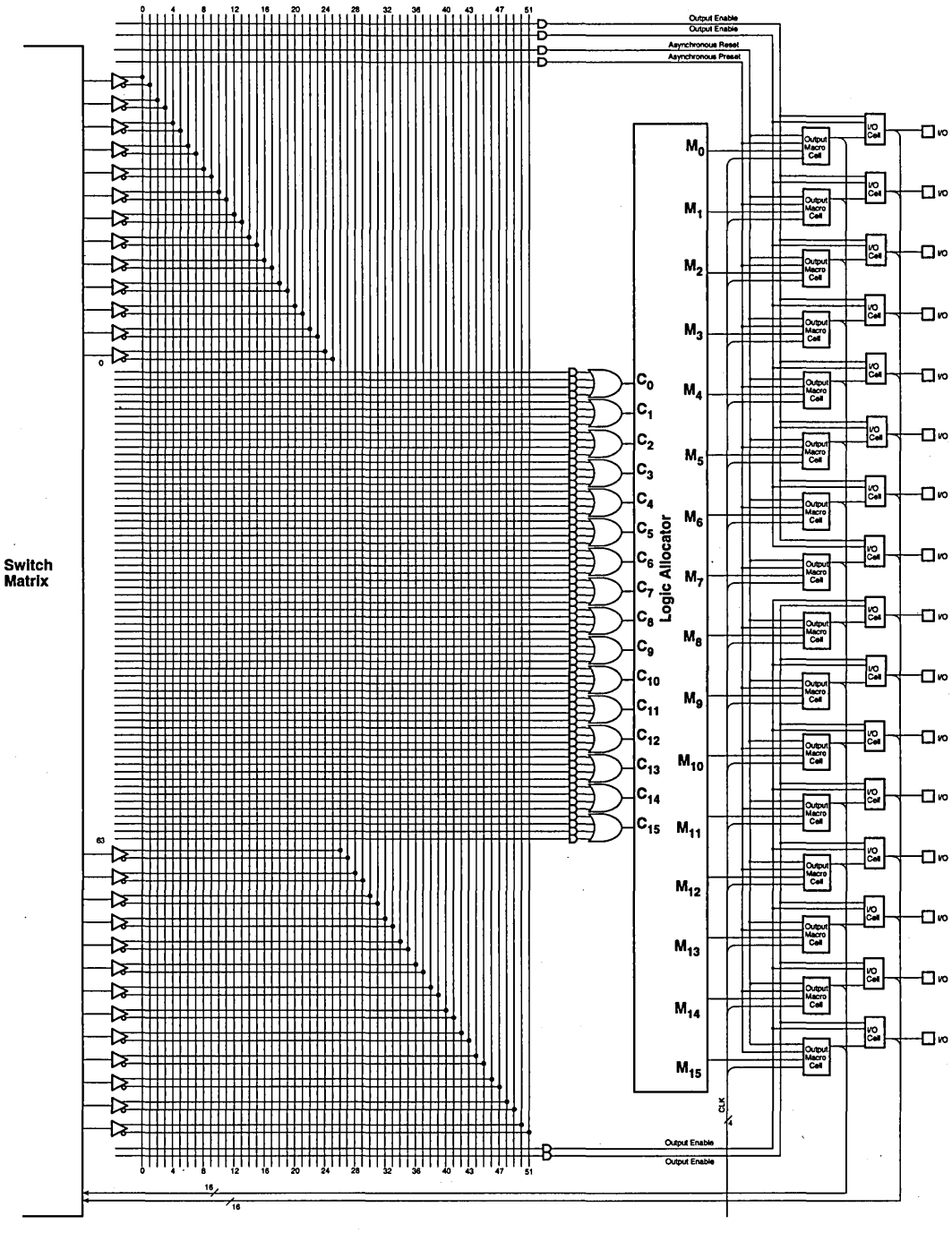


Figure 1. MACH111 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

			PRELIMINARY			
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A=25°C, f = 0 MHz (Note 4)		40		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A=25°C, f = 1 MHz (Note 4)		45		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter program in low-power mode. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = V_{CC} - 0.5$ V	$V_{CC} = 5.0$ V, $T_A = 25°C$	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				PRELIMINARY -5 Min	-5 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					5	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	4		ns
				T-type	4		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					4	ns
t_{WL}	Clock Width			LOW	2.5		ns
t_{WH}				HIGH	2.5		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	125		MHz
				T-type	125		MHz
		Internal Feedback (f_{CNT})		D-type	167		MHz
				T-type	151		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		200		MHz
t_{AR}	Asynchronous Reset to Registered Output					7.5	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				4.5		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				4.5		ns
t_{AP}	Asynchronous Preset to Registered Output					7.5	ns
t_{APW}	Asynchronous Preset Width (Note 1)				4.5		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				4.5		ns
t_{EA}	Input, I/O, or Feedback to Output Enable					7.5	ns
t_{ER}	Input, I/O, or Feedback to Output Disable					7.5	ns
t_{LP}	t_{PD} Increase for Powered-Down Macrocell (Note 3)					10	ns
t_{LPS}	t_S Increase for Powered-Down Macrocell (Note 3)					7	ns
t_{LPCO}	t_{CO} Increase for Powered-Down Macrocell (Note 3)					3	ns
t_{LPEA}	t_{EA} Increase for Powered-Down Macrocell (Note 3)					10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Conditions.*
3. *If a signal is powered down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A=25°C, f = 0 MHz (Note 4)		90		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A=25°C, f = 1 MHz (Note 4)		95		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter program in low-power mode. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = V_{CC} - 0.5$ V	$V_{CC} = 5.0$ V, $T_A = 25°C$	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-7		-10		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					7.5		10	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	5.5		6.5		ns
				T-type	6.5		7.5		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output					5		6	ns
t_{WL}	Clock Width			LOW	3		5		ns
t_{WH}				HIGH	3		5		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	95		80		MHz
				T-type	87		74		MHz
		Internal Feedback (f_{CNT})		D-type	133		100		MHz
				T-type	125		91		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		166.7		100		MHz
t_{AR}	Asynchronous Reset to Registered Output					9.5		11	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				5		7.5		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				5		7.5		ns
t_{AP}	Asynchronous Preset to Registered Output					9.5		11	ns
t_{APW}	Asynchronous Preset Width (Note 1)				5		7.5		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				5		7.5		ns
t_{EA}	Input, I/O, or Feedback to Output Enable					9.5		10	ns
t_{ER}	Input, I/O, or Feedback to Output Disable					9.5		10	ns
t_{LP}	t_{PD} Increase for Powered-Down Macrocell (Note 3)					10		10	ns
t_{LPS}	t_S Increase for Powered-Down Macrocell (Note 3)					7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-Down Macrocell (Note 3)					3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-Down Macrocell (Note 3)					10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Conditions.*
3. *If a signal is powered down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A=25°C, f = 0 MHz (Note 4)		90		mA
	Supply Current (Typical)	V_{CC} = 5 V, T_A=25°C, f = 1 MHz (Note 4)		95		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter program in low power mode. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = V_{CC} - 0.5$ V	$V_{CC} = 5.0$ V, $T_A = 25°C$	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	f = 1 MHz	8	pF

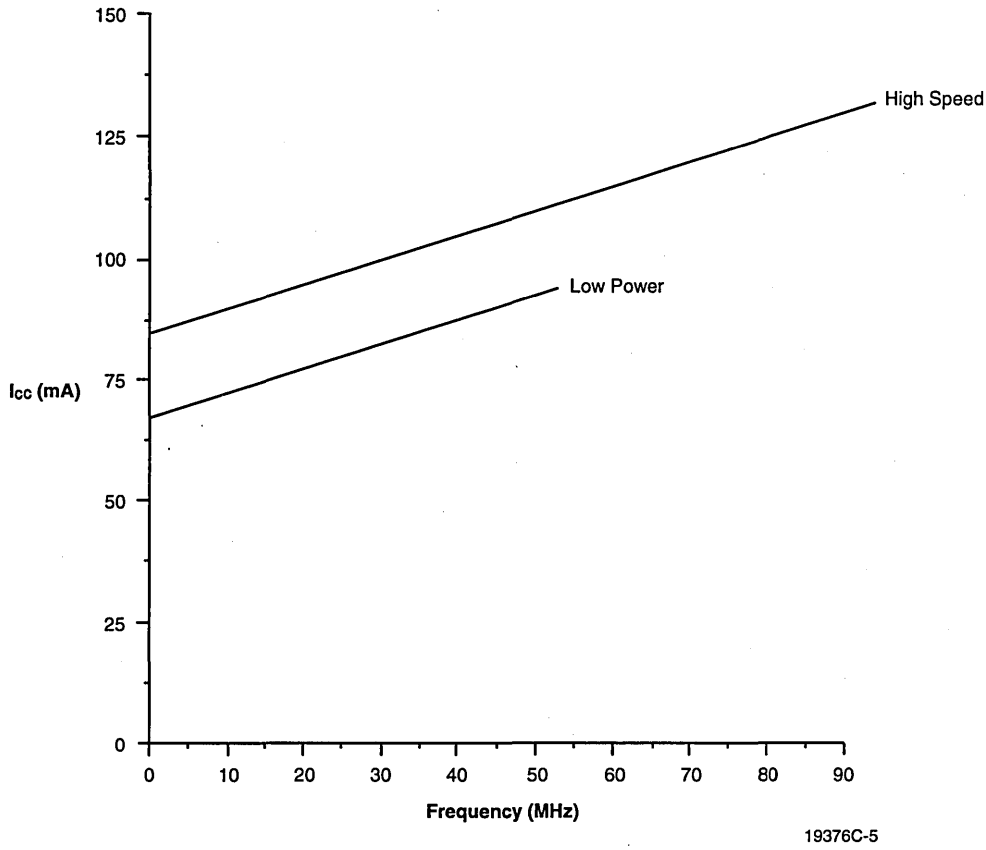
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-15		-20		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Hold Time				0		0		0		ns
t_{CO}	Clock to Output					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	76.9		66.6		47.6		MHz
				T-type	71.4		55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				8		10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)				12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable					12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable					12		15		20	ns
t_{LP}	t_{PD} Increase for Powered-Down Macrocell (Note 3)					10		10		10	ns
t_{LPS}	t_S Increase for Powered-Down Macrocell (Note 3)					7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-Down Macrocell (Note 3)					3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-Down Macrocell (Note 3)					10		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Conditions.*
3. *If a signal is powered down, this parameter must be added to its respective high-speed parameter.*

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ TQFP	Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		11.3	15	°C/W
θ_{ja}	Thermal impedance, junction to ambient		40	53.2	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	34.7	45	°C/W
		400 lfpm air	32.9	42	°C/W
		600 lfpm air	32.5	38	°C/W
		800 lfpm air	31.3	35	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

FINAL COM'L: -12/15/20 IND: -18/24

MACH120-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 48 Macrocells
- 12 ns t_{PD} Commercial
  18 ns t_{PD} Industrial
- 77 MHz f_{CNT} Commercial
- 56 Inputs
- 48 Outputs
- 48 Flip-flops; 4 clock choices
- 4 "PAL26V12" blocks
- Pin-compatible with MACH220 and MACH221

GENERAL DESCRIPTION

The MACH120 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately five times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH120 consists of four PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH120 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

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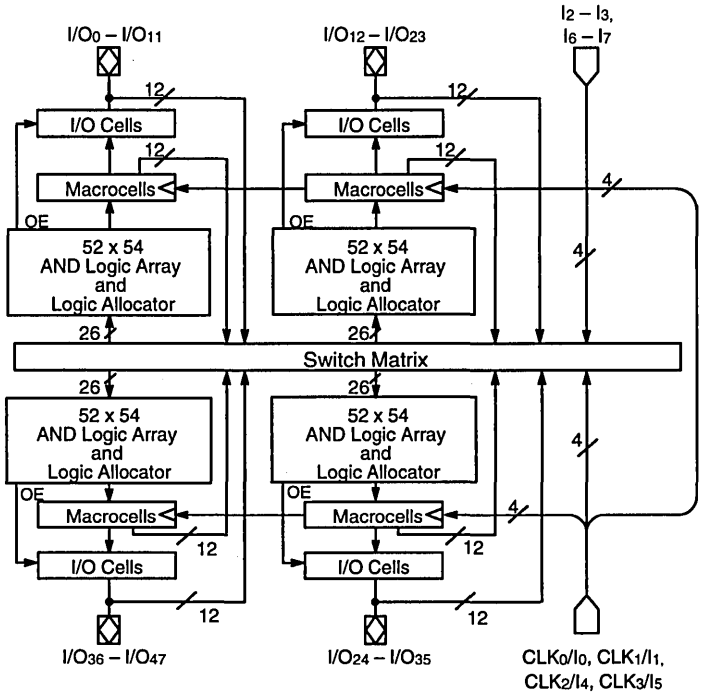
Issue Date: April 1995

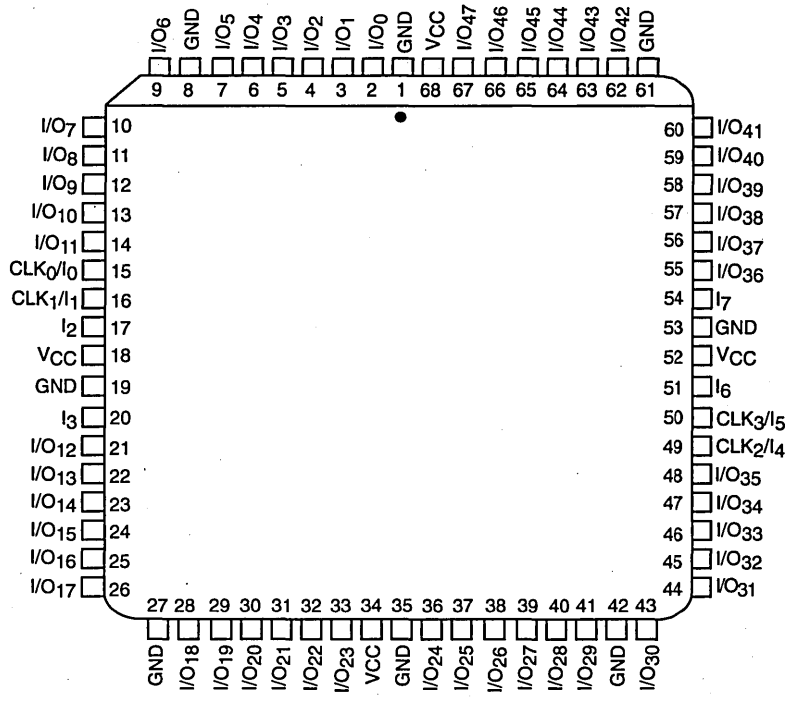
BLOCK DIAGRAM



CONNECTION DIAGRAMS

Top View

PLCC



14129I-2

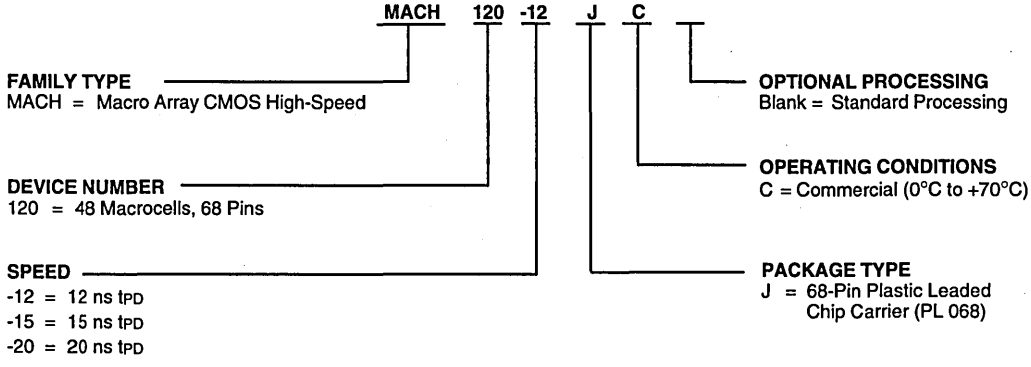
Note:
Pin-compatible with MACH220 and MACH221.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
Vcc = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



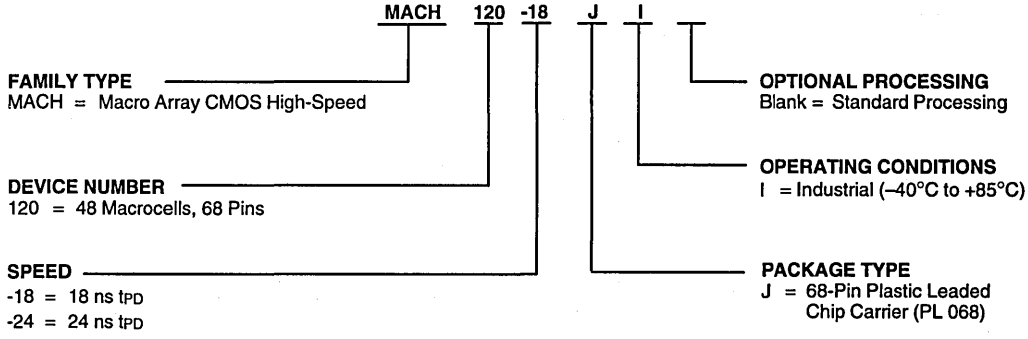
Valid Combinations	
MACH120-12	JC
MACH120-15	
MACH120-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH120-18	JI
MACH120-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH120 consists of four PAL blocks connected by a switch matrix. There are 48 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH120 (Figure 1) contains a 48-product-term logic array, a logic allocator, 12 macrocells and 12 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V12".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 12 I/O cells are divided into 2 banks of 6 macrocells. Each bank is allocated two of the output enable product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH120 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 12 internal feedback signals and 12 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH120 product-term array consists of 48 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the output enable product terms are used for the first six I/O cells; the other two control the last six macrocells.

The Logic Allocator

The logic allocator in the MACH120 takes the 48 logic product terms and allocates them to the 12 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7, C_8
M_8	C_7, C_8, C_9
M_9	C_8, C_9, C_{10}
M_{10}	C_9, C_{10}, C_{11}
M_{11}	C_{10}, C_{11}

The Macrocell

The MACH120 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four global clock pins, which are also available as logic inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH120 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to six I/O cells. Within each PAL block, two product terms are available for selection by the first six three-state outputs; two other product terms are available for selection by the last six three-state outputs.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

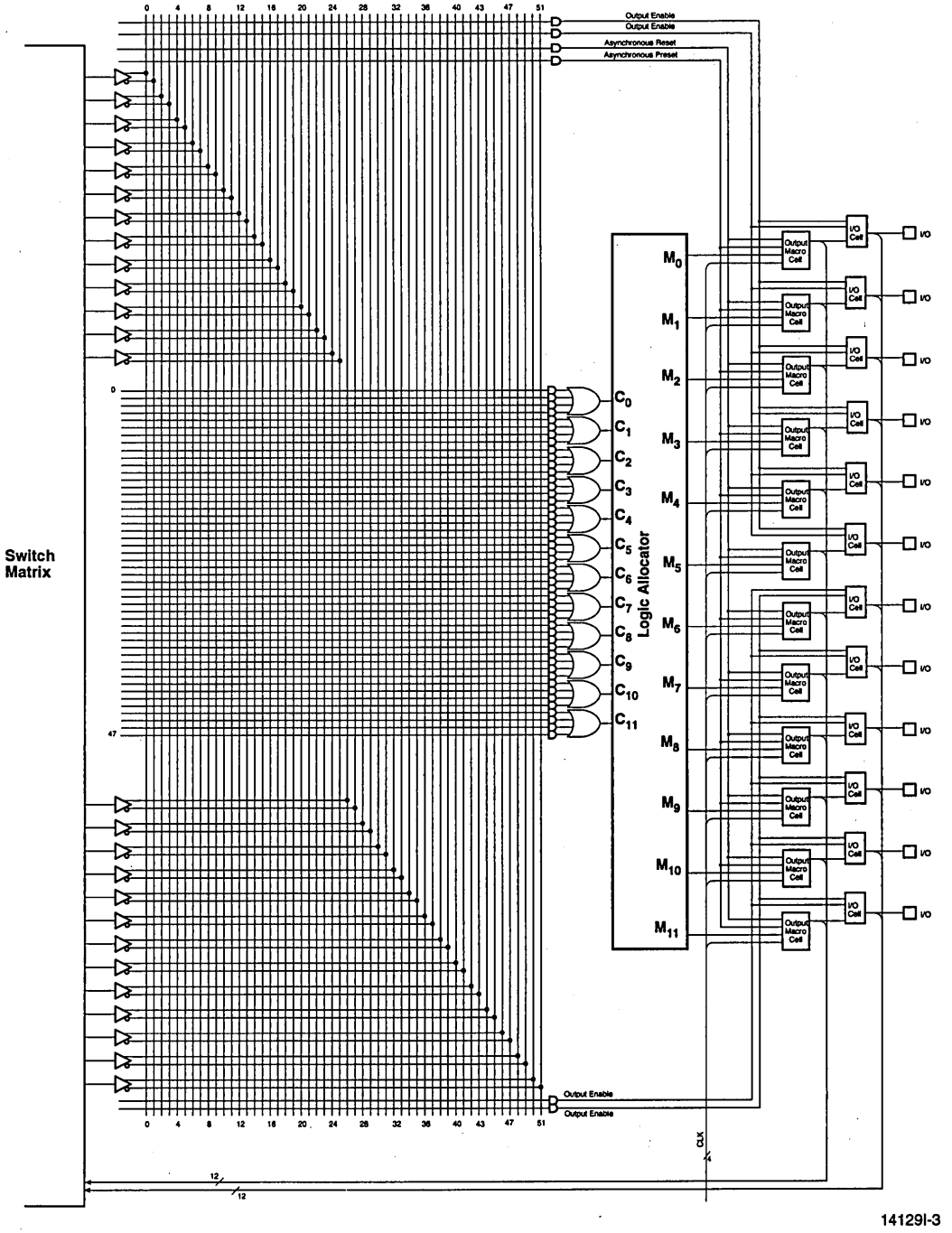


Figure 1. MACH120 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A=25°C, f = 25 MHz (Note 4)		85		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 12-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-12 Min	-12 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				12	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock		D-type	7		ns
			T-type	8		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				8	ns
t_{WL}	Clock Width		LOW	6		ns
t_{WH}			HIGH	6		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	D-type	66.7		MHz
			T-type	62.5		MHz
		Internal Feedback (f_{CNT})	D-type	76.9		MHz
			T-type	71.4		MHz
		No Feedback		83.3		MHz
t_{AR}	Asynchronous Reset to Registered Output				16	ns
t_{ARW}	Asynchronous Reset Width (Note 1)			12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)			8		ns
t_{AP}	Asynchronous Preset to Registered Output				16	ns
t_{APW}	Asynchronous Preset Width (Note 1)			12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)			8		ns
t_{EA}	Input, I/O, or Feedback to Output Enable				12	ns
t_{ER}	Input, I/O, or Feedback to Output Disable				12	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit, for test conditions.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A=25°C, f = 25 MHz (Note 4)		85		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 12-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	11		14		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	1/(t_S + t_{CO})	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	1/(t_{WL} + t_{WH})		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)				15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)					15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)					15		20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 24 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = –40°C to +85°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		85		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 12-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

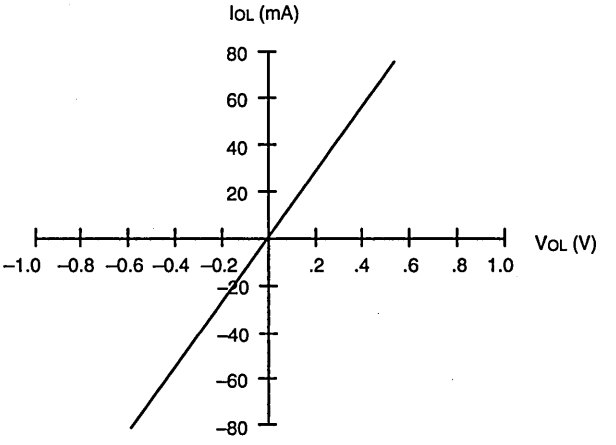
Parameter Symbol	Parameter Description				-18		-24		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	12		16		ns
				T-type	13.5		17		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					12		14.5	ns
t_{WL}	Clock Width			LOW	7.5		10		ns
t_{WH}				HIGH	7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		32		MHz
				T-type	38		30		MHz
		Internal Feedback (f_{CNT})		D-type	53		38		MHz
				T-type	44		34.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		66.5		50		MHz
t_{AR}	Asynchronous Reset to Registered Output					24		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				12		18		ns
t_{AP}	Asynchronous Preset to Registered Output					24		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)				18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				12		18		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)					18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)					18		24	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 24 outputs switching.*

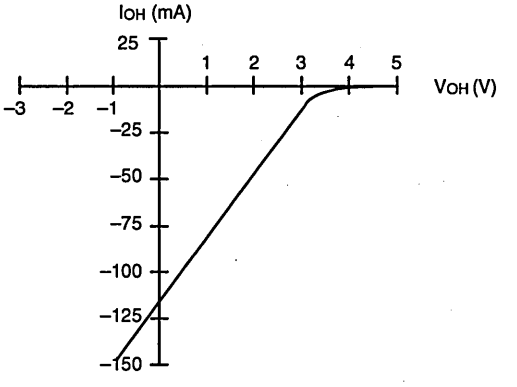
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



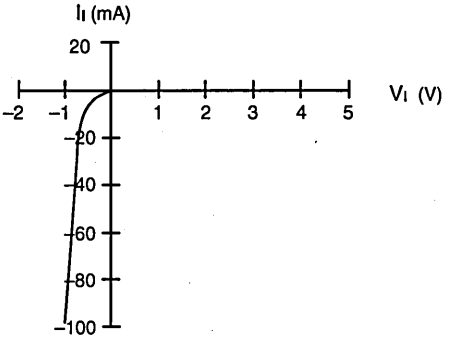
Output, LOW

14129I-4



Output, HIGH

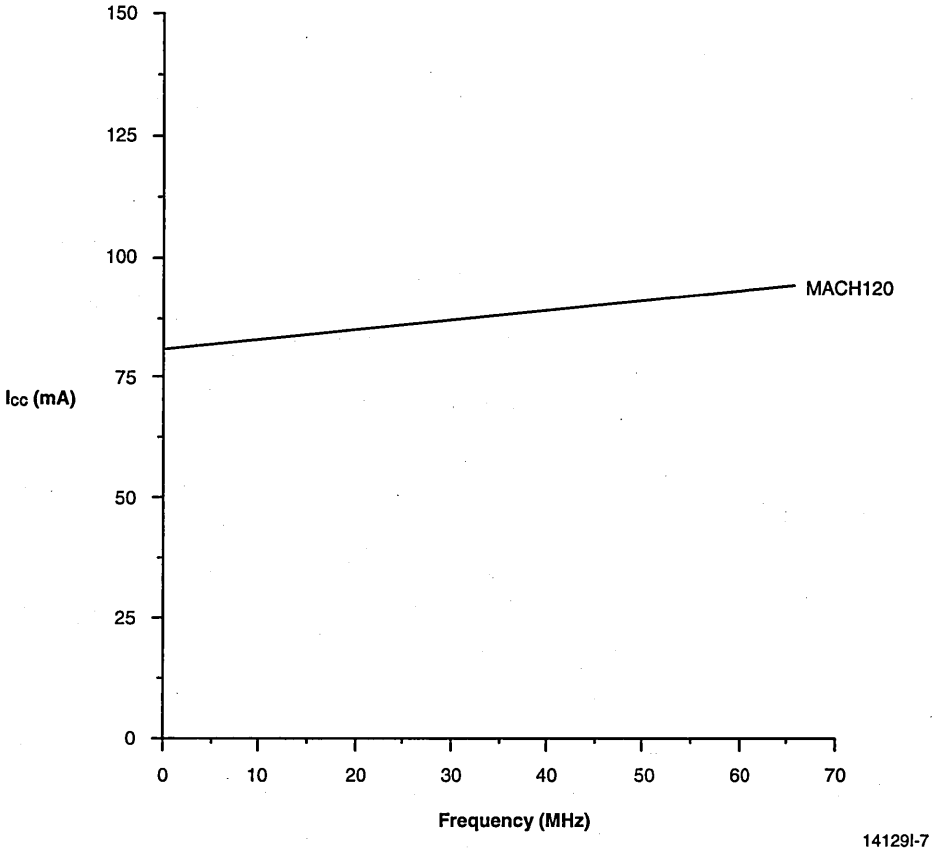
14129I-5



Input

14129I-6

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 12-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

14129H-8

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		13	°C/W
θ_{ja}	Thermal impedance, junction to ambient		37	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	33	°C/W
		400 lfpm air	30	°C/W
		600 lfpm air	28	°C/W
		800 lfpm air	25	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

FINAL COM'L: -15/20 IND: -18/24

MACH130-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 64 Macrocells
- 15 ns t_{PD} Commercial
  18 ns t_{PD} Industrial
- 66.6 MHz f_{CNT}
- 70 Inputs
- 64 Outputs
- 64 Flip-flops; 4 clock choices
- 4 "PAL26V16" Blocks
- Pin-compatible with MACH131, MACH230, MACH231, MACH435

GENERAL DESCRIPTION

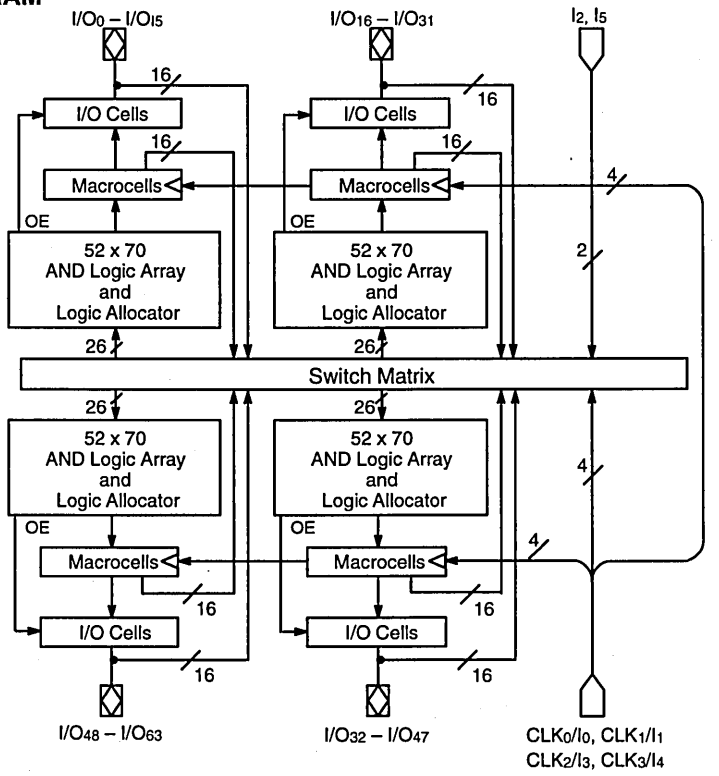
The MACH130 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH130 consists of four PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH130 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

Publication# 14131 Rev. H Amendment/0
Issue Date: April 1995

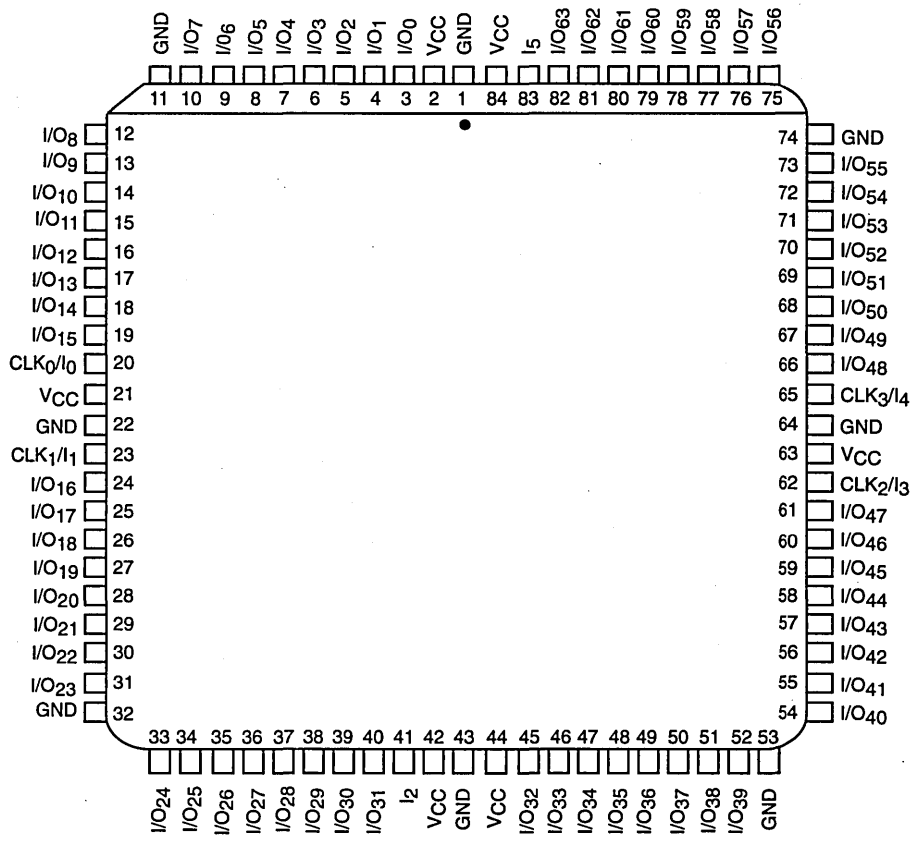
BLOCK DIAGRAM



14131H-1

CONNECTION DIAGRAM
Top View

PLCC



Note:
Pin-compatible with MACH131, MACH230, MACH231, and MACH435.

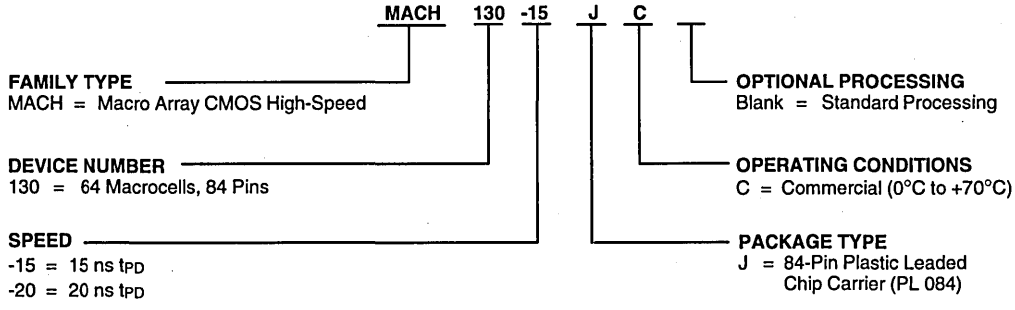
14131H-2

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



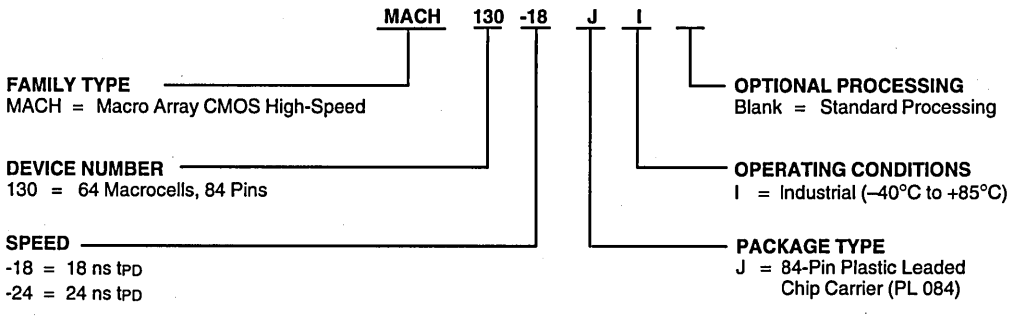
Valid Combinations	
MACH130-15	JC
MACH130-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH130-18	JI
MACH130-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH130 consists of four PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH130 (Figure 1) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the output enable product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH130 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH130 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the output enable product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH130 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7, C_8
M_8	C_7, C_8, C_9
M_9	C_8, C_9, C_{10}
M_{10}	C_9, C_{10}, C_{11}
M_{11}	C_{10}, C_{11}, C_{12}
M_{12}	C_{11}, C_{12}, C_{13}
M_{13}	C_{12}, C_{13}, C_{14}
M_{14}	C_{13}, C_{14}, C_{15}
M_{15}	C_{14}, C_{15}

The Macrocell

The MACH130 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four global clock pins, which are also available as logic inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH130 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells. Within each PAL block, two product terms are available for selection by the first eight three-state outputs; two other product terms are available for selection by the last eight three-state outputs.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

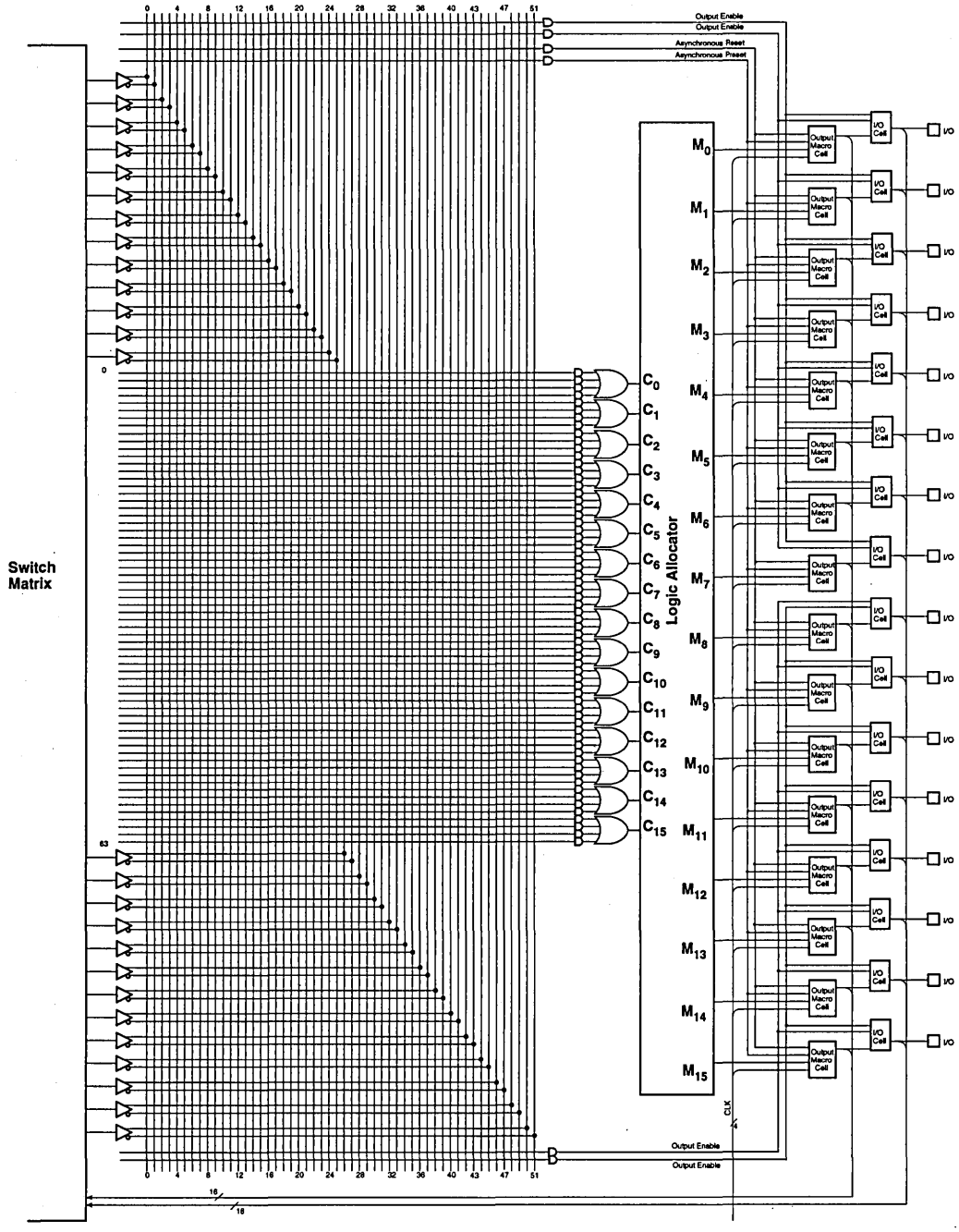


Figure 1. MACH130 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5V, T_A = 25°C, f = 25 MHz (Note 4)		190		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	11		14		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)				15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)					15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)					15		20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 32 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = –40°C to +85°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		190		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

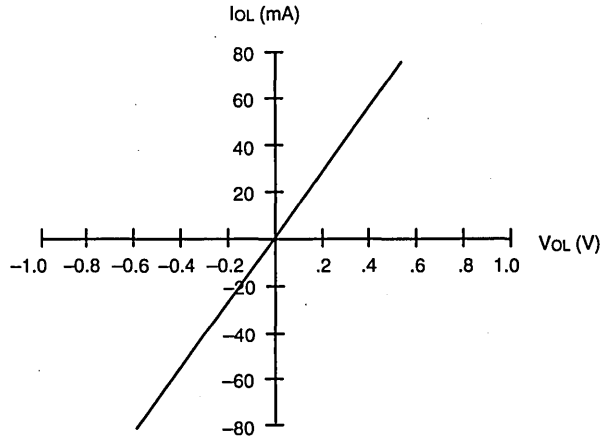
Parameter Symbol	Parameter Description				-18		-24		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	12		16		ns
				T-type	13.5		17		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					12		14.5	ns
t_{WL}	Clock Width			LOW	7.5		10		ns
t_{WH}				HIGH	7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		32		MHz
				T-type	38		30		MHz
		Internal Feedback (f_{CNT})		D-type	53		38		MHz
				T-type	44		34.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		66.5		50		MHz
t_{AR}	Asynchronous Reset to Registered Output					24		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				12		18		ns
t_{AP}	Asynchronous Preset to Registered Output					24		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)				18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				12		18		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)					18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)					18		24	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 32 outputs switching.*

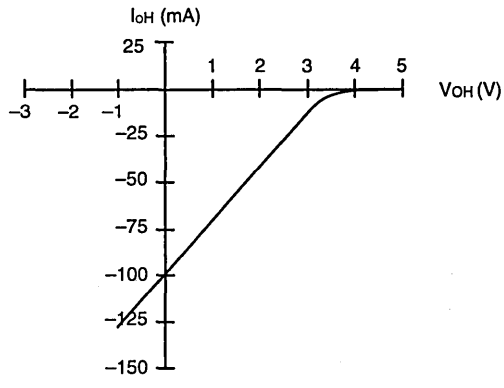
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



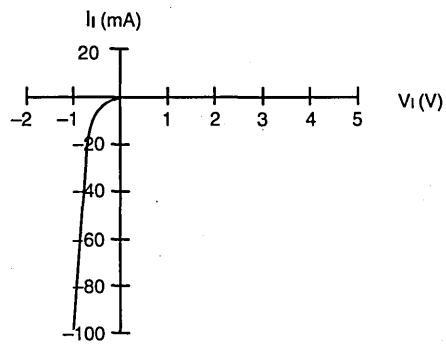
14131H-4

Output, LOW



14131H-5

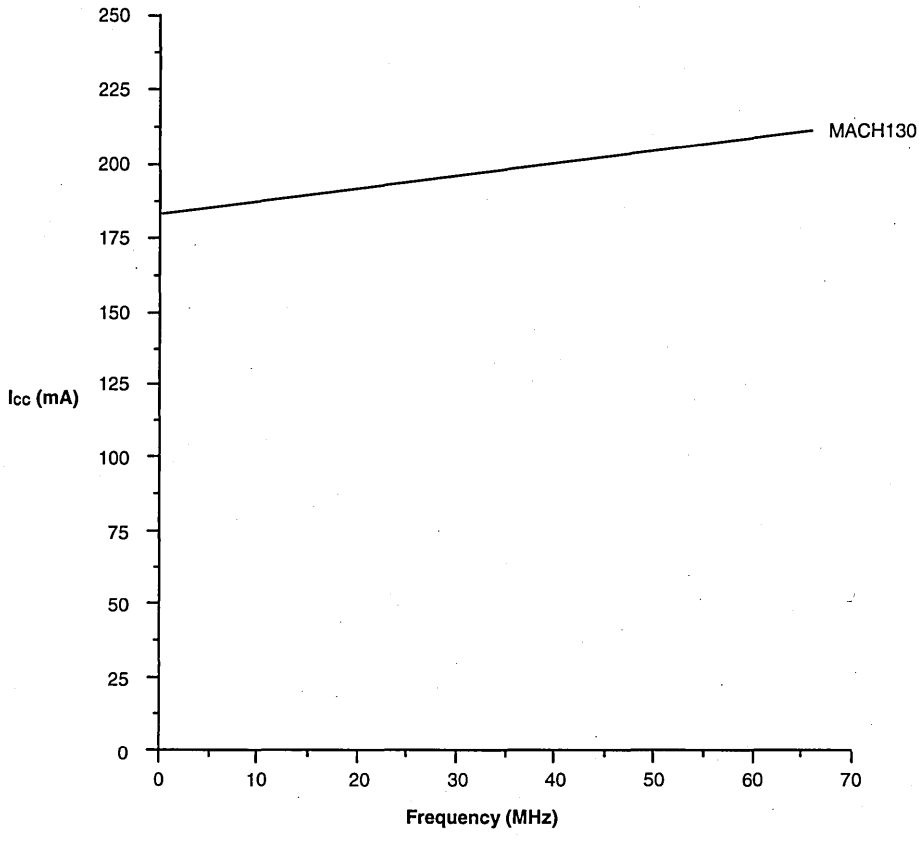
Output, HIGH



14131H-6

Input

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		13	°C/W
θ_{ja}	Thermal impedance, junction to ambient		34	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	30	°C/W
		400 lfpm air	28	°C/W
		600 lfpm air	26	°C/W
		800 lfpm air	25	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

FINAL COM'L: -7.5/10/12/15/20

MACH131-7/10/12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 64 Macrocells
- 7.5 ns t_{PD}
- 133 MHz f_{CNT}
- 70 Bus-friendly inputs
- Peripheral Component Interconnect (PCI) Compliant
- Programmable power-down mode
- 64 Outputs
- 64 Flip-flops; 4 clock choices
- 4 "PAL26V16" Blocks
- Pin-compatible with MACH130, MACH230, MACH231, MACH435
- JEDEC compatible with MACH130

GENERAL DESCRIPTION

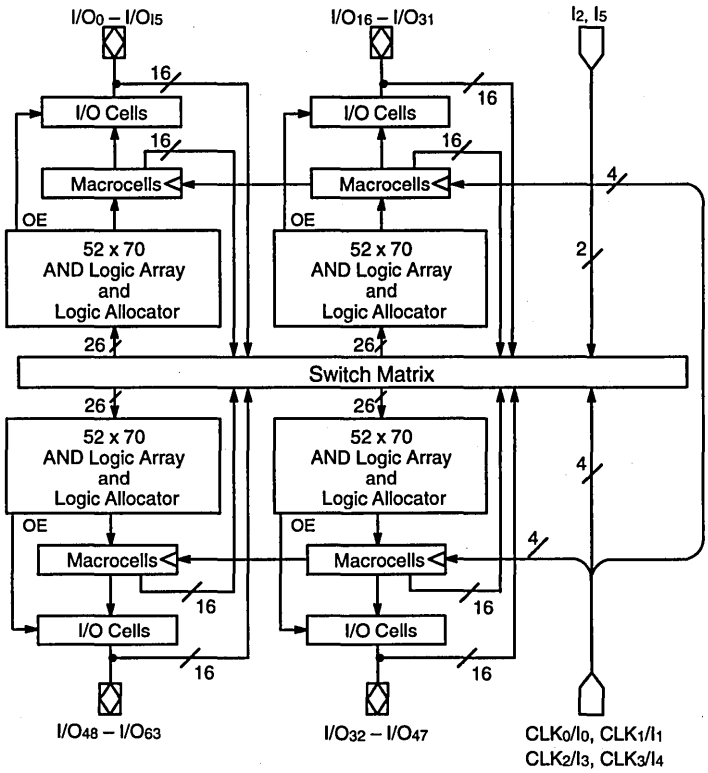
The MACH131 is a member of AMD's EE CMOS Performance Plus MACH 1 family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH131 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL26V12" structures complete with product-term arrays and programmable macrocells, including additional buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH131 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell.

Publication# 18889 Rev. C Amendment/0
Issue Date: April 1995

BLOCK DIAGRAM

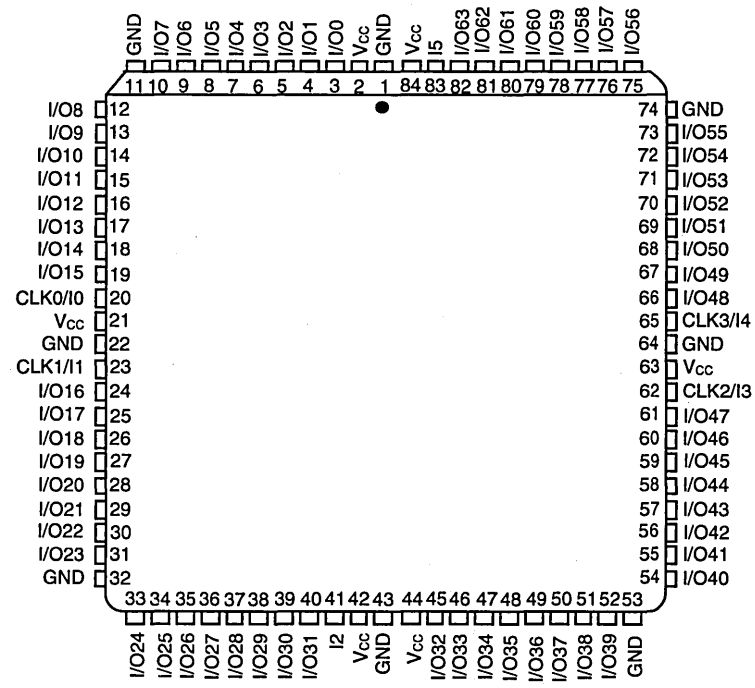


18889C-1

CONNECTION DIAGRAM

Top View

PLCC



18889C-2

Note:
Pin-compatible with MACH130, MACH230, MACH231, and MACH435.

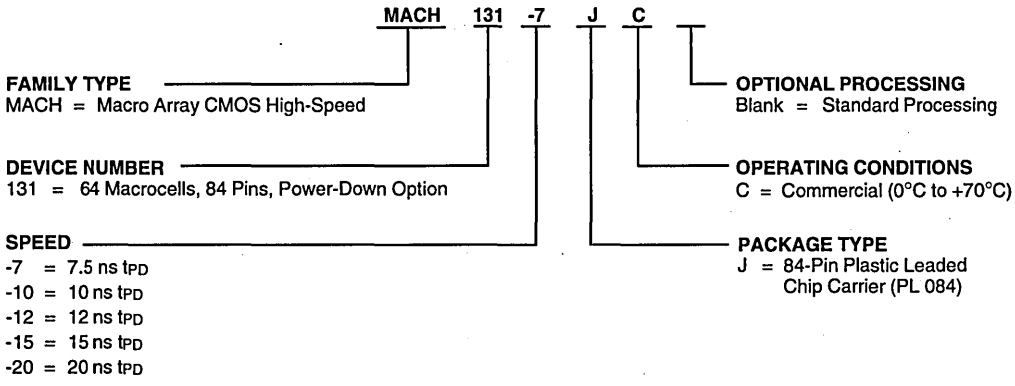
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH131-7	JC
MACH131-10	
MACH131-12	
MACH131-15	
MACH131-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH131 consists of four PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH131 (Figure 1) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the output enable product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH131 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH131 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the output enable product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH131 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7, C_8
M_8	C_7, C_8, C_9
M_9	C_8, C_9, C_{10}
M_{10}	C_9, C_{10}, C_{11}
M_{11}	C_{10}, C_{11}, C_{12}
M_{12}	C_{11}, C_{12}, C_{13}
M_{13}	C_{12}, C_{13}, C_{14}
M_{14}	C_{13}, C_{14}, C_{15}
M_{15}	C_{14}, C_{15}

The Macrocell

The MACH131 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four global clock pins, which are also available as logic inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

Power-Down Mode

The MACH131 features a programmable low-power mode in which individual signal paths can be programmed as low power. These low-power speed paths will be slightly slower than the non-low-power paths. This feature allows speed critical paths to run at maximum frequency while the rest of the paths operate in the low-power mode, resulting in power savings of up to 50%.

The I/O Cell

The I/O cell in the MACH131 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells. Within each PAL block, two product terms are available for selection by the first eight three-state outputs; two other product terms are available for selection by the last eight three-state outputs.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

Bus-Friendly Inputs and I/Os

The MACH131 inputs and I/Os include two inverters in series which loop back to the input. This double inversion reinforces the state of the pin and pulls the voltage away from the input threshold voltage. Unlike a pull-up, this configuration cannot cause contention on a bus. For an illustration of this configuration, please turn to Input and Output equivalent schematics at the end of this data book.

PCI Compliance

The MACH131-7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH231-7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without predictable timing, PCI compliance is dependent upon routing and product term distribution.

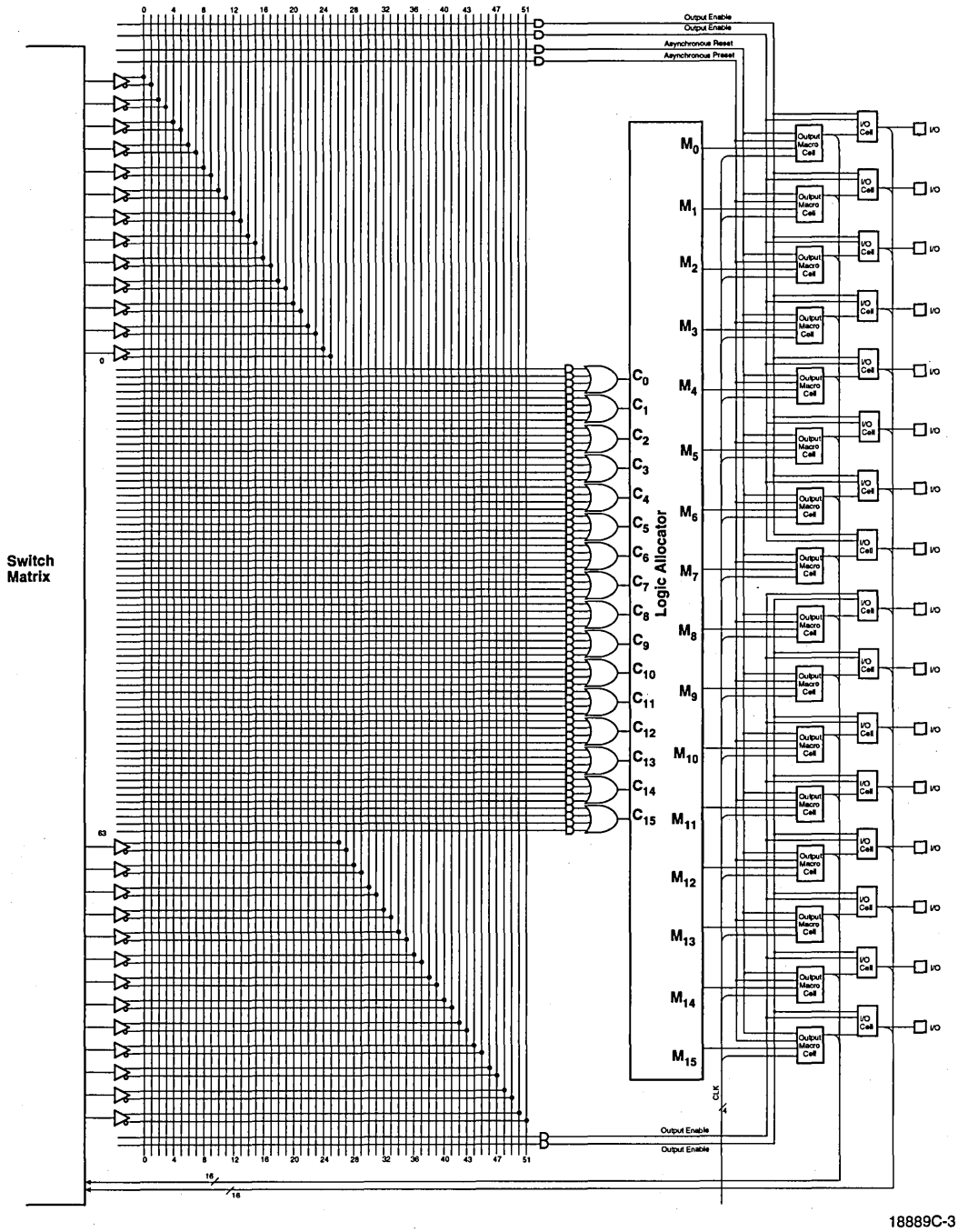


Figure 1. MACH131 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
with Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Static)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		90		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		95		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = V_{CC} - 0.5$ V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-7		-10		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					7.5		10	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	5.5		6.5		ns
				T-type	6.5		7.5		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					5		6	ns
t_{WL}	Clock Width			LOW	3		5		ns
t_{WH}				HIGH	3		5		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	95		80		MHz
				T-type	87		74		MHz
		Internal Feedback (f_{CNT})		D-type	133		100		MHz
				T-type	125		91		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		166.7		100		MHz
t_{AR}	Asynchronous Reset to Registered Output					9.5		11	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				5		7.5		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				5		7.5		ns
t_{AP}	Asynchronous Preset to Registered Output					9.5		11	ns
t_{APW}	Asynchronous Preset Width (Note 1)				5		7.5		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				5		7.5		ns
t_{EA}	Input, I/O, or Feedback to Output Enable					9.5		10	ns
t_{ER}	Input, I/O, or Feedback to Output Disable					9.5		10	ns
t_{LP}	t_{PD} Increase for Powered-Down Macrocell (Note 3)					10		10	ns
t_{LPS}	t_S Increase for Powered-Down Macrocell (Note 3)					7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-Down Macrocell (Note 3)					3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-Down Macrocell (Note 3)					10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Conditions.*
3. *If a signal is powered down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
with Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		90		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		95		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = V_{CC} - 0.5$ V	$V_{CC} = 5.0$ V, $T_A = 25°C$	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	f = 1 MHz	8	pF

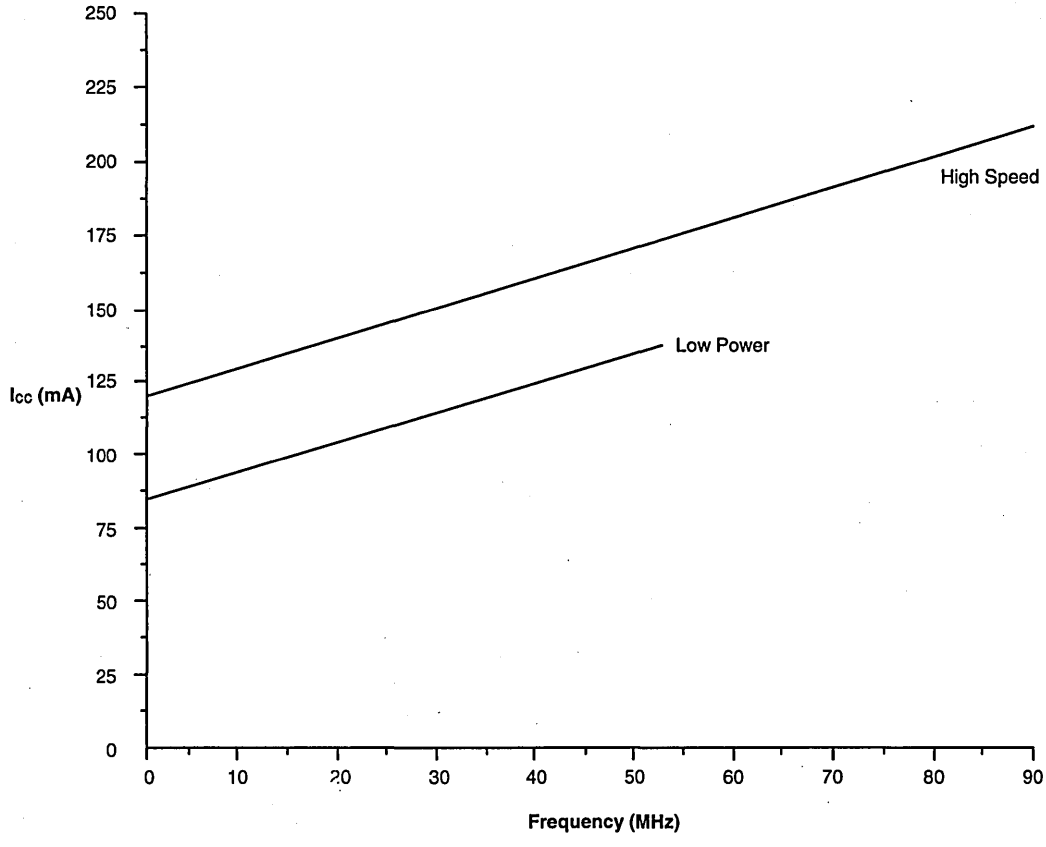
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-15		-20		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	76.8		66.6		47.6		MHz
				T-type	71.4		55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)				12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)				8		10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)				12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)				8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable					12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable					12		15		20	ns
t_{LP}	t_{PD} Increase for Powered-Down Macrocell (Note 3)					10		10		10	ns
t_{LPS}	t_S Increase for Powered-Down Macrocell (Note 3)					7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-Down Macrocell (Note 3)					3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-Down Macrocell (Note 3)					10		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Conditions.*
3. *If a signal is powered down, this parameter must be added to its respective high-speed parameter.*

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



18889C-4

The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

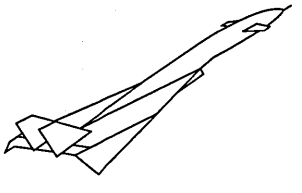
TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		12	°C/W
θ_{ja}	Thermal impedance; junction to ambient		28.1	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	31	°C/W
		400 lfpm air	28	°C/W
		600 lfpm air	26	°C/W
		800 lfpm air	25	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.



FINAL

COM'L: -7/10/12/15/20, Q-12/15/20 IND: -12/14/18/24

MACH210A-7/10/12
MACH210-12/15/20
MACH210AQ-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 64 Macrocells
- 7.5 ns t_{PD} Commercial
  12 ns t_{PD} Industrial
- 133 MHz f_{CNT}
- 38 Inputs; 210A Inputs have built-in pull-up resistors
- Peripheral Component Interconnect (PCI) compliant
- 32 Outputs
- 64 Flip-flops; 2 clock choices
- 4 "PAL22V16" blocks with buried macrocells
- Pin-compatible with MACH110, MACH111, MACH211, and MACH215

GENERAL DESCRIPTION

The MACH210 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH210 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells, including additional buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH210 has two kinds of macrocell: output and buried. The MACH210 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH210 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers or latches for use in synchronizing signals and reducing setup time requirements.

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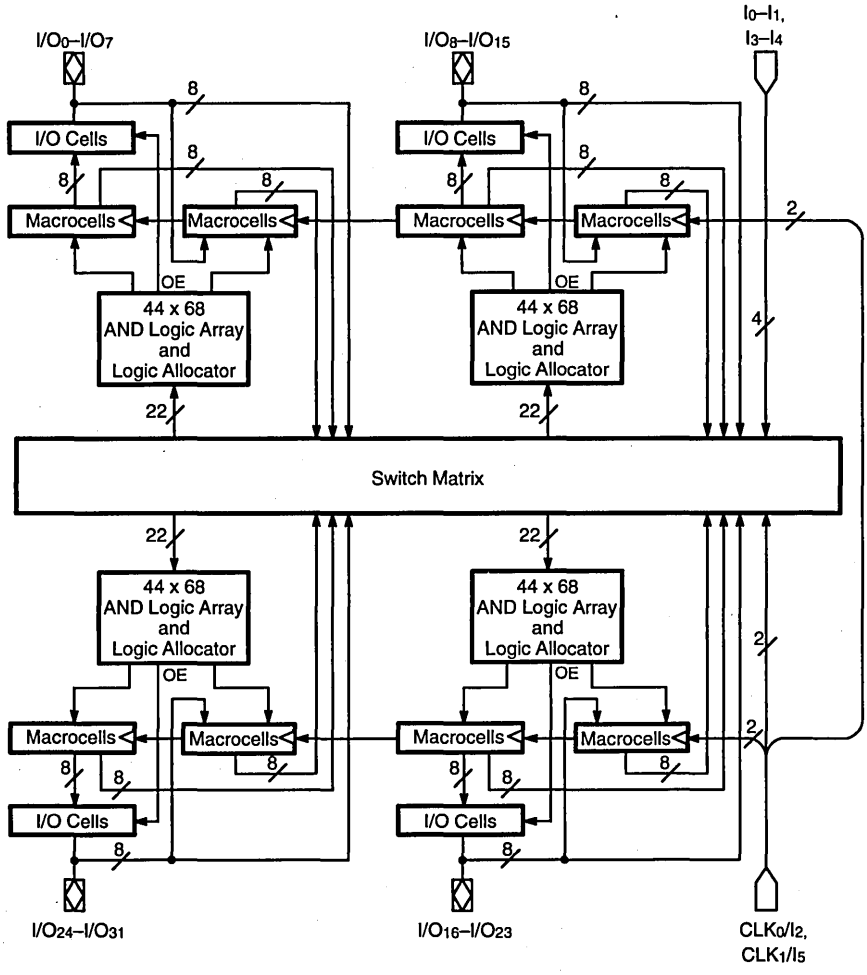
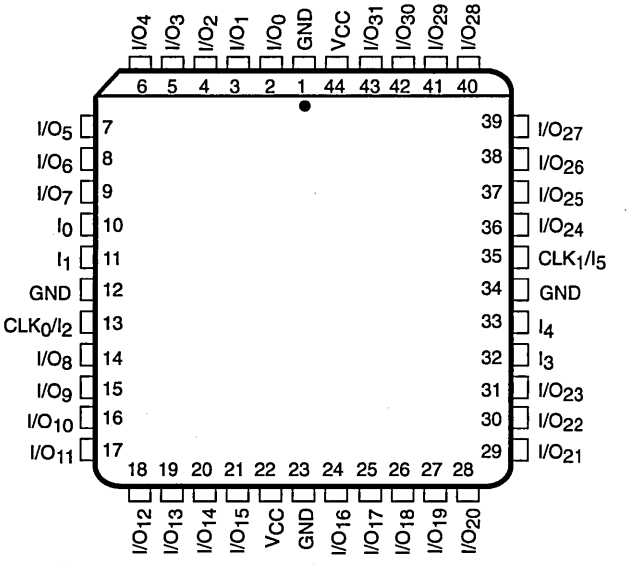
BLOCK DIAGRAM



14128I-1

CONNECTION DIAGRAM
Top View

PLCC

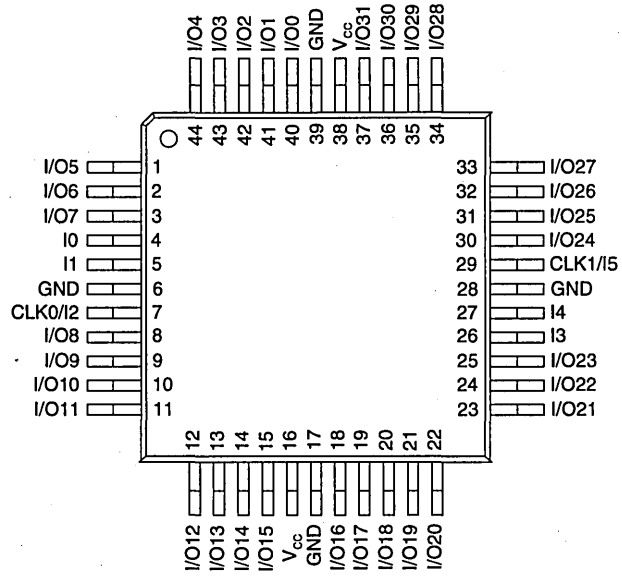


14128I-2

Note:
Pin-compatible with MACH110, MACH111, MACH211, and MACH215.

CONNECTION DIAGRAM
Top View

TQFP



14128I-3

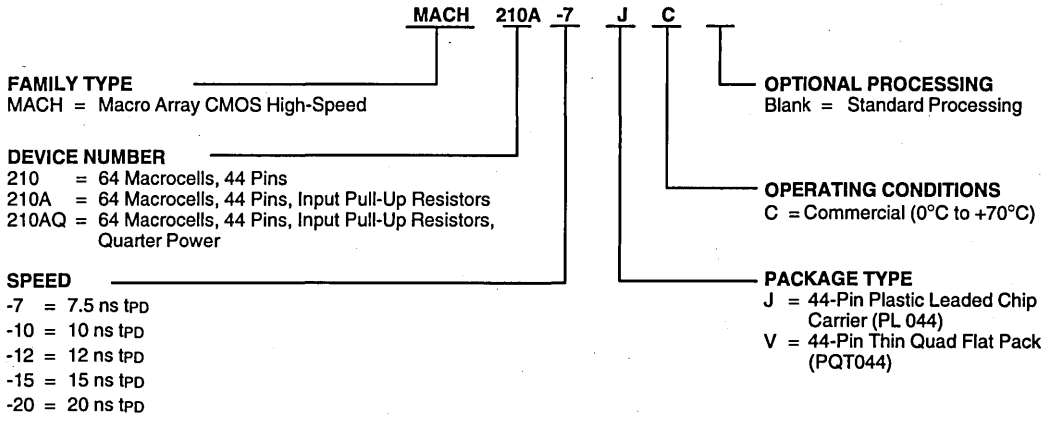
Note:
Pin-compatible with MACH111 and MACH211.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



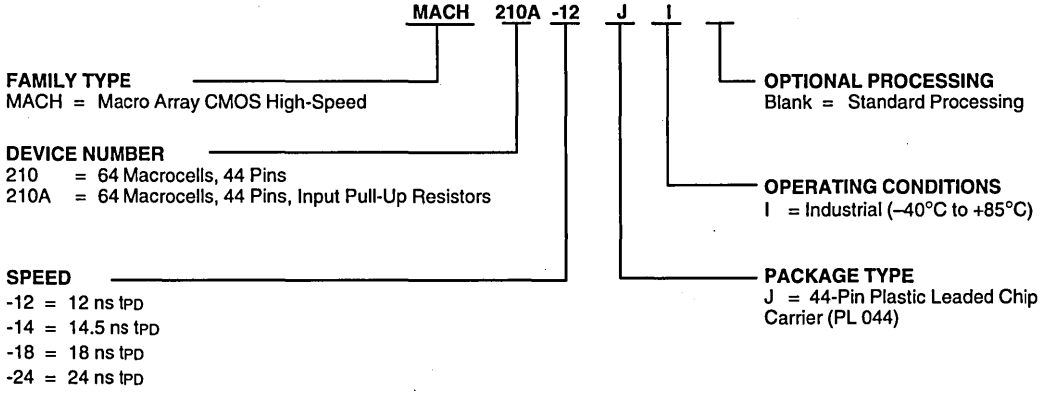
Valid Combinations	
MACH210A-7	JC, VC
MACH210A-10	
MACH210A-12	
MACH210-12	JC
MACH210-15	
MACH210-20	
MACH210AQ-12	
MACH210AQ-15	
MACH210AQ-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH210A-12	JI
MACH210A-14	
MACH210-14	
MACH210-18	
MACH210-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH210 consists of four PAL blocks connected by a switch matrix. There are 32 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs.

The MACH210A inputs and I/O pins have built-in pull-up resistors. While it is always a good design practice to tie unused pins high, the 210A pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH210 (Figure 1) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH210 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-term Array

The MACH210 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable; one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH210 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_{14}		C_{13}, C_{14}, C_{15}
	M_{15}	C_{14}, C_{15}

The Macrocell

The MACH210 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH210 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

PCI Compliance

The MACH210A-7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH210A-7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without predictable timing, PCI compliance is dependent upon routing and product term distribution.

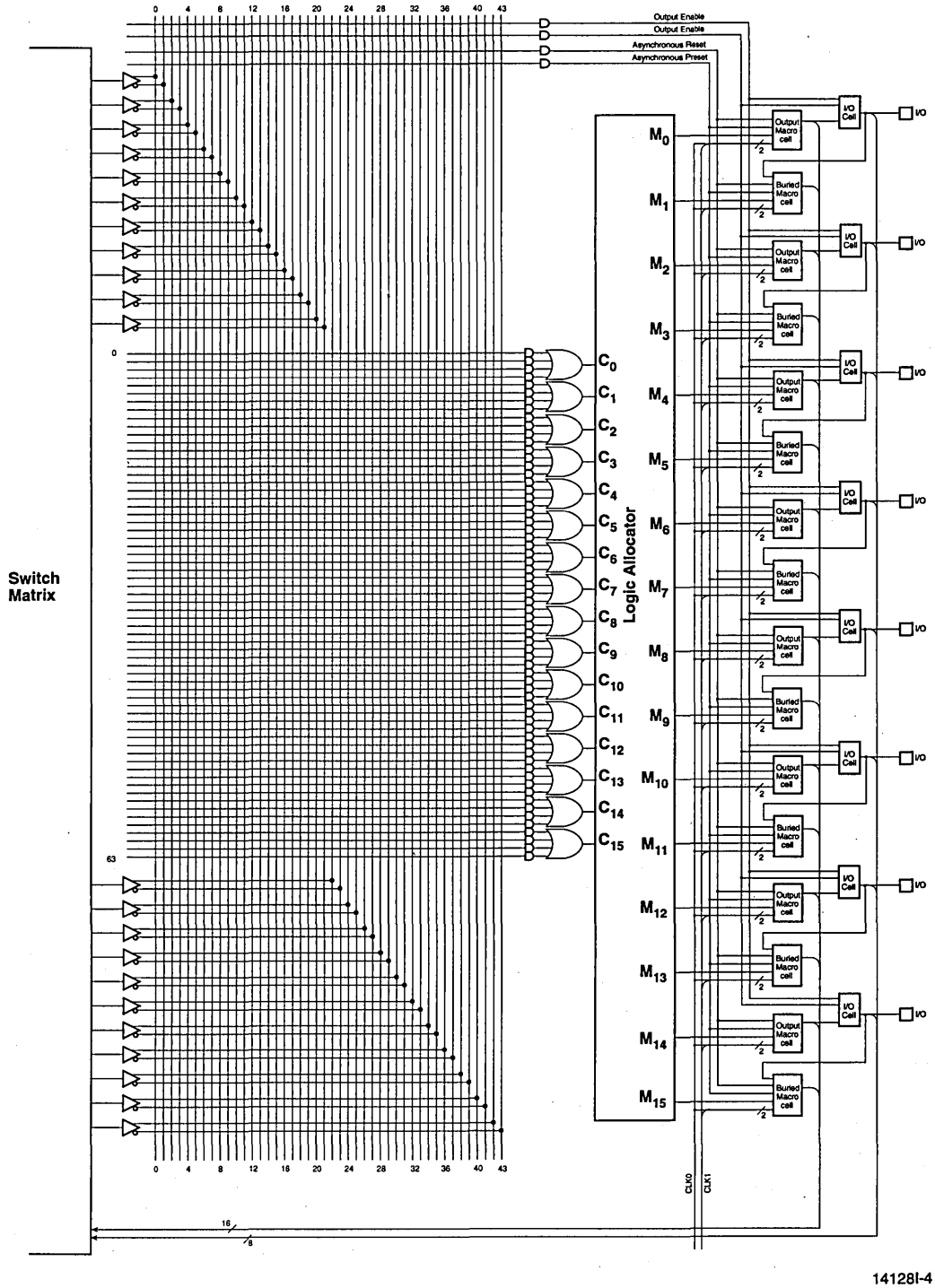


Figure 11. MACH210 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5.0 V, f = 25 MHz, T_A = 25°C (Note 4)		130		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description			-7 Min	-7 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				7.5	ns
t_S	Setup Time from Input, I/O or Feedback to Clock		D-Type	5.5		ns
			T-Type	6.5		ns
t_H	Register Data Hold Time			0		ns
t_{CO}	Clock to Output				5	ns
t_{WL}	Clock Width		LOW	3		ns
t_{WH}			HIGH	3		ns
f_{MAX}	Maximum Frequency	External Feedback	D-Type	100		MHz
			T-Type	91		MHz
		Internal Feedback (f_{CNT})	D-Type	133		MHz
			T-Type	125		MHz
		No Feedback		166.7		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			5.5		ns
t_{HL}	Latch Data Hold Time			0		ns
t_{GO}	Gate to Output				6	ns
t_{GWL}	Gate Width LOW			3		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				9.5	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			2		ns
t_{ICO}	Input Register Clock to Combinatorial Output				11	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-Type	9		ns
			T-Type	10		ns
t_{WICL}	Input Register Clock Width		LOW	3		ns
t_{WICH}			HIGH	3		ns
f_{MAXIR}	Maximum Input Register Frequency			166.7		MHz
t_{SIL}	Input Latch Setup Time			2		ns
t_{HIL}	Input Latch Hold Time			2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				12	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				14	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			7.5		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (continued)

Parameter Symbol	Parameter Description	-7		Unit
		Min	Max	
t_{IGS}	Input Latch Gate to Output Latch Setup	10		ns
t_{WIGL}	Input Latch Gate Width LOW	3		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		11.5	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		12	ns
t_{ARW}	Asynchronous Reset Width	8		ns
t_{ARR}	Asynchronous Reset Recovery Time	8		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		12	ns
t_{APW}	Asynchronous Preset Width	8		ns
t_{APR}	Asynchronous Preset Recovery Time	8		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		7.5	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		7.5	ns

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... −0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	−30		−160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5V, T_A = 25°C, f = 25 MHz (Note 4)		135		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-10 Min	-10 Max	-12 Min	-12 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					10		12	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-Type	6.5		7		ns
				T-Type	7.5		8		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					6		8	ns
t_{WL}	Clock Width			LOW	5		6		ns
t_{WH}				HIGH	5		6		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-Type	80		66.7		MHz
				T-Type	74		62.5		MHz
		Internal Feedback (f_{CNT})		D-Type	100		83.3		MHz
				T-Type	91		76.9		MHz
		No Feedback	$1/(t_S + t_H)$		100		83.3		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				6.5		7		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					7		10	ns
t_{GWL}	Gate Width LOW				5		6		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					12		14	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				2		2		ns
t_{ICO}	Input Register Clock to Combinatorial Output					13		15	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-Type	10		12		ns
				T-Type	11		13		ns
t_{WICL}	Input Register Clock Width			LOW	5		6		ns
t_{WICH}				HIGH	5		6		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		100		83.3		MHz
t_{SIL}	Input Latch Setup Time				2		2		ns
t_{HIL}	Input Latch Hold Time				2		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					14		17	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					16		19	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				8.5		9		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				11		13		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-10		-12		Unit
		Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	5		6		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		14		16	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		25		16	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	10		12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	10		8		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		15		16	ns
t_{APW}	Asynchronous Preset Width (Note 1)	10		12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	10		8		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		10		12	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		10		12	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 16 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Temperature (T_A) Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5V, T_A = 25°C, f = 25 MHz (Note 4)		135		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-14		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		14.5	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-Type	8		8.5		ns
				T-Type	9		10		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					7.5		10	ns
t_{WL}	Clock Width			LOW	6		7.5		ns
t_{WH}				HIGH	6		7.5		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-Type	64		53		MHz
				T-Type	59		50		MHz
		Internal Feedback (f_{CNT})		D-Type	80		61.5		MHz
				T-Type	72.5		57		MHz
		No Feedback	$1/(t_S + t_H)$		80		66.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				8		8.5		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					8.5		12	ns
t_{GWL}	Gate Width LOW				6		7.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14.5		17	ns
t_{SIR}	Input Register Setup Time				2.5		2.5		ns
t_{HIR}	Input Register Hold Time				3		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					16		18	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-Type	12		14.5		ns
				T-Type	13		16		ns
t_{WICL}	Input Register Clock Width			LOW	6		7.5		ns
t_{WICH}				HIGH	6		7.5		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			80		66.5		MHz
t_{SIL}	Input Latch Setup Time				2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				3		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		20.5	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19.5		23	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				10.5		11		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				13.5		16		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-12		-14		Unit
		Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	6		7.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		17		19.5	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		19.5		19.5	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		14.5		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	12		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		18		19.5	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		14.5		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	12		10		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		12		14.5	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		12		14.5	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 16 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5V, T_A = 25°C, f = 25 MHz (Note 4)		120		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-15		-20		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	83.3		66.6		50		MHz
				T-type	76.9		62.5		47.6		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				7		10		13		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output (Note 3)					10		11		12	ns
t_{GWL}	Gate Width LOW				6		6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14		17		22	ns
t_{SIR}	Input Register Setup Time				2		2		2		ns
t_{HIR}	Input Register Hold Time				2		2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					15		18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	12		15		20		ns
				T-type	13		16		21		ns
t_{WICL}	Input Register Clock Width			LOW	6		6		8		ns
t_{WICH}				HIGH	6		6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			83.3		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		2		ns
t_{HIL}	Input Latch Hold Time				2		2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19		22		27	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				9		12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				13		16		21		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	6		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		12		15		20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 16 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = –40°C to +85°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		120		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-14		-18		-24		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					14.5		18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	8.5		12		16		ns
				T-type	10		13.5		17		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12		14.5	ns
t_{WL}	Clock Width			LOW	7.5		7.5		10		ns
t_{WH}				HIGH	7.5		7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	53		40		32		MHz
				T-type	50		38		30.5		MHz
		Internal Feedback (f_{CNT})		D-type	61.5		53		38		MHz
				T-type	57		44		34.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		66.5		66.5		50		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				8.5		12		16		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output (Note 3)					12		13.5		14.5	ns
t_{GWL}	Gate Width LOW				7.5		7.5		10		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		20.5		26.5	ns
t_{SIR}	Input Register Setup Time				2.5		2.5		2.5		ns
t_{HIR}	Input Register Hold Time				3		3.5		4		ns
t_{ICO}	Input Register Clock to Combinatorial Output					18		22		28	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	14.5		18		24		ns
				T-type	16		19.5		25.5		ns
t_{WICL}	Input Register Clock Width			LOW	7.5		7.5		10		ns
t_{WICH}				HIGH	7.5		7.5		10		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			66.5		66.5		50		MHz
t_{SIL}	Input Latch Setup Time				2.5		2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				3		3.5		4		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					20.5		24		30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					23		26.5		32.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				11		14.5		18		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				16		19.5		25.5		ns
t_{WIGL}	Input Latch Gate Width LOW				7.5		7.5		10		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches					19.5		23		29	ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-14		-18		-24		Unit
		Min	Max	Min	Max	Min	Max	
t_{AR}	Asynchronous Reset to Registered or Latched Output		19.5		24		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	14.5		18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	10		12		18		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		19.5		24		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)	14.5		18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	10		12		18		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		14.5		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		14.5		18		24	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 16 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		45		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-12 Min	-12 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				12	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock		D-type	12		ns
			T-type	13		ns
t_H	Register Data Hold Time			0		ns
t_{CO}	Clock to Output				6	ns
t_{WL}	Clock Width		LOW	6		ns
t_{WH}			HIGH	6		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	D-type	55.6		MHz
			T-type	52.6		MHz
		Internal Feedback (f_{CNT})	D-type	83.3		MHz
			T-type	76.9		MHz
		No Feedback		83.3		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			12		ns
t_{HL}	Latch Data Hold Time			0		ns
t_{GO}	Gate to Output				7	ns
t_{GWL}	Gate Width LOW			6		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				14	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			2.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output				17	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-type	15		ns
			T-type	16		ns
t_{WICL}	Input Register Clock Width		LOW	6		ns
t_{WICH}			HIGH	6		ns
f_{MAXIR}	Maximum Input Register Frequency			83.3		MHz
t_{SIL}	Input Latch Setup Time			2		ns
t_{HIL}	Input Latch Hold Time			2.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				19	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				20	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			13		ns
t_{IGS}	Input Latch Gate to Output Latch Setup			16		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-12		Unit
		Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	6		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		18	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		24	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	19		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	19		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		24	ns
t_{APW}	Asynchronous Preset Width (Note 1)	19		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	19		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		12	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		12	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5V, T_A = 25°C, f = 25 MHz (Note 4)		45		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		17		ns
				T-type	14		18		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					7		8	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	1/(t_S + t_{CO})	D-type	50		40		MHz
				T-type	47.6		38.4		MHz
		Internal Feedback (f_{CNT})		D-type	58.8		45.4		MHz
				T-type	55.5		43.4		MHz
		No Feedback	1/(t_S + t_H)	D-type	76.9		58.8		MHz
				T-type	71.4		55.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				13		17		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					8		8	ns
t_{GWL}	Gate Width LOW				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	17		22		ns
				T-type	18		23		ns
t_{WICL}	Input Register Clock Width			LOW	6		8		ns
t_{WICH}				HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	1/(t_{WICL} + t_{WICH})			83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		ns
t_{HIL}	Input Latch Hold Time				2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					22		27	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				15		19		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				18		23		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-15		-20		Unit
		Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		25		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	20		25		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	20		25		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		25		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)	20		25		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	20		25		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		15		20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 16 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = –40°C to +85°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		45		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-18		-24		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	16		20.5		ns
				T-type	17		22		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					8.5		10	ns
t_{WL}	Clock Width			LOW	7.5		10		ns
t_{WH}				HIGH	7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		32		MHz
				T-type	38		30.5		MHz
		Internal Feedback (f_{CNT})		D-type	47		36		MHz
				T-type	44		34.5		MHz
		No Feedback	$1/(t_S + t_H)$	D-type	61.5		47		MHz
				T-type	57		47		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				16		20.5		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					10		10	ns
t_{GWL}	Gate Width LOW				7.5		10		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					20.5		26.5	ns
t_{SIR}	Input Register Setup Time				2.5		2.5		ns
t_{HIR}	Input Register Hold Time				3.5		4		ns
t_{ICO}	Input Register Clock to Combinatorial Output					22		28	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	20.5		26.5		ns
				T-type	22		28		ns
t_{WICL}	Input Register Clock Width			LOW	7.5		10		ns
t_{WICH}				HIGH	7.5		10		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			66.5		50		MHz
t_{SIL}	Input Latch Setup Time				2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				3.5		4		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					24		30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					26.5		32.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				18		23		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				22		28		ns
t_{WIGL}	Input Latch Gate Width LOW				7.5		10		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches					23		29	ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2) (continued)

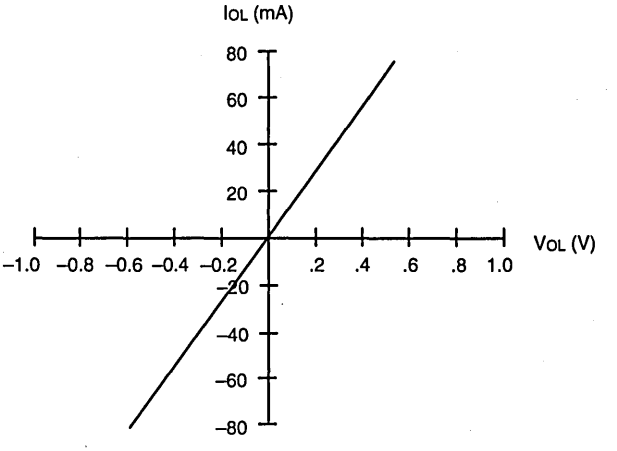
Parameter Symbol	Parameter Description	-18		-24		Unit
		Min	Max	Min	Max	
t_{AR}	Asynchronous Reset to Registered or Latched Output		30		36	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	24		30		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	24		30		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		30		36	ns
t_{APW}	Asynchronous Preset Width (Note 1)	24		30		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	24		30		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		18		24	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Parameters measured with 16 outputs switching.*

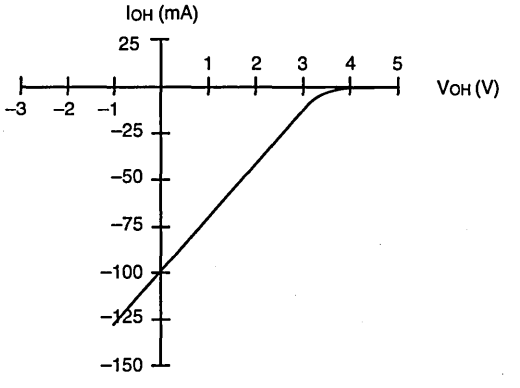
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



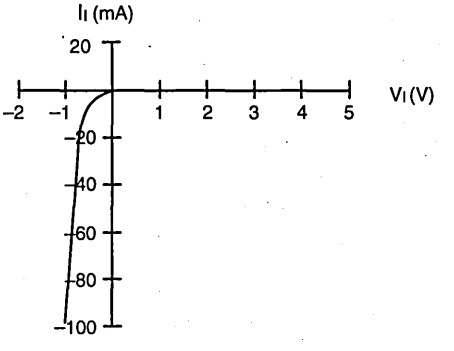
14128I-5

Output, LOW



14128I-6

Output, HIGH

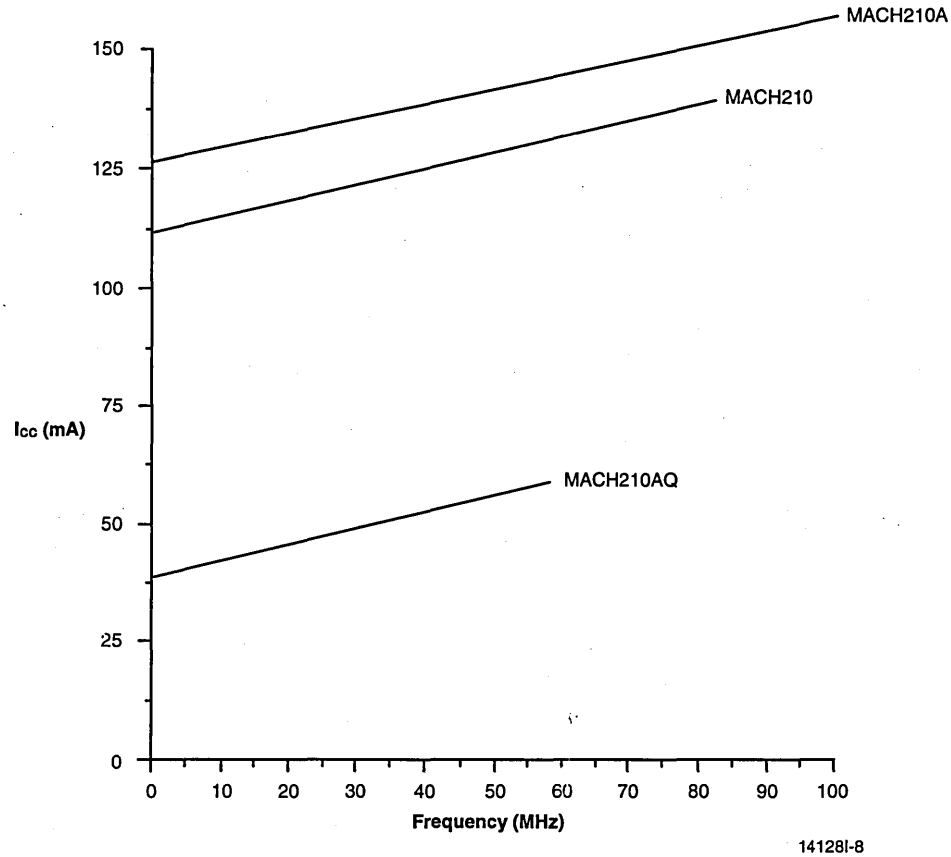


14128I-7

Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			TQFP	PLCC	
θ_{jc}	Thermal impedance, junction to case		11.3	15	°C/W
θ_{ja}	Thermal impedance, junction to ambient		41	40	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	35	36	°C/W
		400 lfpm air	33.7	33	°C/W
		600 lfpm air	32.6	31	°C/W
		800 lfpm air	32	29	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

FINAL COM'L: -12/15/20 IND: -18/24

MACHLV210-12/15/20

High Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Low-voltage operation, 3.3-V JEDEC compatible**
  - — V_{CC} = +3.0 V to +3.6 V
- **< 5 mA standby current**
- **Patented design allows minimal standby current without speed degradation**
- **Exclusively designed for 3.3-V applications**
- **44 Pins**
- **64 Macrocells**
- **12 ns t_{PD} Commercial**
  18 ns t_{PD} Industrial
- **83.3 MHz f_{CNT}**
- **38 Bus-Friendly Inputs**
- **32 Outputs**
- **64 Flip-flops; 2 clock choices**
- **4 "PAL22V16" blocks with buried macrocells**
- **Pin-, function-, and JEDEC-compatible with MACH210**
- **Pin-compatible with MACH110, MACH111, MACH210, MACH211, and MACH215**

GENERAL DESCRIPTION

The MACHLV210 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell. It is architecturally identical to the MACH210, with the addition of I/O pull-up/pull-down resistors and low-voltage, low-power operation.

The MACHLV210 provides 3.3-V operation with low-power CMOS technology. AMD's patented design allows for minimal standby current without speed degradation by limiting the leakage current when signals are not switching. At less than 5 mA maximum standby current, the MACHLV210 is ideal for low-power applications.

The MACHLV210 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells, including additional buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACHLV210 has two kinds of macrocell: output and buried. The MACHLV210 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACHLV210 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers or latches for use in synchronizing signals and reducing setup time requirements.

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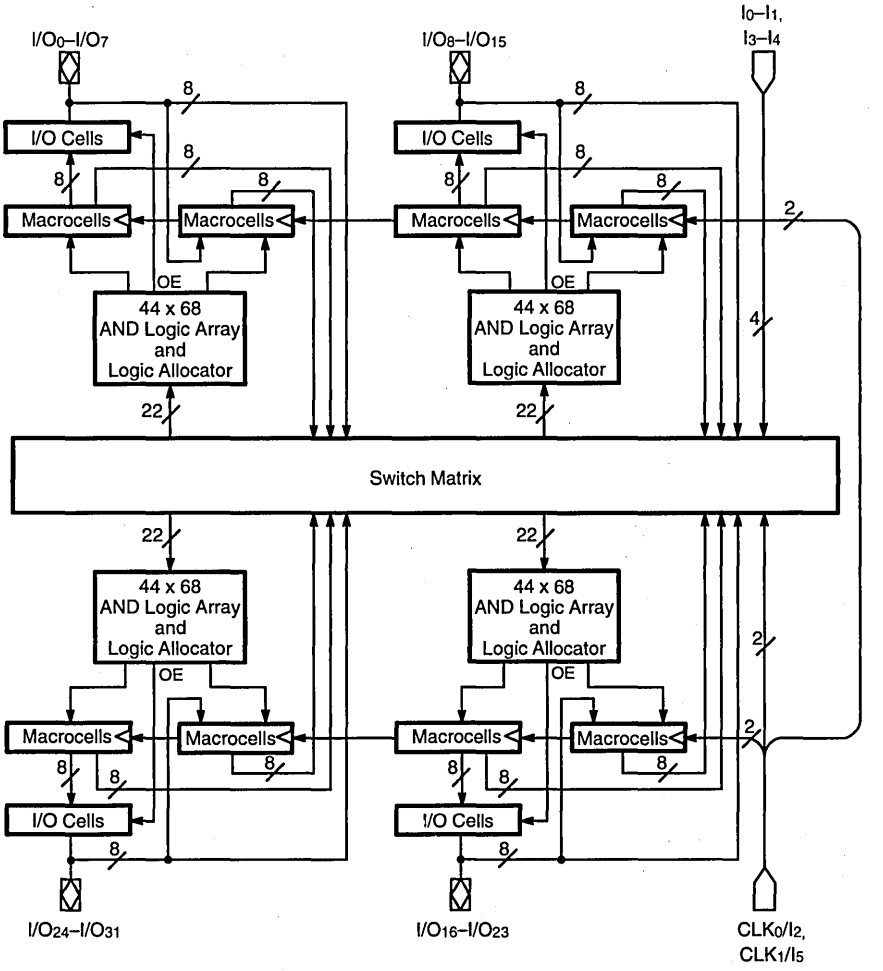
Issue Date: May 1995

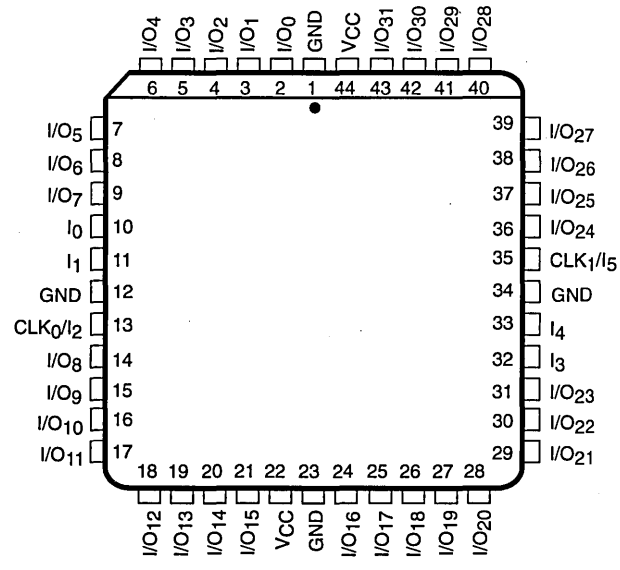
BLOCK DIAGRAM



17908D-1

CONNECTION DIAGRAM
Top View

PLCC



17908D-2

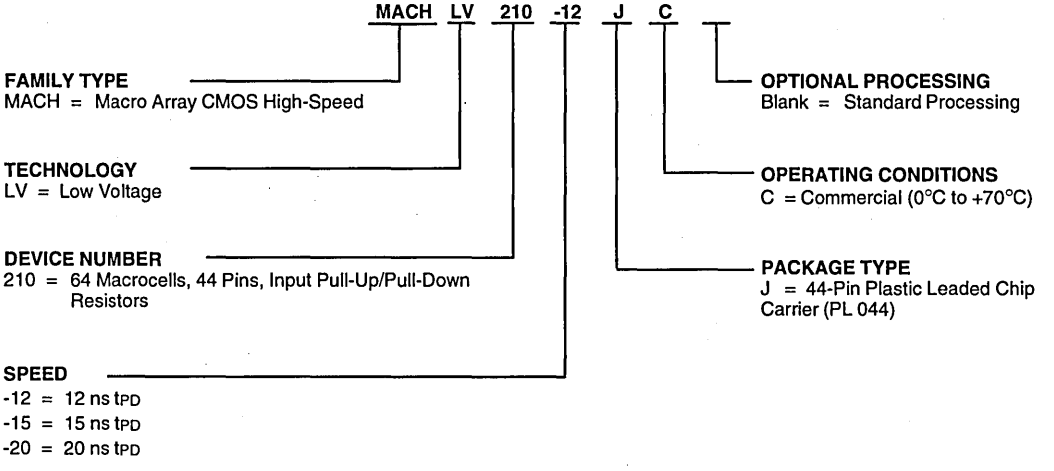
Note:
Pin-compatible with: MACH110, MACH111, MACH210, MACH211, and MACH215.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



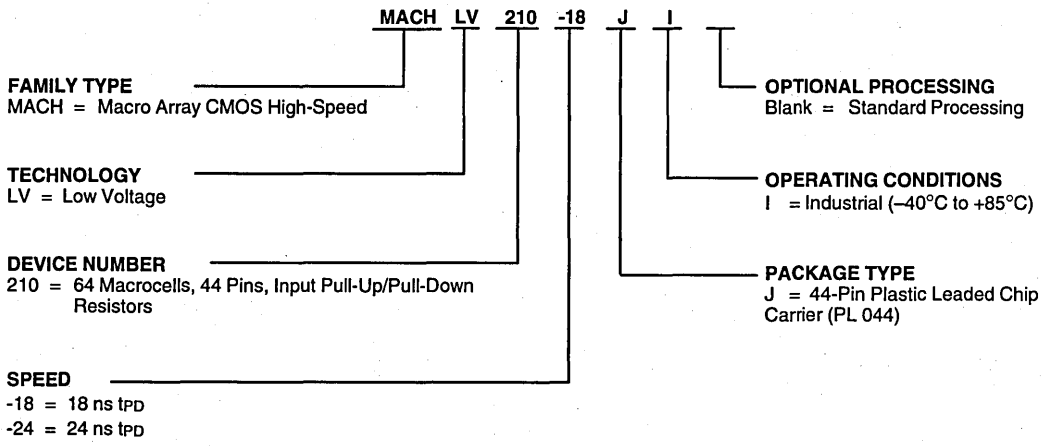
Valid Combinations	
MACHLV210-12	JC
MACHLV210-15	
MACHLV210-20	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACHLV210-18	JI
MACHLV210-24	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACHLV210 consists of four PAL blocks connected by a switch matrix. There are 32 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs.

The MACHLV210 inputs and I/O pins have advanced pull-up/pull-down resistors that enable the inputs to be pulled to the last driven state. While it is always a good design practice to tie unused pins high or low, the MACHLV210 pull-up/pull-down resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACHLV210 (Figure 1) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACHLV210 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-term Array

The MACHLV210 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable; one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACHLV210 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_{14}		C_{13}, C_{14}, C_{15}
	M_{15}	C_{14}, C_{15}

The Macrocell

The MACHLV210 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACHLV210 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

Benefits of Lower Operating Voltage

The MACHLV210 has an operating voltage range of 3.0 V to 3.6 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for portable applications.

Because power is proportional to the square of the voltage, reduction of the supply voltge from 5.0 V to 3.3 V significantly reduces power consumption. This directly translates to longer battery life for portable applications.

Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3-V designs facilitate a reduction in the form factor.

The MACHLV210 is not designed to interface between 3.3-V and 5.0-V logic. Latch-up may occur if V_{OH} for the MACHLV210 is greater than V_{IH} for the 5.0-V device. Although this scenario is unlikely, interfacing the MACHLV210 with 5.0-V devices is not encouraged without necessary latch-up design precautions.

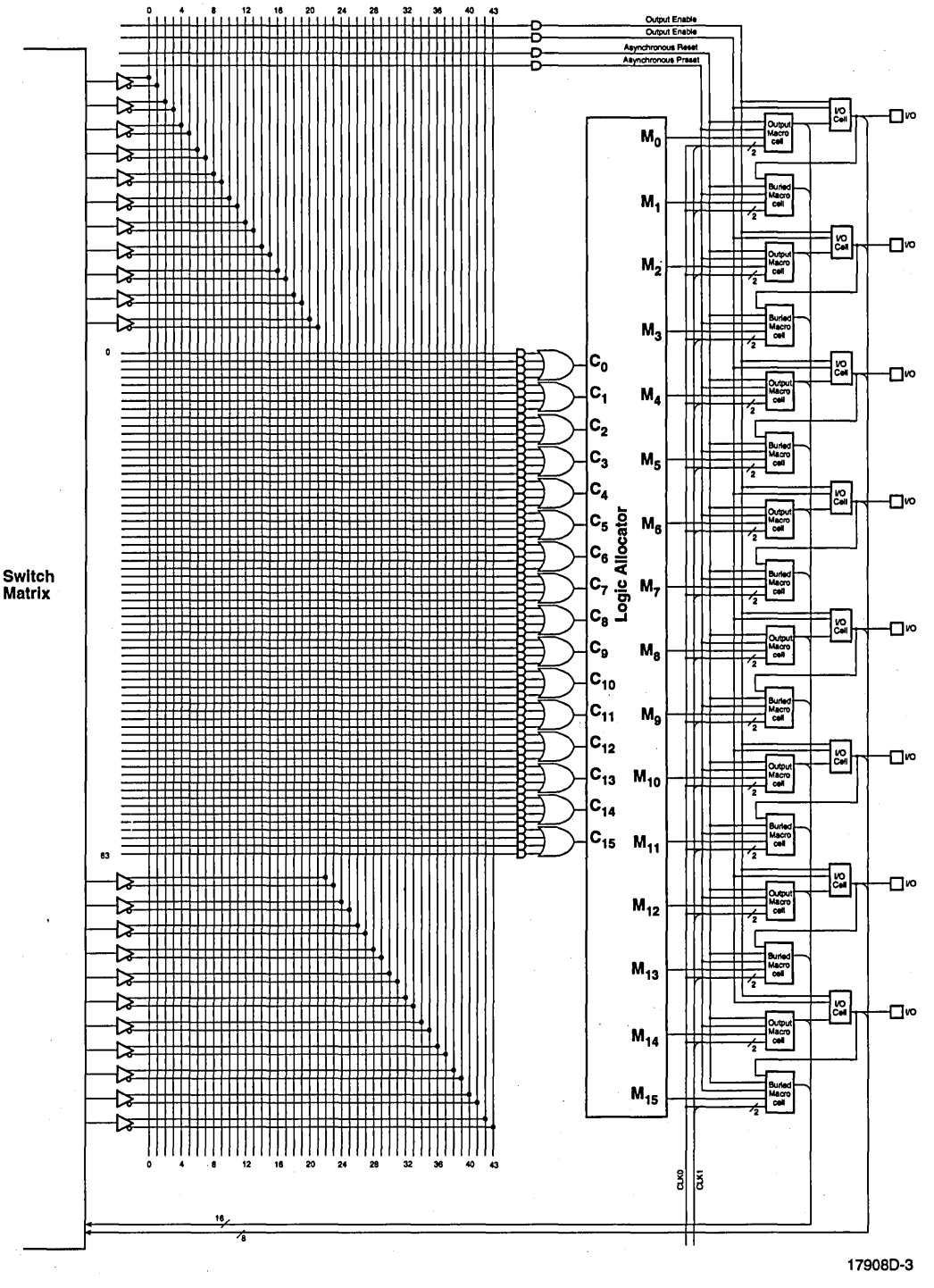


Figure 1. MACHLV210 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +5.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}				0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 3.3 V, T_A = 25°C, (Note 4)	f = 0 MHz		2		mA
			f = 25 MHz		60		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-12 Min	-12 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				12	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock		D-type	9		ns
			T-type	10		ns
t_H	Register Data Hold Time			0		ns
t_{CO}	Clock to Output				8	ns
t_{WL}	Clock Width		LOW	5		ns
t_{WH}			HIGH	6		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	D-type	58.8		MHz
			T-type	55.6		MHz
		Internal Feedback (f_{CNT})	D-type	83.3		MHz
			T-type	76.9		MHz
		No Feedback (f_{CNT})		90.9		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			9		ns
t_{HL}	Latch Data Hold Time			0		ns
t_{GO}	Gate to Output				9	ns
t_{GWL}	Gate Width LOW			5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				15	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			1.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output				15	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-type	12		ns
			T-type	13		ns
t_{WICL}	Input Register Clock Width		LOW	5		ns
t_{WICH}			HIGH	6		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$		90.9		MHz
t_{SIL}	Input Latch Setup Time			2		ns
t_{HIL}	Input Latch Hold Time			1.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				17	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				19	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			10		ns
t_{IGS}	Input Latch Gate to Output Latch Setup			13		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-12		Unit
		Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		17	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		16	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	12		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		16	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		12	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		12	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +5.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}				0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 3.3 V, T_A = 25°C (Note 4)	f = 0 MHz		2		mA
			f = 25 MHz		60		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		14		ns
				T-type	11		15		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	5		7		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	50		38.5		MHz
				T-type	47.6		37		MHz
		Internal Feedback (f_{CNT})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		90.9		66.7		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				10		14		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					11		15	ns
t_{GWL}	Gate Width LOW				5		7		ns
t_{PDL}	Input, I/O, or Feedback to Output Through					17		23	ns
t_{SIR}	Input Register Setup Time				2.5		3		ns
t_{HIR}	Input Register Hold Time				1.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					18		24	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	13		27		ns
				T-type	14		20		ns
t_{WICL}	Input Register Clock Width			LOW	5		7		ns
t_{WICH}				HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			90.9		66.7		MHz
t_{SIL}	Input Latch Setup Time				2.5		3		ns
t_{HIL}	Input Latch Hold Time				1.5		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					19		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					22		29	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				12		16		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				14		18		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-15		-20		Unit
		Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	5		7		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		21		28	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		20		26	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		20		26	ns
t_{APW}	Asynchronous Preset Width (Note 1)	15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		15		20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *Parameters measured with 16 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +5.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = –40°C to +85°C) .... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Temperature (T_A) Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}				0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 3.3 V, T_A = 25°C (Note 4)	f = 0 MHz		2		mA
			f = 25 MHz		60		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance		8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-18 Min	-18 Max	-24 Min	-24 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	12		17		ns
				T-type	13.5		18		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					12		14.5	ns
t_{WL}	Clock Width			LOW	6		8.5		ns
t_{WH}				HIGH	7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		30.5		MHz
				T-type	38		29.5		MHz
		Internal Feedback (f_{CNT})		D-type	53		40		MHz
				T-type	50		38		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		72.5		53		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				12		17		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					13.5		18	ns
t_{GWL}	Gate Width LOW				6		8.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Latch					20.5		28	ns
t_{SIR}	Input Register Setup Time				3		4		ns
t_{HIR}	Input Register Hold Time				2.5		4		ns
t_{ICO}	Input Register Clock to Combinatorial Output					22		29	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	16		32.5		ns
				T-type	17		24		ns
t_{WICL}	Input Register Clock Width			LOW	6		8.5		ns
t_{WICH}				HIGH	7.5		10		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		72.5		53		MHz
t_{SIL}	Input Latch Setup Time				3		4		ns
t_{HIL}	Input Latch Hold Time				2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					23		30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					26.5		34.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				14.5		19.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				17		22		ns

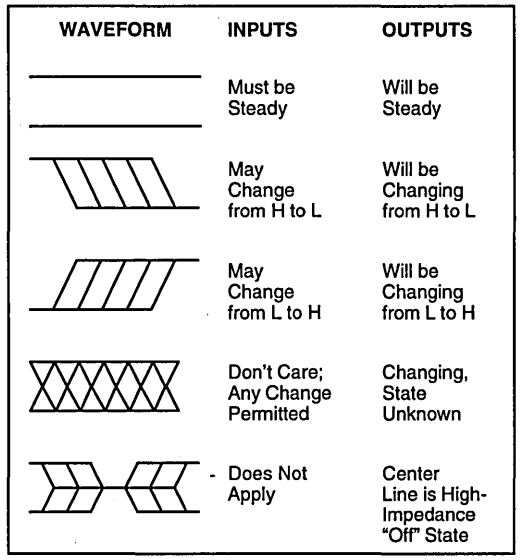
SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-18		-24		Unit
		Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	6		8.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		25.5		34	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		24		31.5	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	18		24		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		24		31.5	ns
t_{APW}	Asynchronous Preset Width (Note 1)	18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	18		24		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		18		24	ns

Notes:

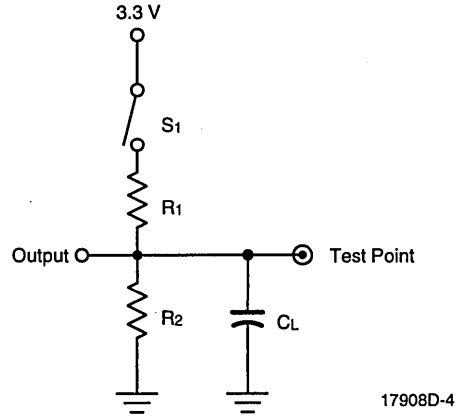
1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit at the back of this Data Book for test conditions.*
3. *Parameters measured with 16 outputs switching.*

KEYS TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT*



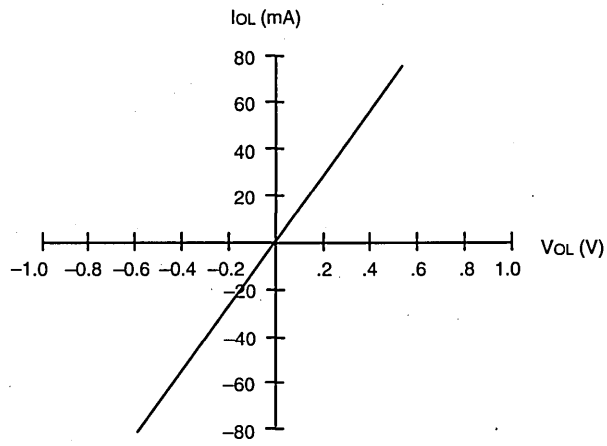
17908D-4

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	30 pF	1.6 K	1.6 K	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

**Switching several outputs simultaneously should be avoided for accurate measurement.*

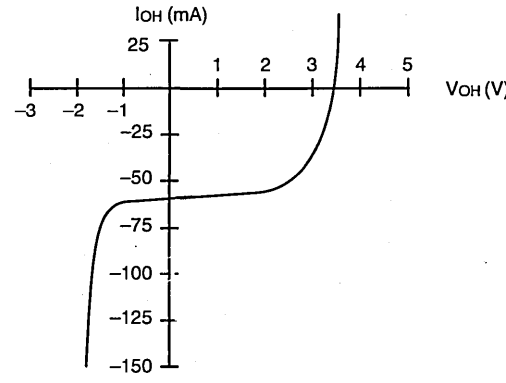
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 3.3 V, T_A = 25°C



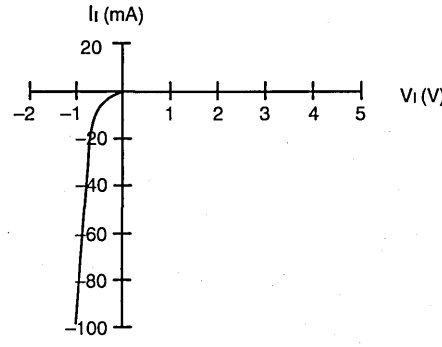
Output, LOW

17908D-5



17908D-6

Output, HIGH

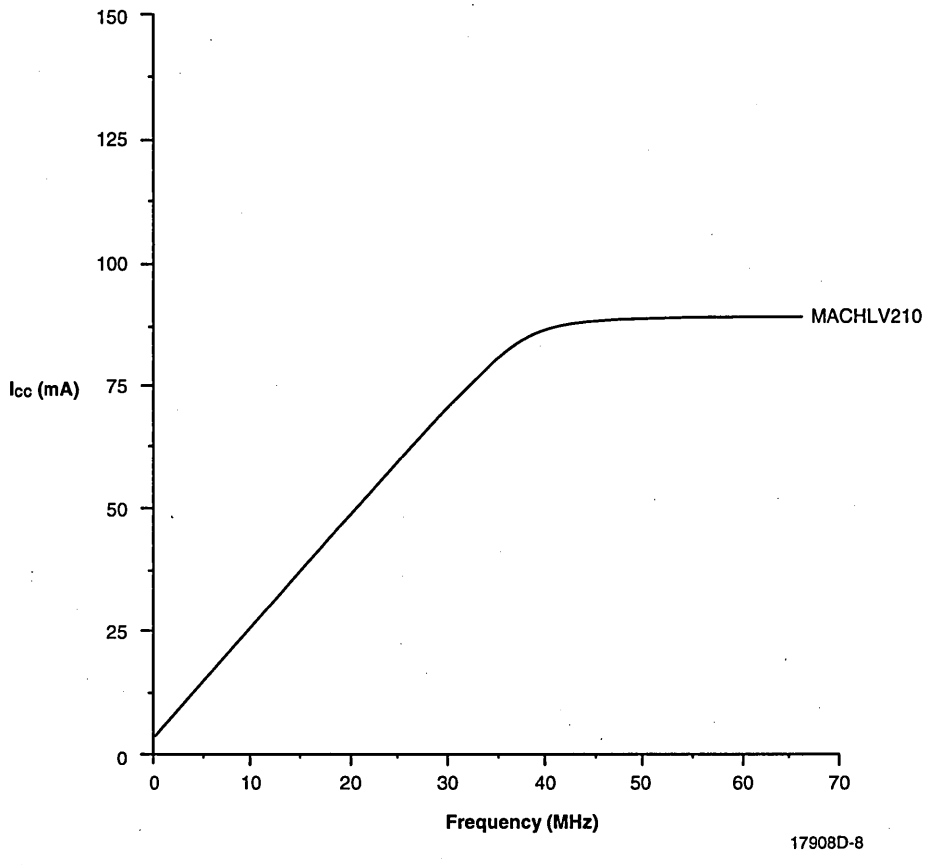


17908D-7

Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 3.3 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

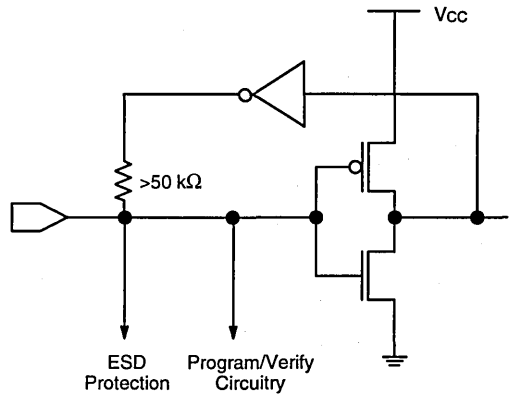
Maximum frequency shown uses internal feedback and a D-type register.

ENDURANCE CHARACTERISTICS

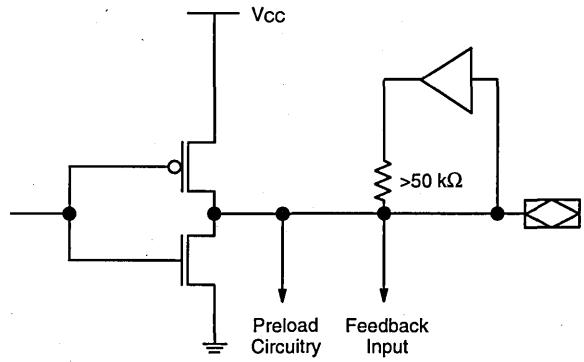
The MACHLV210 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

Parameter Symbol	Parameter Description	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Max Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



Output

17908D-9

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Units
θ_{jc}	Thermal impedance, junction to case		15	°C/W
θ_{ja}	Thermal impedance, junction to ambient		40	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	36	°C/W
		400 lfpm air	33	°C/W
		600 lfpm air	31	°C/W
		800 lfpm air	29	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

PRELIMINARY | COM'L: -7.5/10/12/15/20

MACH211-7/10/12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 64 Macrocells
- 7.5 ns t_{PD}
- 133 MHz f_{CNT}
- 38 Bus-Friendly inputs
- Peripheral Component Interconnect (PCI) compliant
- Programmable power-down mode
- 32 Outputs
- 64 Flip-flops; 4 clock choices
- 4 "PAL26V16" blocks with buried macrocells
- Pin-compatible with MACH110, MACH111, MACH210, MACH215
- Improved routing over the MACH210

GENERAL DESCRIPTION

The MACH211 is a member of AMD's EE CMOS Performance Plus MACH 2 device family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH211 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL26V16" structures complete with product-term arrays and programmable macrocells, which can be programmed as high speed or low power, and buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

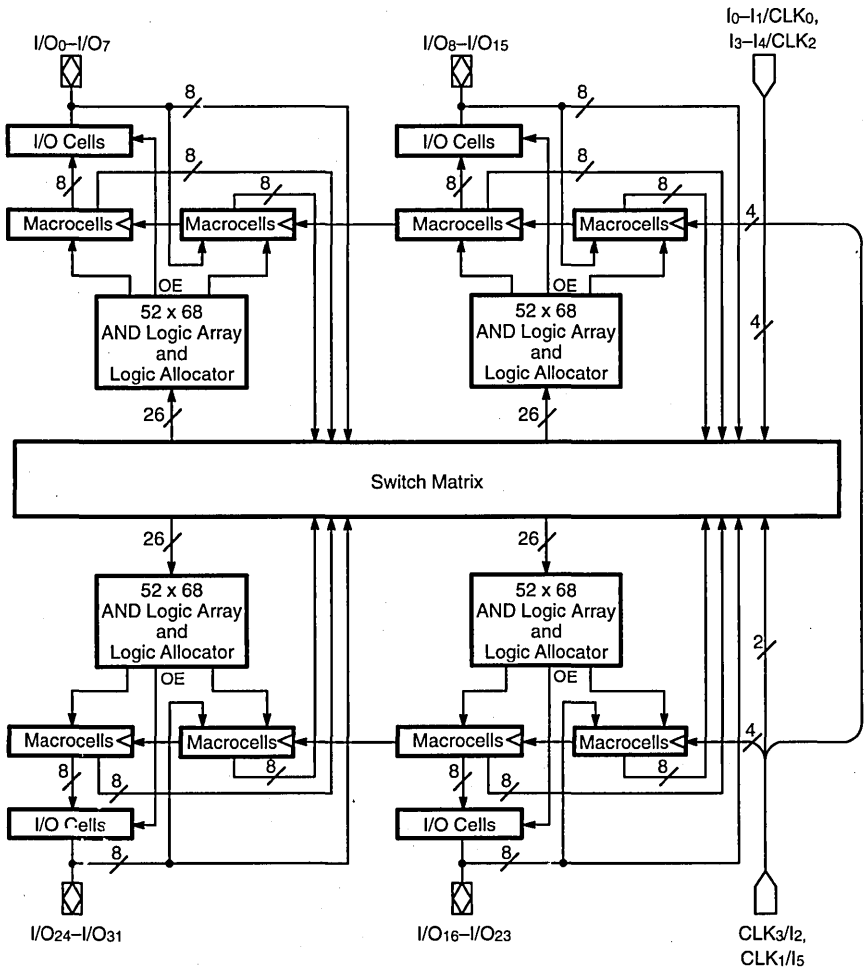
The MACH211 has two kinds of macrocell: output and buried. The MACH211 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH211 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers or latches for use in synchronizing signals and reducing setup time requirements.

Publication# 19601 Rev. A Amendment/0
Issue Date: May 1995

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

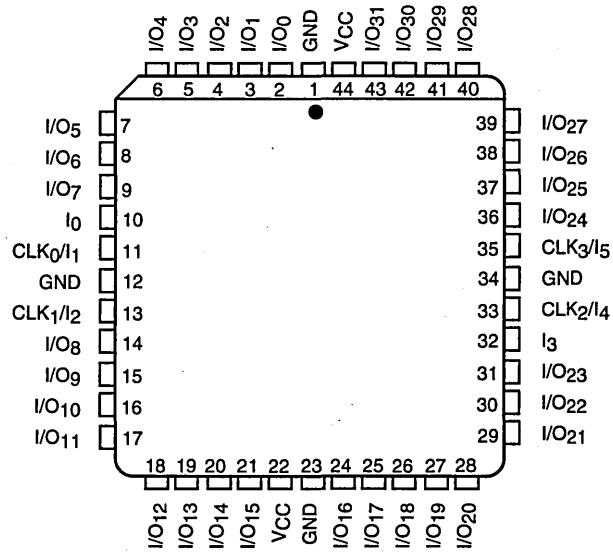
BLOCK DIAGRAM



19601A-1

CONNECTION DIAGRAM
Top View

PLCC

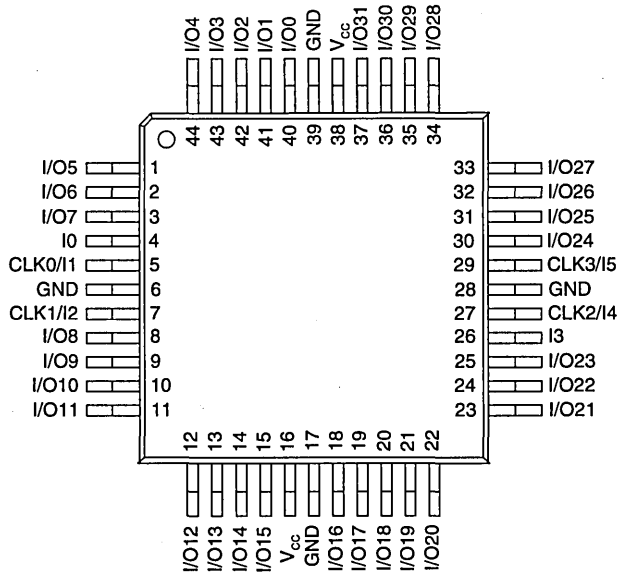


19601A-2

Note:
Pin-compatible with MACH110, MACH111, MACH210, and MACH215.

CONNECTION DIAGRAM
Top View

TQFP



19601A-3

Note:
Pin-compatible with MACH111 and MACH210A.

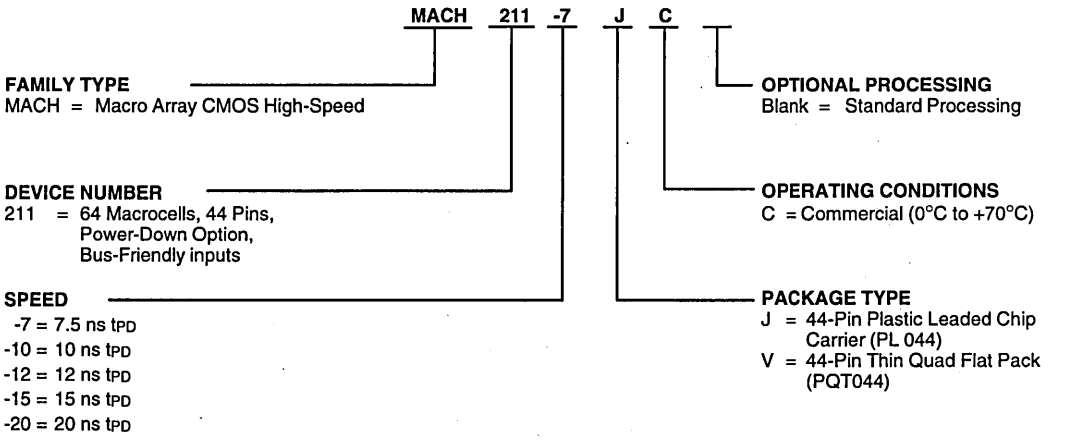
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH211-7	JC, VC
MACH211-10	
MACH211-12	
MACH211-15	
MACH211-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH211 consists of four PAL blocks connected by a switch matrix. There are 32 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH211 (Figure 1) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH211 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-term Array

The MACH211 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable; one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH211 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_{14}		C_{13}, C_{14}, C_{15}
	M_{15}	C_{14}, C_{15}

The Macrocell

The MACH211 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH211 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

Power-Down Mode

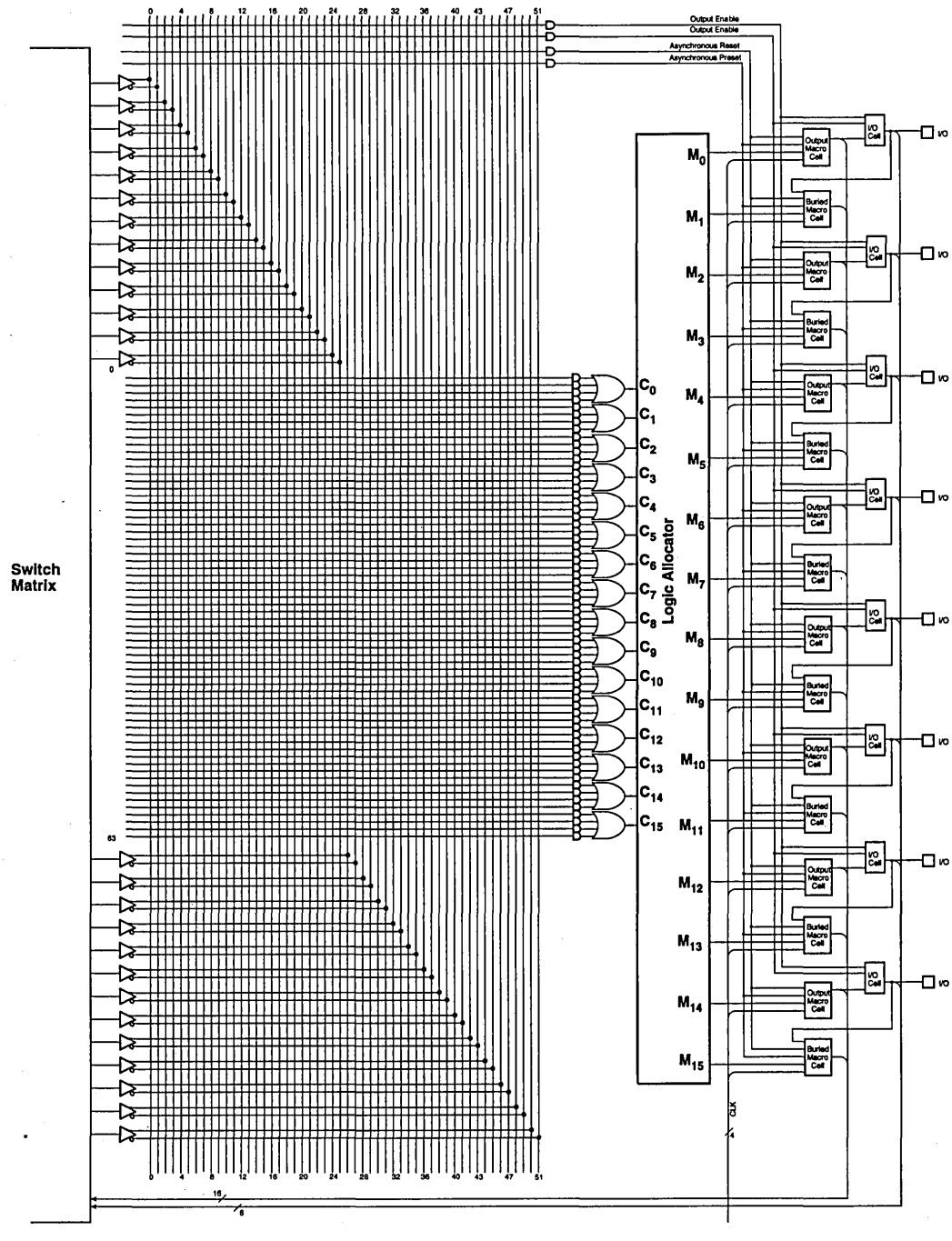
The MACH211 features a programmable low-power mode in which individual signal paths can be programmed as low power. These low-power speed paths will be slightly slower than the non-low-power paths. This feature allows speed critical paths to run at maximum frequency while the rest of the paths operate in the low-power mode, resulting in power savings of up to 75%.

Bus-Friendly Inputs and I/Os

The MACH211 inputs and I/Os include two inverters in series which loop back to the input. This double inversion reinforces the state of the input and pulls the voltage away from the input threshold voltage. Unlike a pull-up, this configuration cannot cause contention on a bus. For an illustration of this configuration, please turn to the input and output equivalent schematics at the end of this data book.

PCI Compliance

The MACH211-7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH211-7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without predictable timing, PCI compliance is dependent upon routing and product term distribution.



19601A-4

Figure 1. MACH211 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

			PRELIMINARY			
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		40		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		45		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			PRELIMINARY -7 Min	-7 Max	-10 Min	-10 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)				7.5		10	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock (Note 3)		D-type	5.5		6.5		ns
			T-type	6.5		7.5		ns
t_H	Register Data Hold Time			0		0		ns
t_{CO}	Clock to Output (Note 3)				5		6	ns
t_{WL}	Clock Width		LOW	3		5		ns
t_{WH}			HIGH	3		5		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	D-type	100		80		MHz
			T-type	91		74		MHz
		Internal Feedback (f_{CNT})	D-type	133		100		MHz
			T-type	125		91		MHz
		No Feedback		166.7		100		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			5.5		6.5		ns
t_{HL}	Latch Data Hold Time			0		0		ns
t_{GO}	Gate to Output				7		7	ns
t_{GWL}	Gate Width LOW			3		5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				9.5		12	ns
t_{SIR}	Input Register Setup Time			2		2		ns
t_{HIR}	Input Register Hold Time			2		2		ns
t_{ICO}	Input Register Clock to Combinatorial Output				11		13	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-type	9		10		ns
			T-type	10		11		ns
t_{WICL}	Input Register Clock Width		LOW	3		5		ns
t_{WICH}			HIGH	3		5		ns
f_{MAXIR}	Maximum Input Register Frequency			166.7		100		MHz
t_{SIL}	Input Latch Setup Time			2		2		ns
t_{HIL}	Input Latch Hold Time			2		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				12		14	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				14		16	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			7.5		8.5		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	PRELIMINARY -7 Min	-7 Max	-10 Min	-10 Max	Unit
t_{IGS}	Input Latch Gate to Output Latch Setup	10		11		ns
t_{WIGL}	Input Latch Gate Width LOW	3		5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		11.5		14	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		9.5		15	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	5		10		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	5		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		9.5		15	ns
t_{APW}	Asynchronous Preset Width (Note 1)	5		10		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	5		10		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		9.5		15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9.5		15	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		10		10	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

			PRELIMINARY			
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		40		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		45		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

					PRELIMINARY						
					-12		-15		-20		
Parameter Symbol	Parameter Description				Min	Max	Min	Max	Min	Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	1/(t_S + t_{CO})	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	83.3		66.6		50		MHz
				T-type	76.9		62.5		47.6		MHz
		No Feedback	1/(t_{WL} + t_{WH})		83.3		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				7		10		13		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output (Note 3)					10		11		12	ns
t_{GWL}	Gate Width LOW				6		6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14		17		22	ns
t_{SIR}	Input Register Setup Time				2		2		2		ns
t_{HIR}	Input Register Hold Time				2		2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					15		18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	12		15		20		ns
				T-type	13		16		21		ns
t_{WICL}	Input Register Clock Width			LOW	6		6		8		ns
t_{WICH}				HIGH	6		6		8		ns
f_{MAXIR}	Maximum Input Register Frequency		1/(t_{WICL} + t_{WICH})		83.3		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		2		ns
t_{HIL}	Input Latch Hold Time				2		2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19		22		27	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				9		12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				13		16		21		ns

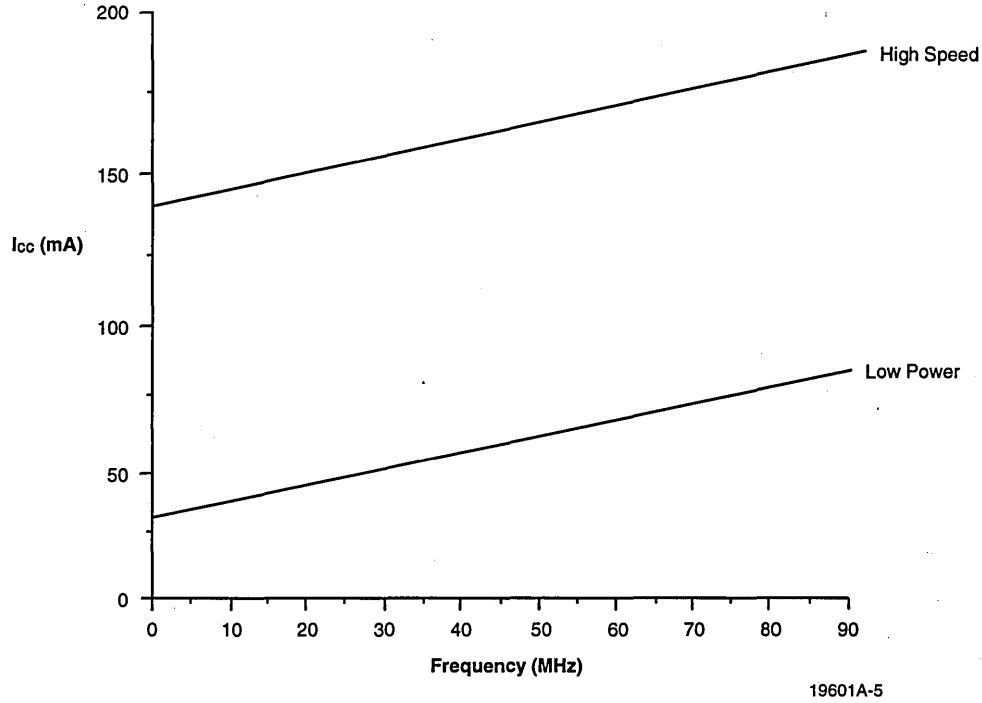
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	PRELIMINARY -12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{WIGL}	Input Latch Gate Width LOW	6		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		12		15		20	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		10		10		10	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Low-power Adder should be added to t_{PD} and t_{SU} in low-power mode.*

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ TQFP	Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		11.3	15	°C/W
θ_{ja}	Thermal impedance, junction to ambient		41	40	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	35	36	°C/W
		400 lfpm air	33.7	33	°C/W
		600 lfpm air	32.6	31	°C/W
		800 lfpm air	32	29	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

FINAL COM'L: -12/15/20 IND: -14/18/24

MACH215-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **44 Pins**
- **32 Output Macrocells**
- **32 Input Macrocells**
- **Product terms for:**
  - — Individual flip-flop clock
  - — Individual asynchronous reset, preset
  - — Individual output enable
- **12 ns t_{PD} Commercial**
  14.5 ns t_{PD} Industrial
- **67 MHz f_{CNT}**
- **38 Inputs with pull-up resistors**
- **32 Outputs**
- **64 Flip-flops**
- **For asynchronous and synchronous applications**
- **4 "PAL22RA8" blocks with buried macrocells**
- **Pin-compatible with MACH110, MACH111, MACH210, and MACH211**

GENERAL DESCRIPTION

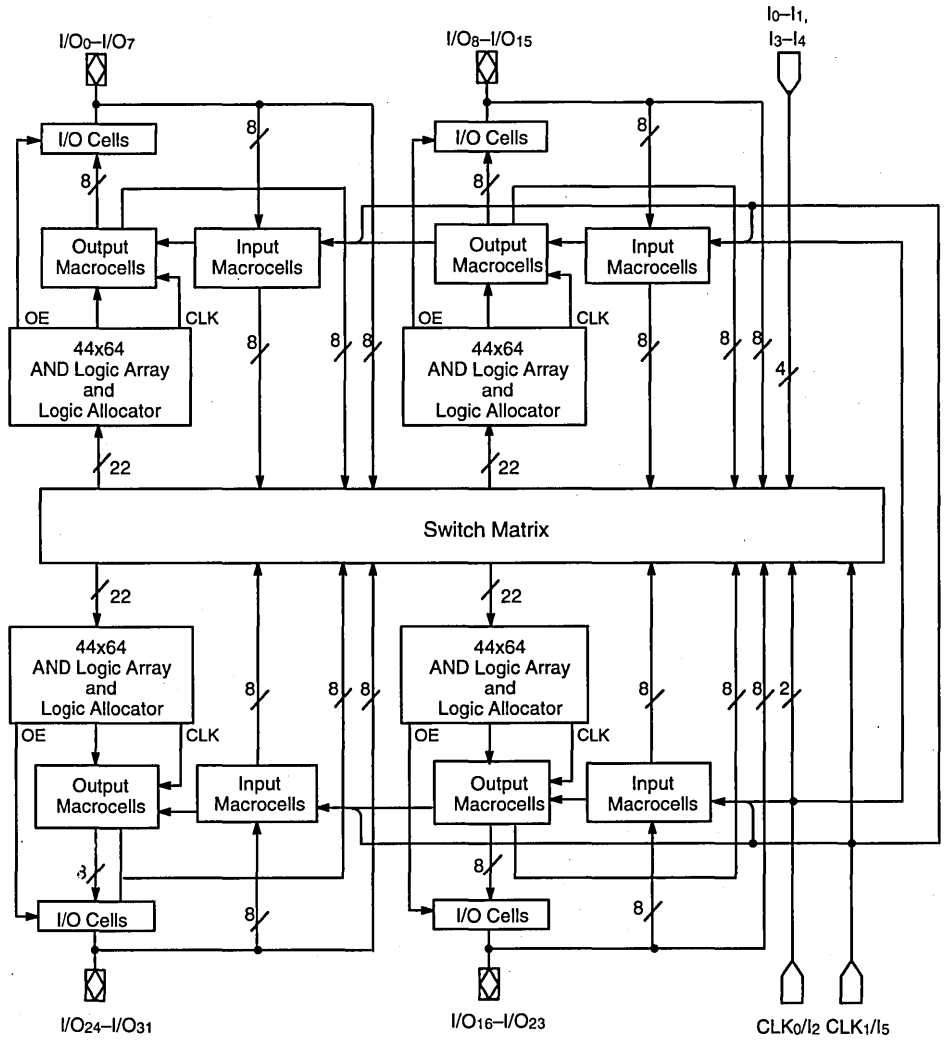
The MACH215 is a member of AMD's high-performance EE CMOS MACH device family. This device has approximately three times the capability of the popular PAL20RA10 without loss of speed. This device is designed for use in asynchronous as well as synchronous applications.

The MACH215 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22RA8" structures complete with product-term arrays and programmable macrocells, individual register control product terms, and input registers. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH215 has two kinds of macrocell: output and input. The MACH215 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. Each macrocell has its own dedicated clock, asynchronous reset, and asynchronous preset control. The polarity of the clock signal is programmable. All output macrocells can be connected to an I/O cell.

The MACH215 has dedicated input macrocells which provide input registers or latches for synchronizing input signals and reducing setup time requirements.

BLOCK DIAGRAM



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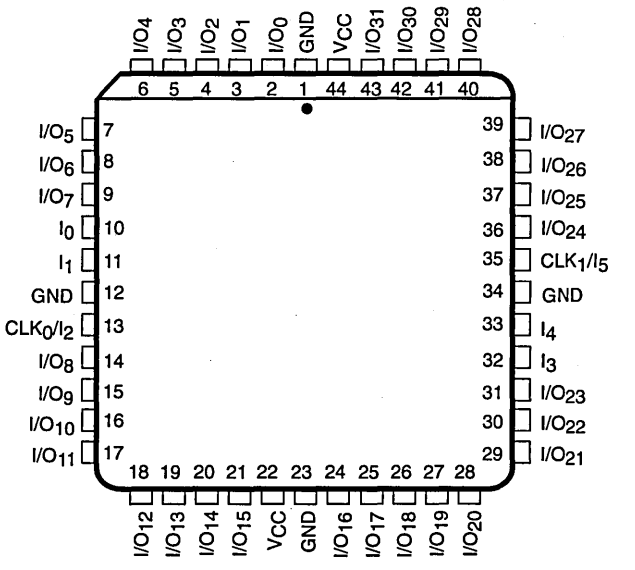
CONNECTION DIAGRAM
Top View

PLCC



16751E-2

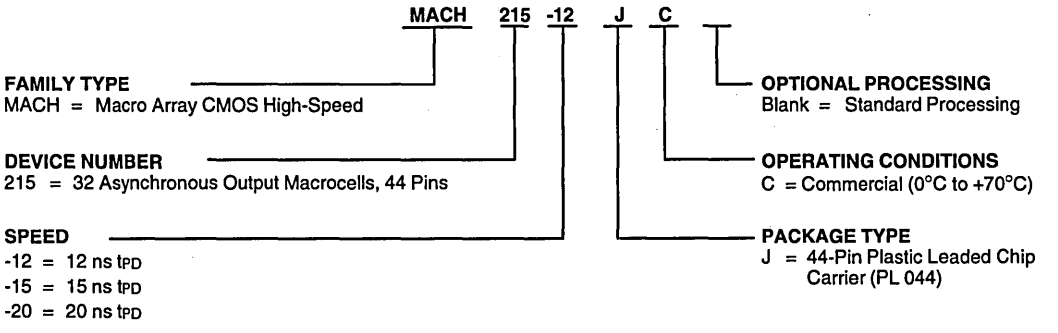
Note:
Pin-compatible with MACH110, MACH111, MACH210, and MACH211.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



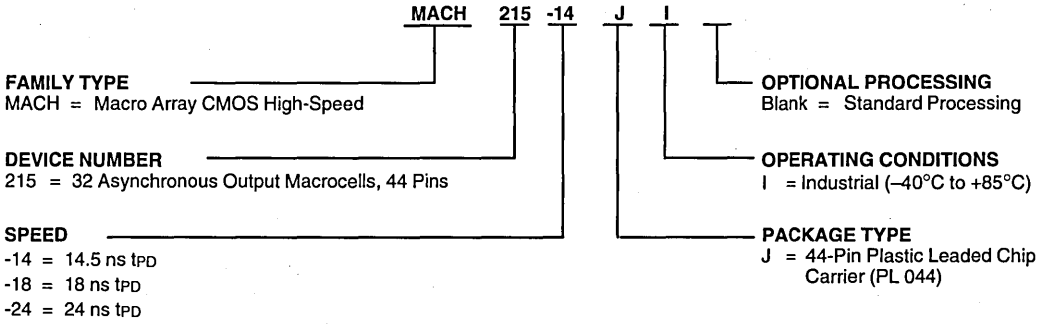
Valid Combinations	
MACH215-12	JC
MACH215-15	
MACH215-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH215-14	JI
MACH215-18	
MACH215-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH215 consists of four asynchronous PAL blocks connected by a switch matrix. There are 32 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are also two additional global clock pins that can be used as dedicated inputs. This device provides two kinds of macrocell: output macrocells and input macrocells. This adds greater logic density without affecting the number of pins.

The PAL Blocks

Each PAL block in the MACH215 (Figure 1) contains a 64-product-term array, a logic allocator, 8 output macrocells, 8 input macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22RA8" with 8 input macrocells. All flip-flops within the device can operate independently.

The Switch Matrix

The MACH215 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-term Array

The MACH215 product-term array consists of 32 product terms for logic use and 32 product terms for generating macrocell control signals.

The Logic Allocator

The logic allocator in the MACH215 (Figure 2) takes the 32 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7

The Macrocell

There are two types of macrocell in the MACH215: output macrocells and input macrocells. The output macrocell takes the logic of the device and provides it to I/O pins and/or provides feedback for additional logic generation. The input macrocell allows I/O pins to be configured as registered or latched inputs.

The output macrocell (Figure 3) can generate registered or combinatorial outputs. In addition, a transparent-low latched configuration is provided. If used, the register can be configured as a T-type or a D-type flip-flop. Register and latch functionality is defined in Table 2. Programmable polarity and the T-type flip-flop both give the software a way to minimize the number of product terms needed. These choices can be made automatically by the software when it fits the design into the device.

Table 2. Register/Latch Operation

Configuration	D/T	CLK/LE*	Q+
D-Register	X	0, 1, ↓ (↑)	Q
	0	↑ (↓)	0
	1	↑ (↓)	1
T-Register	X	0, 1, ↓ (↑)	Q
	0	↑ (↓)	$\overline{Q}$
	1	↑ (↓)	$\overline{Q}$
Latch	X	1 (0)	Q
	0	0 (1)	0
	1	0 (1)	1

**Polarity of CLK/LE can be programmed.*

The output macrocell sends its output back to the switch matrix, via internal feedback, and to the I/O cell. The feedback is always available regardless of the configuration of the I/O cell. This allows for buried combinatorial or registered functions, freeing up the I/O pins for use as inputs if not needed as outputs. The basic output macrocell configurations are shown in Figure 4.

The clock/latch-enable for each individual output macrocell can be driven by one of four signals. Two of the signals are provided by the global clock pin CLK_0/LE_0; either polarity may be chosen. The other two signals come from a product term provided for each output macrocell. Either polarity of the logic generated by the product term can be chosen. The global clock pin is also available as an input, although care must be taken when a signal acts as both clock and input to the same device.

Each individual output macrocell also has a product term for asynchronous reset and a product term for asynchronous preset. This means that any register or latch may be reset or preset without affecting any other register or latch in the device. The functionality of the flip-flops with respect to initialization is illustrated in Table 3.

Table 3. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE	Q+
0	0	X	See Table 12
0	1	X	1
1	0	X	0
1	1	X	0

The input macrocell (Figure 5) consists of a flip-flop that can be used to provide registered or latched inputs. The flip-flop can be clocked by either polarity of one of the two global clock/latch-enable pins.

Reset or preset are not provided for these flip-flops. If combinatorial inputs are desired, this macrocell is not used, and the feedback from the I/O pin is used directly. Both the I/O pin feedback and the output of the input register or latch are always available to the switch matrix.

Possible input macrocell configurations are shown in Figure 6.

The I/O Cell

The I/O cell (Figure 7) provides a three-state output buffer. The three-state control is provided by an individual product term for each I/O cell. Depending on the logic programmed onto this product term, the I/O pin can be configured as an output, an input, or a bidirectional pin. The feedback from the I/O pin is always available to the switch matrix, regardless of the state of the output buffer or the output macrocell.

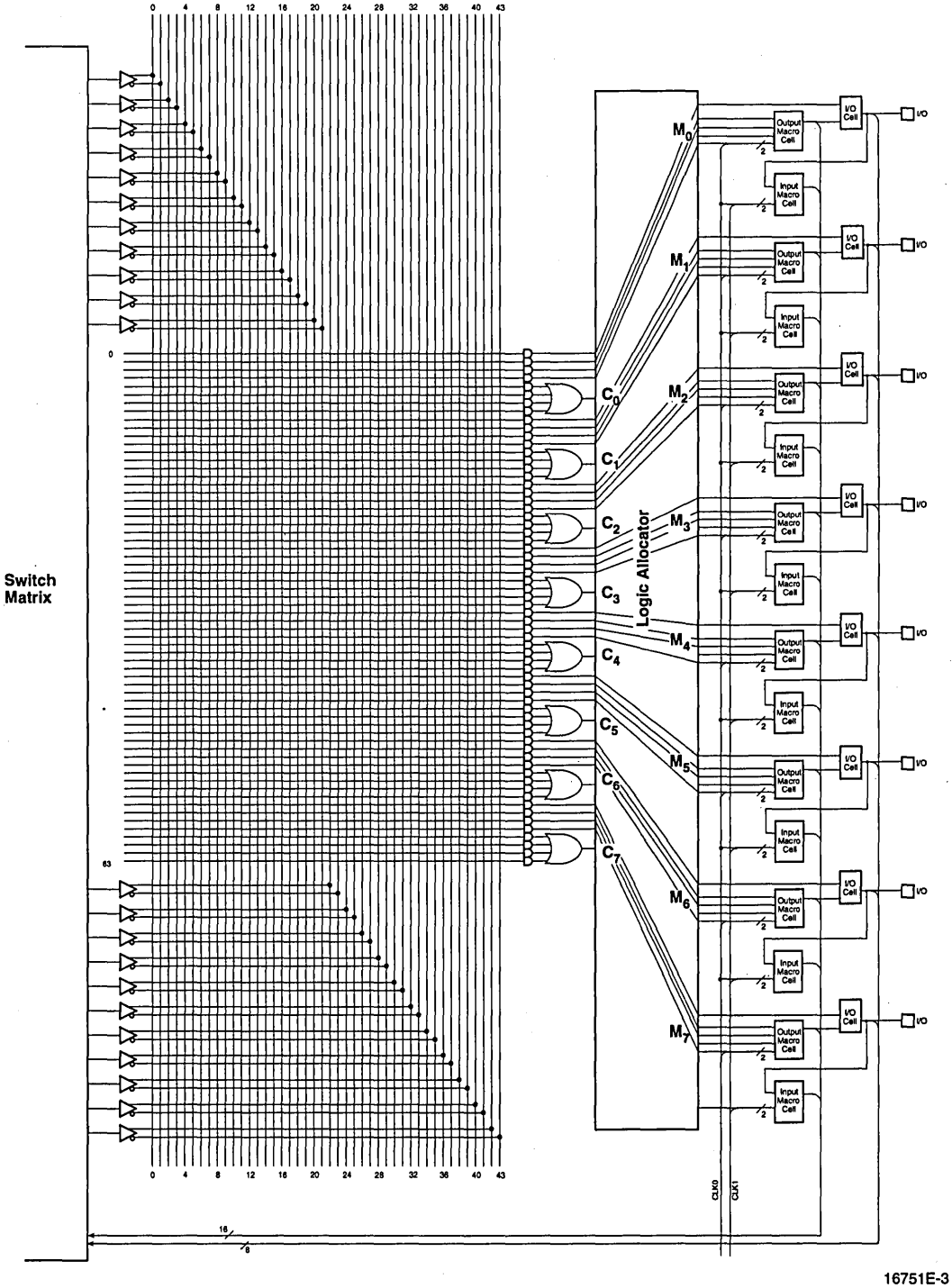


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Figure 1. MACH215 PAL Block

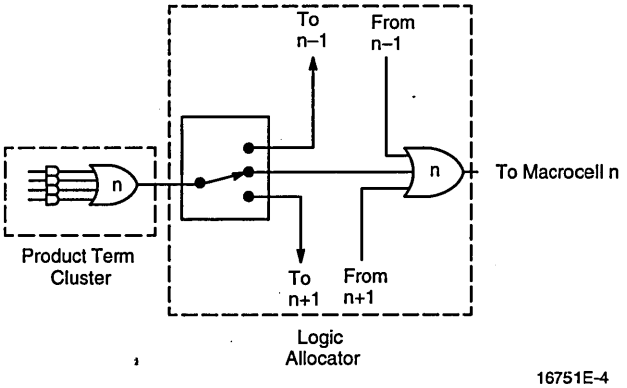


Figure 2. Product Term Clusters and the Logic Allocator

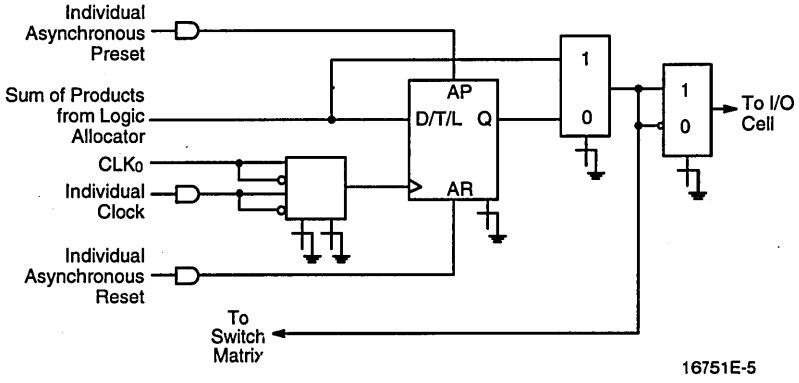
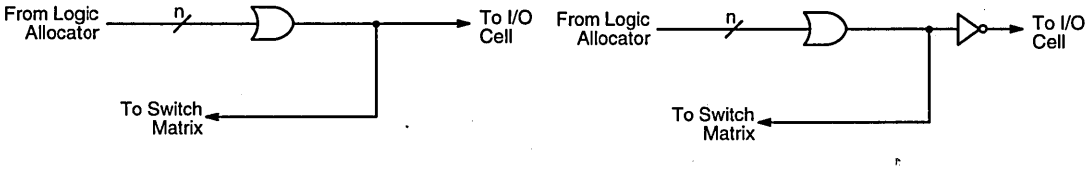
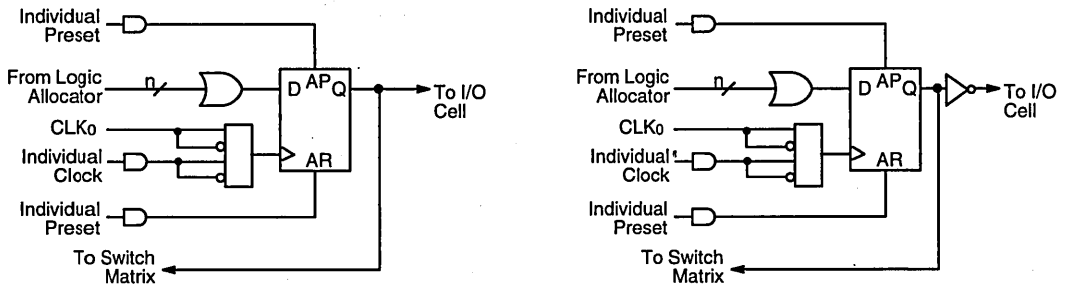


Figure 3. Output Macrocell



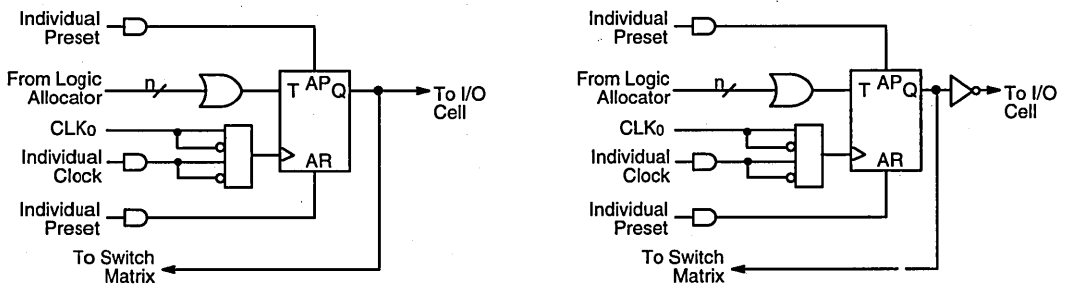
a. Combinatorial, Active High

b. Combinatorial, Active Low



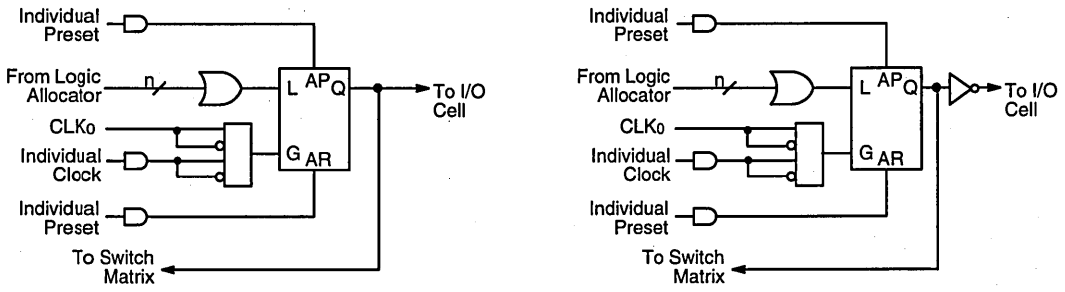
c. D-type Register, Active High

d. D-type Register, Active Low



e. T-type Register, Active High

f. T-type Register, Active Low



g. Latch, Active High

h. Latch, Active Low

16751E-6

Figure 4. Output Macrocell Configurations

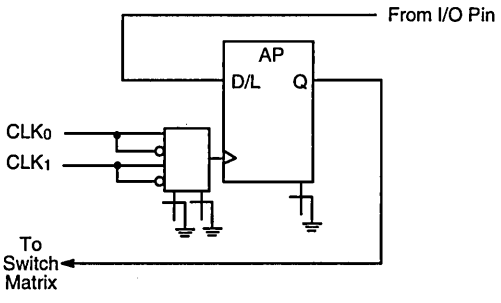


Figure 5. Input Macrocell

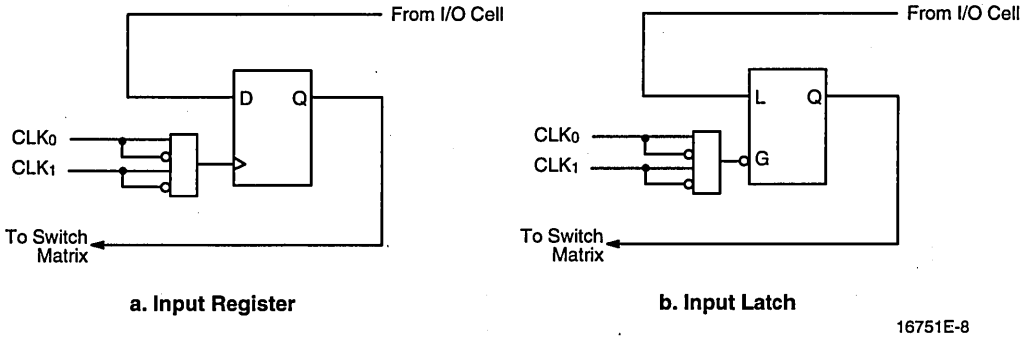


Figure 6. Input Macrocell Configurations

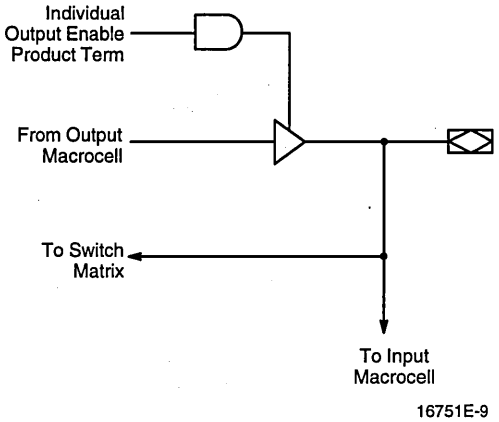


Figure 7. I/O Cell

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
with Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 5)		95		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-15		-20		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)				3	12	3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	5		6		8		ns
				T-type	6		7		9		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				5		6		8		ns
t_{COA}	Product Term Clock to Output (Note 3)				4	14	4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	8		9		12		ns
t_{WHA}				HIGH	8		9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 1)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	52.6		41.7		33.3		MHz
				T-type	50		40		32.2		MHz
		Internal Feedback (f_{CNTA})		D-type	58.8		45.5		35.7		MHz
				T-type	55.6		43.5		34.5		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$		62.5		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		ns
t_{COS}	Global Clock to Output (Note 3)				2	8	2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		6		8		ns
t_{WHS}				HIGH	6		6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 1)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	83.3		66.6		50		MHz
				T-type	76.9		62.5		47.6		MHz
		No Feedback	$1/(t_{WLS} + t_{WHS})$		83.3		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Gate				5		6		8		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				5		6		8		ns
t_{GOA}	Product Term Gate to Output (Note 3)					16		19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				8		9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				7		10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		0		ns
t_{GOS}	Gate to Output (Note 3)					10		11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		6		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description		-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch			14		17		22	ns
t_{SIR}	Input Register Setup Time		2		2		2		ns
t_{HIR}	Input Register Hold Time		2		2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output			15		18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	12		15		20		ns
		T-type	13		16		21		ns
t_{WICL}	Input Register Clock Width	LOW	6		6		8		ns
t_{WICH}		HIGH	6		6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time		2		2		2		ns
t_{HIL}	Input Latch Hold Time		2		2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			17		20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			19		22		27	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		7		8		10		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		7		8		10		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		9		12		15		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		13		16		21		ns
t_{WIGL}	Input Latch Gate Width LOW		6		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			16		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)		12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)		8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)		12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)		8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		2	12	2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		2	12	2	15	2	20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions. Switching waveforms illustrate true clocks only. Switching waveforms can be used to illustrate both synchronous and asynchronous clock timing. For example, t_{SS} is the t_S parameter for synchronous clocks and t_{SA} is the t_S parameter for asynchronous clocks.*
3. *Parameters measured with 16 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = –40°C to +85°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A) Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output I eakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 5)		95		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-14		-18		-24		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					14.5		18		24	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	6		7.5		10		ns
				T-type	7.5		8.5		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				6		7.5		10		ns
t_{COA}	Product Term Clock to Output (Note 3)					17		22		26.5	ns
t_{WLA}	Product Term, Clock Width			LOW	10		11		15		ns
t_{WHA}				HIGH	10		11		15		ns
f_{MAXS}	Maximum Frequency Using Product Term Clock (Note 1)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	42		33		26.5		MHz
				T-type	40		32		25.5		MHz
		Internal Feedback (f_{CNTA})		D-type	47		36		28.5		MHz
				T-type	44		34.5		27.5		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$		50		44.5		33		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	8.5		12		16		ns
				T-type	10		13.5		17		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		ns
t_{COS}	Global Clock to Output (Note 3)					10		12		14.5	ns
t_{WLS}	Global Clock Width			LOW	7.5		7.5		10		ns
t_{WHS}				HIGH	7.5		7.5		10		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 1)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	53		40		32		MHz
				T-type	50		38		30.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.5		53		40		MHz
				T-type	61.5		50		38		MHz
		No Feedback	$1/(t_{WLS} + t_{WHS})$		66.5		66.5		50		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Gate				6		7.5		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				6		7.5		10		ns
t_{GOA}	Product Term Gate to Output (Note 3)					19.5		23		26.5	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				10		11		14.5		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				8.5		12		16		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		0		ns
t_{GOS}	Gate to Output (Note 3)					12		13.5		14.5	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				7.5		7.5		10		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2) (continued)

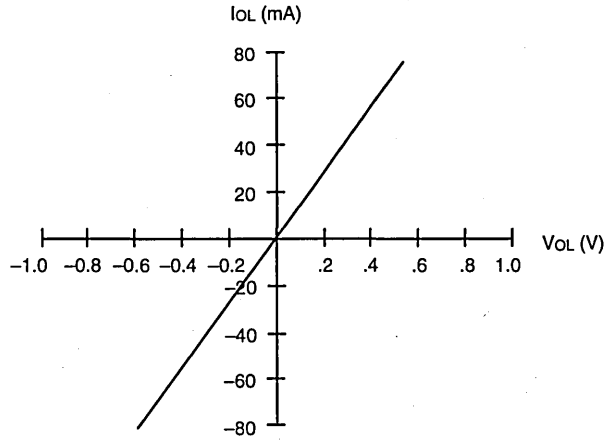
Parameter Symbol	Parameter Description		-14		-18		-24		Unit
			Min	Max	Min	Max	Min	Max	
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch			17		20.5		26.5	ns
t_{SIR}	Input Register Setup Time		2.4		2.4		2.4		ns
t_{HIR}	Input Register Hold Time		3		3.5		4		ns
t_{ICO}	Input Register Clock to Combinatorial Output			18		22		28	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	14.5		18		24		ns
		T-type	16		19.5		25.5		ns
t_{WICL}	Input Register Clock Width	LOW	7.5		7.5		10		ns
t_{WICH}		HIGH	7.5		7.5		10		ns
f_{MAXIR}	Maximum Input Register Frequency $1/(t_{WICL} + t_{WICH})$		66.5		66.5		50		MHz
t_{SIL}	Input Latch Setup Time		2.5		2.5		2.5		ns
t_{HIL}	Input Latch Hold Time		3		3.5		4		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			20.5		24		30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			23		26.5		32.5	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		8.5		10		12		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		8.5		10		12		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		11		14.5		18		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		19.5		25.5		ns
t_{WIGL}	Input Latch Gate Width LOW		7.5		7.5		10		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19.5		23		29	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			19.5		24		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)		14.5		18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)		10		12		18		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			19.5		24		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)		14.5		18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)		10		12		18		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)			14.5		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)			14.5		18		24	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions. Switching waveforms illustrate true clocks only. Switching waveforms can be used to illustrate both synchronous and asynchronous clock timing. For example, t_{SS} is the t_S parameter for synchronous clocks and t_{SA} is the t_S parameter for asynchronous clocks.*
3. *Parameters measured with 16 outputs switching.*

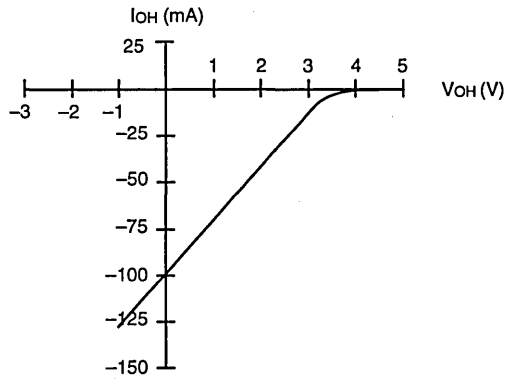
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



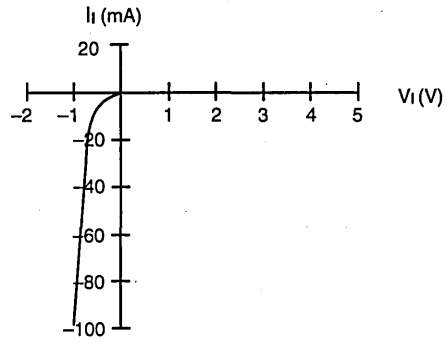
Output, LOW

16751E-10



Output, HIGH

16751E-11

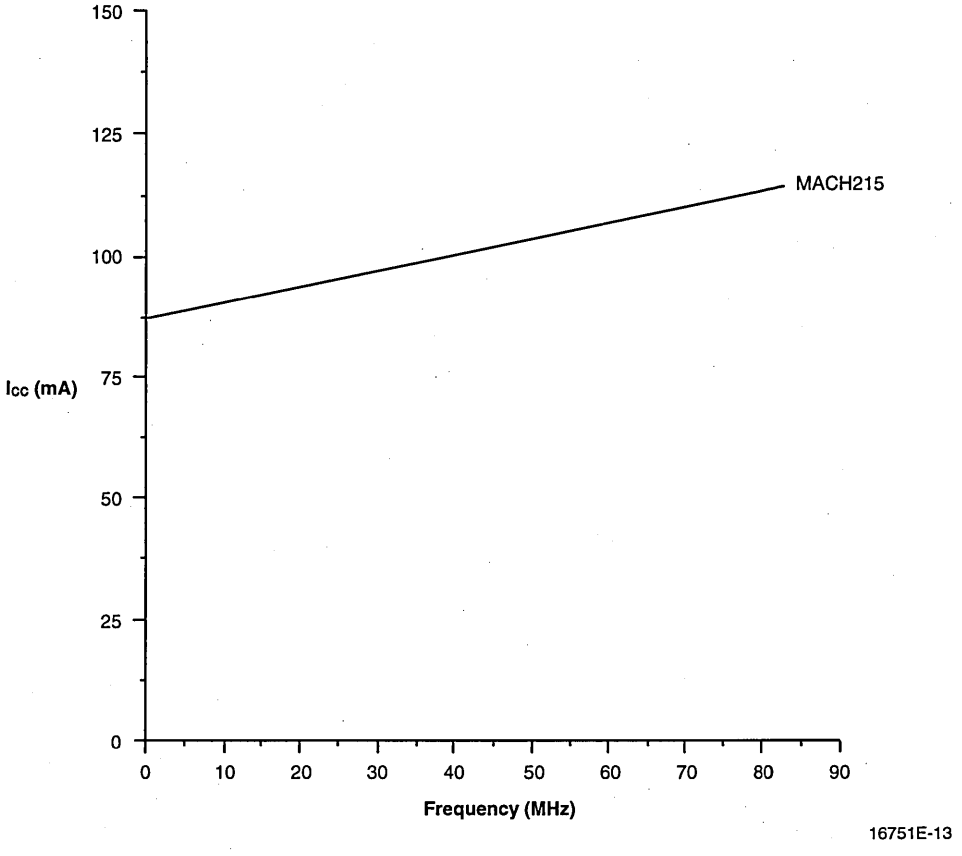


16751E-12

Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Units
θ_{jc}	Thermal impedance, junction to case		15	°C/W
θ_{ja}	Thermal impedance, junction to ambient		40	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	36	°C/W
		400 lfpm air	33	°C/W
		600 lfpm air	31	°C/W
		800 lfpm air	29	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

FINAL

COM'L: -10/12/15/20 IND: -14/18/24

MACH220-10/12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 96 Macrocells
- 10 ns t_{PD}
- 100 MHz f_{CNT}
- 56 Inputs with pull-up resistors
- 48 Outputs
- 96 Flip-flops; 4 clock choices
- 8 "PAL26V12" blocks with buried macrocells
- Pin-compatible with MACH120 and MACH221

GENERAL DESCRIPTION

The MACH220 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately nine times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH220 consists of eight PAL blocks interconnected by a programmable switch matrix. The eight PAL blocks are essentially "PAL26V12" structures complete with product-term arrays, and programmable macrocells, including buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH220 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH220 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

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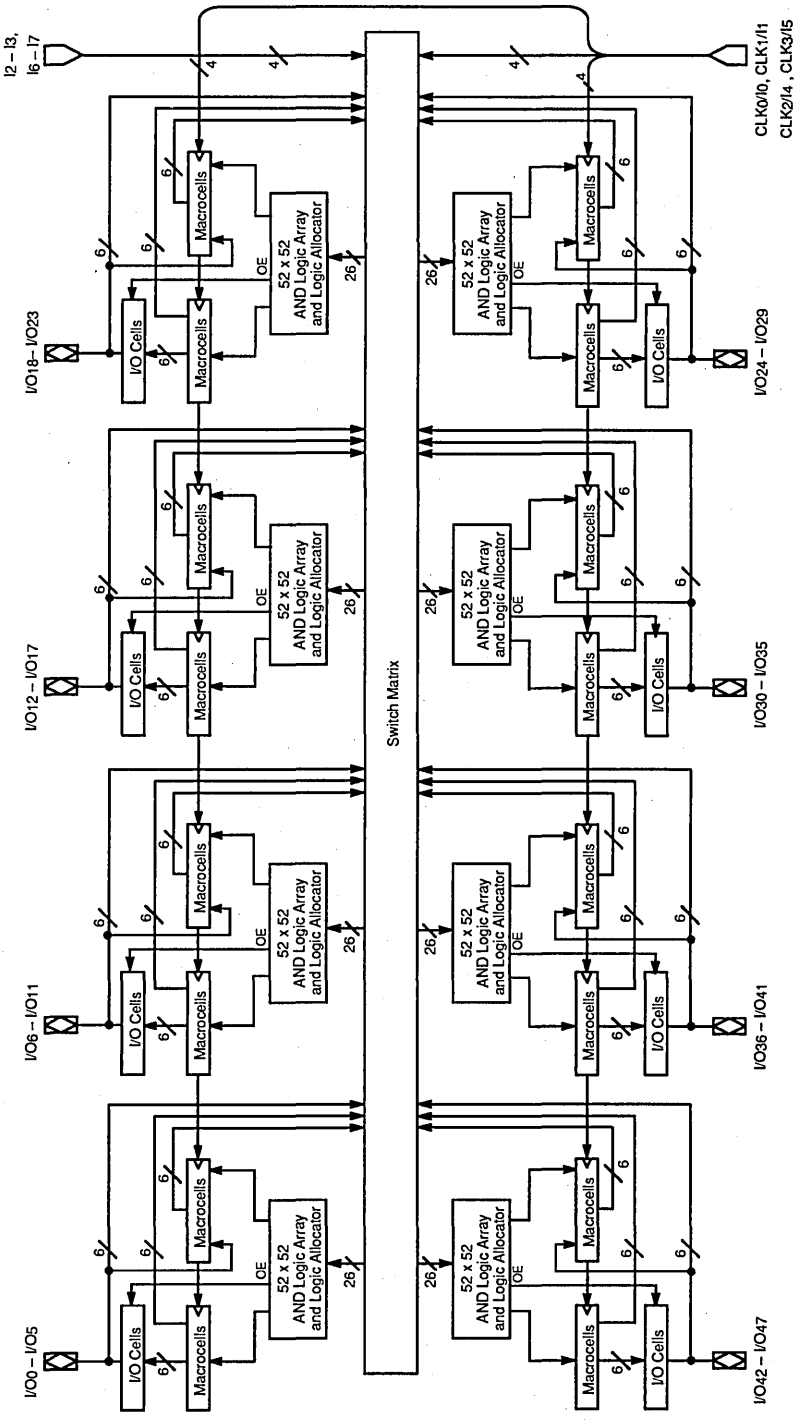
BLOCK DIAGRAM

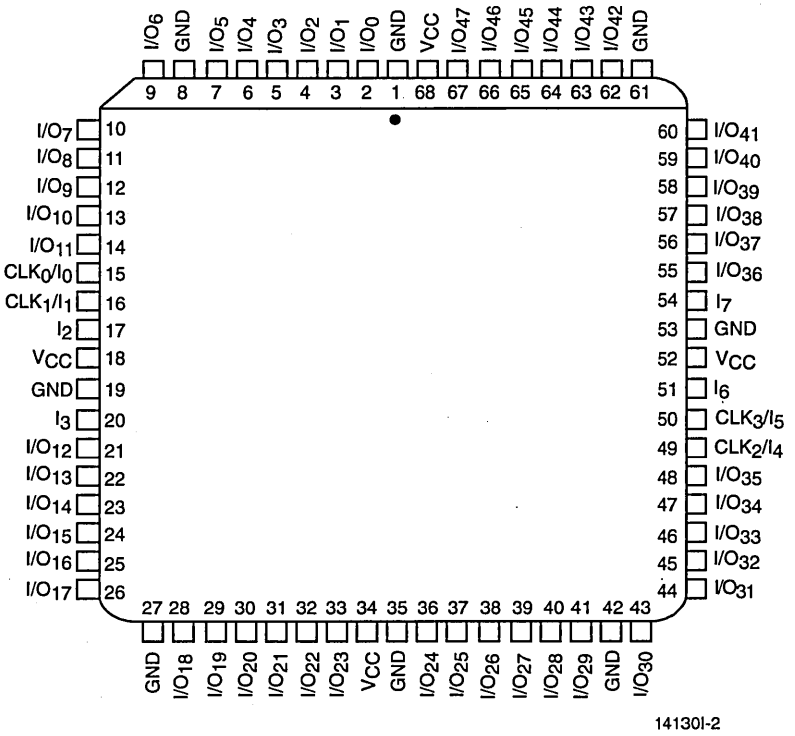


14130I-1

CONNECTION DIAGRAMS

Top View

PLCC



14130I-2

Note:
Pin-compatible with MACH120 and MACH221.

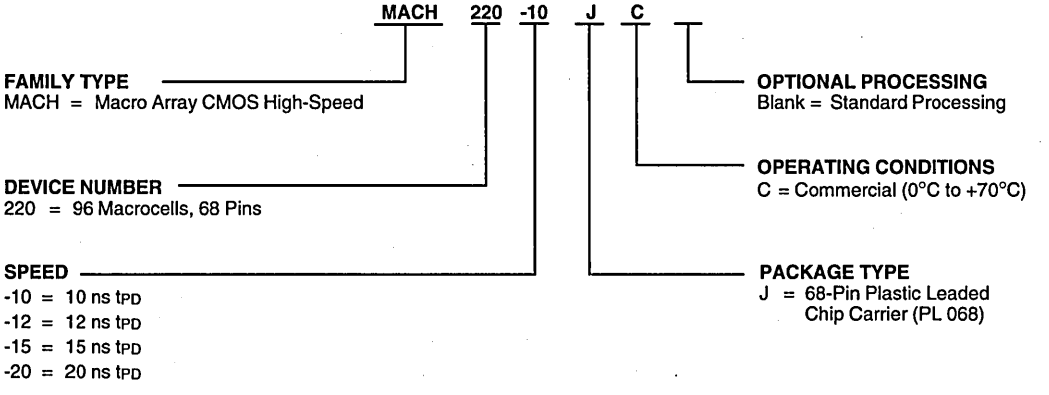
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH220-10	JC
MACH220-12	
MACH220-15	
MACH220-20	

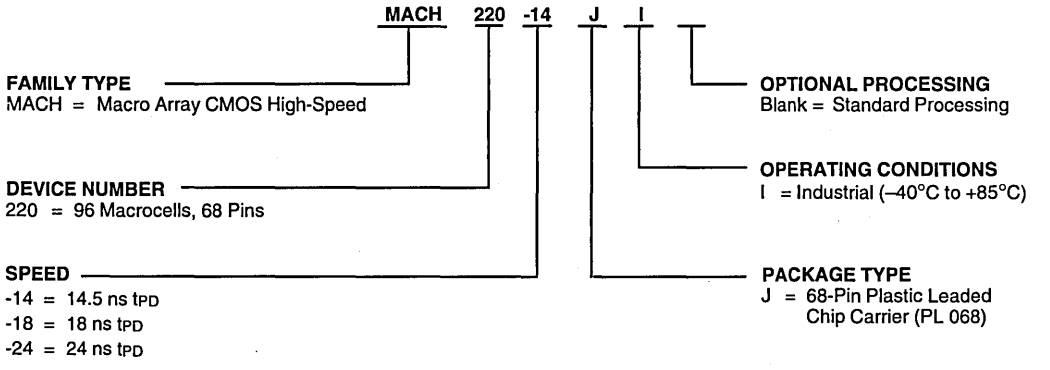
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH220-14	JI
MACH220-18	
MACH220-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH220 consists of eight PAL blocks connected by a switch matrix. There are 48 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high or low, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH220 (Figure 1) contains a 48-product-term logic array, a logic allocator, 6 output macrocells, 6 buried macrocells, and 6 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V12" with 6 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH220 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 12 internal feedback signals and 6 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH220 product-term array consists of 48 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH220 takes the 48 logic product terms and allocates them to the 12 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		C_9, C_{10}, C_{11}
	M_{11}	C_{10}, C_{11}

The Macrocell

The MACH220 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

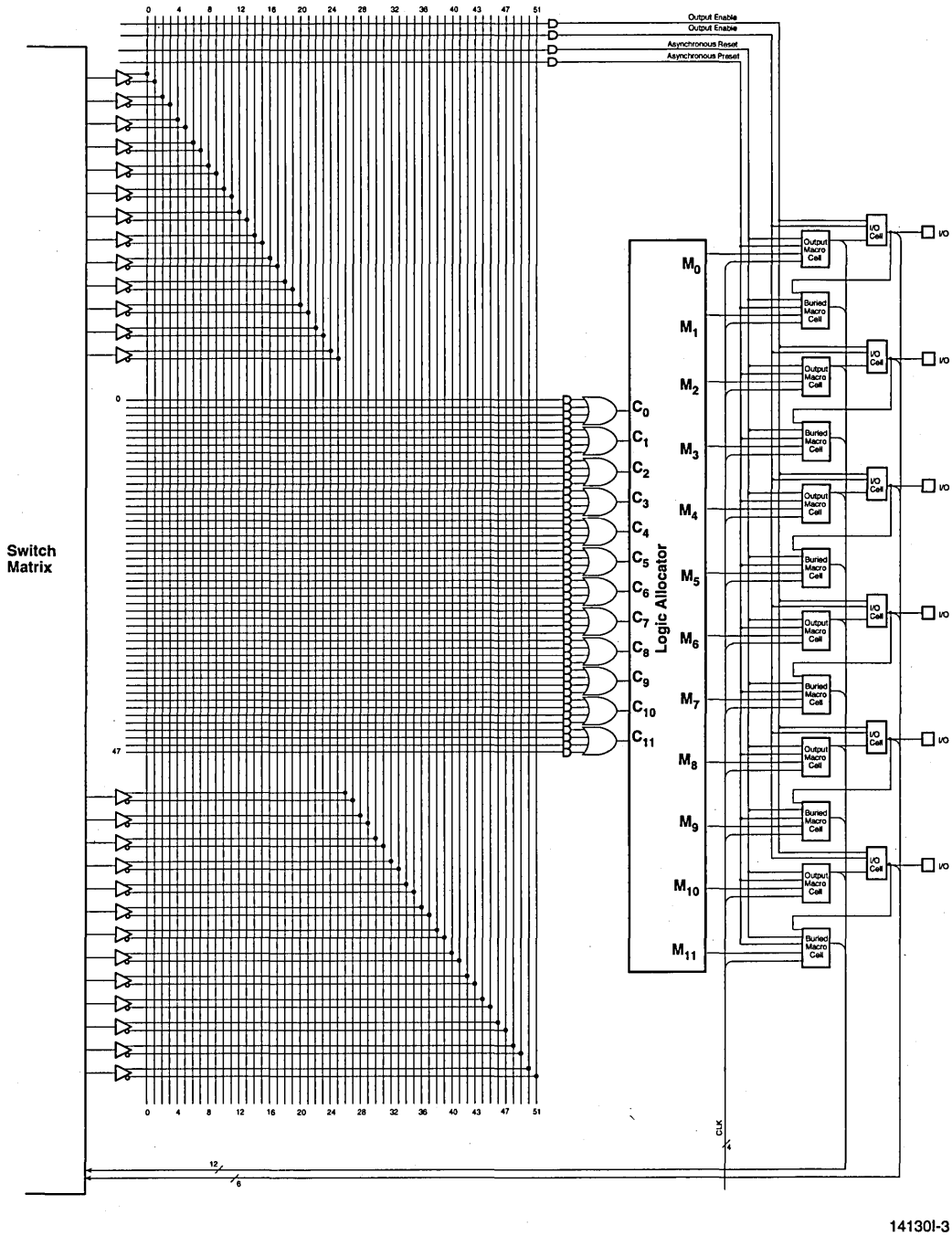
The flip-flops can individually select one of four clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH220 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.



14130I-3

Figure 1. MACH220 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		205		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 12-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10 Min	-10 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock		D-type	6.5		ns
			T-type	7.5		ns
t_H	Register Data Hold Time			0		ns
t_{CO}	Clock to Output				6.0	ns
t_{WL}	Clock Width		LOW	4		ns
t_{WH}			HIGH	4		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	D-type	80		MHz
			T-type	74		MHz
		Internal Feedback (f_{CNT})	D-type	100		MHz
			T-type	91		MHz
		No Feedback		125		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			7		ns
t_{HL}	Latch Data Hold Time			0		ns
t_{GO}	Gate to Output				7.5	ns
t_{GWL}	Gate Width LOW			4		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				14	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			2		ns
t_{ICO}	Input Register Clock to Combinatorial Output				15	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-type	11		ns
			T-type	12		ns
t_{WICL}	Input Register Clock Width		LOW	4		ns
t_{WICH}			HIGH	4		ns
f_{MAXIR}	Maximum Input Register Frequency			125		MHz
t_{SIL}	Input Latch Setup Time			2		ns
t_{HIL}	Input Latch Hold Time			2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				17	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				18	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			10		ns
t_{IGS}	Input Latch Gate to Output Latch Setup			11		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-10		Unit
		Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	4		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		15	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	10		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	8		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		15	ns
t_{APW}	Asynchronous Preset Width (Note 1)	10		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	8		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		10	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... 65°C to +150°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Supply Voltage with
Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −0.5 V to V_{CC} + 0.5 V

DC Output or
I/O Pin Voltage ..... −0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		−30	−130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		205		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 12-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-15		-20		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	83.3		66.6		50		MHz
				T-type	76.9		62.5		47.6		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				7		10		13		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output (Note 3)					10		11		12	ns
t_{GWL}	Gate Width LOW				6		6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14		17		22	ns
t_{SIR}	Input Register Setup Time				2		2		2		ns
t_{HIR}	Input Register Hold Time				2		2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					15		18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	12		15		20		ns
				T-type	13		16		21		ns
t_{WICL}	Input Register Clock Width			LOW	6		6		8		ns
t_{WICH}				HIGH	6		6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			83.3		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		2		ns
t_{HIL}	Input Latch Hold Time				2		2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19		22		27	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				9		12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				13		16		21		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	6		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		12		15		20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *Parameters measured with 24 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... 65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = –40°C to +85°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A) Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		205		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 12-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-14		-18		-24		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					14.5		18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	8.5		12		16		ns
				T-type	10		13.5		17		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12		14.5	ns
t_{WL}	Clock Width			LOW	7.5		7.5		10		ns
t_{WH}				HIGH	7.5		7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	53		40		32		MHz
				T-type	50		38		30.5		MHz
		Internal Feedback (f_{CNT})		D-type	61.5		53		38		MHz
				T-type	57		44		34.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		66.5		66.5		50		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				8.5		12		16		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output (Note 3)					12		13.5		14.5	ns
t_{GWL}	Gate Width LOW				7.5		7.5		10		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		20.5		26.5	ns
t_{SIR}	Input Register Setup Time				2.5		2.5		2.5		ns
t_{HIR}	Input Register Hold Time				3		3.5		4		ns
t_{ICO}	Input Register Clock to Combinatorial Output					18		22		28	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	14.5		18		24		ns
				T-type	16		19.5		25.5		ns
t_{WICL}	Input Register Clock Width			LOW	7.5		7.5		10		ns
t_{WICH}				HIGH	7.5		7.5		10		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			66.5		66.5		50		MHz
t_{SIL}	Input Latch Setup Time				2.5		2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				3		3.5		4		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					20.5		24		30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					23		26.5		32.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				11		14.5		18		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				16		19.5		25.5		ns
t_{WIGL}	Input Latch Gate Width LOW				7.5		7.5		10		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches					19.5		23		29	ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2) (continued)

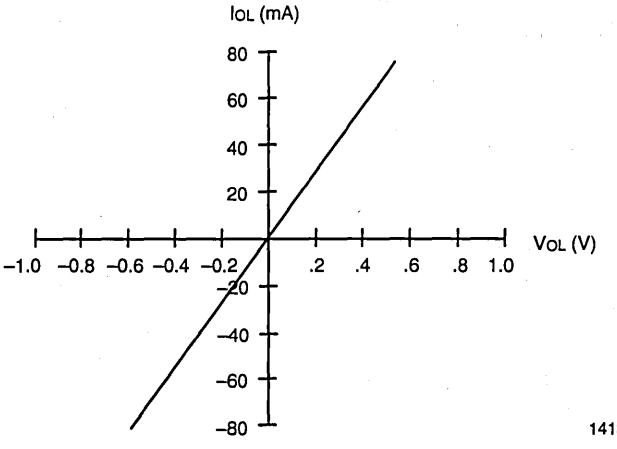
Parameter Symbol	Parameter Description	-14		-18		-24		Unit
		Min	Max	Min	Max	Min	Max	
t_{AR}	Asynchronous Reset to Registered or Latched Output		19.5		24		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	14.5		18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	10		12		18		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		19.5		24		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)	14.5		18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	10		12		18		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		14.5		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		14.5		18		24	ns

Notes:

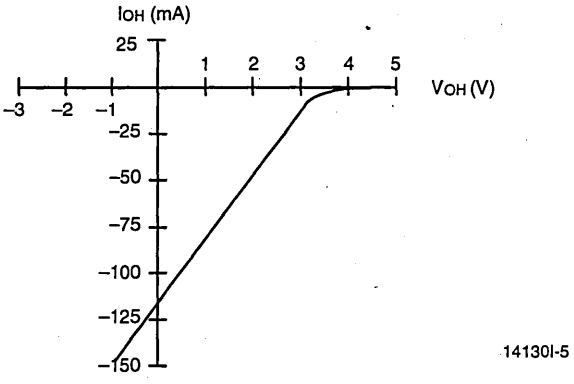
1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *Parameters measured with 24 outputs switching.*

TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

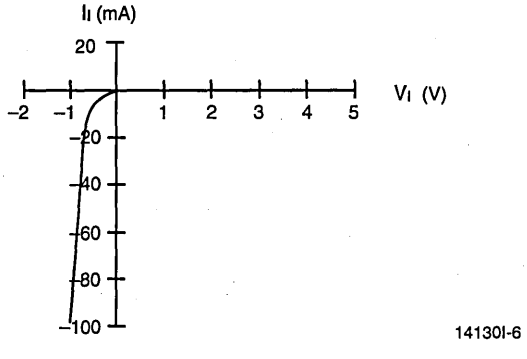
V_{CC} = 5.0 V, T_A = 25°C



Output, LOW



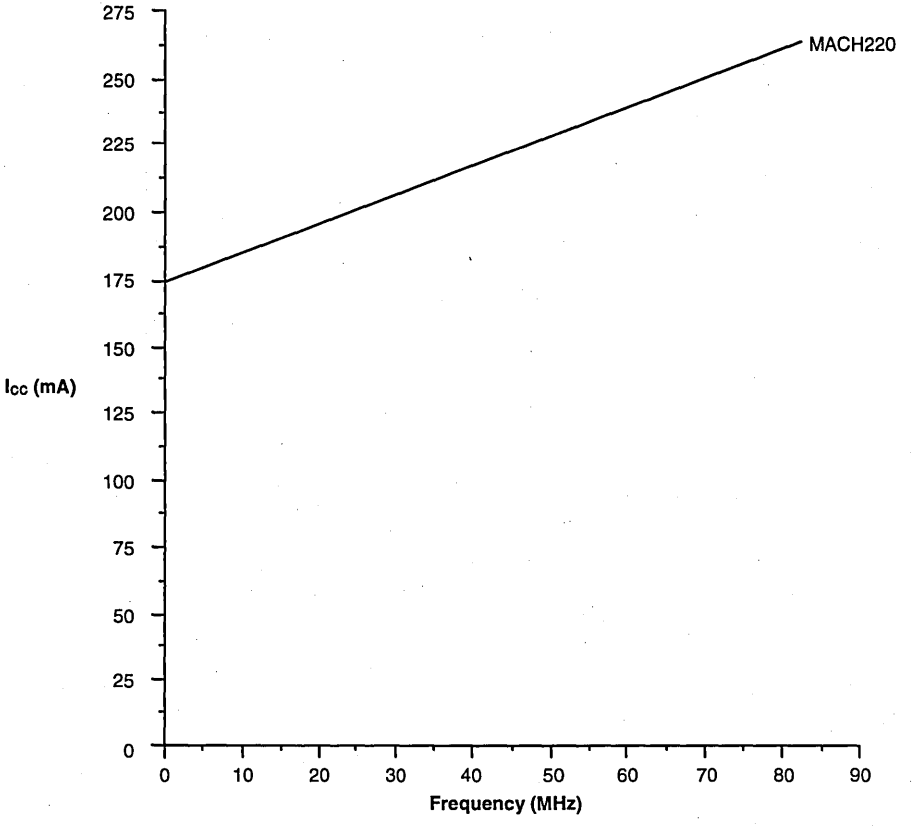
Output, HIGH



Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



14130I-7

The selected "typical" pattern is a 12-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

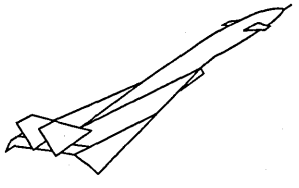
TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Units
θ_{jc}	Thermal impedance, junction to case		10	°C/W
θ_{ja}	Thermal impedance, junction to ambient		33	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	29	°C/W
		400 lfpm air	27	°C/W
		600 lfpm air	24	°C/W
		800 lfpm air	23	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.



PRELIMINARY

COM'L: -7/10/12/15/20

MACH221-7/10/12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 96 Macrocells
- 7.5 ns t_{PD}
- 133 MHz f_{CNT}
- 56 Bus-Friendly Inputs
- Programmable power-down mode
- Peripheral Component Interconnect (PCI) compliant
- 48 Outputs
- 96 Flip-flops; 4 clock choices
- 8 "PAL26V12" blocks with buried macrocells
- Pin-compatible with MACH120 and MACH220

GENERAL DESCRIPTION

The MACH221 is a member of AMD's EE CMOS MACH 2 Performance Plus device family. This device has approximately nine times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH221 consists of eight PAL blocks interconnected by a programmable switch matrix. The two PAL blocks are essentially "PAL26V12" structures complete with product-term arrays, programmable macrocells, which can be programmed as high speed or low power, and buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

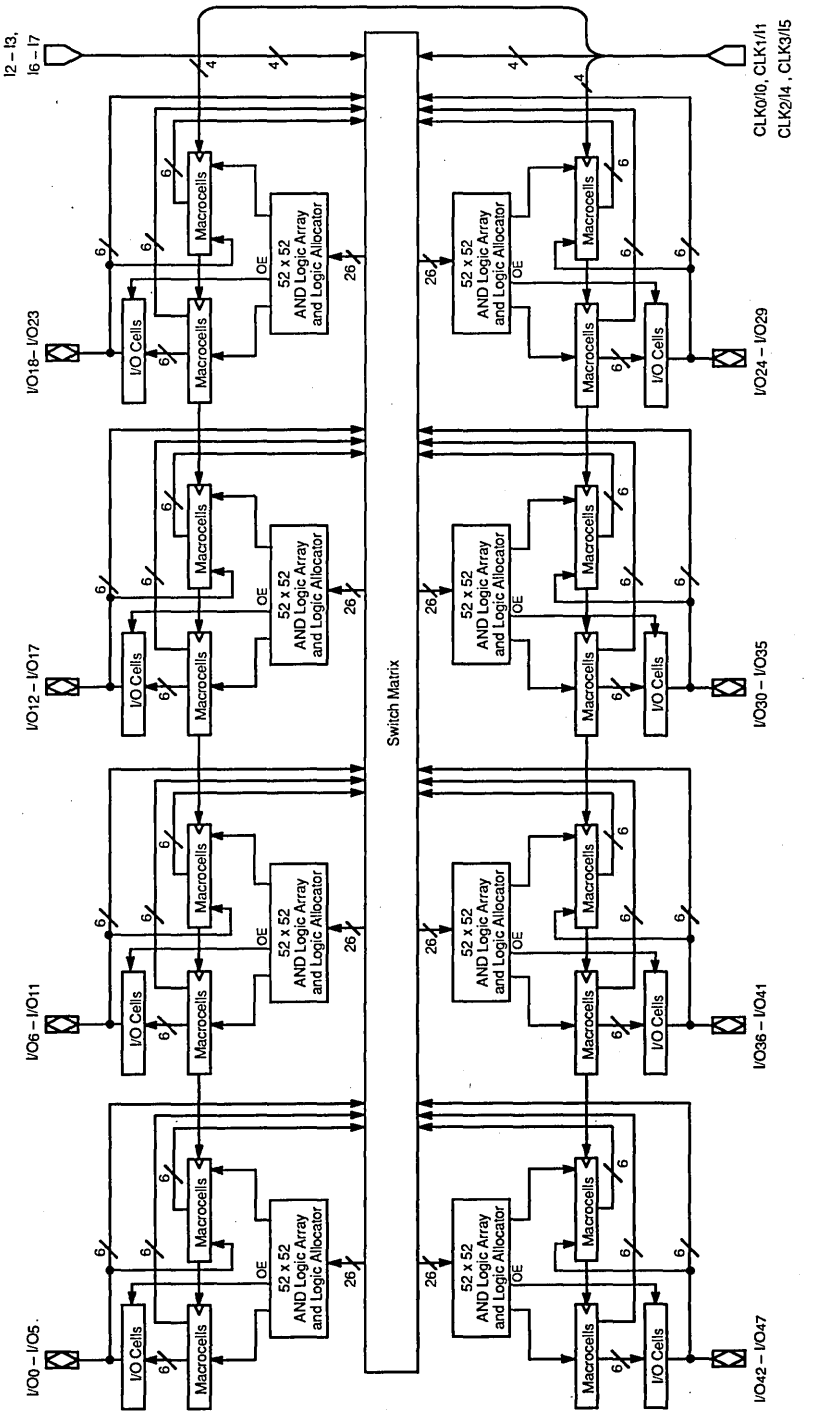
The MACH221 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH221 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

Publication# 20157 Rev. A Amendment/0
Issue Date: May 1995

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

BLOCK DIAGRAM

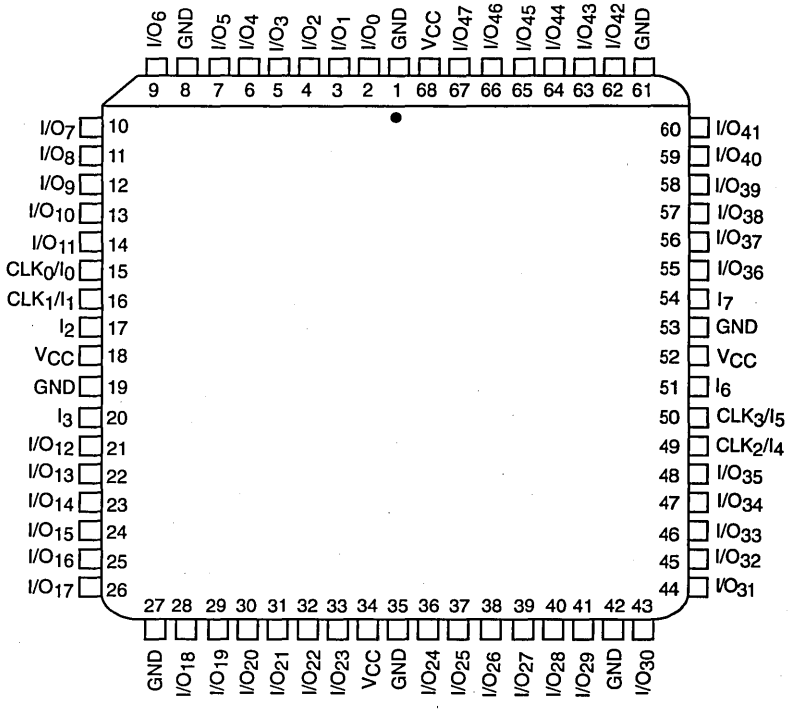


20157A-1

CONNECTION DIAGRAMS

Top View

PLCC



20157A-2

Note:
Pin-compatible with MACH120 and MACH220.

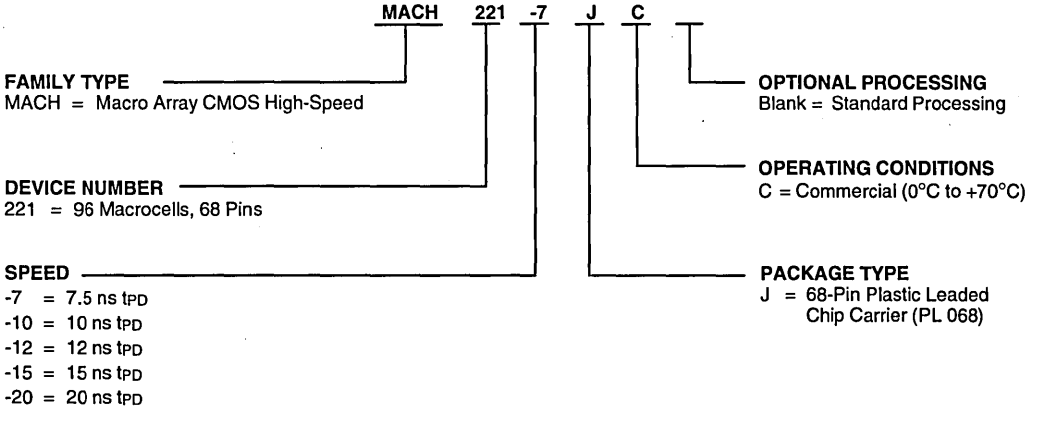
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH221-7	JC
MACH221-10	
MACH221-12	
MACH221-15	
MACH221-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH221 consists of eight PAL blocks connected by a switch matrix. There are 48 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH221 (Figure 1) contains a 48-product-term logic array, a logic allocator, 6 output macrocells, 6 buried macrocells, and 6 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V12" with 6 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH221 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 12 internal feedback signals and 6 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH221 product-term array consists of 48 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH221 takes the 48 logic product terms and allocates them to the 12 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		C_9, C_{10}, C_{11}
	M_{11}	C_{10}, C_{11}

The Macrocell

The MACH221 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH221 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

Power-Down Mode

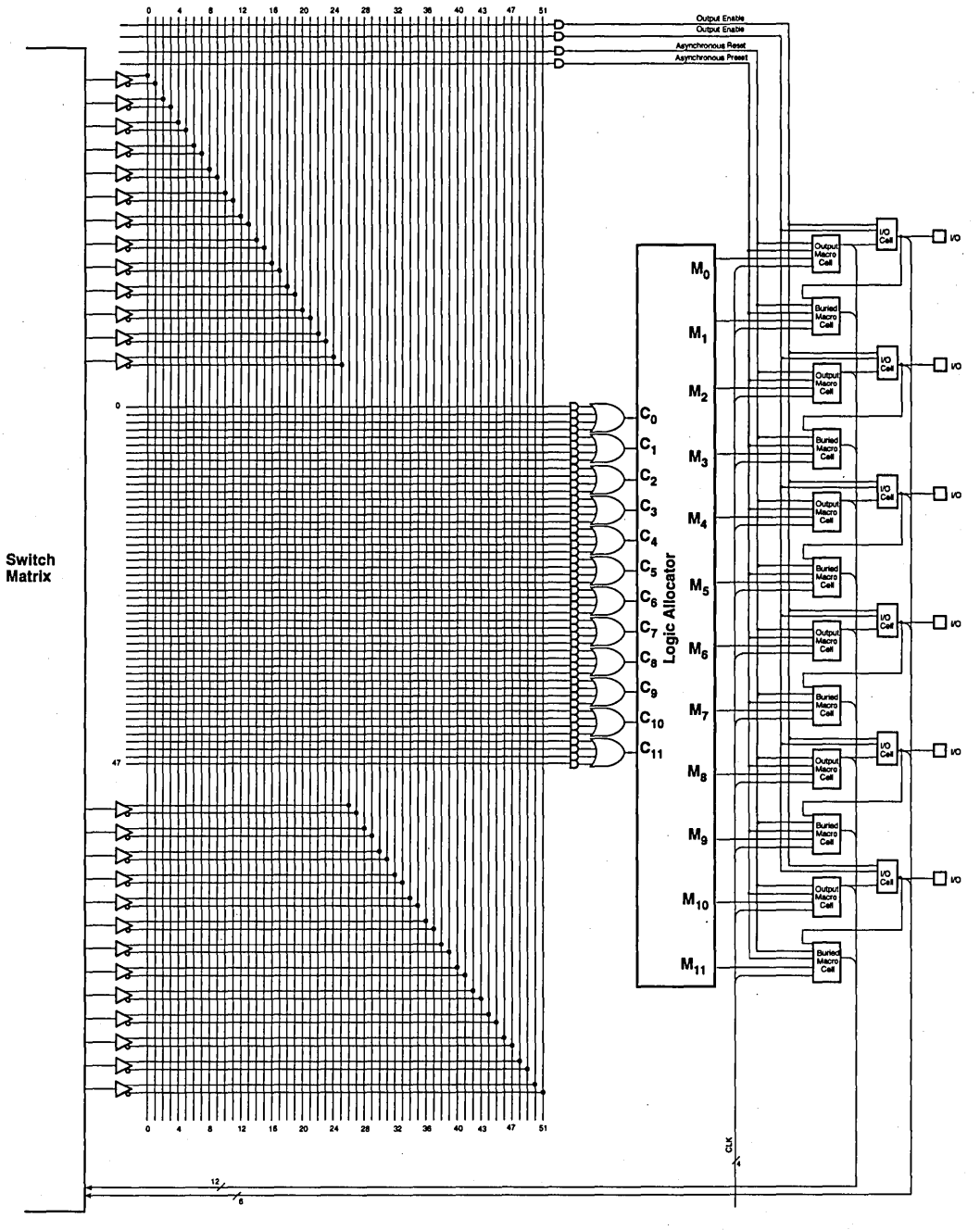
The MACH221 features a programmable low-power mode in which individual signal paths can be programmed as low power. These low-power speed paths will be slightly slower than the non-low-power paths. This feature allows speed critical paths to run at maximum frequency while the rest of the paths operate in the low-power mode, resulting in power savings of up to 50%.

Bus-Friendly Inputs and I/Os

The MACH221 inputs and I/Os include two inverters in series which loop back to the input. This double inversion reinforces the state of the input and pulls the voltage away from the input threshold voltage. Unlike a pull-up, this configuration cannot cause contention on a bus. For an illustration of this configuration, please turn to the input and output equivalent schematics at the end of this data book.

PCI Compliance

The MACH221-7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH221-7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without predictable timing, PCI compliance is dependent upon routing and product term distribution.



20157A-3

Figure 1. MACH221 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

			PRELIMINARY			
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		70		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		75		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			PRELIMINARY -7 Min	-7 Max	-10 Min	-10 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)				7.5		10	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock (Note 3)		D-type	5.5		6.5		ns
			T-type	6.5		7.5		ns
t_H	Register Data Hold Time			0		0		ns
t_{CO}	Clock to Output (Note 3)				5		6	ns
t_{WL}	Clock Width		LOW	3		5		ns
t_{WH}			HIGH	3		5		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	D-type	100		80		MHz
			T-type	91		74		MHz
		Internal Feedback (f_{CNT})	D-type	133		100		MHz
			T-type	125		91		MHz
		No Feedback		166.7		100		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			5.5		6.5		ns
t_{HL}	Latch Data Hold Time			0		0		ns
t_{GO}	Gate to Output				7		7	ns
t_{GWL}	Gate Width LOW			3		5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				9.5		12	ns
t_{SIR}	Input Register Setup Time			2		2		ns
t_{HIR}	Input Register Hold Time			2		2		ns
t_{ICO}	Input Register Clock to Combinatorial Output				11		13	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-type	9		10		ns
			T-type	10		11		ns
t_{WICL}	Input Register Clock Width		LOW	3		5		ns
t_{WICH}			HIGH	3		5		ns
f_{MAXIR}	Maximum Input Register Frequency			166.7		100		MHz
t_{SIL}	Input Latch Setup Time			2		2		ns
t_{HIL}	Input Latch Hold Time			2		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				12		14	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				14		16	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			7.5		8.5		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	PRELIMINARY -7 Min	-7 Max	-10 Min	-10 Max	Unit
t_{IGS}	Input Latch Gate to Output Latch Setup	10		11		ns
t_{WIGL}	Input Latch Gate Width LOW	3		5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		11.5		14	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		9.5		15	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	5		10		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	5		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		9.5		15	ns
t_{APW}	Asynchronous Preset Width (Note 1)	5		10		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	5		10		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		9.5		15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9.5		15	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		10		10	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

			PRELIMINARY			
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		70		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		75		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

					PRELIMINARY						
					-12		-15		-20		
Parameter Symbol	Parameter Description				Min	Max	Min	Max	Min	Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	83.3		66.6		50		MHz
				T-type	76.9		62.5		47.6		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				7		10		13		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output (Note 3)					10		11		12	ns
t_{GWL}	Gate Width LOW				6		6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14		17		22	ns
t_{SIR}	Input Register Setup Time				2		2		2		ns
t_{HIR}	Input Register Hold Time				2		2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					15		18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	12		15		20		ns
				T-type	13		16		21		ns
t_{WICL}	Input Register Clock Width			LOW	6		6		8		ns
t_{WICH}				HIGH	6		6		8		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		83.3		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		2		ns
t_{HIL}	Input Latch Hold Time				2		2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19		22		27	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				9		12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				13		16		21		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

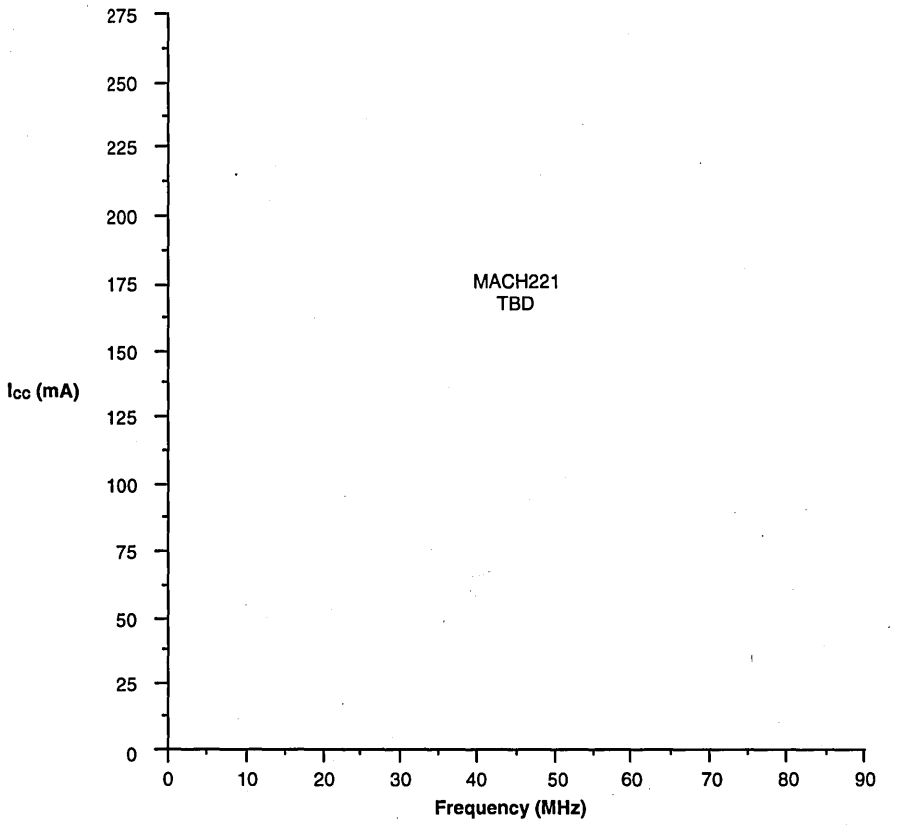
Parameter Symbol	Parameter Description	PRELIMINARY -12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{WIGL}	Input Latch Gate Width LOW	6		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		12		15		20	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		10		10		10	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *Low-power Adder should be added to t_{PD} and t_{SU} in low-power mode.*

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



20157A-4

The selected "typical" pattern is a 12-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

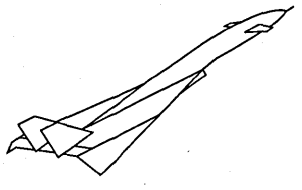
TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Units
θ_{jc}	Thermal impedance, junction to case		10	°C/W
θ_{ja}	Thermal impedance, junction to ambient		33	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	29	°C/W
		400 lfpm air	27	°C/W
		600 lfpm air	24	°C/W
		800 lfpm air	23	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.



FINAL COM'L: -10/15/20 IND: -18/24

MACH230-10/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 128 Macrocells
- 10 ns t_{PD} Commercial
  18 ns t_{PD} Industrial
- 100 MHz f_{CNT}
- 70 Inputs
- 64 Outputs
- 128 Flip-flops; 4 clock choices
- 8 "PAL26V16" blocks with buried macrocells
- Pin-compatible with MACH130, MACH131, MACH231, and MACH435

GENERAL DESCRIPTION

The MACH230 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately twelve times the logic macrocell capability of the popular PAL22V10 without loss of speed.

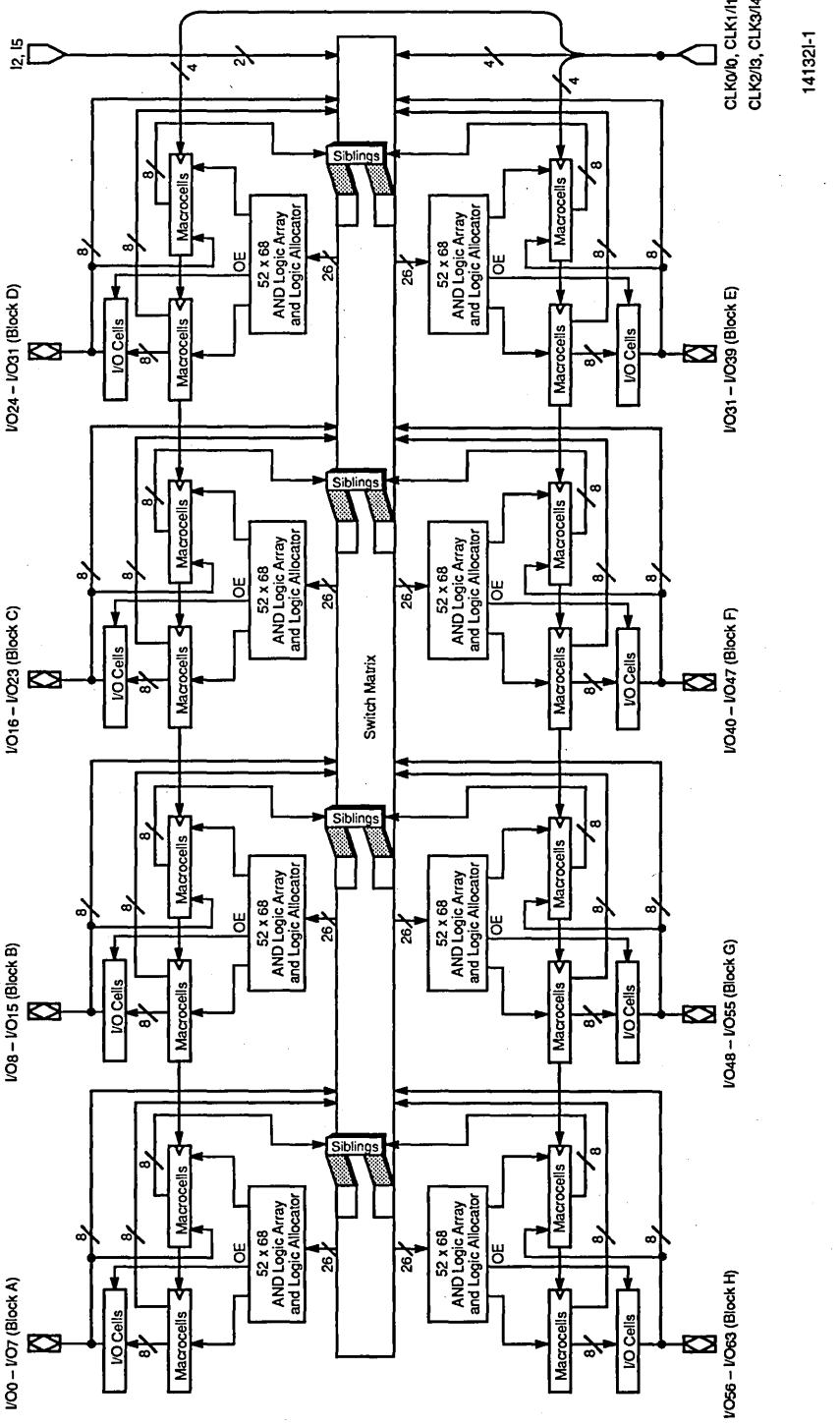
The MACH230 consists of eight PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH230 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH230 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

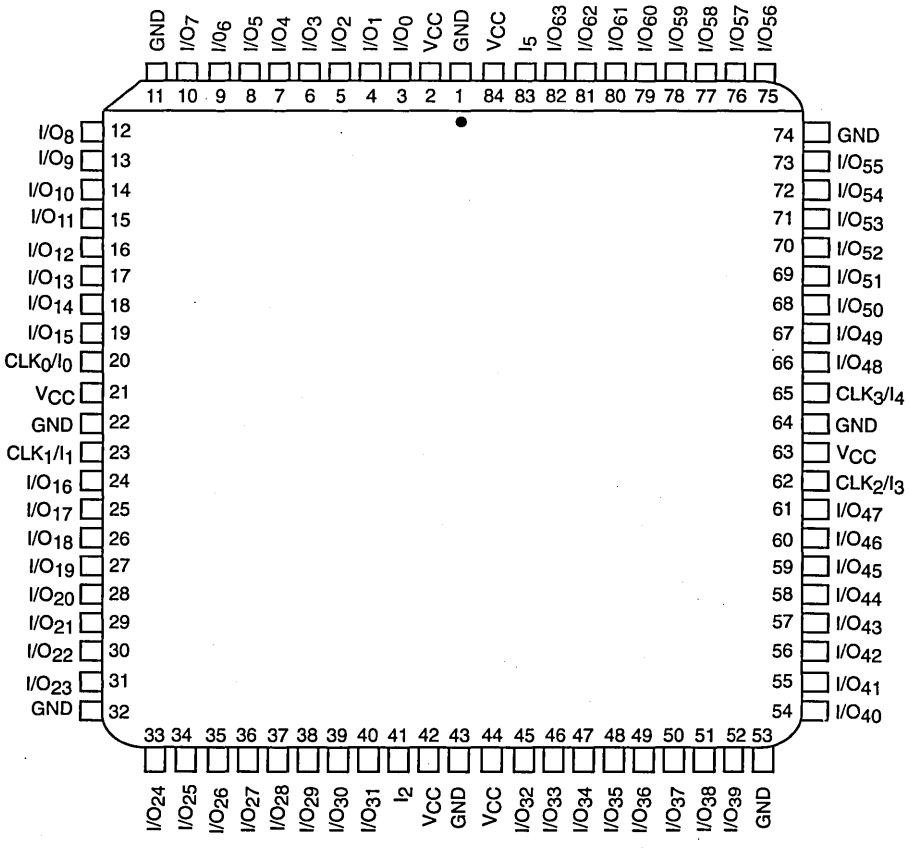
Publication# 14132 Rev. I Amendment/0
Issue Date: May 1995

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View

PLCC



14132I-2

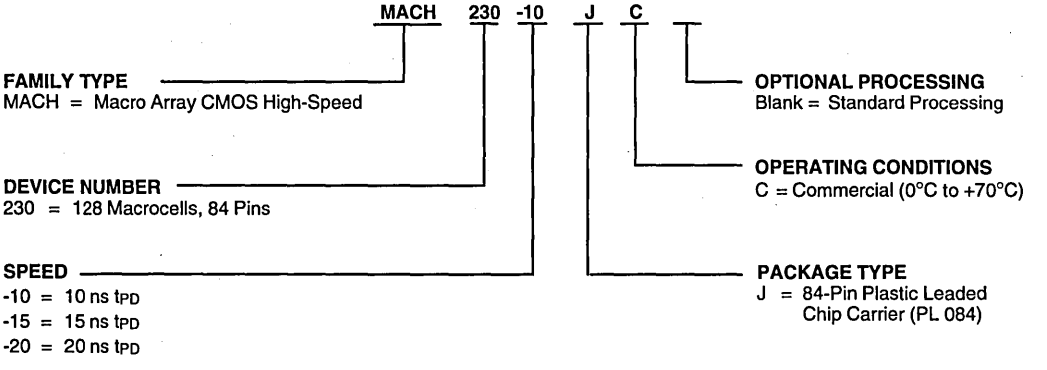
Note:
Pin-compatible with MACH130, MACH131, MACH231, and MACH435.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



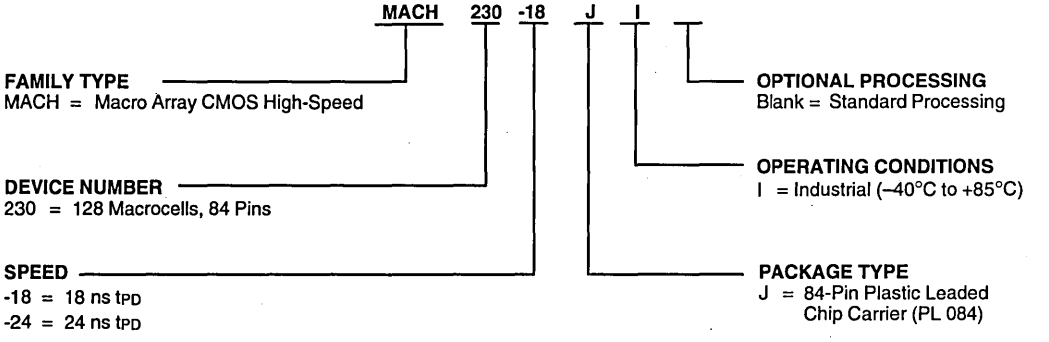
Valid Combinations	
MACH230-10	JC
MACH230-15	
MACH230-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH230-18	JI
MACH230-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH230 consists of eight PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH230 (Figure 1) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH230 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The MACH230 places a restriction on buried macrocell feedback only. Buried macrocell feedback from one block can be used as an input only to that block or its "sibling" block. Sibling blocks are illustrated in the block diagram and in Table 1. Output macrocell feedback is not restricted.

Table 1. Sibling Blocks

PAL Block	Sibling Block
A	H
B	G
C	F
D	E
E	D
F	C
G	B
H	A

The Product-Term Array

The MACH230 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH230 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 2 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 2. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_{14}		C_{13}, C_{14}, C_{15}
	M_{15}	C_{14}, C_{15}

The Macrocell

The MACH230 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH230 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

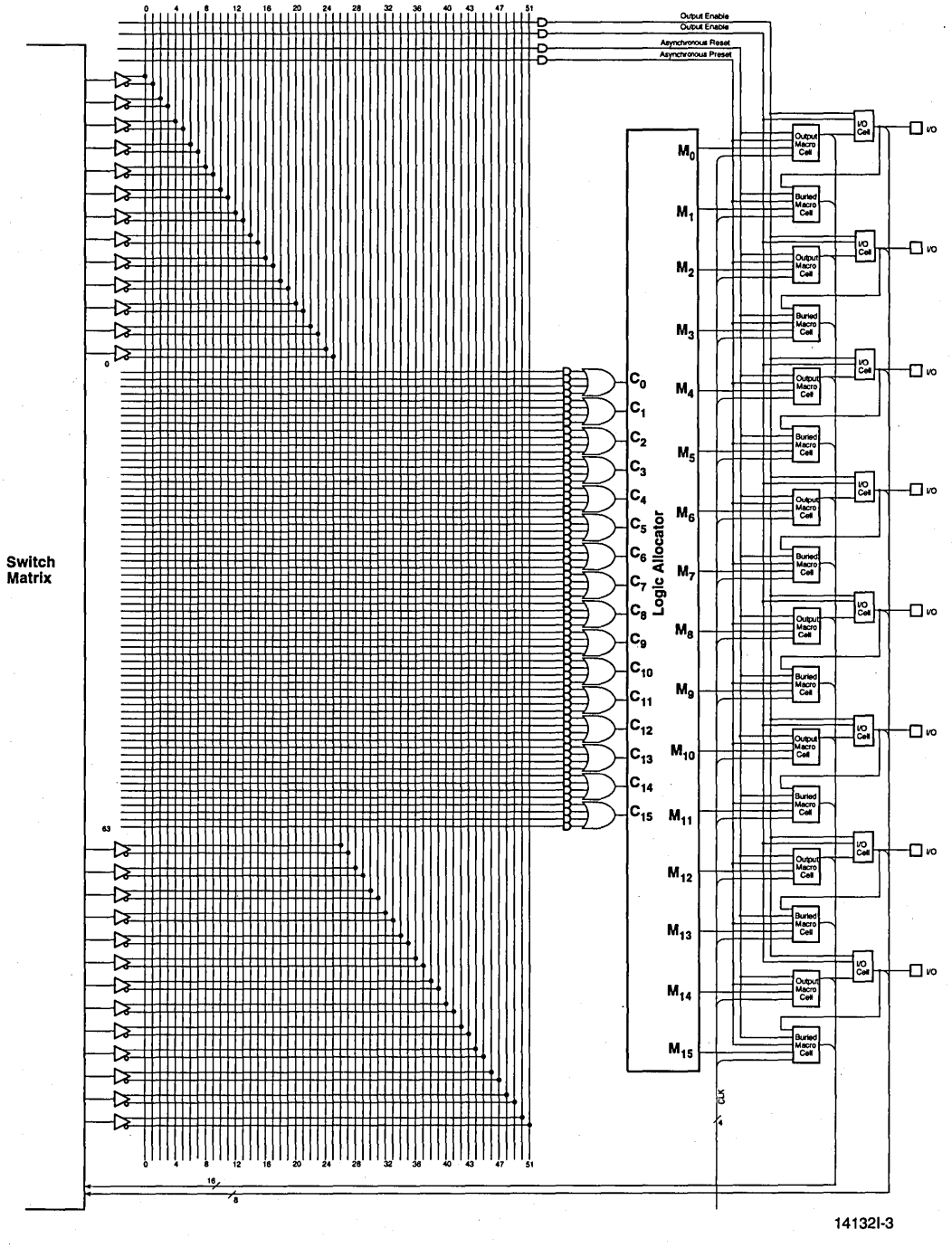


Figure 1. MACH230 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5.0 V, f = 25 MHz, T_A = 25°C (Note 4)		235		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description			-10 Min	-10 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock		D-type	6.5		ns
			T-type	7.5		ns
t_H	Register Data Hold Time			0		ns
t_{CO}	Clock to Output				6.5	ns
t_{WL}	Clock Width		LOW	4		ns
t_{WH}			HIGH	4		ns
f_{MAX}	Maximum Frequency	External Feedback	D-type	77		MHz
			T-type	72		MHz
		Internal Feedback (f_{CNT})	D-type	100		MHz
			T-type	91		MHz
		No Feedback		125		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			8		ns
t_{HL}	Latch Data Hold Time			0		ns
t_{GO}	Gate to Output				7.5	ns
t_{GWL}	Gate Width LOW			4		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				14	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			2.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output				15.5	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-type	11		ns
			T-type	12		ns
t_{WICL}	Input Register Clock Width		LOW	4		ns
t_{WICH}			HIGH	4		ns
f_{MAXIR}	Maximum Input Register Frequency			125		MHz
t_{SIL}	Input Latch Setup Time			2		ns
t_{HIL}	Input Latch Hold Time			2.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				17	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				18	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			10		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (continued)

Parameter Symbol	Parameter Description	-10		Unit
		Min	Max	
t_{IGS}	Input Latch Gate to Output Latch Setup	11		ns
t_{WIGL}	Input Latch Gate Width LOW	4		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		18	ns
t_{ARW}	Asynchronous Reset Width	10		ns
t_{ARR}	Asynchronous Reset Recovery Time	10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		18	ns
t_{APW}	Asynchronous Preset Width	10		ns
t_{APR}	Asynchronous Preset Recovery Time	10		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		15	ns

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		235		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	11		14		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	1/(t_S + t_{CO})	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback	1/(t_{WL} + t_{WH})		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				10		13		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					11		12	ns
t_{GWL}	Gate Width LOW				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	15		20		ns
				T-type	16		21		ns
t_{WICL}	Input Register Clock Width			LOW	6		8		ns
t_{WICH}				HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	1/(t_{WICL} + t_{WICH})			83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		ns
t_{HIL}	Input Latch Hold Time				2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					22		27	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				16		21		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-15		-20		Unit
		Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)	15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		15		20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *Parameters measured with 32 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A =–40°C to +85°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A) Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		235		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-18		-24		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	12		16		ns
				T-type	13.5		17		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					12		14.5	ns
t_{WL}	Clock Width			LOW	7.5		10		ns
t_{WH}				HIGH	7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		32		MHz
				T-type	38		30.5		MHz
		Internal Feedback (f_{CNT})		D-type	53		38		MHz
				T-type	44		34.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		66.5		50		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				12		16		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					13.5		14.5	ns
t_{GWL}	Gate Width LOW				7.5		10		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					20.5		26.5	ns
t_{SIR}	Input Register Setup Time				2.5		2.5		ns
t_{HIR}	Input Register Hold Time				3.5		4		ns
t_{ICO}	Input Register Clock to Combinatorial Output					22		28	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	18		24		ns
				T-type	19.5		25.5		ns
t_{WICL}	Input Register Clock Width			LOW	7.5		10		ns
t_{WICH}				HIGH	7.5		10		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			66.5		50		MHz
t_{SIL}	Input Latch Setup Time				2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				3.5		4		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					24		30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					26.5		32.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				14.5		18		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				19.5		25.5		ns
t_{WIGL}	Input Latch Gate Width LOW				7.5		10		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches					23		29	ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2) (continued)

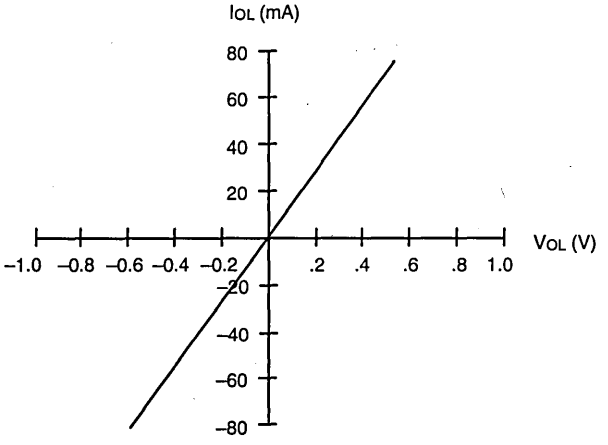
Parameter Symbol	Parameter Description	-18		-24		Unit
		Min	Max	Min	Max	
t_{AR}	Asynchronous Reset to Registered or Latched Output		24		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	12		18		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		24		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)	18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	12		18		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		18		24	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *Parameters measured with 32 outputs switching.*

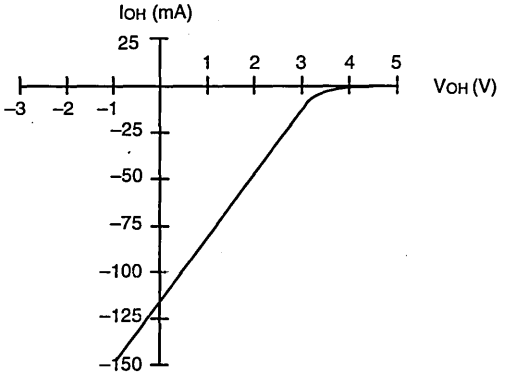
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



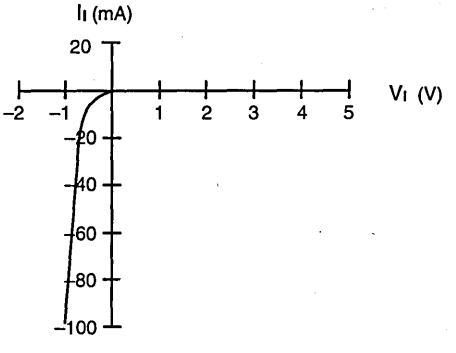
Output, LOW

14132I-6



Output, HIGH

14132I-7

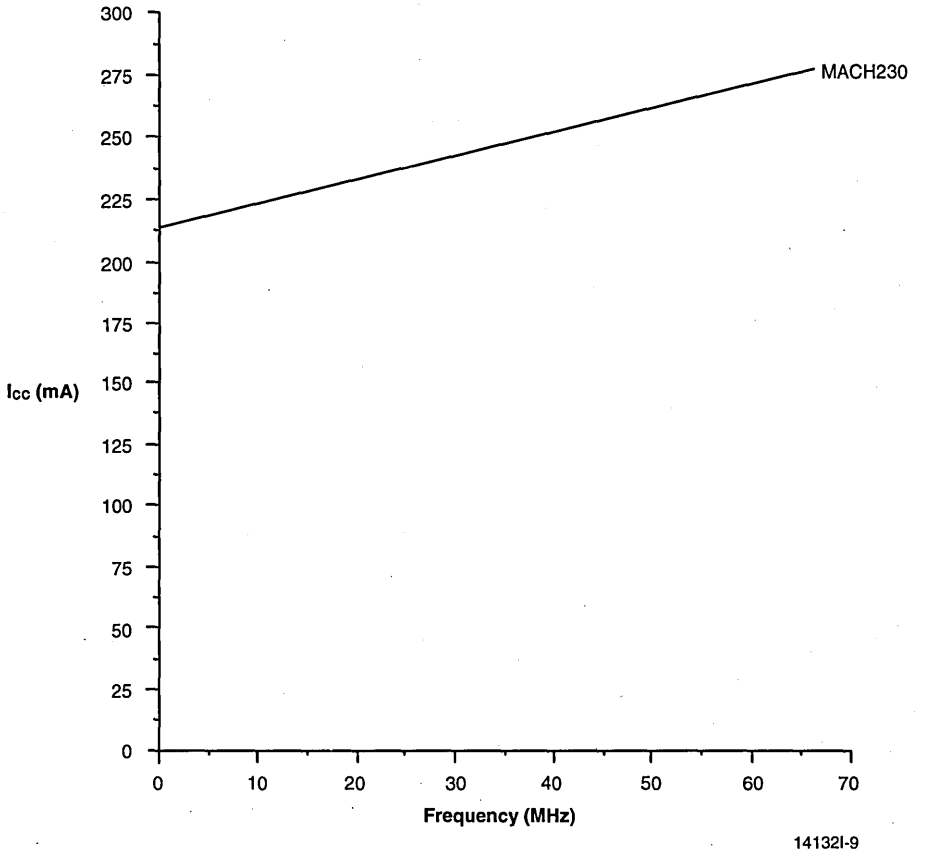


14132I-8

Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

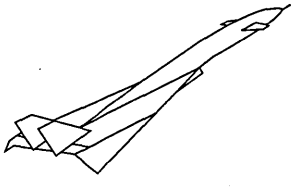
TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Units
θ_{jc}	Thermal impedance, junction to case		5	°C/W
θ_{ja}	Thermal impedance, junction to ambient		20	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	17	°C/W
		400 lfpm air	14	°C/W
		600 lfpm air	12	°C/W
		800 lfpm air	10	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.



FINAL COM'L: -7.5/10/12/15/20

MACH231-7/10/12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 128 Macrocells
- 7.5 ns t_{PD}
- 133 MHz f_{CNT}
- 70 Bus-Friendly Inputs
- Peripheral Component Interconnect (PCI) compliant
- Programmable power-down mode
- 64 Outputs
- 128 Flip-flops; 4 clock choices
- 8 "PAL32V16" blocks with buried macrocells
- Pin-compatible with MACH130, MACH131, MACH230, MACH435
- Improved routing over the MACH230

GENERAL DESCRIPTION

The MACH231 is a member of AMD's EE CMOS Performance Plus MACH 2 device family. This device has approximately twelve times the logic macrocell capability of the popular PAL22V10 without loss of speed.

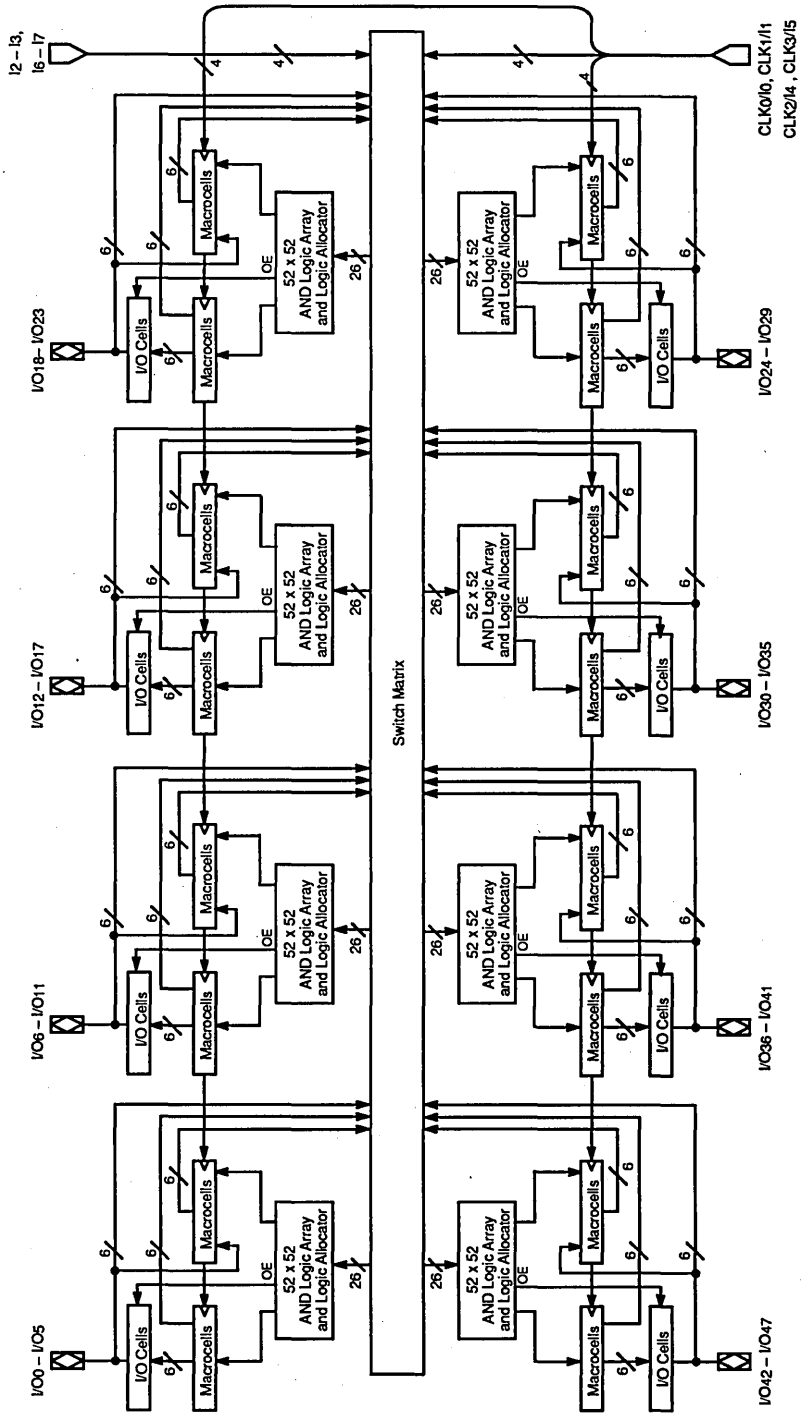
The MACH231 consists of eight PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH231 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH231 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

Publication# 19603 Rev. B Amendment/0
Issue Date: May 1995

BLOCK DIAGRAM

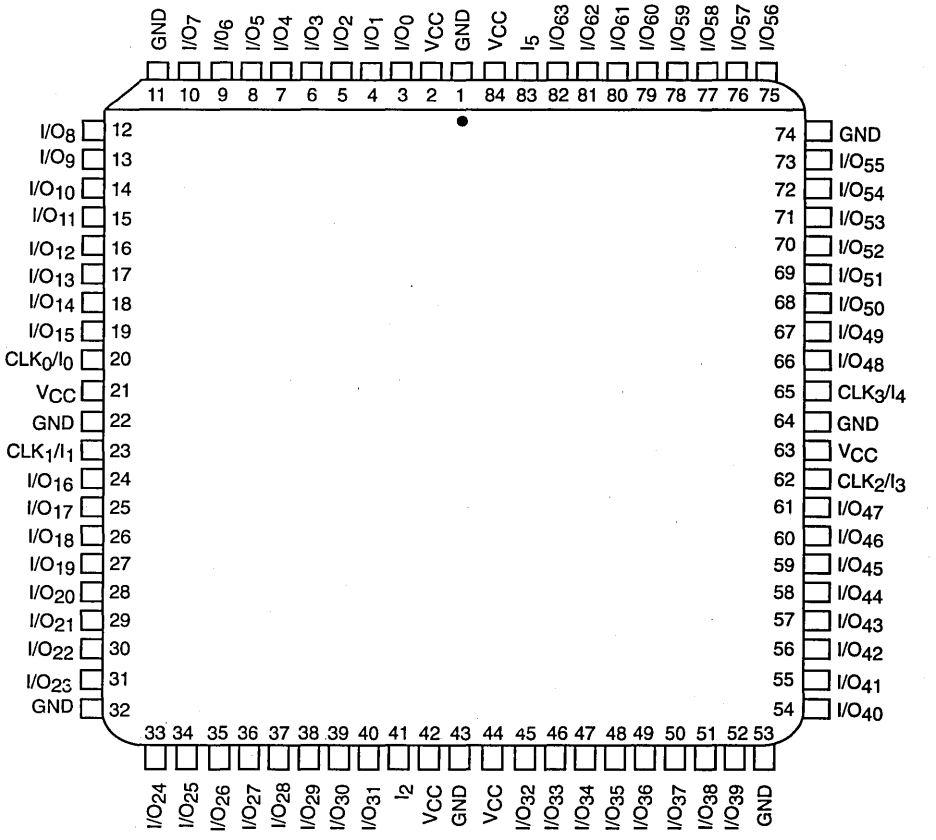


19603B-1

CONNECTION DIAGRAM

Top View

PLCC



19603B-2

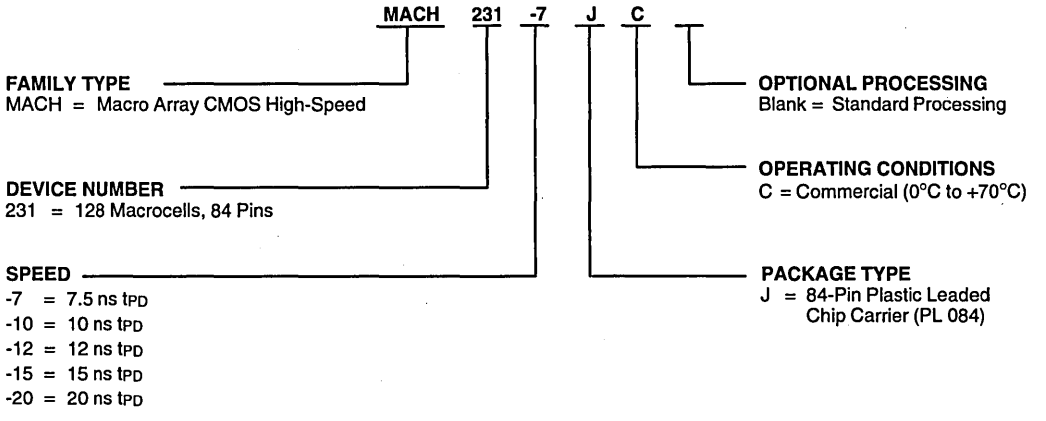
Note:
Pin-compatible with MACH130, MACH131, MACH230, and MACH435.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH231-7	JC
MACH231-10	
MACH231-12	
MACH231-15	
MACH231-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH231 consists of eight PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH231 (Figure 1) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 32 inputs. This makes the PAL block look effectively like an independent "PAL32V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH231 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH231 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH231 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_{14}		C_{13}, C_{14}, C_{15}
	M_{15}	C_{14}, C_{15}

The Macrocell

The MACH231 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

Power-Down Mode

The MACH231 features a programmable low-power mode in which individual signal paths can be programmed as low power. These low-power speed paths will be slightly slower than the non-low-power paths.

This feature allows speed critical paths to run at maximum frequency while the rest of the paths operate in low power mode resulting in power savings of up to 50%. If all signals in a PAL block are low-power, then total power is reduced further.

The I/O Cell

The I/O cell in the MACH231 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

Bus-Friendly Inputs and I/Os

The MACH231 inputs and I/Os include two inverters in series which loop back to the input. This double inversion reinforces the state of the input and pulls the voltage away from the threshold voltage. Unlike a pull-up, this configuration cannot cause contention on a bus. For an illustration of this configuration, please turn to the I/O and Equivalent Schematics section at the end of this data book.

PCI Compliance

The MACH231-7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH231-7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without predictable timing, PCI compliance is dependent upon routing and product term distribution.

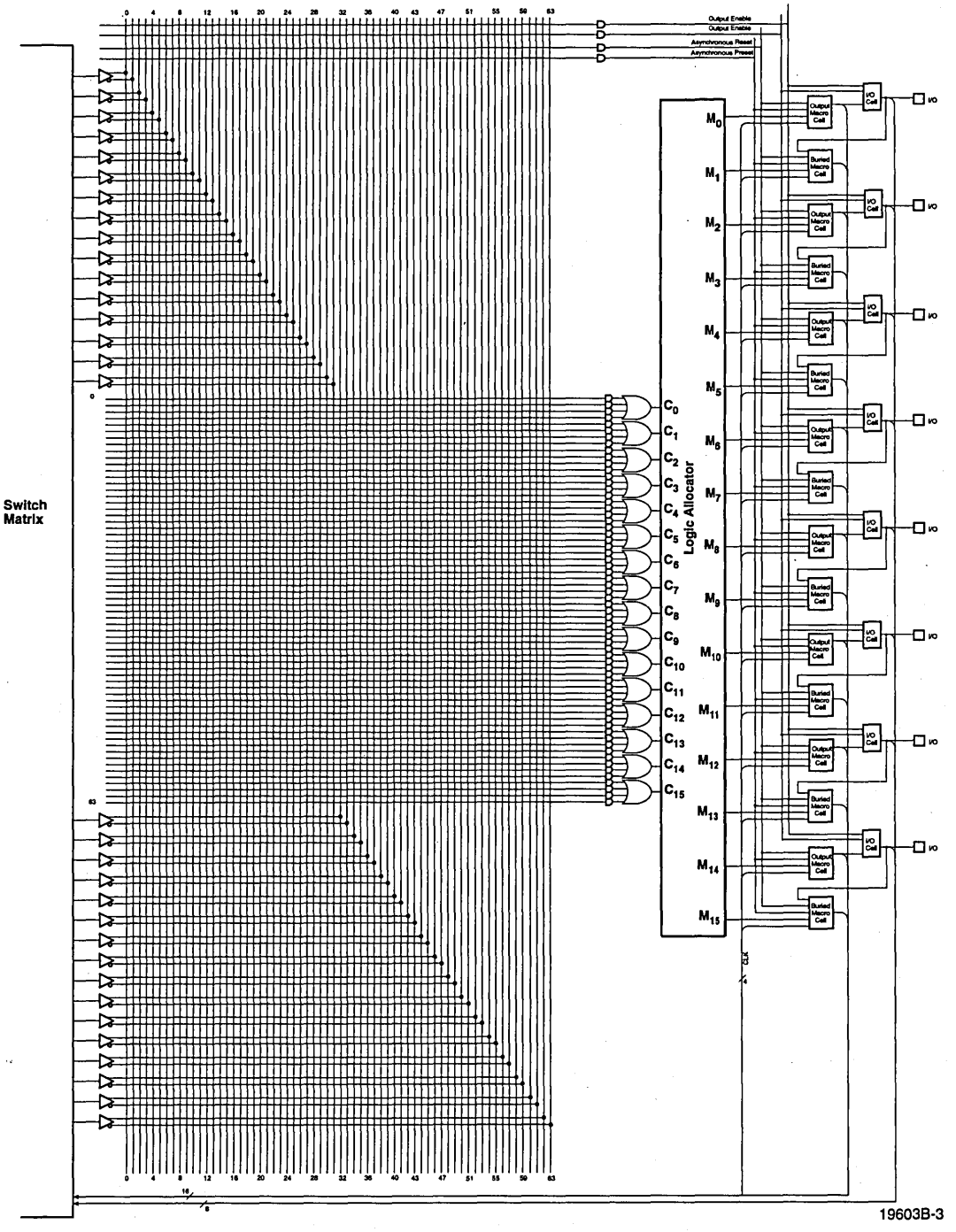


Figure 1. MACH231 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –40°C to +150°C

Ambient Temperature
with Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Static)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5 V, f = 0 MHz, T_A = 25°C (Note 4)		135		mA
	Supply Current (Active)	V_{CC} = 5 V, f = 1 MHz, T_A = 25°C (Note 4)		150		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = V_{CC} - 0.5$ V	V_{CC} = 5.0 V, T_A = 25°C	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	10	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-7		-10		Unit
				Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				7.5		10	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock		D-type	5.5		6.5		ns
			T-type	6.5		7.5		ns
t_H	Register Data Hold Time			0		0		ns
t_{CO}	Clock to Output				5		6.5	ns
t_{WL}	Clock		LOW	3		4		ns
t_{WH}	Width		HIGH	3		4		ns
f_{MAX}	Maximum Frequency	External Feedback	D-type	95		77		MHz
			T-type	87		72		MHz
		Internal Feedback (f_{CNT})	D-type	133		100		MHz
			T-type	125		91		MHz
		No Feedback		166.7		125		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			5.5		8		ns
t_{HL}	Latch Data Hold Time			0		0		ns
t_{GO}	Gate to Output				6		7.5	ns
t_{GWL}	Gate Width LOW			3		4		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				9.5		14	ns
t_{SIR}	Input Register Setup Time			2		2		ns
t_{HIR}	Input Register Hold Time			2		2.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output				11		15.5	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-type	9		11		ns
			T-type	10		12		ns
t_{WICL}	Input Register		LOW	3		4		ns
t_{WICH}	Clock Width		HIGH	3		4		ns
f_{MAXIR}	Maximum Input Register Frequency			166.7		125		MHz
t_{SIL}	Input Latch Setup Time			2		2		ns
t_{HIL}	Input Latch Hold Time			2		2.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				12		17	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				14		18	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			7.5		10		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (continued)

Parameter Symbol	Parameter Description	-7		-10		Unit
		Min	Max	Min	Max	
t_{IGS}	Input Latch Gate to Output Latch Setup	10		11		ns
t_{WIGL}	Input Latch Gate Width LOW	3		4		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		11.5		16	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		9.5		18	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	5		10		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	5.5		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		9.5		18	ns
t_{APW}	Asynchronous Preset Width (Note 1)	5		10		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	5		10		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		9.5		15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9.5		15	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
with Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		135		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		150		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = V_{CC} - 0.5$ V	$V_{CC} = 5.0$ V, $T_A = 25°C$	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	f = 1 MHz	10	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-15		-20		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock			LOW	6		6		8		ns
t_{WH}	Width			HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	76.9		66.6		50		MHz
				T-type	71.4		62.5		47.6		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				8		10		13		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output					8.5		11		12	ns
t_{GWL}	Gate Width LOW				6		6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14.5		17		22	ns
t_{SIR}	Input Register Setup Time				2		2		2		ns
t_{HIR}	Input Register Hold Time				2.5		2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					16		18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	12		15		20		ns
				T-type	13		16		21		ns
t_{WICL}	Input Register			LOW	6		6		8		ns
t_{WICH}	Clock Width			HIGH	6		6		8		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		80		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2.5		2		2		ns
t_{HIL}	Input Latch Hold Time				3		2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19.5		22		27	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				10.5		12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				13.5		16		21		ns

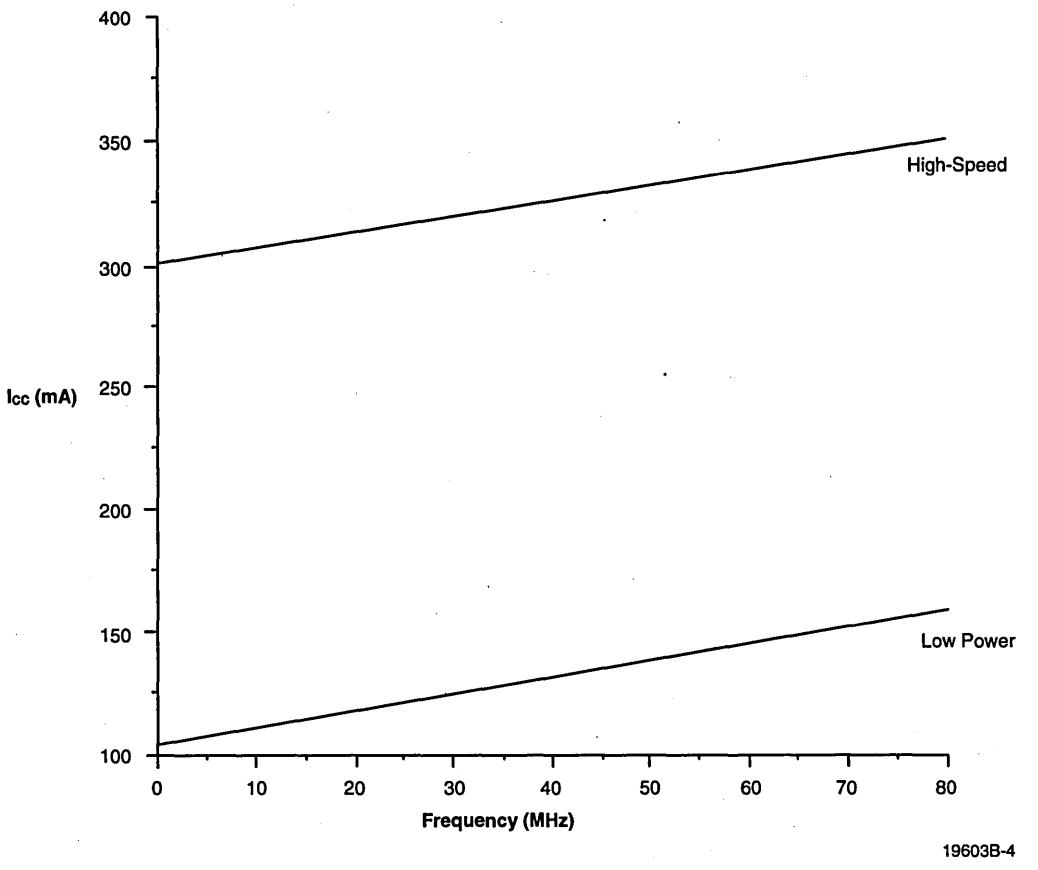
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	6		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		17		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		12		15		20	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

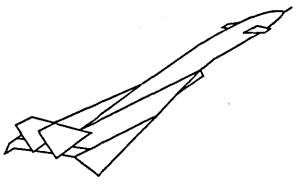
TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Units
θ_{jc}	Thermal impedance, junction to case		5	°C/W
θ_{ja}	Thermal impedance, junction to ambient		20	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	17	°C/W
		400 lfpm air	14	°C/W
		600 lfpm air	12	°C/W
		800 lfpm air	10	°C/W

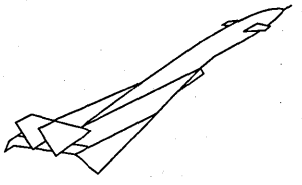
Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.



CHAPTER

2 MACH 3 AND 4 DEVICE FAMILIES



FINAL

MACH 3 and 4 Device Families

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-performance, high-density electrically-erasable CMOS PLD families**
- **Predictable design-independent 12-, 15- and 20-ns speeds**
- **High density, pin count**
  - — 3500–10,000 PLD Gates
  - — 84–208 Pins
  - — 96–384 Registers
- **Input and output switch matrices increase ability to hold a fixed pinout**
- **JTAG, 5-V in-circuit programmability on devices with more than 84 pins**
- **Synchronous and asynchronous modes available for each macrocell**
  - — Clock generator in each PAL block for programmable clocks, edges in either mode
  - — Individual clock, initialization product terms in asynchronous mode
- **Central, input, and output switch matrices**
  - — 100% Routability
- **Up to 20 product terms per function**
- **96–256 configurable macrocells**
  - — D/T/J-K/S-R Registers, latches
  - — Synchronous or asynchronous mode
  - — Programmable polarity
  - — Reset/preset swapping
- **XOR gate available**
- **Registered/latched inputs on MACH 4 series**
- **Extensive third-party software and programmer support through FusionPLD partners**

PRODUCT SELECTOR GUIDE

Device	Pins	Macrocells	PLD Gates	Max Inputs	Max Outputs	Max Flip-Flops	JTAG/ 5 V Prog	Speed
MACH 3 Family								
MACH355	144	96	3500	102	96	96	Y	15, 20
MACH 4 Family								
MACH435	84	128	5000	70	64	192	N	12, 15, 20, Q-25
MACH445	100	128	5000	70	64	192	Y	12, 15, 20
MACH465	208	256	10,000	146	128	384	Y	12, 15, 20

GENERAL DESCRIPTION

The MACH (Macro Array CMOS High-speed/density) family provides a new way to implement large logic designs in a programmable logic device. AMD has combined an innovative architecture with advanced electrically-erasable CMOS technology to offer a device with many times the logic capability of the industry's most popular existing PAL device solutions at comparable speed and cost.

The second-generation MACH devices provide approximately three times the density and register count, and two times the amount of I/O of the original MACH 1 and 2 families. By increasing the pin count, adding functionality, and improving routing, the MACH 3 and 4 families build upon the strength of the MACH architecture without sacrificing predictable timing.

Their unique architecture makes these devices ideal for replacing large amounts of TTL, PAL-device, glue, and gate-array logic. They are the first devices to provide such increased functionality with completely predictable, deterministic speed.

The MACH devices consist of PAL blocks interconnected by a programmable central switch matrix

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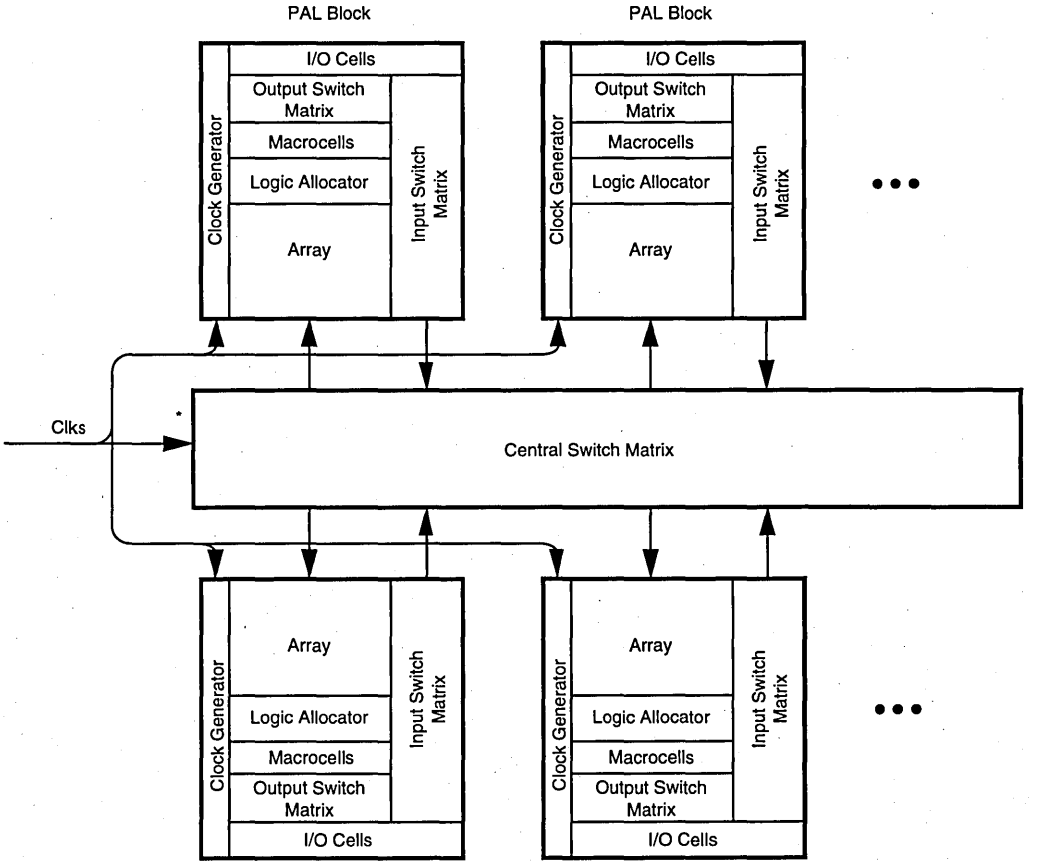
(Figure 1). Designs that consist of several interconnected functional modules can be efficiently implemented by placing the modules into PAL blocks. Designs that are not as modular can also be readily implemented since the central switch matrix provides a very high level of connectivity between PAL blocks.

The use of input and output switch matrices allows logic to be implemented independent of pin connections. This allows greater flexibility when making initial pin assignments for PCB layout, or when trying to maintain the pinout through design changes. The internal arrangement of resources is managed automatically by the design software, so that the designer does not have to be concerned with the logic implementation details.

AMD's FusionPLD program allows MACH device designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide timely, accurate, and quality support. This ensures that a designer does not have to buy a complete new set of tools for each new device, but rather can use the tools with which he or she is already familiar. The MACH devices can programmed on conventional PAL device programmers. Devices with greater than 84 pins also have 5-volt programming and JTAG circuitry, enabling program and test of the devices while soldered onto the board.

MACH devices are manufactured using AMD's state-of-the-art electrically-erasable CMOS process for high performance and logic density. CMOS EE technology provides 100% testability, reducing both prototype development costs and production costs.



*The MACH465 has dedicated clock inputs.

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Figure 1. MACH 3 and 4 Block Diagram

Design Methodology

Design tools for all MACH devices are widely available from both AMD and third-party software vendors. AMD supplies MACHXL software as a low-cost, baseline tool set. AMD also supplies AMD-only versions of popular, feature-rich third-party tools, and works with leading third-party vendors to ensure broad MACH device support. Please see the "Design Tool Support for MACH Devices" section toward the end of this Data Book for more information.

Design entry can be the same as that used for PAL, MACH 1, and MACH 2 devices. The basic logic processing steps are the same steps that are needed to process and minimize logic for any PAL device. Simulation is available for verifying the correct behavior of the device. Functional (unit-delay) simulation of MACH devices is supported in all approved software packages, and other options for simulating the timing and board-level behavior of the MACH devices are available. The end result is a JEDEC file that can be downloaded to a programmer for device configuration.

MACH device design methodology differs somewhat from that of a PAL device due to the automatic design fitting procedure that the software performs. Designs written by logic designers—whether by schematic capture, state machine equations, Boolean equations, or behavioral languages—are partitioned and placed into the PAL blocks of the MACH device. While this procedure is handled automatically by the software, the software can also accept manual direction based upon the user's working knowledge of the design. The overall device utilization provided by the fitter will vary from design to design, but in general significantly higher utilization can be expected from the MACH 3 and 4 families than from the MACH 1 and 2 devices due to the additional routing resources. In addition, MACH 3 and 4 device designs with higher utilization are more likely to retain the same pinout when design changes are made since the output switch matrix allows a pin to be driven by any of a number of macrocells.

AMD recommends allowing the software to decide the best fit and pin placement automatically for the first design iteration. This will provide the best chance of fitting. With this approach, large designs can be implemented incrementally, starting with low device utilization and building up by adding logic until the device is full. This generally means that designs are done without any specific pinout assignments, with the final pinout decided by the software. It is possible to "pre-place" signals, and, given the plentiful routing resources, pre-placement is very likely to be successful on the MACH 3 and 4 families. However, the most successful design fit can still be achieved by allowing the software as much fitting flexibility as possible.

The design is partitioned and placed into the MACH device by the software so as not to affect the performance of the design. With designs that do not fit it is possible to make some performance tradeoffs to aid in fitting (for example, by optimizing the flip-flop type or passing through the device more than once), but those tradeoffs must be specifically requested, and any additional delays are entirely predictable.

Once an initial design fits, there may be subsequent changes to the design. This is important if board layout has already started based on the original pinout. A major role of the input and output switch matrices is to allow such changes without impacting the original pinout. Most designs can easily target 100% utilization without jeopardizing the ability to make design changes and maintain pinout.

SECOND GENERATION MACH DEVICES

The MACH 3 and MACH 4 families consist of several members differentiated primarily by pin count and number of macrocells. The MACH 3 family has one macrocell per I/O pin; the MACH 4 family has two macrocells per I/O pin. In addition, the MACH 4 family has input registers. The MACH 4 register count is therefore three times the I/O pin count.

The devices range in pin count from 84 to 208; in number of macrocells from 96 to 256; and in number of registers from 96 to 384. All devices above 84 pins are provided in space-saving PQFP packages, with JTAG and 5-V, in-circuit programmability. The 84-pin MACH435 comes in a PLCC package, without JTAG or 5-V programming, for pin-compatibility with the MACH130 and MACH230. Its architecture is available with JTAG and 5-V programmability in the 100-pin MACH445.

Functional Description

The fundamental architecture of the MACH devices consists of multiple optimized PAL blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks, and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of multiple devices.

Most pins are I/O pins that can be used as inputs, output, or bidirectional pins. There are some dedicated input pins, but all macrocells have internal feedback, allowing the pin to be used as an input if the macrocell signal is not needed externally.

The key to being able to make effective use of these devices lies in the interconnect schemes. Because of the programmable interconnections, the product term arrays have been decoupled from the central switch matrix; the macrocells have been decoupled from the product terms through the logic allocator; and the I/O pins have been decoupled from the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to place and route designs efficiently.

In a MACH device, all signals incur the same delays, regardless of routing. Performance is design-independent, and is known before the design is begun.

The PAL Blocks

The PAL blocks resemble independent PAL devices on the chip. This provides for logic functions that need the complete interconnect that a PAL device provides. PAL blocks communicate with each other through the central switch matrix.

Each PAL block consists of:

- a product-term array
- a logic allocator
- macrocells
- an output switch matrix
- I/O cells
- an input switch matrix
- a clock generator

The logic allocator distributes the product terms to the macrocells, as required by each individual design. The macrocell configures the signal largely by determining the storage characteristics. Macrocell signals are routed to I/O cells and the I/O pins by the output switch matrix. The I/O cells on MACH 4 devices also allow for registered or latched inputs. The input switch matrix optimizes the routing of input signals into the central switch matrix.

The clock generator uses the four global clock inputs to generate a set of four clock signals available throughout the PAL block. Various combinations of clock signals in both true and complement form can be generated.

Each PAL block also contains an asynchronous reset product term and an asynchronous preset product term to be used for synchronous-mode macrocells. This allows synchronous flip-flops within a single PAL block to be initialized as a bank. Macrocells implemented in asynchronous mode are not affected by the PAL-block initialization.

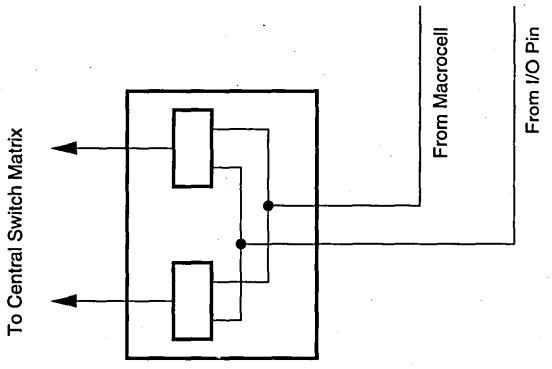
The Central Switch Matrix

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that only return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in MACH devices communicate with each other with consistent, predictable delays.

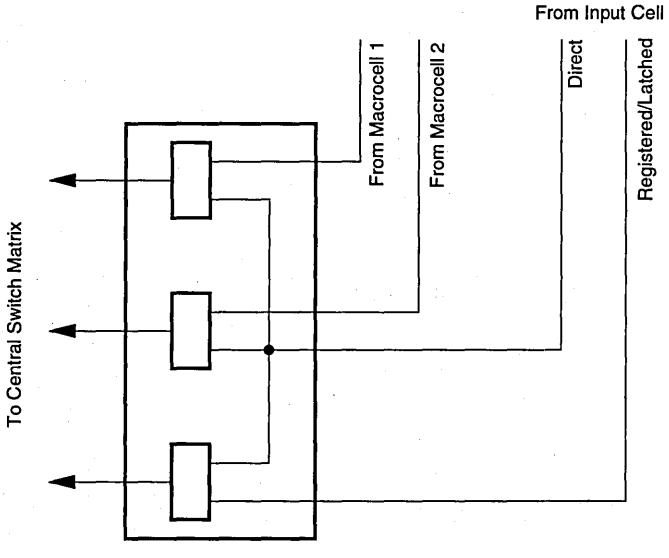
The central switch matrix makes a MACH device more than just several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

The Input Switch Matrix

The input switch matrix (Figure 2) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



a. MACH 3; one per macrocell



b. MACH 4; one for every two macrocells

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Figure 2. Input Switch Matrix

PAL Block Clock Generation

Each MACH 3 and 4 device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 3). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals; Table 1 lists the possible combinations.

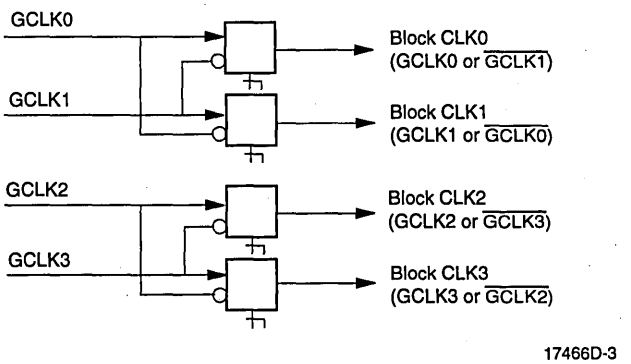


Figure 3. PAL Block Clock Generator

Table 1. PAL Block Clock Combinations

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2	GCLK3
X	X	$\overline{\text{GCLK3}}$	GCLK3
X	X	GCLK2	$\overline{\text{GCLK2}}$
X	X	$\overline{\text{GCLK3}}$	$\overline{\text{GCLK2}}$

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

Synchronous and Asynchronous Operation

The MACH 3 and 4 families can perform synchronous or asynchronous logic. Each individual cell can be programmed as synchronous or asynchronous, allowing unlimited "mixing and matching" of the two logic styles. The selection of synchronous or asynchronous mode affects the logic allocator and the macrocell, since product terms used for logic in the synchronous mode are used for control functions in the asynchronous mode.

The Product Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 2), and are provided in both true and complement forms for efficient logic implementation.

Table 2. PAL Block Inputs

Device	Number of Inputs to PAL Block
MACH355	33
MACH435	33
MACH445	33
MACH446	33
MACH465	34

Because the number of product terms available for a given logic function is not fixed, the full sum of products is not realized in the array. The product terms drive the logic allocator, which allocates the appropriate number of product terms to generate the function.

The Logic Allocator

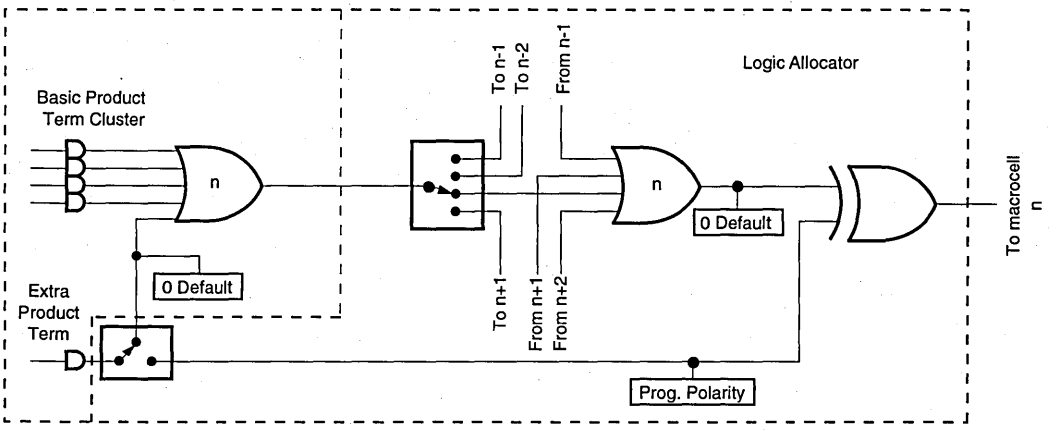
Within the logic allocator, product terms are allocated to macrocells in "product term clusters." The availability and distribution of product term clusters are automatically considered by the software as it places and routes functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many

product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over.

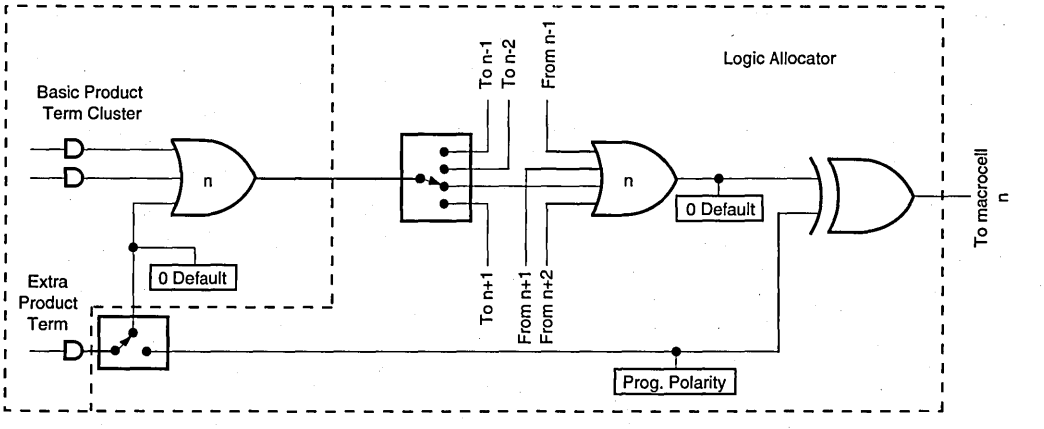
The logic allocator has two fundamental modes, depending on whether the macrocell is synchronous or asynchronous. The synchronous mode (Figure 4a) has a basic product term cluster of four product terms; the asynchronous mode (Figure 4b) has a basic cluster of two product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 5 and 6.



a. Synchronous Mode



b. Asynchronous Mode

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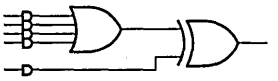
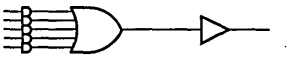
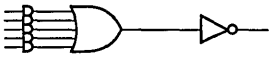
Figure 4. Logic Allocator. Configuration of cluster "n" set by mode of macrocell "n".



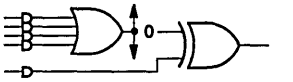
a. Basic cluster with XOR



b. Extended cluster, active high



c. Extended cluster, active low

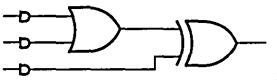


d. Basic cluster routed away; single-product-term, active high

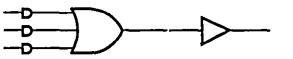
e. Extended cluster routed away

17466D-5

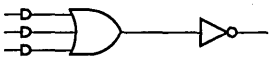
Figure 5. Logic Allocator Configurations: Synchronous Mode



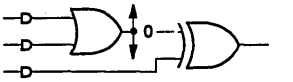
a. Basic cluster with XOR



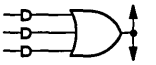
b. Extended cluster, active high



c. Extended cluster, active low



d. Basic cluster routed away; single-product-term, active high



e. Extended cluster routed away

17466D-6

Figure 6. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

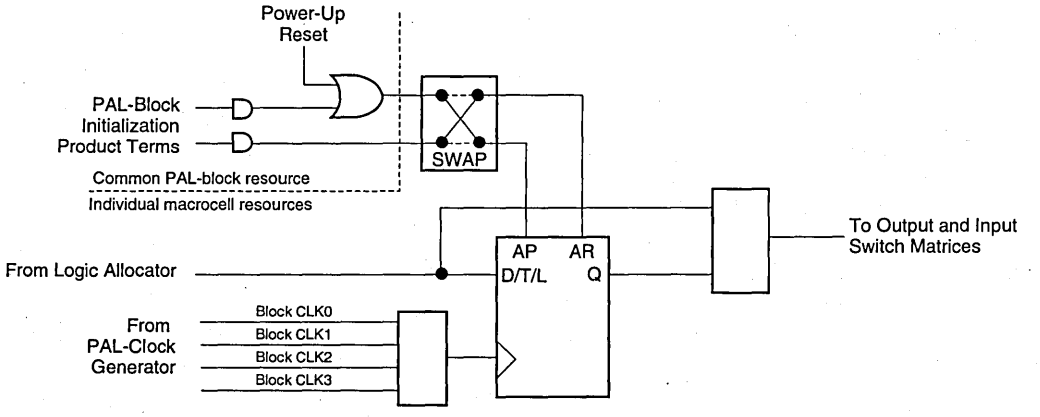
If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is

routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

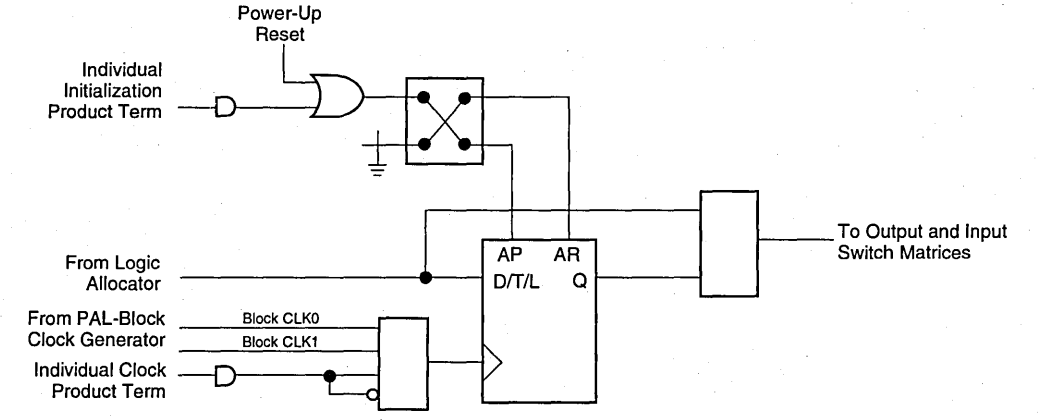
Product term clusters do not "wrap" around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available. Refer to the individual product data sheets for details.

The Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 7). The mode chosen only affects clocking and initialization in the macrocell.



a. Synchronous Mode



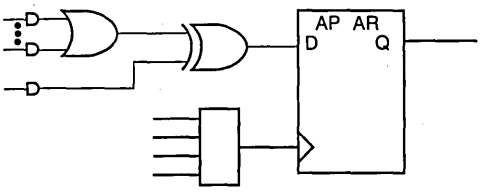
b. Asynchronous Mode

17466D-7

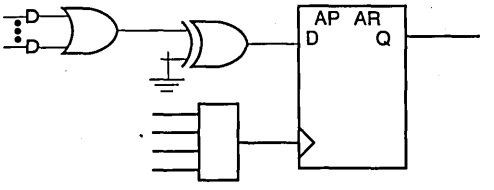
Figure 7. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

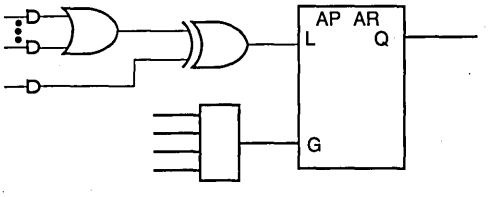
The flip-flop can be configured as a D-type, T-type, J-K, or S-R register or latch. The primary flip-flop configurations are shown in Figure 8, although others are possible. Flip-flop functionality is defined in Table 3. Note that a J-K latch is unadvisable, as it will cause oscillation if both J and K inputs are HIGH.



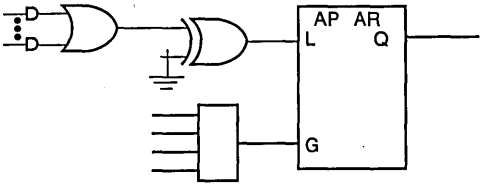
a. D-type with XOR



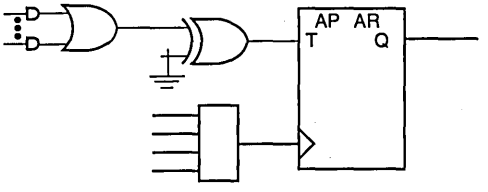
b. D-type with programmable D polarity



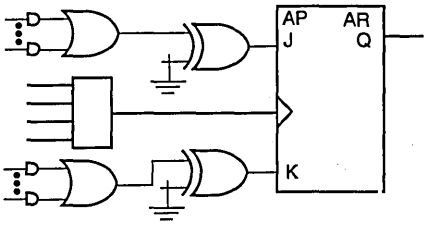
c. Latch with XOR



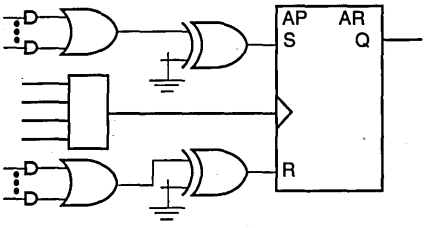
d. Latch with programmable polarity



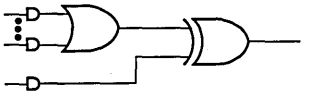
e. T-type with programmable T polarity



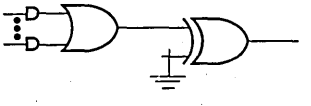
f. J-K with programmable J and K polarity



g. S-R with programmable S and R polarity



h. Combinatorial with XOR



i. Combinatorial with programmable polarity

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Figure 8. Primary Macrocell Configurations

Table 3. Register/Latch Operation

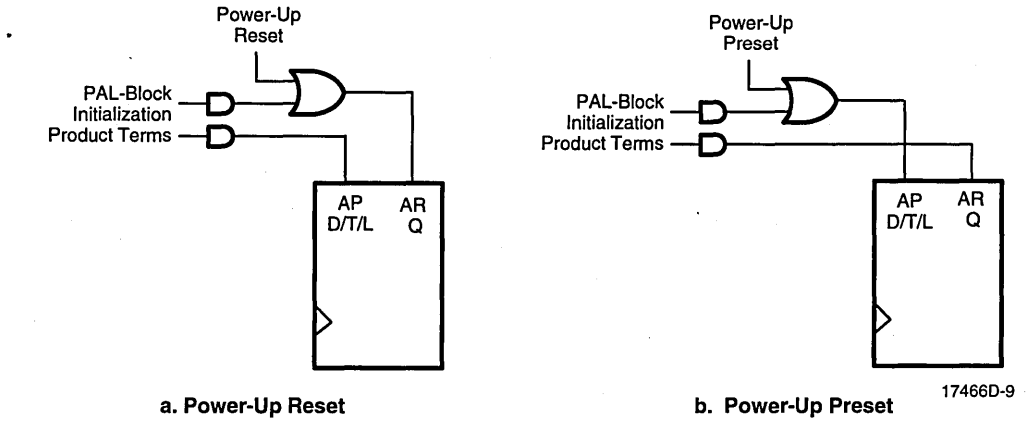
Configuration	Input(s)	CLK/LE*	Q+
D-type Register	D=X	0, 1, ↓(↑)	Q
	D=0	↑(↓)	0
	D=1	↑(↓)	1
T-type Register	T=X	0, 1, ↓(↑)	Q
	T=0	↑(↓)	Q
	T=1	↑(↓)	$\overline{Q}$
J-K Register	J=K=X	0, 1, ↓(↑)	Q
	J=0, K=0	↑(↓)	Q
	J=0, K=1	↑(↓)	0
	J=1, K=0	↑(↓)	1
	J=1, K=1	↑(↓)	$\overline{Q}$
S-R Register	S=R=X	0, 1, ↓(↑)	Q
	S=0, R=0	↑(↓)	Q
	S=0, R=1	↑(↓)	0
	S=1, R=0	↑(↓)	1
	S=1, R=1	↑(↓)	Undefined
D-type Latch	D=X	1(0)	Q
	D=0	0(1)	0
	D=1	0(1)	1

**Polarity of CLK/LE can be programmed.*

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 9), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-Up Reset **b. Power-Up Preset**

Figure 9. Synchronous Mode Initialization Configurations

A subtle difference between MACH 1 and 2 devices and the MACH 3 and 4 devices is that the original devices have programmable output polarity; that is, the polarity control comes after the flip-flop. In the new MACH 3 and 4 architecture, the flip-flop input polarity is programmable. For designs that can be implemented on both the older and newer devices, this makes no difference except that in the older architecture, reset and preset values are affected by polarity; in the new architecture they are not. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility and design compatibility between the old and new architectures.

In asynchronous mode (Figure 10), a single individual product term is provided for initialization. It can be selected to control reset or preset.

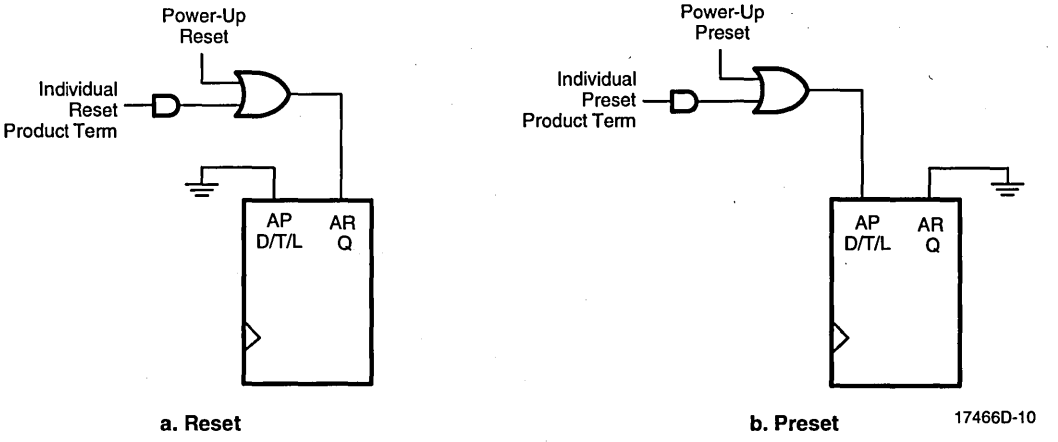


Figure 10. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature affects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 4.

The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 4. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE*	Q+
0	0	X	See Table 3
0	1	X	1
1	0	X	0
1	1	X	0

**Transparent latch is unaffected by AR, AP.*

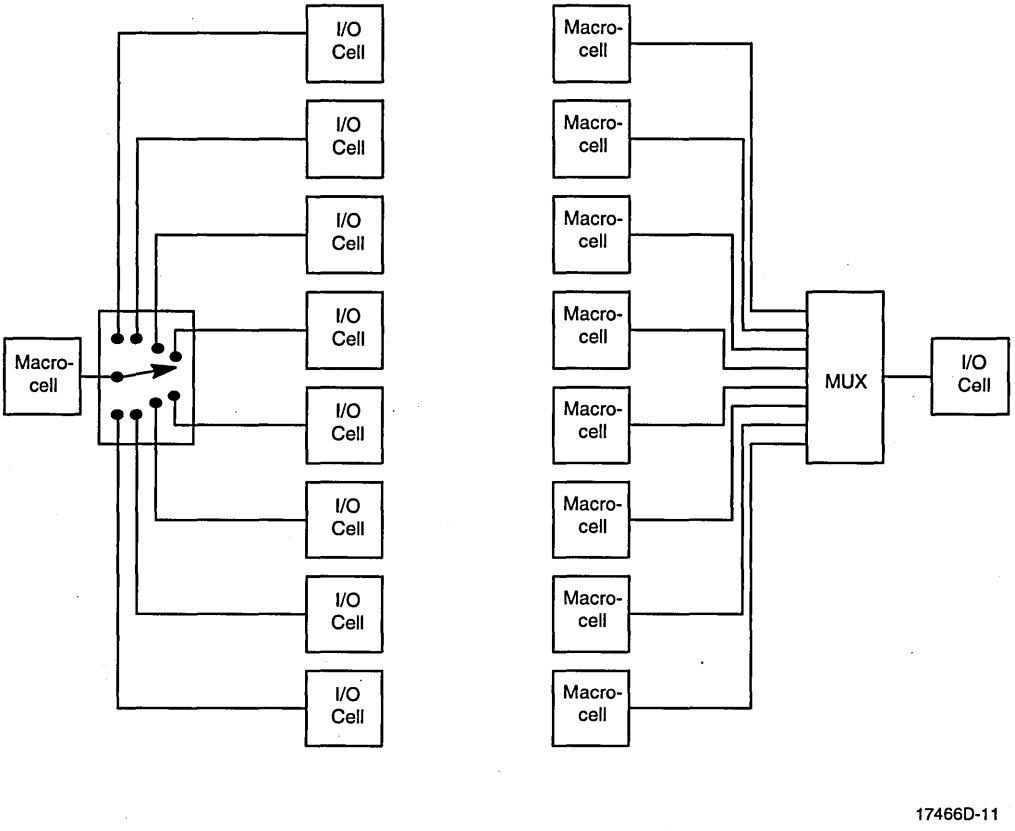
The Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout, and allows design changes that will not affect pinout.

In MACH 3 devices, each PAL block has the same number of macrocells as I/O cells. The output switch matrix allows the design to mix macrocells and I/O pins within the PAL block according to Figure 11. Each I/O cell can choose from eight macrocells; each macrocell has a choice of eight I/O cells.

In MACH 4 devices, each PAL block has twice as many macrocells as I/O cells. The MACH 4 output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 12. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells.

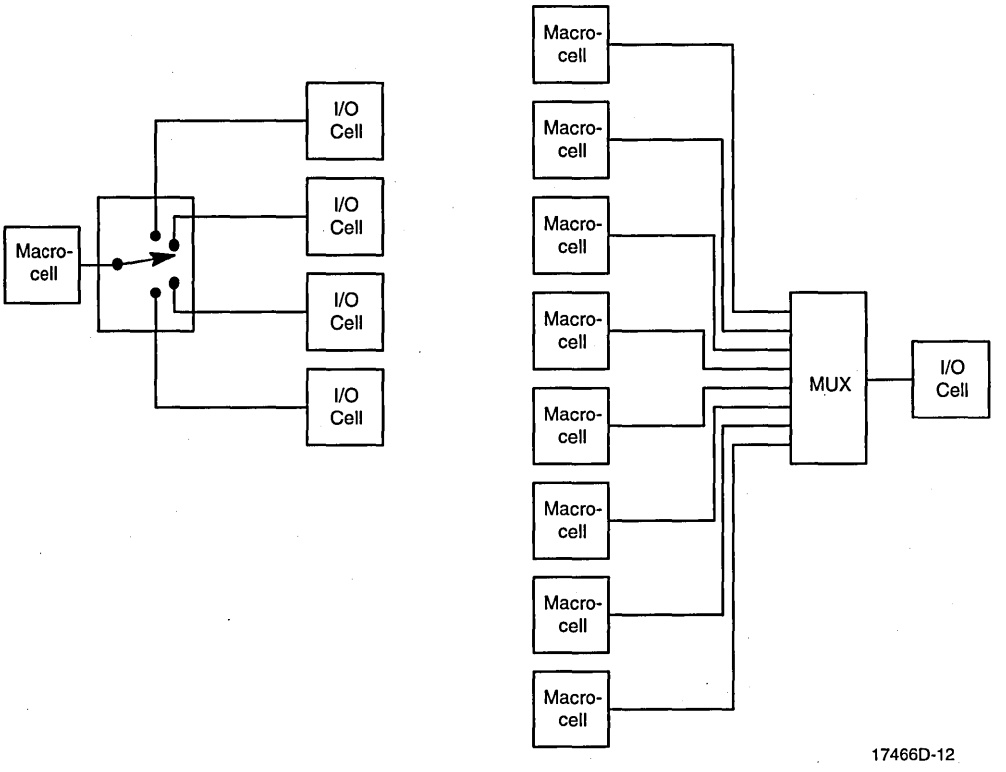
Specific combinations allowed for each device are tabulated in the individual product data sheets. No macrocell may drive more than one I/O cell.



a. Macrocell drives one of 3 I/Os

b. I/O can choose one of 8 macrocells

Figure 11. MACH 3 Output Switch Matrix



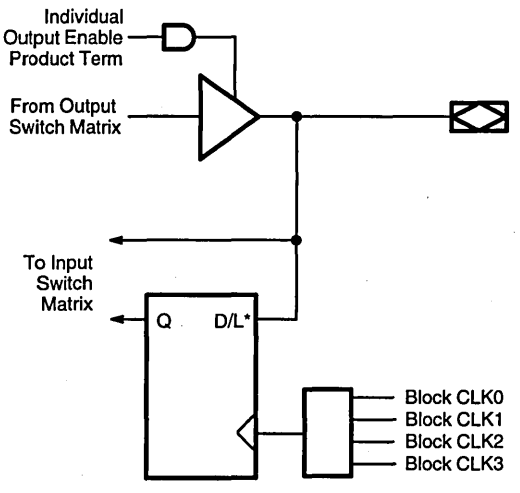
a. Macrocell drives one of 4 I/Os

b. I/O can choose one of 8 macrocells

Figure 12. MACH 4 Output Switch Matrix

The I/O Cell

The I/O cell (Figure 13) simply consists of programmable output enable, a feedback path, and in MACH 4 devices, a flip-flop. An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.



**Flip-flop available on MACH 4 devices only.*

Figure 13. I/O Cell

The MACH 4 I/O cell contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as "time-domain-multiplexed" data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the MACH 4 I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

JTAG Testability Circuit

All MACH 3 and 4 devices with greater than 84 leads have JTAG testability circuits built in. This allows functional testing of the device through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

The only MACH 3 and 4 device without JTAG is the MACH435, which is pin-compatible with the 84-pin MACH130, MACH131, MACH230 and MACH231. This device has preload and observability functions. All registers on the MACH435 can be preloaded to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

In addition to the control offered by preload, testing requires observability of the internal state of the device following a sequence of vectors. The MACH435 offers an observability feature that allows the user to send hidden buried register values to observable output pins.

5-V, In-Circuit Programmability and Erasability

Because high-pin-count PQFPs have leads that are subject to damage, 5-V, in-circuit programmability and erasability have been provided. This allows the devices to be soldered on the board prior to programming. Once on the board, the device leads are immobile, and can be programmed without damage. Because there are no "supervoltages" (voltages above the standard TTL range), devices that share lines on the board will not be damaged by high voltages. Programming is enabled by a dedicated pin; this pin is pulled high during normal operation.

Power-Up Reset/Preset

All flip-flops power up to a known state for predictable system initialization. The power-up value can be programmed through the initialization swapping selection feature. The V_{CC} rise must be monotonic and clock must be inactive until the reset delay time, 10 µs maximum, has elapsed.

Security Bit

A security bit is provided on the MACH devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. Preload and the JTAG circuitry can be used independently of the security bit, since a separate security bit is provided to disable these features. The bits can only be erased in conjunction with the array during an erase cycle.

Quality and Testability

The MACH devices offer a very high level of built-in quality. The fact that the device is erasable allows direct verification of all AC and DC parameters. In addition, this verifies complete programmability and functionality

of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The MACH devices are fabricated with AMD's advanced electrically-erasable floating-gate 0.5 and 0.65-µm CMOS technology. This provides the devices with performance and power consumption that are unmatched in the industry. The floating gate cells rely on Fowler-Nordheim tunneling to charge the gate, and have long proven their endurance and reliability. 20-year data retention is provided over operating conditions when devices are programmed on approved programmers.

The substrate of these devices is grounded, providing for a more efficient circuit. In addition, this provides substrate clamp diodes at all inputs, making them more immune to noisy input signals. All of the MACH 3 and MACH 4 devices have pull-up resistors on all inputs and I/O pins. While it is good design practice to tie unused pins high, the pull-up resistors allow unused pins to float safely.

FINAL

COM'L: -15/20

MACH355-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **144 Pins in PQFP**
- **JTAG, 5-V, in-circuit programmable**
- **IEEE 1149.1 JTAG testing capability**
- **96 Macrocells**
- **15 ns t_{PD}**
- **47.6 MHz f_{CNT}**
- **102 Inputs with pull-up resistors**
- **96 Outputs**
- **96 Flip-flops**
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- **6 "PAL33V16" blocks**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**

GENERAL DESCRIPTION

The MACH355 is a member of AMD's high-performance EE CMOS MACH 3 family. This device has approximately nine times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH355 consists of six PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH355 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH355 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

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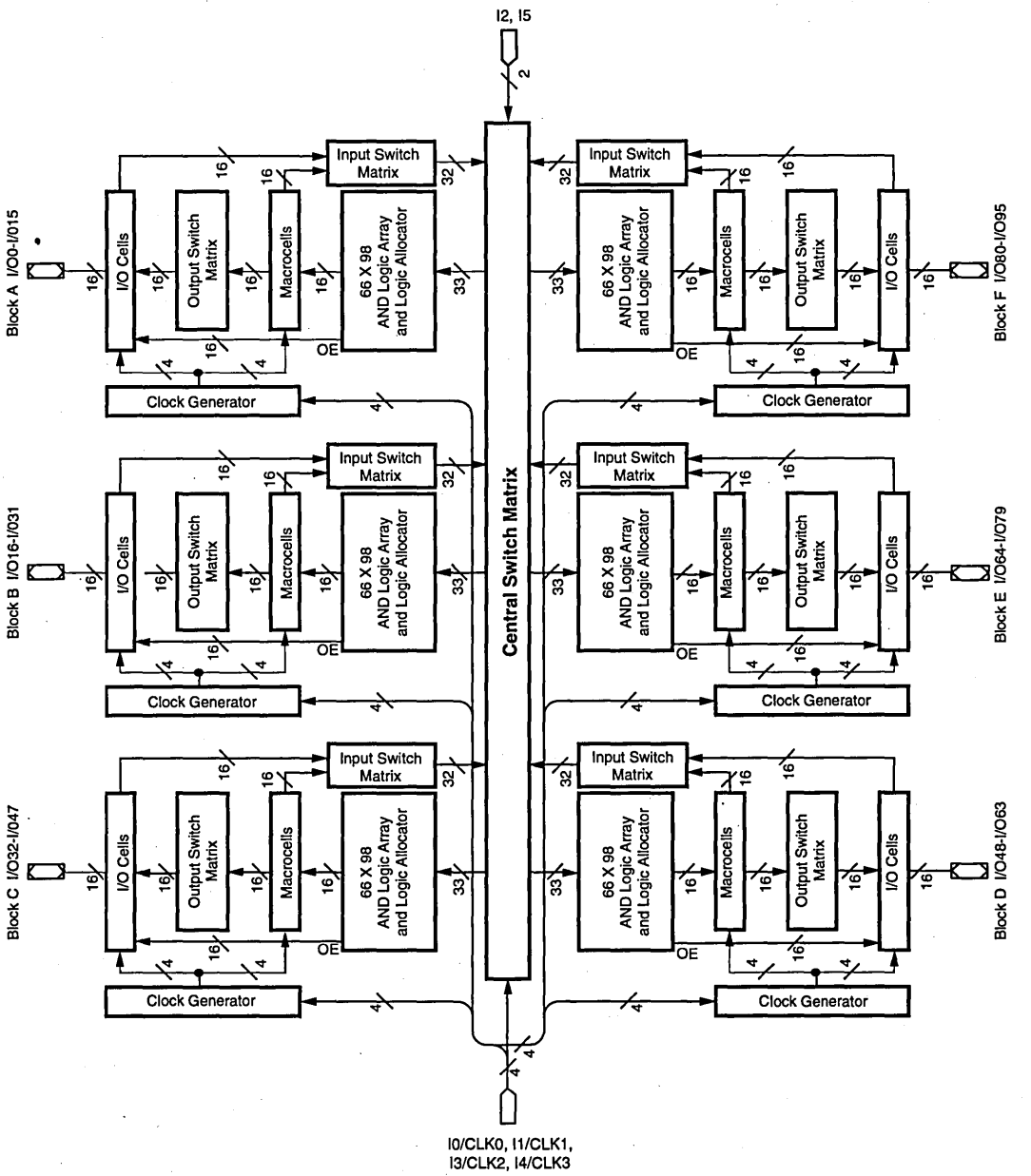
Issue Date: May 1995

BLOCK DIAGRAM

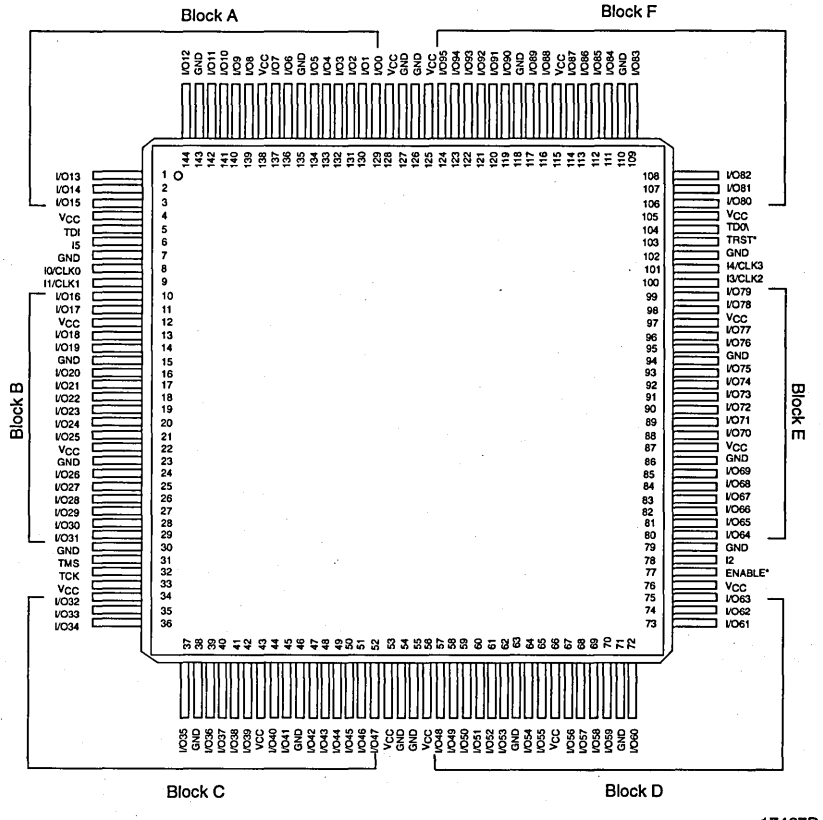


17467D-1

CONNECTION DIAGRAM

Top View

PQFP



17467D-2

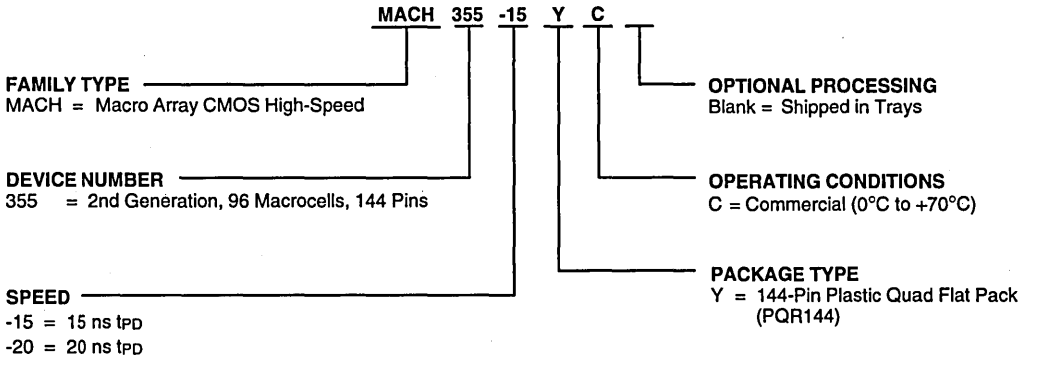
PIN DESIGNATIONS

CLK/I	=	Clock or Input
GND	=	Ground
I	=	Input
I/O	=	Input/Output
V_{CC}	=	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH355-15	YC
MACH355-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH355 consists of six PAL blocks connected by a central switch matrix. There are 96 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH355 (Figure 1) contains a clock generator, a 98-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 16 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent "PAL33V16".

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product term are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

The Central Switch Matrix and Input Switch Matrix

The MACH355 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals and 16 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

The Product-Term Array

The MACH355 product-term array consists of 80 product terms for logic use, 16 product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the MACH355 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms in synchronous mode, or 18 product terms in asynchronous mode. When product terms are routed away from a macrocell, it is possible to redirect all 5 product terms away, which precludes the use of the macrocell for logic generation. It is possible to route only 4 product terms; or it is possible to route only 4 product terms away, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. Emulating all flip-flop types with a D-type flip-flop is also made possible. Register type emulation is automatically handled by the design software.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

Each MACH355 PAL block has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 2. Please refer to Figure 1 for macrocell and I/O pin numbers.

Table 2. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0, M1 M2, M3 M4, M5 M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9 M10, M11 M12, M13 M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M1, M2, M3, M4, M5, M6, M7, M0
I/O2	M2, M3, M4, M5, M6, M7, M0, M1
I/O3	M3, M4, M5, M6, M7, M0, M1, M2
I/O4	M4, M5, M6, M7 M0, M1, M2, M3
I/O5	M5, M6, M7, M0, M1, M2, M3, M4
I/O6	M6, M7, M0, M1, M2, M3, M4, M5
I/O7	M7, M0, M1, M2, M3, M4, M5, M6
I/O8	M8, M9, M10, M11, M12, M13, M14, M15
I/O9	M9, M10, M11, M12, M13, M14, M15, M8
I/O10	M10, M11, M12, M13, M14, M15, M8, M9
I/O11	M11, M12, M13, M14, M15, M8, M9, M10
I/O12	M12, M13, M14, M15, M8, M9, M10, M11
I/O13	M13, M14, M15, M8, M9, M10, M11, M12
I/O14	M14, M15, M8, M9, M10, M11, M12, M13
I/O15	M15, M8, M9, M10, M11, M12, M13, M14

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the MACH355 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The direct I/O signal is available to the input switch matrix, and can be used if desired.

JTAG Testing

JTAG is the commonly used acronym for the IEEE Standard 1149.1–1990. The JTAG standard defines input and output pins, logic control functions, and instructions. AMD has incorporated this standard into the MACH355 device.

The JTAG standard was developed as a means of providing both board-level and device-level testing. Details on this feature can be found in the application note titled, *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices,* at the end of this Data Book.

Five-Volt Programming

Another benefit of the JTAG circuitry is the ability to use the JTAG port for five-volt programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate Plastic Quad Flat Pack, or PQFP, leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially which is ideal for on-board programming since it only requires the use of the Test Access Port. There is an optional ENABLE* pin which can be used to inhibit programming for additional security. These devices can be programmed in any JTAG chain.

Details on this feature can also be found in the *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* application note, at the end of this Data Book.

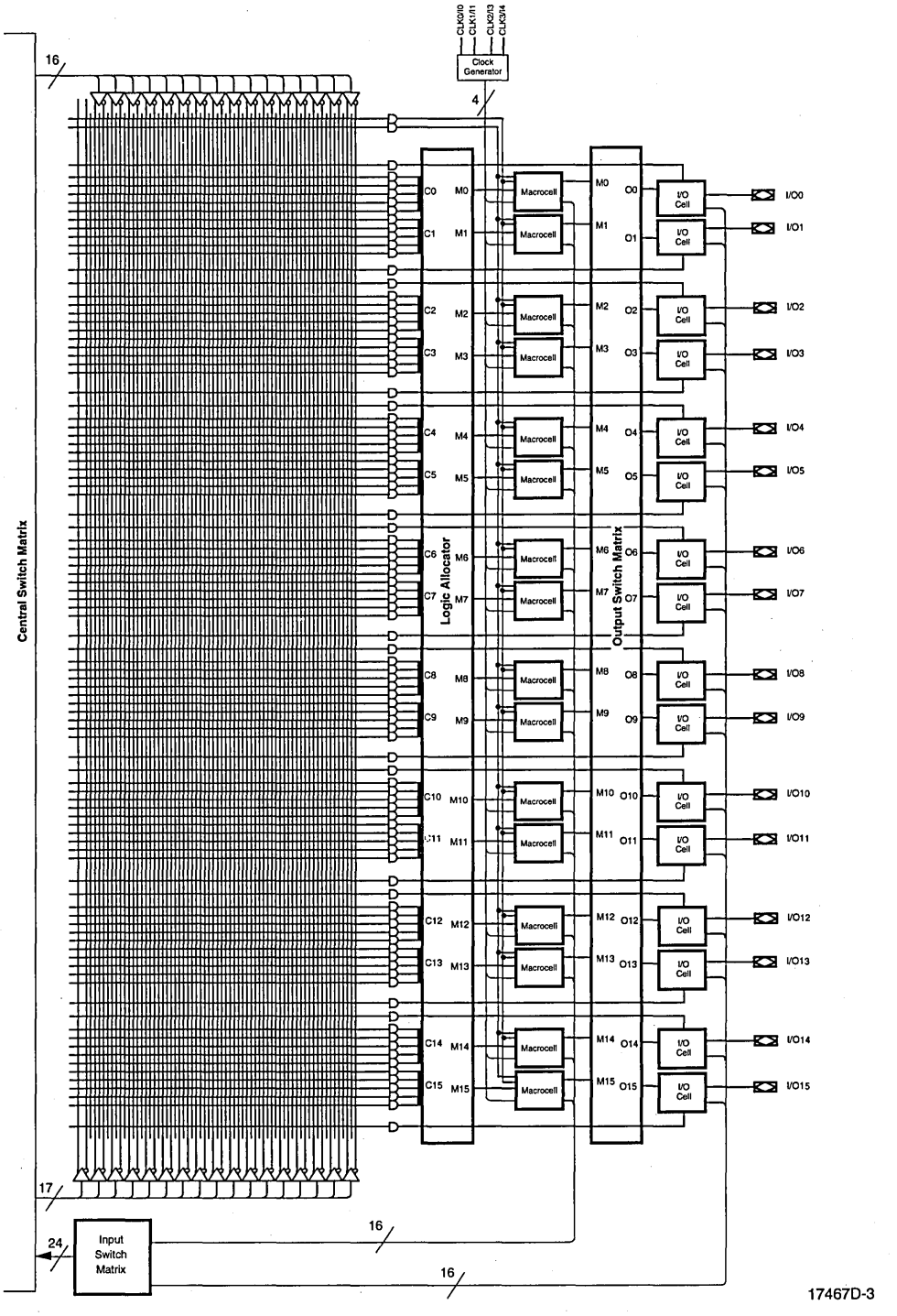


Figure 1. MACH355 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		225		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	8		10		ns
				T-type	9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				8		10		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	9		12		ns
t_{WHA}				HIGH	9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	38.5		31.2		MHz
				T-type	37		30.3		MHz
		Internal Feedback (f_{CNTA})		D-type	47.6		37		MHz
				T-type	45.4		35.7		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	10		13		ns
				T-type	11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		ns
t_{COS}	Global Clock to Output (Note 2)				2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		8		ns
t_{WHS}				HIGH	6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback (Note 4)	$1/(t_{WLS} + t_{WHS})$		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				8		10		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		ns
t_{GOS}	Gate to Output (Note 2)					11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		8		ns
t_{PDL}	Input, I/O or Feedback to Output through Transparent Output Latch					17		22	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

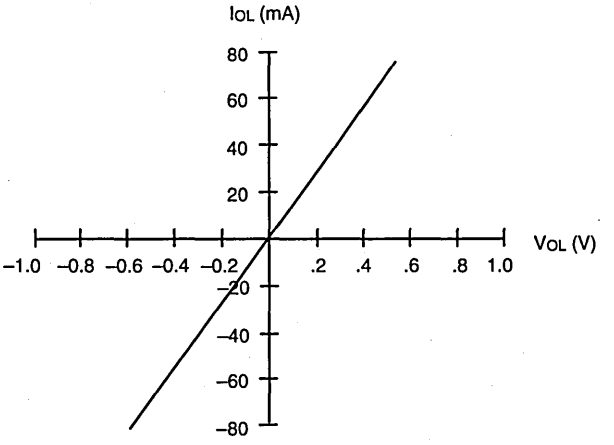
Parameter Symbol	Parameter Description	-15		-20		Unit
		Min	Max	Min	Max	
t_{AR}	Asynchronous Reset to Registered or Latched Output		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)	15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)	15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)	15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)	15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)	2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)	2	15	2	20	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

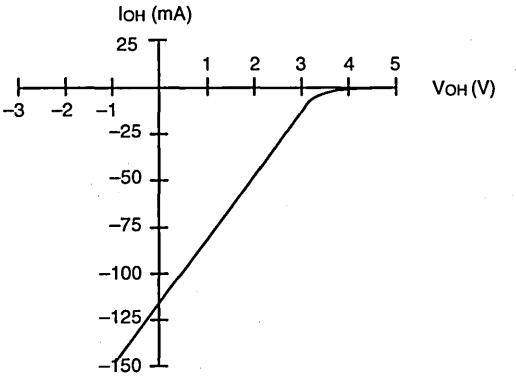
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



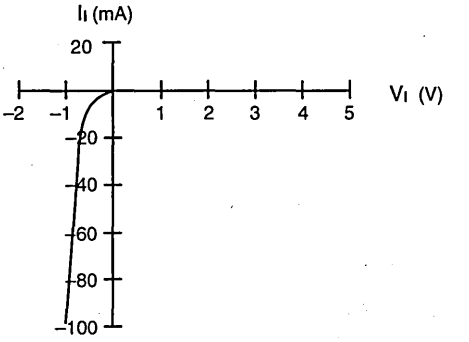
17467D-4

Output, LOW



17467D-5

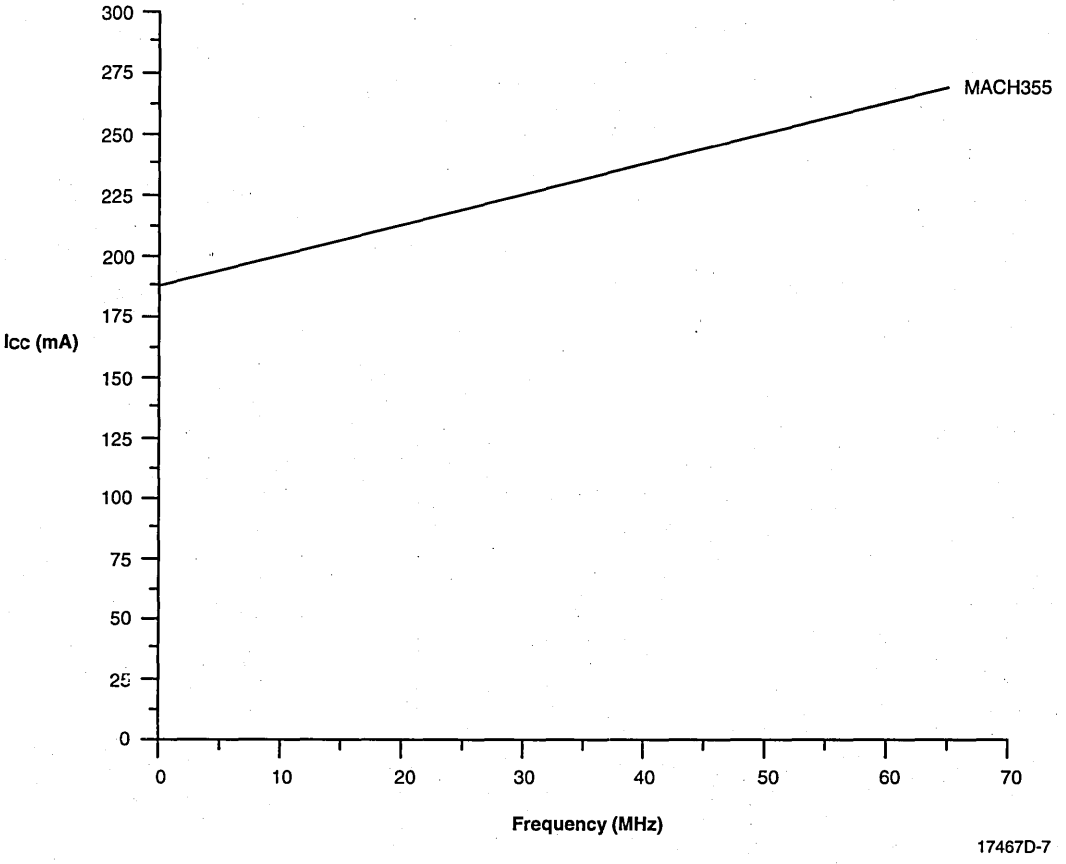
Output, HIGH



17467D-6

Input

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PQFP	Unit
θ_{jc}	Thermal impedance, junction to case		7	°C/W
θ_{ja}	Thermal impedance, junction to ambient		25	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	21	°C/W
		400 lfpm air	18	°C/W
		600 lfpm air	16	°C/W
		800 lfpm air	15	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

MACH435-12/15/20, Q-20/25

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **84 Pins in PLCC**
- **128 Macrocells**
- **12 ns t_{PD}**
- **83.3 MHz f_{CNT}**
- **70 Inputs with pull-up resistors**
- **64 Outputs**
- **192 Flip-flops**
  - 128 Macrocell flip-flops
  - 64 Input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - Four global clock pins with selectable edges
  - Asynchronous mode available for each macrocell
- **8 "PAL33V16" blocks**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**
- **Pin compatible with MACH130, MACH131, MACH230, and MACH231**

GENERAL DESCRIPTION

The MACH435 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH435 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

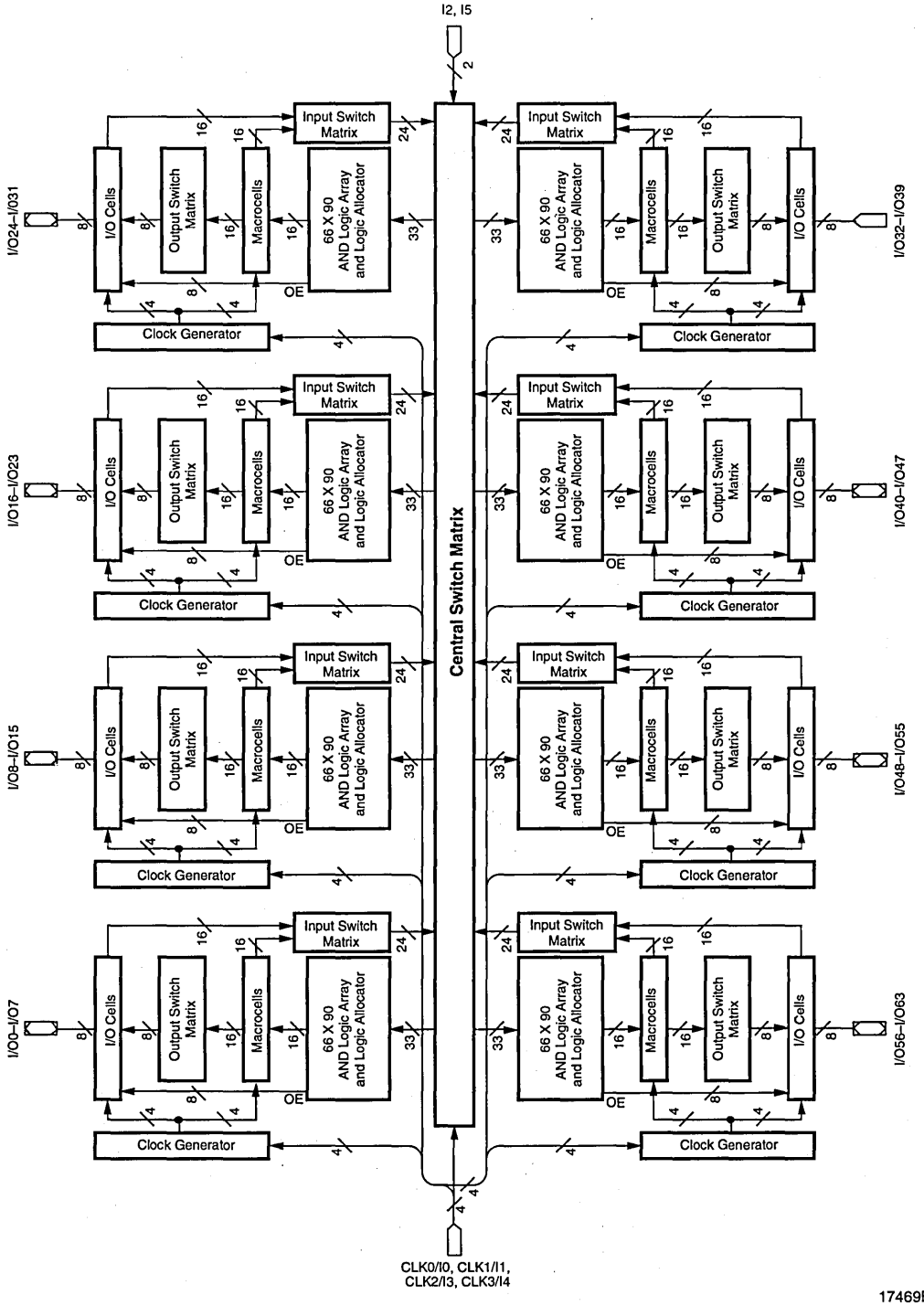
The MACH435 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH435 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

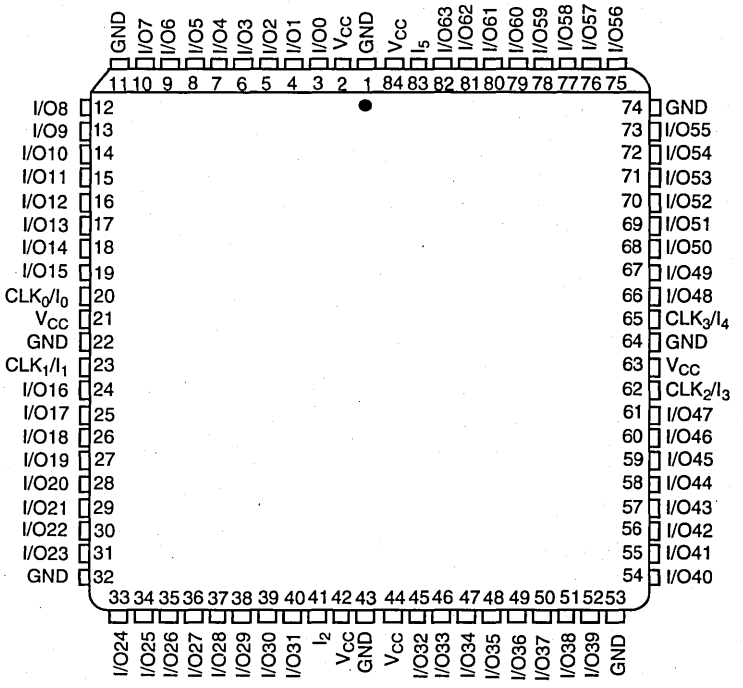
BLOCK DIAGRAM



17469E-1

CONNECTION DIAGRAM
Top View

PLCC



17469E-2

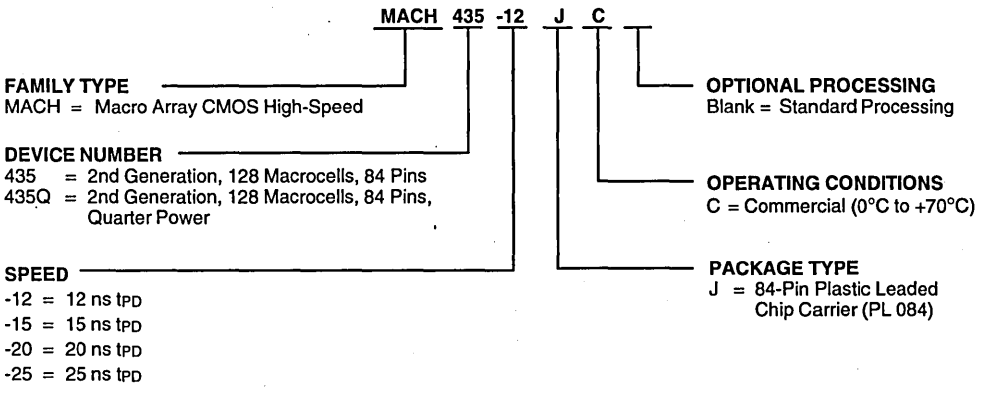
Note:
Pin-compatible with MACH130, MACH131, MACH230, and MACH231

PIN DESIGNATIONS

CLK/I	=	Clock or Input
GND	=	Ground
I	=	Input
I/O	=	Input/Output
V_{CC}	=	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH435-12	JC
MACH435-15	
MACH435-20	
MACH435Q-20	
MACH435Q-25	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH435 consists of eight PAL blocks connected by a central switch matrix. There are 64 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH435 (Figure 1) contains a clock generator, a 90-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 8 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent "PAL33V16" with 8 to 16 buried macrocells.

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product term are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

The Central Switch Matrix and Input Switch Matrix

The MACH435 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals, 8 registered input signals, and 8 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

The Product-Term Array

The MACH435 product-term array consists of 80 product terms for logic use, eight product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the MACH435 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms if in synchronous mode, or 18 product terms if in asynchronous mode. When product terms are routed away from a macrocell, it is possible to route all 5 product terms away, which precludes the use of the macrocell for logic generation; or it is possible to route only 4 product terms away, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. It also makes in possible to emulate all flip-flop types with a D-type flip-flop. Register type emulation is automatically handled by the design software.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

The MACH435 has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 2. Please refer to Figure 1 for macrocell and I/O pin numbers.

Table 2. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0, M1	I/O5, I/O6, I/O7, I/O0
M2, M3	I/O6, I/O7, I/O0, I/O1
M4, M5	I/O7, I/O0, I/O1, I/O2
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M10, M11, M12, M13, M14, M15, M0, M1
I/O6	M12, M13, M14, M15, M0, M1, M2, M3
I/O7	M14, M15, M0, M1, M2, M3, M4, M5

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the MACH435 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The input flip-flop can be configured as a register or latch. Both the direct I/O signal and the registered/latched signal are available to the input switch matrix, and can be used simultaneously if desired.

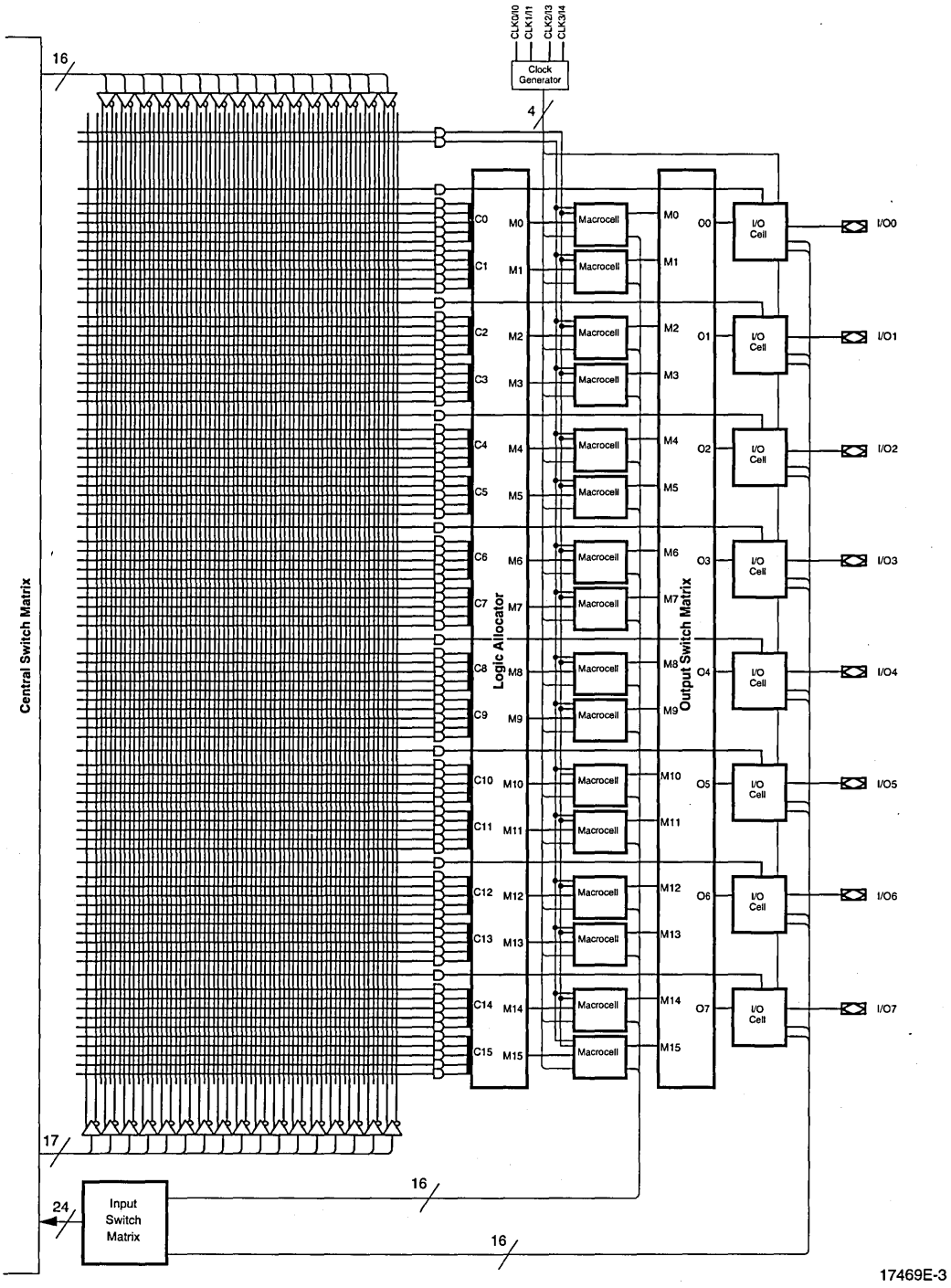


Figure 1. MACH435 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C
Ambient Temperature
with Power Applied ..... –55°C to +125°C
Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V
DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V
DC Output or
I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V
Static Discharge Voltage ..... 2001 V
Latchup Current
(T_A = 0°C to +70°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air ..... 0°C to +70°C
Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		255		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description			-12 Min	-12 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output			3	12	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock		D-type	5		ns
			T-type	6		ns
t_{HA}	Register Data Hold Time Using Product Term Clock			5		ns
t_{COA}	Product Term Clock to Output			4	14	ns
t_{WLA}	Product Term, Clock Width		LOW	8		ns
t_{WHA}			HIGH	8		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	D-type	52.6		MHz
			T-type	50		MHz
		Internal Feedback (f_{CNTA})	D-type	58.8		MHz
			T-type	55.6		MHz
		No Feedback (Note 3)		62.5		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock		D-type	7		ns
			T-type	8		ns
t_{HS}	Register Data Hold Time Using Global Clock			0		ns
t_{COS}	Global Clock to Output			2	8	ns
t_{WLS}	Global Clock Width		LOW	6		ns
t_{WHS}			HIGH	6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	D-type	66.7		MHz
			T-type	62.5		MHz
		Internal Feedback (f_{CNTA})	D-type	83.3		MHz
			T-type	76.9		MHz
		No Feedback (Note 3)		83.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			5		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock			5		ns
t_{GOA}	Product Term Gate to Output				16	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			6		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate			8		ns
t_{HLS}	Latch Data Hold Time Using Global Gate			0		ns
t_{GOS}	Gate to Output				10	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			6		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				14	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			3		ns
t_{ICO}	Input Register Clock to Combinatorial Output				18	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-12 Min	-12 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	9		ns
		T-type	10		ns
t_{WICL}	Input Register Clock Width	LOW	6		ns
t_{WICH}		HIGH	6		ns
f_{MAXIR}	Maximum Input Register Frequency		83.3		MHz
t_{SIL}	Input Latch Setup Time		2		ns
t_{HIL}	Input Latch Hold Time		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			16	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			18	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		4		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		9		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		ns
t_{WIGL}	Input Latch Gate Width LOW		6		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			16	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			16	ns
t_{ARW}	Asynchronous Reset Width (Note 1)		12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			16	ns
t_{APW}	Asynchronous Preset Width (Note 1)		12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)		8		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	12	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	12	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		255		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL Block and capable of being loaded, enabled, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	8		10		ns
				T-type	9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				8		10		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	9		12		ns
t_{WHA}				HIGH	9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	38.5		31.2		MHz
				T-type	37		30.3		MHz
		Internal Feedback (f_{CNTA})		D-type	47.6		37		MHz
				T-type	45.4		35.7		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	10		13		ns
				T-type	11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		ns
t_{COS}	Global Clock to Output (Note 2)				2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		8		ns
t_{WHS}				HIGH	6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback (Note 4)	$1/(t_{WLS} + t_{WHS})$		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				8		10		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		ns
t_{GOS}	Gate to Output (Note 2)					11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				4		5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					20		25	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-15		-20		Unit
			Min	Max	Min	Max	
t_{ICS}	Input Register Clock to Output Register Setup	D-type	15		20		ns
		T-type	16		21		ns
t_{WICL}	Input Register Clock Width	LOW	6		8		ns
t_{WICH}		HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time		2		2		ns
t_{HIL}	Input Latch Hold Time		4		5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			22		27	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		10		12		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		14		19		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		12		16		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		21		ns
t_{WIGL}	Input Latch Gate Width LOW		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	15	2	20	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature
with Power Applied ..... −55°C to +125°C
Supply Voltage with
Respect to Ground ..... −0.5 V to +7.0 V
DC Input Voltage ..... −0.5 V to V_{CC} +0.5 V
DC Output or
I/O Pin Voltage ..... −0.5 V to V_{CC} +0.5 V
Static Discharge Voltage ..... 2001 V
Latchup Current
(T_A = 0°C to +70°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air ..... 0°C to +70°C
Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	−30		−160	mA
I_{CC}	Supply Current (Typical)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		115		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description			-20		Unit
				Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output			3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock		D-type	10		ns
			T-type	11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock			16		ns
t_{COA}	Product Term Clock to Output			5	22	ns
t_{WLA}	Product Term, Clock Width		LOW	12		ns
t_{WHA}			HIGH	12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	D-type	33.3		MHz
			T-type	37.2		MHz
		Internal Feedback (f_{CNTA})	D-type	35.7		MHz
			T-type	34.5		MHz
		No Feedback (Note 3)		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock		D-type	13		ns
			T-type	14		ns
t_{HS}	Register Data Hold Time Using Global Clock			0		ns
t_{COS}	Global Clock to Output			2	12	ns
t_{WLS}	Global Clock Width		LOW	8		ns
t_{WHS}			HIGH	8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	D-type	40.0		MHz
			T-type	38.5		MHz
		Internal Feedback (f_{CNTA})	D-type	47.6		MHz
			T-type	43.5		MHz
		No Feedback (Note 3)		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			8		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock			8		ns
t_{GOA}	Product Term Gate to Output				22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate			13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate			0		ns
t_{GOS}	Gate to Output				12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				22	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			4		ns
t_{ICO}	Input Register Clock to Combinatorial Output				22	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-20 Min	-20 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	15		ns
		T-type	17		ns
t_{WICL}	Input Register Clock Width	LOW	8		ns
t_{WICH}		HIGH	8		ns
f_{MAXIR}	Maximum Input Register Frequency		62.5		MHz
t_{SIL}	Input Latch Setup Time		2		ns
t_{HIL}	Input Latch Hold Time		2.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			24	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		12		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		10		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		15		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		15		ns
t_{WIGL}	Input Latch Gate Width LOW or HIGH		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			25	ns
t_{APW}	Asynchronous Preset Width (Note 1)		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	20	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f=25 MHz, T_A = 25°C, (Note 5)		115		mA

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL Block and capable of being loaded, erased, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of the this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-25 Min	-25 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	25	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	18		ns
				T-type	19		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				18		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	28	ns
t_{WLA}	Product Term, Clock Width			LOW	19		ns
t_{WHA}				HIGH	19		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	21.7		MHz
				T-type	21.3		MHz
		Internal Feedback (f_{CNTA})		D-type	24.4		MHz
				T-type	23.8		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		26.3		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	20		ns
				T-type	21		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		ns
t_{COS}	Global Clock to Output (Note 2)				2	12	ns
t_{WLS}	Global Clock Width			LOW	8		ns
t_{WHS}				HIGH	8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	31.3		MHz
				T-type	30.3		MHz
		Internal Feedback (f_{CNTS})		D-type	37		MHz
				T-type	35.7		MHz
		No Feedback (Note 4)	$1/(t_{SS} + t_{HS})$		50		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				18		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				18		ns
t_{GOA}	Product Term Gate to Output (Note 2)					29	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				19		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				20		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		ns
t_{GOS}	Gate to Output (Note 2)					21	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					27	ns
t_{SIR}	Input Register Setup Time				5		ns
t_{HIR}	Input Register Hold Time				5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					30	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

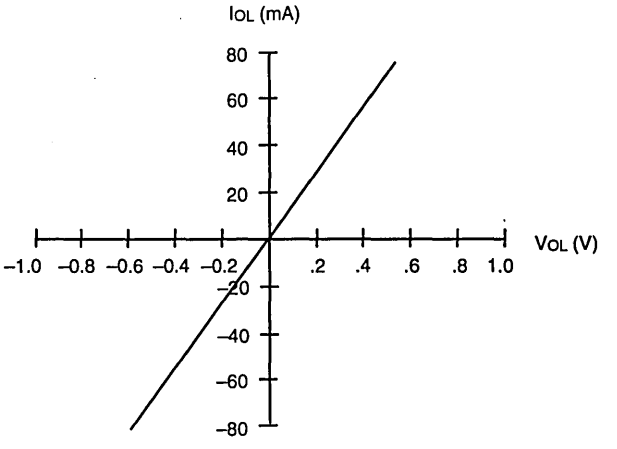
Parameter Symbol	Parameter Description		-25 Min	-25 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	25		ns
		T-type	26		ns
t_{WICL}	Input Register Clock Width	LOW	8		ns
t_{WICH}		HIGH	8		ns
f_{MAXIR}	Maximum Input Register Frequency $1/(t_{WICL} + t_{WICH})$		62.5		MHz
t_{SIL}	Input Latch Setup Time		5		ns
t_{HIL}	Input Latch Hold Time		5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			32	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		20		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		24		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		22		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		26		ns
t_{WIGL}	Input Latch Gate Width LOW or HIGH		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			29	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			30	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		25		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		25		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			30	ns
t_{APW}	Asynchronous Preset Width (Note 3)		25		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		25		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	25	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	25	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

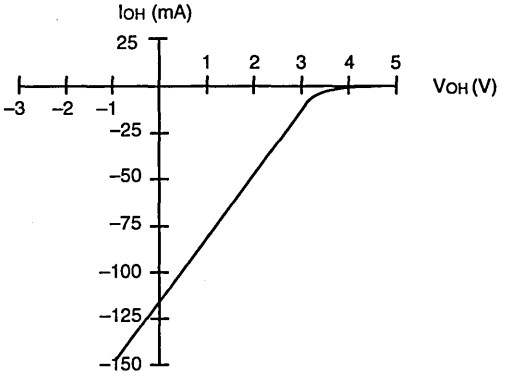
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



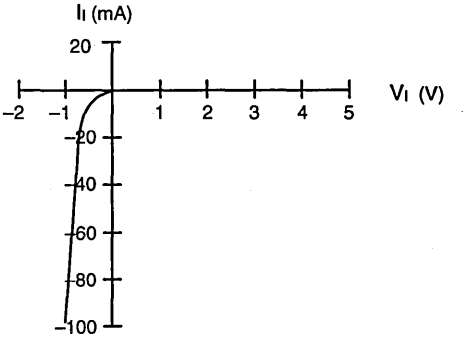
17469E-4

Output, LOW



17469E-5

Output, HIGH

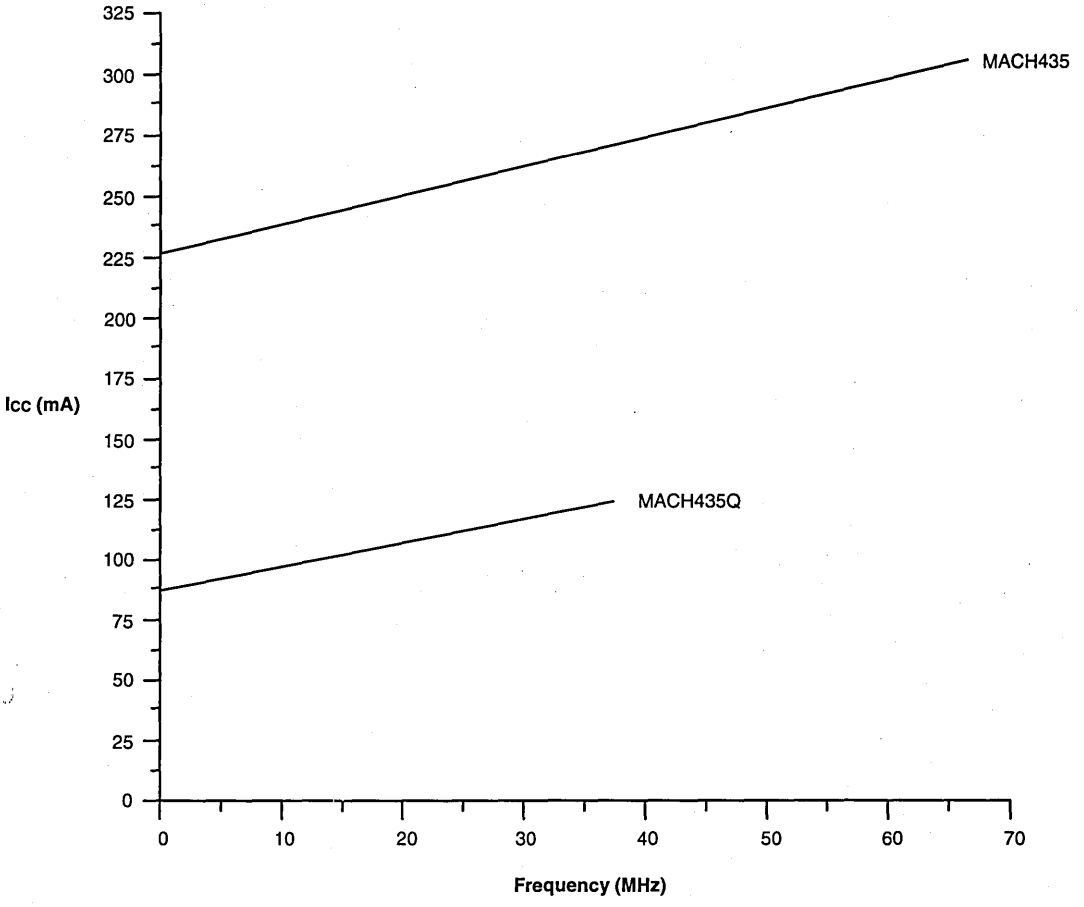


17469E-6

Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		5	°C/W
θ_{ja}	Thermal impedance, junction to ambient		20	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	17	°C/W
		400 lfpm air	14	°C/W
		600 lfpm air	12	°C/W
		800 lfpm air	10	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

MACH445-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 100-pin version of the MACH435 in PQFP
- 5 V, in-circuit programmable
- JTAG, IEEE 1149.1 JTAG testing capability
- 128 macrocells
- 12 ns t_{PD}
- 83 MHz f_{CNT}
- 70 inputs with pull-up resistors
- 64 outputs
- 192 flip-flops
  - — 128 macrocell flip-flops
  - — 64 input flip-flops
- Up to 20 product terms per function, with XOR
- Flexible clocking
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- 8 "PAL33V16" blocks
- Input and output switch matrices for high routability
- Fixed, predictable, deterministic delays
- JEDEC-file compatible with MACH435
- Zero-hold-time input register option

GENERAL DESCRIPTION

The MACH445 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide. It is architecturally identical to the MACH435, with the addition of JTAG and 5-V programming features.

The MACH445 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH445 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH445 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

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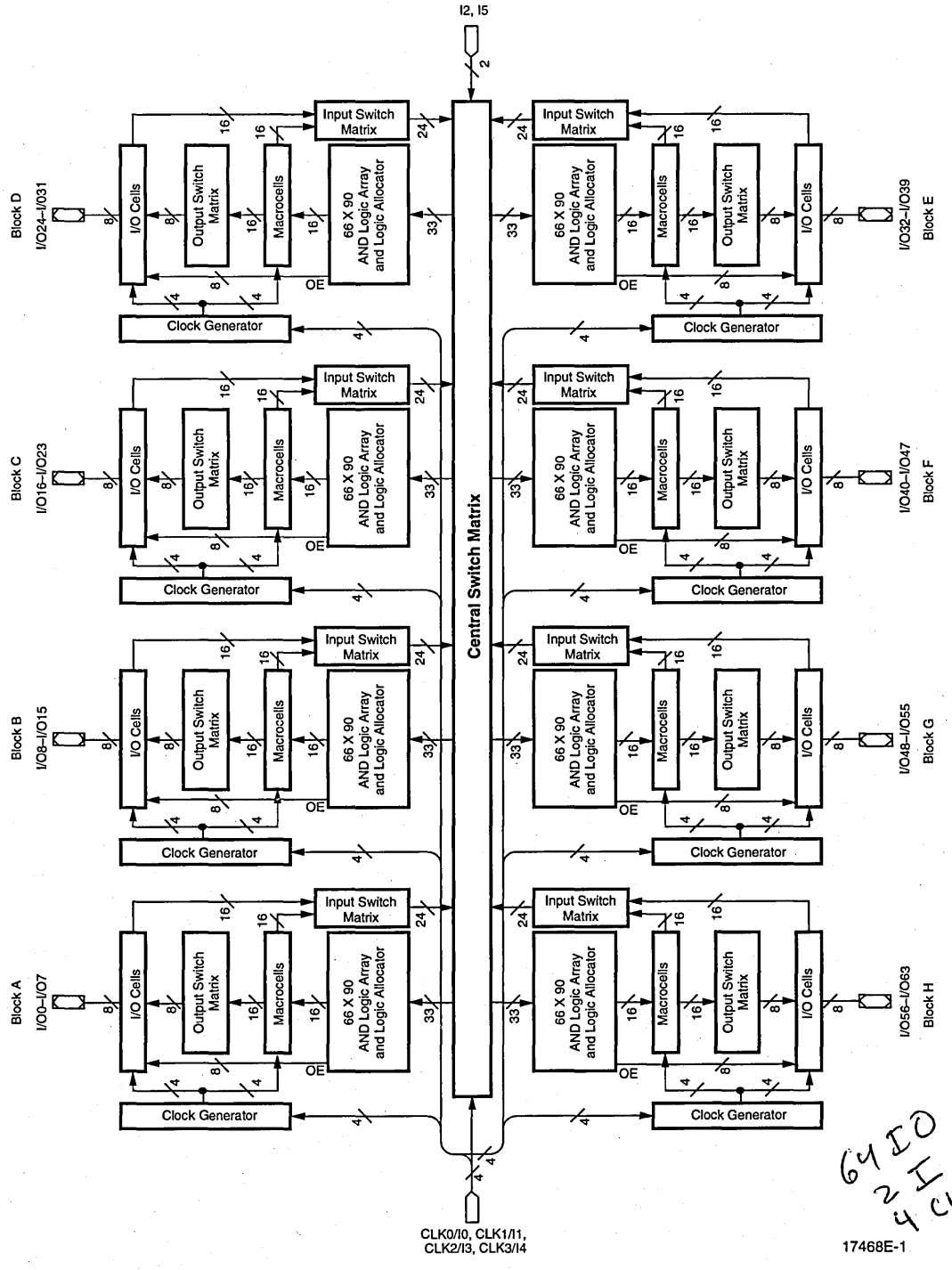
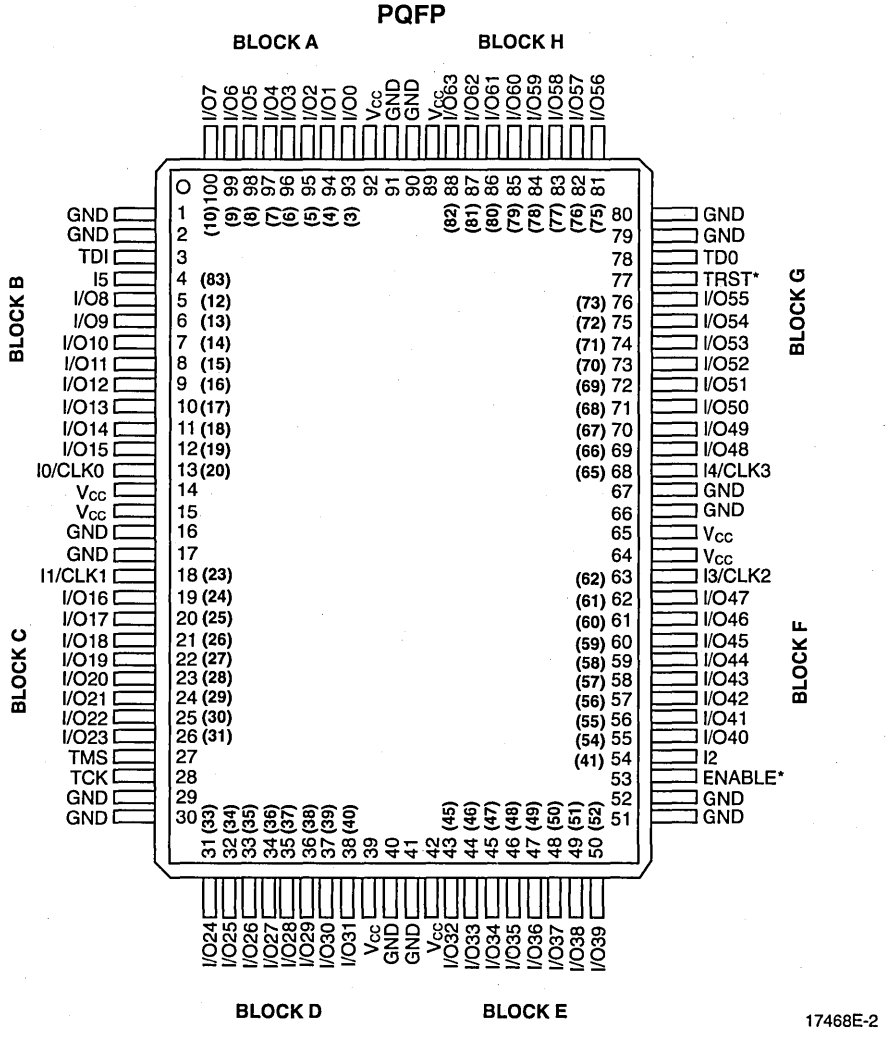
Issue Date: May 1995

BLOCK DIAGRAM



64 IO
2 I
4 clk/I

CONNECTION DIAGRAM MACH445 (MACH435)
Top View



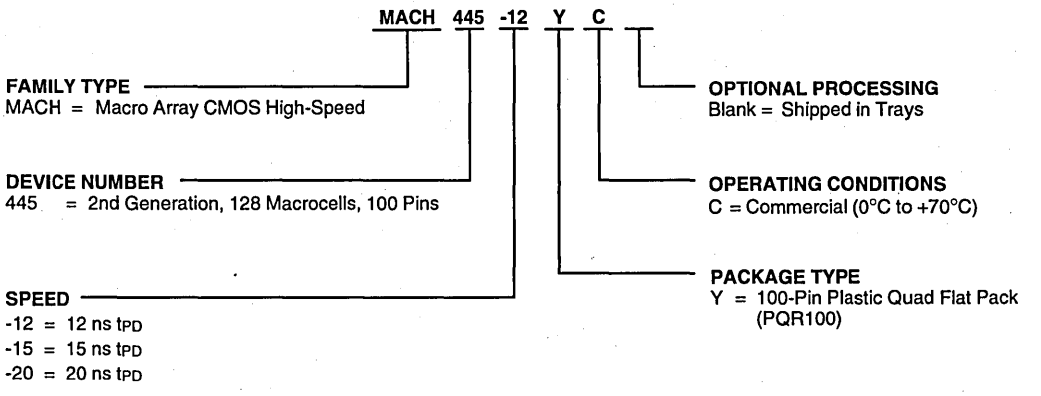
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH445-12	YC
MACH445-15	
MACH445-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH445 consists of eight PAL blocks connected by a central switch matrix. There are 64 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH445 (Figure 1) contains a clock generator, a 90-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 8 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent "PAL33V16" with 8 to 16 buried macrocells.

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product terms are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block nitialization product terms.

The Central Switch Matrix and Input Switch Matrix

The MACH445 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals, 8 registered input signals, and 8 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

The Product-Term Array

The MACH445 product-term array consists of 80 product terms for logic use, eight product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the MACH445 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms in synchronous mode, or 18 product terms in asynchronous mode. When product terms are routed away from a macrocell, all 5 product terms may be redirected, which precludes the use of the macrocell for logic generation. It is possible to redirect only 4 product terms, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. Emulating all flip-flop types with a D-type flip-flop is also made possible. Register type emulation is automatically handled by the design software.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 9. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

The MACH445 has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 2. Please refer to Figure 1 for macrocell and I/O pin numbers.

Table 2. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0, M1	I/O5, I/O6, I/O7, I/O0
M2, M3	I/O6, I/O7, I/O0, I/O1
M4, M5	I/O7, I/O0, I/O1, I/O2
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M10, M11, M12, M13, M14, M15, M0, M1
I/O6	M12, M13, M14, M15, M0, M1, M2, M3
I/O7	M14, M15, M0, M1, M2, M3, M4, M5

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the MACH445 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The input flip-flop can be configured as a register or latch. Both the direct I/O signal and the registered/latched signal are available to the input switch matrix, and can be used simultaneously if desired.

JTAG Testing

JTAG is the commonly used acronym for the IEEE Standard 1149.1–1990. The JTAG standard defines input and output pins, logic control functions, and instructions. AMD has incorporated this standard into the MACH445 device.

The JTAG standard was developed as a means of providing both board-level and device-level testing. Details on this feature can be found in the application note titled, *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* at the end of this Data Book.

Five-Volt Programming

Another benefit from the JTAG circuitry that AMD has derived is the ability to use the JTAG port for five-volt programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate Plastic Quad Flat Pack, or PQFP, leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially which is ideal for on-board programming since it only requires the use of the Test Access Port. Use of the programming Enable Pin (ENABLE*) is optional.

Details on this feature can also be found in the *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* application note at the end of this Data Book.

Zero-Hold-Time Input Register

The MACH445 device has a zero-hold time (ZHT) fuse. This fuse controls the time delay associated with loading data into all I/O cell registers and latches in the MACH445 device.

When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized and the device timing is compatible with the MACH435 device.

This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

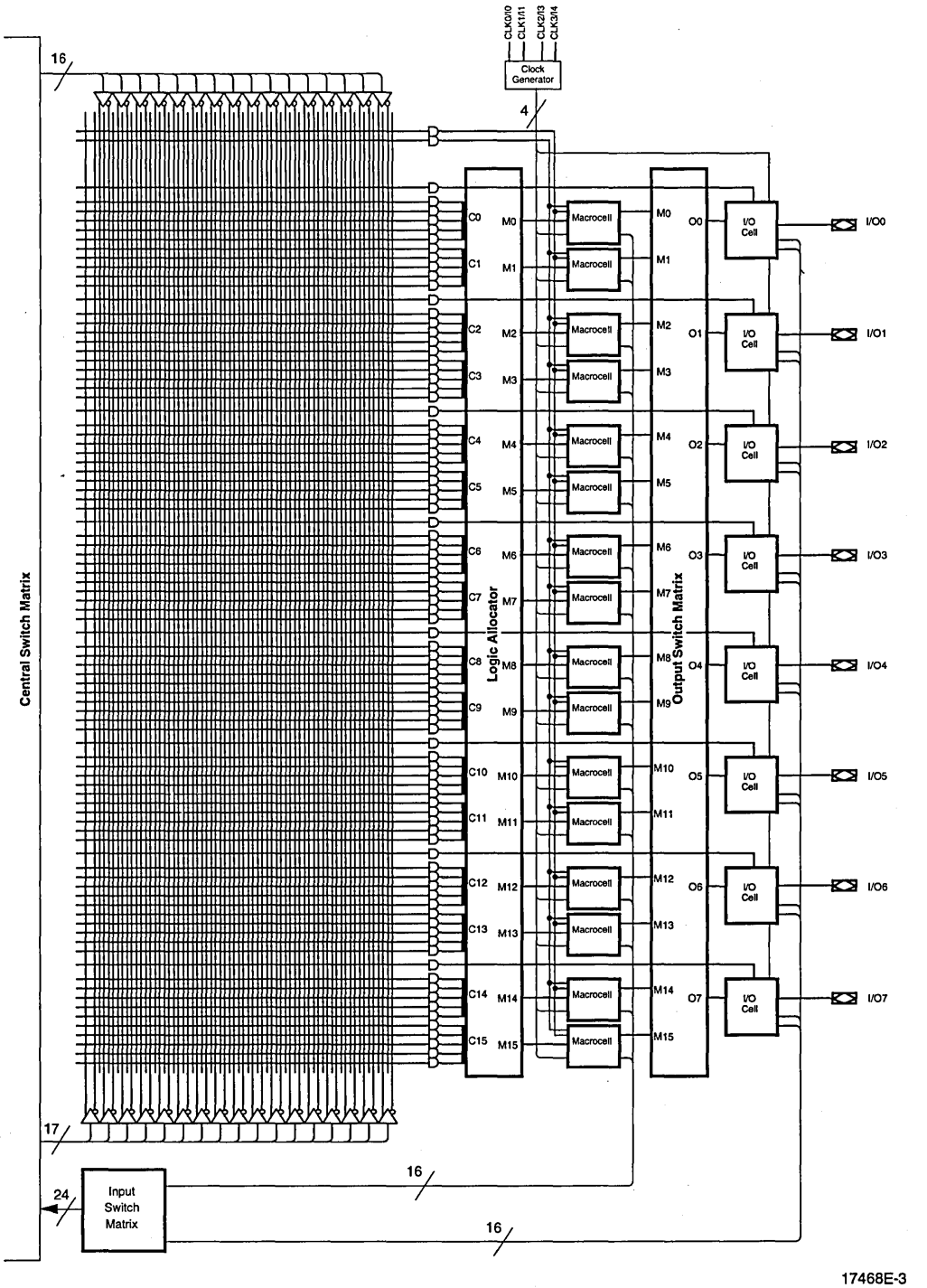


Figure 1. MACH445 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage ..... −0.5 V to V_{CC} +0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	−30		−160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5.0 V, f = 25 MHz, T_A = 25°C (Note 5)		255		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description			-12 Min	-12 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output			3	12	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock		D-type	5		ns
			T-type	6		ns
t_{HA}	Register Data Hold Time Using Product Term Clock			5		ns
t_{COA}	Product Term Clock to Output			4	14	ns
t_{WLA}	Product Term, Clock Width		LOW	8		ns
t_{WHA}			HIGH	8		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	D-type	52.6		MHz
			T-type	50.0		MHz
		Internal Feedback (f_{CNTA})	D-type	58.8		MHz
			T-type	55.6		MHz
		No Feedback (Note 3)		62.5		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock		D-type	7		ns
			T-type	8		ns
t_{HS}	Register Data Hold Time Using Global Clock			0		ns
t_{COS}	Global Clock to Output			2	8	ns
t_{WLS}	Global Clock Width		LOW	6		ns
t_{WHS}			HIGH	6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	D-type	66.7		MHz
			T-type	62.5		MHz
		Internal Feedback (f_{CNTS})	D-type	83.3		MHz
			T-type	76.9		MHz
		No Feedback (Note 3)		83.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			5		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock			5		ns
t_{GOA}	Product Term Gate to Output				16	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			6		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate			8		ns
t_{HLS}	Latch Data Hold Time Using Global Gate			0		ns
t_{GOS}	Gate to Output				10	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			6		ns
t_{ICO}	Input Register Clock to Combinatorial Output				18	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-12 Min	-12 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	9		ns
		T-type	10		ns
t_{WICL}	Input Register Clock Width	LOW	6		ns
t_{WICH}		HIGH	6		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			16	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			18	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		ns
t_{WIGL}	Input Latch Gate Width LOW		6		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			16	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			16	ns
t_{APW}	Asynchronous Preset Width (Note 2)		12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	12	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	12	ns
Input Register with Standard-Hold-Time Option					
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			14	ns
t_{SIR}	Input Register Setup Time		2		ns
t_{HIR}	Input Register Hold Time		3		ns
t_{SIL}	Input Latch Setup Time		2		ns
t_{HIL}	Input Latch Hold Time		3		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate		9		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			16	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description	-12		Unit
		Min	Max	
Input Register with Zero-Hold-Time Option				
t_{PDL}[3]	Input, I/O, or Feedback to Output Through Transparent Input Latch		20	ns
t_{SIR}[3]	Input Register Setup Time	6		ns
t_{HIR}[3]	Input Register Hold Time	0		ns
t_{SIL}[3]	Input Latch Setup Time	6		ns
t_{HIL}[3]	Input Latch Hold Time	0		ns
t_{SLLA}[3]	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	16		ns
t_{SLLS}[3]	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	18		ns
t_{PDLL}[3]	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		22	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		–30	–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz T_A = 25°C (Note 5)		255		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	8		10		ns
				T-type	9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				8		10		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	9		12		ns
t_{WHA}				HIGH	9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	38.5		31.2		MHz
				T-type	37		30.3		MHz
		Internal Feedback (f_{CNTA})		D-type	47.6		37		MHz
				T-type	45.4		35.7		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	10		13		ns
				T-type	11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		ns
t_{COS}	Global Clock to Output (Note 2)				2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		8		ns
t_{WHS}				HIGH	6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback (Note 4)	$1/(t_{WLS} + t_{WHS})$		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				8		10		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		ns
t_{GOS}	Gate to Output (Note 2)					11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		8		ns
t_{ICO}	Input Register Clock to Combinatorial Output					20		25	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	15		20		ns
		T-type	16		21		ns
t_{WICL}	Input Register Clock Width	LOW	6		8		ns
t_{WICH}		HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		62.5		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			22		27	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		14		19		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		21		ns
t_{WIGL}	Input Latch Gate Width LOW		6		8		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	15	2	20	ns
Input Register with Standard-Hold-Time Option							
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			17		22	ns
t_{SIR}	Input Register Setup Time		2		2		ns
t_{HIR}	Input Register Hold Time		4		5		ns
t_{SIL}	Input Latch Setup Time		2		2		ns
t_{HIL}	Input Latch Hold Time		4		5		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate		10		12		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate		12		16		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19		24	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

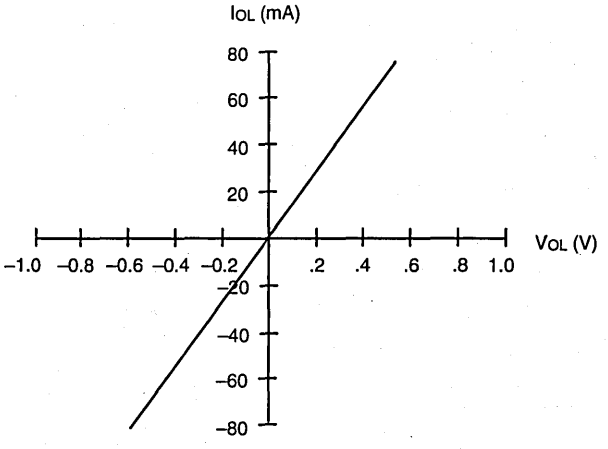
Parameter Symbol	Parameter Description	-15		-20		Unit
		Min	Max	Min	Max	
Input Register with Zero-Hold-Time Option						
t_{PDL}[4]	Input, I/O, or Feedback to Output Through Transparent Input Latch		23		30	ns
t_{SIR}[4]	Input Register Setup Time	6		8		ns
t_{HIR}[4]	Input Register Hold Time	0		0		ns
t_{SIL}[4]	Input Latch Setup Time	6		8		ns
t_{HIL}[4]	Input Latch Hold Time	0		0		ns
t_{SLLA}[4]	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	16		20		ns
t_{SLLS}[4]	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	18		24		ns
t_{PDLL}[4]	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		25		32	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

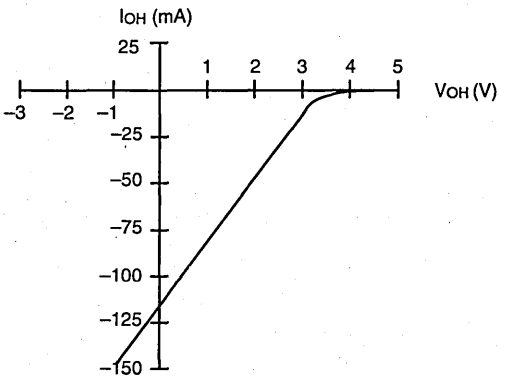
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



Output, LOW

17468E-4



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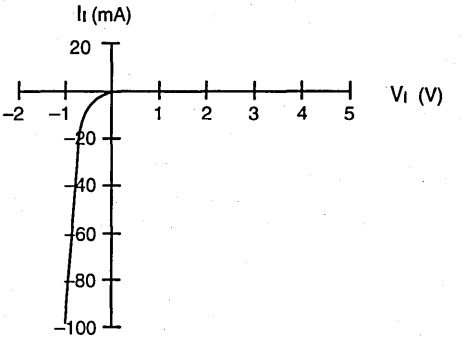
Output, HIGH



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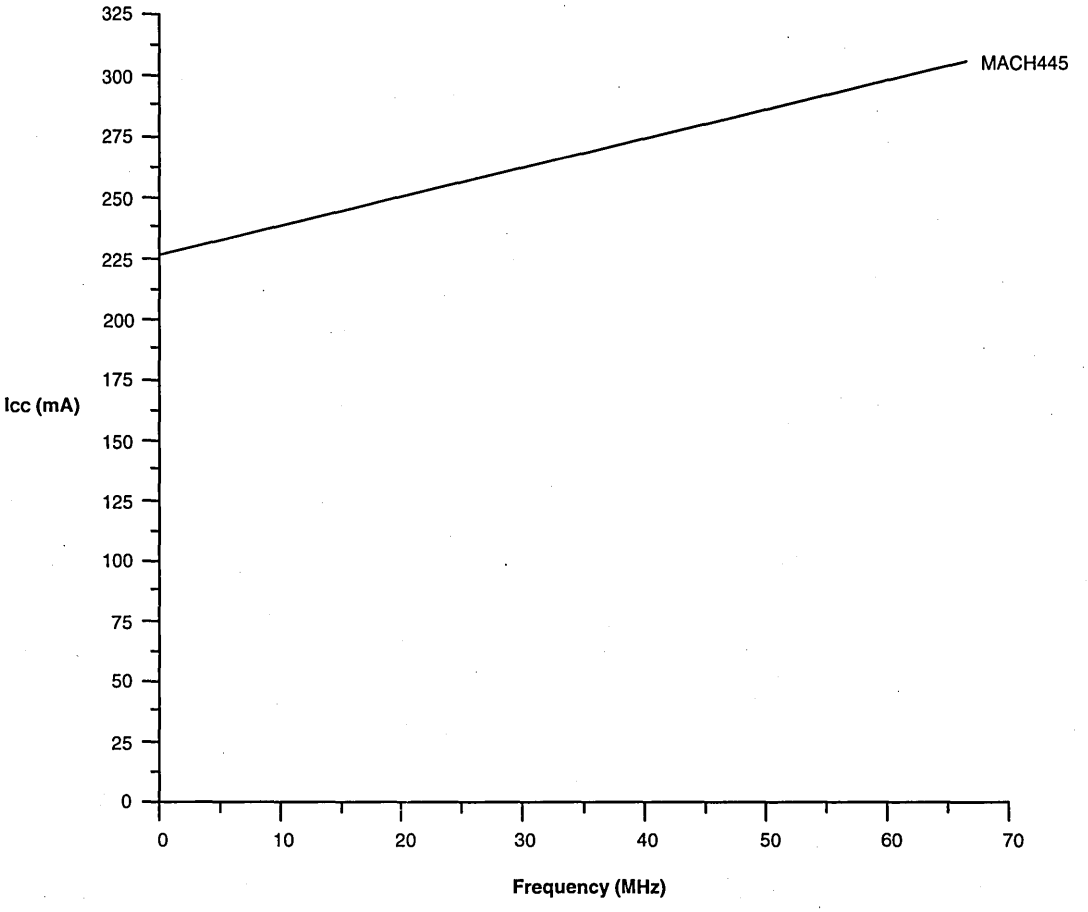
Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

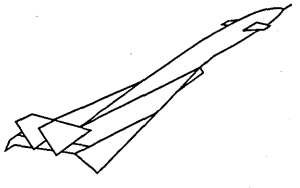
TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PQFP	Unit
θ_{jc}	Thermal impedance, junction to case		5	°C/W
θ_{ja}	Thermal impedance, junction to ambient		38	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	32	°C/W
		400 lfpm air	28	°C/W
		600 lfpm air	26	°C/W
		800 lfpm air	24	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.



FINAL

COM'L: -12/15/20

MACH465-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **208 pins in PQFP**
- **JTAG, 5-V, in-circuit programmable**
- **IEEE 1149.1 JTAG testing capability**
- **256 macrocells**
- **12 ns t_{PD}**
- **83.3 MHz f_{CNT}**
- **146 Inputs with pull-up resistors**
- **128 Outputs**
- **384 flip-flops**
  - — 256 Macrocell flip-flops
  - — 128 Input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- **16 "PAL34V16" blocks**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**
- **Zero-hold-time input register option**
- **Peripheral Component Interconnect (PCI) compliant**

GENERAL DESCRIPTION

The MACH465 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately 25 times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH465 consists of 16 PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH465 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH465 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

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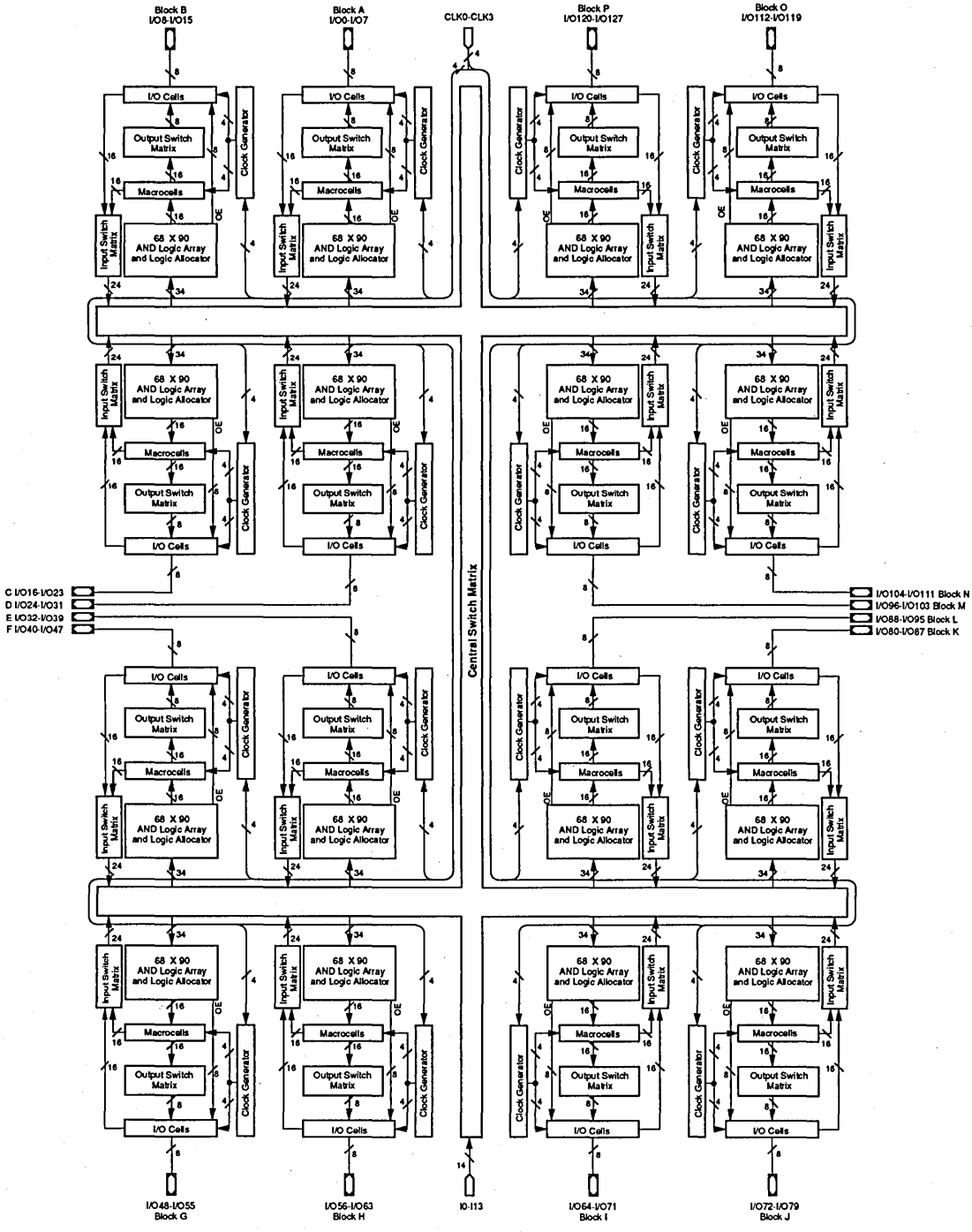
Issue Date: May 1995

BLOCK DIAGRAM

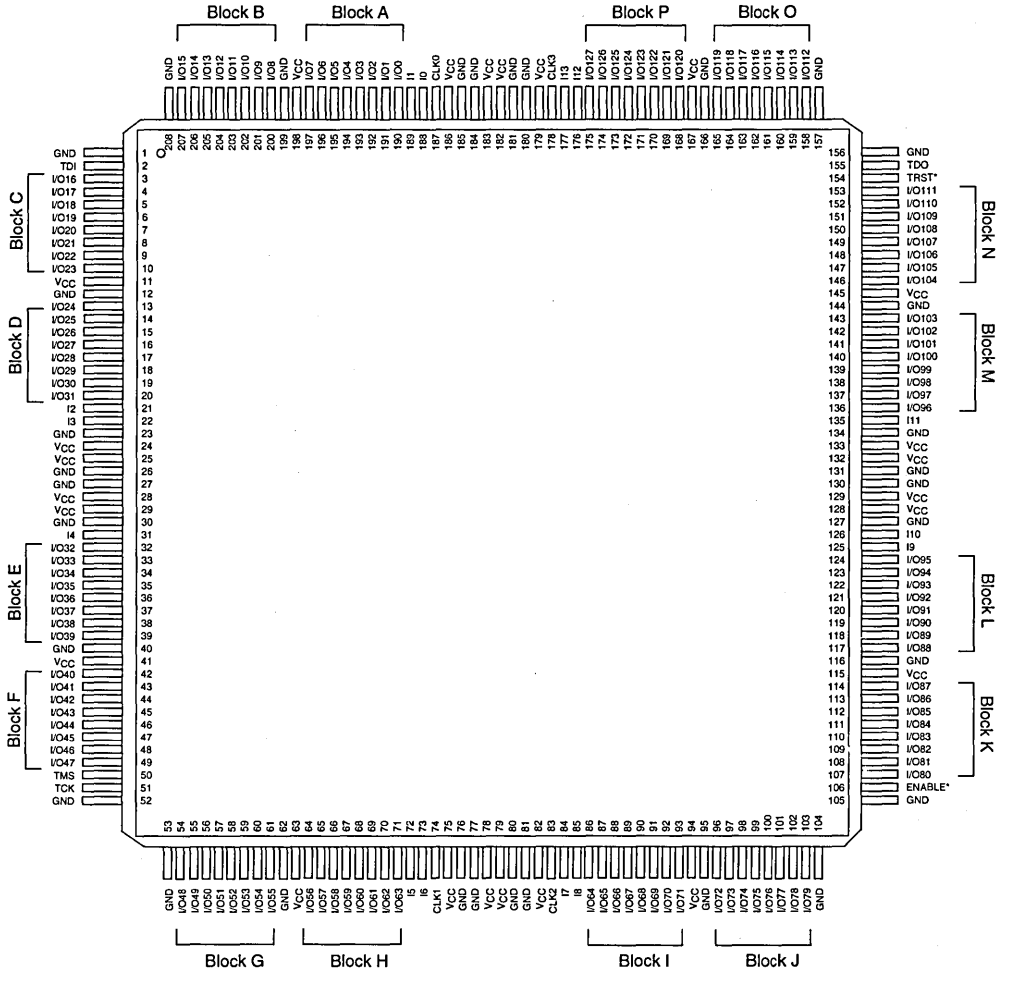


17470D-1

CONNECTION DIAGRAM

Top View

PQFP



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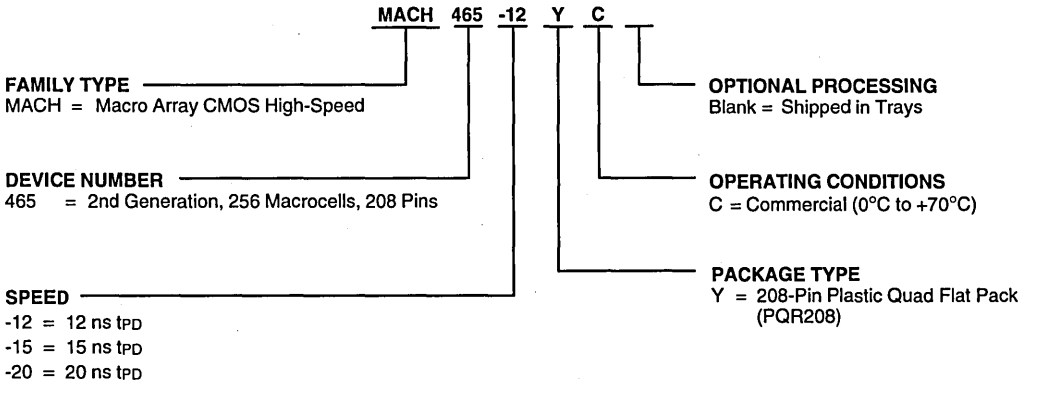
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH465-12	YC
MACH465-15	
MACH465-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH465 consists of sixteen PAL blocks connected by a central switch matrix. There are 128 I/O pins and 14 dedicated input pins feeding the central switch matrix. These signals are distributed to the sixteen PAL blocks for efficient design implementation. There are also 4 global clock pins.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH465 (Figure 1) contains a clock generator, a 90-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 8 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 34 inputs. This makes the PAL block look effectively like an independent "PAL34V16".

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product term are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

The Central Switch Matrix and Input Switch Matrix

The MACH465 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals, 8 registered input signals, and 8 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

The Product-Term Array

The MACH465 product-term array consists of 80 product terms for logic use, eight product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the MACH465 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms if in synchronous mode, or 18 product terms if in asynchronous mode. When product terms are routed away from a macrocell, it is possible to route all 5 product terms away, which precludes the use of the macrocell for logic generation; or it is possible to route only 4 product terms away, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. It also makes in possible to emulate all flip-flop types with a D-type flip-flop. Register type emulation is automatically handled by the design software.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

The MACH465 has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 2. Please refer to Figure 1 for macrocell and I/O pin numbers.

Table 2. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0, M1	I/O5, I/O6, I/O7, I/O0
M2, M3	I/O6, I/O7, I/O0, I/O1
M4, M5	I/O7, I/O0, I/O1 I/O2
M6, M7	I/O0, I/O1, I/O2 I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M10, M11, M12, M13, M14, M15, M0, M1
I/O6	M12, M13, M14, M15, M0, M1, M2, M3
I/O7	M14, M15, M0, M1, M2, M3, M4, M5

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the MACH465 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The direct I/O signal is available to the input switch matrix, and can be used if desired.

JTAG Testing

JTAG is the commonly used acronym for the IEEE Standard 1149.1–1990. The JTAG standard defines and output pins, logic control functions, and instructions. AMD has incorporated this standard into the MACH465 device.

The JTAG standard was developed as a means of providing both board-level and device-level testing. Details on this feature can be found in the application note titled, *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices*, at the end of this data book.

Five-Volt Programming

Another benefit from the JTAG circuitry that AMD has derived is the ability to use the JTAG port for five-volt programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate Plastic Quad Flat Pack, or PQFP, leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially which is ideal for on-board programming since it only requires the use of the Test Access Port, along with the additional ENABLE* pin. Programming can also be done in any JTAG chain.

Details on this feature can also be found in the *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* application note, at the end of this data book.

Zero-Hold-Time Input Register

The MACH465 device has a zero-hold time (ZHT) fuse. This fuse controls the time delay associated with loading data into all I/O cell registers and latches in the MACH465 device.

When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized.

This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

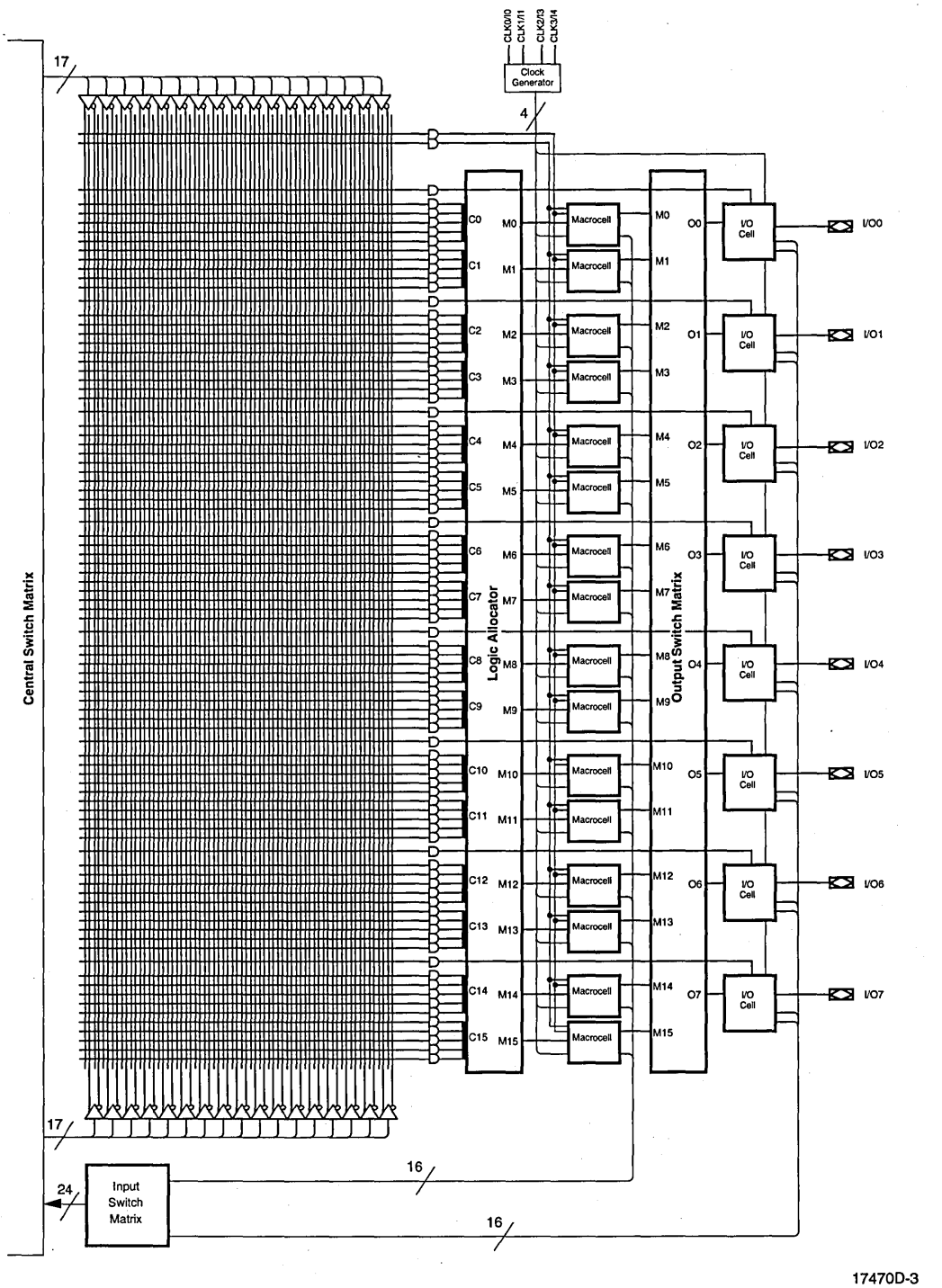


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Figure 1. MACH465 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C
Ambient Temperature
with Power Applied ..... –55°C to +125°C
Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V
DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V
DC Output or
I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V
Static Discharge Voltage ..... 2001 V
Latchup Current
(T_A = 0°C to +70°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air ..... 0°C to +70°C
Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz T_A = 25°C (Note 5)		285		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description			-12 Min	-12 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output			3	12	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock		D-type	5		ns
			T-type	6		ns
t_{HA}	Register Data Hold Time Using Product Term Clock			5		ns
t_{COA}	Product Term Clock to Output			4	14	ns
t_{WLA}	Product Term, Clock Width		LOW	8		ns
t_{WHA}			HIGH	8		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	D-type	52.6		MHz
			T-type	50.0		MHz
		Internal Feedback (f_{CNTA})	D-type	58.8		MHz
			T-type	55.6		MHz
		No Feedback (Note 3)		62.5		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock		D-type	7		ns
			T-type	8		ns
t_{HS}	Register Data Hold Time Using Global Clock			0		ns
t_{COS}	Global Clock to Output			2	8	ns
t_{WLS}	Global Clock Width		LOW	6		ns
t_{WHS}			HIGH	6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	D-type	66.7		MHz
			T-type	62.5		MHz
		Internal Feedback (f_{CNTA})	D-type	83.3		MHz
			T-type	76.9		MHz
		No Feedback (Note 3)		83.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			5		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock			5		ns
t_{GOA}	Product Term Gate to Output				16	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			6		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate			8		ns
t_{HLS}	Latch Data Hold Time Using Global Gate			0		ns
t_{GOS}	Gate to Output				10	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)			6		ns
t_{ICO}	Input Register Clock to Combinatorial Output				18	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-12 Min	-12 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	9		ns
		T-type	10		ns
t_{WICL}	Input Register Clock Width	LOW	6		ns
t_{WICH}		HIGH	6		ns
f_{MAXIR}	Maximum Input Register Frequency $1/(t_{WICL} + t_{WICH})$		83.3		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			16	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			18	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		ns
t_{WIGL}	Input Latch Gate Width LOW		6		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			16	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			16	ns
t_{APW}	Asynchronous Preset Width (Note 2)		12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	12	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	12	ns
Input Register with Standard-Hold-Time Option					
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			14	ns
t_{SIR}	Input Register Setup Time		2		ns
t_{HIR}	Input Register Hold Time		3		ns
t_{SIL}	Input Latch Setup Time		2		ns
t_{HIL}	Input Latch Hold Time		3		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate		9		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			16	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description	-12		Unit
		Min	Max	
Input Register with Zero-Hold-Time Option				
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		20	ns
t_{SIR}^{I}	Input Register Setup Time	6		ns
t_{HIR}^{I}	Input Register Hold Time	0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		22	ns

Notes:

1. *See Switching Test Circuit in the back of this Data Book for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature
with Power Applied ..... −55°C to +125°C
Supply Voltage with
Respect to Ground ..... −0.5 V to +7.0 V
DC Input Voltage ..... −0.5 V to V_{CC} +0.5 V
DC Output or
I/O Pin Voltage ..... −0.5 V to V_{CC} +0.5 V
Static Discharge Voltage ..... 2001 V
Latchup Current
(T_A = 0°C to +70°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air ..... 0°C to +70°C
Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			−100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	−30		−160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz T_A = 25°C (Note 5)		285		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	8		10		ns
				T-type	9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				8		10		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	9		12		ns
t_{WHA}				HIGH	9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	38.5		31.2		MHz
				T-type	37		30.3		MHz
		Internal Feedback (f_{CNTA})		D-type	47.6		37		MHz
				T-type	45.4		35.7		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	10		13		ns
				T-type	11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		ns
t_{COS}	Global Clock to Output (Note 2)				2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		8		ns
t_{WHS}				HIGH	6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback (Note 4)	$1/(t_{WLS} + t_{WHS})$		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				8		10		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		ns
t_{GOS}	Gate to Output (Note 2)					11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		8		ns
t_{ICO}	Input Register Clock to Combinatorial Output					20		25	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	15		20		ns
		T-type	16		21		ns
t_{WICL}	Input Register Clock Width	LOW	6		8		ns
t_{WICH}		HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		62.5		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			22		27	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		14		19		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		21		ns
t_{WIGL}	Input Latch Gate Width LOW		6		8		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	15	2	20	ns
Input Register with Standard-Hold-Time Option							
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			17		22	ns
t_{SIR}	Input Register Setup Time		2		2		ns
t_{HIR}	Input Register Hold Time		4		5		ns
t_{SIL}	Input Latch Setup Time		2		2		ns
t_{HIL}	Input Latch Hold Time		4		5		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate		10		12		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate		12		16		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19		24	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

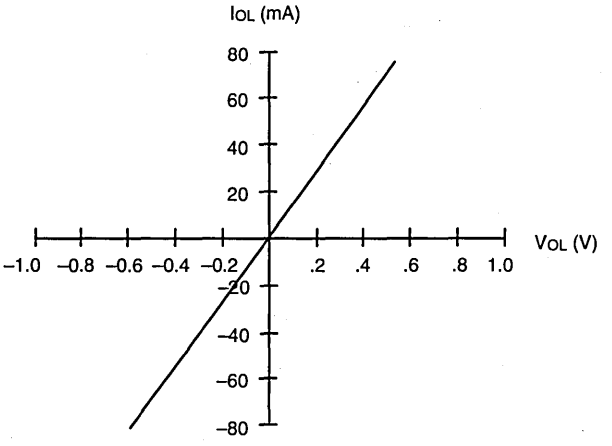
Parameter Symbol	Parameter Description	-15		-20		Unit
		Min	Max	Min	Max	
Input Register with Zero-Hold-Time Option						
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		23		30	ns
t_{SIR}^{I}	Input Register Setup Time	6		8		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		8		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	16		20		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	18		24		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		25		32	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



Output, LOW

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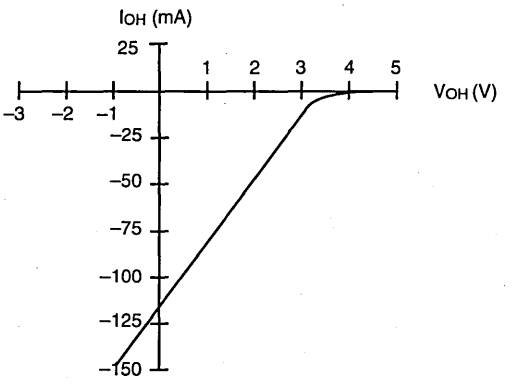
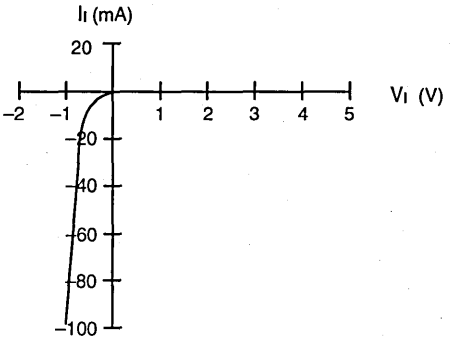


17470D-5

Output, HIGH



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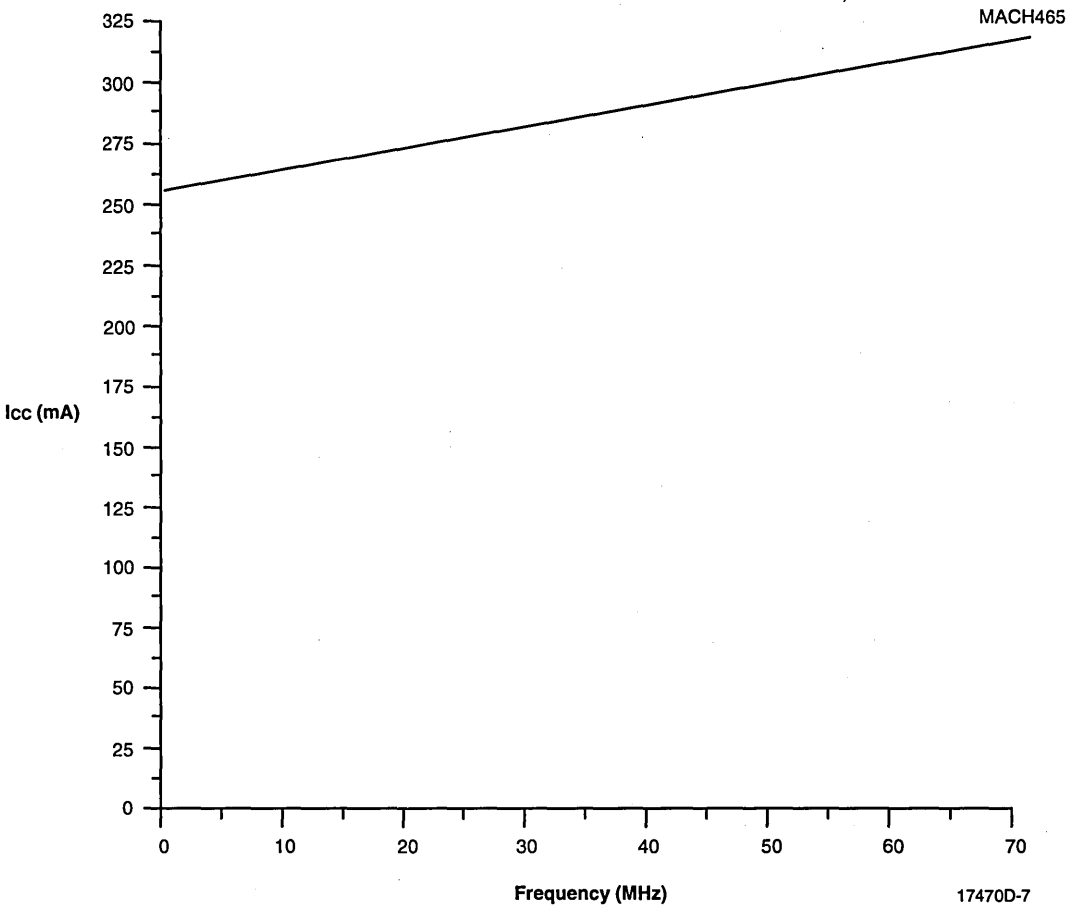
Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

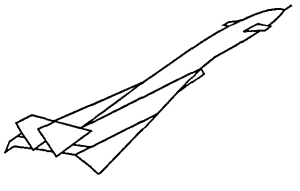
TYPICAL THERMAL GUIDELINES

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PQFP	Unit
θ_{jc}	Thermal impedance, junction to case		4.7	°C/W
θ_{ja}	Thermal impedance, junction to ambient		23.2	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	20.6	°C/W
		400 lfpm air	17.7	°C/W
		600 lfpm air	15.1	°C/W
		800 lfpm air	13.8	°C/W

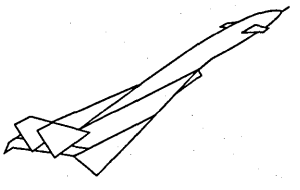
Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

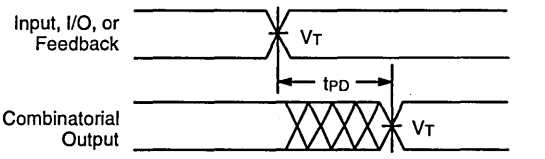


CHAPTER

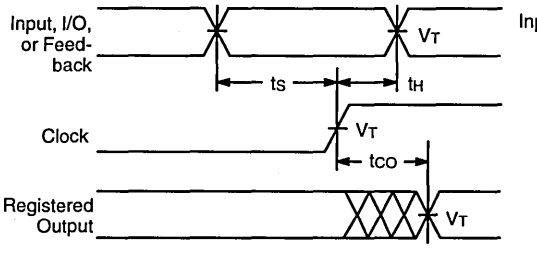
3 GENERAL INFORMATION



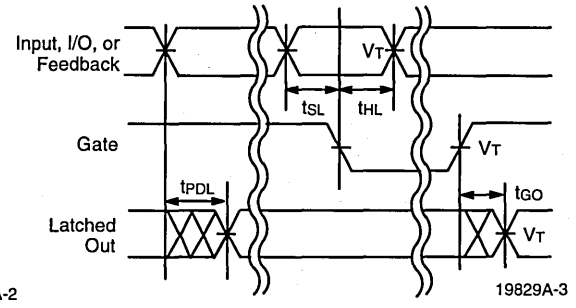
SWITCHING WAVEFORMS



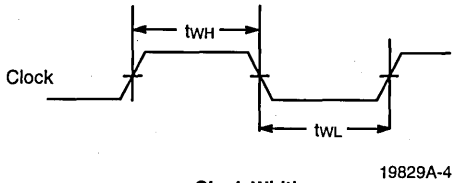
Combinatorial Output



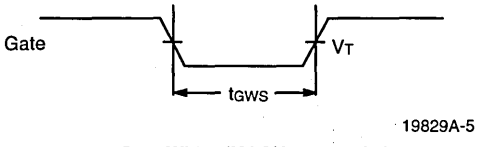
Registered Output



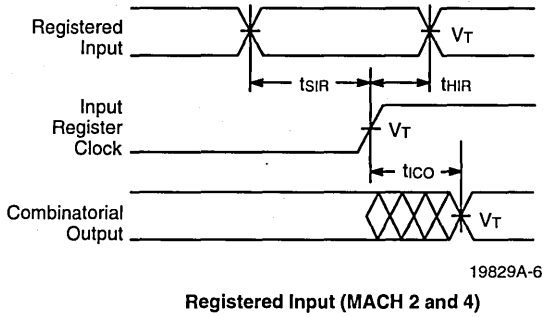
Latched Output (MACH 2, 3, and 4)



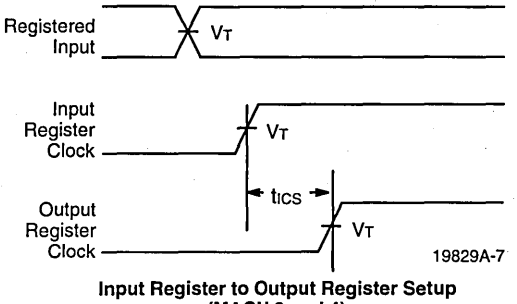
Clock Width



Gate Width (MACH 2, 3, and 4)



Registered Input (MACH 2 and 4)

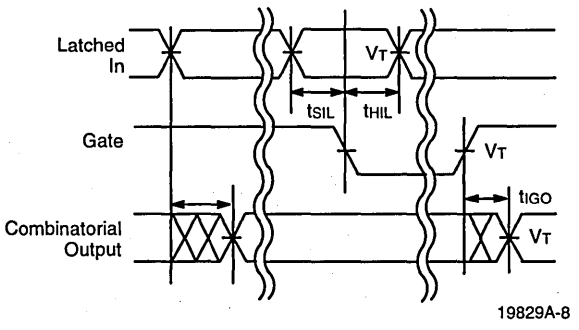


Input Register to Output Register Setup (MACH 2 and 4)

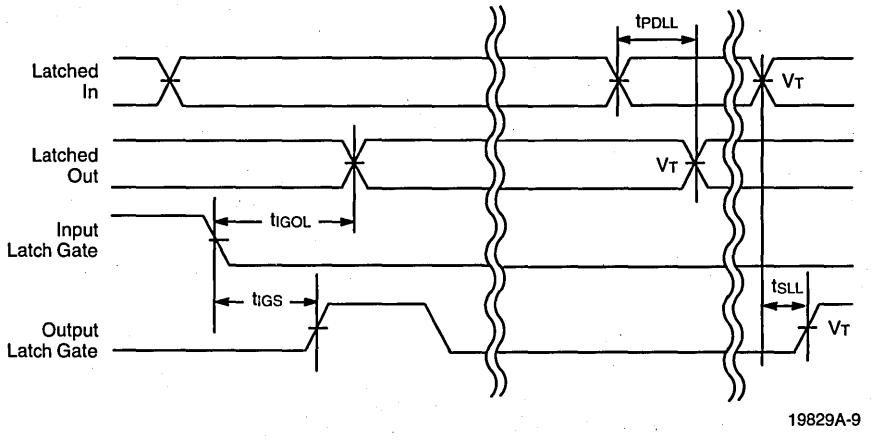
Notes:

1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



Latched Input (MACH 2 and 4)

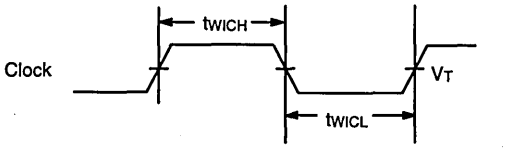


Latched Input and Output (MACH 2, 3, and 4)

Notes:

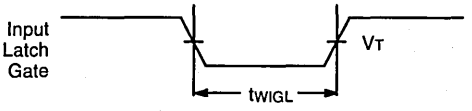
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



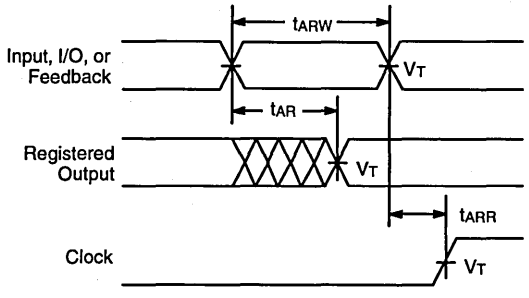
19829A-10

Input Register Clock Width (MACH 2 and 4)



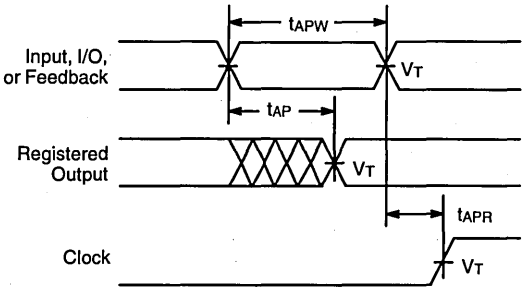
19829A-11

Input Latch Gate Width (MACH 2 and 4)



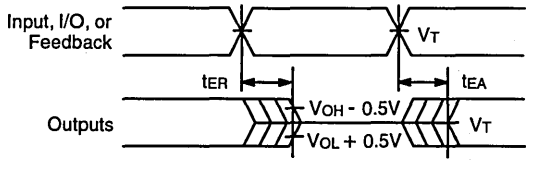
19829A-12

Asynchronous Reset



19829A-13

Asynchronous Preset



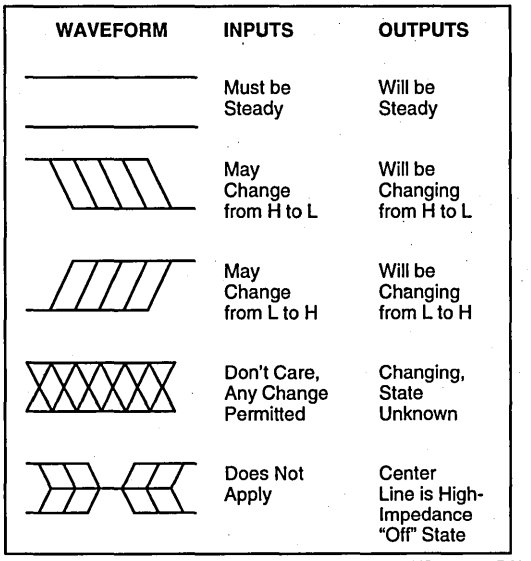
19829A-14

Output Disable/Enable

Notes:

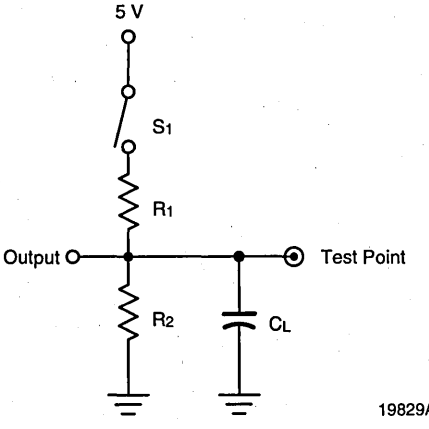
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT



19829A-15

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

**Switching several outputs simultaneously should be avoided for accurate measurement.*

f_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

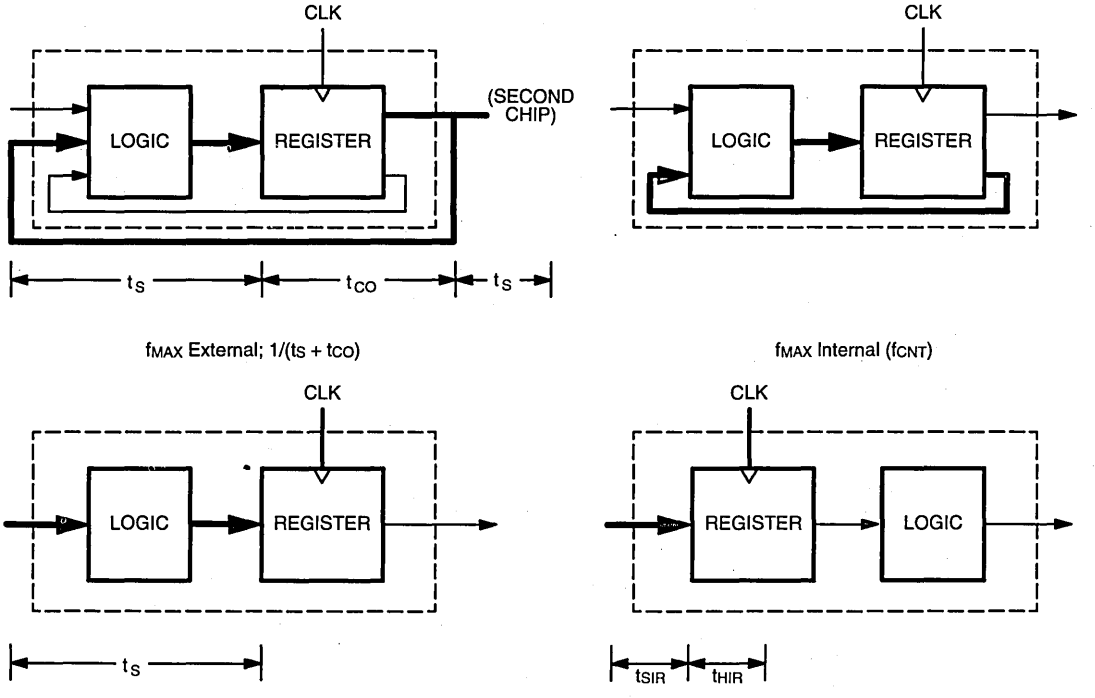
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are use in the same path, the overall frequency will be limited by t_{ICS}.

All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



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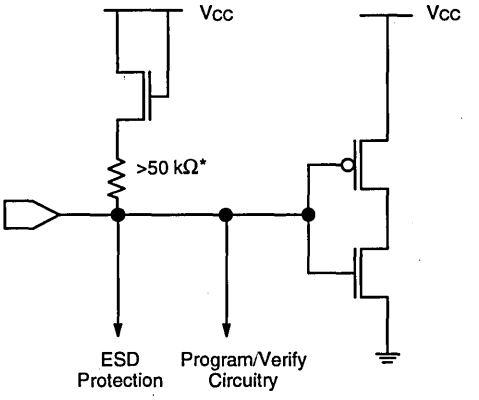
ENDURANCE CHARACTERISTICS

The MACH families are manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

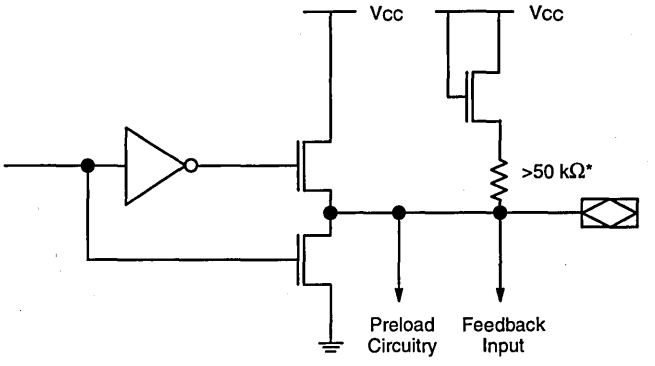
Endurance Characteristics

Parameter Symbol	Parameter Description	Min	Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS (For MACH110, MACH120, MACH130, MACH210, MACH220, MACH230, MACH355, MACH435, MACH445, and MACH465)



Input



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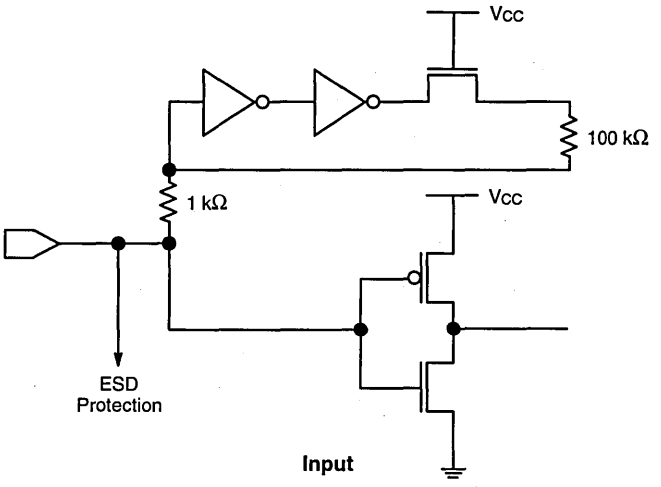
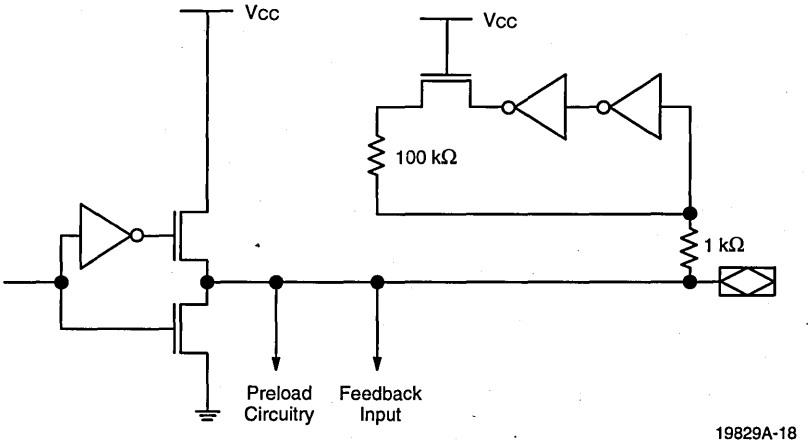
Output

Built-in pull-up is on MACH210A, MACH215, MACH220, MACH355, MACH435, MACH445, and MACH465

INPUT/OUTPUT EQUIVALENT SCHEMATICS
(For MACH111, MACH131, MACH211, MACH221, and MACH231)



Input



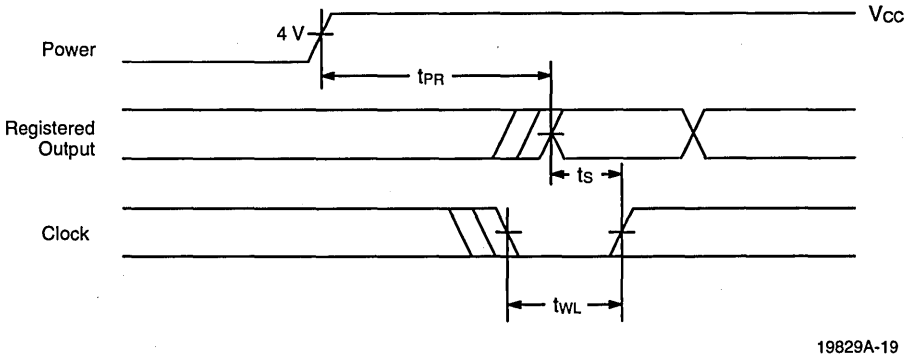
I/O

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

USING PRELOAD AND OBSERVABILITY

In order to be testable, a circuit must be both controllable and observable. To achieve this, the MACH devices incorporate register preload and observability.

In preload mode, each flip-flop in the MACH device can be loaded from the I/O pins, in order to perform functional testing of complex state machines. Register preload makes it possible to run a series of tests from a known starting state, or to load illegal states and test for proper recovery. This ability to control the MACH device's internal state can shorten test sequences, since it is easier to reach the state of interest.

The observability function makes it possible to see the internal state of the buried registers during test by overriding each register's output enable and activating the output buffer. The values stored in output and buried registers can then be observed on the I/O pins. Without this feature, a thorough functional test would be impossible for any designs with buried registers.

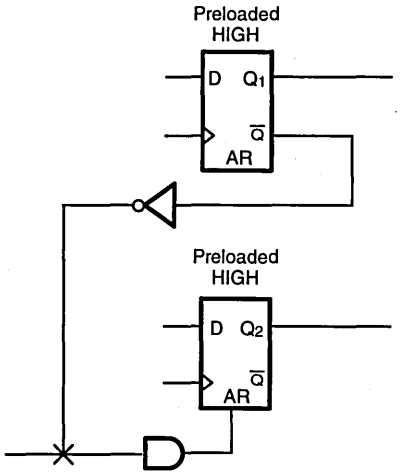
While the implementation of the testability features is fairly straightforward, care must be taken in certain instances to insure valid testing.

One case involves asynchronous reset and preset. If the MACH registers drive asynchronous reset or preset lines and are preloaded in such a way that reset or preset are asserted, the reset or preset may remove the preloaded data. This is illustrated in Figure 1. Care should be taken when planning functional tests, so that states that will cause unexpected resets and presets are not preloaded.

Another case to be aware of arises in testing combinatorial logic. When an output is configured as combinatorial, the observability feature forces the output into registered mode. When this happens, all product terms are forced to zero, which eliminates all combinatorial data. For a straight combinatorial output, the correct value will be restored after the preload or observe function, and there will be no problem. If the function implements a combinatorial latch, however, it relies on feedback to hold the correct value, as shown in Figure 2. As this value may change during the preload or observe operation, you cannot count on the data being correct after the operation. To insure valid testing in these cases, outputs that are combinatorial latches should not be tested immediately following a preload or observe sequence, but should first be restored to a known state.

All MACH 1 devices support preload and all MACH 2 devices support both preload and observability.

Contact individual programming vendors in order to verify programmer support.



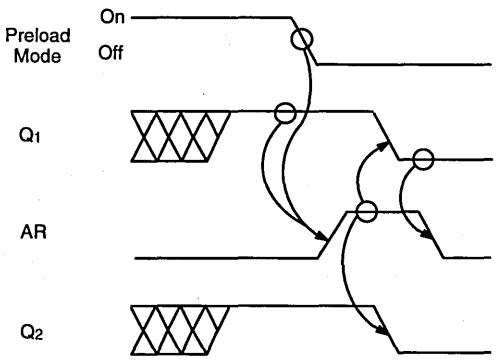


Figure 1. Preload/Reset Conflict

19829A-20

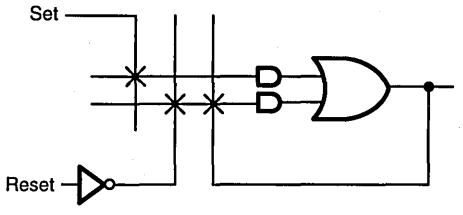


Figure 2. Combinatorial Latch

19829A-21

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	MACHXL® Software Ver. 2.0
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	Design Center/AMD Software
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	AMD-ABEL Software Data I/O MACH Fitters
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	PROdeveloper/AMD Software PROsynthesis/AMD Software
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234	ComposerPIC™ Designer (Requires MACH Fitter) Verilog, LeapFrog, RapidSim Simulators (Models also available from Logic Modeling) Ver. 3.3
Capilano Computing 960 Quayside Dr., Suite 406 New Westminster, B.C. Canada V3M 6G2 (800) 444-9064 or (604) 552-6200	MacABEL™ Software (Requires SmartPart MACH Fitter)
CINA, Inc. P.O. Box 4872 Mountain View, CA 94040 (415) 940-1723	SmartCAT Circuit Analyzer
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™-5 Software (Requires MACH Fitter) Synario™ Software
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (89) 857-6667	PLDSim 90
ISDATA GmbH Daimlerstr. 51 D7500 Karlsruhe 21 Germany Germany: 0721/75 10 87 U.S.: (510) 531-8553	LOG/iC™ Software (Requires MACH Fitter)
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690-6900	SmartModel® Library
Logical Devices, Inc. 692 S. Military Trail Deerfield Beach, FL 33442 (800) 331-7766 or (305) 428-6868	CUPL™ Software

DEVELOPMENT SYSTEMS (subject to change) (continued)

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (503) 685-7000	PLDSynthesis™ (Requires MACH Fitter) QuickSim Simulator (Models also available from Logic Modeling)
MicroSim Corp. 20 Fairbanks Irvine, CA 92718 (714) 770-3022	Design Center Software (Requires MACH Fitter)
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (800) 755-FPGA or (719) 590-1155	PLDesigner™-XL Software (Requires MACH Fitter)
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Programmable Logic Design Tools 386+ Schematic Design Tool 386+ Digital Simulation Tools
SUSIE–CAD 10000 Nevada Highway, Suite 201 Boulder City, NV 89005 (702) 293-2271	SUSIE™ Simulator
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 442-4660 or (508) 480-0881	ViewPLD or PROPLD (Requires PROSim Simulator MACH Fitter) ViewSim Simulator (Models for ViewSim also available from Logic Modeling)
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Test Generation Software
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (87) 857-6667	PLDCheck 90

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APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

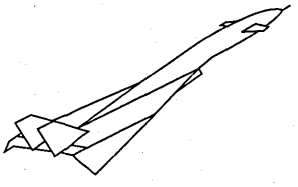
MANUFACTURER	PROGRAMMER CONFIGURATION
Advin Systems, Inc. 1050-L East Duane Ave. Sunnyvale, CA 94086 (408) 243-7000	Pilot U84
BP Microsystems 100 N. Post Oak Rd. Houston, TX 77055-7237 (800) 225-2102 or (713) 688-4600	BP1200
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	UniSite™ • Model 3900 AutoSite
Logical Devices Inc./Digelec 692 S. Military Trail Deerfield Beach, FL 33442 (800) 331-7766 or (305) 428-6868	ALLPRO™–88
SMS North America, Inc. 16522 NE 135th Place Redmond, WA 98052 (800) 722-4122 or SMS Im Grund 15 D-7988 Vangen Im Allgau, Germany 07522-5018	Sprint/Expert
Stag Microsystems Inc. 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire UK AL7 1JT 707-332148	Stag Quazar
System General 510 S. Park Victoria Dr. Milpitas, CA 95035 (408) 263-6667 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Rd., Shin Diau Taipei, Taiwan 2-917-3005	Turpro-1

APPROVED ON-BOARD PROGRAMMERS

MANUFACTURER	PROGRAMMER CONFIGURATION
Corelis, Inc. 12607 Hidden Creek Way, Suite H Cerritos, California 70703 (310) 926-6727	JTAG PROG
Advanced Micro Devices P.O. Box 3453, MS-1028 Sunnyvale, CA 94088-3453 (800) 222-9323	MACHpro

PROGRAMMER SOCKET ADAPTERS (subject to change)

MANUFACTURER	PART NUMBER
EDI Corporation P.O. Box 366 Patterson, CA 95363 (209) 892-3270	Contact Manufacturer
Emulation Technology 2344 Walsh Ave., Bldg. F Santa Clara, CA 95051 (408) 982-0660	Contact Manufacturer
Logical Systems Corp. P.O. Box 6184 Syracuse, NY 13217-6184 (315) 478-0722	Contact Manufacturer
Procon Technologies, Inc. 1333 Lawrence Expwy, Suite 207 Santa Clara, CA 95051 (408) 246-4456	Contact Manufacturer



Design Tool Support for MACH Devices

Advanced Micro Devices

Customers have described the ideal programmable logic design environment as one that supports several different design entry methods, is architecture independent, has an easy to use interface, tightly integrates schematic entry and timing simulation, and offers state of the art technology such as multiple device partitioning across different types of programmable logic devices. Others feel that the ideal programmable design environment should interface tightly to PCB layout and mixed digital and analog simulation tools, while still other customers feel the ideal design tool should support devices from many different programmable logic vendors.

The trouble is that everyone's picture of the ideal programmable logic design environment is different. That's why AMD offers its customers a choice of software and programming tools for designing with MACH devices. With MACH devices, customers have a choice of design environments:

- **Support for universal design tools** customers already own: MACH device fitters and libraries are available from Cadence, Data I/O, Logical Devices, Synopsys Logic Modeling, Mentor, MicroSim, Minc, OrCAD, SUSIE-CAD, Synopsys, and Viewlogic for PC-based and workstation environments. These add-on MACH device Fitters and libraries are available at little or no additional cost from the design tool vendor. Most AMD PAL customers find that an add-on Fitter and MACH device libraries is all that is required to get started designing with AMD MACH devices.

  In addition, add-on MACH device Fitters for Data I/O's ABEL software are also available from AMD and its distributors.

- **AMD-only versions of popular third-party design tools**: Through AMD and its resellers, customers can purchase AMD-only versions of MicroSim's "Design Center" and Data I/O's "ABEL-6" and "Synario". These systems offer complete start-to-finish third-party support for MACH in a single integrated environment. These AMD-only versions also allow customers who are considering upgrading their design tools a chance to get started with higher-end tools at a lower cost. Later on, the customer can upgrade to a full universal version of these tools through the tool vendor at a reduced cost.

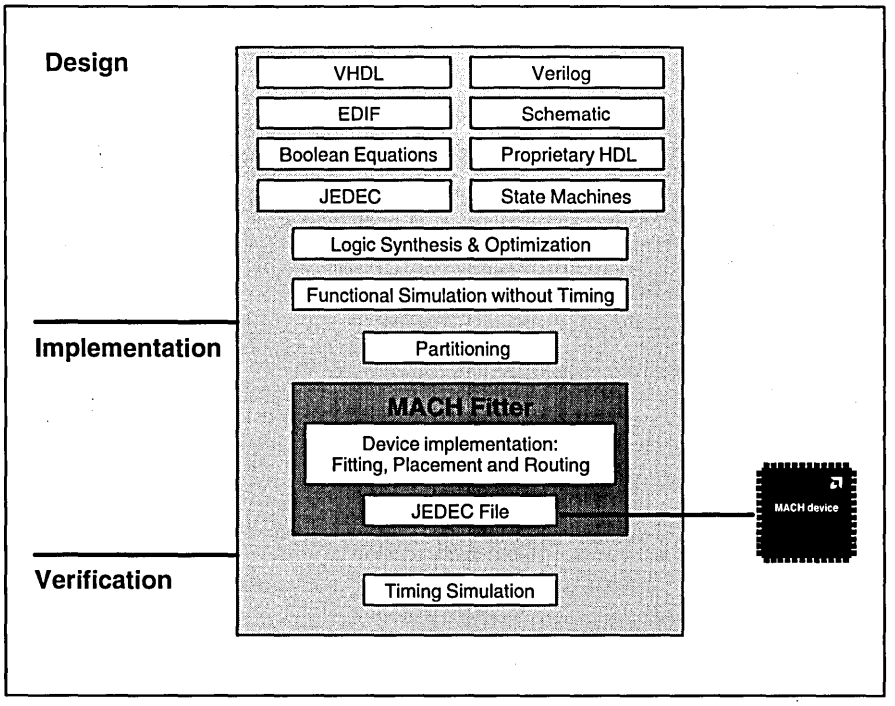
- **AMD-developed MACHXL software** for very low-cost, text-based design environments.

Each of these scenarios are discussed in the sections that follow.

Support for Universal Design Environments

AMD's MACH devices are supported by AMD FusionPLD partners, a select group of leading third-party design tool vendors with proven track records. Actual development work with these vendors begins far in advance of AMD's introduction of new devices. Each FusionPLD partner adheres to AMD's strict quality and certification requirements. The end result is timely support of new AMD MACH devices on a large number of platforms.

Designing with MACH devices is almost as easy as designing with AMD PAL devices. Customers begin their design using traditional design entry methods—Boolean equations, schematic capture, state machine syntax, VHDL, Verilog, or a design tool's HDL—and move through logic synthesis before functionally simulating their design to verify the logic. Once a designer completes the design phase, they move on to the implementation phase where the compiler will partition the logic. An add-on MACH Fitter available from the third-party tool vendor performs the placement and routing steps completely within the native third-party design tool environment.



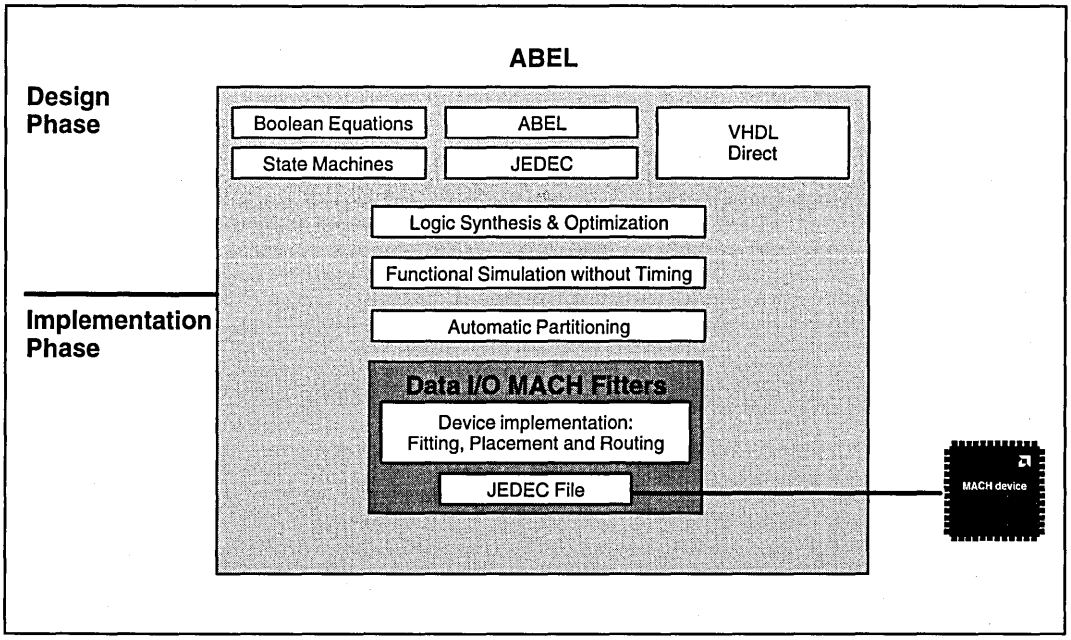
General MACH design flow for third-party design environments

Once the design has been implemented in a MACH device, the designer can verify its operation with the design tool's timing simulator and waveform analysis tools.

Note that Cadence, Mentor, MicroSim, Synopsys and Viewlogic customers who have not used these tools for PAL device designs before may also need to acquire a logic compiler for logic synthesis and minimization. These customers should verify that they have the appropriate programmable logic compiler either by running a PAL device through their system or by contacting their design tool account representative:

- Cadence: PIC-Designer software
- Data I/O: Synario software
- Data I/O: ABEL-6
- Mentor: PLD Synthesis II software
- MicroSim: PLSyn software
- Synopsys: Minc PLDesigner-XL software
- Viewlogic PRO Series: PROPLD software
- Viewlogic WorkView or PowerView: ViewPLD software

MACH device Fitters for these environments can be obtained directly from the third party tool vendor.



Data I/O MACH Fitters

Devices Supported	MACH110, 120, 130, 210, 215, 220, 230, and 435 devices
Design Entry	ABEL-6 for PC-DOS required
AMD Ordering Part Number	PLDSW/AMDABELB1322

Add-on MACH Fitters for Data I/O ABEL software version 6.0 or above are available from AMD and its distributors as well as Data I/O. MACH Fitters for ABEL software integrate tightly into the customer's existing ABEL-6 design environment, providing a transparent link between ABEL design descriptions and MACH-specific device Fitters. Everything a customer needs to design with MACH devices is right there in the Data I/O environment. Customers develop their designs using ABEL syntax, then compile and functionally simulate the design before choosing the SmartPart MACH Fitter from the menu. The MACH Fitter will automatically place and route the device and create the JEDEC file.

Recommended System Configuration

- ABEL-6 for PC-DOS already installed
- 640 Kbyte conventional memory, 2-4 Mbyte extended memory
- 4 Mbyte additional disk space

AMD-only Versions of Third-Party Tools

AMD and its distributors resell AMD-only versions of popular third-party design tools from MicroSim, Data I/O, and Viewlogic. These resale arrangements allow AMD to offer its customers state-of-the-art desktop-based design tools at affordable prices. All these third-party tools are AMD-certified, so designers can be confident of their resulting pinouts and JEDEC files. Most also include one year of free device updates for new MACH devices and maintenance. All these AMD-only third-party design tools can also be upgraded to full universal versions supporting other device manufacturers through the third-party tool vendor at a substantial discount.

Each of these AMD-only third-party software products—MicroSim's Design Center/AMD, Data I/O's AMD/Synario, and Data I/O's AMD-ABEL—are discussed below.

Design Center/AMD tools are developed by MicroSim, the creator of PSpice. Design Center/AMD software offers customers device-independent high-performance logic synthesis carefully integrated with interactive schematic capture and min-max timing simulation. The Design Center/AMD system is available in two versions—a Standard version without timing simulation and a graphical editor for inputting test vectors, and an Advanced version with timing simulation and the graphical stimulus editor. An Evaluation version, supporting only the MACH210 device permits customers to evaluate the Design Center/AMD software and the MACH device architecture.

Design Center/AMD Software

Devices Supported	Standard All PAL and MACH devices	Advanced All PAL and MACH devices	Evaluation MACH231 only
Design Entry			
Schematic capture	X	X	X
Symbol editor	X	X	X
Boolean equations	X	X	X
State machines	X	X	X
Hierarchical design	X	X	X
Mixed schematic and language	X	X	X
Design Processing			
Design rule checks	X	X	X
Logic synthesis and fitting	X	X	X
User-defined device selection criteria and automated device selection	X	X	X
Single device partitioning	X	X	X
Multiple Device Partitioning	option	option	N/A
JEDEC generation	X	X	X
Backannotation of pinouts	X	X	X
Design Verification			
Functional simulation	X	X	X
Timing simulation	N/A	X	X
Waveform viewer	X	X	X
Waveform editing	text	graphical & text	graphical & text
Interactive cross probing from schematic	X	X	X
AMD Ordering Part Number			
Without Multiple Device Partitioning	PLDSW/DCSTDB1322	PLDSW/DCADVB1322	PLDSW/DCEVALB1322
With Multiple Device Partitioning	PLDSW/DCSTDMB1322	PLDSW/DCADVMB1322	N/A

Recommended System Configuration

- 386-based or better PC (486 recommended)
- 8 Mbyte RAM
- 20 Mbyte hard disk space
- MS-DOS 3.0 or higher
- Microsoft Windows 3.1 or later (386 enhanced mode)
- 1.44 Mbyte 3.5" floppy disk drive

Multiple-device partitioning, an option to Design Center/AMD Standard and Advanced products, can be used to partition large designs across different types of programmable logic devices and retarget existing designs. If a design does not fit into a single device, such as a MACH435, this add-on option will split the design and implement it in more than one device, such as a MACH435 and a PALCE22V10. Because the customer controls the device selection constraints and priorities such as frequency, the type of device, maximum propagation delay, power, temperature, technology, the number of pins and the number of devices, the resulting implementation is always under their control. Design Center/AMD software will present the ten top solutions meeting the customer's constraints and priorities before generating JEDEC files for the solution the customer chooses.

AMD/Synario software, based on Data I/O's Synario universal design system, supports AMD PAL and MACH devices in a fully integrated Microsoft Windows environment. AMD/Synario offers mixed-mode design entry (schematics and behavioral descriptions) and hierarchical design support in both modes. Behavioral description design entry is available in VHDL and ABEL HDL. AMD/Synario also features simulation.

Recommended System Configuration

- 386-based or better PC (486 recommended)
- 8 Mbyte RAM minimum (16 Mbyte RAM recommended)
- 20 Mbyte hard drive space
- MS-DOS 5.0 or higher
- Microsoft Windows 3.1 or later
- 1.44 Mbyte 3.5" floppy disk drive

AMD-ABEL software, based on Data I/O's popular ABEL-6 software, supports both AMD PAL and MACH devices and includes MACH device Fitters. AMD-ABEL is ideal for customers who are just beginning to work with AMD MACH devices or who are looking to upgrade their existing tools. It includes everything needed to get new customers designing with AMD PAL or MACH devices in a familiar PC-based environment.

	AMD-ABEL
Devices Supported	All PAL and MACH110, 120, 130, 210, 215, 220, 230, and 435 devices
Design Entry	
Boolean equations	X
State machines	X
VHDL	available from Data I/O
Design Processing	
Design rule checks	X
Logic synthesis and fitting	X
User-defined device selection criteria and automated device selection	X
Single device partitioning	X
JEDEC generation	X
Back annotation of pinouts	X
Design Verification	
Functional simulation	X
Waveform viewer	X
Waveform editing	text
AMD Ordering Part Number	PLDSW/AMDABELB1322

Recommended System Configuration

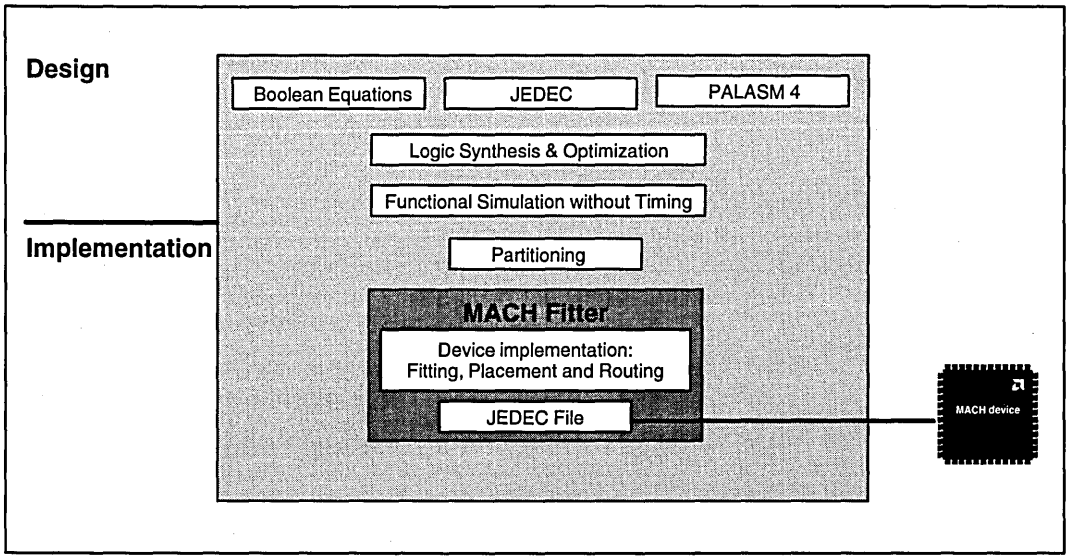
- 386-based or better PC (486 recommended)
- 640 Kbyte RAM conventional memory, 2-4 Mbyte RAM extended memory
- 20 Mbyte disk space
- MS-DOS 5.0 or higher
- 1.44 Mbyte 3.5" floppy disk drive
- Parallel port for key
- Mouse optional
- Note: AMD-ABEL is not a Windows program, but may be used from a DOS application window.

For customers who already have ABEL-6 software, the Data I/O MACH Fitters are also available separately from AMD and its distributors. See the previous section for more information.

AMD-Developed MACHXL Software

AMD's MACHXL software is a menu-driven entry-level tool for designing with AMD MACH devices. Based on AMD's PALASM 4 software, MACHXL software fully supports the density and flexibility of MACH devices in a low-cost, PC-based design environment.

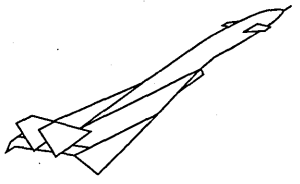
The MACHXL software design flow is shown below:



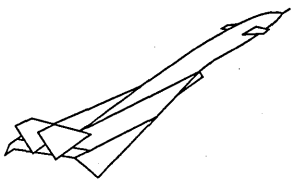
New designs begin with Boolean equation entry, by importing a PALASM 4 file, or by disassembling a JEDEC file. Customers have control over logic synthesis and optimization, and can functionally simulate before implementing their design.

	MACHXL
Devices Supported	All MACH devices and Standard PAL.
Design Entry	
Boolean equations	X
MINC's DSL files	X
PALASM 4 design files	X
Design Processing	
Design rule checks	X
Logic synthesis and fitting	X
Single device partitioning	X
JEDEC generation	X
Back annotation of pinouts	X
Design Verification	
Functional simulation	X
Waveform viewer	X
Waveform editing	text
AMD Ordering Part Number	AMPLDSW/MXLB1322

For a more complete description, see the MACHXL software manual or an AMD sales person.



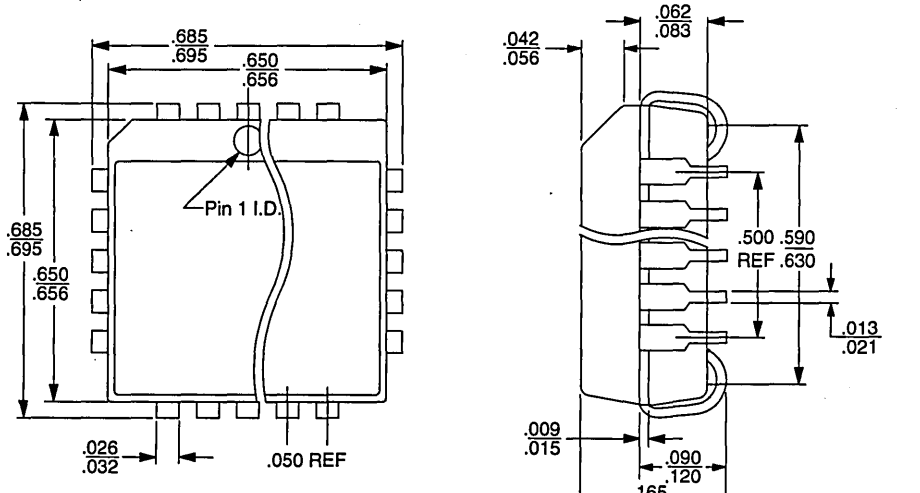
PHYSICAL DIMENSIONS*



PHYSICAL DIMENSIONS*

PL 044

44-Pin Plastic Leaded Chip Carrier (measured in inches)



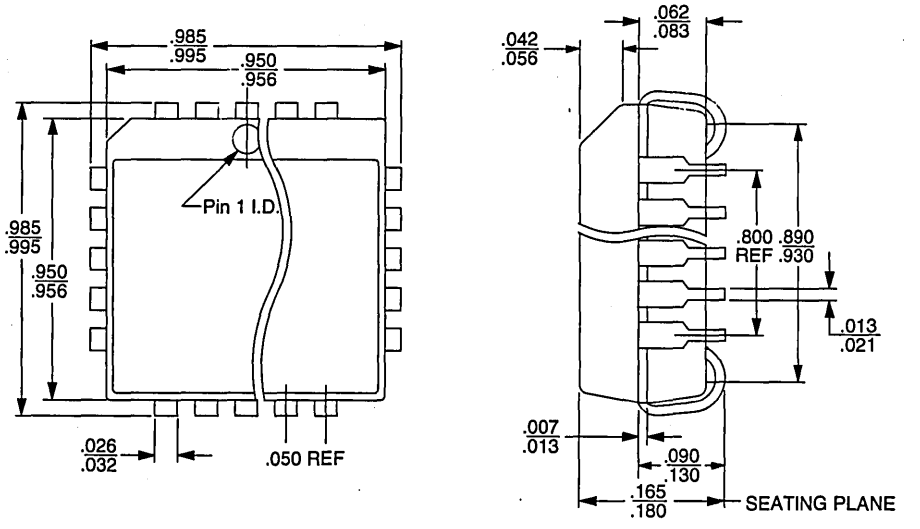
TOP VIEW

SIDE VIEW

16-038-SQ
PL 044
DA78
6-28-94 ae

PL 068

68-Pin Plastic Leaded Chip Carrier (measured in inches)



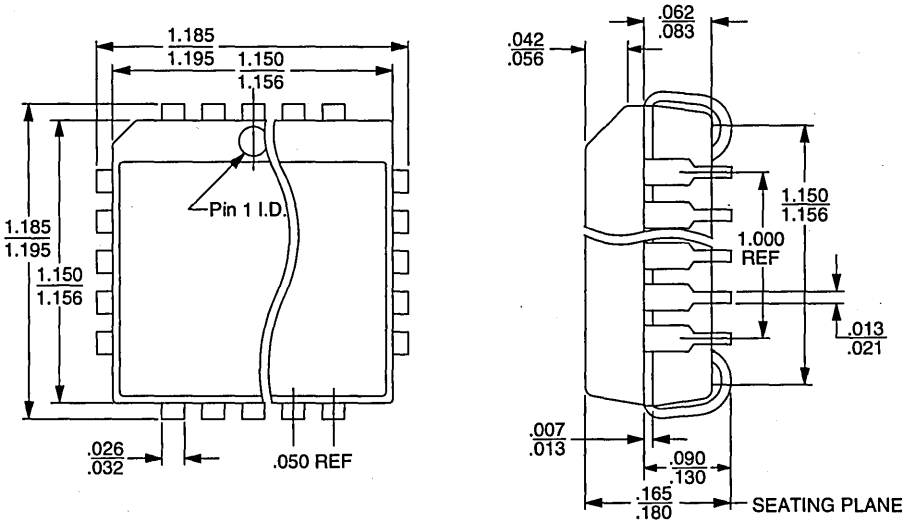
TOP VIEW

SIDE VIEW

16-038-SQ
PL 068
DA78
6-28-94 ae

**For reference only. BSC is an ANSI standard for Basic Space Centering.*

PL 084
84-Pin Plastic Leaded Chip Carrier (measured in inches)



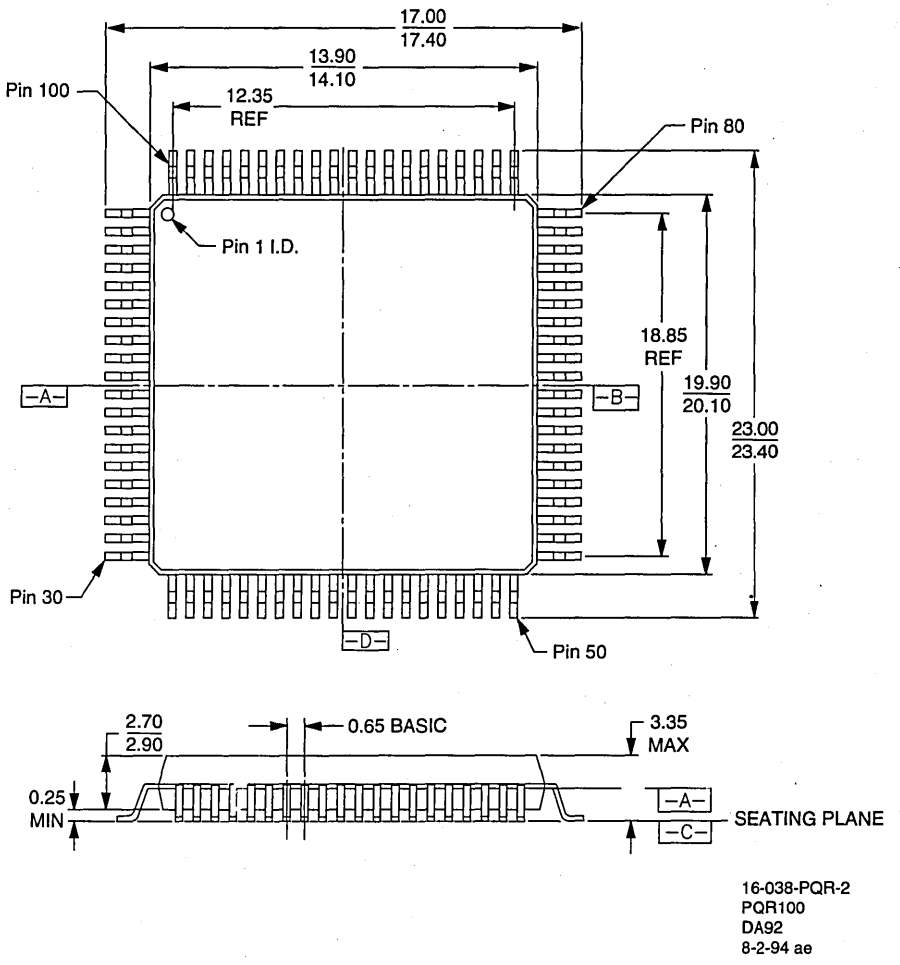
16-038-SQ
PL 068
DA78
6-28-94 ae

**For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS*

PQR100

100-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)



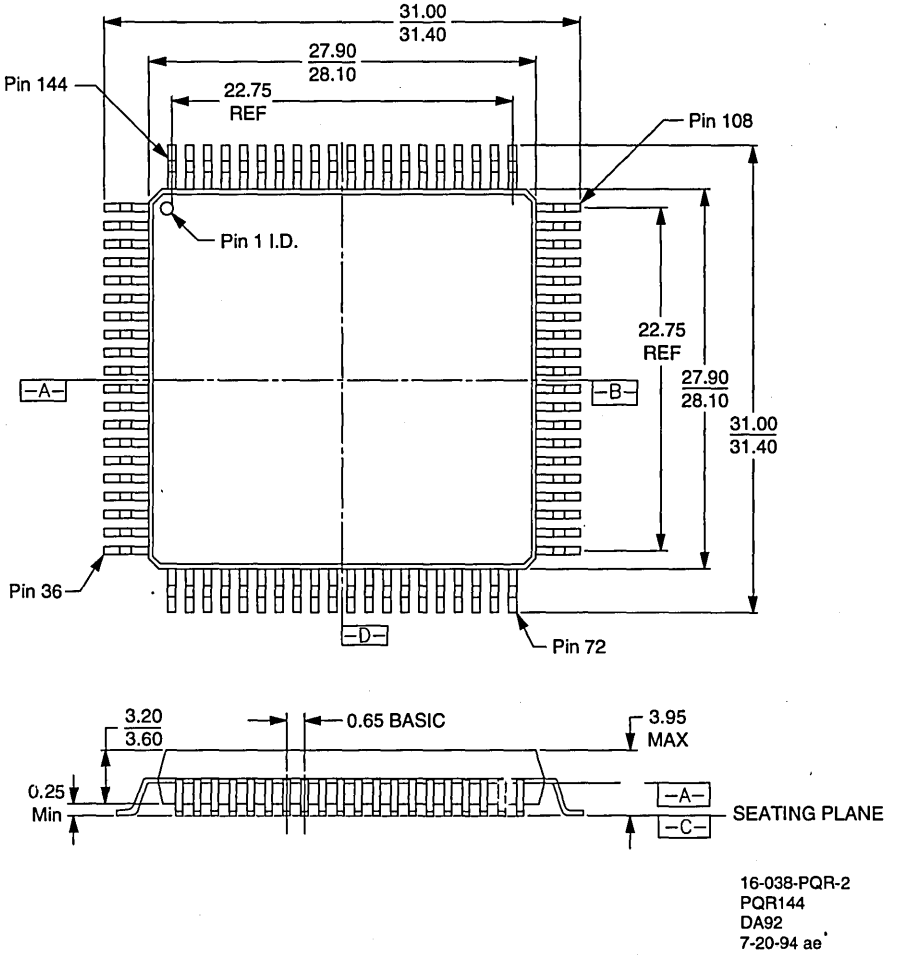
Note:
Although the PQR100 package is drawn as a square package, the actual package is rectangular as the dimensions suggest.

**For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS*

PQR144

144-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)

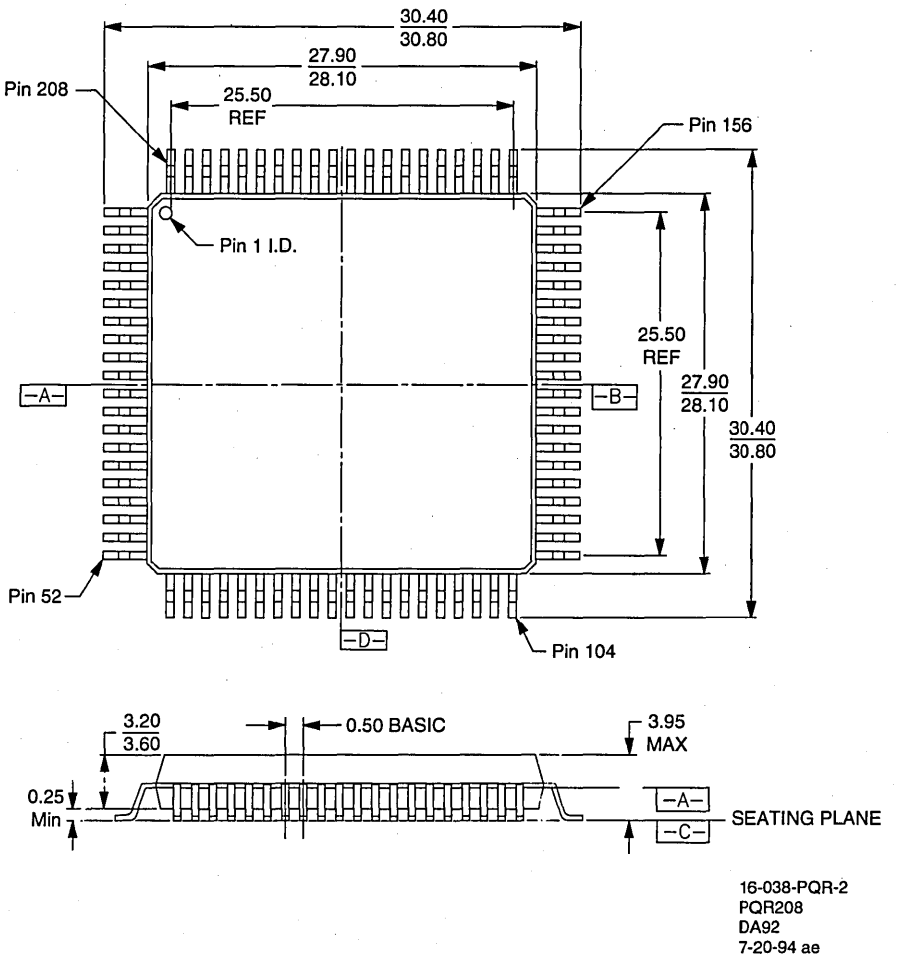


**For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS*

PQR208

208-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)

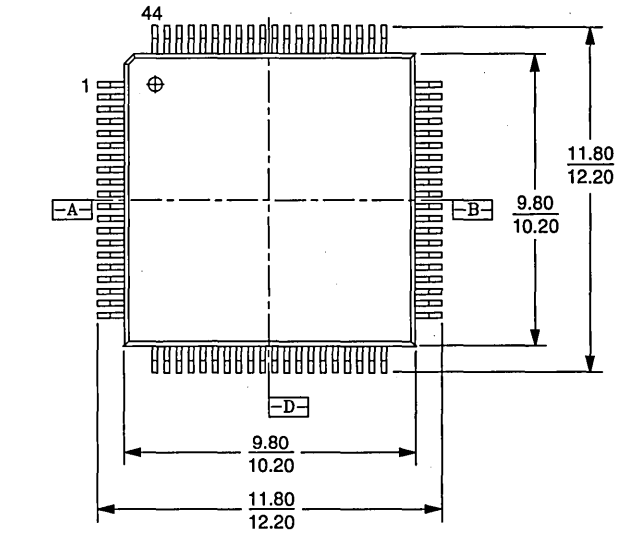


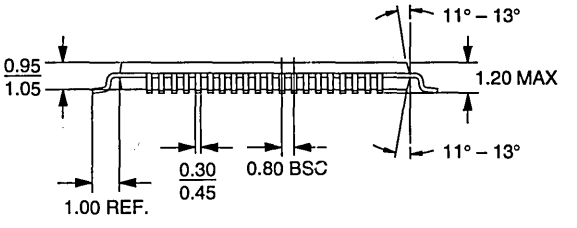
**For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS*

PQT044

44-Pin Thin Quad Flat Pack (measured in millimeters)



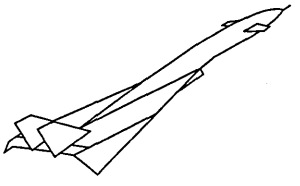


16-038-PQT-2_AH
PQT 44
5-4-95 ae

For reference only. BSC is an ANSI standard for Basic Space Centering.

CHAPTER

4 APPLICATION NOTES



MACH Device Design Planning Guide

Advanced Micro Devices

Application Note

1.0 INTRODUCTION

This technical brief provides planning guidelines for a MACH device design that will lead to its successful implementation. The method presented estimates whether logic will fit in a MACH device before the design has been entered.

The tutorial in this brief is an exhaustive device resource analysis. For many designs, an analysis like this is not practical, and instead, a rough estimation of pins, product term clusters (see definition in section 3.2), reset, preset, and tristate resources is used to predict fitting.

- The planning-process overview in discussion 2 introduces you to the differences between planning PAL device designs and MACH-device designs.
- A counter design is used in discussion 3 to illustrate the MACH design planning process.
- Discussion 4 is a summary.
- The appendices provide the complete PALASM 4 software, .PDS design file and MACH Fitter report.

As a reader, you should be familiar with the MACH devices and architectures described in the *MACH Family Data Book*. You should also know how to count/estimate the number of product terms (PTs) in a design.

2.0 DESIGN PLANNING PROCESS OVERVIEW

The MACH design planning process applied in it's full detail differs from a standard PAL device design process as shown in Figure 1.

PAL devices have a universal internal interconnect while MACH devices provide a reduced interconnect through the switch matrix. The block partitioning steps used when you're estimating with a high degree of detail (as in the following tutorial) are not required when estimating a single PAL device design. Note, however, that if multiple PAL devices are used in a design, similar partitioning steps between PAL devices are necessary.

Both the PAL and MACH device planning processes begin with a well-defined high-level design. You analyze and count the resources required for the design and select an appropriate device.

Block Partitioning Steps *(optional, for detailed planning):*

- Once a MACH device is selected, you begin design partitioning by determining which of the partitioning constraints apply to the design.
- Then you place logic into blocks in a way that maximizes common inputs of equations within the blocks without exceeding the limits of block partitioning constraints.
- Lastly, the resources used in each block are counted.

If the block partitioning steps are performed, you can calculate device and block resources precisely, from which an informed decision may be made as to whether the design will fit. If the block partitioning steps aren't performed, a less reliable decision is made using the information gathered in step 3.2.

3.0 PLANNING A MACH-DEVICE COUNTER DESIGN

The following example illustrates the MACH device planning process in detail. The level of detail in your planning process may vary due to individual design styles and time constraints. Since the design must be entered and the software run to guarantee that the design will fit even if the block partitioning steps have been completed, many users skip the block partitioning steps.

3.1 High-Level Design

Planning begins with a high-level definition of the design. Figure 2 illustrates an 8-bit counter that can be parallel-loaded from I/O pins which also output the count value. The counter counts up or down, based on the control bits, and may be reset or preset. The counter output is decoded to generate several pulse and clock-divide outputs (decoded equations are described and shown in the BUSCNTR.PDS design file in Appendix A).

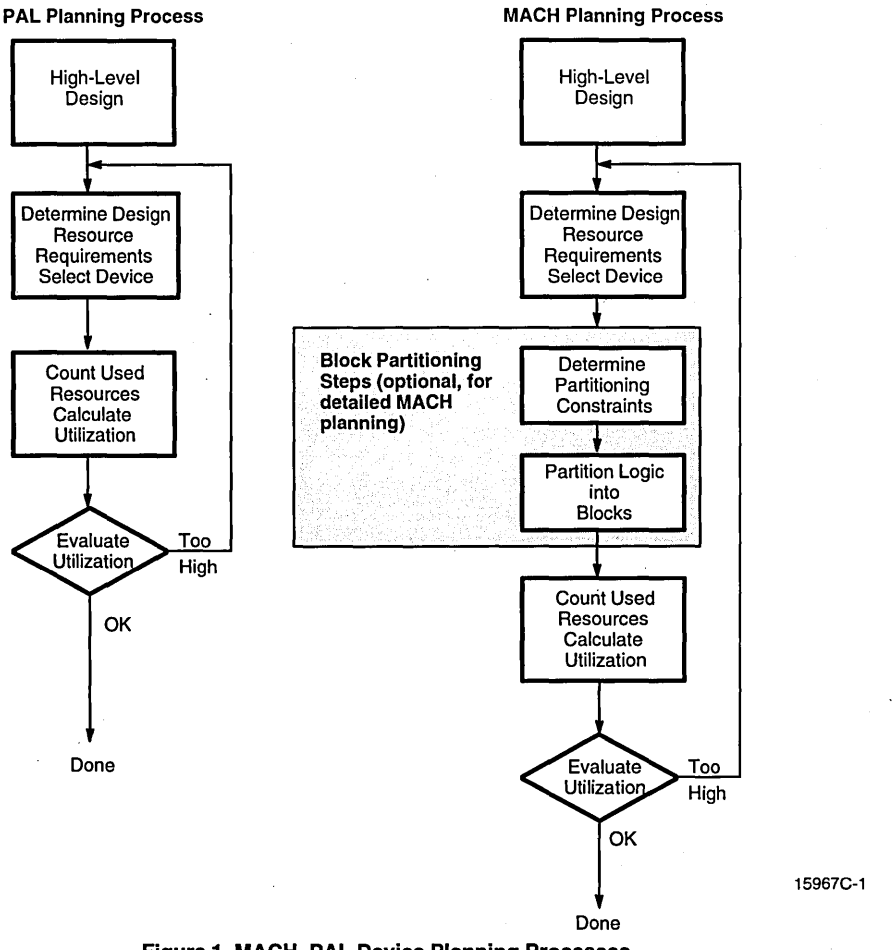


Figure 1. MACH, PAL Device Planning Processes

The counter in this design is implemented using T-type flip-flops rather than D-type because T-type flip-flops require fewer PTs for the hold and count states of each counter bit. Since PTs are required for a T flip-flop only when it changes state, and the most significant bits of a counter do not change during most count states, few PTs are used.

Figure 3 identifies the implementation of each bit in the counter. A T-type flip-flop requires only four PTs: one PT each for counting up and counting down, and two PTs for parallel loading; no PTs are required to hold the macrocell in the same state. In this case, a T-type flip-flop uses less PTs; however, it also reduces the maximum clock frequency of the counter from 76.9 MHz to 71.4 MHz[1].

The count bits are fed back from the counter macrocells via internal feedback and parallel-loaded count values are input via the I/O pins. Each counter macrocell therefore feeds two array inputs simultaneously.

[1] See individual MACH data sheets for all timing specifications.

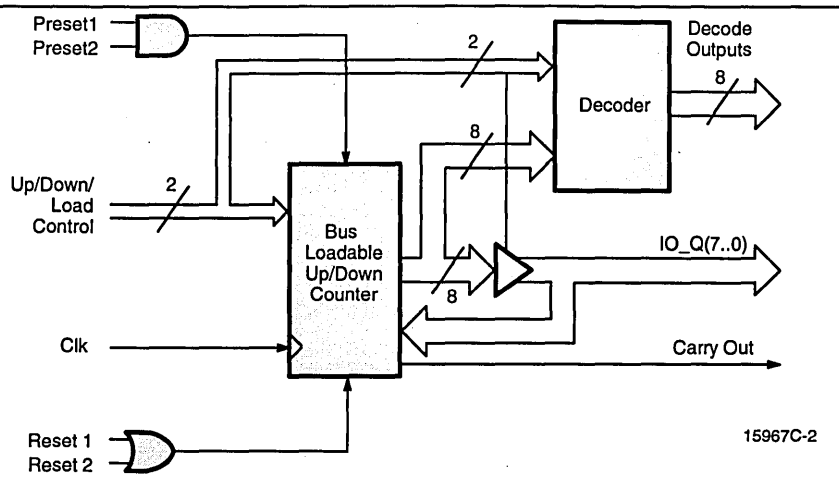


Figure 2. Bus Loadable Up/Down Counter with Decoded Outputs

3.2 Determine Resource Requirements/ Select Device

You must count design resource requirements and match these to an appropriate MACH device. Counting the number of pins, clocks, asynchronous resets and presets, and output enables is a straightforward process. Array input utilization cannot be calculated at this point because the design hasn't been partitioned into blocks.

The group of four PTs associated with each macrocell in a MACH device is called a product-term cluster. One cluster is allocated when from one to four PTs are required by an equation. Each counter bit requires four PTs, or one PT cluster.

Two of the decoded outputs, XORXNOR and Pulse 16, each require more than four PTs. Additional clusters of four product terms each are allocated as needed when the 5th, 9th, etc. PTs are used in an equation. At this point, you must decide whether to estimate the number of PTs used by these equations or reduce the equations to the fewest number of PTs and count them[2]. If you can estimate with a high degree of confidence, the detailed calculation of product terms can be eliminated.

One asynchronous reset PT is available per MACH110 block. In this design, the reset input uses more than one product term and requires an additional product-term cluster, which adds an extra feedback delay to it. The output enable and preset inputs use only one product term; additional product-term clusters are not required.

Resource	Used
Pins	24
PT Clusters	?
Clock	1
Reset	1
Preset	1
Output Enable	1
Array Inputs	?

3.2.1 Product-Term Calculations

When planning your own design, an estimation of product-term requirements may be sufficient. As you use these estimations to analyze device utilization, you should account for the minimization of PTs which will be performed during compilation and may result in fewer PTs than you expected.

Note: *This discussion explains PT estimation in detail. However, counting PT resources in your own designs, for example, in a complicated state-machine design written in high-level syntax, may not prove as straightforward. If counting PTs is difficult, or estimation can be done with a high degree of confidence, you should estimate the number of PT clusters used in your design rather than count them.*

Optional steps to calculate the number of PTs required by the sample XORXNOR and Pulse 16 equations are shown below. The sample XORXNOR equation is discussed first.

```
XORXNOR = (((Q0*Q1*Q2*Q3*Q4*Q5) :+: Q6)
          :*:Q7);
```

[2] Because this is a non-trivial task, it is explained in detail under discussion 3.2.1.

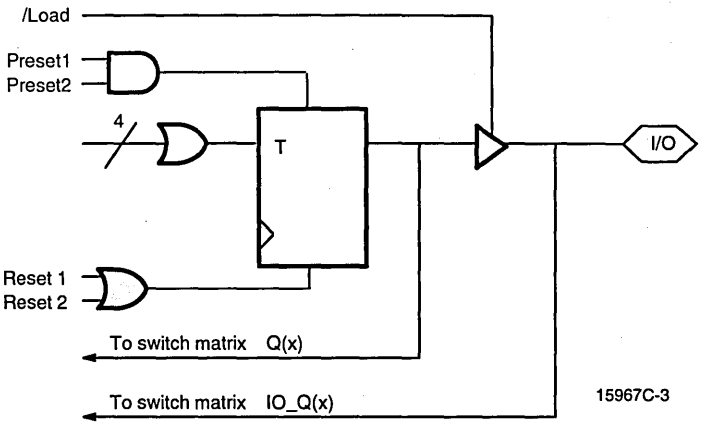


Figure 3. Counter Macrocell

To simplify the equation you set the following, then expand XORXNOR into a sum-of-products form as shown below.

Set

$A = (Q_0*Q_1*Q_2*Q_3*Q_4*Q_5)$

XOR Expansion

$XORXNOR = (A*/Q_6 + /A*Q_6) :*: Q_7$

XORXNOR Expansion

$XORXNOR = (A*/Q_6 + /A*Q_6)*Q_7$
$+ (/A + Q_6)*(A + /Q_6)*/Q_7$

Sum-of-products form

$XORXNOR = A*/Q_6*Q_7$
$+ A*Q_6*/Q_7$
$+ /A*Q_6*Q_7$
$+ /A*/Q_6*/Q_7$

/A requires 6 PTs. Therefore, the two latter equations expand into six product terms each.

Since

$/A = /Q_0 + /Q_1 + /Q_2 + /Q_3 + /Q_4 + /Q_5$

6 PTs are required for each of the following

$/A*Q_6*Q_7$
$/A*/Q_6*/Q_7$

The sample XORXNOR equation requires a total of 14 product terms, or four PT clusters. Clearly, terms using XOR and XNOR operators may require many product terms.

Note: *The XORXNOR equation uses more than 12 product terms. Gate splitting and an extra feedback path are required to implement it in a MACH110 device. The maximum clock speed of the counter is reduced if timing-critical signals route through this feedback path.*

The Pulse 16 equation is shown next. This equation requires five product terms, or two product-term clusters.

$Pulse16 = Q_0*Q_1*Q_2*Q_3*/Q_4*Q_5*Q_6$
$+ Q_0*Q_1*Q_2*Q_3*Q_4*/Q_6$
$+ Q_0*Q_1*Q_2*Q_3*/Q_5*/Q_6$
$+ Q_0*Q_1*Q_2*Q_3*/Q_7$
$+ Q_0*Q_1*Q_2*Q_3*Q_4*/Q_5$

3.2.2 Product-Term Cluster Summary

Following are the product-term cluster requirements for this counter design.

Bus counter Decoded outputs Reset	9 PT clusters 8 + 3 + 1 = 12 PT clusters 1 PT cluster
Total	22 PT clusters used, 69% of the 32 available

3.2.3 Select a Device

A summary of device-resource requirements for this design is shown below. This design will fit in a MACH110 device. The only unknown is the number of array inputs, which will be determined using the block partitioning steps.

Resource	Used	MACH110	Utilization
Pins	24	38	63%
PT Clusters	22	32	69%
Clock	1	2	OK
Reset	1	2	OK
Preset	1	2	OK
Output Enable	1	8	OK
Array Inputs	?	22 per block	?

3.3 Determine Partitioning Constraints (*optional*)

Once the device has been selected, you can determine block partitioning constraints. Reset, preset, and output enable signals constrain block partitioning if you use more of the resource than will fit in 1 block. In this design, however, the single reset, preset, and output enable do not constrain logic to a certain block.

The total number of product terms and array inputs used in this design won't fit into one block. Therefore, these resource requirements constrain the partitioning of logic into blocks. A summary of possible partitioning constraints, and those that impact this design, appear next. Note that MACH2XX devices have 7 possible constraints. Pins are a constraint since the user must differentiate between buried and I/O macrocell resources. Macrocells are also a constraint if input registers are used.

In this design, since array inputs and product term clusters are constraints, they will be considered when partitioning the design. The reset, preset, and output enable resources can be ignored.

3.4 Partition Logic into Blocks (*optional*)

Once partitioning constraints have been determined, the logic can be partitioned into blocks within those constraints so array inputs will be minimized.

To minimize array inputs, equations with similar inputs are placed in the same block. If all equations driven by a signal are in one block, the input signal uses only one array input. An additional array input is needed for each additional block a signal drives.

The block diagram in Figure 2 shows a distinct division of logic between the counter and the output decoder. This helps direct the partitioning process. This design can be partitioned in two ways.

A. Place the counter in one block and the decoder in the other.

B. Divide the counter and decoder into bit slices and place half of each into a single block.

Note that the two presets and the ORed reset are not inputs to the output decoder, so grouping the counter logic in one block uses three fewer array inputs than splitting it into two blocks. Therefore, the first partition will be used.

3.5 Count Resources Used, Calculate Utilization (*optional*)

The constraining resources used in each block (product term clusters and array inputs) are now counted.

3.5.1 Count Resources

Counter-block resources are determined before decoder-block resources because the counter block uses more array inputs than the decoder block (8 extra inputs from counter pins), so the logic is more difficult to place. The following analysis applies to the counter block.

Product-term clusters in counter block

8	$Q_{(7...0)}$
+1	carry out
9	

Array inputs in counter block

8 * 2	$IO\_Q_{(7...0)}$, $Q_{(7...0)}$
3	reset, preset1, preset2
+ 2	control signals
21	

Possible Constraints	Used	# Provided in 1 block	Constraint in Counter? (more than will fit in 1 block)
Product-Term Clusters	24	16	Yes
Asynchronous Resets	1	2	No
Asynchronous Presets	1	2	No
Output Enables	1	at least 2	No
Array Inputs	?	22	Yes
Pins (MACH2XX only)	N/A	N/A	N/A
Macrocells (MACH2XX only)	N/A	N/A	N/A

Note: *If the fitting process cannot place all 21 array inputs into this block, they may be reduced in one of the following ways.*

- *Moving Q[7] to the decoder block reduces array inputs to this block by two. Since it is the counter MSB, it's not used in any other equations within the block. When it's moved to the decoder block, IO_Q[7] and Q[7] drive the decoder block instead of the counter block.*
- *"ANDing" preset1 and preset2 in the decoder block reduces array inputs to this block by one. This will cause the counter block to have only 1 preset input instead of 2.*

Refer to Figure 2 and section 3.2 as you count the product-term clusters and array inputs in the decoder block.

Product-term clusters in decoder block

8	output equations
1	carry out
1	reset
3	extra for XORXNOR
+ 1	extra for pulse 16
14	

Array inputs in decoder block

8	$Q_{(7...0)}$
2	control
2	reset1, reset2
+ 1	XORXNOR gate splitting
13	

Though 14 of the 16 product-term clusters in this block are used, only 13 of the 22 array inputs are used. Placing this logic should pose no problem.

3.5.2 Calculate Total Utilization

At this point, you can calculate total utilization (as listed in the MACH Fitter report file) for the design. This is not a necessary planning step but is shown for clarification and to provide you with an additional planning tool. Total utilization is the average of the following itemized utilizations.

- Pin utilization: defined as the number of pins used divided by the number available.
- Product-term utilization: defined as the number of allocated product-term clusters divided by the number available.
- Array input utilization: defined as the number of array inputs used divided by the total available.

The following utilizations apply to this counter design.

Pin Utilization	24 used, or 63% of the 38 available
Product-term Utilization	(8 + 14) = 22 PT Clusters or 69% of the 32 available
Array Input Utilization	(21 + 13) = 34 or 77% of the 44 available
Total Utilization	(63% + 69% + 77%) / 3 = 70%

4.0 SUMMARY

Overall utilization is only one measure of the likelihood of achieving a successful fit during implementation. Individual resource utilization within blocks must also be taken into account. Partitioning minimizes the total number of array inputs. However, at 21 array inputs, the counter block's switch-matrix utilization in this design is high even after partitioning. This design meets overall device-utilization guidelines and will fit in a MACH111 device or MACH110 device.

Note: *In this brief, a detailed pre-entry analysis of the device resources used in a MACH device design was performed. When estimating whether your own design will fit, you may execute a detailed analysis using the block partitioning steps detailed in this document, or simply estimate the resources used as was done in sections 3.1 and 3.2.*

APPENDIX

A .PDS DESIGN FILE FROM PALASM 4 SOFTWARE: BUSCNTR. PDS

```
TITLE           cntr_reg
REVISION        1
PATTERN         cntr_register
AUTHOR          Arthur Khu, Jerry Vea
COMPANY         AMD
DATE            01/07/1991
CHIP cntr_reg MACH110
; This design is a bus-loadable, up/down counter, with outputs generated from
; the decoded count value and control inputs. The following MACH constructs are
; illustrated in the design: grouping, output pairing, gate splitting,
; registered logic, combinatorial logic, xor operator, xnor operator, tristate
; input, reset input, and preset input. Also, PALASAM 4 software-specific string
; statements and vector notation are used.
;
; The counter counts up, down or is loaded based on the value of the mode bits.
; The outputs CNT7, CNT7REG, PULSE16, DIV16, and XORXNOR are decoded from the
; count bits Q[7..0]. CNT15UP, CNT15DN, and LD0 are decoded from Q[7..0] and
; mode[1..0]. The count bits are fed back at their node to the switch matrix,
; and also output to pins as IO_Q[7..0].

; This design falls within suggested macrocell, product term and switch matrix
; specifications for successful MACH110 fitting. It has been implemented
; and fitted using PALASM 4 and at least one other 3rd party software tool.
;
; Note: suggested fitting options are: expand small - on, max packing -on,
; and expand all - off.

PIN ? CLK               ; Inputs: Counter clock
PIN ? mode[1..0]        ; Inputs: Count up, count down, load control
PIN ? IO_Q[7..0]        ; Outputs: Count value
PIN ? CARRY0            ; Output: Carry look-ahead
PIN ? CNT7              ; Output: Pulses high on count of 7
PIN ? CNT7REG           ; Output: Set high on count of 7
PIN ? CNT15UP           ; Output: Pulses high when counting up to 15
PIN ? CNT15DN           ; Output: Pulses high when counting down to 15
PIN ? PULSE16           ; Output: Pulses high on certain multiples of 16
PIN ? DIV16             ; Output: Divides clock rate by 16
PIN ? LD0               ; Output: Pulses high on load of 0
PIN ? XORXNOR           ; Output: Uses xor, xnor operators
PIN ? RESET1            ; Input: If both resets are high, resets counter
PIN ? RESET2            ; Input: If both resets are high, resets counter
PIN ? PRESET1           ; Input: If both presets are high, presets counter
PIN ? PRESET2           ; Input: If both presets are high, presets counter
NODE ? Q[7..0] PAIR IO_Q[7..0]  ; Nodes: count value feedback
NODE ? RESET            ; Node: asynchronous reset signal

;*****************************************************************************
; Group statements partitioned so design will fit: notice count values in one
; block.
group mach_seg_a IO_Q[7..0]
group mach_seg_b CNT7 CNT7REG CNT15UP CNT15DN LD0 PULSE16 DIV16 XORXNOR
                 RESET

;*****************************************************************************
; String statements improve readability of equations
string CNT_UP '(/mode[1] * /mode[0])'
string CNT_DN '(/mode[1] *  mode[0])'
string LOAD   '( mode[1] * /mode[0])'
string Q3_Q0  '(Q[0] * Q[1] * Q[2] * Q[3])'
;*****************************************************************************
; Counter equations
```

```
EQUATIONS

Q[ 0].T   := CNT_UP +
             CNT_DN +
             LOAD*(Q[ 0] :+: IO_Q[ 0]);

Q[ 1].T   := CNT_UP* Q[0] +
             CNT_DN*/Q[0] +
             LOAD*(Q[ 1] :+: IO_Q[ 1]);

Q[ 2].T   := CNT_UP* Q[0]* Q[1] +
             CNT_DN*/Q[0]*/Q[1] +
             LOAD*(Q[ 2] :+: IO_Q[ 2]);

Q[ 3].T   := CNT_UP* Q[0]* Q[1]* Q[2] +
             CNT_DN*/Q[0]*/Q[1]*/Q[2] +
             LOAD*(Q[ 3] :+: IO_Q[ 3]);

Q[ 4].T   := CNT_UP* Q[0]* Q[1]* Q[2]* Q[3] +
             CNT_DN*/Q[0]*/Q[1]*/Q[2]*/Q[3] +
             LOAD*(Q[ 4] :+: IO_Q[ 4]);

Q[ 5].T   := CNT_UP* Q[0]* Q[1]* Q[2]* Q[3]* Q[4] +
             CNT_DN*/Q[0]*/Q[1]*/Q[2]*/Q[3]*/Q[4] +
             LOAD*(Q[ 5] :+: IO_Q[ 5]);

Q[ 6].T   := CNT_UP* Q[0]* Q[1]* Q[2]* Q[3]* Q[4]* Q[5] +
             CNT_DN*/Q[0]*/Q[1]*/Q[2]*/Q[3]*/Q[4]*/Q[5] +
             LOAD*(Q[ 6] :+: IO_Q[ 6]);

Q[ 7].T   := CNT_UP* Q[0]* Q[1]* Q[2]* Q[3]* Q[4]* Q[5]* Q[6] +
             CNT_DN*/Q[0]*/Q[1]*/Q[2]*/Q[3]*/Q[4]*/Q[5]*/Q[6] +
             LOAD*(Q[ 7] :+: IO_Q[ 7]);

CARRY0  := CNT_UP*
            /Q[ 0]* Q[ 1]* Q[ 2]* Q[ 3]* Q[ 4]* Q[ 5]* Q[ 6]* Q[ 7] +
             CNT_DN*
             Q[ 0]*/Q[ 1]*/Q[ 2]*/Q[ 3]*/Q[ 4]*/Q[ 5]*/Q[ 6]*/Q[ 7];
;*************************************************************************
; DECODED OUTPUTS
CNT7 =       Q[ 0]* Q[ 1]* Q[ 2]* /Q[ 3]* /Q[ 4]* /Q[ 5]* /Q[ 6]* /Q[ 7];

CNT7REG :=  Q[ 0]* Q[ 1]* Q[ 2]* /Q[ 3]* /Q[ 4]* /Q[ 5]* /Q[ 6]* /Q[ 7];

CNT15UP =   Q[ 0]* Q[ 1]* Q[ 2]* Q[ 3]* /Q[ 4]* /Q[ 5]* /Q[ 6]* /Q[ 7] *
             CNT_UP;

CNT15DN =   Q[ 0]* Q[ 1]* Q[ 2]* Q[ 3]* /Q[ 4]* /Q[ 5]* /Q[ 6]* /Q[ 7] *
             CNT_DN;

PULSE16 =    Q3_Q0 * /Q[ 4]* Q[ 5]* Q[ 6] +
             Q3_Q0 * Q[ 4]* /Q[ 6] +
             Q3_Q0 * /Q[ 5]* /Q[ 6] +
             Q3_Q0 *  /Q[ 7] +
             Q3_Q0 * Q[ 4]* /Q[ 5];

DIV16 =      Q[3];

XORXNOR =        (((Q[0] * Q[ 1] *  Q[ 2] *  Q[ 3] * Q[ 4] *
            Q[ 5]):+: Q[ 6]):*: Q[ 7]);

LD0 =        /Q[ 0]* /Q[ 1]* /Q[ 2]* /Q[ 3]* /Q[ 4]* /Q[ 5]* /Q[ 6]* /Q[ 7] *
             LOAD;

RESET = RESET1 + RESET2;
;*************************************************************************
; Count output assignments
IO_Q[ 0].T := {Q[ 0].T};
IO_Q[ 1].T := {Q[ 1].T};
IO_Q[ 2].T := {Q[ 2].T};
IO_Q[ 3].T := {Q[ 3].T};
IO_Q[ 4].T := {Q[ 4].T};
IO_Q[ 5].T := {Q[ 5].T};
```

```
IO_Q[ 6].T := {Q[ 6].T};

IO_Q[ 7].T := {Q[ 7].T};
;*************************************************************************
; Reset, preset, and tristate equations

IO_Q[7..0].trst = CNT_UP + CNT_DN;
Q[7..0].RSTF = RESET;
CNT7REG.RSTF = GND;
CARRY0.RSTF  = GND;
Q[7..0].SETF = PRESET1 * PRESET2;
CNT7REG.SETF = GND;
CARRY0.SETF  = GND;
Q[7..0].CLKF = CLK;
CARRY0.CLKF  = CLK;
CNT7REG.CLKF = CLK;
```

APPENDIX

B PALASM 4 MACH FITTER REPORT BUSCNTR.RPT

```
PALASM 4.1 MACH FITR - MARKET RELEASE (1-24-91)
 (C) - COPYRIGHT ADVANCED MICRO DEVICES INC., 1990
Reading User Design (TRE File)...
Flags Used:              Unplace=False        Max Packing=True
Flags Used:        Expand Small=True           Expand All=False
Reading Device Database ...
*************************************************
     MACH PLD Fitter - v 1.46          cntr_reg
*************************************************
PAIR Analysis...
Pre-Placement & Equation Usage Checks...

*** Timing Analysis for Signals
 Parameter    Min    Max          Signal List (Those having Max delay.)
      Tpd      1      1          CNT15UP          CNT15DN              LD0
      Tsu      1      2          IO_Q[7]          IO_Q[6]          IO_Q[5]
                                 IO_Q[4]          IO_Q[3]          IO_Q[2]
                                 IO_Q[1]          IO_Q[0]
      Tco      0      0          IO_Q[7]          IO_Q[6]          IO_Q[5]
                                 IO_Q[4]          IO_Q[3]          IO_Q[2]
                                 IO_Q[1]          CNT7REG

 Key:
 Tpd - Combinatorial propagation delay, input to output
 Tsu - Combinatorial setup delay before clock
 Tco - Register clock to combinatorial output
 Tcr - Register thru combinatorial logic to setup
 All delay values are expressed in terms of array passes

*** Device Resource Checks
               Available        Used        Remaining
        Clocks:     2             1             1
          Pins:    38            24            14      ->    63%
     I/O Macro:    32            17            15
   Total Macro:    32            19            13
 Product Terms:   128            61            40      ->    68%

MACH-PLD Resource Checks OK!


Partitioning Design into Blocks...

*** Last Equations Placed in Blocks

Weakly -

*** Block Partitioning Results
              Array    Macros     # I/O    Buried   Product    Signal
             Inputs    Remain     Macro     Logic    Terms     Fanout
   Block-> A    21         8         8         0       32        24
   Block-> B    13         5         9         2       56         2

*** Block Signal List
Block-> A          Q[0]          IO_Q[0]           Q[1]          IO_Q[1]
                   Q[2]          IO_Q[2]           Q[3]          IO_Q[3]
                   Q[4]          IO_Q[4]           Q[5]          IO_Q[5]
                   Q[6]          IO_Q[6]           Q[7]          IO_Q[7]
Block-> B         _NODE0          CARRY0          RESET          XORXNOR
                    LD0            DIV16         PULSE16         CNT15DN
                 CNT15UP         CNT7REG            CNT7

|> INFORMATION F050 - Device Utilization..... *: 68 %
```

```
Assigning Resources...

*** Macro Block A

   I/O Macros>          IO_Q[1]          IO_Q[2]          IO_Q[3]          IO_Q[4]
      Targets>   0( 2)   6( 8)   9(15)  12(18)
        IO_Q[1] (A  0) -> (A  3) (A  0) (B  0)
        IO_Q[2] (A  6) -> (A  5) (A  6) (B  6)
        IO_Q[3] (A  9) -> (A 10) (A  9) (B  9)
        IO_Q[4] (A 12) -> (A 15) (A 12) (B 12)

 I/O Macros>          IO_Q[5]          IO_Q[6]          IO_Q[7]
      Targets>   1( 3)   7( 9)  13(19)
        IO_Q[5] (A  1) -> (A  2) (A  1) (B  1)
        IO_Q[6] (A  7) -> (A  4) (A  7) (B  7)
        IO_Q[7] (A 13) -> (A 14) (A 13) (B 13)

I/O Macros>          IO_Q[0]
      Targets>   2( 4)  10(16)  14(20)
        IO_Q[0] (A  2) -> (A 18) (A 21) (B  2)

*** Macro Block Inputs

       Inputs>          MODE[0]          MODE[1]          PRESET1          PRESET2
RESET1
      Targets>   0(10)   1(11)   2(13)   3(32)   4(33)
        MODE[0] (I  0) -> (A 16) (B 16)
        MODE[1] (I  1) -> (A 17) (B 17)
        PRESET1 (I  2) -> (A 19)
        PRESET2 (I  3) -> (A 20)
         RESET1 (I  4) -> (B 21)

*** Macro Block B

   I/O Macros>          PULSE16
      Targets>   0(24)   2(26)   4(28)   6(30)   8(36)  10(38)  12(40)  14(42)


        PULSE16 (B  0)

  I/O Macros>            CNT7             LD0          CNT15DN          XORXNOR
DIV16          CNT15UP
      Targets>   1(25)   4(28)   6(30)   8(36)  10(38)  12(40)  14(42)
            CNT7 (B  1)              LD0 (B  4)           CNT15DN (B  6)
          XORXNOR (B  8)            DIV16 (B 10)           CNT15UP (B 12)

 Buried Logic>           _NODE0
      Targets>  14(42)
         _NODE0 (B 14) -> (B 14)

  I/O Macros>          CNT7REG          CARRY0
      Targets>   2(26)   5(29)   7(31)   9(37)  11(39)

 CNT7REG (B  2)           CARRY0 (B  5)

 Buried Logic>           RESET
      Targets>   7(31)   9(37)  11(39)

 * Retry Mapping
          RESET (B 11) -> (A 11)

       Inputs>          RESET2
      Targets>   3( 5)   4( 6)   5( 7)   8(14)  10(16)  11(17)  14(20)  15(21)


     * Retry Mapping
     * Retry Mapping
     * Retry Mapping

 RESET2 (A 11) -> (B  8)

*** Signals - Tabular Information
```

Signal	#	P/N #	(Loc)	Type	Logic	# PT	Blocks
CLK	1	35	I 5	clock pin	.		
MODE[1]	2	11	I 1	input	.		AB
MODE[0]	3	10	I 0	input	.		AB
IO_Q[7]	4	19	A 13	i/o pin	t-ff	4	A
IO_Q[6]	5	9	A 7	i/o pin	t-ff	4	A
IO_Q[5]	6	3	A 1	i/o pin	t-ff	4	A
IO_Q[4]	7	18	A 12	i/o pin	t-ff	4	A
IO_Q[3]	8	15	A 9	i/o pin	t-ff	4	A
IO_Q[2]	9	8	A 6	i/o pin	t-ff	4	A
IO_Q[1]	10	2	A 0	i/o pin	t-ff	4	A
IO_Q[0]	11	4	A 2	i/o pin	t-ff	3	A
CARRY0	12	29	B 5	i/o pin	d-ff	2	
CNT7	13	25	B 1	i/o pin	comb	1	
CNT7REG	14	26	B 2	i/o pin	d-ff	1	
CNT15UP	15	40	B 12	i/o pin	comb	1	
CNT15DN	16	30	B 6	i/o pin	comb	1	
PULSE16	17	24	B 0	i/o pin	comb	5	
DIV16	18	38	B 10	i/o pin	comb	1	
LD0	19	28	B 4	i/o pin	comb	1	
XORXNOR	20	36	B 8	i/o pin	comb	3	
RESET1	21	33	I 4	input	.		B
RESET2	22	17	A 11	input	.		B
PRESET1	23	13	I 2	input	.		A
PRESET2	24	32	I 3	input	.		A
Q[7]	25	15	A 13	out pair	t-ff	4	AB
Q[6]	26	9	A 7	out pair	t-ff	4	AB
Q[5]	27	3	A 1	out pair	t-ff	4	AB
Q[4]	28	14	A 12	out pair	t-ff	4	AB
Q[3]	29	11	A 9	out pair	t-ff	4	AB
Q[2]	30	8	A 6	out pair	t-ff	4	AB
Q[1]	31	2	A 0	out pair	t-ff	4	AB
Q[0]	32	4	A 2	out pair	t-ff	3	AB
RESET	33	29	B 11	buried	comb	2	A
_NODE0	34	32	B 14	buried	comb	12	B

Key:
P/N # - Pin/Node Number
.?. - Signal Unplaced
(Loc) - Macrocell Location (Block & Cell)
PT - Number of used product terms in logic
Blocks- Device blocks driven by signal
comb - Combinatorial logic function
d-ff - D-Type Flip-flop
t-ff - T-Type Flip-flop

*** Signals - Equations Where Used

Signal Source	Fanout List			
CLK				
MODE[1]:	IO_Q[7]	IO_Q[6]	IO_Q[5]	IO_Q[4]
:	IO_Q[3]	IO_Q[2]	IO_Q[1]	IO_Q[0]
:	CARRY0	CNT15UP	CNT15DN	LD0
:	Q[7]	Q[6]	Q[5]	Q[4]
:	Q[3]	Q[2]	Q[1]	Q[0]
{AAAA AAAA BBBB AAAA AAAA}				
MODE[0]:	IO_Q[7]	IO_Q[6]	IO_Q[5]	IO_Q[4]
:	IO_Q[3]	IO_Q[2]	IO_Q[1]	IO_Q[0]
:	CARRY0	CNT15UP	CNT15DN	LD0
:	Q[7]	Q[6]	Q[5]	Q[4]
:	Q[3]	Q[2]	Q[1]	Q[0]
{AAAA AAAA BBBB AAAA AAAA}				
IO_Q[7]:	IO_Q[7]	Q[7]		
{AA}				
IO_Q[6]:	IO_Q[6]	Q[6]		
{AA}				
IO_Q[5]:	IO_Q[5]	Q[5]		
{AA}				
IO_Q[4]:	IO_Q[4]	Q[4]		
{AA}				
IO_Q[3]:	IO_Q[3]	Q[3]		
{AA}				

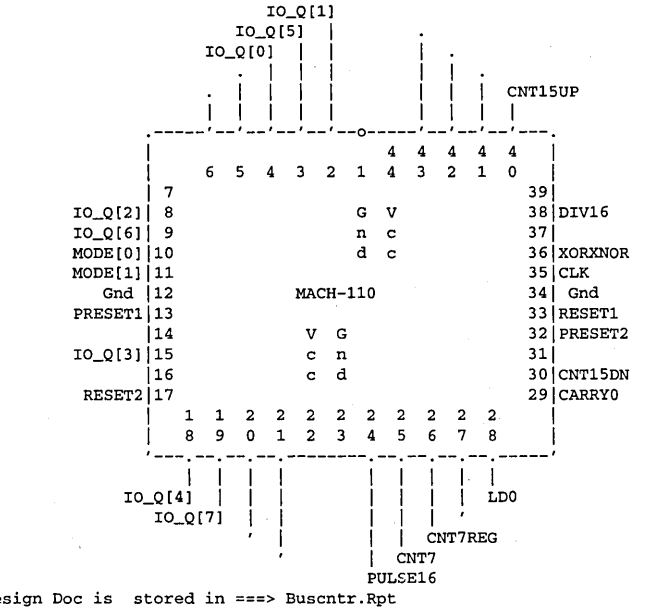
```
IO_Q[2]:        IO_Q[2]             Q[2]
       {AA}
IO_Q[1]:        IO_Q[1]             Q[1]
       {AA}
IO_Q[0]:        IO_Q[0]             Q[0]
       {AA}
 RESET1:          RESET
       {B}
 RESET2:          RESET
       {B}
PRESET1:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]         IO_Q[1]         IO_Q[0]
       :           Q[7]            Q[6]            Q[5]            Q[4]
       :           Q[3]            Q[2]            Q[1]            Q[0]
       {AAAA AAAA AAAA AAAA}
PRESET2:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]         IO_Q[1]         IO_Q[0]
       :           Q[7]            Q[6]            Q[5]            Q[4]
       :           Q[3]            Q[2]            Q[1]            Q[0]
       {AAAA AAAA AAAA AAAA}
   Q[7]:        IO_Q[7]          CARRY0           CNT7         CNT7REG
       :        CNT15UP         CNT15DN         PULSE16             LD0
       :        XORXNOR            Q[7]          _NODE0
       {ABBB BBBB BAB}
   Q[6]:        IO_Q[7]         IO_Q[6]          CARRY0           CNT7
       :        CNT7REG         CNT15UP         CNT15DN         PULSE16
       :            LD0         XORXNOR            Q[7]            Q[6]
       :         _NODE0
       {AABB BBBB BBAA B}
   Q[5]:        IO_Q[7]         IO_Q[6]         IO_Q[5]          CARRY0
       :           CNT7         CNT7REG         CNT15UP         CNT15DN
       :        PULSE16             LD0         XORXNOR            Q[7]
       :           Q[6]            Q[5]          _NODE0
       {AAAB BBBB BBBA AAB}
   Q[4]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :         CARRY0           CNT7         CNT7REG         CNT15UP
       :        CNT15DN         PULSE16             LD0         XORXNOR
       :           Q[7]            Q[6]            Q[5]            Q[4]
       :         _NODE0
       {AAAA BBBB BBBB AAAA B}
   Q[3]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]          CARRY0           CNT7         CNT7REG
       :        CNT15UP         CNT15DN         PULSE16           DIV16
       :            LD0         XORXNOR            Q[7]            Q[6]
       :           Q[5]            Q[4]            Q[3]          _NODE0
       {AAAA ABBB BBBB BBAA AAAB}
   Q[2]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]          CARRY0           CNT7
       :        CNT7REG         CNT15UP         CNT15DN         PULSE16
       :            LD0         XORXNOR            Q[7]            Q[6]
       :           Q[5]            Q[4]            Q[3]            Q[2]
       :         _NODE0
       {AAAA AABB BBBB BBAA AAAA B}
   Q[1]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]         IO_Q[1]          CARRY0
       :           CNT7         CNT7REG         CNT15UP         CNT15DN
       :        PULSE16             LD0         XORXNOR            Q[7]
       :           Q[6]            Q[5]            Q[4]            Q[3]
       :           Q[2]            Q[1]          _NODE0
       {AAAA AAAB BBBB BBBA AAAA AAB}
   Q[0]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]         IO_Q[1]         IO_Q[0]
       :         CARRY0           CNT7         CNT7REG         CNT15UP
       :        CNT15DN         PULSE16             LD0         XORXNOR
       :           Q[7]            Q[6]            Q[5]            Q[4]
       :           Q[3]            Q[2]            Q[1]            Q[0]
       :         _NODE0
       {AAAA AAAA BBBB BBBB AAAA AAAA B}
 RESET:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]         IO_Q[1]         IO_Q[0]
       :           Q[7]            Q[6]            Q[5]            Q[4]
       :           Q[3]            Q[2]            Q[1]            Q[0]
       {AAAA AAAA AAAA AAAA}
```

```
          _NODE0:        XORXNOR
               (B)

*** Outputs with no feedback

          CARRY0          CNT7        CNT7REG        CNT15UP        CNT15DN
         PULSE16         DIV16            LD0        XORXNOR

*** Feedback Map - cntr_reg
 Gbl Inp .--.     I/O  .--+--A--+--.  I/O          I/O  .--+--B--+--.  I/O
         | 0|     Q[1] : 0|     |21| Q[0]         Q[1] : 0|     |21| RESET1
         | 1|     Q[5] : 1|     |20| PRESET2      Q[5] : 1|     |20|
         | 2|  IO_Q[5] : 2|     |19| PRESET1      Q[0] : 2|     |19|
         | 3|  IO_Q[1] : 3|     |18| IO_Q[0]           | 3|     |18|
         | 4|  IO_Q[6] : 4|     |17| MODE[1]          | 4|     |17| MODE[1]
         | 5|  IO_Q[2] : 5|     |16| MODE[0]          | 5|     |16| MODE[0]
         '--'     Q[2] : 6|     |15: IO_Q[4]       Q[2] : 6|     |15|
                  Q[6] : 7|     |14: IO_Q[7]       Q[6] : 7|     |14: _NODE0
                       | 8|     |13: Q[7]        RESET2 : 8|     |13: Q[7]
                  Q[3] : 9|     |12: Q[4]          Q[3] : 9|     |12: Q[4]
                IO_Q[3] :10|     |11: RESET              |10|     |11|
                        '--+-u--u+--'                    '--+-u--u+--'
*** Logic Map - cntr_reg
 Gbl Inp .--.     I/O  .--+--A--+--.  I/O          I/O  .--+--B--+--.  I/O
  MODE[0]| 0|  IO_Q[1] | 0| 4   |21|              PULSE16 | 0| 5   |21|
  MODE[1]| 1|  IO_Q[5] | 1| 4   |20|                CNT7 | 1| 1   |20|
  PRESET1| 2|  IO_Q[0] | 2| 3   |19|             CNT7REG | 2| 1   |19|
  PRESET2| 3|          | 3| .   |18|                     | 3| *   |18|
   RESET1| 4|          | 4| .   |17|                 LD0 | 4| 1   |17|
     CLK| 5|          | 5| .   |16|              CARRY0 | 5| 2   |16|
        '--'  IO_Q[2] | 6| 4  .|15|              CNT15DN | 6| 1  *|15|
              IO_Q[6] | 7| 4  .|14|                     | 7| . 12|14| _NODE0
                      | 8| .  4|13| Q[7][7]     XORXNOR | 8| 3  *|13|
              IO_Q[3] | 9| 4  4|12| Q[4][4]             | 9| .  1|12| CNT15UP
                      |10| .  .|11|               DIV16 |10| 1  2|11| RESET
                      '--+-u--u+--'                    '--+-u--u+--'
*** Pin Map - cntr_reg
```




```
The Design Doc is  stored in ===> Buscntr.Rpt
The Jedec Data is  stored in ===> Buscntr.Jed
The Placements are stored in ===> Buscntr.Plc

%% FITR %% Error Count: 0, Warning Count: 0
%% FITR %% File Processed Successfully. - File: Buscntr
```

The Evolution of Bus-Friendly Inputs and I/O

Application Note
by Eddie Aparicio

Advanced Micro Devices

OVERVIEW

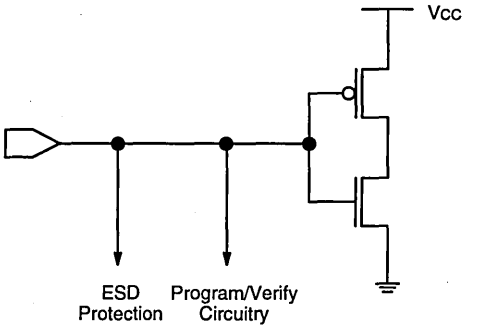
The purpose of this document is to inform the reader about certain changes that have occurred within some of AMD's CMOS PLDs. The document serves as an informative, historical account with descriptions and figures of all the types of inputs and I/O configurations implemented over the last decade. In addition, the document states reasons for the changes and should give designers a better understanding of AMD's CMOS PLDs.

INTRODUCTION

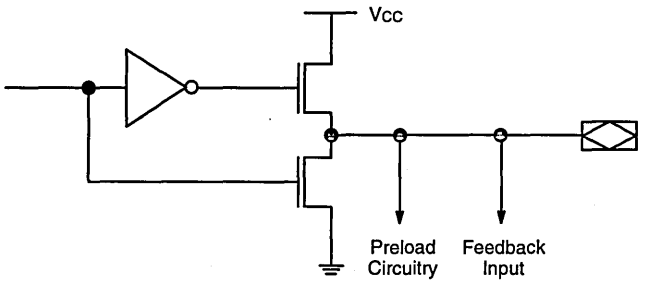
AMD's CMOS PLDs have evolved throughout time. Like Darwin's theory of evolution and adaptation, AMD's CMOS PLDs have evolved and adapted to the dynamic world of digital logic. When AMD's CMOS PLDs were first introduced to the market in the mid 1980s, they had different characteristics than the PLDs presently in existence. The older devices were larger in size, slower in speed, and hungrier for power than their contemporary counterparts. As the computer industry evolved to accommodate applications requiring faster, smaller, and lower power devices, PLDs were modified in order to accommodate these changes and stay competitive in the PLD market arena.

DEVICES WITH UNBIASED INPUTS AND I/O

Originally, AMD introduced CMOS PLDs with unbiased inputs and I/O which is basically a carry over of the bipolar configuration. The circuit configuration is shown in Figure 1 and consists of a buffer that is directly connected to the pin pad.



Typical Input



Typical I/O

19671A-1

Figure 1. Equivalent Schematic of the Unbiased Input and I/O Scheme

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If the pin is left unconnected, this configuration is termed "floating" because an unused input pin is allowed to float to any state, since there is no circuitry that would bias the pin to a known state. The consequence in leaving the pin floating is that excessive noise or having a voltage near the threshold voltage of the PLD could influence the PLD to produce an unwanted oscillatory output that could disturb the system. In addition, the noise on V_{CC} will also increase due to this oscillation. Figure 2 shows the event of device oscillation due to a noisy input signal through an unused input pin.

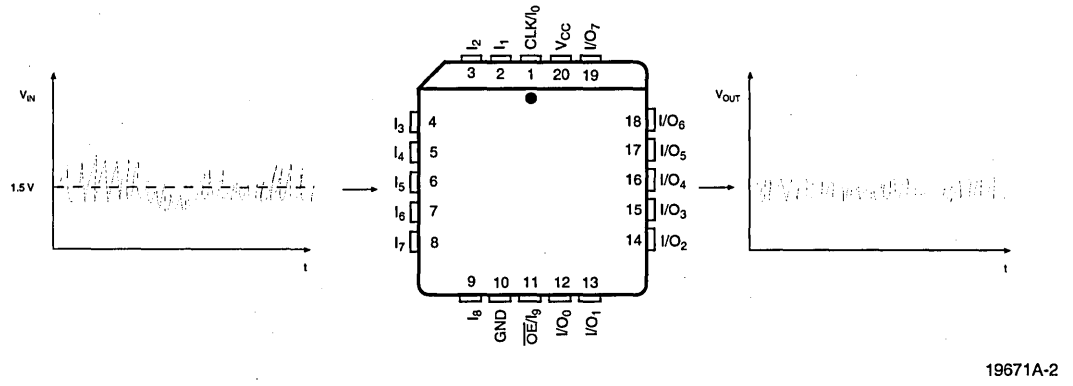
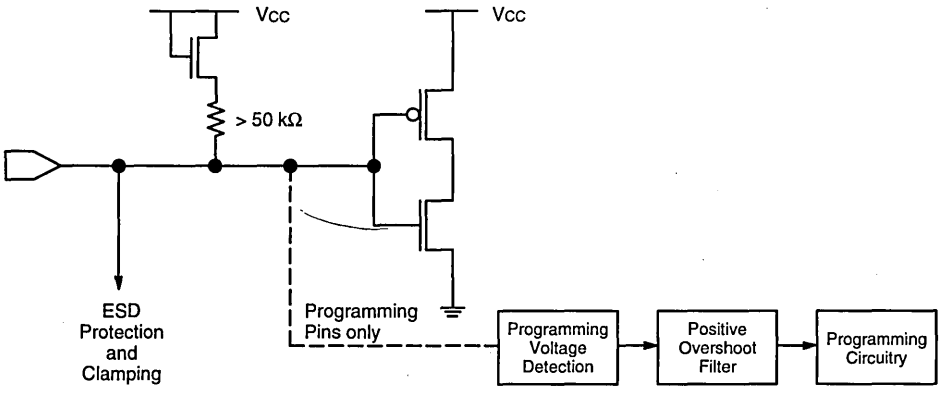


Figure 2. Output Oscillation Due to Noisy Input of an Unbiased "Floating" Input Pin

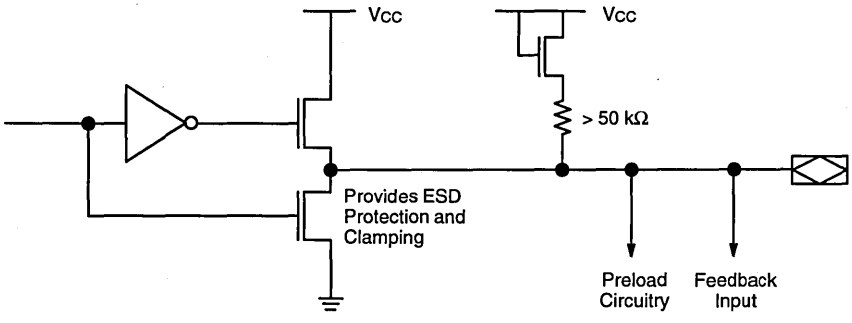
Even though it is recommended to tie unused input pins to ground or V_{CC}, traces must be cut on a printed circuit board in order to free the tied pins when changes are made. Unfortunately, this poses an inconvenience to the customer. As a result, AMD decided it was best to modify the input and I/O circuitry of all PAL devices.

PULL-UP RESISTOR ENHANCEMENT

The improvement was to add a pull-up resistor to the input and I/Os so that if the pin was left floating, the device could pull its pin voltage to a known voltage state. Figure 3 shows the circuit configuration of the pull-up resistor scheme.



Typical Input



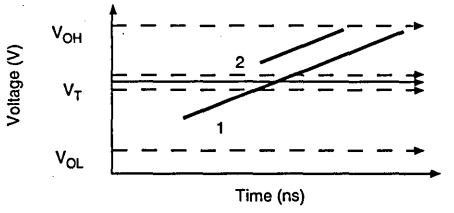
Typical I/O

19671A-3

Figure 3. Equivalent Schematic of Pull-up Resistor Scheme

This scheme consists of a 50 kΩ resistor that is connected to a constant current source, which is used to hold down any excessive current in the event that the 50 kΩ resistor is disabled. The pull-up resistor scheme pulls the voltage of the pin to about 3.5 V–4.0 V. The 50 kΩ resistor value is used because this value provides a voltage that is easy enough for another driver to overcome when necessary because of the current limiting effect of the large resistance.

Even though the pin is pulled to a known state, the pull-up scheme can potentially introduce oscillation to a system if the voltage of a tri-state bus is left below the threshold voltage of the PLD. The reason for the potential problem is due to the nature of the pull-up resistor within the PLD. The internal pull-up resistor is only capable of pulling from a low to a high voltage state. In addition, the slew rate is slow due to the 50 kΩ current-limiting resistor. Thus, when a pin voltage is left below the threshold voltage of the PLD, the pull-up resistor has no other choice but to pull the pin voltage slowly through the threshold voltage region of the PLD. On the contrary, if the voltage of the tri-state bus is at a voltage state higher than the threshold voltage of the PLD, then the PLD will not exhibit oscillation. Note that if some other device overpowers the weak pull-up resistor of the PLD causing the tri-state bus voltage to reside around the threshold voltage of the PLD, then device oscillation is also possible. Both the high and low tri-state bus scenarios are shown in slew rate curves in Figure 4.



Bus Scenario

1 = Tri-State Bus left low with Pull-up scheme
2 = Tri-State Bus left high with Pull-up scheme

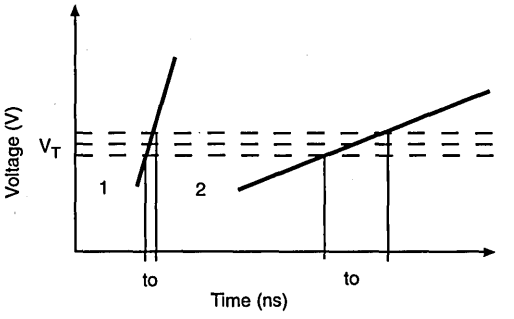
19671A-4

Figure 4. Slew Rate Comparison of Pull-up Scheme Showing Bus Scenarios

DEVICE OSCILLATION

The reason a device oscillates is due to the nature of the threshold voltage of the transistors within the input and I/O buffers of the PLD. Typically, the threshold voltage of an input buffer is 1.5 V. When a pin voltage is around the threshold voltage, the complementary transistor pair does not know whether to switch high or low, thus oscillation is possible at the output. Usually, this fickle nature lasts no more than a few nanoseconds, however, for faster systems this can be significant.

When a large pull-up resistor is used such as those used in the PLD industry, the slow slew rate allows the voltage to reside in the threshold region longer than if a smaller pull-up resistor is used. For comparison, Figure 5 shows the difference in the time of oscillation between a 50 kΩ resistor and a 1 kΩ resistor through slew rate curves.



1 = Slew rate of 1 kΩ pull-up resistor
2 = Slew rate of 50 kΩ pull-up resistor
to = Time of potential oscillation

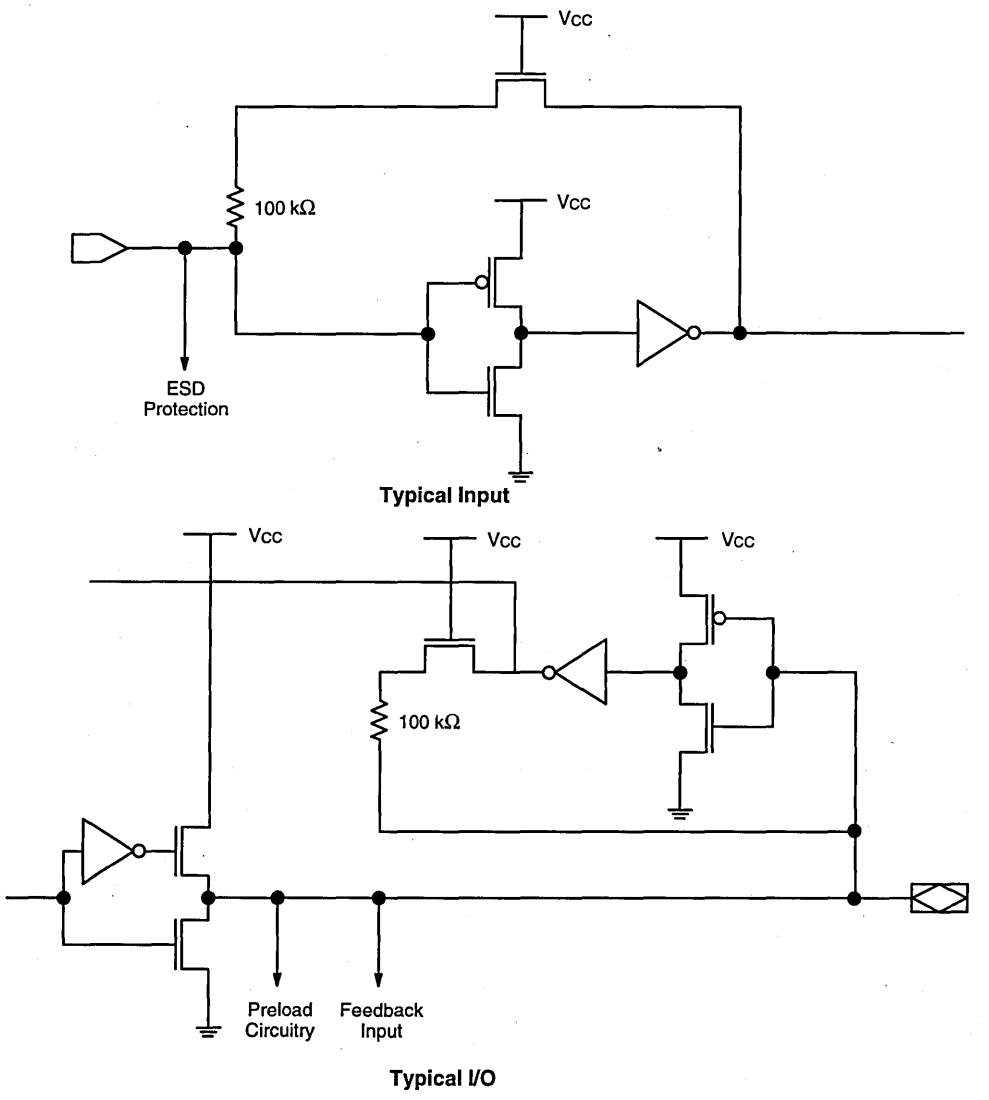
19671A-5

Figure 5. Slew Rate Comparison Between a 1 kΩ and 50 kΩ Pull-up Resistor

Because the possibility of device oscillation could occur with the pull-up resistor scheme, another scheme had to be implemented.

BUS-FRIENDLY INPUT AND I/O

Bus-Friendly inputs and I/O have the ability to hold the input buffer at either a high or a low depending on the last state of the pin connected to the bus. The scheme is termed "Bus-Friendly" because it allows the bus connected to the PLD to be left at any state (other than the 1.5 V threshold voltage of the input and I/O buffers). For PAL devices, the Bus-Friendly scheme is accomplished by reconfiguring already existing resources of the pull-up scheme as shown in Figure 6.



19671A-6

Figure 6. Equivalent Schematic of the Bus-Friendly Input and I/O for PAL Devices

While in the MACH® products, the scheme is configured slightly different by having a separate circuit performing the "latch" characteristic as shown in Figure 7.

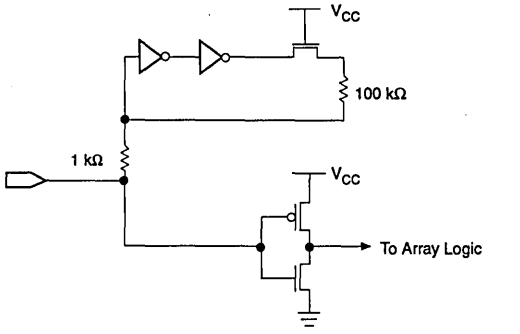


Figure 7. Equivalent Schematic of the Bus-Friendly Input and I/O for MACH CPLDs

The Bus-Friendly circuitry pulls the voltage at the input buffer to a TTL voltage high or low. This input and I/O scheme is accomplished by a double inverter input buffer which loops back to the input of the PLD through a 100 kΩ resistor. This configuration acts as a "latch" because it holds the pin voltage of the PLD at either a TTL level high or low until the pin voltage of the PLD changes state. Bus-Friendly circuitry weakly holds the voltage so that another driver on the bus can overcome the voltage when necessary. Please note that the default state of the pin is no longer a voltage high but is rather dependent on the last driven state of the pin. Designers who need to have the pull-up feature will need to provide an external pull-up resistor rather than depend on the pull-up resistor of the PLD.

The Bus-Friendly scheme provides a solution to the instance where the pull-up scheme could potentially cause input buffer oscillation. As illustrated earlier in Figure 4, the pull-up scheme cannot resolve the case when the tri-state bus connected to the PLD is left at a voltage below the threshold voltage of the PLD. This type of bus scenario promotes undesirable device oscillation. The Bus-Friendly idea is an improvement over the pull-up resistor scheme because the Bus-Friendly circuitry does not allow the voltage to cross the threshold region of the PLD, thus avoiding the possibility of device oscillation. Figure 8 shows how the Bus-Friendly PLDs deal with same bus scenarios that the pull-up resistor scheme did in Figure 4.

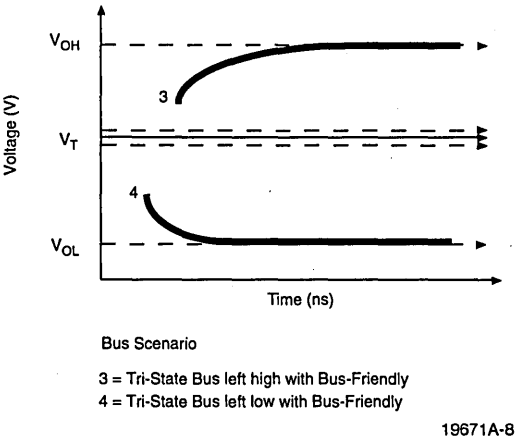


Figure 8. Slew Rate Comparison of Bus-Friendly Scheme Showing Bus Scenarios

Note that if another driver on the bus is forcing the tri-state bus to reside in the threshold voltage region of the PAL, then no matter what type of input and I/O scheme is used, the PAL device can oscillate for a few nanoseconds.

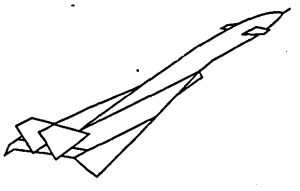
The Bus-Friendly enhancement does not affect the existing DC and AC specifications for both the MACH and PAL products which previously had the pull-up resistor enhancement. Bus-Friendly was intended to remedy device oscillation without changing any of the device's specifications. This enhancement will be implemented on all new PAL and MACH designs in the future.

SUMMARY

Just as the computer industry has evolved, so have AMD's PLDs. The input and I/O circuitry of AMD PLDs have changed to accommodate the different applications that have emerged due to the evolution of the computer industry. The circuitry has evolved from unbiased to pull-up to Bus-Friendly inputs and I/O. The unbiased inputs and I/Os have disadvantages due to the nature of the floating input. When left unconnected, unbiased inputs and I/O "float" and are susceptible to the influence of noise, which can cause the PLD to oscillate. Because of this oscillation, the pull-up resistor became the next link in the PLD input and I/O evolution chain.

The pull-up resistor can bias an unconnected pin to a high voltage state. However, the one-dimensional nature of the large pull-up resistor could not avoid device oscillation in particular situations. As board designs required the tri-state bus to be left low, the current-limiting, internal pull-up resistor would slowly pull the voltage of the pin through the threshold region of the PAL, thus causing device oscillation. Because this situation can potentially occur in different instances other than the low voltage, tri-state bus scenario, it was clear that a new pin bias scheme should be implemented.

Bus-Friendly inputs and I/O have the ability to hold the last voltage state of the tri-state bus at a discrete TTL voltage level. The advantage of this scheme is that a tri-state bus can be at either a high or a low voltage state without having the PLD oscillate. It is because of this feature the name "Bus-Friendly" was used to describe this pin bias scheme.



PCI Bus Interface Using AMD PLDs

Application Note
by Eddie Aparicio and Peter Trott

Advanced Micro Devices

BACKGROUND

A personal computer system bus is the medium where data is transferred between the microprocessor and its peripherals such as disk drives, monitors, and printers. Since software has become more demanding, the traditional bus system has run into a performance wall. Traditional bus systems were designed to support a 16-bit microprocessor, and operate at speeds of only 8.33 MHz. Since the computer industry is moving towards higher resolution graphics which requires higher data widths and higher clock speeds (25–33 MHz), an information bottleneck effect, due to data traffic, has developed on the traditional bus system "highway." This bottleneck effect is attributed to the performance limitations of traditional bus system architectures, which has caused the CPU to wait for the slower peripheral components residing on the 8-bit or 16-bit expansion bus slot. As the computer industry moves towards applications requiring even more performance, such as multimedia, the need for an alternate bus system architecture is apparent.

A standard local bus architecture appears to be the savior for applications requiring high performance. Local bus architecture allows peripherals to be directly connected to the CPU bus, thus access to the faster clock of the CPU. The CPU has shorter wait cycles because its peripherals operate at the same rate as the 33 MHz system clock. Local bus also offers the advantage of larger data widths (32 or 64-bits), which allows two to four times as many signals for transmission over traditional bus architectures. The computer industry has already developed some local bus architecture standards in order to alleviate this bottleneck effect. All of the current local bus standards are capable of breaking system bottlenecks, yet the industry is embracing Peripheral Component Interconnect (PCI) as the most robust and flexible bus standard for the future.

PCI Bus Overview

PCI offers some distinct advantages which has board vendors excited about its capabilities. Data transfer is accomplished via burst mode, which means data is transferred in groups of 32-bit words per protocol rather than in a word per protocol manner. In addition, PCI is a high performance, 32-bit, multiplexed address and data line bus, in which peripherals are synchronous with the faster system clock. The fact that the bus is multiplexed reduces the number of pins necessary to support the protocol because more than one signal can be sent or received at a pin, rather than having each individual signal have a dedicated pin. As a result of this feature, only 49 pins are necessary to be a master device, and 47 pins to be a target (slave) device.

Lower pin count means smaller package size. This benefit results in lower silicon cost and ease of implementation for vendors who produce the chips for the boards. PCI may force some vendors to design around the standard because Intel has defined this standard as a silicon based interconnect rather than a board to board interconnect. PCI is termed a "glueless" interconnect mechanism because no other external components or boards to the system are necessary to establish the interface between the components within the system.

PCI offers a high degree of flexibility because it is software transparent and processor independent. PCI is termed "software transparent" because PCI components are fully compatible with various classes of software platforms and applications. PCI is a processor independent bus standard which can be used with multiple families of processors as well as future processors. It also allows full multi-master capability where any PCI master can have access to any other PCI master/target making the bus a true peer-to-peer network.

Publication# 19896 Rev. B Amendment/0
Issue Date: May 1995

Typical PCI System Architecture

The typical PCI-based system architecture consists of a processor local bus, which connects the CPU to the memory subsystem, and the PCI local bus. Figure 1 represents a typical PCI-based system architecture.

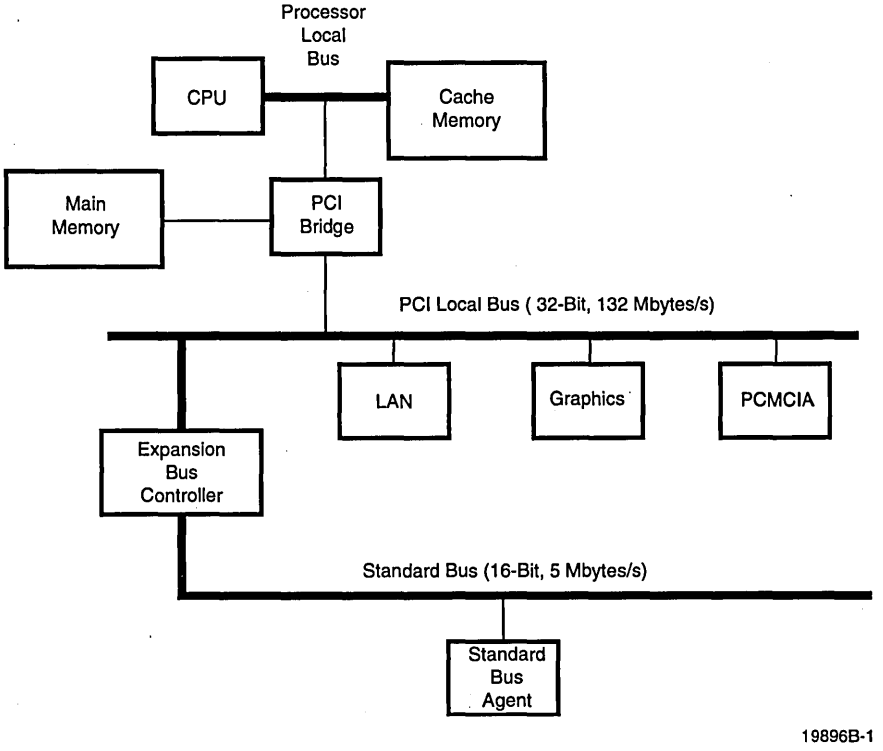


Figure 1. Typical PCI-Based System Architecture

The PCI bus allows peripherals access to the faster processor local bus through a PCI bridge, or controller, which can be implemented using traditional programmable logic. The PCI electrical specifications define both a master and target bridge implementation, where 47 pins are needed for a target device and 49 pins are necessary to implement a master device. Figure 2 shows the pins required on a PCI controller where the pins on the left are the necessary pins for the protocol, and the pins on the right are optional. The PCI bridge serves as an interface between high performance peripherals such as LAN, SCSI, and Graphics with the main system memory.

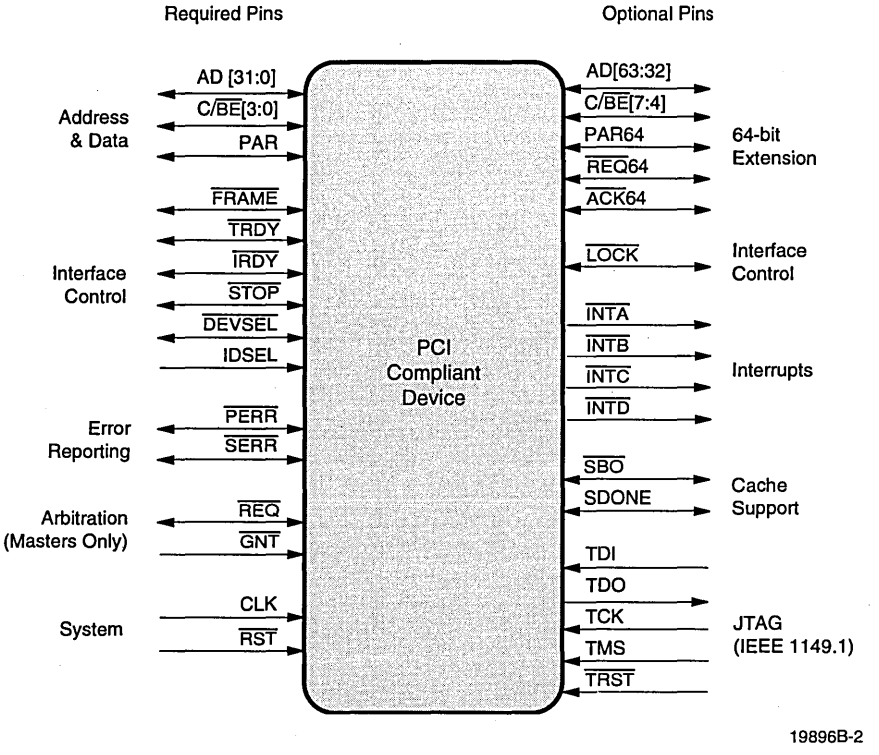


Figure 2. PCI Pin List

Table 1 provides a description of the signals indicated in Figure 2. For more information on the signals, please consult the *PCI Local Bus Specification, Revision 2.1.*

Table 1. PCI Signal Description

Signal Name	Type	Description
AD[xx:xx]	t/s	Address and Data.
C/BE[x:x]	t/s	Bus Command and Byte Enable.
PAR	t/s	Parity Across AD[xx:xx] and C/BE[x:x].
$\overline{\text{FRAME}}$	s/t/s	Cycle Frame. It indicates beginning and length of transaction.
$\overline{\text{TRDY}}$	s/t/s	Target Ready.
$\overline{\text{IRDY}}$	s/t/s	Initiator Ready.
$\overline{\text{STOP}}$	s/t/s	Stop. Current target is requesting a halt on current transaction.
$\overline{\text{DEVSEL}}$	s/t/s	Device Select.
IDSEL	input	Initialization Device Select.
$\overline{\text{PERR}}$	s/t/s	Parity Error.
$\overline{\text{SERR}}$	o/d	System Error.
$\overline{\text{REQ}}$	output	Request. It indicates that an agent is requesting use of the bus.
$\overline{\text{GNT}}$	t/s	Grant.
CLK	input	Clock.
$\overline{\text{RST}}$	input	Reset.
$\overline{\text{ACK64}}$	s/t/s	Acknowledge 64-Bit Transfer.
$\overline{\text{LOCK}}$	s/t/s	Lock.
$\overline{\text{INTA}}$ – $\overline{\text{INTD}}$	o/d	Interrupt.
$\overline{\text{SBO}}$	in/out	Snoop Backoff.
SDONE	in/out	Snoop Done.

Signal Type Definitions

in = Standard input-only signal.

out = Totem Pole Output.

t/s = Tri-state.

s/t/s = Sustained Tri-state. It must be driven high for one clock before floating.

o/d = Open Drain. It allows multiple devices to share as a wire-OR.

PCI Electrical Specifications

PCI is a robust design which supports both 3.3 and 5 Volt signaling environments. PCI is based on reflected wave signaling. It allows drivers to switch the bus half-way to its desired voltage, and when the incident signal reflects back from the unterminated end, the reflected wave adds to the incident wave through constructive interference, thus completing the voltage and current drive requirement. Since PCI is a non-terminated bus architecture, it should be treated as a non-terminated transmission line.

All of the devices connected to the bus must meet the alternating current (AC), direct current (DC), timing, and protocol requirements in order to have access to the bus. Tables 2–4 show the PCI electrical and timing specifications with the MACH210A-7/10 specifications included for comparison (for more specific information on the specifications, refer to chapter 4 of the *PCI Local Bus Specification, Revision 2.1*).

Table 2. PCI DC Specifications for 5 V Signaling

Symbol	Parameter	Condition	PCI Specification		MACH210A-7/10 Specification		Units	Compliant
			Min	Max	Min	Max		
V_{CC}	Supply Voltage		4.75	5.25	4.75	5.25	V	Yes
V_{IH}	Input High Voltage		2.00	V_{CC}+0.5	2.00		V	Yes
V_{IL}	Input Low Voltage		–0.5	0.8		0.8	V	Yes
I_{IH}	Input High Leakage Current	V_{IN} = 2.7 Volts		70.00		10	µA	Yes
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5 Volts		–70.00		–100[1]	µA	Yes
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		2.4		V	Yes
V_{OL}	Output Low Voltage	I_{OUT} = 3 mA, 6 mA		0.55		0.5	V	Yes
C_{IN}	Input Pin Capacitance			10.00		6	pF	Yes
CCLK	CLK Pin Capacitance		5.00	12.00		6	pF	Yes
CIDSEL	IDSEL Pin Capacitance			8.00		8.00	pF	Yes
Lpin[2]	Pin Inductance			20.00		20.00	nH	Yes

Table 3. PCI AC Specifications for 5 V Signaling[3]

Symbol	Parameter	Condition	PCI Specification		MACH210A-7/10 Specification		Units	Compliant
			Min	Max	Min	Max		
I_{OH} (AC)	Switching Current High	0 < V_{OUT} < = 1.4	–44		–50		mA	Yes
		1.4 < V_{OUT} < = 2.4	Eqtn C		Eqtn C		mA	Yes
		3.1 < V_{OUT} < V_{CC}		Eqtn A		Eqtn A	mA	Yes
	(test point)	V_{OUT} = 3.1		–142		–142	mA	Yes
I_{OL} (AC)	Switching Current Low	V_{OUT} > = 2.2	95		95		mA	Yes
		2.2 > V_{OUT} > 0.55	V_{OUT}/0.023		V_{OUT}/0.023		mA	Yes
		0.71 > V_{OUT} > 0		Eqtn B		Eqtn B	mA	Yes
	(test point)	V_{OUT} = 0.71		206		206	mA	Yes
Icl	Low Clamp Current	V_{IN} > –5, V_{IN} ≤ –1	Eqtn D		Eqtn D		mA	Yes
tr	Output Rise Slew Rate	0.4 V to 2.4 V	1.00	5.00	1.00	5.00	V/ns	Yes
tf	Output Fall Slew Rate	2.4 V to 0.4 V	1.00	5.00	1.00	5.00	V/ns	Yes

Equation A:

$I_{OH} = 11.9*(V_{OUT} - 5.25)*(V_{OUT} + 2.45)$ *for* $V_{CC} > V_{OUT} > 3.1$ V

Equation B:

$I_{OL} = 78.5*V_{OUT}*(4.4 - V_{OUT})$ *for* $0 V < V_{OUT} < 0.71$ V

Equation C:

$I_{OH} = -44 + (V_{OUT} - 1.4)/0.024$

Equation D:

$Icl = -25 + (V_{IN} + 1)/0.015$

Notes:

1. *Measured with V_{IN} = 0 Volts.*
2. *This parameter is not 100% tested, but was verified on the bench.*
3. *All AC specifications are not 100% tested, but were verified on the bench. Characterization data verifying bench measurements is available upon request.*

Table 4. PCI Timing Parameters

Symbol	Parameter	PCI Specification		MACH210A-7/10 Specification		Units	Compliant
		Min	Max	Min	Max		
t_{VAL}	CLK to Signal Valid Delay – Bussed Signals	2	11		6	ns	Yes
t_{VAL}(PTP)	CLK to Signal Valid Delay – Point to Point	2	12	2	7	ns	Yes
t_{ON}	Float to Active Delay (Note 1)	2		2		ns	Yes
t_{OFF}	Active to Float Delay		28		12	ns	Yes
t_{SU}	Input Set up Time to CLK – Bussed Signals	7		6.5		ns	Yes
t_{SU}(PTP)	Input Set up Time to CLK – Point to Point	10,12		6.5		ns	Yes
t_H	Input Hold Time from CLK	0		0		ns	Yes

Note:

1. *Parameter is not 100% tested. Not guaranteed under device specifications, but can be verified with initial device characterization.*

The essential PCI drive requirements are AC. PCI specifies the sink and source current limits in V/I curves where the transition from one logic level to the other are shown in the switching state and not in the typical DC, or steady state. The AC specification is based on a 10 load maximum where peripherals on the system count as one, and peripherals in expansion slots count as two. Although the PCI specification stresses operation in the dynamic realm, PCI devices should be designed for static or DC to support a 0 MHz state of the system clock.

V/I Curves

The minimum and maximum drive characteristics of PCI output buffers are specified in V/I curves. These curves are to be interpreted as DC transistor curves with the exception that the "DC Drive Point" is the only point on the pull-down and pull-up curves which is intended strictly as a steady state condition. The higher current portions of the curves are expected to be reached momentarily during bus switching transients. The "AC Drive Point" is the point which defines the minimum instantaneous current required to switch the bus with a single reflection. The "Test Point" is a requirement to limit the amount of switching noise and refers to the maximum allowable instantaneous current. The V/I curves are included for reference in Figure 3. The curves are representations and are not drawn to scale. If the output buffers do not remain in the shaded region during the transition, then the output buffers are not compliant to the AC specifications of PCI.

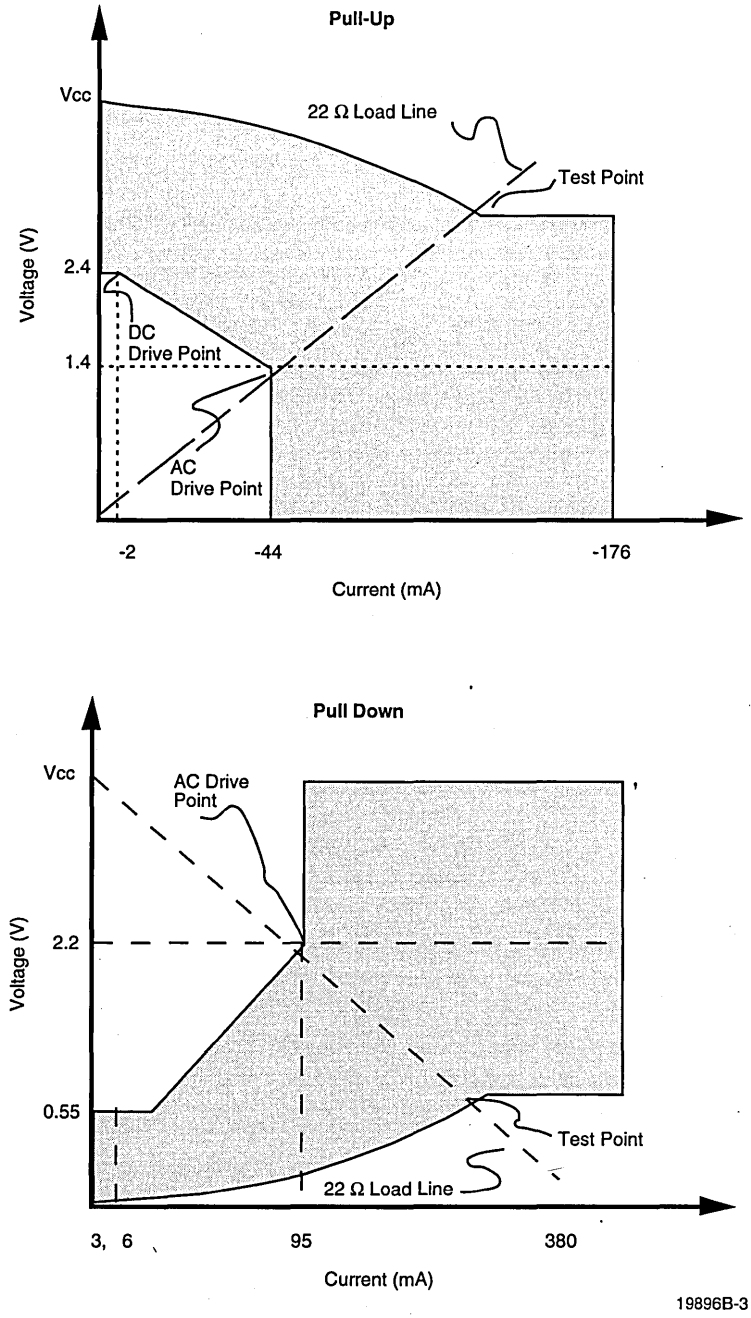


Figure 3. PCI V/I Curves for 5 V Signaling

Protocol Fundamentals

The basic data transfer mechanism on the PCI bus is burst. Burst is a data transfer method that allows packets of 32-bit words each out of phase from the other to be sent on the bus. Burst consists of an address phase followed by one or more data phases. PCI supports burst transfer in both the memory and I/O address spaces.

All data transfer is controlled by 3 signals which are sampled only on the rising edge of the clock: FRAME, IRDY, and TRDY. Refer to Table 1 for a description of the signals. A specific signal sequence must occur in order for data transfer to commence.

The address phase begins when FRAME is asserted. Once FRAME is asserted, the bus and address codes are transferred to configure the bus for the type of transaction about to occur. On the next clock edge the data transfer phase is initiated. One or more data phases can take place in which data is transferred between master and target devices on the bus as long as IRDY and TRDY are asserted on the same rising clock edge. Since data transfer is dependent on both IRDY and TRDY being asserted, wait cycles may be inserted by deasserting either the IRDY or the TRDY signal when FRAME is still asserted. Once a data transfer is implemented, neither the master nor the target device can cease the transaction in progress until the current data phase is complete. Data phase completion occurs when both IRDY and TRDY are both deasserted. The bus returns to the idle state when both FRAME and IRDY are deasserted. Figure 4 illustrates the protocol fundamentals discussion and shows a basic read operation on PCI.

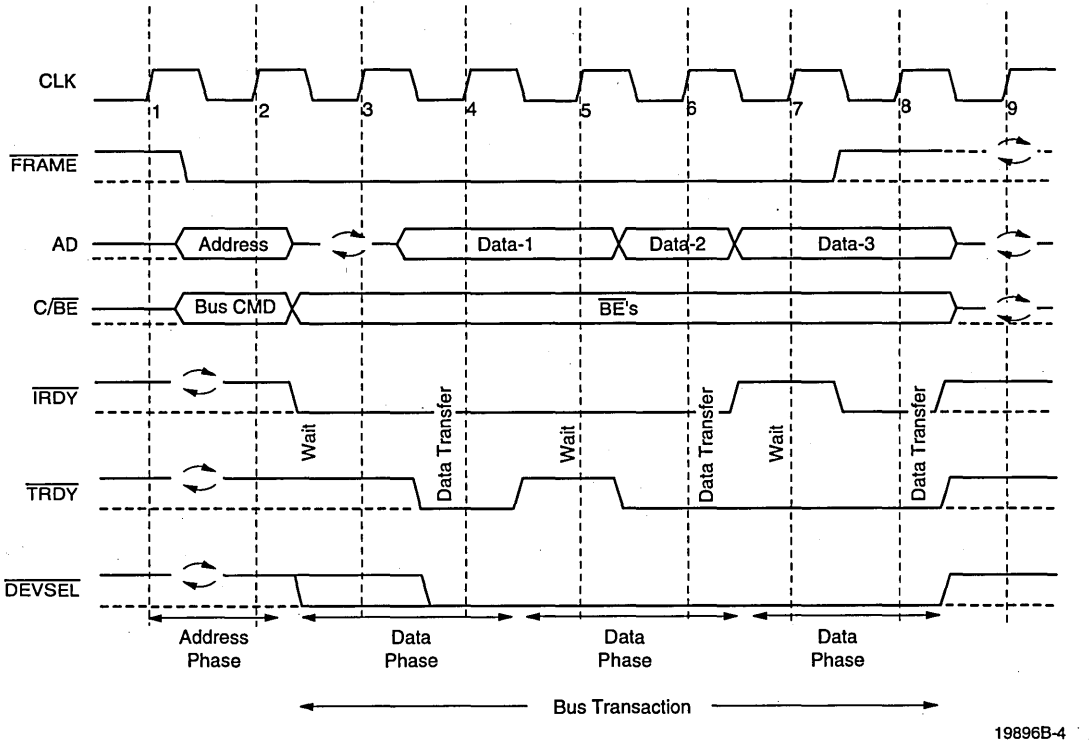


Figure 4. Basic Read Operation on PCI

PCI Compliance

Compliance is an industry recognized term that describes a device's adherence to the minimum electrical and timing specifications of PCI. Any other term used to describe this condition should be investigated for its meaning. PCI compliance is the condition that insures full functionality of a device on the bus. The PCI Local Bus Standard specification contains a checklist which, if adhered, will ensure PCI compliance. This checklist demonstrates the minimum amount of work required in order to claim compliance. PCI compliance is considered a must in systems that are to be sold in the market in order to attain highest performance from a system.

The PCI bridge, which is necessary to interface the peripherals with the processor local bus, can contain multiple master and target devices depending on the complexity of the board design. The PCI specification states that a PCI agent or target device should have a minimum of 47 pins to implement the protocol. However, implementing the PCI protocol is not restricted to the duties of one large device. A valid alternative is to use a combination of CPLDs and SPLDs to perform separate tasks of the protocol. For instance, a MACH445 can be used for bus addressing while a PALCE16V8 can perform the task of Interrupt Controller. A 5 Volt only checklist is included in Appendix A of the application note and shows PCI compliance for the MACH210A-7/10 devices.

66 MHz PCI

PCI Revision 2.1 has defined electrical specifications for boards to operate up to a maximum clock speed of 66 MHz. Access to a 66 MHz system clock for PCI provides connectivity to very high bandwidth applications such as advanced video and 3-D graphics.

The DC and AC specifications are the same as the 3.3 Volt specifications for 33 MHz PCI. The only difference between 33 and 66 MHz PCI entails the requirement for faster timing parameters and redefined measuring conditions.

The flexibility of the PCI bus standard allows for coexistence between 33 MHz devices and 66 MHz busses or vice-versa because the slower device or bus will dictate the timing functionality of PCI. However, to ensure this coexistence, PCI devices must meet both 66 and 33 MHz PCI electrical and timing requirements. While the 33 MHz PCI bus drivers are defined by their V/I curves, 66 MHz PCI bus drivers are defined by their AC and DC drive points, timing parameters and slew rate. The PCI Special Interest Group has given definition to the minimum and maximum drive points:

The minimum AC drive point defines an acceptable first step voltage and must be reached within the maximum Tval time. The maximum AC drive point limits the amount of overshoot and undershoot in the system. The DC drive point specifies steady state conditions. The minimum slew rate and the timing parameters guarantee 66 MHz operation. The maximum slew rate minimizes system noise.

Since the specifications for 66 MHz PCI are so strict, many silicon manufacturers will need to design new devices to meet the requirements.

PCI Bus Interface Design using the MACH465

The purpose of this design is to provide a simple master and slave interface onto the PCI bus. The master interface should be able to support burst accesses. In order to implement this design, the following assumptions were made:

1. The MACH465 device provides an interface between the PCI bus and a proprietary local bus on an adapter card or embedded application.
2. Any application specific data buffering is implemented outside of this design.
3. Dedicated configuration registers are implemented outside of this device.

The implemented basic features are:

1. Single and burst master reads and writes.
2. Access to memory or I/O space.
3. Signal parity generation and checking.
4. The ability to respond to Target Aborts and Retry.
5. The ability to suspend the transaction on Master Abort.

Since the PCI bus is a synchronous bus, the back-end signals are synchronized to the PCI clock as well. Table 5 shows a list of the backend signals used in the design.

Table 5. Back-End Signal Summary

Signal Name	Type	Description
AD[31:0]	t/s	Address and Data.
C/$\overline{BE}$[3:0]	t/s	Bus Command and Byte Enable.
BURST	input	Burst, indicates that the master transfer is burst access.
CNFG_$\overline{RD}$	output	Configuration Read. The slave access was decoded as a configuration read.
CNFG_$\overline{RDY}$	input	Configuration Ready. This input terminates the configuration access.
CNFG_$\overline{WR}$	output	Configuration Write. The slave access was decoded as a configuration write.
DATA[31..0]	t/s	Data bus.
$\overline{DEV\_REQ}$	input	Master Request. The back-end device wants to perform a PCI bus access.
$\overline{DEV\_ACK}$	output	Master Acknowledge. The interface logic indicates that the PCI bus access has completed.
$\overline{M\_ABORT}$	output	Master Abort. If a PCI access is attempted and no target responds, a master abort signal is asserted to inform the back-end I/O device.
MEM/IO	input	Memory I/O. This signal indicates whether the access is destined to memory or I/O space.
$\overline{NEXT}$	output	Next. This signal dictates whether the access is to memory or I/O space.
$\overline{RETRY}$	output	Retry. An indication that the target can not proceed at the current time.
$\overline{RD/WR}$	input	Read/Write. The master transfer is a read or a write access.
$\overline{T\_ABORT}$	output	Target Abort. The current target has indicated a fatal error.

Signal Type Definitions

in = Standard input-only signal.

out = Totem Pole Output.

t/s = Tri-state.

s/t/s = Sustained Tri-state. It must be driven high for one clock before floating.

o/d = Open Drain which allows multiple devices to share as a wire-OR.

State Machine Description

A simple state machine performs the main control between the PCI interface and the back-end interface (Figure 5). The state machine contains a total of 10 states. The idle state, or State 0 as shown in Figure 5, designates an inactive period when no relevant PCI slave or master data transfers are executed. The transition of states 1 through 7 depends on the type of read or write access executed by a PCI bus master. Whether it be a single or burst transaction, both are supported by the state machine design. If errors occur during the transfer, the state machine allows escape routes back to the idle state. States 8 through 10 provide the interface of a slave or configuration access.

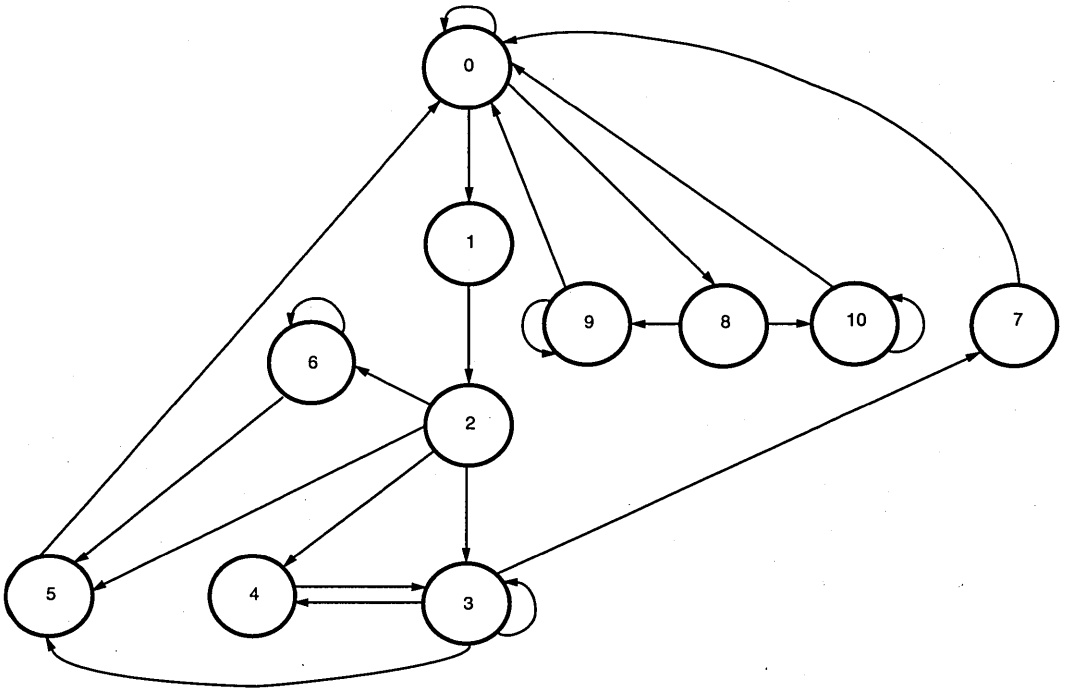


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Figure 5. State Machine Diagram

In the idle state, both the PCI interface and the back-end interface of the MACH465 are examined to determine whether a master or configuration access is required from the PCI bus. If a master access is requested, the state machine moves to state 1 where the data of the ADDR[31..0] pins is transferred to the AD[31..0] pins of the PCI bus. The address is actually latched in state 0 until enabled to the address pins of the bus in state 1. The subsequent state is state 2 which acts as the hub of the state machine because transition from this state is determined by the nature of the transaction. The different types of transactions that can occur are single access, burst access, target aborted transfer, and read or write access. If the requested transaction is a burst access, the state machine then proceeds to state 4. There are several instances when the state machine can move to state 5, all of which are target initiated, such as target abort, retry, disconnect and transfer complete. State 5 is the final state of the master transfer before returning to the idle state. If the transaction is not completed in a single data cycle, the state machine transitions to state 3. State 3 performs the same function as state 2 with two exceptions. As defined in the *PCI Local Bus Specification, revision 2.1*, parity can be implemented on both the address and data phases as long as its available one cycle after the given phase. Thus, the address parity must be made available during state 2. However, if a write access occurs, then parity is enabled during state 3 because the parity signal should only be enabled for data on write accesses. The other difference between States 2 and 3 is the influence of an internal counter which is used to prohibit the PCI bus from locking during an invalid transaction. If a master requests an access to a non-existent target or memory , the current transaction must complete gracefully and not lock the bus. All PCI transactions must complete within four cycles. If a target has not responded in this time frame, then the transaction is forced to retire at state 7. A transaction enters state 4 if a burst access is initiated. This state serves the purpose of adding a wait state into the burst access. The burst will continue for as long as the burst signal is asserted by the back-end device. State 5, as mentioned earlier, is the final state before returning to the idle state. All PCI signals that have been driven during the transaction are de-asserted during the idle state.

A transition from state 0 to state 8 occurs when a configuration access is requested by the PCI bus. The first action required is for the back-end device to release its local bus. If the back-end device is requesting a PCI

master transfer during its release of the local bus, then the request must be aborted. The state machine will proceed from state 8 to either state 9 or 10 depending on whether the transfer is a configuration read or write, respectively. When the back-end I/O device asserts the CNFG_RDY signal to indicate the completion of the configuration access, the state machine will transition back to the idle state.

Logic Compilation using the MicroSim Development Tool

A logic compiler used for large designs such as the interface example just described, can have a significant impact on the final device selection and implementation. AMD supplies a wide array of different compilers ranging from the basic MACHXL to the more graphically enhanced OEM tools such as MicroSim. The interface design example was implemented using the MicroSim PLD compiler, and for various reasons. Since the example is an I/O intensive design, verification is crucial before commitment to Printed Circuit Board (PCB) layout. A development tool such as MicroSim should provide an easy mechanism for modification, the capability of fitting designs into different devices, and the ability to simulate all aspects of the implementation. However, the main reason for using MicroSim is because a large number of the signals on this design are bi-directional. Historically, many of the basic logic compilers had a problem in simulating busses and bi-directional signals.

The MicroSim development platform is a Windows based tool. The software package integrates the schematic and text features of the MicroSim tool with the Minc compiler. Functional simulation of the design can be performed as part of the development flow. Device selection and the fitting process are executed only when the design is complete.

Device selection based on different criteria can be selected by placing constraints on the compiler. Devices can be selected based on a specific architecture, vendor, package or speed. A design is considered complete once the tool selects the appropriate device or devices, compiles the design, and fits the design within the device or devices selected. The ten best fitting options based on the user's criteria are displayed once the fitting process is complete. One of the many useful features of this compiler is its ability to partition designs across multiple devices. The PCI interface design example fits into a MACH465 device. However, if the design is intended for an embedded, enclosed PCI application, it may be necessary to partition the design across several MACH® devices or standard PLDs, or a combination of both. The MicroSim package is capable of producing a JEDEC file for each device if this is the only alternative. Once the fit is found, simulation should be re-executed in order to include the timing information of the selected device.

The primary entry mechanism for MicroSim is via a schematic, although text entry is also permissible. Appendix B contains the schematic capture file for the design example, while Appendix C contains the text file. Appendix D contains the simulation output of a basic master read, master write, burst read, burst write, configuration read and configuration write.

Device Selection

The complete design utilizes a relatively large programmable logic resource. The design requirements are:

Input Pins	9
Clock Pins	1
Output Pins	118
Buried Macrocells	21
Logical Product Terms	525
Total Logic Macrocells	146

An implementation using the MACH465 utilizes:

Percent of available resources:

Input Pins	7	50%
Clock Pins	1	25%
Output pins	126	98%
Macrocells	146	57%
Logical Product Terms	525	41%

Less than half of the available logic is used within the design. As a result, enough space is available within the MACH465 for any proprietary back-end interface. The MACH465 provides the required pin count and I/O necessary to fit the design into a single CPLD. The MACH465 is a 196 pin CPLD which contains 256 macrocells, 128 input registers, 128 I/O pins, 14 dedicated input pins and 4 clock pins all supplied in a PQFP package. The internal architecture is based around the classic MACH family with 16 PAL34V16 building blocks. Each macrocell of the PAL® block can utilize up to 20 product terms before encountering any impact on the device's performance. The block diagram can be seen in Figure 6.

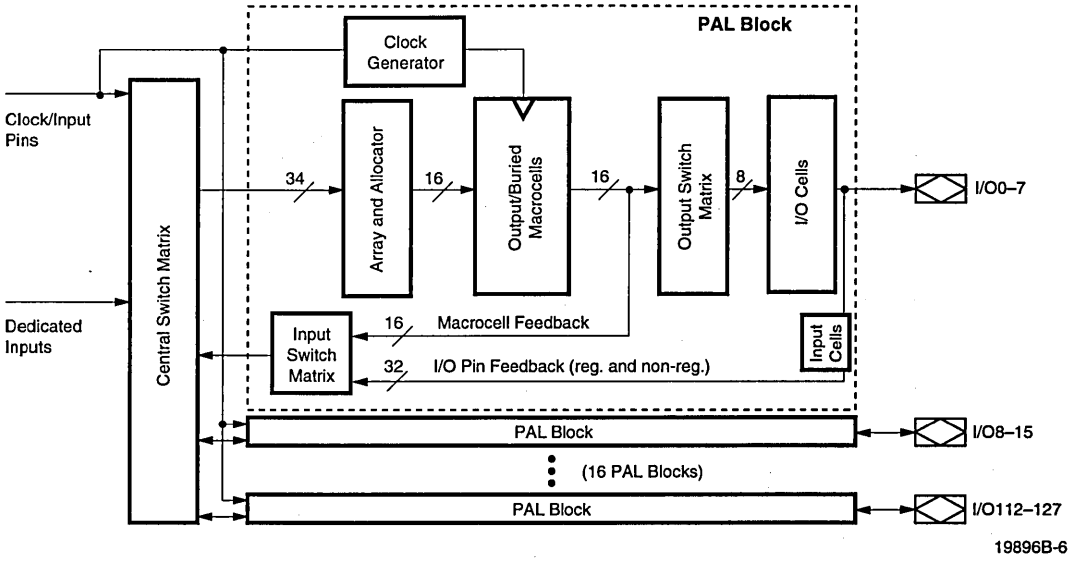


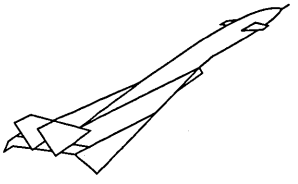
Figure 6. The MACH465 Architecture

Since the device is supplied in a PQFP package, programming the device via a programmer can pose a problem due to the finer lead pitches. Once the device is mounted on a PCB it is impossible to remove the device safely without damaging the quality of the pins. To alleviate this problem from occurring, AMD has employed the industry standard JTAG interface to all MACH devices over 84 pins in size. JTAG not only allows in-system testing, but AMD has also used the interface, together with an extra 5 V enable pin, to perform in-system programming.

Closing Statements

The main focus of this application note is the design example which should help designers implement the PCI protocol using AMD's MACH465. The rest of the document should serve as a brief synopsis of PCI fundamentals. For a more thorough discussion on any of the topics included in the document, please consult the *PCI Local Bus Specification, Revision 2.1.*

AMD has a wide assortment of devices to choose from to meet your PCI needs. To obtain any further information on any of AMD's PCI devices, please consult with your local AMD sales office. Characterization data for any of AMD's PCI compliant PLDs is available upon request. Please consult with your local sales office for further information.



APPENDIX

A PCI COMPONENT ELECTRICAL CHECKLIST

This checklist applies to the following Component/Manufacturer: MACH210A-7/10

All items were verified over the following range of junction temperatures: 26°C min 103°C max

5 V Signaling

CE1.	Component supports 5 V signaling environment?	yes X	no ___
CE2.	Component operates over voltage range 5V± 5%?	yes X	no ___
CE3.	Voltages between 2.0 V and V_{CC}+0.5 V are recognized as logic high?	yes X	no ___
CE4.	Voltages between –0.5 V and 0.8 V are recognized as logic low?	yes X	no ___
CE5.	All inputs sink less than 70 µA when pulled to 2.7 V DC?	yes X	no ___
CE6.	All inputs source less than 70 µA when pulled to 0.5 V DC?	yes X	no ___
CE7.	All outputs drive to 2.4 V (min) in the high state while sourcing 2 mA?	yes X	no ___
CE8.	All outputs drive to 0.55 V (max) in the low state, sinking 3 or 6 mA?	yes X	no ___
CE9.	Outputs source at least 44 mA at 1.4 V in the high state?	yes X	no ___
CE10.	Outputs source no more than 142 mA at 3.1 V in the high state?	yes X	no ___
CE11.	Outputs sink at least 95 mA at 2.2 V in the low state?	yes X	no ___
CE12.	Outputs sink no more than 206 mA at 0.71 V in the low state?	yes X	no ___
CE13.	$\overline{REQ}$, $\overline{GNT}$ outputs source at least 22 mA at 1.4 V in the high state?	yes X	no ___
CE14.	$\overline{REQ}$, $\overline{GNT}$ outputs sink at least 47 mA at 2.2 V in the low state?	yes X	no ___
CE15.	Clamps on all signals source at least 25 mA at –1 V, and 91 mA at –2 V?	yes X	no ___
CE16.	Unloaded edge rates are no lower than 1 V/ns between 0.4 and 2.4 V?	yes X	no ___
CE17.	Unloaded fall times are no lower than 1 V/ns between 2.4 and 0.4 V?	yes X	no ___

Loading and Device Protection

CE35.*	Capacitance on all PCI signals (except CLK, IDSEL) is less than or equal to 10 pF?	yes X	no ___
CE36.*	Capacitance on CLK signal is between 5 and 12 pF?	yes X	no ___
CE37.*	Capacitance on IDSEL signal is less than 8 pF?	yes X	no ___
CE38.	Read, understand section "Maximum AC Ratings and Device Protection"?	yes X	no ___

**Met by device specifications.*

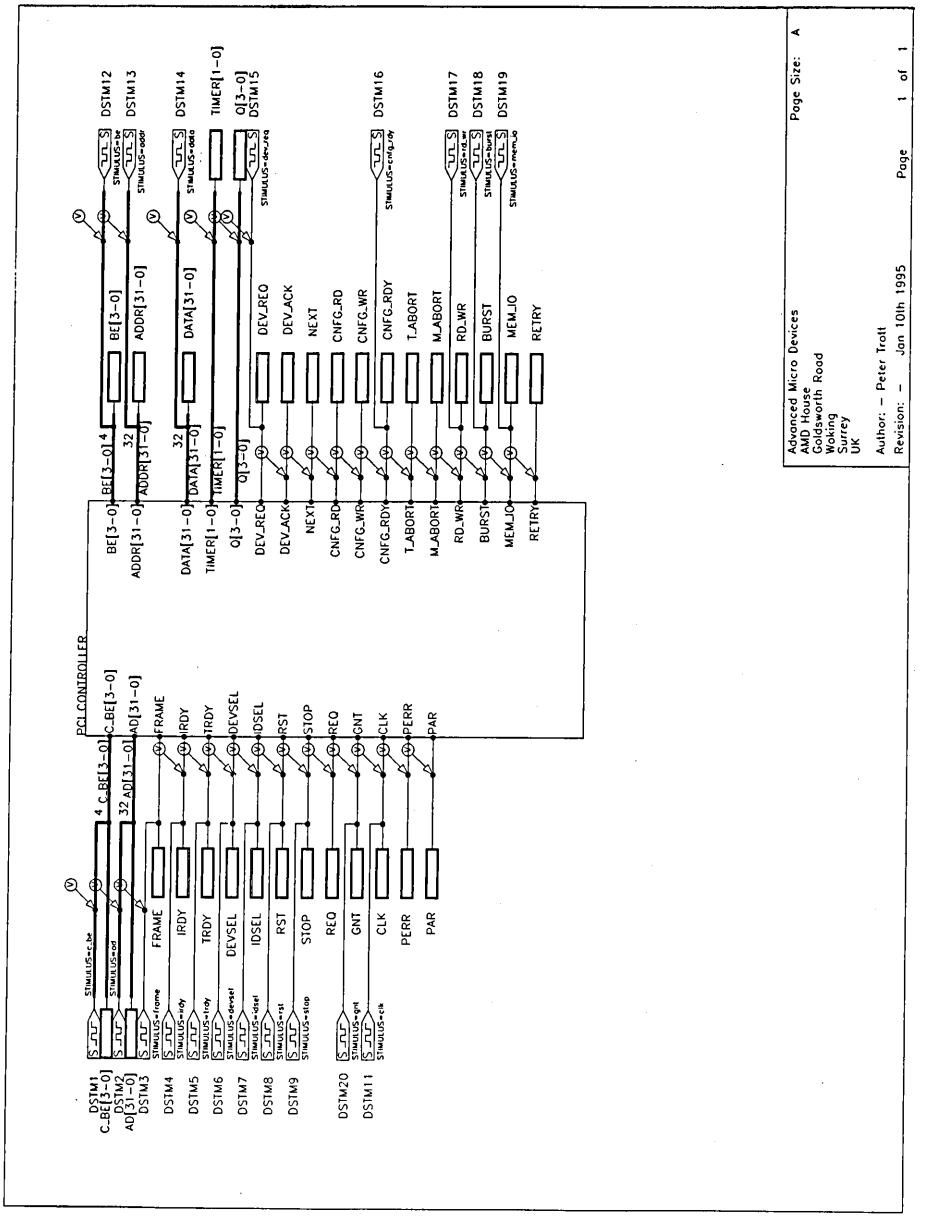
Timing Specification

CE39.*	Component is operational at any frequency between DC and 33 MHz?	yes X	no ___
CE40.*	Component is operational with a CLK High Time of 12 ns?	yes X	no ___
CE41.*	Component is operational with a CLK Low Time of 12 ns?	yes X	no ___
CE42.*	All bussed signals are driven valid between 2 ns and 11 ns after CLK?	yes X	no ___
CE43.	$\overline{REQ}$ and $\overline{GNT}$ signals are driven valid between 2 ns and 12 ns after CLK?	yes X	no ___
CE44.*	All Tri-state signals become active no earlier than 2 ns after CLK?	yes X	no ___
CE45.	All Tri-state signals float no later than 28 ns after CLK?	yes X	no ___
CE46.*	All bussed inputs require no more than 7 ns setup to CLK?	yes X	no ___
CE47.	$\overline{REQ}$ requires no more than 12 ns setup to CLK?	yes X	no ___
CE48.*	$\overline{GNT}$ requires no more than 10 ns setup to CLK?	yes X	no ___
CE49.*	All inputs require no more than 0 ns of hold time after CLK?	yes X	no ___
CE50.	All outputs are Tri-stated within 40 ns after $\overline{RST}$ goes low?	yes X	no ___
CE51	Component senses, during $\overline{RST}$ active, its connection to 64-bit wires?	yes X	no ___
CE52.	64-bit signals will be stable when not connected?	yes X	no ___

**Met by device specifications.*

APPENDIX

B MICROSIM SCHEMATIC CAPTURE FILE



MICROSIM TEXT FILE

```
PROCEDURE PCI_CONT( INPUT IDSEL;
 INPUT RST;
 INPUT STOP;
 INPUT GNT;
 INPUT CLK;
 INPUT CNFG_RDY;
 INPUT DEV_REQ;
 INPUT RD_WR;
 INPUT MEM_IO;
 INPUT BURST;
 OUTPUT DEVSEL CLOCKED_BY CLK ENABLED_BY TRST4;
 OUTPUT Q[3..0] CLOCKED_BY CLK RESET_BY /RST;
 OUTPUT REQ CLOCKED_BY CLK PRESET_BY /RST;
 OUTPUT DEV_ACK CLOCKED_BY CLK PRESET_BY /RST;
 OUTPUT NEXT CLOCKED_BY CLK PRESET_BY /RST;
 OUTPUT CNFG_RD CLOCKED_BY CLK PRESET_BY /RST;
 OUTPUT CNFG_WR CLOCKED_BY CLK PRESET_BY /RST;
 OUTPUT M_ABORT;
 OUTPUT T_ABORT CLOCKED_BY CLK RESET_BY /RST;
 OUTPUT RETRY CLOCKED_BY CLK RESET_BY /RST;
 OUTPUT TIMER[1..0] CLOCKED_BY CLK PRESET_BY /DEVSEL;
 BIPUT C_BE[3..0] CLOCKED_BY CLK ENABLED_BY TRST1;
 BIPUT BE[3..0] CLOCKED_BY CLK ENABLED_BY TRST4;
 BIPUT FRAME CLOCKED_BY CLK ENABLED_BY TRST1;
 BIPUT IRDY CLOCKED_BY CLK ENABLED_BY TRST3;
 BIPUT TRDY CLOCKED_BY CLK ENABLED_BY TRST4;
 OUTPUT PERR CLOCKED_BY CLK PRESET_BY RST ENABLED_BY PERR_OE;
 BIPUT ADDR[31..0] ENABLED_BY TRST7;
 BIPUT AD[31..0] CLOCKED_BY CLK ENABLED_BY TRST2;
 BIPUT DATA[31..0] CLOCKED_BY CLK ENABLED_BY TRST5;
 BIPUT PAR ENABLED_BY TRST6);

NODE TRST1, TRST3, TRST4;
NODE TRST2;
NODE TRST5, PERR1;
NODE PERR_OE, PAR1, PAR2, PAR3, PAR4, PAR5, PAR6 CLOCKED_BY CLK;
NODE TRST6, TRST7 ;

STATE_MACHINE MASTER STATE_BITS Q CLOCKED_BY CLK;

STATE ZERO [0000B]:
      IF (/FRAME * GNT * C_BE[3] * /C_BE[2] * C_BE[1] * IDSEL
            * /AD[1] * /AD[0]) THEN
      GOTO EIGHT;
      ELSIF (/DEV_REQ * /GNT * FRAME * IRDY) THEN
      GOTO ONE;
      ELSIF (/DEV_REQ * GNT * (/FRAME + /IRDY)) THEN
      GOTO ZERO;
      ELSIF (DEV_REQ * FRAME) THEN
      GOTO ZERO;
      END IF;

STATE ONE [0001B]:
      GOTO TWO;
```

```
STATE TWO [0010B]:
      IF (BURST * /DEVSEL * /TRDY * STOP) THEN
      GOTO FIVE;
      ELSIF (/BURST * /DEVSEL * /TRDY * STOP) THEN
      GOTO FOUR;
      ELSIF (/DEVSEL * /TRDY * /STOP) THEN
      GOTO FIVE;
      ELSIF (/DEVSEL * TRDY * /STOP) THEN
      GOTO FIVE;
      ELSIF (DEVSEL * /STOP) THEN
      GOTO FIVE;
      ELSIF (/DEVSEL * TRDY * STOP * RD_WR ) THEN
      GOTO SIX;
      ELSIF (DEVSEL * STOP) THEN
      GOTO THREE;
      END IF;

STATE THREE [0011B]:
      IF (BURST * /DEVSEL * /TRDY * STOP) THEN
      GOTO FIVE;
      ELSIF (/BURST * /DEVSEL * /TRDY * STOP) THEN
      GOTO FOUR;
      ELSIF (/BURST * /DEVSEL * TRDY * /IRDY * STOP) THEN
      GOTO THREE;
      ELSIF (/DEVSEL * /TRDY * /STOP) THEN
      GOTO FIVE;
      ELSIF (/DEVSEL * TRDY * /STOP) THEN
      GOTO FIVE;
      ELSIF (DEVSEL * /STOP) THEN
      GOTO FIVE;
      ELSIF (DEVSEL  * STOP  * /TIMER[1] * /TIMER[0]) THEN
      GOTO SEVEN;
      END IF;

STATE FOUR [0100B]:
      GOTO THREE;

STATE FIVE [0101B]:
      GOTO ZERO;

STATE SIX [0110B]:
      IF (/TRDY) THEN
      GOTO FIVE;
      ELSE
      GOTO SIX;
      END IF;

STATE SEVEN [0111B]:
      GOTO ZERO;

STATE EIGHT [1000B]:
      IF (/DEV_REQ ) THEN
      GOTO EIGHT;
```

```
        ELSIF (DEV_REQ * /CNFG_RD ) THEN
        GOTO NINE;
        ELSIF (DEV_REQ * CNFG_RD * /CNFG_WR ) THEN
        GOTO TEN;
        END IF;

STATE NINE [1001B]:
        IF (/CNFG_RD) THEN
        GOTO NINE;
        ELSE
        GOTO ZERO;
        END IF;

STATE TEN [1010B]:
        IF (/CNFG_WR) THEN
        GOTO TEN;
        ELSE
        GOTO ZERO;
        END IF;

STATE ELEVEN [1011B]:
            GOTO ZERO;

STATE TWELVE [1100B]:
            GOTO ZERO;

STATE THIRTEEN [1101B]:
            GOTO ZERO;

STATE FOURTEEN [1110B]:
            GOTO ZERO;

STATE FIFTEEN [1111B]:
            GOTO ZERO;

END MASTER;


TIMER[1] = /Q[3] * /Q[2] * /Q[1] * Q[0]
      + /Q[3] * /Q[2] * Q[1] * /Q[0] * TIMER[1] * TIMER[0]
      + /Q[3] * /Q[2] * Q[1] * Q[0] * TIMER[1] * TIMER[0];
TIMER[0] = /Q[3] * /Q[2] * /Q[1] * Q[0]
      + /Q[3] * /Q[2] * Q[1] * /Q[0] * TIMER[1] * /TIMER[0]
      + /Q[3] * /Q[2] * Q[1] * Q[0] * TIMER[1] * /TIMER[0];

FRAME =/( /Q[3] * /Q[2] * /Q[1] * /Q[0] * /DEV_REQ * /GNT * FRAME * IRDY
    + /Q[3] * /Q[2] * /Q[1] * Q[0] * /BURST
    + /Q[3] * /Q[2] * Q[1] * /Q[0] * /BURST
    + /Q[3] * /Q[2] * Q[1] * Q[0] * /BURST
    + /Q[3] * Q[2] * Q[1] * /Q[0] * /BURST);

TRST1 = /Q[3] * /Q[2] * /Q[1] * Q[0]
    + /Q[3] * /Q[2] * Q[1] * /Q[0]
    + /Q[3] * /Q[2] * Q[1] * Q[0]
```

```
      + /Q[3] * Q[2] * Q[1] * /Q[0]
      + /Q[3] * Q[2] * /Q[1] * /Q[0];

 REQ = /(/Q[3] * /Q[2] * /Q[1] * /Q[0] * /DEV_REQ * GNT);

 C_BE[0] = /Q[3] * /Q[2] * /Q[1] * /Q[0] * /RD_WR
       + /Q[3] * /Q[2] * /Q[1] * Q[0] * BE[0]
       + /Q[3] * /Q[2] * Q[1] * /Q[0] * BE[0]
       + /Q[3] * /Q[2] * Q[1] * Q[0] * BE[0]
       + /Q[3] * Q[2] * Q[1] * /Q[0] * BE[0]
       + /Q[3] * Q[2] * /Q[1] * /Q[0] * BE[0];
 C_BE[1] = /Q[3] * /Q[2] * /Q[1] * /Q[0]
       + /Q[3] * /Q[2] * /Q[1] * Q[0] * BE[1]
       + /Q[3] * /Q[2] * Q[1] * /Q[0] * BE[1]
       + /Q[3] * /Q[2] * Q[1] * Q[0] * BE[1]
       + /Q[3] * Q[2] * Q[1] * /Q[0] * BE[1]
       + /Q[3] * Q[2] * /Q[1] * /Q[0] * BE[1];
 C_BE[2] = /Q[3] * /Q[2] * /Q[1] * /Q[0] * /MEM_IO
       + /Q[3] * /Q[2] * /Q[1] * Q[0] * BE[2]
       + /Q[3] * /Q[2] * Q[1] * /Q[0] * BE[2]
       + /Q[3] * /Q[2] * Q[1] * Q[0] * BE[2]
       + /Q[3] * Q[2] * Q[1] * /Q[0] * BE[2]
       + /Q[3] * Q[2] * /Q[1] * /Q[0] * BE[2];
 C_BE[3] = /Q[3] * /Q[2] * /Q[1] * Q[0] * BE[3]
       + /Q[3] * /Q[2] * Q[1] * /Q[0] * BE[3]
       + /Q[3] * /Q[2] * Q[1] * Q[0] * BE[3]
       + /Q[3] * Q[2] * Q[1] * /Q[0] * BE[3]
       + /Q[3] * Q[2] * /Q[1] * /Q[0] * BE[3];

 IRDY = /(/Q[3] * /Q[2] * /Q[1] * Q[0]
     + /Q[3] * /Q[2] * Q[1] * /Q[0] * (TRDY + DEVSEL)
     + /Q[3] * /Q[2] * Q[1] * Q[0] * (TRDY + DEVSEL)
     + /Q[3] * Q[2] * Q[1] * /Q[0] * (TRDY + DEVSEL)
     + /Q[3] * Q[2] * /Q[1] * Q[0] * (TRDY + DEVSEL)
     + /Q[3] * Q[2] * /Q[1] * /Q[0] * BURST);

 TRST3 = /Q[3] * /Q[2] * Q[1] * /Q[0]
     + /Q[3] * /Q[2] * Q[1] * Q[0]
     + /Q[3] * Q[2] * Q[1] * /Q[0]
     + /Q[3] * Q[2] * /Q[1] * /Q[0]
     + /Q[3] * Q[2] * /Q[1] * Q[0];

 TRDY = /(Q[3] * /Q[2] * /Q[1] * Q[0] * /CNFG_RDY
          + Q[3] * /Q[2] * Q[1] * /Q[0] * /CNFG_RDY);

 TRST4 = Q[3] * /Q[2] * /Q[1] * Q[0]
     + Q[3] * /Q[2] * Q[1] * /Q[0];

 DEVSEL = /(Q[3] * /Q[2] * /Q[1] * /Q[0]
      + Q[3] * /Q[2] * /Q[1] * Q[0] * /CNFG_RD
      + Q[3] * /Q[2] * Q[1] * /Q[0] * /CNFG_WR);


BE[3..0] = C_BE[3..0];
```

```
NEXT = /(/Q[3] * /Q[2] * Q[1] * /Q[0] * /TRDY * /DEVSEL * /BURST
   + /Q[3] * /Q[2] * Q[1] * Q[0] * /TRDY * /DEVSEL * /BURST);

DEV_ACK = /(/Q[3] * Q[2] * /Q[1] * Q[0]);

T_ABORT = /Q[3] * /Q[2] * Q[1] * /Q[0] * /STOP * DEVSEL
     + /Q[3] * /Q[2] * Q[1] * Q[0] * /STOP * DEVSEL
     + /Q[3] * Q[2] * Q[1] * /Q[0] * /STOP * DEVSEL
     * /Q[3] * Q[2] * /Q[1] * /Q[0] * /STOP * DEVSEL;

RETRY = /Q[3] * /Q[2] * Q[1] * /Q[0] * /STOP * /DEVSEL
     + /Q[3] * /Q[2] * Q[1] * Q[0] * /STOP * /DEVSEL
     + /Q[3] * Q[2] * Q[1] * /Q[0] * /STOP * /DEVSEL
     * /Q[3] * Q[2] * /Q[1] * /Q[0] * /STOP * /DEVSEL;

CNFG_RD = /(/Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
     * C_BE[3] * /C_BE[2] * C_BE[1] * /C_BE[0] * IDSEL
     * /AD[1] * /AD[0]
     + Q[3] * /Q[2] * /Q[1] * /Q[0] * /CNFG_RD
        + Q[3] * /Q[2] * /Q[1] * Q[0] * CNFG_RDY * TRDY);

CNFG_WR = /(/Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
     * C_BE[3] * /C_BE[2] * C_BE[1] * C_BE[0] * IDSEL
     * /AD[1] * /AD[0]
     + Q[3] * /Q[2] * /Q[1] * /Q[0] * /CNFG_WR
        + Q[3] * /Q[2] * Q[1] * /Q[0] * CNFG_RDY * TRDY);

M_ABORT = /Q[3] * Q[2] * Q[1] * Q[0];

AD[0] = ADDR[0] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[0] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[0] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[0] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[0] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[0] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[1] = ADDR[1] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[1] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[1] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[1] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[1] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[1] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[2] = ADDR[2] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[2] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[2] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[2] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[2] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[2] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[3] = ADDR[3] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[3] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[3] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
```

```
        + DATA[3] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[3] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[3] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[4] = ADDR[4] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[4] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[4] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[4] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[4] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[4] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[5] = ADDR[5] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[5] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[5] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[5] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[5] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[5] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[6] = ADDR[6] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[6] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[6] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[6] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[6] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[6] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[7] = ADDR[7] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[7] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[7] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[7] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[7] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[7] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[8] = ADDR[8] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[8] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[8] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[8] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[8] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[8] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[9] = ADDR[9] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[9] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[9] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[9] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[9] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[9] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[10] = ADDR[10] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[10] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[10] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[10] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[10] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[10] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[11] = ADDR[11] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
```

```
        + DATA[11] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[11] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[11] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[11] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[11] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[12] = ADDR[12] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[12] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[12] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[12] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[12] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[12] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[13] = ADDR[13] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[13] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[13] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[13] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[13] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[13] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[14] = ADDR[14] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[14] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[14] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[14] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[14] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[14] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[15] = ADDR[15] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[15] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[15] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[15] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[15] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[15] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[16] = ADDR[16] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[16] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[16] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[16] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[16] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[16] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[17] = ADDR[17] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[17] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[17] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[17] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[17] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[17] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[18] = ADDR[18] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[18] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[18] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[18] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[18] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[18] * Q[3] * /Q[2] * /Q[1] * Q[0] ;
```

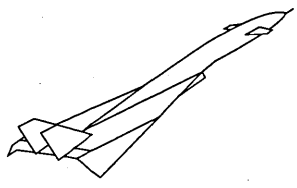
```
AD[19] = ADDR[19] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
       + DATA[19] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
       + DATA[19] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
       + DATA[19] * /Q[3] * /Q[2] * Q[1] * Q[0]
       + DATA[19] * /Q[3] * Q[2] * /Q[1] * /Q[0]
       + DATA[19] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[20] = ADDR[20] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
       + DATA[20] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
       + DATA[20] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
       + DATA[20] * /Q[3] * /Q[2] * Q[1] * Q[0]
       + DATA[20] * /Q[3] * Q[2] * /Q[1] * /Q[0]
       + DATA[20] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[21] = ADDR[21] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
       + DATA[21] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
       + DATA[21] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
       + DATA[21] * /Q[3] * /Q[2] * Q[1] * Q[0]
       + DATA[21] * /Q[3] * Q[2] * /Q[1] * /Q[0]
       + DATA[21] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[22] = ADDR[22] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
       + DATA[22] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
       + DATA[22] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
       + DATA[22] * /Q[3] * /Q[2] * Q[1] * Q[0]
       + DATA[22] * /Q[3] * Q[2] * /Q[1] * /Q[0]
       + DATA[22] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[23] = ADDR[23] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
       + DATA[23] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
       + DATA[23] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
       + DATA[23] * /Q[3] * /Q[2] * Q[1] * Q[0]
       + DATA[23] * /Q[3] * Q[2] * /Q[1] * /Q[0]
       + DATA[23] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[24] = ADDR[24] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
       + DATA[24] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
       + DATA[24] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
       + DATA[24] * /Q[3] * /Q[2] * Q[1] * Q[0]
       + DATA[24] * /Q[3] * Q[2] * /Q[1] * /Q[0]
       + DATA[24] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[25] = ADDR[25] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
       + DATA[25] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
       + DATA[25] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
       + DATA[25] * /Q[3] * /Q[2] * Q[1] * Q[0]
       + DATA[25] * /Q[3] * Q[2] * /Q[1] * /Q[0]
       + DATA[25] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[26] = ADDR[26] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
       + DATA[26] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
       + DATA[26] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
       + DATA[26] * /Q[3] * /Q[2] * Q[1] * Q[0]
```

```
        + DATA[26] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[26] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[27] = ADDR[27] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[27] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[27] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[27] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[27] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[27] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[28] = ADDR[28] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[28] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[28] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[28] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[28] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[28] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[29] = ADDR[29] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[29] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[29] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[29] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[29] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[29] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[30] = ADDR[30] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[30] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[30] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[30] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[30] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[30] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

AD[31] = ADDR[31] * /Q[3] * /Q[2] * /Q[1] * /Q[0]
        + DATA[31] *  /Q[3] * /Q[2] * /Q[1] * Q[0]
        + DATA[31] *  /Q[3] * /Q[2] * Q[1] * /Q[0]
        + DATA[31] * /Q[3] * /Q[2] * Q[1] * Q[0]
        + DATA[31] * /Q[3] * Q[2] * /Q[1] * /Q[0]
        + DATA[31] * Q[3] * /Q[2] * /Q[1] * Q[0] ;

TRST2 =   /Q[3] * /Q[2] * /Q[1] * Q[0]
   + /Q[3] * /Q[2] * Q[1] * /Q[0] * /RD_WR
   + /Q[3] * /Q[2] * Q[1] * Q[0] * /RD_WR
   + /Q[3] * Q[2] * /Q[1] * /Q[0] * /RD_WR
   + Q[3] * /Q[2] * /Q[1] * Q[0];

ADDR[31] = AD[31] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[31] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[30] = AD[30] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[30] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[29] = AD[29] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[29] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[28] = AD[28] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
```

```
        + ADDR[28] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[27] = AD[27] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[27] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[26] = AD[26] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[26] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[25] = AD[25] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[25] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[24] = AD[24] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[24] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[23] = AD[23] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[23] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[22] = AD[22] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[22] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[21] = AD[21] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[21] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[20] = AD[20] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[20] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[19] = AD[19] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[19] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[18] = AD[18] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[18] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[17] = AD[17] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[17] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[16] = AD[16] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[16] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[15] = AD[15] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[15] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[14] = AD[14] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[14] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[13] = AD[13] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[13] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[12] = AD[12] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[12] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[11] = AD[11] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[11] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[10] = AD[10] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
```

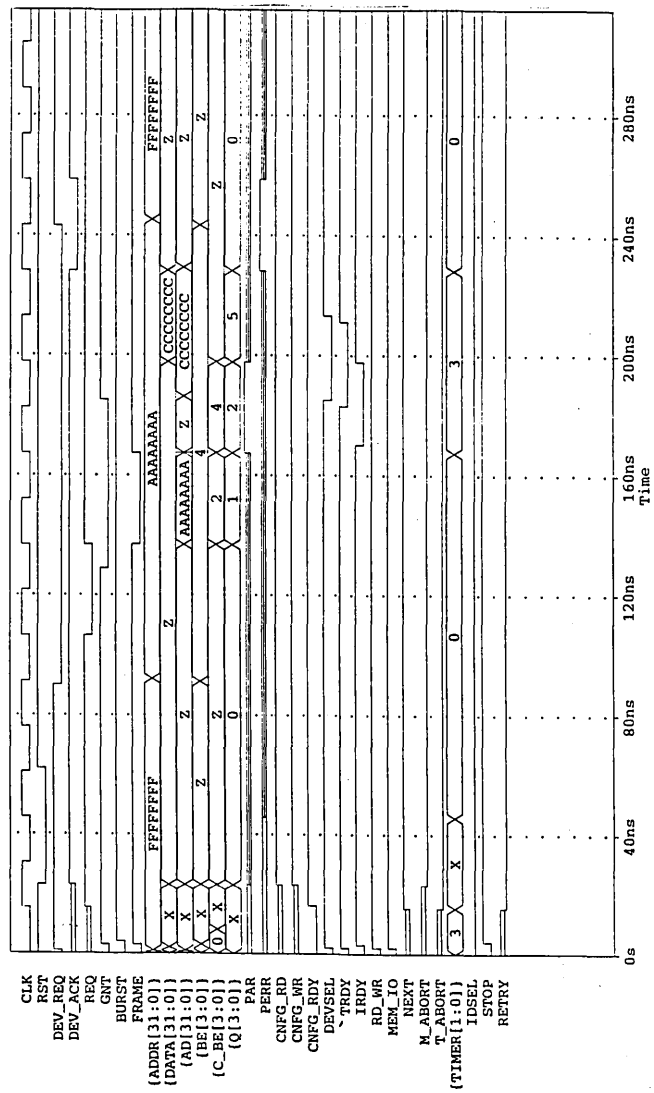
```
        + ADDR[10] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[9] = AD[9] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[9] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[8] = AD[8] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[8] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[7] = AD[7] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[7] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[6] = AD[6] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[6] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[5] = AD[5] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[5] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[4] = AD[4] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[4] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[3] = AD[3] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[3] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[2] = AD[2] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[2] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[1] = AD[1] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[1] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

ADDR[0] = AD[0] * Q[3] * /Q[2] * /Q[1] * /Q[0] * /FRAME
        + ADDR[0] * Q[3] * /Q[2] * (/CNFG_RD + /CNFG_WR) * FRAME;

TRST7 = /CNFG_RD + /CNFG_WR;

DATA = AD;

TRST5 = /Q[3] * Q[2] * /Q[1] * Q[0] * RD_WR
    + /Q[3] * Q[2] * /Q[1] * /Q[0] * RD_WR
    + Q[3] * /Q[2] * Q[1] * /Q[0];

PAR1 = AD[0] (+) AD[1] (+) AD[2] (+) AD[3] (+) AD[4] (+) AD[5];
PAR2 = AD[6] (+) AD[7] (+) AD[8] (+) AD[9] (+) AD[10] (+) AD[11];
PAR3 = AD[12] (+) AD[13] (+) AD[14] (+) AD[15] (+) AD[16] (+) AD[17];
PAR4 = AD[18] (+) AD[19] (+) AD[20] (+) AD[21] (+) AD[22] (+) AD[23];
PAR5 = AD[24] (+) AD[25] (+) AD[26] (+) AD[27] (+) AD[28] (+) AD[29];
PAR6 = AD[30] (+) AD[31] (+) C_BE[0] (+) C_BE[1] (+) C_BE[2] (+) C_BE[3];

PAR = (PAR1 (+) PAR2) (+) (PAR3 (+) PAR4) (+) PAR5 (+) PAR6;

TRST6 = /Q[3] * /Q[2] * Q[1] * /Q[0]
    + /Q[3] * /Q[2] * Q[1] * Q[0] * /RD_WR
    + /Q[3] * Q[2] * /Q[1] * Q[0] * /RD_WR;

PERR = /Q[3] * Q[2] * /Q[1] * Q[0]
```

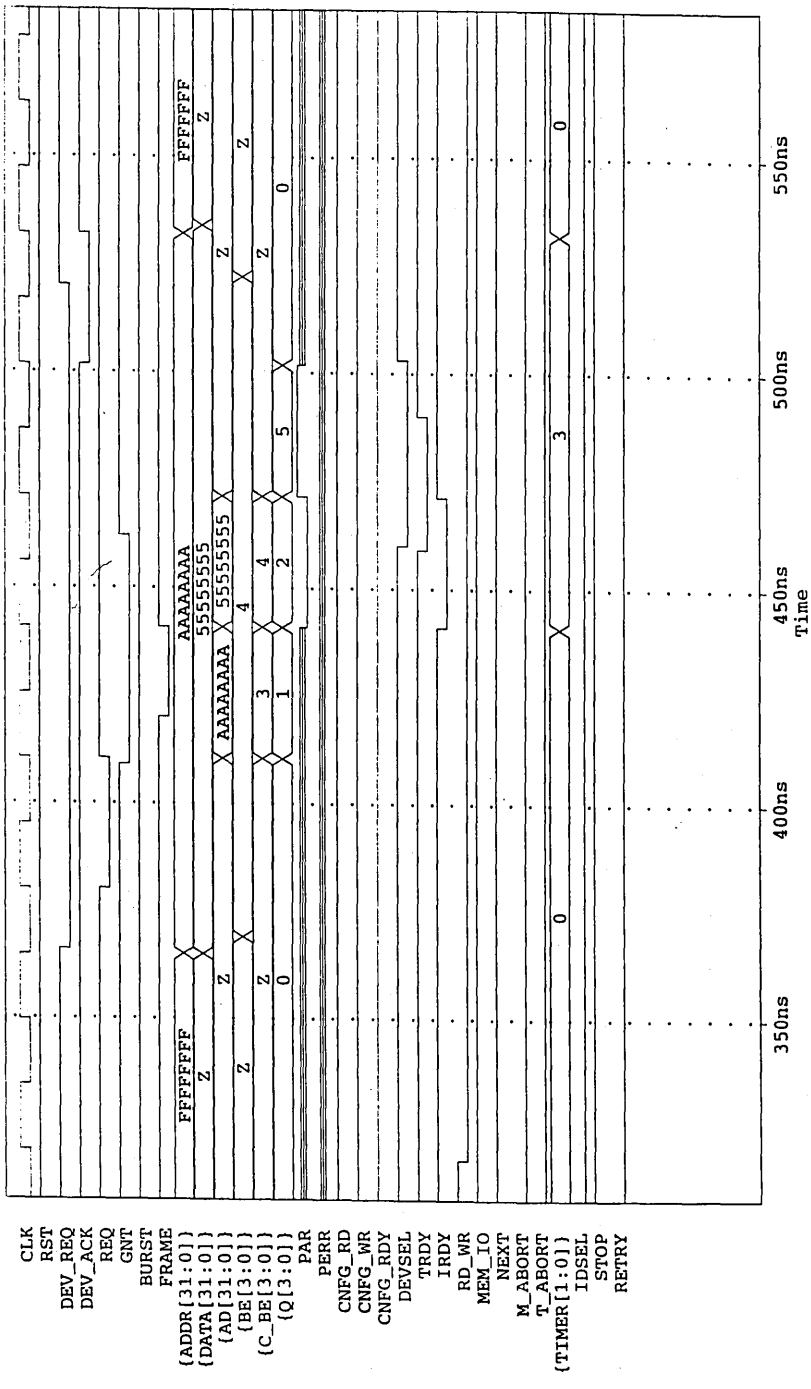
```
    * (PAR (+) PERR1);

PERR1 = PAR1 (+) PAR2 (+) PAR3 (+) PAR4 (+) PAR5 (+) PAR6;

PERR_OE = /Q[3] * Q[2] * /Q[1] * /Q[0] * RD_WR * BURST
    + /Q[3] * Q[2] * /Q[1] * Q[0] * RD_WR;

END PCI_CONT;
```

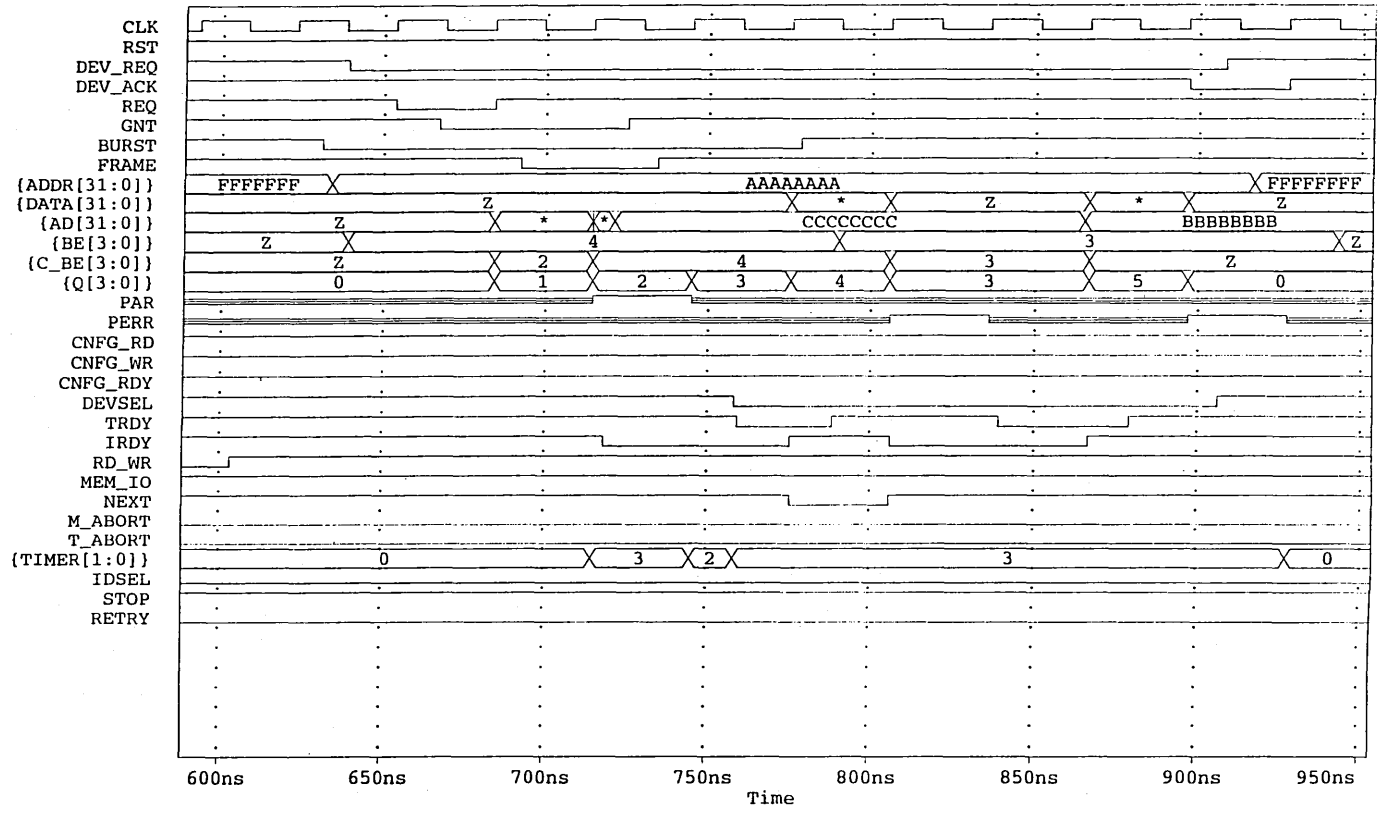


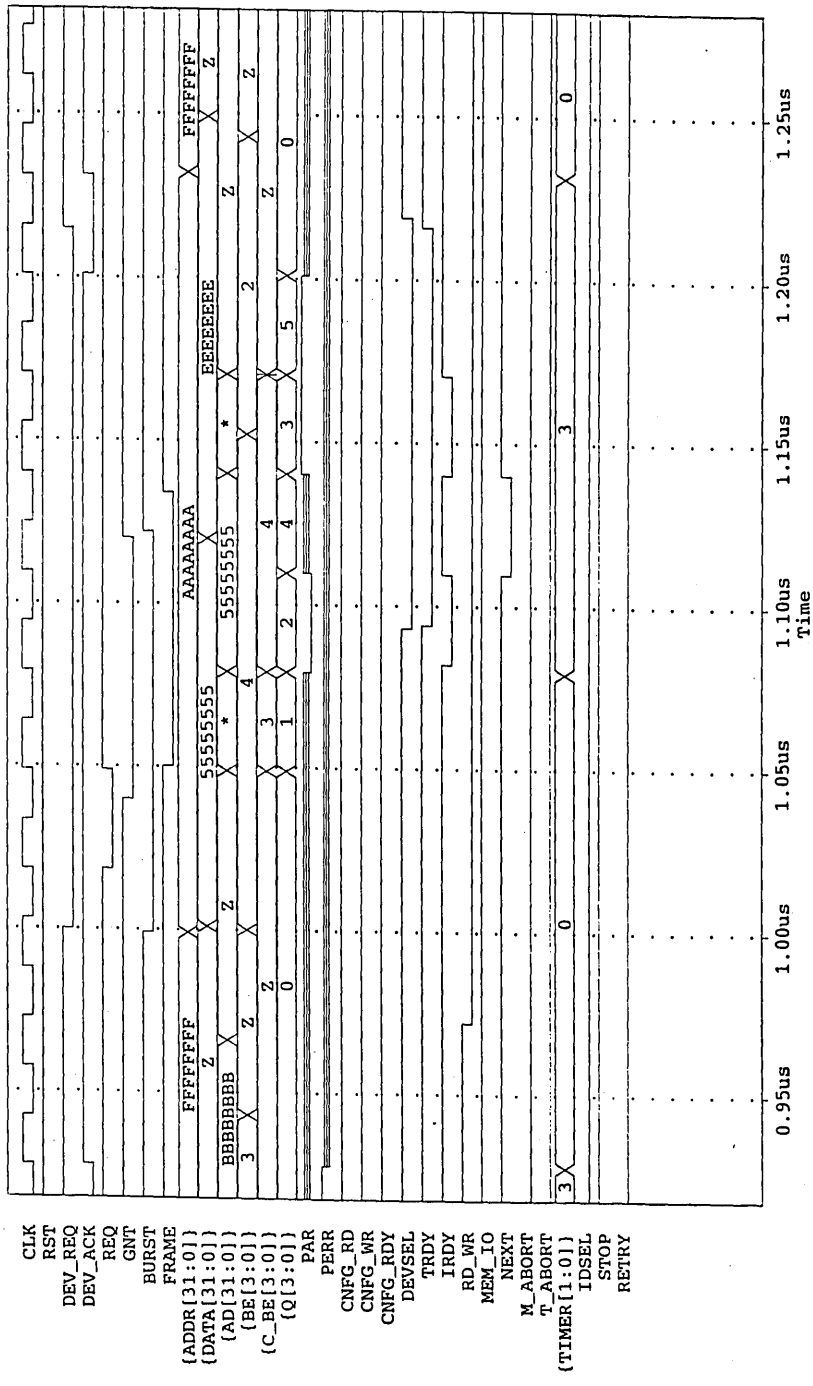
APPENDIX

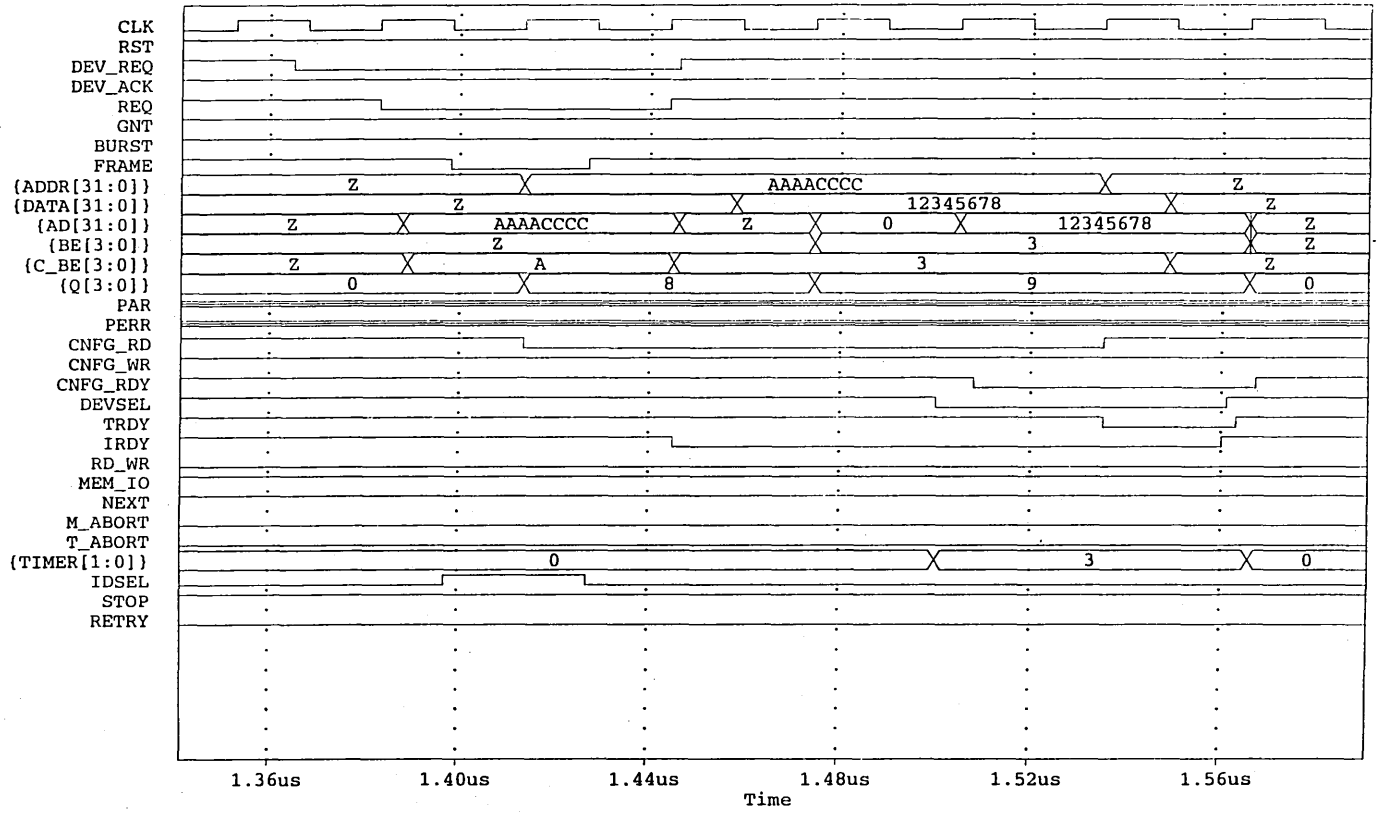
D SIMULATION OUTPUT FILES

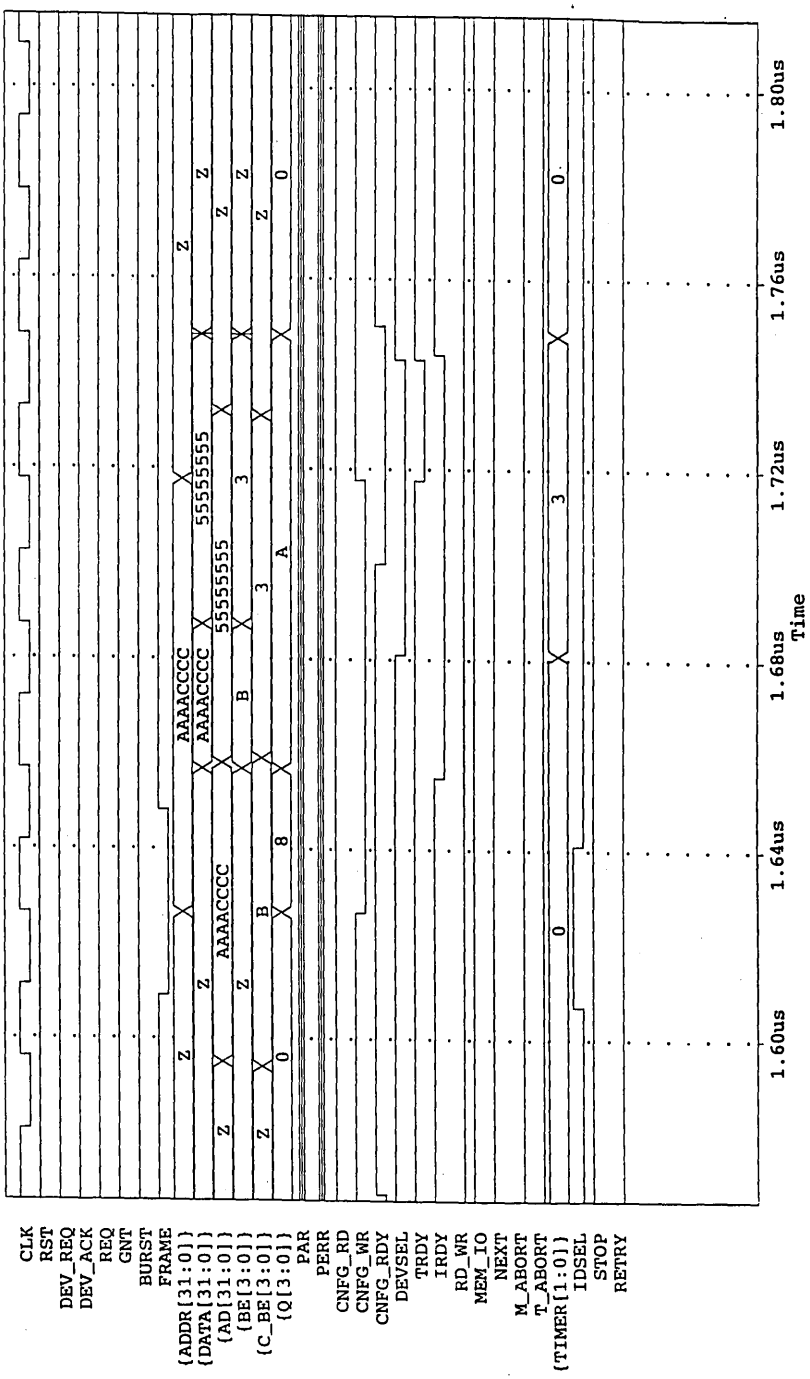



CLK
RST
DEV_REQ
DEV_ACK
REQ
GNT
BURST
FRAME
{ADDR[31:0]}
{DATA[31:0]}
{AD[31:0]}
{BE[3:0]}
{C_BE[3:0]}
{Q[3:0]}
PAR
PERR
CNFG_RD
CNFG_WR
CNFG_RDY
DEVSEL
TRDY
IRDY
RD_WR
MEM_IO
NEXT
M_ABORT
T_ABORT
{TIMER[1:0]}
IDSEL
STOP
RETRY
FFFFFFFF
Z
AAAAAAAA
55555555
4
0
1
2
3
5
350ns
400ns
450ns
500ns
550ns
Time


CLK
RST
DEV_REQ
DEV_ACK
REQ
GNT
BURST
FRAME
{ADDR[31:0]}
{DATA[31:0]}
{AD[31:0]}
{BE[3:0]}
{C_BE[3:0]}
{Q[3:0]}
PAR
PERR
CNFG_RD
CNFG_WR
CNFG_RDY
DEVSEL
TRDY
IRDY
RD_WR
MEM_IO
NEXT
M_ABORT
T_ABORT
{TIMER[1:0]}
IDSEL
STOP
RETRY
FFFFFFFF
AAAAAAAA
FFFFFFFF
CCCCCCCC
BBBBBBBB
600ns
650ns
700ns
750ns
800ns
850ns
900ns
950ns
Time


CLK
RST
DEV_REQ
DEV_ACK
REQ
GNT
BURST
FRAME
{ADDR[31:0]}
{DATA[31:0]}
{AD[31:0]}
{BE[3:0]}
{C_BE[3:0]}
{Q[3:0]}
PAR
PERR
CNFG_RD
CNFG_WR
CNFG_RDY
DEVSEL
TRDY
IRDY
RD_WR
MEM_IO
NEXT
M_ABORT
T_ABORT
{TIMER[1:0]}
IDSEL
STOP
RETRY
FFFFFFFF
Z
BBBBBBBB
3
0
55555555
AAAAAAAA
EEEEEEEE
FFFFFFFF
0.95us
1.00us
1.05us
1.10us
1.15us
1.20us
1.25us
Time


CLK
RST
DEV_REQ
DEV_ACK
REQ
GNT
BURST
FRAME
{ADDR[31:0]}
{DATA[31:0]}
{AD[31:0]}
{BE[3:0]}
{C_BE[3:0]}
{Q[3:0]}
PAR
PERR
CNFG_RD
CNFG_WR
CNFG_RDY
DEVSEL
TRDY
IRDY
RD_WR
MEM_IO
NEXT
M_ABORT
T_ABORT
{TIMER[1:0]}
IDSEL
STOP
RETRY
Z
AAAACCCC
12345678
0
A
3
8
9
1.36us
1.40us
1.44us
1.48us
1.52us
1.56us
Time


CLK
RST
DEV_REQ
DEV_ACK
REQ
GNT
BURST
FRAME
{ADDR[31:0]}
{DATA[31:0]}
{AD[31:0]}
{BE[3:0]}
{C_BE[3:0]}
{Q[3:0]}
PAR
PERR
CNFG_RD
CNFG_WR
CNFG_RDY
DEVSEL
TRDY
IRDY
RD_WR
MEM_IO
NEXT
M_ABORT
T_ABORT
{TIMER[1:0]}
IDSEL
STOP
RETRY
AAAACCCC
55555555
1.60us
1.64us
1.68us
1.72us
1.76us
1.80us
Time

Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices

Advanced Micro Devices

Application Note

Certain members of the second-generation, high-performance, high-density, MACH devices contain features that require a formal introduction: JTAG testing capabilities and five-volt programming. Any MACH device with more than 84 pins will contain the JTAG and programming enhancements. These devices presently include the MACH445, the MACH355, and the MACH465.

The purpose of this application note is to provide the user with the basic knowledge required to understand the topics of JTAG and five-volt, on-board programming. A listing of AMD and third-party support tools is also included. Descriptions of the associated AMD MACHXL programming software files are found in the AMD MACHPRO™ software manual. An additional application note containing advanced system-level reconfiguration techniques is available for more exotic applications.

A BRIEF HISTORY OF JTAG

JTAG is the commonly used acronym for the IEEE Standard 1149.1-1990. The concept for this standard was proposed by a group of European companies known as the Joint European Test Action Group, or JETAG, in 1985. A year later, this group was expanded to include companies from North America and the name was changed to Joint Test Action Group, or JTAG. This group developed a standard so that circuit connectivity could be checked using a boundary-scan register approach. This standard was adopted by the Institute of Electrical and Electronics Engineers, or IEEE, in 1990. An amendment, Supplement "A", was passed in 1993 and included corrections, clarifications, and additions to the original standard.

Before the standard for boundary scan was developed, many companies were implementing their own serial or parallel scan testing methods. The JTAG standard was developed as a means of providing both board-level and device-level testing. The JTAG standard defines input and output pins, logic control functions, and instructions. To use JTAG for testing, all that is required is a four- or five-wire interface to accommodate a serial data stream and the software to drive that interface. JTAG allows access and control of each node of each JTAG-compatible integrated circuit, or IC, in order to test board connections as well as board functionality.

There are a number of benefits associated with the JTAG approach. As IC manufacturers reduce the size and increase the complexity of their devices, testing becomes more difficult with conventional methods. Printed Circuit Board, or PCB, traces have decreased in width by a factor of ten and IC package pin sizes have decreased by a factor of eight, increasing the probability of damage to the leads during conventional testing with bulky test probes. The internal array of Boundary-Scan Cells, or BSCs, become a virtual "bed-of-nails" multi-point test set-up which makes it possible to test PCB connections and circuit logic functionality independently. The structured approach of JTAG enables the research and development testing to be easily transferred to manufacturing on conventional bed-of-nails testers.

JTAG Boundary – Scan Architecture

Figure 1 illustrates an example of a device containing JTAG circuitry. The core logic remains intact, but a separate boundary scan control circuit is added to perform the JTAG functions. The five JTAG pins are used to access the state machine, instruction register, and data registers. These five pins are known as the Test Access Port, or TAP. The TMS and TCK pins drive the state-machine-based TAP controller. A boundary-scan cell is paired with every important node in the device. These nodes include all inputs, all outputs, and enable control lines. The ENABLE* pin is a dedicated, optional non-JTAG programming pin that is utilized by AMD to enable programming a MACH device.

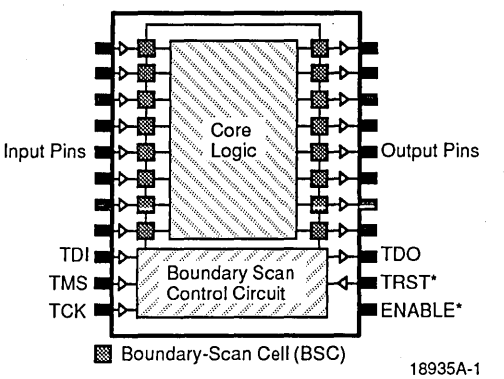


Figure 1. Boundary-Scan Architecture

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The five JTAG pins and associated functions are defined in Table 1. The ENABLE* programming pin is included in the definitions, but is not considered part of the JTAG TAP. Details on programming appear later in this application note. The TRST* and ENABLE* pins are active LOW inputs as denoted by the asterisk.

Table 1. TAP Pin Descriptions

TCK (Test Clock)	This pin controls the state machine and data transfer operations
TMS (Test Mode Select)	Selects the boundary scan test mode, which controls the state machine test operations
TDI (Test Data Input)	Receives serial instruction codes and data on the rising edge of the TCK signal
TDO (Test Data Output)	Shifts serial output data on the falling edge of the TCK signal
TRST* (Test Reset)	Optional JTAG pin used to reset the state machine
ENABLE* (Program)	Non-JTAG pin used for programming MACH devices

JTAG TAP Controller

All implementations of JTAG are required to contain three key elements for the TAP controller. These elements include the state machine, the instruction register and the data registers. The synchronous finite state machine controls the function of the various JTAG registers. The state machine determines whether the device is in reset mode, receiving an instruction, receiving data, or idling. The state machine, as illustrated in Figure 2, is completely controlled by the TCK, TMS, and TRST* pins. The value of TMS on the edge of TCK is located next to each transition in Figure 2.

The TAP controller shifts and updates the individual JTAG registers. The data enters on the TDI pin and exits through the TDO pin. After the data is shifted into place, the TAP controller updates the register to make the data current. As stated earlier, there are boundary-scan cells on all of the inputs into the core logic and on all of the outputs from the core logic. The TAP controller manipulates both the input and the output BSCs. This allows the capability to drive inputs and capture outputs or vice versa. The pause states are included so that the shifting of data can be temporarily stopped.

When power is applied to the device, the TAP controller is forced into the Test Logic Reset state and the IDCODE register is initialized. Note that from any state position in the state machine, five consecutive ones on the TMS pin will reset the logic without the use of the optional TRST* pin. If standard four-pin JTAG is desired, tie the TRST* pin high. To disable the JTAG circuitry entirely, tie the TRST* pin low.

The second required element is an instruction register, or IR, which holds the instruction word. The instruction word length in a MACH device is six bits. The instruction decoder interprets the instruction word held in the IR. The instruction in the instruction register dictates which JTAG register acts as the data register being shifted and updated.

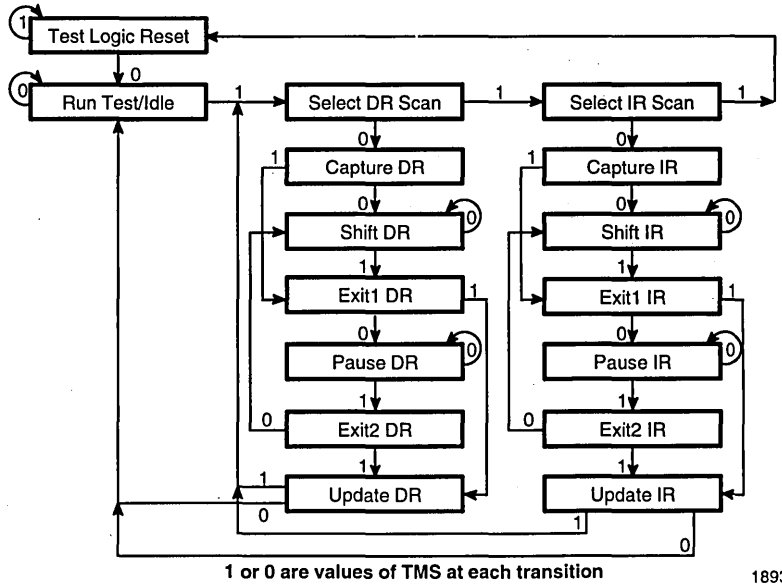


Figure 2. TAP Controller State Machine

The third element is the data registers, or DR, which could be the boundary-scan register, the IDCODE register, the USERCODE register, the row register, the column register, or the bypass register, depending on the individual instruction.

The registers illustrated in Figure 3 are part of the JTAG circuitry, with the exception of the row and column registers. The MACH device instruction register, as defined earlier, holds the six-bit instruction words. The Boundary-Scan Register is a term for the sum of all of the BSCs, so the size of this register varies with the size of the device. The IDCODE register is an optional register that contains a 32-bit word with three components: the manufacturer identification, the device identification, and the revision number. The USERCODE register is a user-specified, 32-bit word. The bypass register is a single shift register stage which provides a serial path between the TDI and TDO pins.

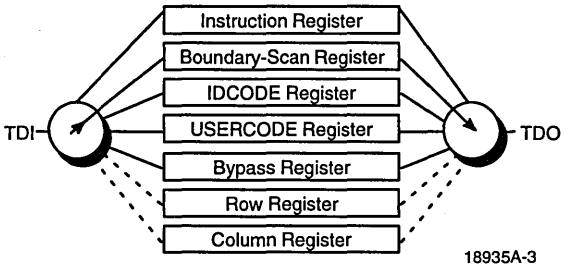


Figure 3. JTAG Instruction and Data Registers

The row and column registers implemented by AMD are not actually part of the JTAG standard but have been included here for educational purposes. The row register contains the row address when programming or verifying the device. The column register contains the column data during programming or verification.

JTAG Testing Procedure

The actual JTAG testing procedure will not be addressed in this application note. The purpose of this note is to introduce the concept of JTAG and the various components that comprise the feature. AMD does not directly support JTAG testing, however, there are a number of third-party vendors that specialize in JTAG testing hardware and software packages. These vendors include bed-of-nails manufactures such as GenRad and Teradyne, as well as exclusive JTAG testers manufactured by Texas Instruments and Corelis. A listing of presently available JTAG support contacts is provided at the end of this document.

FIVE-VOLT PROGRAMMING

Another benefit from the JTAG circuitry that AMD has derived is the ability to use the JTAG TAP for five-volt programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate Plastic Quad Flat Pack, or PQFP, leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially which is ideal for on-board programming since it only requires the use of the TAP, along with the additional ENABLE* pin.

The ENABLE* pin is used for extra programming security. If desired, the ENABLE* pin can be connected to ground, and the device programmed with only the TAP. If TRST* is not used in the system, it too, can be removed by connecting it to V_{CC}.

Programming is the process where MACH devices are loaded with a pattern defined in a JEDEC file obtained from MACHXL software or third-party software. Programming the MACH device after it has been placed on a circuit board is a relatively simple task. Programming is accomplished by initially placing the device into programming mode, using the MACHPRO programming software provided by AMD through MACHXL or third-party software. The device is initially bulk erased and the JEDEC file is then loaded. After the data is transferred into the device, the PROGRAM instruction is loaded and the ENABLE* pin is pulsed to complete the programming sequence. Further programming details can be found in the additional advanced application note.

On-Board Programming Options

Since the MACHPRO software performs these steps automatically, the following programming options are published for educational purposes.

The configuration file, which is also known as the chain file, defines the MACH device scan path. The file contains the information concerning which JEDEC file is to be placed into which device, the state which the outputs should be placed, and whether the security fuses should be programmed. The configuration file is discussed in detail in the MACHPRO software manual.

The state of the I/Os during programming can be controlled by preloading the boundary-scan cells at the I/Os into a known state or by disabling the Output Enable for each I/O giving the I/Os a high-impedance output. This preload value is obtained from the configuration file.

There are two optional security bits for the MACH devices. The first one is the program and verify security bit. Once this bit has been programmed, all of the programming and verification options are disabled until the device is erased. Programming the second bit also prohibits the option to preload and observe the macrocell registers of the device. This allows the user to protect proprietary patterns and designs.

Program verification of a MACH device involves reading back the programmed pattern and comparing it with the original JEDEC file. The AMD method of program verification performed on the MACH devices permits the verification of only one device at a time.

Accidental Programming or Erasure Protection

It is virtually impossible to program or erase a MACH device inadvertently. The following conditions must be met before programming actually takes place:

- The device must be in the password-protected program mode
- The programming or bulk erase instruction must be in the instruction register
- The ENABLE* pin must be low

If the above conditions are not met, the programming circuitry cannot be activated. Even if the device is in program mode with a programming instruction in the register, an internal pull-up resistor on the ENABLE* pin prevents any accidental pulses from occurring.

To ensure that the AMD ten year device data retention guarantee applies, the following programming conditions should be observed:

- 100 program/erase cycle limit should not be exceeded
- Programming should not be done above 35°C ambient

These devices cannot be reprogrammed instantaneously or "on the fly" if the ambient temperature is too high. The system ambient temperature should be cooled until at least 35°C ambient before in-system programming is initiated.

Programming Multiple MACH Devices

There will often be more than one JTAG-compatible MACH device in a circuit and these devices will be connected to form a scan path. The simplest scan path is when all JTAG-compatible devices have their TMS, TCK and TRST* pins connected in parallel. The TDI and TDO pins are connected serially, where the TDO of one device is connected to the TDI of the next device. The ENABLE* pins may be connected in parallel or remain separate for individual MACH device programming access. More complex scan paths could involve multiple TDI and TDO paths or multiple TMS paths. Multiple device programming does not imply multiple device verification since verification is performed one device at a time. The user specifies which devices in the scan path to program, and the MACHPRO software will program them.

Figure 4 illustrates a map of the scan path which contains each device and its position in the chain. Any device in a scan path which has not been selected for programming must be bypassed for the entire programming and program verification cycle. This is done by loading the appropriate instruction into the device any time new instructions are loaded. Additionally, the bypass register must be taken into account any time data is being shifted through the path.

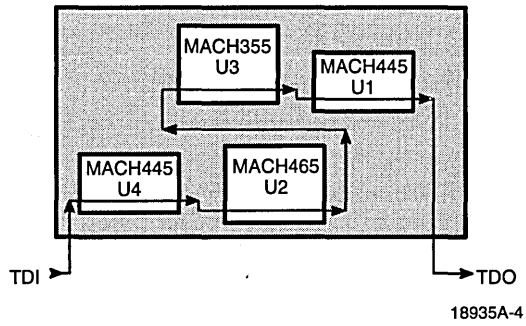


Figure 4. JTAG Scan-Path Map

The order in which program and program verification is completed is from the first device in the scan path to the last device in the chain.

Programming Hardware

The hardware interface for supporting both the JTAG and five-volt programming features requires six pins for the TAP and ENABLE* pins. Additional pins to accommodate power and ground, as well as specialized functions such as in-circuit reconfigurability and multiple scan path configurations, may be desirable.

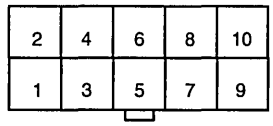
A parallel printer port of any IBM-compatible Personal Computer, or PC, is sufficient to interface with the target board containing the MACH devices. AMD supplies a cable that could be used to adequately program and test the MACH devices.

Some PC systems have software keys connected to the parallel port. Please remove these keys before using the supplied software.

The AMD cable contains the five required interface signals, plus the ENABLE* signal for programming and a ZCTL signal for advanced in-circuit configuration applications. If in-circuit reconfigurability is not required, ZCTL should be tied to ground. There is also a V_{CC} pin and two ground connections for signal integrity.

The target board cable connector is a 10 (5x2) pin female connector. The connector chosen by AMD is manufactured by Dupont and their connector number is 71602-010. The suggested target board male connector is Dupont number 71918-110 which is a 10-pin header with latches that allow for a quick disconnect. Figure 5

illustrates the cable header connector pinout locations. There is a locator key opposite of pin 5 for safety purposes.



Pin 1 - TCK Pin 2 - GND
Pin 3 - TMS Pin 4 - GND
Pin 5 - TDI Pin 6 - V_{CC}
Pin 7 - TDO Pin 8 - GND
Pin 9 - TRST* Pin 10 - ENABLE*

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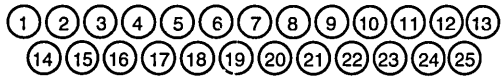
Figure 5. Board Header Cable Connector Pin Locations

The pin locations of the board header were chosen to minimize crosstalk between the wires in the ribbon cable. This header-pin configuration is supported by AMD, but individual applications may require an alternate header-pin arrangement. The AMD cable is six feet in length. If the distance from the user's computer to the target application is more than six feet, proper cable design rules should be followed in order to reliably program the MACH devices.

The connector for the computer end of the cable is a standard DB-25 male connector. The connections are illustrated in Figure 6.



Pin 1 - TRST* (STROBEB) Pin 2 - TCK (D0)
Pin 3 - TDI (D1) Pin 4 - TMS (D2)
Pin 11 - TDO (PRINTER_BUSY) Pin 12 - V_{CC} (PE)
Pin 17 - ENABLE* (ACT_SELB) Pin 23 - GND
Pin 24 - GND Pin 25 - GND

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Figure 6. Computer Port Cable Connector Pin Locations

A third-party programmer could also provide programming support for the MACH devices. The programmer also uses the AMD cable which plugs into a 28-pin socket on the programmer instead of the PC parallel port. An assortment of programmer manufacturers are listed at the end of this document.

There are a number of additional programming scenarios that could also be considered. Programming practices used while protyping could vary significantly from final production methods. A number of bed-of-nails tester vendors, including GenRad and Teradyne, support MACH device programming. Contact individual vendors listed at the end of this application note for more information.

Software Support Tools

AMD's MACHXL software includes support for programming MACH devices. This software is an easy to use tool that supports the design entry, fitting, and simulation of MACH device applications. Once the design has been completed, it may be downloaded to the MACH device through the programming operation.

The five-volt programming software in MACHXL software supports multiple MACH devices and allows the user to combine AMD MACH devices with other JTAG devices in a chain. A listing of third-party software support appears at the end of this note. The FusionPLD Catalog contains a complete list of available third-party software support.

Programming Procedure Overview

This section provides an overview of a typical programming procedure using the MACHPRO software. This assumes that the MACH devices are already placed on the board and are linked in a serial chain with the other JTAG devices. Additional details of the programming process are available in the MACHXL software documentation as well as in the advanced application note.

Initially, the JEDEC files for the MACH devices to be programmed are generated using MACHXL or other third-party tools. Next, a serial chain description file, listing the JTAG devices in the chain and the actions to be performed on each device, is written. Then, the target board is connected to a power supply and the JTAG programming cable is attached to both the PC parallel port and the board. Finally, after the target board supply is switched on, the MACHPRO software with the associated chain file is used to program the MACH devices.

Please refer to the MACHPRO software manual for more information on writing a chain description file.

Boundary Scan Description Language File

The Boundary Scan Description Language, or BSDL, file describes the pinout of an IC. The file also describes the instruction codes and layout of the boundary-scan cells. The file does not describe the JTAG scan path. The MACHXL software creates the BSDL file from the JEDEC file.

The BSDL file declares TAP pin locations, instruction codes, register length/structure, device ID code, and whether there is a TRST* pin. To test a JTAG board, a

collection of all of the BSDL files for the JTAG ICs is required along with a netlist describing how these ICs are connected.

Additional information on BSDL files may be obtained from the Suggested Reading section.

SUGGESTED READING

IEEE Standard 1149.1-1990

IEEE Standard 1149.1-1990 Supplement A

The Boundary-Scan Handbook by Kenneth Parker

Meeting the Challenge of Boundary Scan by GenRad

Preliminary JTAG and/or Programming Support for MACH Devices

Manufacturer	Bed-of-Nails Tester Tools
GenRad 300 Baker Avenue Concord, MA 01742 508-369-4400	Model 2272
Teradyne 179 Lincoln Street Boston, MA 617-422-3567	Victory Software
Hewlett Packard Loveland, CO 80539	3070 Series

Manufacturer	JTAG Analyzer
Corelis 12607 Hidden Creek Way Suite H Cerritos, CA 90701 310-926-6727	SCANIO/280 SCANTEST Software
Texas Instruments P.O. Box 869305 Plano, TX 75086 214-575-6396	Asset

Manufacturer	Software Development System
Advanced Micro Devices P.O. Box 3453 Sunnyvale. CA 94086 (800) 222-9323	MACHXL
Data I/O 10525 Willows Road N.E P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL5
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155	PLDesigner

Manufacturer	Programmer Support
BP Microsystems 1000 N. Post Rd. Houston, TX 77055-7237 (800) 225-2102 or (713)688-4600	BP1200
Data I/O 10525 Wiilows Road N.E P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	UniSite Model 3900 AutoSite
System General 510 S. Park Victoria Dr. Milpitas, CA 95035 (408) 263-6667	Turpro-1

Advanced In-circuit Programming Guidelines for MACH 3 and 4 Devices

Advanced Micro Devices

Application Note

by Kenneth Cuy, Applications Engineer, Programmable Logic Division and David Stoenner, Member of the Technical Staff, Field Applications

INTRODUCTION

This application note serves as a guideline for using the JTAG interface on selected MACH 3 and 4 devices to perform in-circuit programming via a microcontroller. Although this application note will concentrate on an in-circuit programming example with an AMD Am29240™ RISC microcontroller, the information contained within can be extended to other such applications.

An additional application note entitled *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* is available to provide the basic knowledge required to understand the topics of JTAG and five-volt, on-board programming.

System Configuration

The parallel port of a standard PC was chosen as the initial tool to interface with the JTAG port for programming control. The ubiquitous availability of PCs provide a universal development environment for the MACH 3 and 4 devices that support JTAG.

The standard parallel port on a PC is composed of two register addresses in the I/O space of the PC. The two ports are the data port and the control port. The control port consists of two signals; Control which writes to the address and Status which reads to the address.

The six JTAG lines were placed on the parallel port in the following manner. TMS, TCLK and TDI are positive true, output only lines and thus were chosen to be put on the data port. As a convenience for the programmer, the data port is a positive true interface. TRST* and ENABLE* are negative true, output only lines and thus were chosen to be put on the control port. Besides being a negative true interface, the control port is always reset to a known value on power-up. TRST* and ENABLE* were selected to be Strobe and Printer Initiate signals respectively.

The only input needed is for TDO, which was selected as input on the Status Register bit D7, the Printer Busy bit.

The interfacing PAL device, that is used for in-circuit programming, was developed to mimic the parallel port, except that only the bits needed were implemented. This allows the entire control to be put in one PAL device for simplicity, cost, and board space considerations. The example design uses a PALCE22V10 to implement the in-circuit programmability interface for the 29240 microprocessor. The design file for the 22V10 is included in Appendix A.

Interfacing PAL Device

The PALCE22V10 contained in the file JTAG.V10 has been designed to look like a standard microprocessor peripheral using a Chip Select ($\overline{CS}$), I/O Read ($\overline{RD}$), I/O Write ($\overline{WR}$) and A0. The 22V10 is composed of two sections, one to support the data port and the other to support the control and status port. The A1 bit is used in the Am29240. A higher order chip select (PIACS0) is provided with A23–A0. This allows the chip select to occupy 16 megabytes of address space. A1 is used in the equations so the MACH device can be accessed independent of the JTAG controller.

In the Am29240, the two registers (normally byte oriented) are configured on word (32 bit) boundaries for both the Am29240 hardware and the C software. Therefore, the A0 bit in the JTAG.V10 design is connected to the Am29240 address bit A2, and A1 in the 22V10 is connected to A3 of the Am29240.

The PALCE22V10 has only one clock input (pin 1) which can be used to clock any of the macrocells within the PALCE22V10. However, two registers in the design require different clocks. To solve this problem, the clock pin is used to clock the data register and the control register is implemented as transparent latches arranged in a master/slave configuration. The equation WR_CLK is used to generate the clock for the data register and is externally looped back to pin 1. The equation for WR_CLK is simply the chip select ANDED with I/O write at the correct address. D0, D1 and D2 are then registered into TDI, TCLK and TMS respectively. This is the same bit order that is used in the PC printer port configuration. These outputs are controlled by the term TRI_DISABLE which in turn is controlled by the parallel port cable. If the cable is plugged in then the outputs of the PALCE22V10 are disabled to prevent output contention. This arrangement can even be used in a manufacturing system for both development as well as in field updates.

The TRST* signal is generated from a reset input as well as the master latch called TRST_LAT. The input pin RESET will not only reset all the registers and latches but will also enable TRST* on the interface to reset the JTAG state machine in the selected MACH 3 or 4 device. In the design file, the latch equations are surrounded by MINIMIZE_OFF and MINIMIZE_ON. This is done because of the cross terms in the latch equations

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that are necessary to hold the output stable as the latch enable term goes false.

The slave latches are controlled only by chip select (CS) so any activity with the interfacing PAL device will hold TRST* and ENABLE* stable.

The remainder of the PALCE22V10 design is very straight forward in its implementation and can be followed in the design file.

System Dependent Source Code

The software written for the Am29240 interface consists of a group of low level drivers written in pseudo ANSI C for the 29K™ family and is included in Appendix B. These drivers are the only ones that change from system to system. If a different interface was chosen for the JTAG port, these drivers are all that is needed to be re-written for the target system. These drivers are written so that they can directly interface to the C compiler for the 29K family and adhere to the 29K calling convention.

Please contact your local sales office for details on a supplement entitled *MACHPRO™ Downloading Software: C Source Code* which contains the C source code for AMD's MACHPRO programming software. MACHPRO uses the JTAG circuitry on selected MACH devices to program and verify the devices via the PC parallel port. The required drivers listed below need to be integrated with the existing MACHPRO software so that programming may now be performed via a microcontroller.

Required Drivers

Listed below are all of the low level drivers necessary to implement in-circuit programming with the selected JTAG compatible MACH devices. An effort was made to keep the drivers simple and easy to embed for the user.

- _JTAG_reset_interface()

  This routine is called at the beginning of the main program and establishes the JTAG interface to a known state.

  This state is:

ENABLE*	FALSE (Logic High)
TRST*	FALSE (Logic High)
TMS	FALSE (Logic Low)
TCLK	TRUE (Logic High)
TDI	FALSE (Logic Low)

- _JTAG_reset()

  This routine will pulse the TRST* pin for a reset pulse

- _JTAG_pgm_pulse(pulse_width)

  This routine will pulse the ENABLE* pin for the duration of the input variable pulse_width in milliseconds. For the 29K there is a system call to the Host Interface (HIF) that will return a clock with a resolution of 1 millisecond. So this routine will set the ENABLE* pin true and then call the clock routine once to establish a starting time and then it will loop calling the clock routine again until the correct time has elapsed. It will then set the ENABLE* pin false and return.

- _JTAG_pgm_set(value)

  This routine will set the ENABLE* pin to the value specified in the D3 bit position of the input variable.

- _JTAG_shift(TDI_value, TMS_value)

  This routine will shift out one bit on to the TDI line and at the end will read the TDO input and return this value. The routine will first set TCLK low, TDI to the value specified in the TDI_value variable and TMS to the value specified in the TMS_value variable. Then the TCLK pin will be set high and then set low and the D7 bit will be read and right justified in the return register.

- _setup()

  This routine simply sets up the PIA port of the Am29240 for 3 clock cycle wait state operation. This is also compatible with the Am29200™.

REFERENCES

Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices

MACH 3 and 4 Family Data Book

MACHPRO™ Programming Software Manual

Am29240™, Am29245™, and Am29243™ RISC Microcontrollers User's Manual and Data Sheet

IEEE Standard 1149.1–1990

IEEE Standard 1149.1–1990 Supplement A

APPENDIX

A PALASM DESIGN FILES

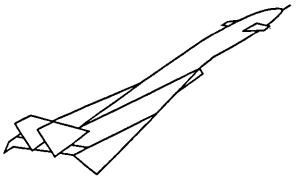
```
;PALASM Design Description

;---------------------------------- Declaration Segment ------------

TITLE    JTAG CONTROL PAL FOR MACH 3XX AND MACH4XX PAL FAMILY
PATTERN  JTAG.V10
REVISION A
AUTHOR   DAVID STOENNER
COMPANY  ADVANCED MICRO DEVICES

DATE     06/21/93

CHIP  _jtag  PAL22V10

;---------------------------------- PIN Declarations ---------------

PIN  1          CLK                                                 ;
PIN  2          /CS                                                 ;
PIN  3          /RD                                                 ;
PIN  4          /WR                                                 ;
PIN  5          A0                                                  ;
PIN  6          A1                                                  ;
PIN  7          D0                                                  ;
PIN  8          D1                                                  ;
PIN  9          D2                                                  ;
PIN  10         D3                                                  ;
PIN  11         /RESET                                              ;
PIN  12         GND                                                 ;
PIN  13         /TRI_DISABLE                                        ;
PIN  14         D7                                                  ;
PIN  15         /PRM_EN                                             ;
PIN  16         TRST_LAT                                            ;
PIN  17         PRM_EN_LAT                                          ;
PIN  18         /TRST                                               ;
PIN  19         TDO                                                 ;
PIN  20         TDI                                                 ;
PIN  21         TMS                                                 ;
PIN  22         TCLK                                                ;
PIN  23         /WR_CLK                                             ;
PIN  24         VCC                                                 ;
NODE 1          GLOBAL                                              ;

;---------------------------------- Boolean Equation Segment ------

EQUATIONS

GLOBAL.RSTF = RESET

MINIMIZE_OFF
```

```
TRST =   RESET
       + TRST_LAT*/CS*/RESET
       + TRST*TRST_LAT*/RESET
       + TRST*CS*/RESET

PRM_EN =    PRM_EN_LAT*/CS*/RESET
          + PRM_EN*PRM_EN_LAT
          + PRM_EN*CS*/RESET

TRST_LAT =   CS*WR*A0*D0*/A1*/RESET
           + TRST_LAT*/(CS*WR*A0*/A1)*/RESET
           + TRST_LAT*D0*/RESET

PRM_EN_LAT =   CS*WR*A0*/A1*D3*/RESET
             + PRM_EN_LAT*/(CS*WR*A0*/A1)*/RESET
             + PRM_EN_LAT*D3*/RESET

MINIMIZE_ON

WR_CLK = CS*WR*/A0*/A1*/RESET

; NOTE PIN 23 ( WR_CLK ) IS EXTERNALLY CONNECTED TO PIN 1 ( CLK ) FOR

; THE CLOCKED REGISTER.

TDI := D0

TCLK := D1

TMS := D2

D7 = TDO

D7.TRST = CS*RD*/A1*A0*/RESET

TRST.TRST = /TRI_DISABLE*/RESET

TDI.TRST = /TRI_DISABLE*/RESET

TCLK.TRST = /TRI_DISABLE*/RESET

PRM_EN.TRST = /TRI_DISABLE*/RESET

;-------------------------------------------------------------------
```

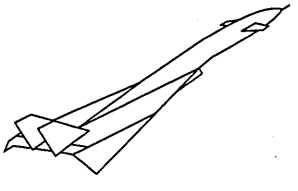
```
    pragma On(Pointers_compatible_with_ints);

    volatile int *Data_Reg ;
    volatile int *Command_Reg ;
    volatile int *Status_Reg ;
    volatile int *PIA_Control;

#define     TRST        0x1
#define     PGM_EN      0x8
#define     TDI         0x1
#define     TCLK        0x2
#define     TMS         0x4

extern clock();

void JTAG_reset_interface()

/* We will give the interface a reset pulse and then do 5 TCLK with TMS
   = 1 which will reset the state machine to reset if the reset pulse
   did not work. It will then leave the interface with the command
   register = 0 and the data register = tclk = 0 tdi = 0 and tms = 1. */

{

    *Command_Reg = TRST;
    *Command_Reg = 0;
    *Data_Reg = TMS;
    *Data_Reg = TMS | TCLK;
    *Data_Reg = TMS;
    *Data_Reg = TMS | TCLK;
    *Data_Reg = TMS;
    *Data_Reg = TMS | TCLK;
    *Data_Reg = TMS;
    *Data_Reg = TMS | TCLK;
    *Data_Reg = TMS;
    *Data_Reg = TMS | TCLK;
    *Data_Reg = TMS;

    return;

}

void JTAG_reset()

{

    *Command_Reg = TRST;
    *Command_Reg = 0;

    return;

}

void JTAG_pgm_pulse(w)

    int w;
```

```
{
    int start;

/* Now that the program enable is on we will start the timeout in
   milliseconds for the pulse width.  A system call to clock ( HIF
   service call 273 ) will return the time in milliseconds in gr96, so
   we will just do a compare to the pulse width value and loop till the
   time has passed. */

    start = clock();
    *Command_Reg = PGM_EN;

/* now do another system clock call and start the timeout loop */

    while(clock()-start < w){;}
    *Command_Reg=0;

   return;

}

void JTAG_pgm_set(in)

int in;

{

    *Command_Reg = (in & 0x1)<<3;

    return;

}

int JTAG_shift(tdi,tms)

    int tms,tdi;

{

    int temp;
   temp = ( tms & 1 ) << 2 | ( tdi & 1 );
    *Data_Reg = temp;
    *Data_Reg = temp | TCLK;
    *Data_Reg = temp;
    return(( *Status_Reg & 0x80 ) >> 7 );

}

void setup()

/* This routine sets up the PIA controller on the 292XX microcontroller
   to the needed values. For any race conditions we will set the IO
   extend bit and make the interface 3 wait states so that both the
   29200 and 29240 behave identical. This port is at 0x80000020. We will
   only affect PIACS0 so we will leave the other set up as is. */
{

    Data_Reg = 0x90000000;
    Command_Reg = 0x90000004;
    Status_Reg = 0x90000004;
    PIA_Control = 0x80000020;
    *PIA_Control = ( *PIA_Control & 0x00ffffff ) | 0x83<<24;

    return;
}
```

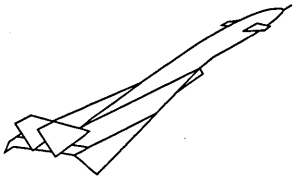
Notes



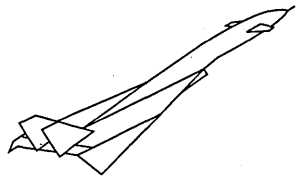
Notes



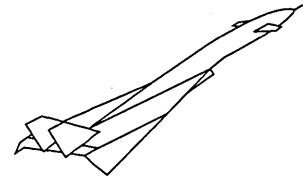
Notes



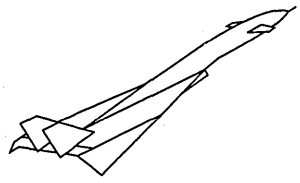
Notes



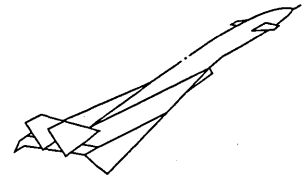
Notes



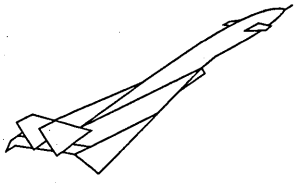
Notes



Notes



Notes



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