AMI.
MOS Products Catalogue
Winter 1979

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MOS/LSI is the Business of AMI

...and MOS/LSI is AMI's only business. The first company to produce commercial quantities of MOS circuits starting in 1966, AMI has ever since been among the leaders in circuit design, process technology and new product and market development. Today, the company is a major producer of standard products for the electronic data processing, telecommunications, and consumer product industries.

DESIGN EXPERIENCE — Many areas of applications in which MOS is used today were pioneered with an AMI-designed device. This accumulated experience results in a line of high performance standard products and imaginatively designed, cost-effective custom circuits.

PROCESS VERSATILITY — AMI's head start in the industry gives it a mature capability in every one of the major production processes: P-channel — high voltage and ion implanted metal gate, and silicon gate; N-channel — silicon gate, ion implanted silicon gate with depletion loads, high density and narrow geometry "H" MOS; and CMOS — metal and silicon gate, and high density, isoplanar silicon gate. AMI's new patented process, VMOS, is already producing high speed, low power state-of-the-art memory products.

PRODUCTION CAPABILITY — AMI has three major facilities worldwide. Headquarters in Santa Clara, California has 327,000 square feet of office and manufacturing space and about 1,000 employees. Administration, R&D, the majority of the engineering staff, one of the company's two wafer fabrication facilities, pilot assembly and a final test facility are located there. The other major fabrication facility is at Pocatello, Idaho with 103,000 square feet and about 600 employees. The plant includes an engineering group, four fabricating lines and some final test activity. Located at Inchon, Korea is KMI, the company's major circuit assembly plant. It covers 116,000 square feet, employs about 1,300 persons. This combination of facilities can produce over 2,000,000 LSI circuits per month using the latest production equipment to maximize yields in today's more complex circuits.

PRODUCT RELIABILITY — By designing reliability into the product — a standard procedure for AMI, the most experienced designer of custom MOS circuits — problems are minimized or eliminated. Process control (and we run more processes than any other MOS manufacturer) is the second most important step in maintaining our reputation for reliability. Design and process control are buttressed by a closed feedback loop that continually collects AMI internal data and field data from our customers to analyze and solve design, layout and process problems. These activities are further supported by accelerated tests to determine failure rates and the activation energies for observed failure modes.

IT'S STANDARD AT AMI — The company's dedication to the design and manufacture of high performance MOS/LSI products is reflected in the variety of products listed in this catalog.

AMI and Made-to-Order MOS

Since 1966, AMI has designed and manufactured over 1,000 custom MOS circuits. The largest design engineering staff in the industry has helped to keep AMI in the number one position among custom MOS producers.

If your product can be controlled by an MOS circuit, and you plan to manufacture it in high volume, you should contact your nearest AMI Sales Office or the main office in Santa Clara, California. AMI will be happy to discuss the possibility of designing a custom circuit for your application, or manufacturing such a circuit from your tooling.

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AMI Sales Offices

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Domestic Reps

International Reps

Ordering Information

Packaging

Terms of Sale

Product Assurance Program

MOS Processes

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Any product in this MOS Products Catalog can be ordered using the simple system described below. With this system it is possible to completely specify any standard device in this catalog in a manner that is compatible with AMI's order processing methods. The example below shows how this ordering system works and will help you to order your parts in a manner that can be expedited rapidly and accurately.

All orders (except those in sample quantities) are normally shipped in plastic carriers or aluminum tube containers, which protect the devices from static electricity damage under all normal handling conditions. Either container is compatible with standard automatic IC handling equipment.

Any device described in this catalog is an AMI Standard Product. However, ROM devices that require mask preparation or programming to the requirements of a particular user, devices that must be tested to other than AMI Quality Assurance standard procedures, or other devices requiring special masks are sold on a negotiated price basis.

$$S\ 6\ 8\ 2\ 1\ A\ -\ 1\ P$$

Device Number — prefix S, followed by four (or five*) numeric digits that define the basic device type. If there are versions to the basic device, the numeric digits will be followed by additional alphanumeric digits, in this example A-1. The last digit should always be followed by a space.

*Organ Circuits

Package Type — a single letter designation which identifies the basic package type. The letters are coded as follows:

P — Plastic package

E — Cer-DIP package

S — SLAM package

C — Ceramic (three-layer) package

T — TO type package

PLASTIC PACKAGE

The AMI plastic dual-in-line package is the equivalent of the widely accepted industry standard, refined by AMI for MOS/LSI applications. The package consists of a plastic body, transfer-molded directly onto the assembled lead frame and die. The lead frame is Kovar or Alloy 42, with external pins tin plated. Internally, there is a 50μin. gold spot on the die attach pad and on each bonding fingertip. Gold bonding wire is attached with the thermocompression gold ball bonding technique.

Materials of the lead frame, the package body, and the die attach are all closely matched in thermal expansion coefficients, to provide optimum response to various thermal conditions. During manufacture every step of the process is rigorously monitored to assure maximum quality of the AMI plastic package.

Avaliable in: 8, 14, 16, 18, 22, 24, 28 and 40 pin configurations.

GOLD BONDING WIRE
GOLD PLATING
BODY
LEAD FRAME
SEALANT
TIN PLATING
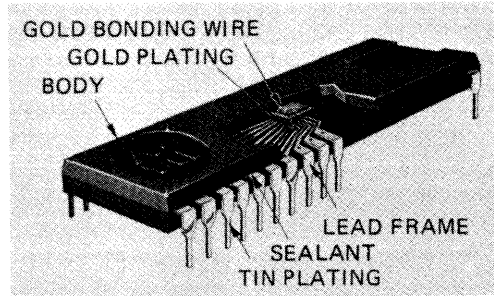
Cer-DIP PACKAGE

The Cer-DIP dual-in-line package has the same high performance characteristics as the standard three-layer ceramic package, yet approaches plastic in cost. It is a military approved type package, with excellent reliability characteristics. Although the Cer-DIP concept has been around for a number of years, AMI leads the technology with this package, having eliminated the device instability and corrosion problems of earlier Cer-DIP processes.

The package consists of an Alumina (Al_2O_3) base and the same material lid, hermetically fused onto the base with low temperature solder glass. Inert gasses are sealed inside the die cavity.

Available in: 16, 18, 22, 24, 28 and 40 pin configurations.

1. ALUMINUM WIRE TO DIE
2. GOLD WIRE BETWEEN GROUND BOND AND CAVITY METALLIZATION
ALUMINUM METALLIZATION ON BONDING FINGERS
96% ALUMINA LID
CORNING 7583 SOLDER GLASS
96% ALUMINA BASE
42 NICKEL-IRON ALLOY LEAD FRAME PLATED 200 MICROINCHES ELECTRONIC GRADE & TIN
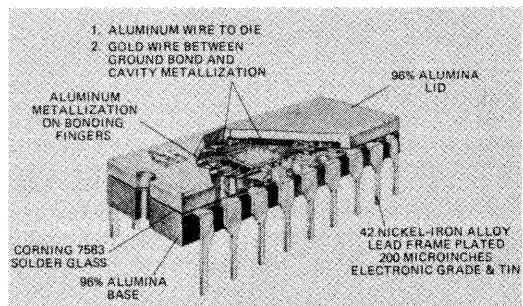
SLAM PACKAGE

The SLAM (single layer metallization) dual-in-line package is an AMI innovation that offers a lower cost alternative to three-layer ceramic packages, without sacrifice of performance or reliability.

The SLAM package uses the same basic materials as ceramic, but is constructed in a simpler and thereby more reliable manner. It uses a 96% Alumina base, one basic refractory metallization layer, coated with an Alumina passivation layer, and brazed-on Kovar leads. The leads are suitable for either socket insertion or soldering. Either a ceramic or a Kovar lid is used to hermetically seal the package. The ceramic lid is attached with an epoxy resin sealant, but a gold-silicon eutectic solder is used for Kovar lids.

Avaliable in: various 14 to 40 pin configurations.
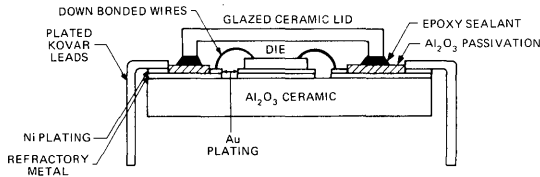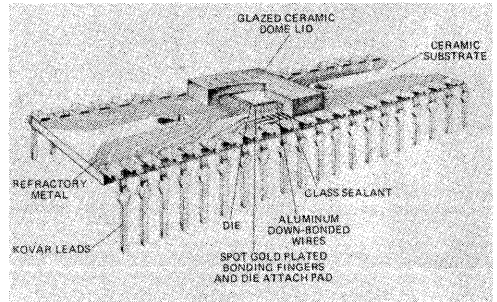
EPOXY SEAL PACKAGE

CERAMIC PACKAGE

Industry standard high performance, high reliability package, made of three layers of Al_2O_3 ceramic and nickel-plated refractory metal. Either a low temperature glass sealed ceramic lid or a gold tin **eutectic** sealer Kovar lid is used to form the hermetic cavity of this package. Package leads are available with gold over nickle or tin plating for socket insertion or soldering.
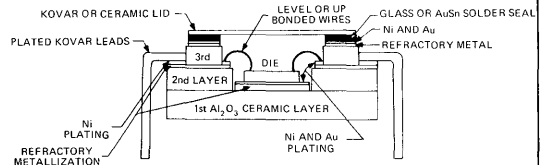
8-PIN PLASTIC
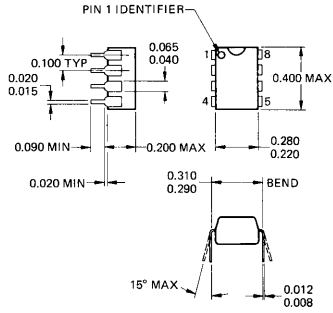
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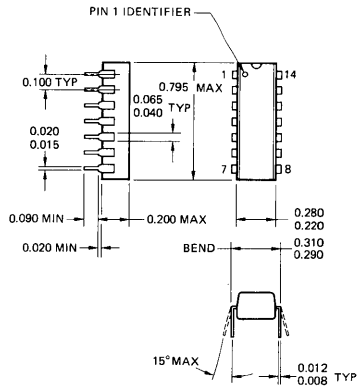
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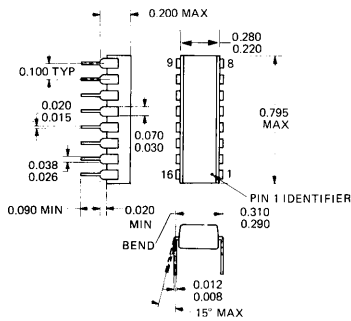
16-PIN Cer-DIP
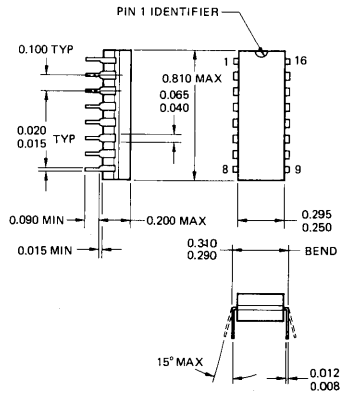
16-PIN CERAMIC
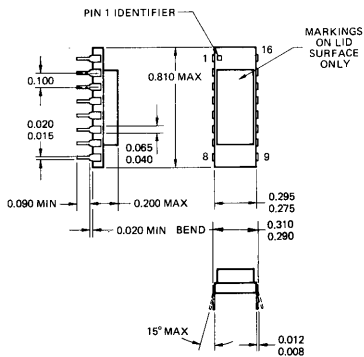
18-PIN PLASTIC

18-PIN CERAMIC

PIN 1 IDENTIFIER

MARKINGS
ON LID
SURFACE
ONLY

0.100

0.920 MAX

0.065
0.040

0.020
0.015

0.090 MIN — 0.200 MAX

0.295
0.275

0.020 MIN

0.310
0.290

15° MAX

0.012
0.008

18-PIN Cer-DIP

PIN 1 IDENTIFIER

0.100

0.920 MAX

0.065
0.040

0.020
0.015

0.090 MIN — 0.200 MAX

0.295
0.250

0.020 MIN BEND

0.310
0.290

15° MAX

0.012
0.008

22-PIN PLASTIC

PIN 1 IDENTIFIER

0.100

1.130 MAX

0.065
0.040

0.020
0.015

0.090 MIN — 0.200 MAX

0.380
0.320

0.020 MIN BEND

0.410
0.390

15° MAX

0.012
0.008

22-PIN Cer-DIP

PIN 1 IDENTIFIER

0.100

1.110 MAX

0.065
0.040

0.020
0.015

0.090 MIN — 0.200 MAX

0.395
0.355

0.015 MIN BEND

0.410
0.390

15° MAX

0.012
0.008

22-PIN CERAMIC

PIN 1 IDENTIFIER

MARKINGS
ON LID
SURFACE
ONLY

0.100

1.120 MAX

0.065
0.040

0.020
0.015

0.090 MIN — 0.200 MAX

0.395
0.375

0.020 MIN

0.410
0.390

15° MAX

0.012
0.008

24-PIN PLASTIC

PIN 1 IDENTIFIER

0.100

1.270 MAX

0.065
0.040

0.020
0.016

0.090 MIN — 0.200 MAX

0.580
0.515

0.020 MIN BEND

0.610
0.590

15° MAX

0.012
0.008

24-PIN Cer-DIP

PIN 1 IDENTIFIER

1   24

1.310 MAX

0.100
0.065
0.040
0.020
0.015

.12   13

0.090 MIN   0.200 MAX   0.590
0.480
0.015 MIN   BEND   0.610
0.590

15° MAX   0.012
0.008

24-PIN SLAM

PIN 1 IDENTIFIER

1   24

1.310 MAX

0.100
0.065
0.040
0.020
0.015

12   13

0.090 MIN   0.200 MAX   0.580
0.480
0.020 MIN   BEND   0.610
0.590

15° MAX   0.012
0.008

24-PIN CERAMIC

PIN 1 IDENTIFIER

1   24

MARKINGS
ON LID
SURFACE
ONLY

0.100
1.310 MAX

0.065
0.040
0.020
0.015

12   13

0.090 MIN   0.200 MAX   0.595
0.575
0.020 MIN   0.610
0.590

15° MAX   0.012
0.008

87696

28-PIN PLASTIC

PIN 1 IDENTIFIER

1   28

1.450 MAX

0.100
0.065
0.040
0.020
0.015

14   15

0.090 MIN   0.200 MAX   0.585
0.515
0.020 MIN   BEND   0.610
0.590

15° MAX   0.012
0.008

28-PIN Cer-DIP

PIN 1 IDENTIFIER

1   28

1.520

0.100
0.065
0.040
0.020
0.015

14   15

0.090 MIN   0.590
0.480
0.015 MIN   0.200 MAX   0.610
0.590   BEND

15° MAX   0.012
0.008

40-PIN PLASTIC

PIN 1 IDENTIFIER

1   40

2.060 MAX

0.100
0.065
0.040
0.020
0.015

20   21

0.090 MIN   0.580
0.515
0.020 MIN   0.200 MAX   0.610
0.590   BEND

15° MAX   0.012
0.008

40-PIN SLAM

40-PIN CERAMIC
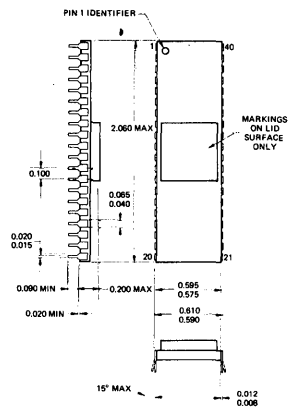
40-PIN CER-DIP

64-PIN CERAMIC

NOTE A. Each pin centerline is located within 0.010 of its true longitudinal position.
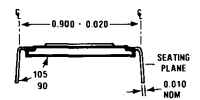
1. **ACCEPTANCE:** THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items described above and acknowledged hereby are firm and not subject to audit, price revision, or price redetermination.

2. **PAYMENT:**
   (a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.
   (b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.
   (c) Each shipment shall be considered a separate and independent transaction, and payment therefor shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. **TAXES:** Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority, (national, state, local or other) applicable to the products covered by this order, or the manufacturer or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, Railway Express, Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. **DELIVERY:** Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lock-outs, slow-downs, shortages, factory or labor conditions, errors in manufacture, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such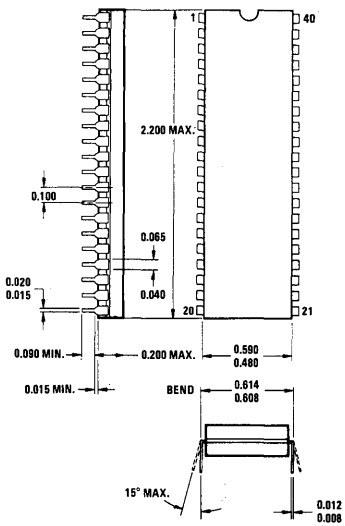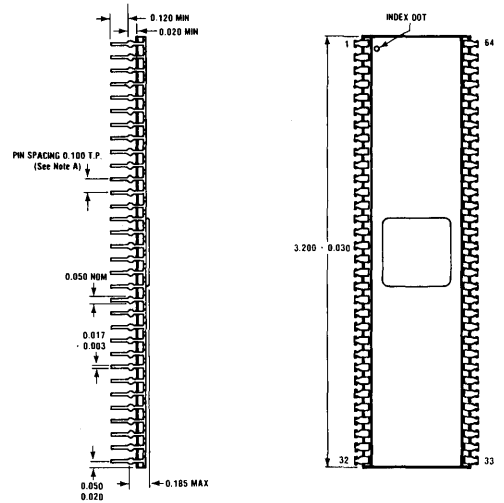 delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

   In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

   Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined; the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. **INSPECTION:** Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. **WARRANTY:** The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

   It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. **GENERAL:**
   (a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.
   (b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.
   (c) In no event shall Seller be liable for consequential or special damages.
   (d) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.
   (e) Except to the extent provided in Paragraph 10, below, this order is not subject to cancellation or termination for convenience.
   (f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities, domestic or foreign.
   (g) In the event that the cost of the products are increased as a result of increases in materials, labor costs, or duties, Seller may raise the price of the products to cover the cost increases.
   (h) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

10. **GOVERNMENT CONTRACT PROVISIONS:** If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Armed Services Procurement Regulation are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be — i.e., "Contracting Officer" shall mean "Buyer", "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

    7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Rhodesia and Certain Communist Areas; 7-103.16, Contract Work Hours and Safety Standards Act — Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity Clause; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government (only to the extent that Buyer's contract is terminated for the convenience of the government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-103.24, Responsibility for Inspection; 7-103.25, Commercial Bills of Lading Covering Shipments Under FOB Origin Contracts; 7-103.27, Listing of Employment Openings; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.15, Examination of Records by Comptroller General; 7-104.20, Utilization of Labor Surplus Area Concerns.

Product Assurance Program

INTRODUCTION

Quality is one of the most used, least understood, and variously defined assets of the semiconductor industry. At AMI we have always known just how important effective quality assurance, quality control, and reliability monitoring are in the ability to deliver a repeatably reliable product. Particularly, through the manufacture of custom MOS/LSI, experience has proved that one of the most important tasks of quality assurance is the effective control and monitoring of manufacturing processes. Such control and monitoring has a twofold purpose: to assure a consistently good product, and to assure that the product can be manufactured at a later date with the same degree of reliability.

To effectively achieve these objectives, AMI has developed a Product Assurance Program consisting of three major functions:

- Quality Control
- Quality Assurance
- Reliability

Each function has a different area of concern, but all share the responsibility for a reliable product.

The AMI Product Assurance Program

The program is based on MIL-STD-883, MIL-M-38510, and MIL-Q-9858A methods. Under this program, AMI manufactures highest quality MOS devices for all segments of the commercial and industrial market and, under special adaptations of the basic program, also manufactures high reliability devices to full military specifications for specific customers.

The three aspects of the AMI Product Assurance Program — Quality Control, Quality Assurance, and Reliability — have been developed as a result of many years of experience in MOS device design and manufacture.

Quality Control establishes that every method meets, or fails to meet, product parameters — *QA checks results.*

Quality Control establishes that every method meest, or fails to meet, processing or production standards — *QC checks methods.*

Reliability establishes that QA and QC are effective — *Reliability checks device performance.*

One indication that the AMI Product Assurance Program has been effective, is that NASA has endorsed AMI products for flight quality hardware since 1967. The Lunar Landers and Mars Landers all have incorporated AMI circuits, and AMI circuits have also been utilized in the Viking and Vinson programs, as well as many other military airborne and reconnaissance hardware programs.

QUALITY CONTROL

The Quality Control function in AMI's Product Assurance Program involves constant monitoring of all aspects of materials and production, starting with the raw materials purchased, through all processing steps, to device shipment. There are three major areas of Quality Control:

- Incoming Materials Control
- Microlithography Control
- Process/Assembly Control

Incoming Materials Control

All purchased materials, including raw silicon, are checked carefully to various test and sampling plans. The purpose of incoming materials inspection is to ensure that all items required for the production of AMI MOS circuits meet such standards as are required for the production of high quality, high reliability devices.

Incoming inspection is performed to specifications agreed to by suppliers of all materials. The Quality Control group continuously analyzes supplier performance, performs comparative analysis of different suppliers, and qualifies the suppliers.

Tests are performed on all direct material, including packages, wire, lids, eutectics, and lead frames. These tests are performed using a basic sampling plan in accordance with MIL-S-19500, generally to a Lot Tolerance Percent Defective (LTPD) level of 10%. The AQL must be below 1% overall.

Two incoming material inspection sequences illustrate the thoroughness of AMI Quality Control:

- Purchased packages are first inspected visually. Then, dimensional inspections are performed, followed by a full functional inspection, which subjects the packages to an entire production run simulation. Finally, a full electrical evaluation is made, including checks of the insulation, resistance, and lead-to-lead isolation. A package lot which passes these tests to an acceptable LTPD level is accepted.

- Raw silicon must also pass visual and dimensional checks. In addition, a preferential etch quality inspection is performed. For this inspection, the underlayers of bulk silicon are examined for potential anomalies such as dislocation, slippage, or etch pits. Resistivity of the silicon is also tested.

Microlithography Control

Microlithography involves the processes which result in finished working plates, used for the fabrication of wafers. These processes are pattern or artwork generation, photoreduction, and the actual printing of the working plates.

Pattern generation now is the most common practice at AMI. The circuit layout is digitized and stored on a tape, which then is read into an automated pattern generator, which prints a highly accurate 10x reticle directly.

In cases where the more traditional method of artwork generation is used whether Rubylith, Gerber Plots, AMI generated or customer generated — the artwork is thoroughly inspected. It is checked for level-to-level registration and dimensional tolerances. Also, a close visual inspection of the workmanship is made. AMI artwork is usually produced at 200x magnification and must conform to stringent design rules, which have been developed over a period of years, as part of the process control requirements.

Acceptable artwork is photographically reduced to a 20x magnification, and then further to a 10x magnification. The resulting 10x reticles are then used for producing 1x masters. The masters undergo severe registration comparisons to a registration master and all dimensions are checked to insure that reductions have been precise. During this step, image and geometry are scrutinized for missing or faded portions and other possible photographic omissions.

For a typical P-channel silicon gate device, master sets are checked at all six geometry levels in various combinations against each other and against a proven master set. Allowable deviations within the die are limited to 0.5 micron, deviations within a plate are limited to 1 micron, and all plate deviations are considered cumulatively.

Upon successful completion of a device master set, it is released to manufacturing where the 1x plates are printed. A sample inspection is performed by manufacturing on each 30-plate lot and the entire lot is returned to Quality Control for final acceptance. Quality Control performs audits on each manufacturing inspector daily, by sample inspection techniques.

The plates can be rejected first by manufacturing, when the 30-plate lots are inspected, or by Quality Control when the lots are submitted for final acceptance. If either group rejects the plates, they are rescreened and then undergo the same inspection sequence. In the rescreening process, the plates undergo registration checks; visual checks for pin holes, protrusions, and faded or missing images, as well as all critical dimension checks.

Process Control

Once device production has started in manufacturing, AMI Quality Control becomes involved in one of the most important aspects of the Product Assurance Program — the analysis and monitoring of virtually all production processes, equipment, and devices.

Process controls are performed in the fabrication area, by the Quality Control Fabrication Group, to assure adherence to

specifications. This involves checks on operators, equipment and environment. Operators are tested for familiarity with equipment and adherence to procedure. Equipment is closely checked both through calibration and maintenance audits. Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possiblity of contamination or adverse effects due to temperature or humidity excesses.

Experience has proven that such close control of the operators, equipment, and environment is highly effective towards improved quality and increased yields.

In addition to the specification adherence activities of the QC Fabrication Group, a QC Laboratory performs constant process monitoring of virtually every step of all processes. Specimens are taken from all production steps and critically evaluated. Sampling frequency varies, depending on the process, but generally, oxidation, diffusion, masking, and evaporization are the most closely monitored steps.

Results are supplied both to manufacturing and engineering. When evidence of a problem occurs, QC provides recommendations for corrections and follows up the corrective action taken.

Optical inspections are performed at several steps; quality control limits are based on a 10% LTPD. The chart in Figure 1 shows process steps and process control points.

QUALITY ASSURANCE

The Quality Assurance function in the Product Assurance Program involves checking the ability of manufactured parts to meet specifications. In addition, the QA group also is responsible for calibration of all equipment, and for the maintenance of AMI internal product specifications, to assure that they are always in conformance with customer specifications, or other AMI specifications.

After devices undergo 100% testing in manufacturing, they are sent to Quality Assurance for acceptance. Lots are defined, and using the product specifications, sample sizes are determined, along with the types of tests to be performed and the test equipment to be used. Lots must pass QA testing either with an LTPD or 10%, or less, if the specification requires tighter limits.

Three types of tests are performed on the samples: visual/mechanical, parametric, and functional. All tests are performed both at room temperature and at elevated temperature. In addition, a number of other special temperature tests may be performed, if required by the specification. Generally, high temperature tests are at 125°C.

To perform the tests, QA uses AMI *PAFT* test systems, ROM test systems, Macrodata testers, Fairchild *Sentry* systems,

Figure 1. Flowchart of Product Assurance Program Implementation

INCOMING MATERIALS — QC INSPECTION

PHOTO SUPPORT QC INSPECTION — WAFER FAB — QC FAB INSPECTION QC LAB MONITORS

WAFER SORT — QC INSPECTION

PACKAGING QC INSPECTION — ASSEMBLY Scribe/Break 1st Optical Die Attach Bond 2nd Optical Seal — QC INSPECTIONS

ASSEMBLY ENVIRONMENTAL TESTING — QC INSPECTION

ELECTRICAL — MANUFACTURING

QA ACCEPTANCE Program Verification Visual/Mechanical Testing Functional Testing Parametric Testing Temperature Testing

MARK AND PACK

FINAL VISUAL — QA INSPECTION

PLANT CLEARANCE — QA INSPECTION

SHIP

Western Digital *Spartan* systems, *Impact* testers, and various bench test units. In special instances a part may also be tested in a real life environment, in the equipment which is to finally utilize it.

If a lot is rejected during QA testing, it is returned to the production source for an electrical rescreening. It is then returned to QA for acceptance, but is identified as a resubmitted lot. If it fails again, it is discarded and corrective action

in engineering is initiated. As evidence of the problem is detected, the parts may also be traced all the way back to the wafer run, to analyze the cause.

When a lot is acceptable, it is sent to packaging and then to finished goods. When parts are sent from finished goods, they are again checked by the QA group to a 10% LTPD, with visual/mechanical tests. Also, all supporting documentation for the parts is verified, including QA acceptance, special customer specifications, certificates of compliance, etc. Only after this last check are devices considered ready for plant clearance.

If there are customer returns, they are first sample tested by QA, to determine the cause of the return. (Many times an invalid customer test will incorrectly cause returns.) After QA evaluates all returns, they are sent to Reliability for failure analysis.

RELIABILITY

The Reliability function in the Product Assurance Program involves process qualification, device qualification, package qualification, reliability program qualification, and failure analysis. To perform these functions AMI Reliability group is organized into two major areas:

- Reliability Laboratory
- Failure Analysis

Reliability Laboratory

AMI Reliability Laboratory is responsible for the following functions:

- New Process Qualification
- Process Change Qualification
- Process Monitoring
- New Device Qualification
- Device Change Qualification
- New Package Qualification
- Device Monitoring
- Package Change Qualification
- Package Monitoring
- High Reliability Programs

There are various closely interrelated and interactive phases involved in the development of a new process, device, package, or reliability program. A process change may affect device performance, a device change may affect process repeatability, and a package change may affect both device performance and process repeatability. To be effective, the Reliability Laboratory must monitor and analyze all aspects of new or changed processes, devices, and packages. It must be determined what the final effect is on product reliability, and then evaluate the merits of the innovation or change.

Process Qualification

For example, AMI Research and Development group recommends a new process or process alteration when it feels that the change can result in product improvement. The Reliability Laboratory then performs appropriate environmental and electrical evaluations of new process. Typically, a special test vehicle, or "rel chip", generated by R&D during process development, is used to qualify the recommended new process or process change.

The rel chip is composed of circuit elements similar to those that may be required under worst-case circuit design conditions. The rel chip elements are standard for any given process, and thus allow precise comparisons between diffusion runs. The following is an example of what is included on a typical rel chip:

- A discrete inverter and an MOS capacitor
- A large P-N junction covered by an MOS capacitor
- A large P-N junction area (identical to the junction area above, but without the MOS capacitor)
- A large area MOS capacitor over substrate
- Several long contact strings with different contact geometries.
- Several long conductor geometries, which cross a series of eight deeply etched areas.

Each circuit element of a rel chip allows a specific test to be performed. As an example, the discrete inverter and MOS load device accommodate power life tests. As a consequence, any type of parameter drift can be observed. The MOS capacitor, covering the large P-N junction, can serve to indicate the presence of contamination in the oxide, under the oxide, or in the bulk silicon. If unusual drift is evidenced, the location of contamination can be determined through analysis of the additional MOS capacitor and the large P-N junction area. The metal conductor interconnecting contacts is useful for life testing under relatively high current conditions. It facilitates the detection of metal separation when moisture or other contaminants are present.

The conductors crossing deeply etched areas allow the checking of process control. Rather than depending upon optical inspection of metal quality, burned out areas caused by high currents are readily identified and provide a quantitative measure of metal quality.

If the Reliability Laboratory determines that a recommended new process or process change is viable for manufacturing purposes, further analysis is necessary to determine that production devices can be manufactured in high volume, in a repeatable and reliable manner.

Process Monitoring

In addition to process qualification, the Reliability group also conducts ongoing process monitoring programs. Once every 90 days each major production process is evaluated using rel chips as test vehicles. The resulting test data is analyzed for parameter limits and process stability. In this manner AMI can help assure repeatability and high product quality.

Package Qualification

New packages are also qualified before they are adopted. To analyze packages, a qualification matrix is designed, according to which the new package and an established package (used for control) are tested concurrently. The test matrix consists of a full spectrum of electrical and environmental stress tests, in accordance with MIL-STD-883.

Failure Analysis

Another important function of the Reliability group is failure analysis. Scanning electron microscopes, high power optical microscopes, diagnostic probe stations, and other equipment is used in failure analysis of devices submitted from various sources. It is the function of the Reliability group to determine the cause of failure and recommend corrective action.

The Reliability group provides a failure anlaysis service for the previously mentioned in-house programs and for the evaluation of customer returns. All AMI customers are provided a failure analysis service for any part that fails within one year from date of purchase and the results of the analysis are returned in the form of a written report.

SUMMARY

The Product Assurance Program at AMI is oriented towards process control and monitoring, and the evaluation of devices. The Program consists of three major functions: Quality Control, Quality Assurance, and Reliability. Constant monitoring of all phases of production, with information feedback at all levels, allows fast and efficient detection of problems, evaluation and analysis, correction, and verification of the correction. The overall result is a line of products which are highly repeatable and reliable, with a very low reject level.

PROCESS DESCRIPTIONS

Each of the major MOS processes is described on the following pages. First, the established production proven processes are described, followed by those advanced processes, which are starting to go into volume production now. In each case, the basic processes is described first, followed by an explanation of its advantages, applications, etc.

P-CHANNEL METAL GATE PROCESS

Of all the basic MOS processes, P-channel Metal Gate is the oldest and the most completely developed. It has served as the foundation for the MOS/LSI industry and still finds use today in some devices. Several versions of this process have

evolved since its earliest days. A thin slice (8 to 10 mils) of lightly doped N-type silicon wafer serves as the substrate or body of the MOS transistor. Two closely spaced, heavily doped P-type regions, the source and drain, are formed within the substrate by selective diffusion of an impurity that provides holes as majority electrical carriers. A thin deposited layer of aluminum metal, the gate, covers the area between the source and drain regions, but is electrically insulated from the substrate by a thin layer (1000-1500 Å) of silicon dioxide. The P-channel transistor is turned on by a negative gate voltage and conducts current between the source and the drain by means of holes as the majority carriers.

The basic P-channel metal gate process can be subdivided in two general categories: *high-threshold and low-*

FIGURE 10-1. SUMMARY OF MOS PROCESS CHARACTERISTICS
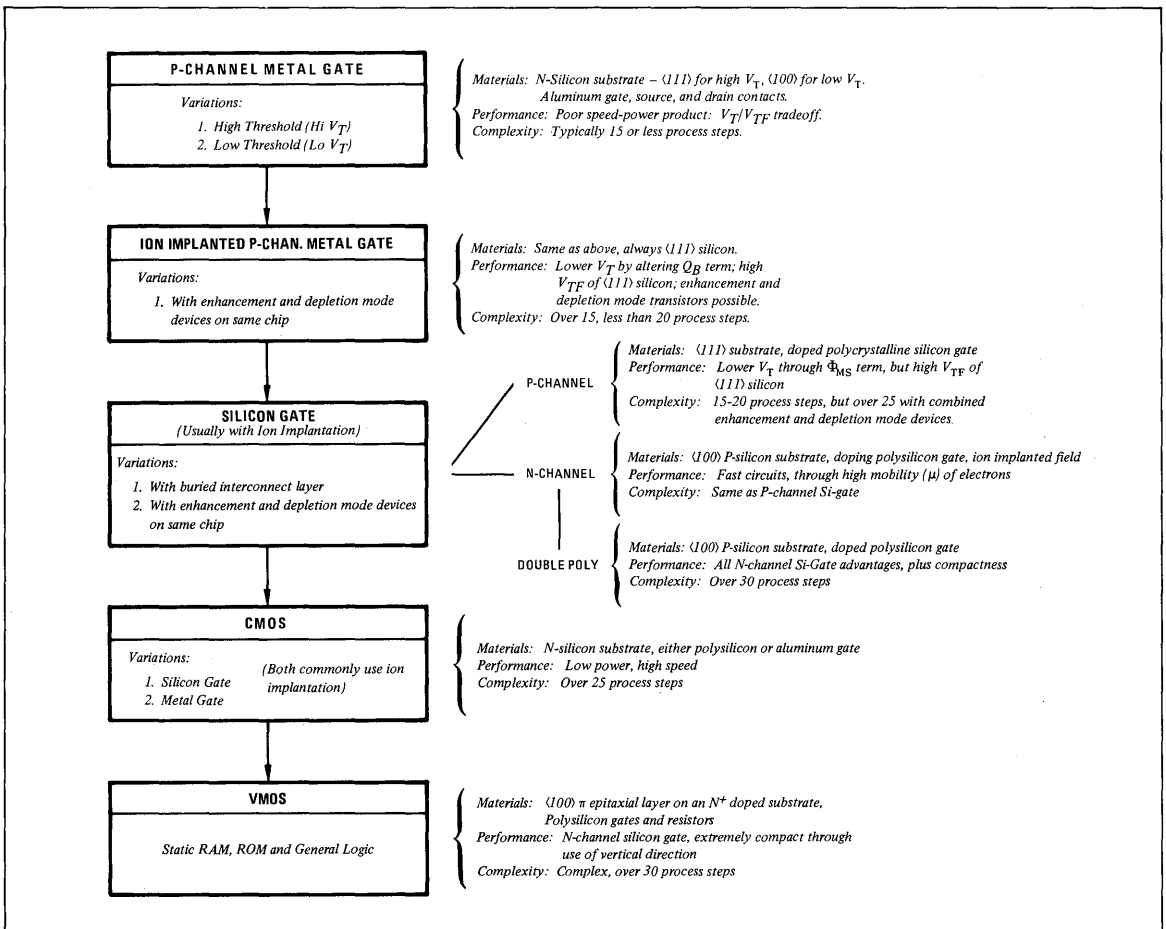
threshold. Various manufacturers use different techniques (particularly so with the low threshold process) to achieve similar results, but the difference between them always rests in the threshold voltage V_T required to turn a transistor on. The high threshold V_T is typically -3 to -5 volts and the low threshold V_T is typically -1.5 to -2.5 volts.

The original technique used to achieve the difference in threshold voltages was by the use of substrates with different crystalline structures. The high V_T process used ⟨111⟩ silicon, whereas the low V_T process used ⟨100⟩ silicon. The difference in the silicon structure causes the surface charge between the substrate and the silicon dioxide to change in such a manner that it lowers the threshold voltages.

One of the main advantages of lowering V_T is the ability to interface the device with TTL circuitry. However, the use of ⟨100⟩ silicon carries with it a distinct disadvantage also. Just as the surface layer of the ⟨100⟩ silicon can be inverted by a lower V_T, so it also can be inverted at other random locations — through the thick oxide layers — by large voltages that may appear in the metal interconnections between circuit components. This is undesirable because it creates parasitic transistors, which interfere with circuit operation. The maximum voltage that can be carried in the interconnections is called the parasitic field oxide threshold voltage V_{TF}, and generally limits the overall voltage at which a circuit can operate. This, then, is the main factor that limits the use of the low V_T process. A drop in V_{TF} between a high V_T and low V_T process may, for example, be from -28V to -17V.

The low V_T process, because of its lower operating voltages, usually produces circuits with a lower operating speed than the high V_T process, but is easier to interface with other circuits, consumes less power, and therefore is more suitable for clocked circuits. Both P-channel metal gate processes yield devices slower in speed than those made by other MOS processes, and have a relatively poor speed/power product. Both processes require two power supplies in most circuit designs, but the high V_T process, because it operates at a high threshold voltage, has excellent noise immunity.

ION IMPLANTED P-CHANNEL METAL GATE PROCESS

The P-channel Ion Implanted process uses essentially the same geometrical structure and the same materials as the high V_T P-channel process, but includes the ion implantation step. The purpose of ion implantation is to introduce P-type impurity ions into the substrate in the limited area under the gate electrode. By changing the characteristics of the substrate in the gate area, it is possible to lower the threshold voltage V_T of the transistor, without influencing any other of its properties.

Figure 10-2 shows the ion implantation step in a diagrammatic manner. It is performed after the gate oxide is deposited, but before the source, gate, and drain metallization deposition. The wafer is exposed to an ion beam which penetrates through the thin gate oxide layer and implants ions into the silicon substrate. Other areas of the substrate are protected both by the thicker oxide layer and sometimes also by other masking means. Ion implantation can be used with any process and, therefore could, except for the custom of the industry, be considered a special technique, rather than a process in itself.

The implantation of P-type ions into the substrate, in effect, reduces the effective concentration of N-type ions in the channel area and thus lowers the V_T required to turn the transistor on. At the same time, it does not alter the N-type ion concentration elsewhere in the substrate and therefore, does not reduce the parasitic field oxide threshold voltage V_{TF} (a

FIGURE 10-2. DIAGRAM OF ION IMPLANTATION STEP

Boron (P-type) ions from Implanter Accelerator

SILICON OXIDE

P SOURCE   P DRAIN

N-TYPE SUBSTRATE

Ions Implanted Here

Note: Implantation step is performed after gate oxidation.
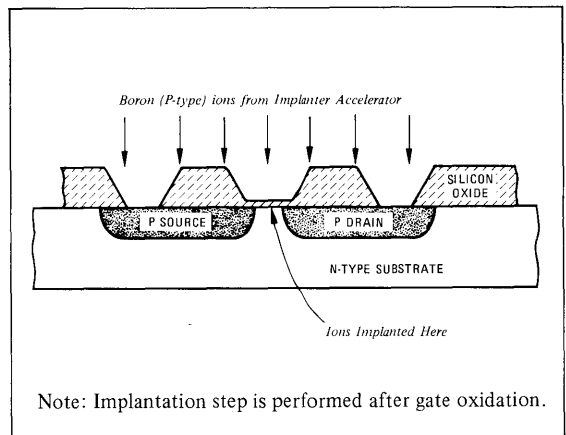
problem with the low V_T P-channel Metal Gate process, described above). The ⟨111⟩ silicon usually is used in ion-implanted transistors.

In fact, if the channel area is exposed to the ion beam long enough, the substrate in the area can be turned into P-type silicon (while the body of the substrate still remains N-type) and the transistor becomes a depletion mode device. In any circuit some transistors can be made enhancement type, while others are depletion type, and the combination is a very useful circuit design tool.

The Ion-implanted P-channel Metal Gate process is very much in use today. Among all the processes, it represents a good optimization between cost and performance and thus is the logical choice for many common circuits, such as memory devices, data handling (communication) circuits, and others.

Because of its low V_T, it offers the designer a choice of using low power supply voltages to conserve power or increase supply voltages to get more driving power and thus increase speed. At low power levels it is more feasible to implement clock generating and gating circuits on the chip. In most circuit designs only a single power supply voltage is required.

N-CHANNEL PROCESS

Historically, N-channel process and its advantages were known well at the time when the first P-channel devices were successfully manufactured, however it was much more difficult to produce N-channel. One of the main reasons was that the polarity of intrinsic charges in the materials combined in such a way that a transistor was on at 0V and had a V_T of only a few tenths of a volt *(positive)*. Thus, the transistor operated as a marginal depletion mode device, without a well-defined *on/off* biasing range. Attempts to raise V_T by varying gate oxide thickness, increasing the substrate doping, and back biasing the substrate, created other objectionable results and it was not until research into materials, along with ion implantation, silicon gates, and other improvements came about that N-channel became practical for high density circuits.

The N-channel process gained its strength only after the P-channel process, ion implantation, and silicon gate all were already well developed. N-channel went into volume productions with advent of the 4K dynamic RAM and the microprocessor, both of which required speed and high density. Because P-channel processes were nearing their limits in both of these respects, N-channel became the logical answer.

The N-channel process is structurally different from any of the processes described so far, in that the source, drain, and channel all are N-type silicon, whereas the body of the substrate is P-type. Conduction in the N-channel is by means of electrons, rather than holes.

The main advantage of the N-channel process is that the mobility of electrons is about three times greater than that of holes and, therefore, N-channel transistors are faster than P-channel. In addition, the increased mobility allows more current flow in a channel of any given size, and therefore N-channel transistors can be made smaller. The positive gate voltage allows an N-channel transistor to be completely compatible with TTL.

Although metal gate N-channel processes have been used, the predominant N-channel process is a silicon gate process. Among the advantages of silicon gate is the possibility of a buried layer of interconnect lines, in addition to the normal aluminum interconnections deposited on the surface of the chip. This gives the circuit designer more latitude in layout

and often allows the reduction of the total chip size. Because the polysilicon gate electrode is deposited in a separate step, after the thick oxide layer is in place, the simultaneous deposition of additional polysilicon interconnect lines is only a matter of masking. These interconnect lines are buried by later steps, as shown in Figure 10-3.

FIGURE 10-3. CROSSECTION OF A SILICON GATE MOS TRANSISTOR

(a) Transistor Ready for Source and Drain Diffusions

(b) Finished Transistor
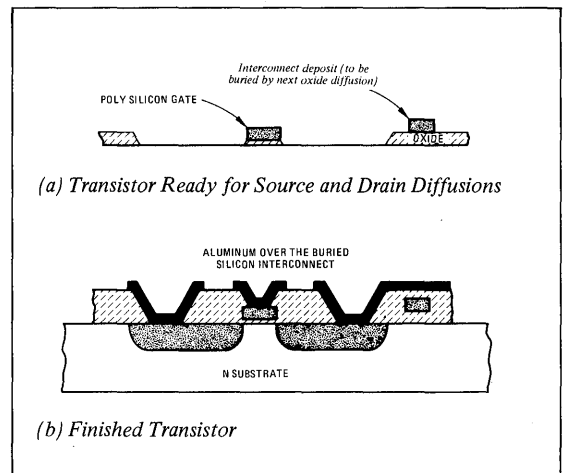
One minor limitation associated with the buried interconnect lines is their location. Because the source and drain diffusions are done after the polysilicon is deposited [see (a) of Figure 10-3] the interconnect lines cannot be located over these diffusion regions.

A second advantage of a silicon gate is associated with the reduction of overlap between the gate and both the source and drain. This reduces the parasitic capacitance at each location and improves speed, as well as power consumption characteristics. Whereas in the metal gate process, the P region source and drain diffusion must be done prior to deposition of the gate electrode, in silicon gate process, the electrode is in place during diffusion, see (a) of Figure 10-3. Therefore, no planned overlap for manufacturing tolerance purposes need exist and the gate is said to be *self-aligned*. The only overlap that occurs is due to the normal lateral extension of the source and drain regions during the diffusion process.

The silicon-gate process produces devices that are more compact than metal gate, and are slightly faster because of the reduced gate overlap capacitance. Because the basic silicon gate process is relatively simple, it is also economical. It is a versatile process that is used in memory devices and most any other circuit.

Because N-channel is relatively new, however, its production techniques and variations in applications still are undergoing development. However, the combination of high speed, TTL compatibility, low power requirements, and compactness have already made N-channel the most widely used process. The cost of N-channel has been coming down also.

In addition to its use in large memory chips and microprocessors, N-channel has become a good general purpose process for circuits in which compactness and high speed are important. The addition of a second layer of polysilicon to this process has allowed the formation of overlapping electrodes making possible charge coupled devices for very compact dynamic memory cells, for filters, and for analog/digital conversion.

CMOS

The basic CMOS circuit is an inverter, which consists of two adjacent transistors − one an N-channel, the other a P-channel, as shown in Figure 10-4. The two are fabricated on the same substrate, which can be either N or P type.

The CMOS inverter in Figure 10-4 is fabricated on an N-type silicon substrate in which a P "tub" is diffused to form the body for the N-channel transistor. All other steps, including the use of silicon gates and ion implantation, are much the same as for other processes.

The main advantage of CMOS is its extremely low power consumption. When the common input to both gate electrodes is at a logic 1 (a positive voltage) the N-channel transistor is biased on, the P-channel is off, and the output is near ground potential. Conversely, when the input is at a logic 0 level, its negative voltage biases only the P-channel transistor on and the output is near the drain voltage $+V_{DD}$. In either case, only one of the two transistors is on at a time and thus, there is virtually no current flow and no power consumption. Only during the transition from one logic level to the other are both transistors on and current flow increases momentarily.

Silicon Gate CMOS is also fast, approaching speeds of bipolar TTL circuits. On the other hand, the use of two transistors in every device makes CMOS slightly more complex,

FIGURE 10-4. CROSSECTION AND SCHEMATIC DIAGRAM OF A CMOS INVERTER
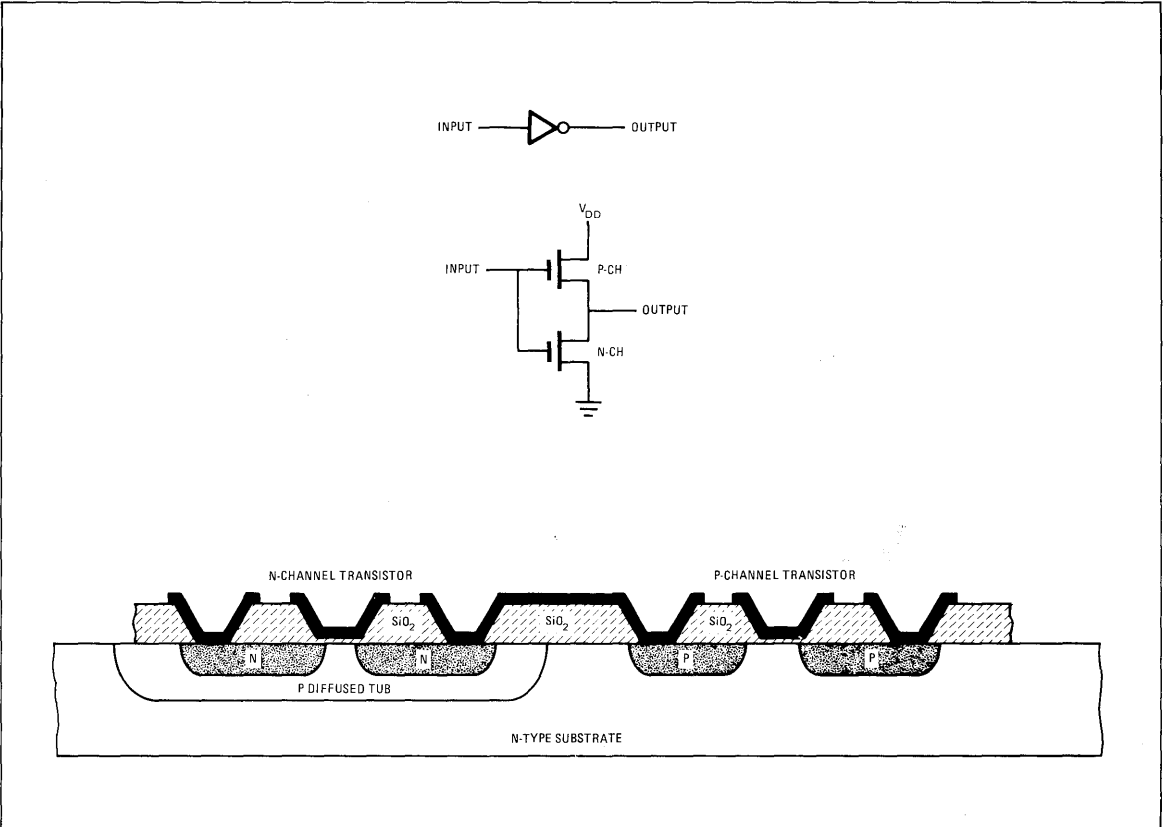
costly, and requires more chip size. For these reasons, the original popularity of CMOS was in SSI logic elements and MSI circuits — logic gates, inverters, small shift registers, counters, etc. These CMOS devices constitute a logic family in the same way at TTL, ECL, and other bipolar circuits do and in the areas of very low power consumption, high noise immunity, and simplicity of operation, are still widely accepted by discrete logic circuit designers.

Low power CMOS circuits made the watch circuit possible and also have been used in space exploration, battery operated consumer products, and automotive control devices. As experience was gained with CMOS, tighter design rules and reduced device sizes have been implemented and now LSI circuits, such as 1K RAM memories and microprocessors, are being manufactured in volume.

CMOS circuits can be operated on a single power supply voltage, which can be varied from +3 to about +18 volts, with a higher voltage giving more speed and higher noise immunity.

VMOS

AMI's patented VMOS process is a significant departure from the other processes described so far. The VMOS transistor is constructed along the sides of a V-shaped groove, that has been etched into the silicon, as shown in the simplified diagram of Figure 10-5(a). (A distinction arises between the VMOS transistor and the planar transistor, whose source, gate, and drain are laid out in the usual manner, along the surface plane of the substrate.)

The source is a heavily N doped region, diffused into the substrate (heavy doping is denoted by + after the N). An epitaxially grown layer over the source constitutes the channel. The lower part of this layer is more heavily P-doped and its depth determines the effective channel length. The upper part, designated π, is very lightly P-doped and is used as an isolating layer, to improve device performance characteristics (as described below). The drain is a heavily N-doped diffusion on the surface of the structure.

The gate oxide and gate electrode are deposited all along the bias surfaces of the V-groove, as shown in the crossection (b), and a field oxide layer extends over the drain. On the surface of a die, the VMOS transistor appears as in (c).

In producing a VMOS device, the source diffusion, epitaxial growth of the channel layer, drain diffusions and insulating oxide all are completed first and only then the V-groove is etched. The precise V shape of the groove results because of the interaction of the etchant with the anisotropic crystal structure.

The VMOS process has several significant advantages:

- Because it uses the sides of the V-groove for device construction, the VMOS transistor requires a much smaller chip surface area than any planar transistor. For this reason, very high density circuits can be built with VMOS.

- Devices with very short channels and large W/ℓ ratios can be built, making possible the design of very high speed circuits, that can carry large currents. In any planar process the channel length can be no smaller than the physical limits of photolithographic masks, whereas in VMOS the effective channel length is controlled only by diffusion and epitaxial thickness, and can be 2 μm or less. On the other hand, channel width is the perimeter distance around all four sides of the V-groove (at the channel elevation) and this clearly is an advantage in getting a high W/ℓ ratio without using up a large surface area. (The perimeter distance is 2-3 times that of a corresponding chip surface area planar device.)

- The π type epitaxial layer isolates the heavily doped N^+ drain from the P channel and thus reduces substrate-to-drain capacitance and increases drain breakdown voltage. Other parasitic capacitances are also typically smaller than those of planar devices and so the overall power consumption at a given operating speed is smaller than that of other processes (with the exception of CMOS).

On the strength of its density and speed advantages, VMOS appears to be most promising for next generation memories — the 16K and larger RAMs. However, various other device configurations, besides the floating source transistor shown in Figure 10-5, are possible and thus VMOS can become a good all-purpose process — usable on ROMs, EPROMs, microprocessors, and random logic. For example, in a ROM the N^+ source diffusion is eliminated and instead, the entire substrate is N type. In this manner all the cells have a common grounded source and a very simple straightforward structure results.

FIGURE 10-5. THE VMOS TRANSISTOR

a. The V-groove of a Floating Source VMOS Transistor

b. Crossection of a Completed Floating Source VMOS Transistor

c. Photograph of Two Parallel VMOS Transistors with Surface V-Groove Dimensions of 6μm x 23μm
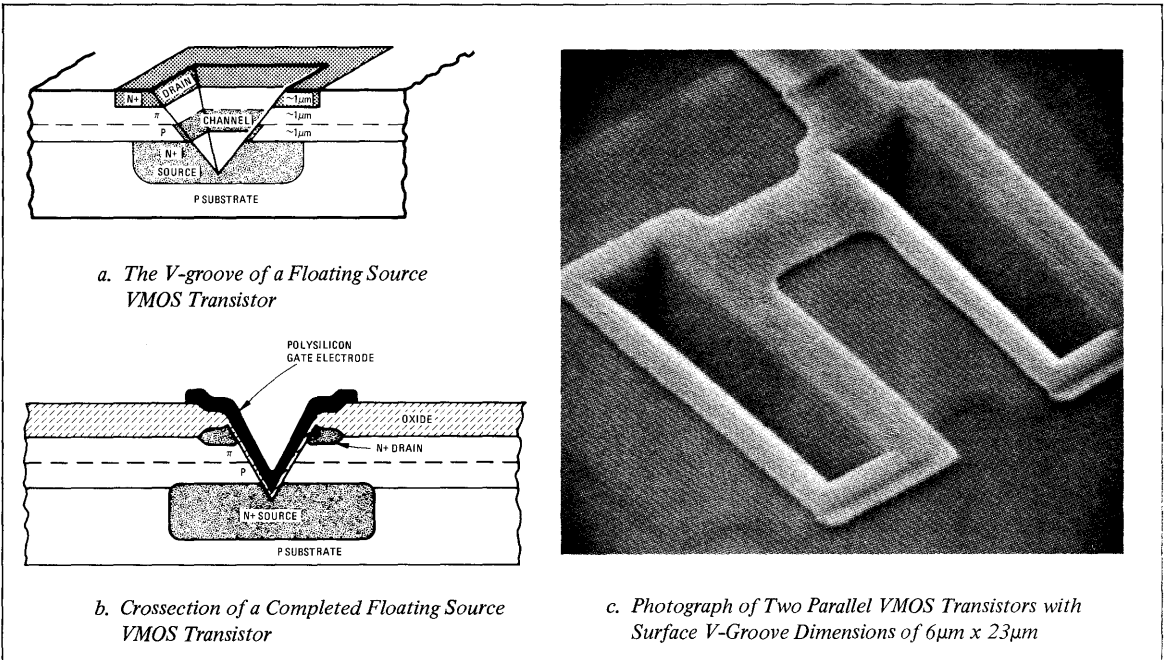
FIGURE 10-6. COMPARATIVE DATA ON MAJOR MOS PROCESSES

RELATIVE SPEED-POWER PRODUCT (NS-MW)

RELATIVE POWER (AT FIXED SPEED)

RELATIVE PROPAGATION DELAY

MASKS REQUIRED

RELATIVE COST PER LOGIC FUNCTION

AMI®

2
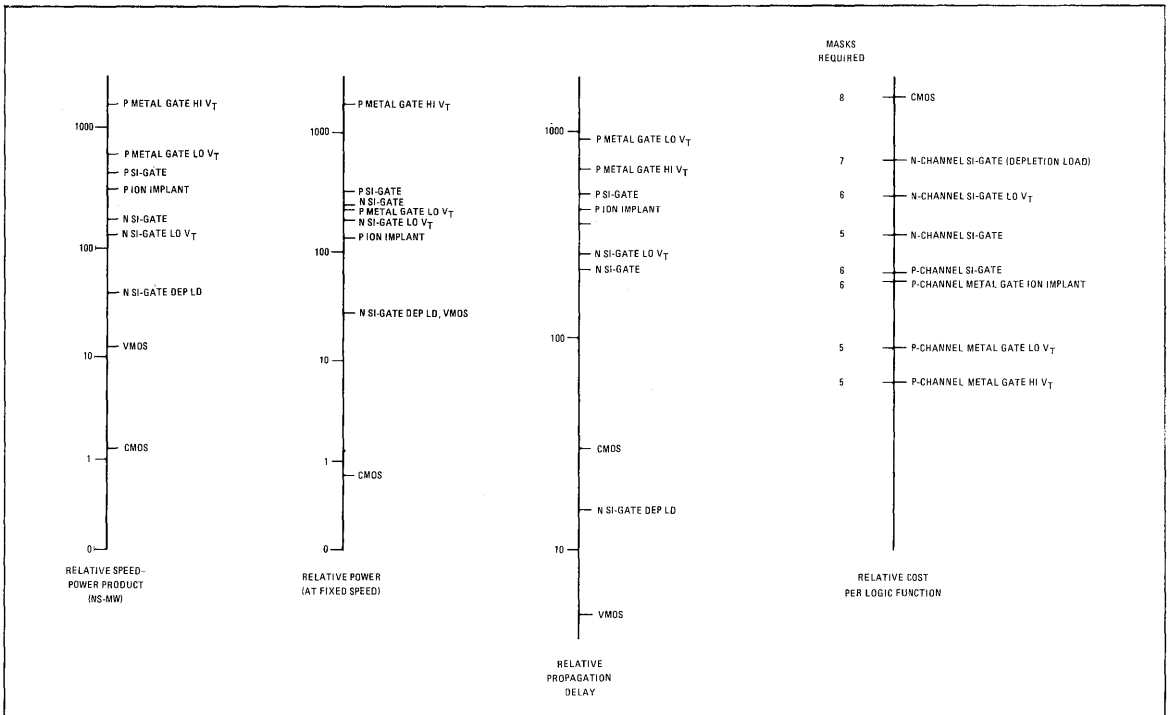
Memories
(RAMs, ROMs
and EPROMs)

MOS STATIC RANDOM ACCESS MEMORIES

PART NO.	ORGANIZATION	PROCESS	MAX. ACCESS TIME (ns)	MAX. ACTIVE POWER (mW)	MAX. STANDBY POWER (mW)	POWER SUPPLIES	PACKAGE
S68B10	128 x 8	NMOS	250	420	N/A	+5V	24 PIN
S68A10	128 x 8	NMOS	360	420	N/A	+5V	24 PIN
S4015-2	1024 x 1	VMOS	60	660	N/A	+5V	16 PIN
S4025-2	1024 x 1	VMOS	60	660	N/A	+5V	16 PIN
S2114H[3]	1024 x 4	VMOS	70	790	N/A	+5V	18 PIN
S2114A-1	1024 x 4	VMOS	150	265	N/A	+5V	18 PIN
S2114L-1	1024 x 4	VMOS	150	370	N/A	+5V	18 PIN
S2114-1	1024 x 4	VMOS	150	525	N/A	+5V	18 PIN
S2114A-2	1024 x 4	VMOS	200	265	N/A	+5V	18 PIN
S2114L-2	1024 x 4	VMOS	200	370	N/A	+5V	18 PIN
S2114-2	1024 x 4	VMOS	200	525	N/A	+5V	18 PIN
S2114A-3	1024 x 4	VMOS	300	265	N/A	+5V	18 PIN
S2114L-3	1024 x 4	VMOS	300	370	N/A	+5V	18 PIN
S2114-3	1024 x 4	VMOS	300	525	N/A	+5V	18 PIN
S4017-3	4096 x 1	VMOS	55	660	N/A	+5V	18 PIN
S4017	4096 x 1	VMOS	70	660	N/A	+5V	18 PIN
S2147-3[3]	4096 x 1	VMOS	55	945	160	+5V	18 PIN
S2147[3]	4096 x 1	VMOS	70	840	105	+5V	18 PIN
S4028[3]	2048 x 8	VMOS	200	525	N/A	+5V	24 PIN

CMOS STATIC RANDOM ACCESS MEMORIES

PART NO.	ORGANIZATION	MAX. ACCESS TIME (ns)	MAX. ACTIVE POWER (mW)	MAX. STANDBY POWER (mW)	POWER SUPPLIES	PACKAGE
S2222[1]	512 x 1	350	25	.05	+10V	16 PIN
S2222A[1]	512 x 1	700	25	.25	+10V	16 PIN
S5101L-1	256 x 4	450	115	.055	+5V	22 PIN
S5101L	256 x 4	650	115	.055	+5V	22 PIN
S5101L-3	256 x 4	650	115	.735	+5V	22 PIN
S5101L-8	256 x 4	800	115	2.7	+5V	22 PIN
S5101-8	256 x 4	800	115	2.7	+5V	22 PIN
S6508-1	1024 x 1	300	13	.055	+5V	16 PIN
S6508	1024 x 1	460	13	.55	+5V	16 PIN
S6508A-1	1024 x 1	275/115[2]	12.5/50[2]	1.1	+4V to +11V	16 PIN
S6508A	1024 x 1	460/185[2]	12.5/50[2]	5.5	+4V to +11V	16 PIN
S6518-1	1024 x 1	300	13	.055	+5V	18 PIN
S6518	1024 x 1	460	13	.55	+5V	18 PIN
S6518A-1	1024 x 1	275/115[2]	12.5/50[2]	1.1	+4V to +11V	18 PIN
S6518A	1024 x 1	460/185[2]	12.5/50[2]	5.5	+4V to +11V	18 PIN

MEMORY PRODUCTS

MOS DYNAMIC RANDOM ACCESS MEMORIES

PART NO.	ORGANIZATION	PROCESS	MAX. ACCESS TIME (ns)	MAX. ACTIVE POWER (mW)	MAX. STANDBY POWER (mW)	POWER SUPPLIES	PACKAGE
S1103A[1]	1024 x 1	PMOS	205	425	2.0	+16/+19	18 PIN
S4006[1]	1024 x 1	PMOS	400	450	50	−12/+5	16 PIN
S4008-9[1]	1024 x 1	PMOS	800	450	50	−12/+5	16 PIN

UV ERASABLE ELECTRICALLY PROGRAMMABLE READ ONLY MEMORIES

PART NO.	ORGANIZATION	PROCESS	MAX. ACCESS TIME (ns)	MAX. ACTIVE POWER (mW)	MAX. STANDBY POWER (mW)	POWER SUPPLIES	PACKAGE
S6834	512 x 8	PMOS	575	750	N/A	+5/−12	24 PIN
S6834-1	512 x 8	PMOS	750	750	N/A	+5/−12	24 PIN
S5204A	512 x 8	PMOS	750	750	N/A	+5/−12	24 PIN
S4716[3]	2048 x 8	VMOS	250	525	132	+5	24 PIN
S4532[3]	4096 x 8	VMOS	250	525	132	+5	24 PIN

MOS READ ONLY MEMORIES

PART NO.	DESCRIPTION	ORGANIZATION	PROCESS	MAX. ACCESS TIME (ns)	MAX. ACTIVE POWER (mW)	POWER SUPPLIES	PACKAGE
S8773[1]	2560 Bit Static ROM	256 x 10 or 512 x 5	PMOS	600	600	+5/−12	24/28 PIN
S8564[1]	64 x 7 x 9 Charac. Gen.	64 Words	PMOS	450	1100	+5/−12	28 PIN
S3514[1]	4096 Bit Static ROM	512 x 8 or 1024 x 4	PMOS	1000	500	+5/−12	24 PIN
S5232[1]	4096 Bit Static ROM	512 x 8 or 1024 x 4	PMOS	1000	500	+5/−12	24 PIN
S8771[1]	5120 Bit Static ROM	512 x 10 or 1024 x 5	PMOS	450	1000	+5/−12	28 PIN
S6830[1]	8192 Bit Static ROM	1024 x 8	NMOS	575	680	+5	24 PIN
S8865[1]	8192 Bit Dynamic ROM	1024 x 8	PMOS	1700	635	+5/−12	24 PIN
S4216B	16,384 Bit Static ROM	2048 x 8	VMOS	250	500	+5	24 PIN
S6831[1]	16,384 Bit Static ROM	2048 x 8	NMOS	450	420	+5	24 PIN
S6831A	16,384 Bit Static ROM	2048 x 8	NMOS	450	420	+5	24 PIN
S6831B	16,384 Bit Static ROM	2048 x 8	NMOS	450	420	+5	24 PIN
S6831C[1]	16,384 Bit Static ROM	2048 x 8	NMOS	450	420	+5	24 PIN
S8996[1]	16,384 Bit Dynamic ROM	4096 x 4	PMOS	1800	370	+5/−12	24 PIN
S8996[1]	16,384 Bit Dynamic ROM	2048 x 8	PMOS	1800	370	+5/−12	24 PIN
S68332	32,768 Bit Static ROM	4096 x 8	NMOS	450	630	+5	24 PIN
S4264	65,536 Bit Static ROM	8192 x 8	VMOS	350	800	+5	24 PIN

[1] NOT RECOMMENDED FOR NEW DESIGNS
[2] FIRST NUMBER IS AT +5V, SECOND IS AT +10V
[3] TO BE ANNOUNCED

AMI®

4096 BIT (1024x4)
STATIC VMOS RAM

Features

☐ High Speed Operation:
Access Time: 150ns Maximum (–1)

☐ High Density 18 Pin Package

☐ Single +5 Volt Power Supply

☐ Completely Static Operation:
No Clocks Required

☐ Completely TTL Compatible

☐ Common Data I/O:
Three-State Outputs

☐ Fan-Out of 5 TTL: I_{OL} = 8mA @ 0.4V

General Description

The AMI S2114 is a 4096 bit fully static RAM organized as 1024 words by 4 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V supply. The common data input/output pins facilitate interface with systems utilizing a bidirectional data bus. The stored data is read out non-destructively and is the same polarity as the original input data.

The S2114 is fully static requiring no clocks or refreshing for operation. This simplifies device operation as no address setup times are required. The chip select function facilitates memory system expansion by allowing the input/output pins to be OR-tied to other devices.

The S2114 is fabricated using AMI's proprietary VMOS technology. This process permits the manufacture of high performance memory devices suitable for high volume production.

Block Diagram

877308

Pin Names

A_0 - A_{11}	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select	V_{CC}	+5V Power
I/O_1 - I/O_4	Data Input/Output		

Logic Symbol

877309

Pin Configuration

877310

Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	Hi - Z	Not Selected
L	L	L	Hi - Z	Write "0"
L	L	H	Hi - Z	Write "1"
L	H	X	D_{OUT}	Read

2.4

Absolute Maximum Ratings*

Ambient Temperature Under Bias	$-10°$C to $80°$C
Storage Temperature	$-65°$C to $150°$C
Voltage on Any Pin With Respect to Ground	-0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Operating Conditions (V_{CC} = 5V ±5%; T_A = 0°C to 70°C)

Symbol	Parameter	S2114A-1 S2114A-2 S2114A-3 Min.	Max.	S2114L-1 S2114L-2 S2114L-3 Min.	Max.	S2114-1 S2114-2 S2114-3 Min.	Max.	Units	Conditions
I_{LI}	Input Leakage Current		10		10		10	μA	V_{IN} = 0V to 5.25V
$|I_{LO}|$	I/O Leakage Current		10		10		10	μA	CS = 2.4 V; $V_{I/O}$ = 0.4V to V_{CC}
I_{CC}	Power Supply Current		45		65		95	mA	V_{IN} = 5.25V; T_A = 25°C
			50		70		100	mA	V_{IN} = 5.25V; T_A = 0°C
V_{IL}	Input LOW Voltage	-0.5	0.8	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V	
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	I_{OL} = 8mA
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH} = -1mA
I_{OS}	Output Short Circuit Current		100		100		100	mA	Duration not to exceed 30 sec.

Capacitance (T_A = 25°C; f = 1.0MHz)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$C_{I/O}$	Input/Output Capacitance			10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance			5	pF	V_{IN} = 0V

A.C. Characteristics (V_{CC} = 5V ±5%; T_A = 0°C to 70°C)
Read Cycle

Symbol	Parameter	S2114A-1 S2114L-1 S2114-1 Min.	Max.	S2114A-2 S2114L-2 S2114-2 Min.	Max.	S2114A-3 S2114L-3 S2114-3 Min.	Max.	Units	Conditions
t_{RC}	Read Cycle Time	150		200		300		ns	
t_A	Access Time		150		200		300	ns	
t_{CO}	Chip Selection to Output Valid		70		70		100	ns	See Test Circuit and Waveforms
t_{CX}	Chip Selection to Output Active	15		15		15		ns	
t_{OTD}	Output 3-State from Deselection		40		60		80	ns	
t_{OHA}	Output Hold from Address Change	30		30		30		ns	

2.5

A.C. Characteristics (Continued)
Write Cycle

Symbol	Parameter	S2114A-1 S2114L-1 S2114-1 Min.	Max.	S2114A-2 S2114L-2 S2114-2 Min.	Max.	S2114A-3 S2114L-3 S2114L-3 Min.	Max.	Units	Conditions
t_{WC}	Write Cycle Time	150		200		300		ns	
t_W	Write Time	90		120		150		ns	See
t_{WR}	Write Release Time	0		0		0		ns	Test
t_{OTW}	Output 3-State from Write		40		60		80	ns	Circuit and
t_{DW}	Data to Write Time Overlap	90		120		150		ns	Waveforms
t_{DH}	Data Hold from Write Time	0		0		0		ns	

Read Cycle (note 1)
Propagation Delay From Address Inputs

Propagation Delay From Chip Select

Write Cycle (note 2)

NOTES:
1. A read occurs during the overlap of a LOW $\overline{CS}$ and a HIGH $\overline{WE}$.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW WE.
3. t_{WR} is referenced to the positive transition of $\overline{WE}$.
4. $\overline{WE}$ must be HIGH during all address transitions.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with the $\overline{WE}$ LOW transition, then the output buffers remain in the high impedance state.

A.C. Test Conditions

Input Pulse Levels . . . . 0.8V to 2.4V

Input Rise & Fall Times 10ns

Input and Output Timing Level 1.5V

A.C. Test Load

S2114

+5V

510Ω

390Ω

100pF

AMI ®

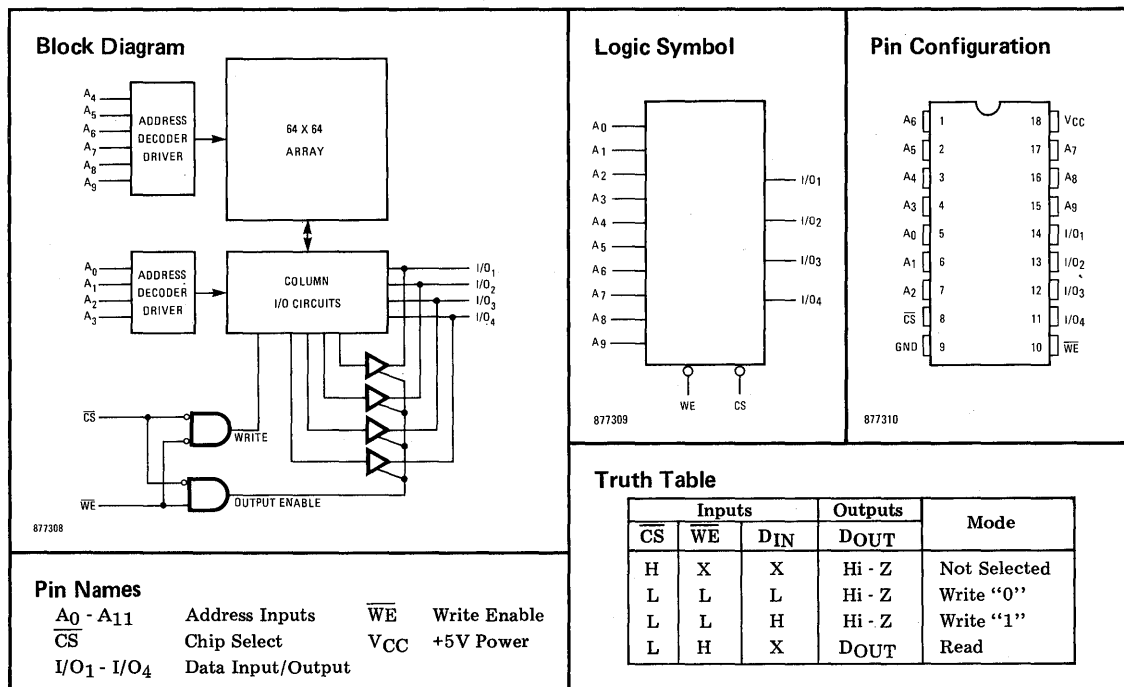# 4096 BIT (1024x4) HIGH SPEED STATIC VMOS RAM

RAMs

Features

☐ High Speed Operation:
   Access Time: 70ns Maximum

☐ High Density 18 Pin Package

☐ Single +5 Volt Power Supply

☐ Completely Static Operation:
   No Clocks Required

☐ Completely TTL Compatible

☐ Common Data I/O:
   Three-State Outputs

☐ Fan-Out of 5 TTL: $I_{OL} = 8mA @ 0.45V$

General Description

The AMI S2114H is a 4096 bit fully static RAM organized as 1024 words by 4 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V supply. The common data input/output pins facilitate interface with systems utilizing a bidirectional data bus. The stored data is read out non-destructively and is the same polarity as the original input data.

The S2114H is fully static requiring no clocks or refreshing for operation. This simplifies device operation as no address setup times are required. The chip select function facilitates memory system expansion by allowing the input/output pins to be OR-tied to other devices.

The S2114H is fabricated using AMI's proprietary VMOS technology. This process permits the manufacture of high performance memory devices suitable for high volume production.

Block Diagram

877308

Pin Names

$A_0 - A_{11}$	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select	V_{CC}	+5V Power
$I/O_1 - I/O_4$	Data Input/Output		

Logic Symbol

877309

Pin Configuration

877310

Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	Hi - Z	Not Selected
L	L	L	Hi - Z	Write "0"
L	L	H	Hi - Z	Write "1"
L	H	X	D_{OUT}	Read

Absolute Maximum Ratings*

Ambient Temperature Under Bias .... $-10°$ C to $80°$ C
Storage Temperature .... $-65°$ C to $150°$ C
Voltage on Any Pin With Respect to Ground .... -0.5 V to 7V
Power Dissipation 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Operating Characteristic (V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to 5.25V
$|I_{LO}|$	I/O Leakage Current			10	μA	CS = 2.4V; $V_{I/O}$ = 0.4V to V_{CC}
I_{CC}	Power Supply Current			150	mA	V_{IN} = 5.25V, T_A = 0°C
V_{IL}	Input LOW Voltage	-0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{OL}	Output LOW Voltage			0.45	V	I_{OL} = 8mA
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	I_{OH} = -1mA
I_{OS}	Output Short Circuit Current			100	mA	Duration not to exceed 30 sec.

Capacitance (T_A = 25°C; f = 1.0 MHz)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IO}	Input/Output Capacitance			10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance			5	pF	V_{IN} = 0V

A.C. Characteristics (V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Read Cycle						
t_{RC}	Read Cycle Time	70			ns	See A.C. Test
t_A	Address Access Time			70	ns	Conditions
t_{OHA}	Output Hold from Address	0			ns	&
t_{CO}	Chip Select Access Time			40	ns	Load
t_{CX}	Chip Select to Output Active	0			ns	
t_{OTD}	Output H-Z from Chip Select			30	ns	
Write Cycle						
t_{WC}	Write Cycle Time	70			ns	See A.C. Test
t_W	Write Time	50			ns	Conditions
t_{WR}	Write Release Time	0			ns	&
t_{OTW}	Output H-Z from Write Enable			30	ns	Load
t_{DW}	Data to Write Time Overlap	40			ns	
t_{DH}	Data Hold Time	0			ns	

Read Cycle (note 1)
Propagation Delay From Address Inputs

Propagation Delay From Chip Select

Write Cycle (note 2)

NOTES:
1. A read occurs during the overlap of a LOW $\overline{CS}$ and a HIGH $\overline{WE}$.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW WE.
3. t_{WR} is referenced to the positive transition of $\overline{WE}$.
4. $\overline{WE}$ must be HIGH during all address transitions.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with the $\overline{WE}$ LOW transition, then the output buffers remain in the high impedance state.

A.C. Test Conditions

Input Pulse Levels .... 0.8V to 2.4V

Input Rise & Fall Times 10ns

Input and Output Timing Level 1.5V

A.C. Test Load

4096 BIT (4096×1)
HIGH SPEED STATIC VMOS RAM

Features

☐ High Speed Operation:
Access Time: 55ns Max. (−3)

☐ Automatic Power-Down

☐ High Density 18 Pin Package

☐ Single +5V Power Supply

☐ Completely Static Operation

☐ Completely TTL Compatible Inputs

☐ Three-State TTL Compatible Output

☐ Fan-Out of 5 TTL: I_{OL} = 8mA @ 0.45V

General Description

The AMI S2147 is a high speed 4096 bit fully static RAM organized as 4096 one-bit words. The device is fully TTL compatible and has a single +5V power supply. It has separate data input and output pins for maximum design flexibility. The three-state output facilitates memory expansion by allowing the output to be OR-tied to other devices. The stored data is read out non-destructively and is the same polarity as the input data.

The automatic power down feature offers significant system power savings. This feature causes no performance degradation, as chip enable access and address access are equal. The S2147 is fully static eliminating the need for clocks or address set up and hold times as well as maximizing data rates since access times and cycle times are equal.

The S2147 is fabricated using AMI's proprietary VMOS technology. The process permits the manufacture of high performance memory devices suitable for high volume production.

Block Diagram

Logic Symbol

Pin Configuration

Pin Names

A_0-A_{11}	Address Inputs	D_{IN}	Data Input
$\overline{CE}$	Chip Enable	D_{OUT}	Data Output
$\overline{WE}$	Write Enable	V_{CC}	+5V Power

Truth Table

Inputs			Output	Mode	Power
$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}		
H	X	X	H-Z	Deselected	Standby
L	L	L	H-Z	Write "0"	Active
L	L	H	H-Z	Write "1"	Active
L	H	X	D_{OUT}	Read	Active

RAMs

Absolute Maximum Ratings*

Ambient Temperature Under Bias .... $-10°$C to $80°$C
Storage Temperature .... $-65°$C to $150°$C
Voltage on Any Pin With Respect to Ground .... -0.5V to 7V
Power Dissipation 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: $V_{CC} = 5V \pm 5\%$, $T_A = 0°$C to $70°$C

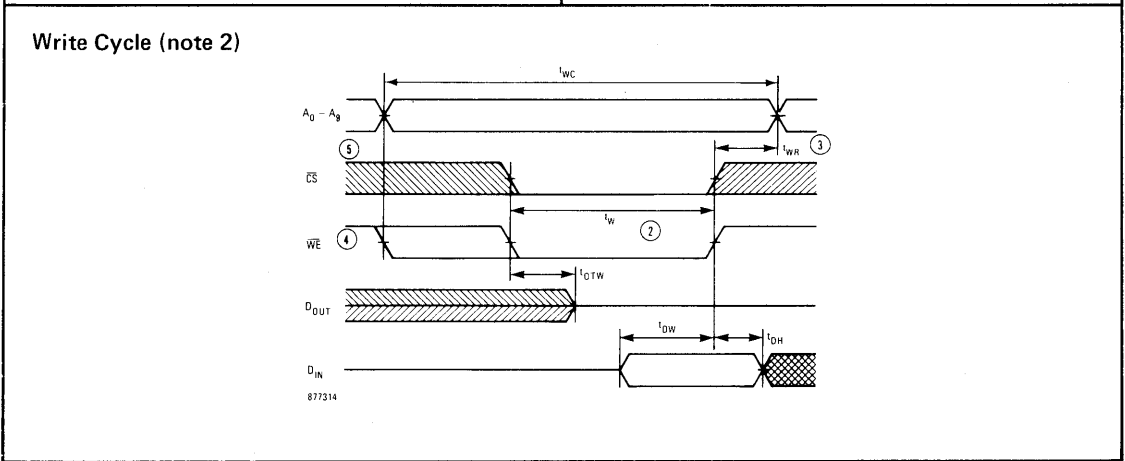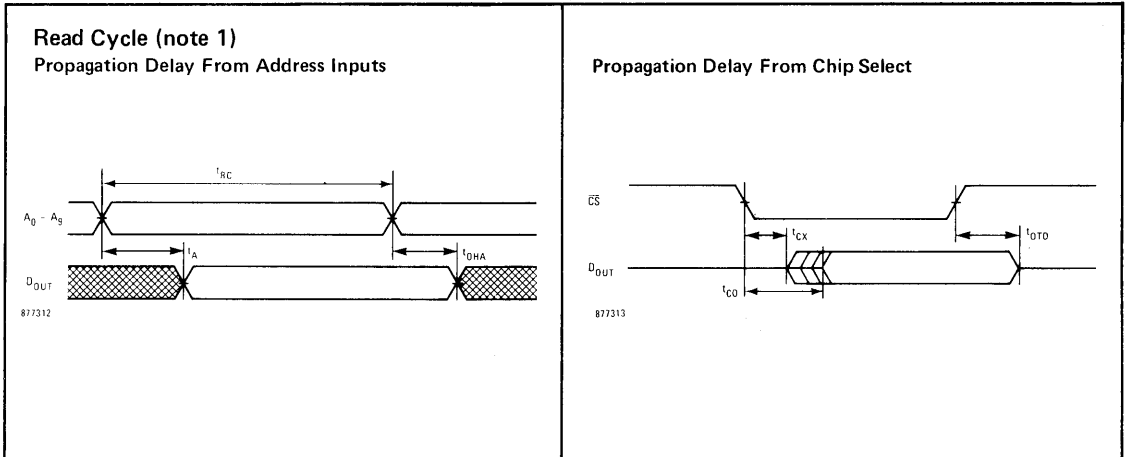| Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage				0.45	V	$I_{OL} = 8$mA
V_{OH}	Output HIGH Voltage		2.4			V	$I_{OH} = -4.0$mA
V_{IL}	Input LOW Voltage				0.8	V	
V_{IH}	Input HIGH Voltage		2.1			V	
I_{LI}	Input Leakage Current				10	μA	V_{CC} = Max., V_{IN} = 0 to V_{CC}
$|I_{LO}|$	Output Leakage Current				50	μA	$\overline{CS} = 2.1$V, V_{CC} = Max. V_{OUT} = 0.4 to 4.5V
I_{OS}	Output Current Short Circuit to Ground				-100	mA	V_{CC} = Max., for not more than one second.
I_{CC}	Operating Current	S2147			160	mA	V_{CC} = Max., $\overline{CE} = V_{IL}$, $T_A = 0°$C, Outputs Open
		S2147-3			180	mA	
I_{SB}	Standby Current	S2147			20	mA	V_{CC} = Max., $\overline{CE} = V_{IH}$
		S2147-3			30	mA	

Capacitance: $T_A = 25°$C, $f = 1.0$MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			5	pF	$V_{IN} = 0$V
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0$V

A.C. Characteristics: $T_A = 0°$C to $75°$C, $V_{CC} = +5$V $\pm 5\%$

Read Cycle

Symbol	Parameter	S2147-3 Min.	S2147-3 Max.	S2147 Min.	S2147 Max.	Units	Conditions
t_{RC}	Read Cycle Time	55		70		ns	See A.C. Test Conditions and Waveform
t_{AA}	Address Access Time		55		70	ns	
t_{AC}	Chip Enable Access Time		55		70	ns	
t_{OH}	Output Hold from Address Change	10		10		ns	
t_{LZ}	Chip Enable to Output LZ	10		10		ns	
t_{HZ}	Chip Enable to Output HZ		30		30	ns	
t_{PU}	Chip Enable to Power Up Time	0		0		ns	
t_{PD}	Chip Disable to Power Down Time		40		50	ns	

Write Cycle

Symbol	Parameter	S2147-3		S2147		Units	Conditions
		Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	55		70		ns	
t_{CW}	Chip Enable to End of Write	45		55		ns	
t_{AW}	Address Valid to End of Write	45		55		ns	See A.C. Test
t_{AS}	Address Setup Time	5		5		ns	Conditions
t_{WP}	Write Pulse Width	35		40		ns	and
t_{WR}	Write Recovery Time	10		15		ns	Waveforms
t_{DW}	Data Valid to End of Write	25		30		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{WZ}	Write Enable to Output HZ	0	25	0	30	ns	
t_{OW}	Output Active from End of Write	0	25	0	30	ns	

READ CYCLE
Propogation Delay From Address Inputs

Propagation Delay From Chip Enable

WRITE CYCLE

NOTES:
1. A read occurs during the overlap of a LOW $\overline{CE}$ and a HIGH $\overline{WE}$.
2. A write occurs during the overlap of a LOW $\overline{CE}$ and a LOW $\overline{WE}$.
3. t_{WR} is referenced to the positive transition of $\overline{WE}$.
4. $\overline{WE}$ must be HIGH during all address transitions.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with the $\overline{WE}$ LOW transition, then output buffers remain in the high impedance state.

A.C. Test Load

A.C. Test Conditions
ALL INPUT PULSES
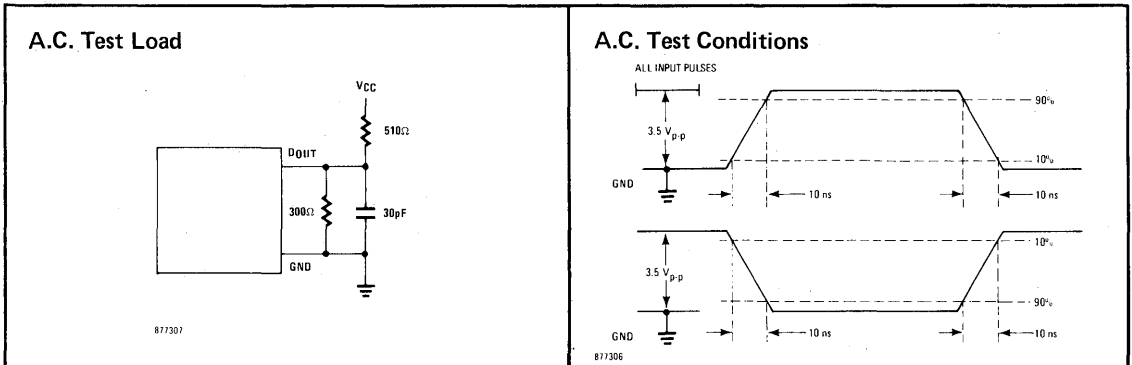
1024 BIT (1024x1)
HIGH SPEED STATIC VMOS RAM

RAMs

Features

☐ **Pin Compatible with 93415 (S4015) and 93425 (S4025)**

☐ **Single +5V Power Supply**

☐ **Completely TTL Compatible**

☐ **Open Collector Output — S4015**

☐ **Three-State Output — S4025**

☐ **Fan-Out of 10 TTL — I_{OL} = 16mA @ 0.45V**

☐ **Completely Static — no Clocks or Refreshing**

General Description

The AMI S4015/S4025 family of 1024x1 bit high speed VMOS RAMs offers fully static operation with a single 5V supply. The device is completely TTL compatible on inputs and output. The family is available in two output configurations. The S4015 has an open collector (open drain) output and the S4025 has a three-state output. The stored data is read out nondestructively and is the same polarity as the original input data.

The family is completely static requiring no clocks or refreshing for operation. Chip Select ($\overline{CS}$) controls the output and simplifies memory system expan-sion. The fast chip select time allows decoding the chip select from the address without increasing address access time.

Block Diagram

Logic Symbol

Pin Configuration

Pin Names

$\overline{CS}$	Chip Select	D_{IN}	Data Input
$A_0 - A_9$	Address Inputs	D_{OUT}	Data Output
$\overline{WE}$	Write Enable		

Truth Table

Inputs			Output (D_{OUT})		Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	S4015	S4025	
H	X	X	H	H − Z	Not selected
L	L	L	H	H − Z	Write "0"
L	L	H	H	H − Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read
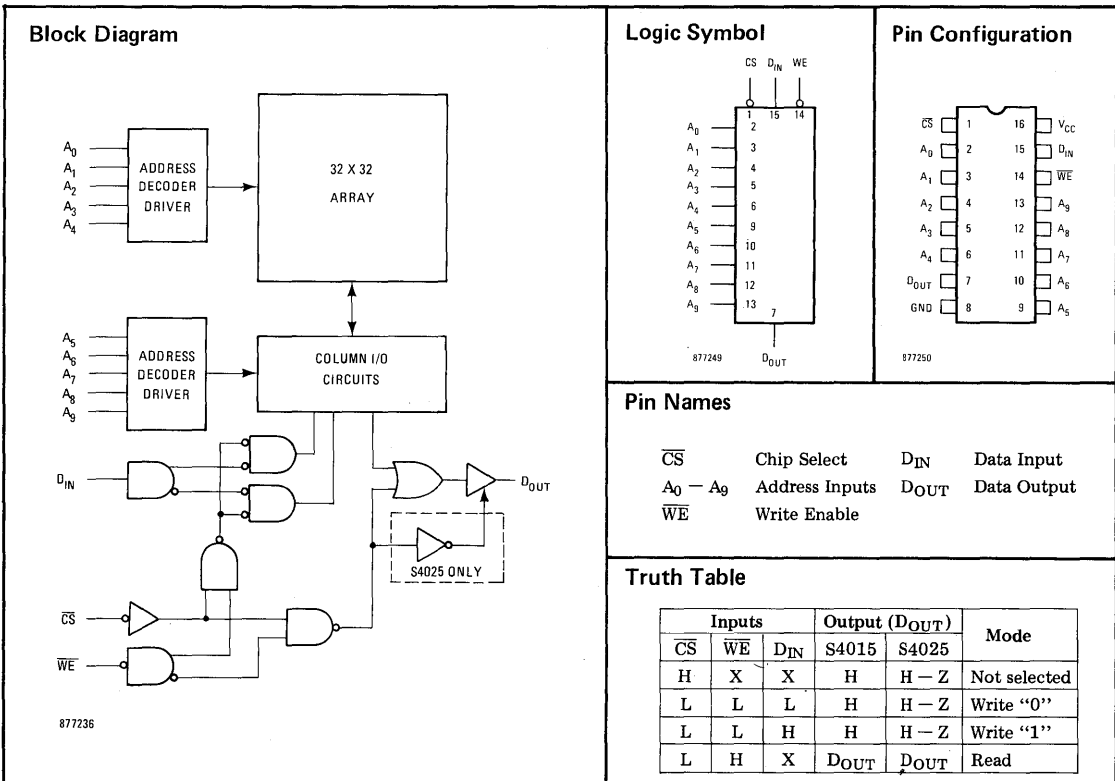
General Description (Continued)

The S4015/S4025 is fabricated using AMI's proprietary VMOS process, thus allowing the production of high speed MOS RAMs that are fully compatible with bipolar RAMs but offering the advantage of lower power dissipation.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	$-10°C$ to $+85°C$
Storage Temperature	$-65°C$ to $+150°C$
Output or Supply Voltages	$-0.5V$ to $+7V$
Input Voltages	$-0.5V$ to $+5.5V$
Power Dissipation	1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $75°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.45	V	V_{CC}=Min, I_{OL}=16mA
V_{OH}	Output HIGH Voltage (S4025 Family)	2.4			V	V_{CC}=Min, I_{OH}=-5.2mA
V_{IL}	Input LOW Voltage			0.8	V	
V_{IH}	Input HIGH Voltage	2.1			V	
I_{IL}	Input LOW Current			-40	μA	V_{CC}=Max, V_{IN}=0.4V
I_{IH}	Input HIGH Current			40	μA	V_{CC}=Max, V_{IN}=4.5V
I_{CEX}	Output Leakage Current (S4015 Family)			50	μA	V_{CC}=Max, V_{OUT}=4.5V
I_{OFF}	Output Current (High Z) - (S4025 Family)			50	μA	V_{CC}=Max, V_{OUT}=2.4V
				-50	μA	V_{CC}=Max, V_{OUT}=0.5V
I_{OS}	Output Current Short Circuit to Ground (S4025 Family)			-100	mA	V_{CC}=Max, for not more than 1 second
I_{CC}	Power Supply Current			125	mA	V_{CC}=Max All Inputs Grounded Output Open

Capacitance

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			5	pF	All inputs=0V
C_{OUT}	Output Capacitance			8	pF	Output=0V

A.C. Characteristics: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $75°C$

Read Cycle

Symbol	Parameter	S4015(25) - 2			Units	Conditions
		Min.	Typ.	Max.		
t_{ACS}	Chip Select Time			40	ns	See Test
t_{RCS}	Chip Select Recovery Time			40	ns	Circuit &
t_{AA}	Address Access Time			60	ns	Waveforms

Write Cycle

t_{WS}	Write Disable Time			40	ns	
t_{WR}	Write Recovery Time	0		40	ns	
t_W	Write Pulse Width	40			ns	
t_{WSD}	Data Set-up Time Prior to Write	5			ns	See Test
t_{WHD}	Data Hold Time After Write	5			ns	Circuit &
t_{WSA}	Address Set-up Time	5			ns	Waveforms
t_{WHA}	Address Hold Time	5			ns	
t_{WSCS}	Chip Select Set-up Time	5			ns	
t_{WHCS}	Chip Select Hold Time	5			ns	

Read Cycle

Propagation Delay From Address Inputs
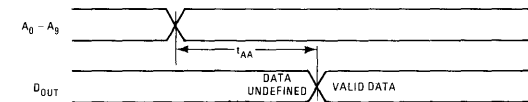
877303

Propagation Delay From Chip Select
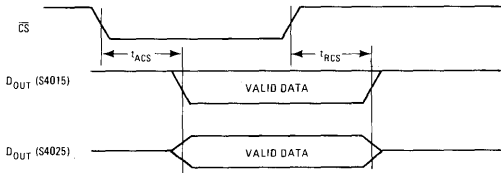
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Write Cycle
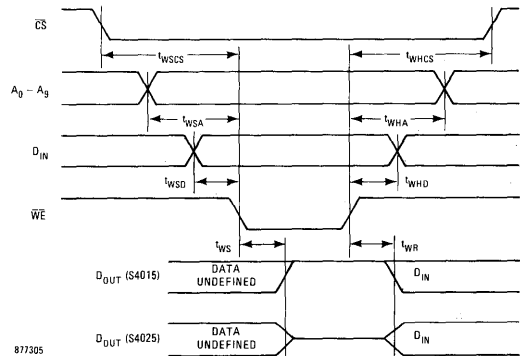
877305

A.C. Test Load

	R₁	R₂
S4015	270Ω	600Ω
S4025	220Ω	150Ω

877307

A.C. Test Conditions

ALL INPUT PULSES

877306

AMI ®
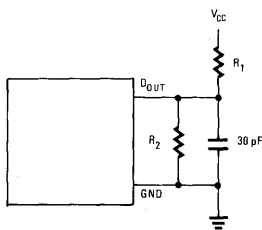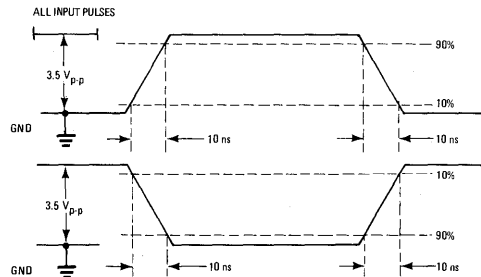
4096 BIT (4096x1)
HIGH SPEED STATIC VMOS RAM

Features

☐ High Speed Operation:

  Address Access Time: 55ns Maximum

  Chip Select Access Time: 30ns Maximum

☐ Fast Chip Select Optimizes Access Time

☐ High Density 18 Pin Package

☐ Single +5V Power Supply

☐ Completely Static Operation

☐ Completely TTL Compatible Inputs

☐ Three-State TTL Compatible Output

☐ Fan-Out of 5 TTL: I_{OL} = 8mA @ 0.45V

General Description

The AMI S4017 is a high speed 4096 bit fully static RAM organized as 4096 one-bit words. The device is fully TTL compatible and has a single +5V power supply. It has separate data input and output pins for maximum design flexibility. The three-state output facilitates memory expansion by allowing the output to be OR-tied to other devices. The stored data is read out non-destructively and is the same polarity as the original input data.

The fast chip select access time offers a significant performance advantage. As the chip select is normally decoded from the address, the time required to decode the chip select will not impact the overall access time.

The S4017 is fabricated using AMI's proprietary VMOS technology. The process permits the manufacture of high performance memory devices suitable for high volume production.

Block Diagram

Pin Names

A_0-A_{11}	Address Inputs	D_{IN}	Data Input
$\overline{CS}$	Chip Select	D_{OUT}	Data Output
$\overline{WE}$	Write Enable	V_{CC}	+5V Power

Logic Symbol

Pin Configuration

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	H-Z	Not Selected
L	L	L	H-Z	Write "0"
L	L	H	H-Z	Write "1"
L	H	X	D_{OUT}	Read

RAMs

Absolute Maximum Ratings*

Ambient Temperature Under Bias .... $-10°C$ to $80°C$
Storage Temperature .... $-65°C$ to $150°C$
Voltage on Any Pin With Respect to Ground .... $-0.5V$ to $7V$
Power Dissipation .... $1W$

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = 5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.45	V	I_{OL} = 8mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = -4.0mA
V_{IL}	Input LOW Voltage			0.8	V	
V_{IH}	Input HIGH Voltage	2.1			V	
I_{LI}	Input Leakage Current			10	μA	V_{CC} = Max., V_{IN} = 0 to V_{CC}
$|I_{LO}|$	Output Leakage Current			50	μA	$\overline{CS}$ = 2.1V, V_{CC} = Max. V_{OUT} = 0.4 to 4.5V
I_{OS}	Output Current Short Circuit to Ground			-100	mA	V_{CC} = Max., for not more than one second.
I_{CC}	Power Supply Current			125	mA	V_{CC} = Max., $\overline{CS}$ = V_{IL} Output Open

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			8	pF	V_{OUT} = 0V

A.C. Characteristics: T_A = 0°C to 75°C, V_{CC} = +5V ± 5%

Read Cycle

Symbol	Parameter	S4017-3 Min.	S4017-3 Max.	S4017 Min.	S4017 Max.	Units	Conditions
t_{RC}	Read Cycle Time	55		70		ns	See A.C. Test Condition and Waveform
t_{AA}	Address Access Time		55		70	ns	
t_{ACS}	Chip Select Access Time		30		40	ns	
t_{OH}	Output Hold from Address Change	10		10		ns	
t_{LZ}	Chip Select to Output L — Z	10		10		ns	
t_{HZ}	Chip Select to Output H — Z		30		30	ns	

Write Cycle

Symbol	Parameter	S4017-3		S4017		Units	Conditions
		Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	55		70		ns	
t_{CW}	Chip Select to End of Write	40		50		ns	
t_{AW}	Address Valid to End of Write	45		55		ns	See A.C. Test
t_{AS}	Address Setup Time	5		5		ns	Conditions
t_{WP}	Write Pulse Width	35		40		ns	and
t_{WR}	Write Recovery Time	10		15		ns	Waveforms
t_{DW}	Data Valid to End of Write	25		30		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{WZ}	Write Enable to Output HZ	0	25	0	30	ns	
t_{OW}	Output Active from End of Write	0	25	0	30	ns	

Write Cycle
Propagation Delay from Chip Enable

Read Cycle

Propogation Delay From Chip Select

NOTES:
1. A read occurs during the overlap of a LOW $\overline{CS}$ and a HIGH $\overline{WE}$.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is referenced to the positive transition of $\overline{WE}$.
4. $\overline{WE}$ must be HIGH during all address transitions.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with the $\overline{WE}$ LOW transition, then the output buffers remain in the high impedance state.

A.C. Test Load

A.C. Test Conditions

AMI®

RAMs

16,384 BIT (2048 X 8) STATIC VMOS RAM

Features

☐ **High Speed Operation:**
  Access Time: 200ns Max.

☐ **Single +5V Power Supply**

☐ **Pin Compatible with 16K EPROM/ROM**

☐ **Fully Static Operation**

☐ **Completely TTL Compatible**

☐ **Common Data Input/Output:**
  Three-State Outputs

☐ **Output Enable Function for Easy Control of**
  Data Output

General Description

The AMI S4028 is a 16,384 bit fully static VMOS random access memory organized as 2048 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The common data input/output pins and output enable function facilitate interface with systems utilizing a bi-directional data bus. Data is read out non-destructively and is the same polarity as the input data.

The S4028 is fully static requiring no clocks or refreshing for operation. This simplifies device operation as no address setup or hold times are required. The chip select and output enable functions facilitate memory expansion by allowing the input/output pins to be OR-tied to other devices.

The S4028 is fabricated using AMI's proprietary VMOS technology. This permits the manufacture of high performance memory devices suitable for high volume production.

Block Diagram

Logic Symbol

Pin Configuration

Pin Names

$A_0 - A_{10}$	Address Inputs	$\overline{OE}$	Output Enable
$I/O_1 - I/O_8$	Data Inputs/Outputs	$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select	V_{CC}	+5V Power Supply

Truth Table

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Data In	Data Out
Deselected	H	X	X	X	Hi−Z
Read	L	L	H	Hi−Z	Data Out
Write	L	H	L	Data In	Hi−Z
Write	L	L	L	Data In	Hi−Z
Selected, Output Hi−Z	L	H	H	X	Hi−Z

AMI®

1024 BIT (256x4) STATIC CMOS RAM

Features

☐ Ultra Low Standby Power

☐ Data Retention at 2V (L Version)

☐ Single +5 Volt Power Supply

☐ Completely Static Operation

☐ Completely TTL Compatible Inputs

☐ Three-State TTL Compatible Outputs

General Description

The AMI S5101 family of 256 x 4-bit ultra low power CMOS RAMs offers fully static operation with a single + 5 volt power supply. All inputs and outputs are directly TTL compatible. With data inputs and outputs on adjacent pins, either separate or common data I/O operations can easily be implemented for maximum design flexibility. The three-state outputs will drive one full TTL load and are disabled (high impedance state) by output disable (OD), either chip enable (CE1 or CE2), or in a write cycle (R/W = LOW). This facilitates the control of common data I/O systems.

Block Diagram

Logic Symbol

Pin Configuration

Truth Table

$\overline{CE1}$	CE2	OD	R/W	DIN	Output	Mode
H	X	X	X	X	High Z	Not selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	High Z	Write
L	H	L	H	X	Dout	Read

Pin Names

A_0 - A_7	Address Inputs	$\overline{CE1}$	Chip Enable
DI_1 - DI_4	Data Inputs	CE2	Chip Enable
DO_1 - DO_4	Data Outputs	R/W	Read/Write Input
OD	Output Disable	V_{CC}	+5 Volt Power Supply
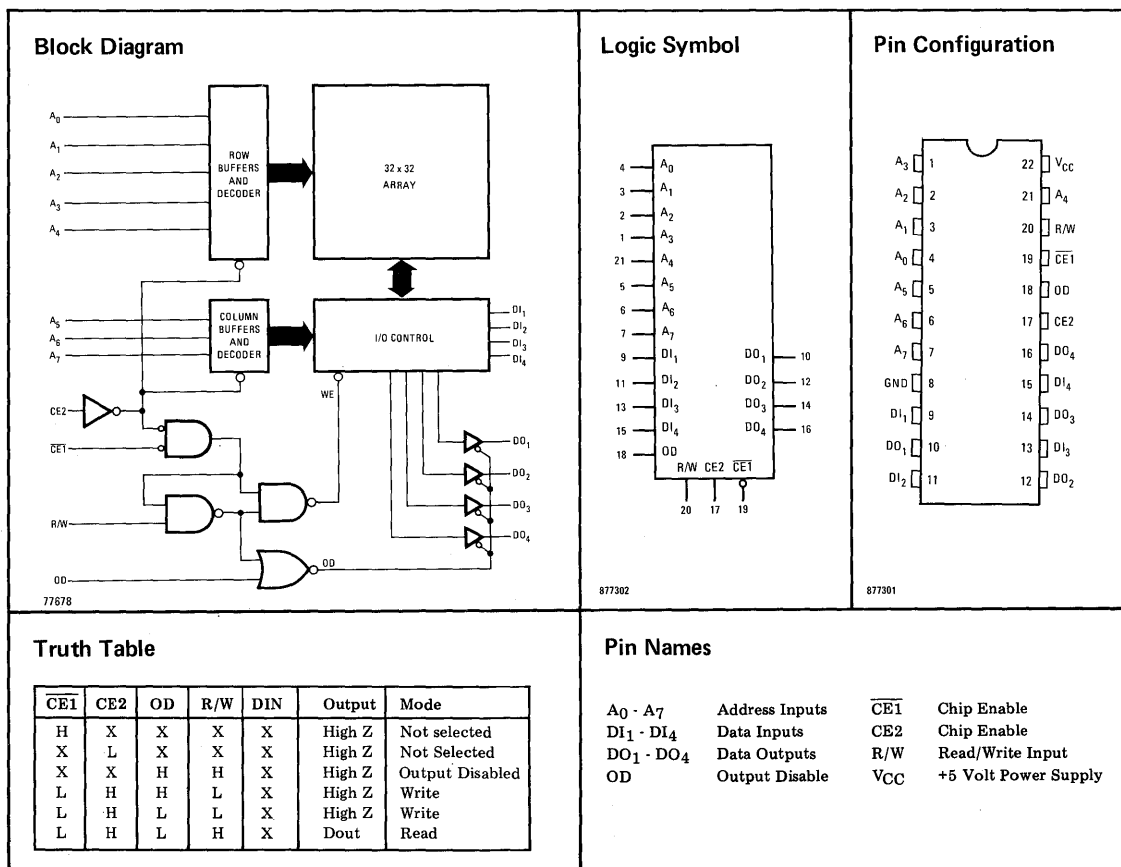
General Description (Continued)

The stored data is read out nondestructively and is the same polarity as the original input data. The S5101 is totally static, making clocks unnecessary for a new address to be accepted. The device has two chip enable inputs ($\overline{CE1}$ and CE2) allowing easy system expansion. CE2 disables the entire device but $\overline{CE1}$ does not disable the address buffers and decoders. Thus, minimum power dissipation is achieved when CE2 is low.

The L version of the S5101 has the additional feature of guaranteed data retention with the power supply as low as 2 volts. This makes the device an ideal choice when battery augmented non-volatile RAM storage is mandatory.

The S5101 is fabricated using a silicon gate CMOS process suitable for high volume production of ultra low power, high performance memories.

Absolute Maximum Ratings*

Ambient Temperature Under Bias .... –10°C to 80°C
Storage Temperature .... –65°C to 150°C
Voltage on Any Pin with Respect to Ground .... –0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage 11V
Power Dissipation 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Unless otherwise specified)

Symbol	Parameter		Limits Min.	Limits Max.	Units	Conditions
I_{LI}	Input Leakage Current			1	μA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current			1	μA	$\overline{CE1} = V_{IH}$ $V_{OUT} = 0V$ to V_{CC}
I_{CC}	Operating Supply Current			22	mA	Outputs = Open, $V_{IN} = V_{IL}$ to V_{CC}
I_{CCL}	Standby Supply Current	S5101L1, S5101L		10	μA	$V_{IN} = 0V$ to V_{CC} except CE2 $\leqslant 0.2V$
		S5101L3		140	μA	
		S5101L8, S5101-8		500	μA	
V_{IL}	Input Low Voltage		–0.3	0.65	V	
V_{IH}	Input High Voltage		2.2	V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 2$ mA
V_{OH}	Output High Voltage		2.4		V	$I_{OH} = -1$ mA

Capacitance

Symbol	Parameter	Limits Min.	Limits Max.	Units	Conditions
C_{IN}	Input Capacitance		8	pF	$V_{IN} = 0V$, on all Input Pins
C_O	Output Capacitance		12	pF	$V_O = 0V$

A.C. Characteristics for Read Cycle: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Unless otherwise specified)

Symbol	Parameter	S5101L1 Limits		S5101L S5101L3 Limits		S5101L8 S5101-8 Limits		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{RC}	Read Cycle Time	450		650		800		ns	
T_{ACC}	Access Time		450		650		800	ns	
T_{CO1}	$\overline{CE1}$ to Output Delay		400		600		800	ns	
T_{CO2}	CE2 to Output Delay		500		700		850	ns	See A.C. Conditions of Test and A.C. Test Load
T_{OD}	Output Disable to Enabled Output Delay		250		350		450	ns	
T_{DF}	Output Disable to Output H-Z State Delay	0	130	0	150	0	200	ns	
T_{OH1}	Output Data Valid Into Next Cycle with respect to Address	0		0		0		ns	
T_{OH2}	Output Data Valid Into Next Cycle with respect to Chip Enable	0		0		0		ns	

Read Cycle
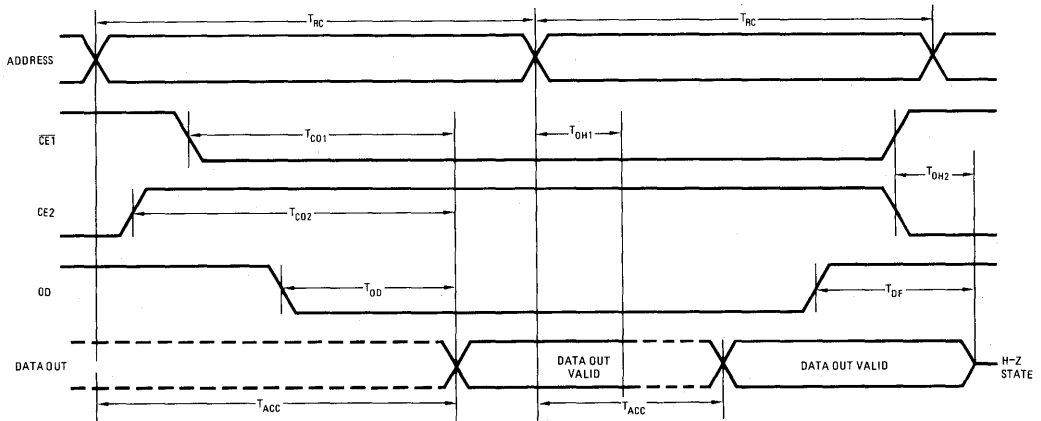
1076145

Note:
1. OD may be tied low for seaprate I/O information.
2. The output will go into a high impedance state if either CE1 is high, CE2 is low, OD is high or R/W is low.

A.C. Characteristics for Write Cycle — Separate or Common Data I/O Using Output Disable

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Unless otherwise specified)

Symbol	Parameter	S5101L1 Limits		S5101L S5101L3 Limits		S5101L8 S5101-8 Limits		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{WC}	Write Cycle Time	450		650		800		ns	
T_{AW}	Address To Write Delay	130		150		200		ns	
T_{CW1}	CE1 to Write Delay	350		550		650		ns	See A.C.
T_{CW2}	CE2 to Write Delay	350		550		650		ns	Conditions
T_{DW}	Data Set-Up to End of Write Time	250		400		450		ns	of Test and A.C.
T_{DH}	Data Hold After End of Write Time	50		100		100		ns	Test Load
T_{WP}	Write Pulse Width	250		400		450		ns	
T_{WR}	End of Write to New Address Recovery Time	50		50		100		ns	
T_{DS}	Output Disable to Data-In Set-Up Time	130		150		200		ns	

Write Cycle — For Separate or Common Data I/O
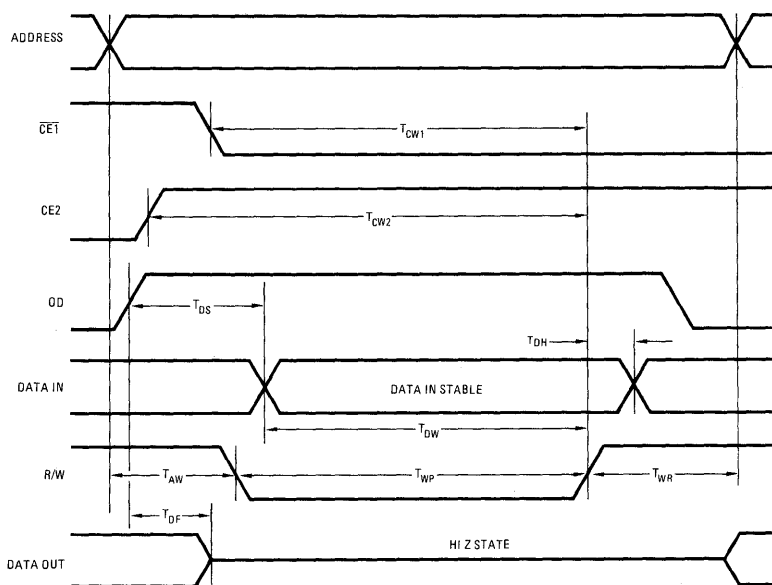
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Low V$_{CC}$ Data Retention Characteristics for S5101L, S5101L1, S5101L3 and S5101L8 [1]
T$_A$ = 0°C to 70°C

Symbol	Parameter		Min.	Max.	Units	Conditions
V$_{DR}$	V$_{CC}$ for Data Retention		2.0		V	CE2 ≤ 0.2V
I$_{CCDR}$	Data Retention Supply Current	S5101L1, S5101L		10	μA	V$_{CC}$ = V$_{DR}$
		S5101L3		140	μA	T$_R$ = T$_F$ = 20ns
		S5101L8		500	μA	CE2 ≤ 0.2V
T$_{CRD}$	Chip Deselect to Data Retention Time		0		ns	
T$_R$	Operation Recovery Time		T$_{RC}$[2]		ns	

Notes:
[1] For guaranteed low V$_{CC}$ Data Retention @ 2.0V, order must specify S5101L, S5101L1, S5101L3 or S5101L8.
[2] T$_{RC}$ = Read Cycle Time.

Low V$_{CC}$ Data Retention Wave Form


```
1.  4.75V
2.  V_DR
3.  V_IH
4.  0.2V
```

477215

A.C. Test Load

1076146

A.C. Conditions of Test

Input Levels	0.65V to 2.2V
Input Rise and Fall Time	20ns
Timing Measurement Reference Level	1.5V
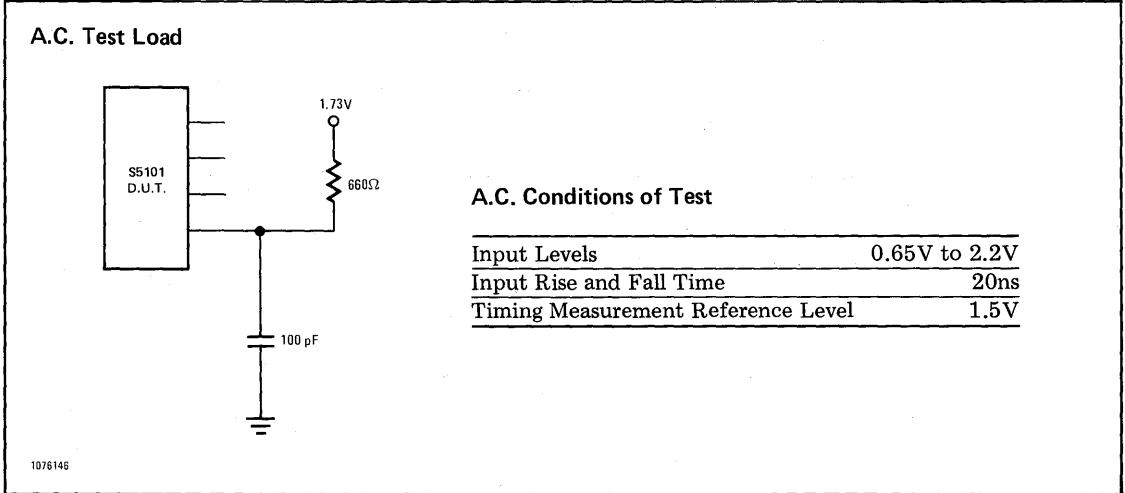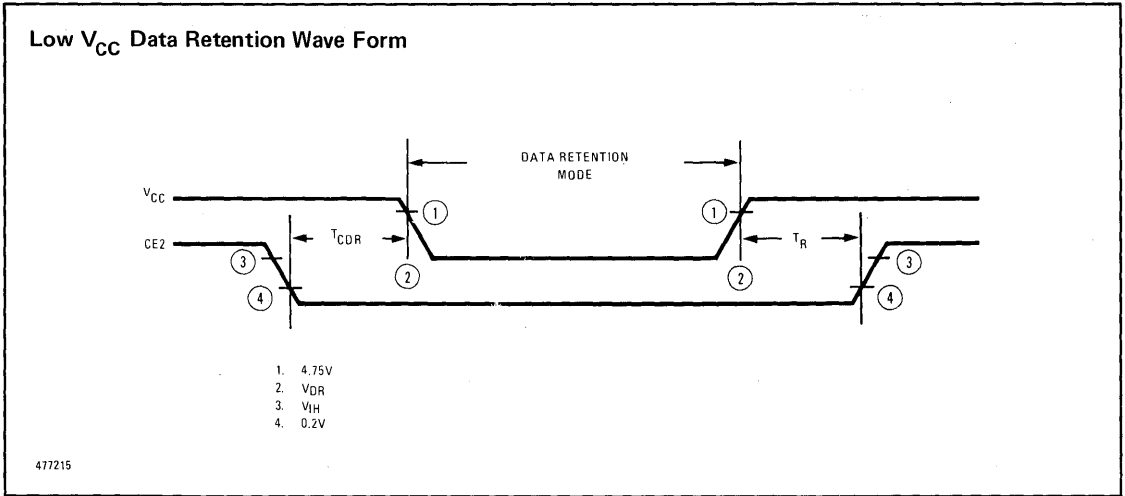
1024 BIT (1024 x 1) STATIC CMOS RAM

RAMs

Features

☐ Ultra Low Standby Power

☐ S6508 Completely TTL Compatible

☐ S6508A Completely CMOS Compatible

☐ 4V to 11V Operation (S6508A)

☐ Data Retention at 2V

☐ Three-State Output

☐ Low Operating Power: 10mW @ 1MHz (5V)

☐ Fast Access Time: 115ns @ 10V

General Description

The AMI S6508 family of 1024x1 bit static CMOS RAMs offers ultra low power dissipation with a single power supply. The device is available in two versions. The basic part (S6508) operates on 5V and is directly TTL compatible on all inputs and the three-state output. The S6508 "A" operates from 4V to 11V and is fully CMOS compatible. The data is stored in ultra low power CMOS static RAM cells (six transistor). The stored data is read out nondestructively and is the same polarity as the original input data. The address is buffered by on-chip address registers. These internal registers are latched by the HIGH to LOW transition of chip enable ($\overline{CE}$). The write enable and chip enable functions are designed such that either separate or common data I/O operations can be easily implemented for maximum design flexibility.

Block Diagram

Logic Symbol

Pin Configuration

Pin Names

A0-A9	Address Inputs	$\overline{CE}$	Chip Enable
D_{IN}	Data Input	$\overline{WE}$	Write Enable
D_{OUT}	Data Output	V_{CC}	Power Supply
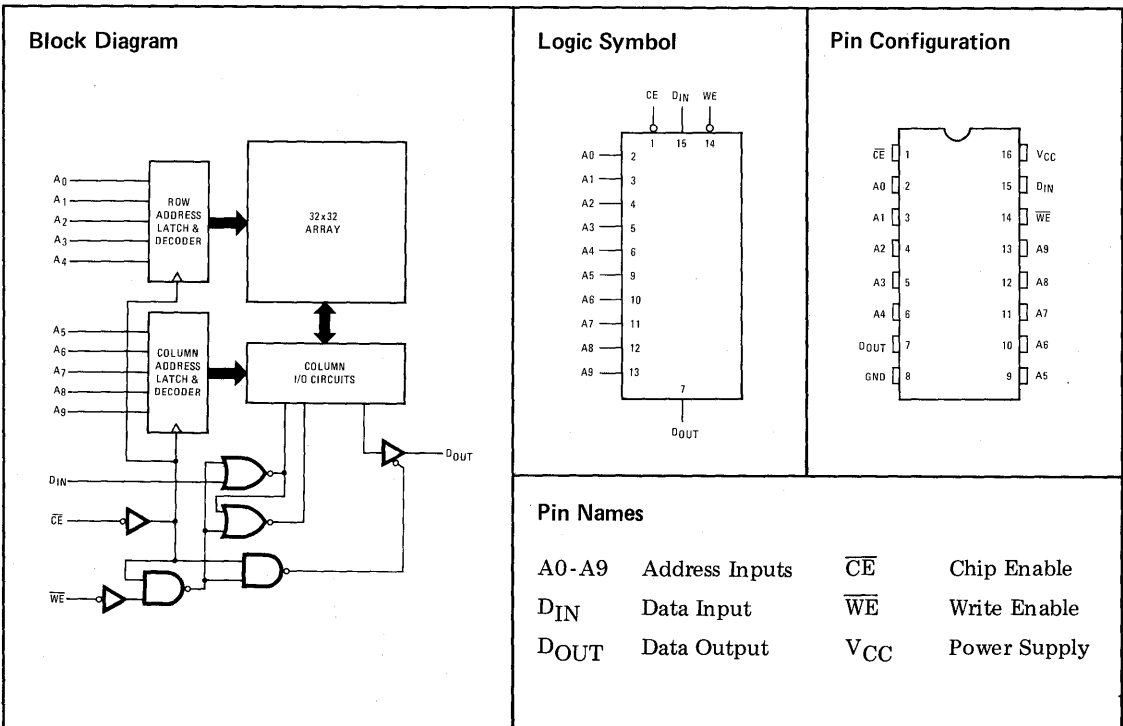
General Description (Continued)

The S6508 is fabricated using a silicon gate CMOS process suitable for high volume production of high performance, ultra low power memories. When deselected ($\overline{CE}$ = HIGH), the S6508-1 draws less than 10 microamps from the 5V supply. In addition, it offers guaranteed data retention with the power supply as low as 2 volts. This process makes the device an ideal choice where battery augmented nonvolatile RAM storage is mandatory.

CMOS to TTL — S6508/S6508-1
Absolute Maximum Ratings

Supply Voltage 8.0V
Input or Output Voltage Supplied .... GND – 0.5V to V_{CC} + 0.5V
Storage Temperature Range .... –65°C to 150°C
Operating Temperature Range, Commercial .... 0°C to 70°C

D.C. Characteristics (V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Units	Conditions
V_{IH}	Logical "1" Input Voltage		V_{CC}- 2.0		V	
V_{IL}	Logical "0" Input Voltage			0.8	V	
I_{IL}	Input Leakage		-1.0	1.0	μA	$0V < V_{IN} < V_{CC}$
V_{OH2}	Logical "1" Output Voltage		V_{CC}- 0.01		V	I_{OUT} = 0
V_{OH1}	Logical "1" Output Voltage		2.4		V	I_{OH} = - 0.2mA
V_{OL2}	Logical "0" Output Voltage			GND + 0.01	V	I_{OUT} = 0
V_{OL1}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage		-1.0	1.0	μA	$0V < V_O < V_{CC}$, $\overline{CE}$ = V_{IH}
I_{CCL}	Standby Supply Current	S6508		100	μA	V_{IN} = V_{CC}
		S6508-1		10	μA	
I_{CC}	Supply Current S6508/S6508-1			2.5	mA	f = 1MHz
C_{IN}	Input Capacitance			7.0	pF	
C_O	Output Capacitance			10.0	pF	

A.C. Characteristics (V_{CC} = 5.0V ± 10%, C_L = 50pF (One TTL Load), T_A = 0°C to 70°C)

Symbol	Parameter	S6508-1		S6508		Units	Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Access Time from $\overline{CE}$		300		460	ns	
t_{EN}	Output Enable Time		180		285	ns	
t_{DIS}	Output Disable Time		180		285	ns	
t_{CEH}	$\overline{CE}$ HIGH	200		300		ns	
t_{CEL}	$\overline{CE}$ LOW	300		460		ns	See A.C. conditions of test and A.C. test load.
t_{WP}	Write Pulse Width (LOW)	200		300		ns	
t_{AS}	Address Setup Time	7		15		ns	
t_{AH}	Address Hold Time	90		130		ns	
t_{DS}	Data Setup Time	200		300		ns	
t_{DH}	Data Hold Time	0		0		ns	
t_{MOD}	Data Modify Time	0		0		ns	

CMOS to CMOS — S6508A/S6508A-1

Absolute Maximum Ratings

Supply Voltage 12.0V
Input or Output Voltage Applied .... −0.5V to V_{CC} + 0.5V
Storage Temperature Range .... −65°C to 150°C
Operating Temperature Range, Commercial .... 0°C to 70°C

D.C. Characteristics (V_{CC} = 4V to 11V, T_A = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Units	Conditions
V_{IH}	Logical "1" Input Voltage		70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage		−1.0	1.0	μA	$0V < V_{IN} < V_{CC}$
V_{OH}	Logical "1" Output Voltage		V_{CC}− 0.01		V	$I_{OUT} = 0$
V_{OL}	Logical "0" Output Voltage			GND+0.01	V	$I_{OUT} = 0$
I_O	Output Leakage		−1.0	1.0	μA	$0V < V_O < V_{CC}$, $\overline{CE} = V_{IH}$
I_{CCL}	Standby Supply Current	S6508A		500	μA	$V_{IN} = V_{CC}$
		S6508A-1		100	μA	
I_{CC}	Supply Current (S6508A/S6508A-1)	$V_{CC} = 5V$		2.5	mA	f = 1MHz
		$V_{CC} = 10V$		5.0	mA	
C_{IN}	Input Capacitance			7.0	pF	
C_O	Output Capacitance			10.0	pF	

A.C. Characteristics (V_{CC} = V_{CC} ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	V_{CC}	S6508A-1 Min.	S6508A-1 Max.	S6508A Min.	S6508A Max.	Units	Conditions
t_{ACC}	Access Time from $\overline{CE}$	5V		275		460	ns	
		10V		115		185	ns	
t_{EN}	Output Enable Time	5V		165		285	ns	
		10V		75		120	ns	
t_{DIS}	Output Disable Time	5V		165		285	ns	
		10V		75		120	ns	
t_{CEH}	$\overline{CE}$ HIGH	5V	175		300		ns	
		10V	80		125		ns	
t_{CEL}	$\overline{CE}$ LOW	5V	275		460		ns	
		10V	115		185		ns	
t_{WP}	Write Pulse Width (LOW)	5V	175		300		ns	See A.C. conditions of test and A.C. test load.
		10V	80		125		ns	
t_{AS}	Address Setup Time	5V	7		15		ns	
		10V	7		15		ns	
t_{AH}	Address Hold Time	5V	80		130		ns	
		10V	40		60		ns	
t_{DS}	Data Setup Time	5V	175		300		ns	
		10V	80		125		ns	
t_{DH}	Data Hold Time	5V	0		0		ns	
		10V	0		0		ns	
t_{MOD}	Data Modify Time	5V	0		0		ns	
		10V	0		0		ns	

Read Cycle

Write Cycle

Read Modify Write Cycle

NOTES:

1. The write operation is terminated on any positive edge of Chip Enable ($\overline{CE}$) or Write Enable ($\overline{WE}$).
2. The data output will be in the high impedance state whenever $\overline{WE}$ is LOW.
3. $\overline{WE}$ is HIGH during a read operation.
4. Rise and fall times of V_{CC} equal 20ns.

2.28

RAMs

Low V_{CC} Data Retention Characteristics ($T_A = 0°C$ to $70°C$)

Symbol	Parameter		Min.	Max.	Units	Conditions
V_{DR}	V_{CC} for Data Retention		2.0		V	$\overline{CE} = 2.0V$
I_{CCDR}	Data Retention Supply Current	S6508, S6508A		10	μA	$V_{CC} = V_{DR}$ Min.
		S6508-1, S6508A-1		1.0	μA	$V_{IN} = V_{CC}$
t_{CDR}	Deselect Setup Time		t_{CEH}		ns	
t_R	Recovery Time		t_{CEH}		ns	

Low V_{CC} Data Retention Waveform (note 4)
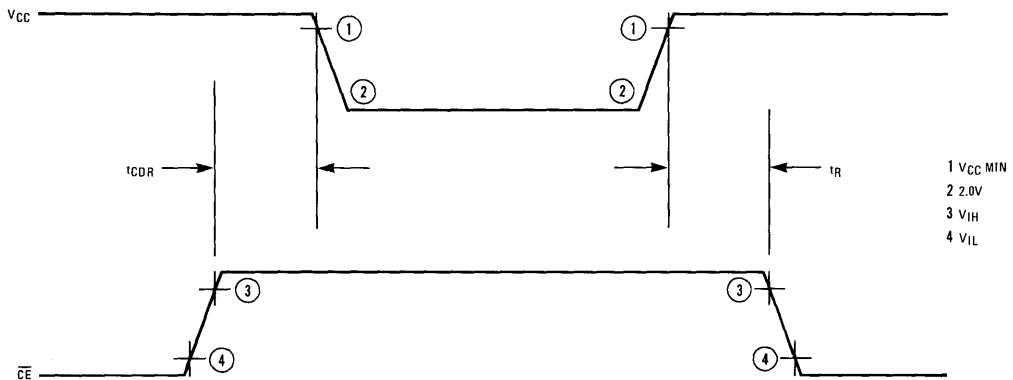
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A.C. Test Load

A.C. Test Conditions

Input Levels .... V_{IL} to V_{IH}
Input Rise & Fall 20ns
Timing Measurement Reference Level
   S6508/S6508-1 .... 1.5V
   S6508A/S6508-1 .... 50% V_{CC}

877244

2.29

1024 BIT (1024x1) STATIC CMOS RAM

Features

☐ Ultra Low Standby Power

☐ S6518 Completely TTL Compatible

☐ S6518A Completely CMOS Compatible

☐ 4V to 11V Operation (S6518A)

☐ Data Retention at 2V

☐ Three-State Output

☐ Low Operating Power: 10mW @1MHz (5V)

☐ Fast Access Time: 115ns @10V

General Description

The AMI S6518 family of 1024x1 bit static CMOS RAMs offers ultra low power dissipation with a single power supply. The device is available in two versions. The basic part (S6518) operates on +5V and is directly TTL compatible on all inputs and the three-state output. The S6518 "A" operates from +4V to +11V and is fully CMOS compatible. The data is stored in ultra low power CMOS six transistor static RAM cells. The data is read out non-destructively (into a data latch) and is the same polarity as the original input data. The address is buffered by on-chip address registers. These internal registers are latched by the HIGH to LOW transition of chip enable ($\overline{CE}$). In addition, there are two chip selects ($\overline{CS1}$ and $\overline{CS2}$) which facilitate memory expansion. The write enable, chip enable and chip select functions are designed such that either separate or common data I/O operations can be easily implemented.

Block Diagram

Pin Names

$A_0 - A_9$	Address Inputs	$\overline{CS1}$, $\overline{CS2}$	Chip Selects
D_{IN}	Data Input	$\overline{WE}$	Write Enable
D_{OUT}	Data Output	V_{CC}	Power Supply
$\overline{CE}$	Chip Enable		

Logic Symbol

Pin Configuration

Truth Table

Inputs					Output	Mode
$\overline{CE}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{WE}$	D_{IN}	D_{OUT}	
L	L	L	L	L	Hi-Z	Write "0"
L	L	L	L	H	Hi-Z	Write "1"
L	L	L	H	X	D_{OUT}	Read
X	H	X	X	X	Hi-Z	Deselected
X	X	H	X	X	Hi-Z	Deselected
H	X	X	L	X	Hi-Z	Deselected
H	L	L	H	X	D_{OUT}	Output Latched To Last Data
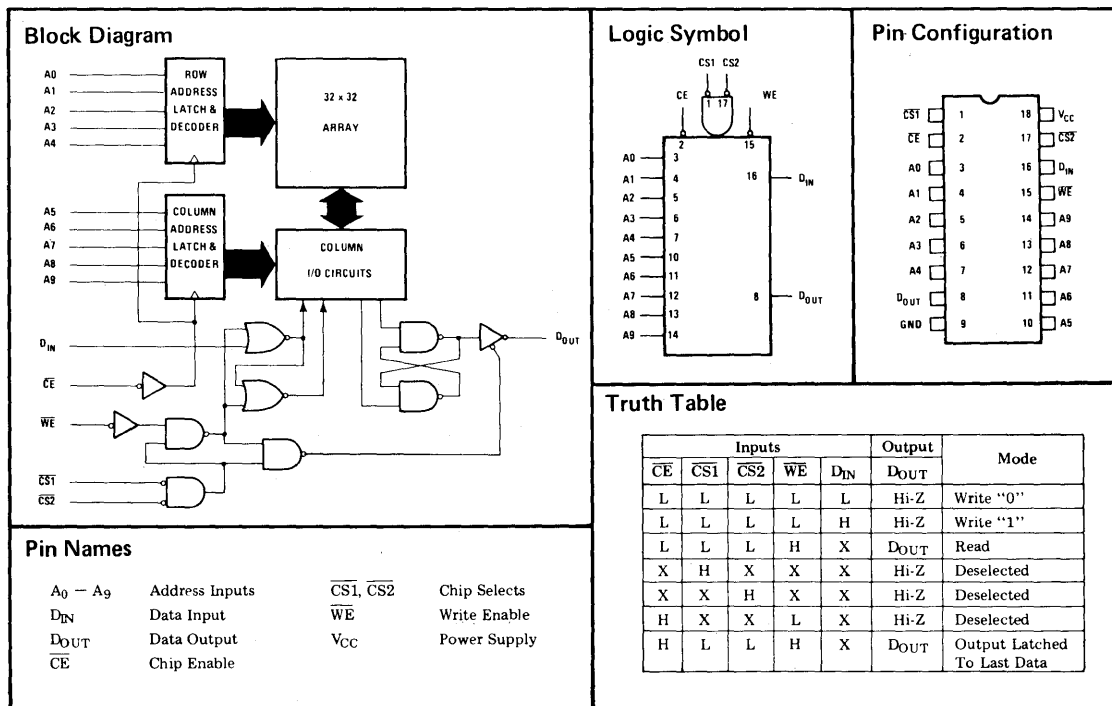
General Description (Continued)

The S6518 is fabricated using a silicon gate CMOS process suitable for high volume production of high performance, ultra low power memories. When de-selected ($\overline{CE}$ = HIGH, $\overline{CS1}$ or $\overline{CS2}$ = HIGH), the S6518-1 draws less than 10 microamps from the +5V supply. In addition, the S6518 family offers guaranteed data retention with the power supply as low as 2 volts. This makes the device an ideal choice when battery augmented non-volatile RAM storage is mandatory.

CMOS to TTL — S6518/S6518-1
Absolute Maximum Ratings

Supply Voltage 8.0V
Input or Output Voltage Supplied .... GND – 0.5V to V_{CC} + 0.5V
Storage Temperature Range .... –65°C to 150°C
Operating Temperature Range, Commercial .... 0°C to 70°C

D.C. Characteristics (V_{CC} = 0.5V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Units	Conditions
V_{IH}	Logical "1" Input Voltage		V_{CC} - 2.0		V	
V_{IL}	Logical "0" Input Voltage			0.8	V	
I_{IL}	Input Leakage		– 1.0	1.0	μA	$0V < V_{IN} < V_{CC}$
V_{OH2}	Logical "1" Output Voltage		V_{CC} - 0.01		V	I_{OUT} = 0
V_{OH1}	Logical "1" Output Voltage		2.4		V	I_{OH} = - 0.2mA
V_{OL2}	Logical "0" Output Voltage			GND +0.01	V	I_{OUT} = 0
V_{OL1}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage		– 1.0	1.0	μA	$0V < V_O < V_{CC}$, $\overline{CS1}$ or $\overline{CS2}$ = V_{IH}
I_{CCL}	Standby	S6518		100	μA	$V_{IN} = V_{CC}$
	Supply Current	S6518-1		10	μA	
I_{CC}	Supply Current S6518/S6518-1			2.5	mA	f = 1MHz
C_{IN}	Input Capacitance			7.0	pF	
C_O	Output Capacitance			10.0	pF	

A.C. Characteristics (V_{CC} = 5.0V ± 10%, C_L = 50pF (One TTL Load), T_A = 0°C to 70°C)

Symbol	Parameter	S6518-1		S6518		Units	Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Access Time from $\overline{CE}$		300		460	ns	
t_{EN}	Output Enable Time		180		285	ns	
t_{DIS}	Output Disable Time		180		285	ns	
t_{CEH}	$\overline{CE}$ HIGH	200		300		ns	
t_{CEL}	$\overline{CE}$ LOW	300		460		ns	See A.C. conditions of
t_{WP}	Write Pulse Width (LOW)	200		300		ns	test and A.C. test load.
t_{AS}	Address Setup Time	7		15		ns	
t_{AH}	Address Hold Time	90		130		ns	
t_{DS}	Data Setup Time	200		300		ns	
t_{DH}	Data Hold Time	0		0		ns	
t_{MOD}	Data Modify Time	0		0		ns	

CMOS to CMOS — S6518A/S6518A-1
Absolute Maximum Ratings

Supply Voltage 12.0V
Input or Output Voltage Applied .... −0.5V to V_{CC} + 0.5V
Storage Temperature Range .... −65°C to 150°C
Operating Temperature Range, Commercial .... 0°C to 70°C

D.C. Characteristics (V_{CC} = 4V to 11V, T_A = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Units	Conditions
V_{IH}	Logical "1" Input Voltage		70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage		−1.0	1.0	μA	$0V < V_{IN} < V_{CC}$
V_{OH}	Logical "1" Voltage		V_{CC}−0.01		V	I_{OUT} = 0
V_{OL}	Logical "0" Voltage			GND+0.01	V	I_{OUT} = 0
I_O	Output Leakage		−1.0	1.0	μA	$0 < V_O < V_{CC}$, $\overline{CS1}$ or $CS2 = V_{IH}$
I_{CCL}	Standby	S6518A		500	μA	$V_{IN} = V_{CC}$
	Supply Current	S6518A-1		100	μA	
I_{CC}	Supply Current (S6518A/S6518A-1)	V_{CC} = 5V		2.5	mA	f = 1MHz
		V_{CC} = 10V		5.0	mA	
C_{IN}	Input Capacitance			7.0	pF	
C_O	Output Capacitance			10.0	pF	

A.C. Characteristics (V_{CC} = V_{CC} ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	V_{CC}	S6518A-1 Min.	S6518A-1 Max.	S6518A Min.	S6518A Max.	Units	Conditions
t_{ACC}	Access Time from $\overline{CE}$	5V		275		460	ns	See A.C. conditions of test and A.C. test load.
		10V		115		185	ns	
t_{EN}	Output Enable Time	5V		165		285	ns	
		10V		75		120	ns	
t_{DIS}	Output Disable Time	5V		165		285	ns	
		10V		75		120	ns	
t_{CEH}	$\overline{CE}$ HIGH	5V	175		300		ns	
		10V	80		125		ns	
t_{CEL}	$\overline{CE}$ LOW	5V	275		460		ns	
		10V	115		185		ns	
t_{WP}	Write Pulse Width (LOW)	5V	175		300		ns	
		10V	80		125		ns	
t_{AS}	Address Setup Time	5V	7		15		ns	
		10V	7		15		ns	
t_{AH}	Address Hold Time	5V	80		130		ns	
		10V	40		60		ns	
t_{DS}	Data Setup Time	5V	175		300		ns	
		10V	80		125		ns	
t_{DH}	Data Hold Time	5V	0		0		ns	
		10V	0		0		ns	
t_{MOD}	Data Modify Time	5V	0		0		ns	
		10V	0		0		ns	

Read Cycle

Write Cycle

Read Modify Write Cycle

Notes:
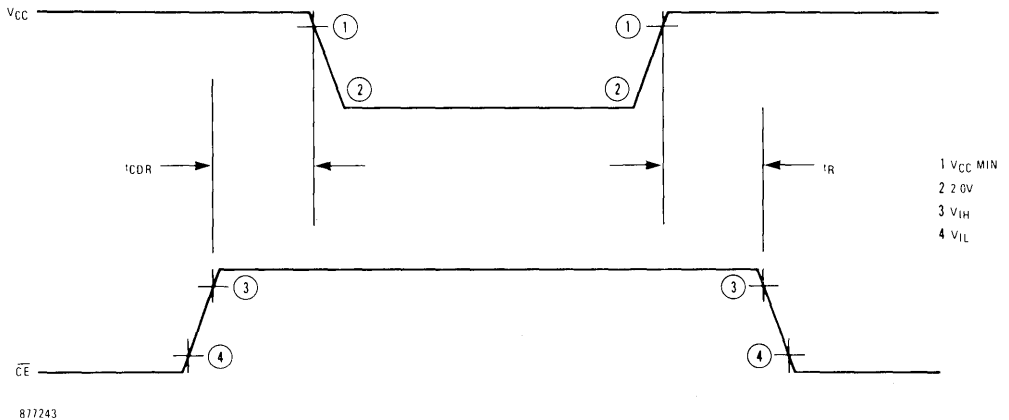1. The write operation occurs when $\overline{CE} = \overline{CS1} = \overline{CS2} = \overline{WE} = LOW$. The write operation is terminated on any positive edge of $\overline{CS1}$, $\overline{CS2}$, $\overline{CE}$ or $\overline{WE}$.
2. The data output will be in the high impedance state whenever $\overline{WE}$ is LOW.
3. $\overline{WE}$ is HIGH during a read operation.
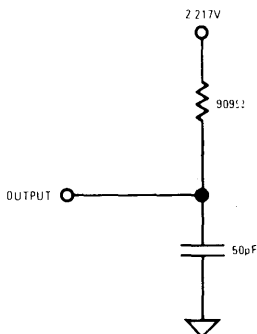4. Rise and fall times of V_{CC} equal 20ns.

Low V$_{CC}$ Data Retention Characteristics (T$_A$ = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Units	Conditions
V$_{DR}$	V$_{CC}$ for Data Retention		2.0		V	$\overline{CE}$ = 2.0V
I$_{CCDR}$	Data Retention Supply Current	S6518, S6518A		10	μA	V$_{CC}$ = V$_{DR}$ Min.
		S6518-1, S6518A-1		1.0	μA	V$_{IN}$ = V$_{CC}$
t$_{CDR}$	Deselect Setup Time		t$_{CEH}$		ns	
t$_R$	Recovery Time		t$_{CEH}$		ns	

Low V$_{CC}$ Data Retention Waveform (note 4)

877243

A.C. Test Load

2 217V

909Ω

OUTPUT

50pF

877244

A.C. Test Conditions

Input Levels .... V$_{IL}$ to V$_{IH}$

Input Rise & Fall 20ns

Timing Measurement Reference Level

S6518/S6518-1 .... 1.5V

S6518A/S6518A-1 .... 50% V$_{CC}$

AMI®

16,384 BIT (2048 x 8) STATIC VMOS ROM

Features

☐ Fast Access Time: 250ns Maximum

☐ Fully Static Operation

☐ Single +5V ± 10% Power Supply

☐ Directly TTL Compatible Inputs

☐ Three-State TTL Compatible Outputs

☐ Three Programmable Chip Selects

☐ EPROM Pin Compatible

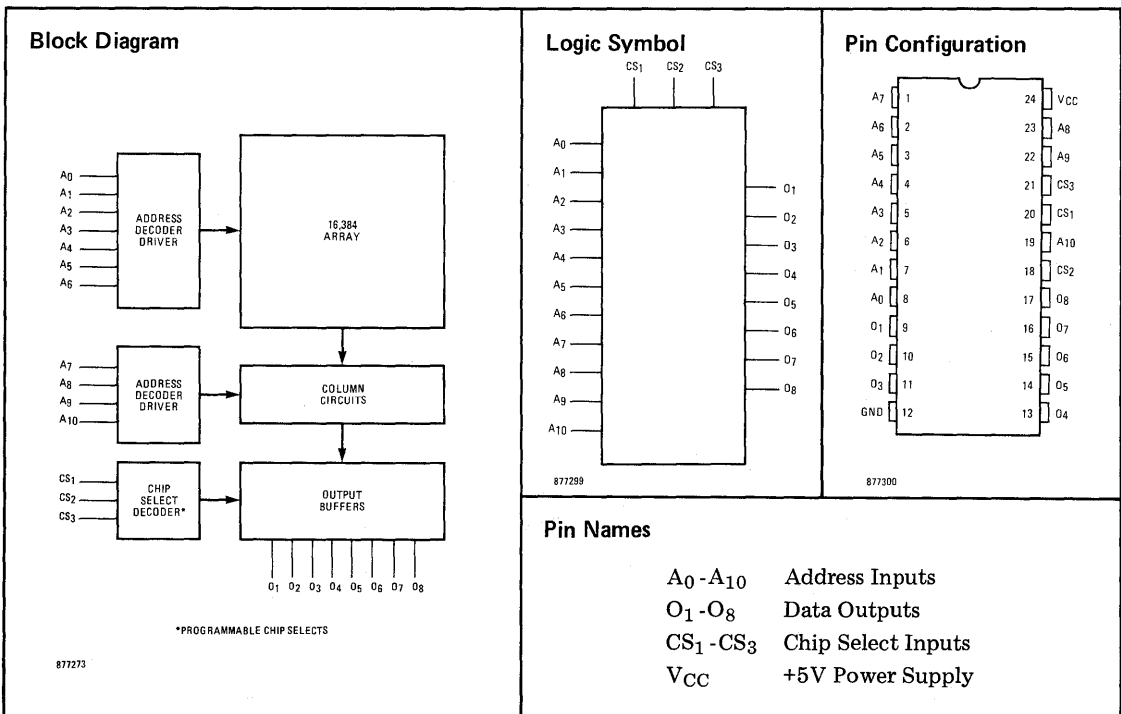☐ Fan-Out of 5 TTL: I_{OL} = 8mA @ 0.4V

General Description

The AMI S4216B is a 16,384 bit static mask programmable VMOS ROM organized as 2048 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has single + 5V power suply. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S4216B is fully compatible with 16K UV EPROMs (+ 5V version) making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The three chip selects are mask programmable, the active level for each being specified by the user.

The S4216B is fabricated using AMI's proprietary N-Channel VMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

877273

*PROGRAMMABLE CHIP SELECTS

Logic Symbol

877299

Pin Configuration

877300

Pin Names

A_0 -A_{10}	Address Inputs
O_1 -O_8	Data Outputs
CS_1 -CS_3	Chip Select Inputs
V_{CC}	+5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias .... $-10°C$ to $80°C$
Storage Temperature .... $-65°C$ to $150°C$
Output or Supply Voltage .... $-0.5V$ to $7V$
Input Voltage .... $-0.5V$ to $5.5V$
Power Dissipation 1W

*Comment:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. Characteristics:** $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 8\,mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -800\mu A$
V_{IL}	Input LOW Voltage	-0.3		0.8	V	
V_{IH}	Input HIGH Voltage	2.2		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to $5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_O = 0.4$ to $5.5V$, Chip Deselected
I_{CC}	Power Supply Current			90	mA	$V_{CC} = Max.$, $T_A = 0°C$, Outputs Open

Capacitance: $T_A = 25°C$, $f = 1Mhz$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics: $T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			250	ns	See A.C. Test
t_{ACS}	Chip Select Access Time			100	ns	Conditions
t_{OFF}	Chip Select Turn-off Time			100	ns	& Waveforms
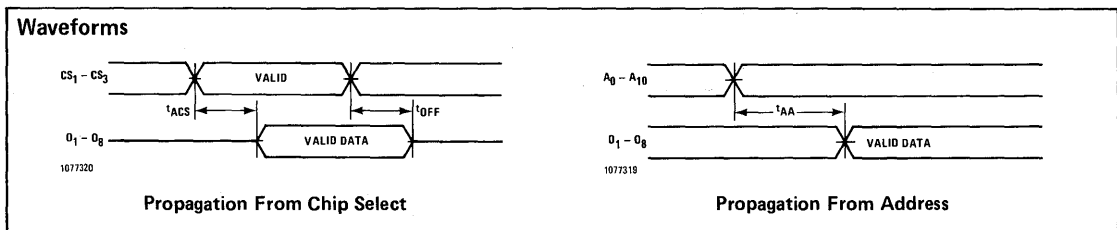
Waveforms

Propagation From Chip Select

Propagation From Address

A.C. Test Conditions

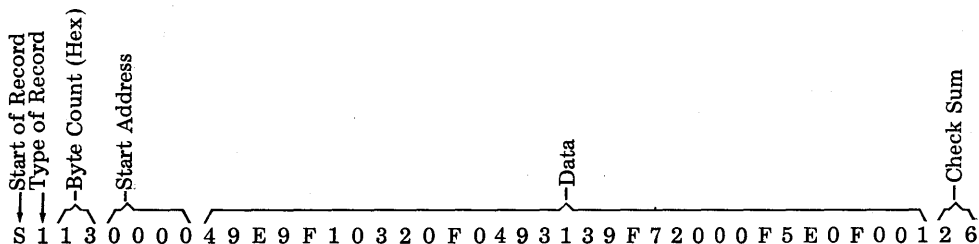|	
Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10ns
Input/Output Timing Levels	1.5V

A.C. Test Load

1077318

ROMs

Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	Start of record (Letter S)
2	Type of record
	0 — Header record (comments)
	1 — Data record
	9 — End of file record
3, 4	Byte Count
	Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	Address Value
	The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	Data
	Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	Checksum
	The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example: S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C

NOTES:
1. Only positive logic formats for E_0, E_1, E_2 are accepted. $1 = V_{HIGH}$; $0 = V_{LOW}$
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

AMI®

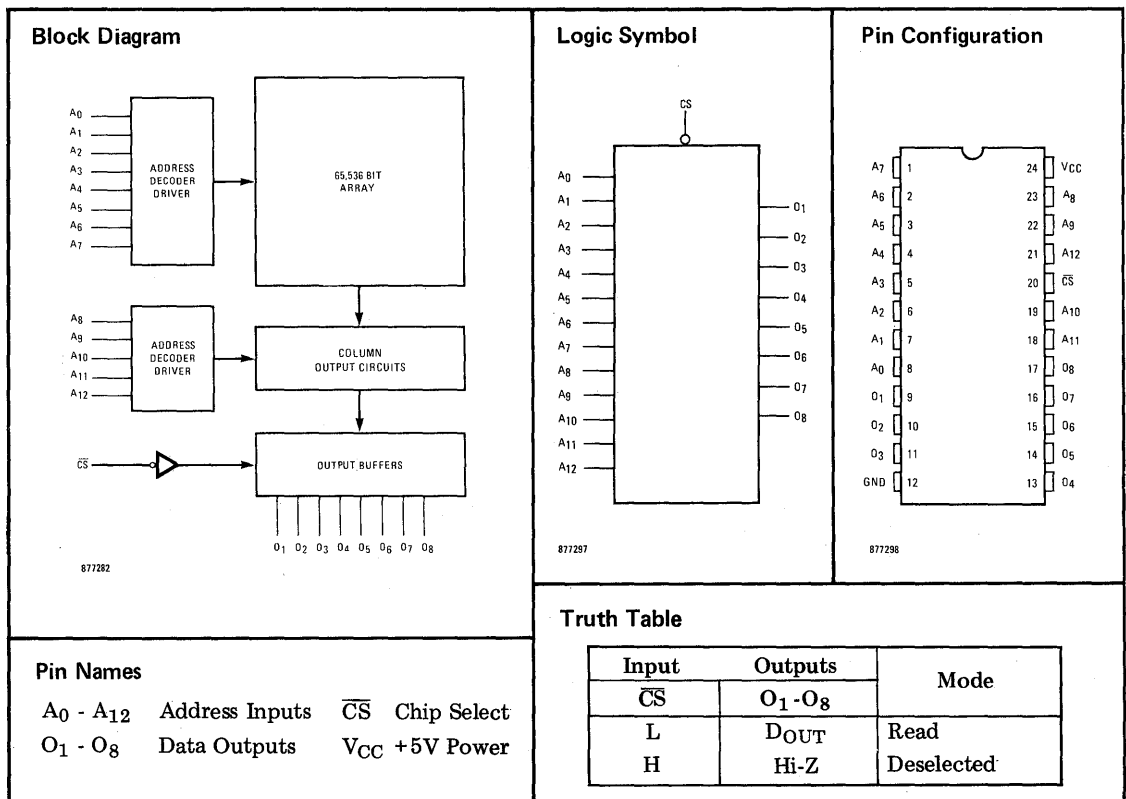# 65,536 BIT (8192 x 8) STATIC VMOS ROM

Features

☐ Single +5V ± 10% Power Supply

☐ High Performance:
  Maximum Access Time: 350ns

☐ EPROM Compatible for Cost Effective
  System Development

☐ Completely Static Operation

☐ Directly TTL Compatible Inputs

☐ Three-State TTL Compatible Outputs

☐ Fan-out of 5 TTL: I_{OL} = 8mA @ 0.4V

General Description

The AMI S4264 is a 65,536 bit fully static VMOS mask programmable ROM organized as 8192 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single + 5V power supply. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S4264 is fully static requiring no clocks for operation. Data access is simple as no address setup times are required. The byte organization of the S4264 makes it ideal for microprocessor applications.

The S4264 is fabricated using AMI's proprietary VMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

877282

Logic Symbol

877297

Pin Configuration

877298

Pin Names

A_0 - A_{12}	Address Inputs	$\overline{CS}$	Chip Select
O_1 - O_8	Data Outputs	V_{CC}	+5V Power

Truth Table

Input	Outputs	Mode
$\overline{CS}$	O_1-O_8	
L	D_{OUT}	Read
H	Hi-Z	Deselected

Absolute Maximum Ratings*

Ambient Temperature Under Bias	$-10°C$ to $80°C$
Storage Temperature	$-65°C$ to $150°C$
Output or Supply Voltages	$-0.5V$ to $7V$
Input Voltages	$-0.5V$ to $5.5V$
Power Dissipation	$1W$

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 8\,mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -400\mu A$
V_{IL}	Input LOW Voltage	-0.3		0.8	V	
V_{IH}	Input HIGH Voltage	2.2		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to $5.5V$
I_{LO}	Output Leakage Current			50	μA	$\overline{CS} \geqslant 2.4V$, $V_O = 0.4V$ to $5.5V$
I_{CC}	Power Supply Current			145	mA	$V_{CC} = Max.$, $T_A = 0°C$, Outputs Open

Capacitance: $T_A = 25°C$, $f = 1\,MHz$.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			350	ns	See Test Circuit
t_{ACS}	Chip Select Access Time			150	ns	&
t_{OFF}	Chip Deselect Time	0		150	ns	Waveforms

Wave Forms

Propagation Delay From Address — **Propagation Delay From Chip Select**
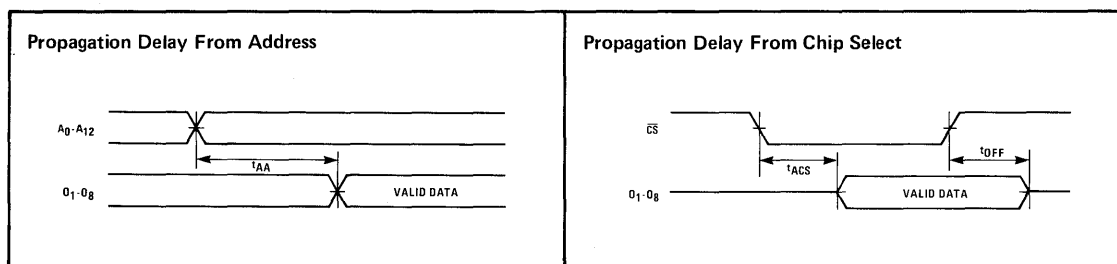
A.C. Test Conditions

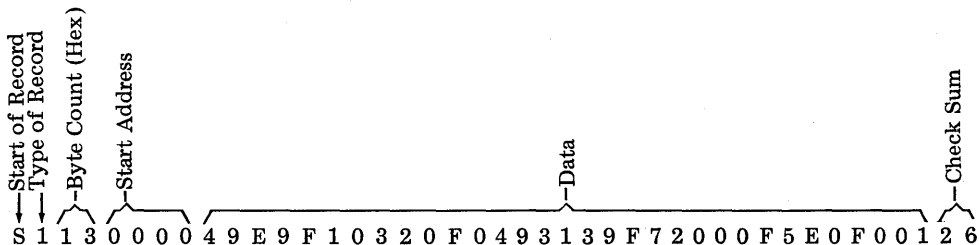|	
Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10ns
Input/Output Timing Levels	1.5V

A.C. Test Load

Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	Start of record (Letter S)
2	Type of record
	0 — Header record (comments)
	1 — Data record
	9 — End of file record
3, 4	Byte Count
	Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	Address Value
	The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	Data
	Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	Checksum
	The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example: S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C

NOTES:
1. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

AMI ®

S6831A/B

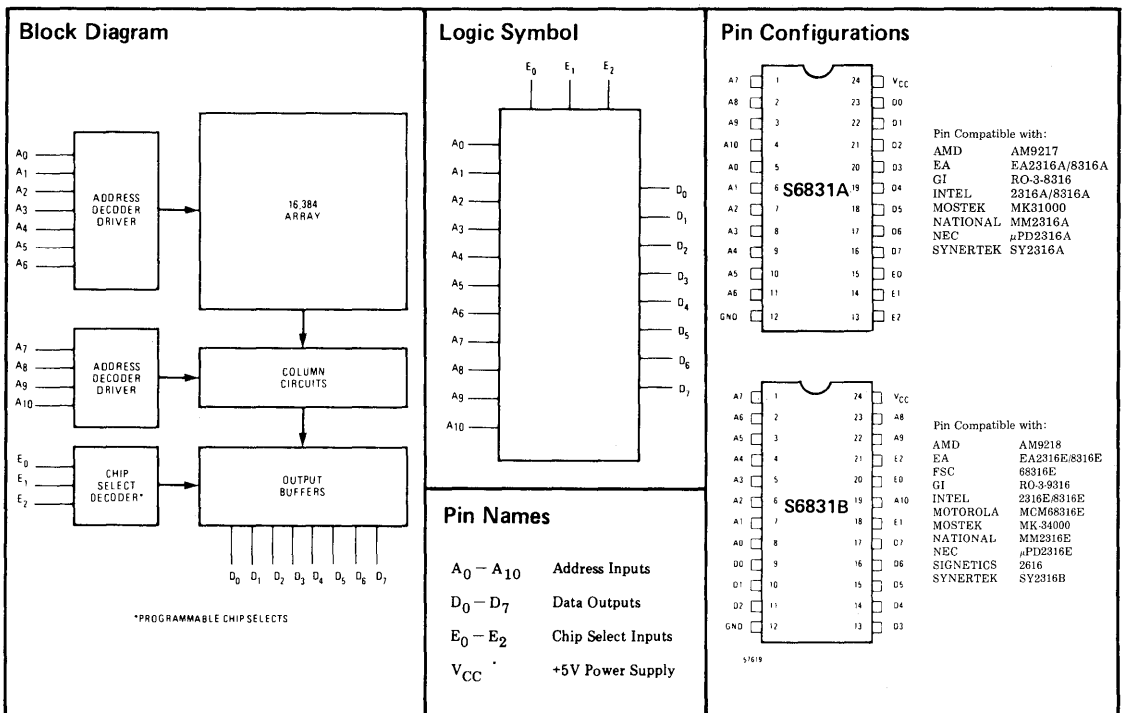# 16,384 BIT (2048x8) STATIC NMOS ROM

Features

- [ ] Single +5V Power Supply
- [ ] Directly TTL Compatible Inputs
- [ ] Three-State TTL Compatible Outputs
- [ ] Three Programmable Enables
- [ ] Access Time: 450ns Maximum
- [ ] S6831A: Intel 2316A Pin Compatible
- [ ] S6831B: 2716 EPROM Pin Compatible
- [ ] Low Power: Supply Current is 80mA Maximum

General Description

The AMI 6831 family of 16,384 bit mask program-mable Read-Only-Memories offers fully static opera-tion with a single + 5V power supply. The device is fully TTL compatible on all inputs and three-state outputs. The three enables are mask programmable, the active level is specified by the user.

The S6831 family is available in two pin configurations. One of these, the S6813A, is the pin configuration of a popular ROM: the Intel 2316A. The second pin configuration, the S6813B, is pin compatible with the 2708 and 2716 EPROMs. Software developed in EPROMs can be put in low cost ROM for high volume production.

The device is organized as 2048 words by 8 bits, a con-figuration particularly suitable for microprocessors. The S6831 family is manufactured with an N-channel silicon gate depletion load technology.

Block Diagram

*PROGRAMMABLE CHIP SELECTS

Logic Symbol

Pin Names

$A_0 - A_{10}$	Address Inputs
$D_0 - D_7$	Data Outputs
$E_0 - E_2$	Chip Select Inputs
V_{CC}	+5V Power Supply

Pin Configurations

Pin Compatible with:

AMD	AM9217
EA	EA2316A/8316A
GI	RO-3-8316
INTEL	2316A/8316A
MOSTEK	MK31000
NATIONAL	MM2316A
NEC	μPD2316A
SYNERTEK	SY2316A

Pin Compatible with:

AMD	AM9218
EA	EA2316E/8316E
FSC	68316E
GI	RO-3-9316
INTEL	2316E/8316E
MOTOROLA	MCM68316E
MOSTEK	MK-34000
NATIONAL	MM2316E
NEC	μPD2316E
SIGNETICS	2616
SYNERTEK	SY2316B

Absolute Maximum Ratings*

Ambient Temperature Under Bias .... $-10°C$ to $80°C$
Storage Temperature .... $-65°C$ to $150°C$
Output or Supply Voltage .... $-0.5V$ to $7V$
Input Voltage .... $-0.5V$ to $5.5V$
Power Dissipation .... $1W$

*Comment: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

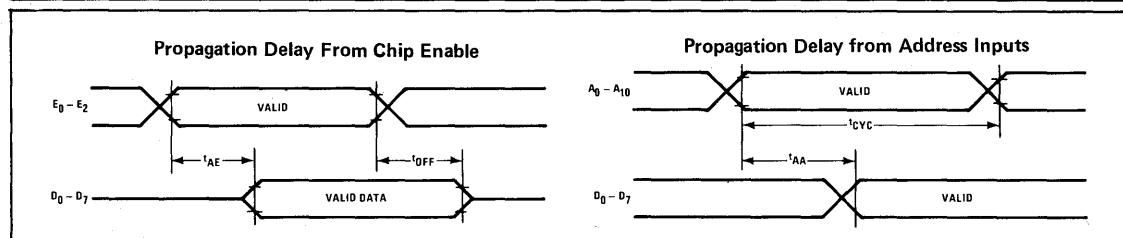**D.C. Characteristics:** $V_{CC} = +5V \pm 5\%$; $T_A = 0°C$ to $+70°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 2.1\,mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -100\mu A$
V_{IL}	Input LOW Voltage	-0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to $5.25V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 0.4$ to $2.4V$, Chip Deselected
I_{CC}	Power Supply Current			70	mA	$V_{CC} = $ Max. $T_A = 25°C$
				80	mA	$V_{CC} = $ Max. $T_A = 0°C$

Capacitance: $f = 1.0$ MHz; $T_A = 25°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7.5	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics: $V_{CC} = +5V \pm 5\%$; $T_A = 0°C$ to $+70°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{CYC}	Read Cycle Time	450			ns	
t_{AA}	Address Access Time			450	ns	See Test Circuit
t_{AE}	Enable Access Time			200	ns	& Waveforms
t_{OFF}	Output Disable Time	10		150	ns	

Propagation Delay From Chip Enable

Propagation Delay from Address Inputs

A.C. Test Conditions

Output Load . . . . 1 TTL Gate and C_L = 100 pF
Input Pulse Levels . . . . 0.8 to 2.4V
Input Rise and Fall Times (10% to 90%) . . . . 20 ns

Timing Measurement Reference Level

Input . . . . 1V and 2.2V
Output . . . . 0.8V and 2.0V

ROMs

Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	Start of record (Letter S)
2	Type of record
	0 — Header record (comments)
	1 — Data record
	9 — End of file record
3, 4	Byte Count
	Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	Address Value
	The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	Data
	Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	Checksum
	The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example: S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
             S 9 0 3 0 0 0 0 F C

NOTES:
1. Only positive logic formats for E_0, E_1, E_2 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should be NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.
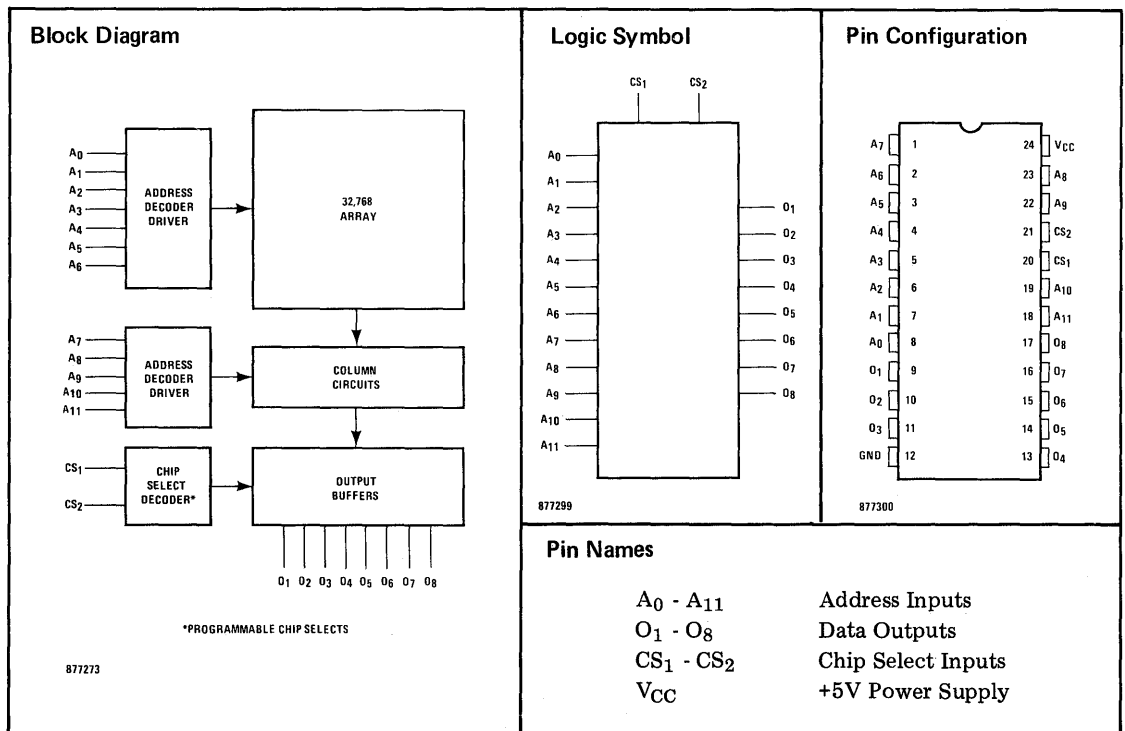
32,768 BIT (4096x8) STATIC NMOS ROM

Features

☐ Fast Access Time: 450ns Maximum

☐ Fully Static Operation

☐ Single +5V ± 10% Power Supply

☐ Directly TTL Compatible Inputs

☐ Three-State TTL Compatible Outputs

☐ Two Programmable Chip Selects

☐ EPROM Pin Compatible

General Description

The AMI S68332 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S68332 is pin compatible with UV EPROMs making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The two chip selects are mask programmable, the active level for each being specified by the user.

The S68332 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

O_1 O_2 O_3 O_4 O_5 O_6 O_7 O_8

*PROGRAMMABLE CHIP SELECTS

877273

Logic Symbol

877299

Pin Configuration

877300

Pin Names

A_0 - A_{11}	Address Inputs
O_1 - O_8	Data Outputs
CS_1 - CS_2	Chip Select Inputs
V_{CC}	+5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias .... $-10°C$ to $80°C$
Storage Temperature .... $-65°C$ to $150°C$
Output or Supply Voltages .... $-0.5V$ to $7V$
Input Voltages .... $-0.5V$ to $5.5V$
Power Dissipation .... $1W$

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 2.1mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -200\mu A$
V_{IL}	Input LOW Voltage	-0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to $5.5V$
I_{LO}	Output Leakage Current			50	μA	$V_O = 0.4V$ to $5.5V$, Chip Deselected
I_{CC}	Power Supply Current			100	mA	$V_{CC} = Max$, $T_A = 0°C$

Capacitance: $T_A = 25°C$, $f = 1$ MHz.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			450	ns	See Test Circuit
t_{ACS}	Chip Select Access Time			150	ns	&
t_{OFF}	Chip Deselect Time	0		150	ns	Waveforms

Waveforms

1077320

Propagation From Chip Select
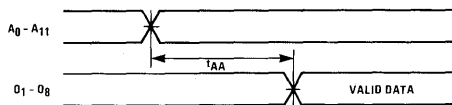
1077319

Propagation From Address

A.C. Test Conditions

Input Pulse Levels .... 0.8V to 2.0V
Input Rise and Fall Times 10ns
Input/Output Timing Levels 1.5V
Output Load .... 1 TTL Load and 100pF

Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	Start of record (Letter S)
2	Type of record
	0 — Header record (comments)
	1 — Data record
	9 — End of file record
3, 4	Byte Count
	Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	Address Value
	The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, ..., N	Data
	Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	Checksum
	The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example: S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
              S 9 0 3 0 0 0 0 F C

S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6

Start of Record — S
Type of Record — 1
Byte Count (Hex) — 1 3
Start Address — 0 0 0 0
Data — 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1
Check Sum — 2 6

NOTES:
1. Only positive logic formats for CS_1 and CS_2 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

AMI®

32, 768 BIT (4096 X 8)
UV ERASABLE VMOS EPROM

Features

☐ **Single +5 Volt Power Supply**

☐ **Fast Access Time: 250ns Maximum**

☐ **Automatic Power Down**

☐ **Pin Compatible with AMI's 32K ROM: S68332**

☐ **Fully TTL Compatible During Read and Program**

☐ **+15V Programming Power Supply: Easy On-Board Programming**

General Description

The S4532 is a 32,768 bit ultraviolet light erasable, electrically programmable read-only memory (EPROM) organized as 4096 words by 8 bits. It is fabricated using AMI's proprietary N-channel VMOS technology. The device is fully static requiring no clocks for operation. All the inputs and outputs are fully TTL compatible during both the read and program modes. The S4532 operates from a single +5V supply (read mode) and has a static power down feature that significantly reduces power dissipation.

The S4532 is pin compatible with AMI's 32K ROM, the S68332. Thus for volume production, the user can switch to lower cost ROM.

The S4532 requires a +15V supply for programming but all the programming signals are TTL compatible. This considerably eases on-board programming.

EPROMS

Block Diagram

Logic Symbol

Pin Configuration

Truth Table

Mode	PD/PGM	Vcc	VPP	Outputs
Read	V_{IL}	+5V	+5V	Data Out
Power Down	V_{IH}	+5V	+5V	High Z
Program	Pulsed V_{IH} to V_{IL} to V_{IH}	+5V	+15V	Data In
Program Inhibit	V_{IH}	+5V	+15V	High Z

Pin Names

$A_0 - A_{11}$	Address Inputs	VCC	+5V Power Supply
$O_1 - O_8$	Data Outputs	VPP	+15V Power Supply
PD/PGM	Power Down Program		

AMI®

16,384 BIT (2048 X 8) UV ERASABLE VMOS EPROM
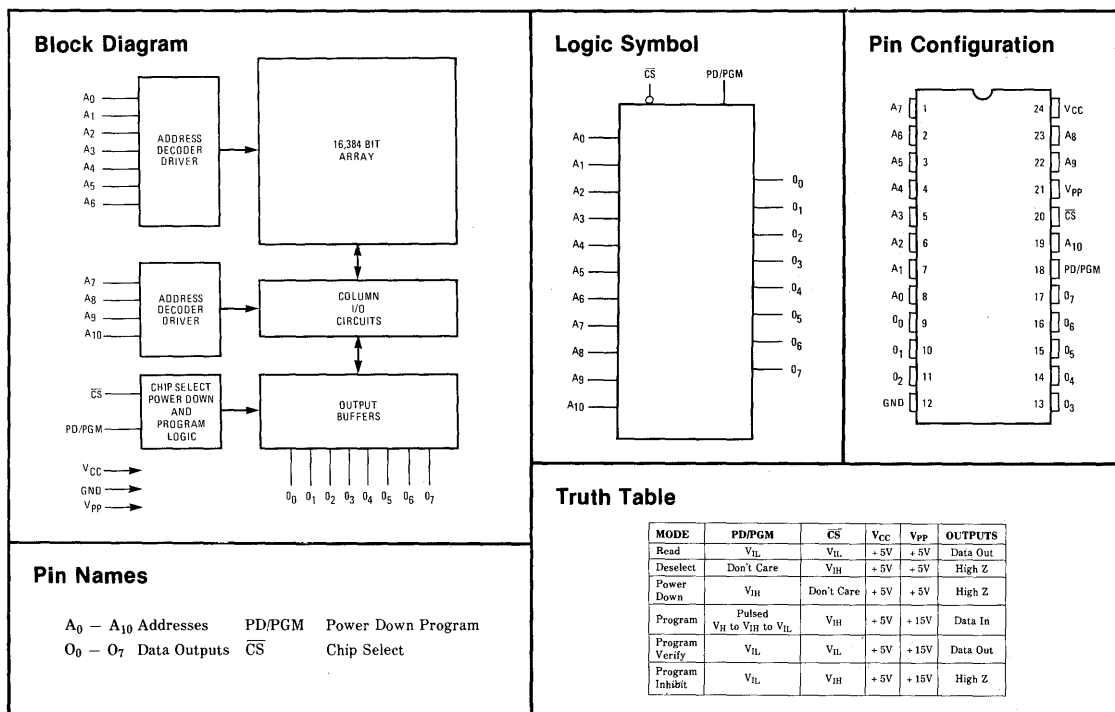
Features

☐ **Single + 5 Volt Power Supply**

☐ **Fast Access Time: 250ns Maximum**

☐ **Pin Compatible with AMI's 16K, 32K and 64K ROMs**

☐ **Low Power Dissipation**
  525mA Maximum Active Power
  132mW Maximum Standby Power

☐ **Fully TTL Compatible During Read and Program**

☐ **+ 15V Programming Power Supply: Easy On-Board Programming**

General Description

The S4716 is a 16,384 bit ultraviolet light erasable, electrically programmable read-only memory (EPROM) organized as 2048 words by 8 bits. It is fabricated using AMI's proprietary N-Channel VMOS technology. The device is fully static requiring no clocks for operation. All the inputs and outputs are fully TTL compatible during both the read and program modes. The S4716 operates from a single + 5V power supply and has a static power down feature that significantly reduces power dissipation.

The S4716 is fully pin compatible with the S4216B and S6831B 16K ROMs, the S68332 32K ROM and the S4264 64K ROM. Thus for volume production, the user can switch to a lower cost ROM.

The S4716 requires a + 15V supply for programming but all the programming signals are TTL. This considerably eases on-board programming.

Block Diagram

Pin Names

A$_0$ — A$_{10}$ Addresses   PD/PGM   Power Down Program

O$_0$ — O$_7$ Data Outputs $\overline{CS}$ Chip Select

Logic Symbol

Pin Configuration

Truth Table

MODE	PD/PGM	$\overline{CS}$	V$_{CC}$	V$_{PP}$	OUTPUTS
Read	V$_{IL}$	V$_{IL}$	+ 5V	+ 5V	Data Out
Deselect	Don't Care	V$_{IH}$	+ 5V	+ 5V	High Z
Power Down	V$_{IH}$	Don't Care	+ 5V	+ 5V	High Z
Program	Pulsed V$_{IH}$ to V$_{IL}$	V$_{IH}$	+ 5V	+ 15V	Data In
Program Verify	V$_{IL}$	V$_{IL}$	+ 5V	+ 15V	Data Out
Program Inhibit	V$_{IL}$	V$_{IH}$	+ 5V	+ 15V	High Z

AMI®

512 × 8 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

Features

☐ On-Board Programmability
☐ Fast Access Time — 750ns Max.
☐ High Speed Programming — Less than 1 Minute for all 4096 Bits
☐ Programmed with R/W, CS and V_{PROG} Pins
☐ Completely TTL Compatible — Excluding the V_{PROG} Pin during Read or Write
☐ Ultraviolet Light Erasable — Less than 10 Minutes
☐ Static Operation — No Clocks Required
☐ Three-State Data I/O
☐ Standard Power Supplies — +5V and -12V
☐ Mature P-Channel Process

General Description

The S5204A is a high speed, static, 512x8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24-pin hermetically sealed dual in-line package, the bit pattern can be erased by exposing the chip to an ultraviolet light source through the transparent lid, after which a new pattern can be written.

EPROMs

Block Diagram
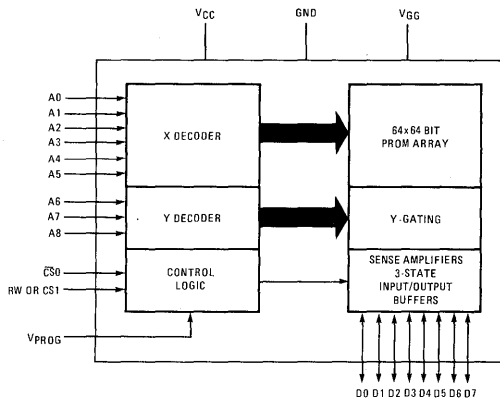
77675

Pin Configuration
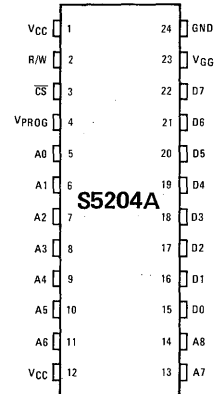
877254

Typical Applications

☐ ROM Program Debugging
☐ Code Translation
☐ Microprogramming
☐ Look-up Tables
☐ Random Logic Replacement
☐ Programmable Waveforms
☐ Character Generation
☐ Electronic Keyboards

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} except the V_{PROG} pin	+0.3 to −20V
Voltage on the V_{PROG} pin relative to V_{SS}	+0.3 to −60V
Operating Temperature	0°C to +70°C
Storage Temperature (programmed)	−55°C to +85°C
Storage Temperature (unprogrammed)	−55°C to 150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS (V_{CC} = +5.0V ± 5%, V_{GG} = −12.0V ± 5% T_A = 0 − 70°C unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
V_{IL}	INPUT VOLTAGE LOW		0.8	V
V_{IH}	INPUT VOLTAGE HIGH	V_{CC} −2.25	V_{CC} +.3	V
V_{OL}	OUTPUT VOLTAGE LOW I_{OL} = 1.6 ma		0.4	V
V_{OH}	OUTPUT VOLTAGE HIGH I_{OH} = 200μA	2.4		V
I_{LI}	INPUT LEAKAGE CURRENT		10	μa
I_{LO}	OUTPUT LEAKAGE CURRENT CS = 5V		20	μa
I_{GG}	V_{GG} SUPPLY CURRENT		45	ma
I_{CC}	V_{CC} SUPPLY CURRENT		50	ma
P_D	POWER DISSIPATION		750	mw

NOTE: Program input V_{PROG} may be tied to V_{CC} during the Read.

AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
T_{ACC}	ACCESS TIME		750	ns
T_{CO}	CHIP SELECT TO OUTPUT DELAY		400	ns
T_{DD}	CHIP DESELECT TO OUTPUT DELAY			ns

FIGURE 1 — TEST CONDITIONS

FIGURE 2 — READ CYCLE TIMING WAVEFORMS

EPROMs

PROGRAM CHARACTERISTICS (R/W G$_{nd}$, Program pulse rise and fall time (10% to 90%) are both at 1μs max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
T$_{AS}$	ADDRESS SET UP TIME	10		μs
T$_{CSS}$	CHIP SELECT SET UP TIME	10		μs
T$_{DS}$	DATA SET UP TIME	10		μs
T$_{AH}$	ADDRESS HOLD TIME	10		μs
T$_{CSH}$	CHIP SELECT HOLD TIME	10		μs
T$_{DH}$	DATA HOLD TIME	10		μs
T$_{PWL}$	PROGRAM PULSE WIDTH LOW	3	5	ms
T$_{PWH}$	PROGRAM PULSE WIDTH HIGH	500		μs
V$_{PROG}$*	PROGRAM AMPLITUDE	−55	−50	V
I$_{PROG}$	PROGRAM CURRENT		35	ma
T$_{WS}$	WRITE SET UP TIME	10		μs
T$_{WH}$	WRITE HOLD TIME	5		μs
T$_{RS}$	READ SET UP TIME	10		μs

*Note that in the WRITE mode the MIN value of V$_{PROG}$ should not be exceeded and that chip select, address, and data lines may remain at TTL level, as in the READ mode

FIGURE 3 —PROGRAMMING CYCLE TIMING WAVEFORMS

FIGURE 4 —READ/PROGRAM/READ CYCLE TIMING WAVEFORM

INTERFACE DESCRIPTION

Pin	Label	Function
(15)	D0	**Data Lines** — with the R/W line selected for Read (V_{IL}), the Data Lines (D0 through D7) are
(16)	D1	set to reflect the contents of the selected memory location. When the R/W line is set for
(17)	D2	Write (V_{IH}), the Data Lines are stored at the addressed location of the 5204A when V_{PROG}
(18)	D3	is present. The Data Bus output drivers are three-state devices that remain in the high im-
(19)	D4	pedance (off) state whenever CS is in the V_{IH} state or when R/W is in the V_{IL} state.
(20)	D5	
(21)	D6	
(22)	D7	
(2)	R/W	**Read/Write** — When this input line is set to V_{IH}, the device is in the Write mode, a low (V_{IL}) signal puts it into the Read mode.
(3)	CS	**Chip Select** — This input line must be set to V_{IL} for a Read or Write operation to be performed. When it is High (V_{IH}) the output data bus is set to a high-impedance three-state condition.
(4)	V_{PROG}	**Program** — In the Write mode, a 50Volt programming pulse at this input causes the data at the Data Lines to be stored in the selected address location. This pin should be tied to V_{CC} for normal Read operations.
(5)	A0	**Address Lines** — These lines select the 8 bit word in memory for Read or Write operation.
(6)	A1	
(7)	A2	
(8)	A3	
(9)	A4	
(10)	A5	
(11)	A6	
(13)	A7	
(14)	A8	

EPROMs

CONTROL FUNCTION TRUTH TABLE

CS	R/W	V_{PROG}	MODE	OUTPUTS
0	1	V_{PROG}	Write	Active Data Inputs
0	0	V_{CC}	Read	Active
1	X	X	Standby	Floating

OPERATION

Initially, and after each erasure, all bits of the 5204A are in the LOW state (output 0 volts). Data is stored by selectively programming a HIGH into the desired bit locations. The R/W input (pin 2) is used to select the desired mode of operation. When the R/W input is HIGH the chip is in the write enable mode of operation. The outputs ($D_0 - D_7$) are disabled (floating) with the corresponding pins becoming the data inputs. The word address is selected in the same manner as in the Read mode. Data to be programmed is presented 8 bits in parallel and after the address and data are set up a programming pulse ($V_P = -50$ volts) is applied. V_{PROG} electrically writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a HIGH during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and V_{PROG} inputs are common and the device to be programmed is selected by means of the chip select input as during read operations.

The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses (N) times the program pulse width (t_{pw}) (N x $t_{pw} \geqslant 60$ msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

The read operation is accomplished by a LOW at the R/W input with the program input connected to V_{SS} potential. True data (data out = date in) is valid after the address is stable. The CS input will disable (float) the outputs when HIGH to allow capability with bus organized systems.

Erasure is accomplished by exposing the array to a 2537Å ultra-violet light source (such as Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54, Turner Designs PROM Eraser, Model 30 or equivalent) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

AMI®

S6834

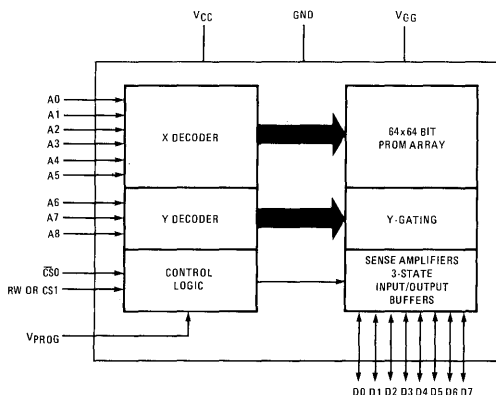# ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

Features

- ☐ On-Board Programmability
- ☐ Fast Access Time — 575ns Typ.
- ☐ Pin Configuration Similar to the S6830 1K x 8 Bit ROM
- ☐ High Speed Programming — Less than 1 Minute for All 4096 Bits
- ☐ Programmed with R/W, CS and V_{PROG} Pins
- ☐ Completely TTL Compatible — Excluding the V_{PROG} Pin
- ☐ Ultraviolet Light Erasable — Less than 10 Minutes
- ☐ Static Operation — No Clocks Required
- ☐ Three-State Data I/O
- ☐ Standard Power Supplies +5V and −12V
- ☐ Mature P-Channel Process

General Description

The S6834 is a high speed, static, 512 x 8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24 pin hermetically sealed dual in-line package the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written.

Block Diagram

Pin Configuration

GND	1	24	A_0
D_0	2	23	A_1
D_1	3	22	A_2
D_2	4	21	A_3
D_3	5	20	A_4
D_4	6	19	A_5
D_5	7	18	A_6
D_6	8	17	A_7
D_7	9	16	A_8
V_{GG}	10	15	$\overline{CS}$
V_{PROG}	11	14	R/W
V_{CC}	12	13	V_{CC}

Typical Applications

- ☐ ROM Program Debugging
- ☐ Code Translation
- ☐ Microprogramming
- ☐ Look-up Tables
- ☐ Random Logic Replacement
- ☐ Programmable Waveforms
- ☐ Character Generation
- ☐ Electronic Keyboards

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} except the V_{PROG} pin	+0.3 to −20V
Voltage on the V_{PROG} pin relative to V_{SS}	+0.3 to −60V
Operating Temperature . . . . :	0°C to +70°C
Storage Temperature (programmed)	−55°C to +85°C
Storage Temperature (unprogrammed)	−55°C to 150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS (V_{CC} = +5.0V ± 5%, V_{GG} = −12.0V ± 5% T_A = 0 − 70°C unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
V_{IL}	INPUT VOLTAGE LOW		0.8	V
V_{IH}	INPUT VOLTAGE HIGH	V_{CC} −2.25	V_{CC} +.3	V
V_{OL}	OUTPUT VOLTAGE LOW I_{OL} = 1.6 ma		0.4	V
V_{OH}	OUTPUT VOLTAGE HIGH I_{OH} = 200μA	2.4		V
I_{LI}	INPUT LEAKAGE CURRENT		10	μa
I_{LO}	OUTPUT LEAKAGE CURRENT CS = 5V		20	μa
I_{GG}	V_{GG} SUPPLY CURRENT		45	ma
I_{CC}	V_{CC} SUPPLY CURRENT		50	ma
P_D	POWER DISSIPATION		750	mw

NOTE: Program input V_{PROG} may be tied to V_{CC} during the Read.

AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX		UNIT
			(6834)	(6834−1)	
T_{ACC}	ACCESS TIME		575	750	ns
T_{CO}	CHIP SELECT TO OUTPUT DELAY		300	400	ns
T_{DD}	CHIP DESELECT TO OUTPUT DELAY		250	325	ns

FIGURE 1 — TEST CONDITIONS   **FIGURE 2 — READ CYCLE TIMING WAVEFORMS**
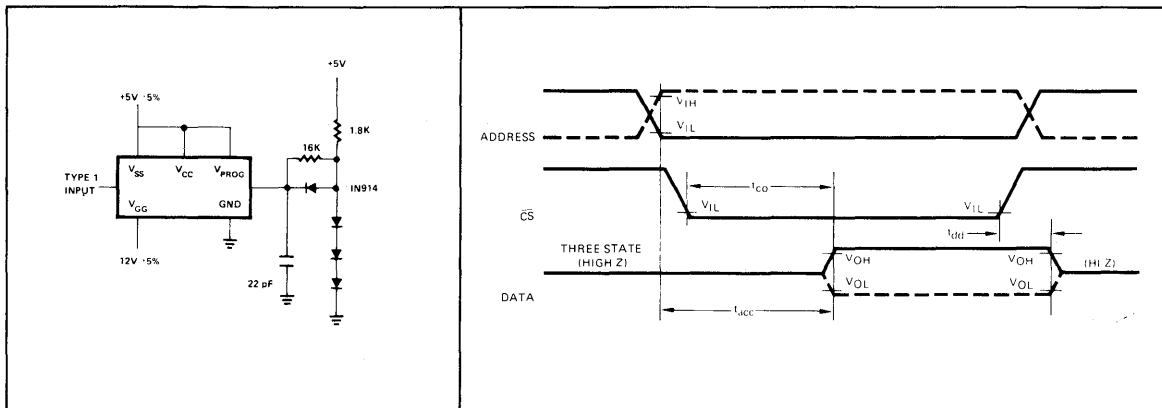
EPROMs

PROGRAM CHARACTERISTICS (R/W G_{nd}, Program pulse rise and fall time (10% to 90%) are both at $1\mu s$ max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
T_{AS}	ADDRESS SET UP TIME	10		μs
T_{CSS}	CHIP SELECT SET UP TIME	10		μs
T_{DS}	DATA SET UP TIME	10		μs
T_{AH}	ADDRESS HOLD TIME	10		μs
T_{CSH}	CHIP SELECT HOLD TIME	10		μs
T_{DH}	DATA HOLD TIME	10		μs
T_{PWL}	PROGRAM PULSE WIDTH LOW	3	5	ms
T_{PWH}	PROGRAM PULSE WIDTH HIGH	500		μs
$V_{PROG}*$	PROGRAM AMPLITUDE	−55	−50	V
I_{PROG}	PROGRAM CURRENT		35	ma
T_{WS}	WRITE SET UP TIME	10		μs
T_{WH}	WRITE HOLD TIME	5		μs
T_{RS}	READ SET UP TIME	10		μs

*Note that in the WRITE mode the MIN value of V_{PROG} should not be exceeded and that chip select, address, and data lines may remain at TTL level, as in the READ mode

FIGURE 3 —PROGRAMMING CYCLE TIMING WAVEFORMS

FIGURE 4 —READ/PROGRAM/READ CYCLE TIMING WAVEFORM

INTERFACE DESCRIPTION

Pin	Label	Function
(2) (3) (4) (5) (6) (7) (8) (9)	D0 D1 D2 D3 D4 D5 D6 D7	**Data Lines** — with the R/W line selected for Read (V_{IL}), the Data Lines (D0 through D7) are set to reflect the contents of the selected memory location. When the R/W line is set for Write (V_{IH}), the Data Lines are stored at the addressed location of the 5204A when V_{PROG} is present. The Data Bus output drivers are three-state devices that remain in the high impedance (off) state whenever CS is in the V_{IH} state or when R/W is in the V_{IL} state.
(14)	R/W	**Read/Write** — When this input line is set to V_{IH}, the device is in the Read mode, a low (V_{IL}) signal puts it into the Write mode.
(15)	CS	**Chip Select** — This input line must be set to V_{IL} for a Read or Write operation to be performed. When it is HIGH (V_{IH}) the output data bus is set to a high-impedance three-state condition and disables the Write operation.
(11)	V_{PROG}	**Program** — In the Write mode, a −50V programming pulse at this input causes the data at the Data Lines to be stored in the selected address location. This pin should be tied to V_{CC} for normal Read operations.
(24) (23) (22) (21) (20) (19) (18) (17) (16)	A0 A1 A2 A3 A4 A5 A6 A7 A8	**Address Lines** — These lines select the 8 bit word in memory for Read or Write operation.

EPROMs

CONTROL FUNCTION TRUTH TABLE

CS	R/W	V_{PROG}	MODE	OUTPUTS
0	0	V_{PROG}	Write	Active Data Inputs
0	1	V_{CC}	Read	Active
1	X	X	Standby	Floating

OPERATION

Initially, and after each erasure, all bits of the 6834 are in the LOW state (output 0 volts) Data is stored by selectively programming a HIGH into the desired bit locations. The R/W input pin 14 is used to select the desired mode of operation. When the R/W input is LOW, the chip is in the write enable mode of operation. The outputs ($0_1 - 0_8$) are disabled (floating) with the corresponding pins becoming the data inputs ($0_1 \rightarrow D_{IN} 1$ etc.). The word address is selected in the same manner as in the read mode. Data to be programmed is presented 8 bits in parallel and after the address and data are set up a programming pulse ($V_p = -50$ volts) is applied. V_{PROG} writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a LOW during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and V_{PROG} inputs are common and the device to be programmed is selected by means of the chip select input as during read operations.

The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses (N) times the program pulse width (t_{pw}) (N x $t_{pw} \geq 60$ msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

The read operation is accomplished by a HIGH at the R/W input with the program input connected to V_{SS} potential. True data (data out = data in) is valid after the address is stable. The CS input will disable (float) with the outputs when HIGH to allow capability with bus organized systems.

Erasure is accomplished by exposing the array to a high intensity ultra-violet light source (such as, Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

AMI®

THE AMI S6800 MICROCOMPUTER SYSTEMS FAMILY

PART NO.	DESCRIPTION	POWER SUPPLIES	INPUT/OUTPUT	PACKAGES
S6800	8-Bit Microprocessor (1.0MHz Clock Rate)	+5V	TTL	40 Pin
S68A00	8-Bit Microprocessor (1.5MHz Clock Rate)	+5V	TTL	40 Pin
S68B00	8-Bit Microprocessor (2.0MHz Clock Rate)	+5V	TTL	40 Pin
S6801	8-Bit Microcomputer	+5V	TTL	TBA
S6802	1024 Bit (128x8) Microprocessor		TTL	40 Pin
S6809	High Performance Monolithic Microprocessor	+5V	TTL	TBA
S6810A	1024 Bit (128x8) Static Read/Write Memory			24 Pin
	(450ns Access Time)	+5V	DTL/TTL	40 Pin
S6180A-1	1024 Bit (128x8) Static Read/Write Memory			
	(350ns Access Time)	+5V	TTL/CMOS	24 Pin
S68A10	1024 Bit (128x8) Static Read/Write Memory			
	(360ns Access Time)	+5V	TTL/CMOS	24 Pin
S68B10	1024 Bit (128x8) Static Read/Write Memory			
	(250ns Access Time)	+5V	TTL	24 Pin
S6820	Peripheral Interface Adapter (PIA)	+5V	TTL	40 Pin
S6821	Peripheral Interface Adapter (PIA)	+5V	TTL	40 Pin
S68A21	Peripheral Interface Adapter (PIA)	+5V	TTL/CMOS	40 Pin
S68B21	Peripheral Interface Adapter (PIA)	+5V	TTL/CMOS	40 Pin
S6831A	16,384 Bit (2048x8) ROM	+5V	TTL	24 Pin
S6831B	16,384 Bit (2048x8) ROM	+5V	TTL	24 Pin
S6834	4096 Bit (512x8) EPROM	+5V, −12V	Three-State	24 Pin
S6840	Programmable Timer	+5V	TTL	28 Pin
S6846	NMOS Combination ROM, I/O, Timer	+5V	TTL	40 Pin
S6850	Asynchronous Communication Interface Adapter	+5V	TTL	24 Pin
S68A50	Asynchronous Communication Interface Adapter	+5V	TTL	24 Pin
S68B50	Asynchronous Communication Interface Adapter	+5V	TTL	24 Pin
S6852	Synchronous Serial Data Adapter (SSDA)	+5V	TTL	24 Pin
S6854	Advanced Data Link Controller	+5V	TTL	24 Pin
S68A54	Advanced Data Link Controller	+5V	TTL	24 Pin
S68047	Video Display Generator	+5V	TTL	40 Pin
S68488	General Purpose Interface Adapter (GPIA)	+5V	TTL	40 Pin

8-BIT
MICROPROCESSOR

BLOCK DIAGRAM

PIN CONFIGURATION
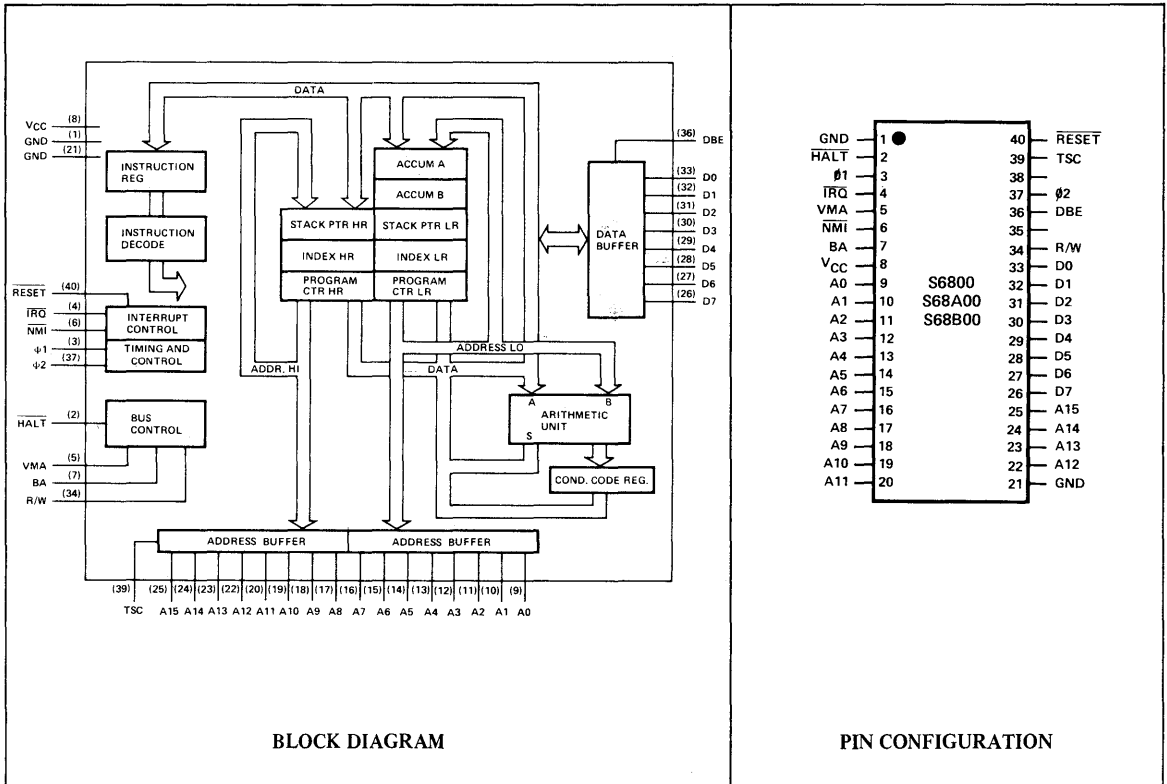
FEATURES

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus — 65536 Bytes of Addressing
- 72 Instructions — Variable Length
- Seven Addressing Modes — Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- 2 Microsecond Instruction Execution
- Maskable Interrupt Vector

- Separate Non-Maskable Interrupt — Internal Registers Saved in Stack
- Six Internal Registers — Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Access (DMA) and Multiple Processor Capability
- Clock Rates — S6800 — 1.0 MHz
  S68A00 — 1.5 MHz
  S68B00 — 2.0 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}		Operating Temperature Range T_A	$0°C$ to $+70°C$
Input Voltage V_{IN}	-0.3 to $+7.0V$	Industrial Temperature Range	$-40°C$ to $+85°C$
		Military Temperature Range	$-55°C$ to $+125°C$
		Storage Temperature Range T_{stg}	$-55°C$ to $+150°C$

ELECTRICAL CHARACTERISTICS

($V_{CC} = 5.0V$, $\pm 5\%$, $V_{SS} = 0$, T_A unless otherwise noted.)

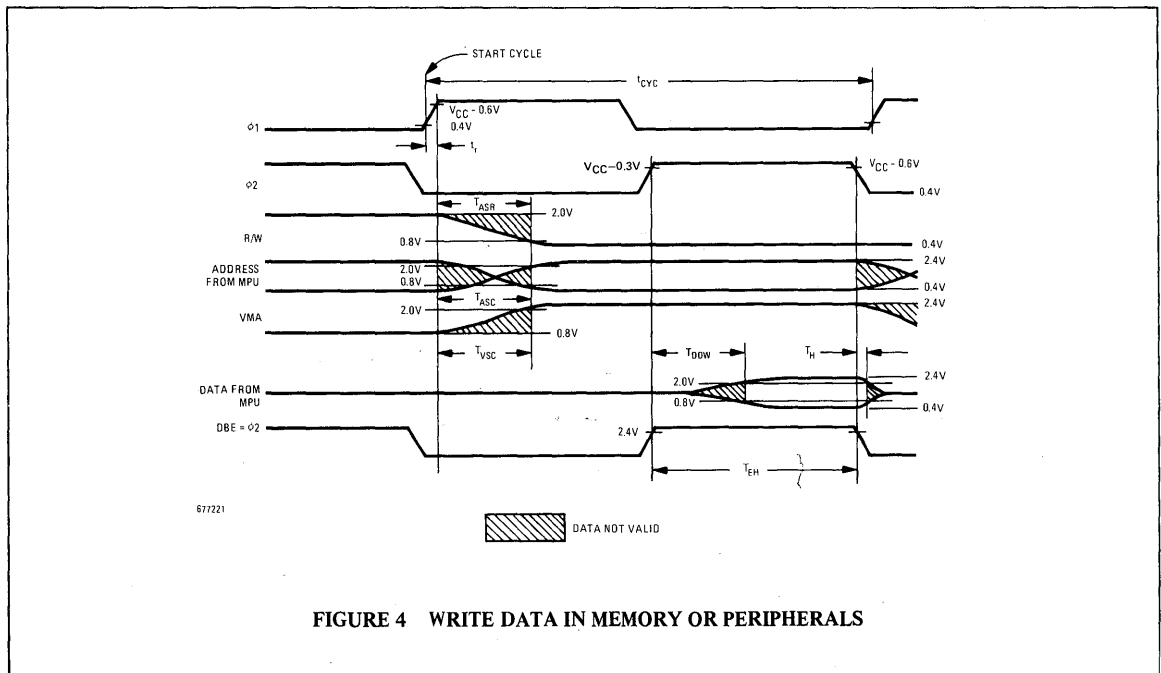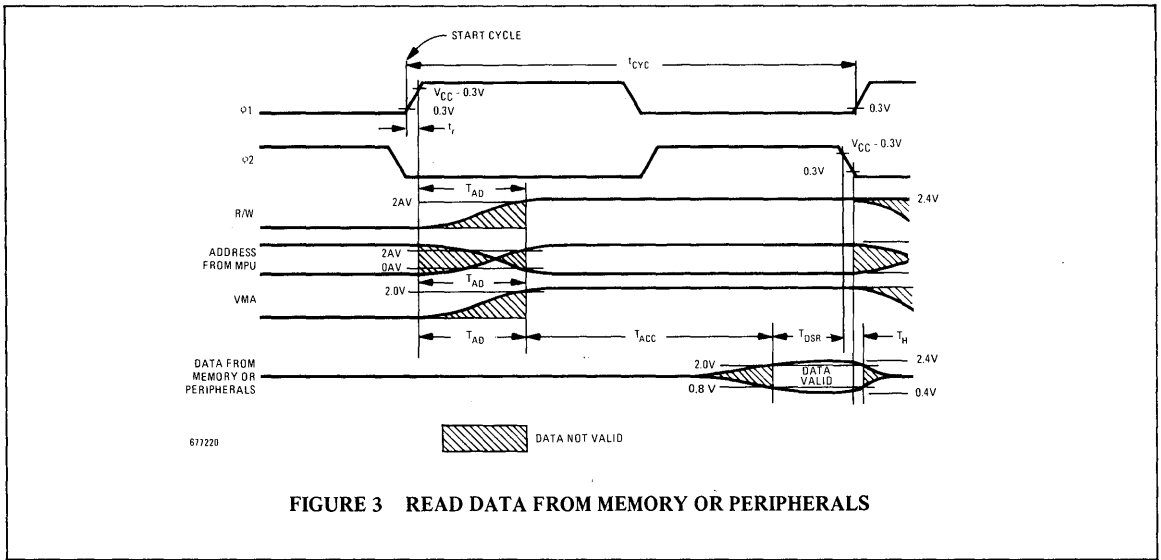| SYMBOL	CHARACTERISTICS		MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage (Normal Operating Levels)	Logic	$V_{SS} + 2.0$	—	V_{CC}	Vdc
V_{IHC}		$\phi 1, \phi 2$	$V_{CC} - 0.6$	—	$V_{CC} + 0.3$	
V_{IL}	Input Low Voltage (Normal Operating Levels)	Logic	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	Vdc
V_{ILC}		$\phi 1, \phi 2$	$V_{SS} - 0.3$	—	$V_{SS} + 0.4$	
I_{IN}	Input Leakage Current					μAdc
	($V_{IN} = 0$ to $5.25V$, $V_{CC} = $ Max)	Logic*	—	1.0	2.5	
	($V_{IN} = 0$ to $5.25V$, $V_{CC} = 0.0V$)	$\phi 1, \phi 2$	—	—	100	
I_{TSI}	Three-State (Off State) Input Current	D0 – D7	—	2.0	10	μAdc
	$V_{IN} = 0.4$ to $2.4V$, $V_{CC} = $ Max	A0 – A15, R/W	—	—	100	
V_{OH}	Output High Voltage					Vdc
	($I_{LOAD} = -205\mu Adc$, $V_{CC} = $ Min)	D0 – D7	$V_{SS} + 2.4$	—	—	
	($I_{LOAD} = -145\mu Adc$, $V_{CC} = $ Min)	A0 – A15, R/W, VMA	$V_{SS} + 2.4$	—	—	
	($I_{LOAD} = -100\mu Adc$, $V_{CC} = $ Min)	BA	$V_{SS} + 2.4$	—	—	
V_{OL}	Output Low Voltage		—	—	$V_{SS} + 0.4$	Vdc
	($I_{LOAD} = 1.6mAdc$, $V_{CC} = $ Min)					
P_D	Power Dissipation		—	0.5	1.0	W
C_{IN}	Capacitance #					pF
	($V_{IN} = 0$, $T_A = 25°C$, $f = 1.0$ MHz)	$\phi 1$	—	—	35	
		$\phi 2$	—	—	70	
		D0 – D7	—	10	12.5	
		Logic Inputs	—	6.5	10	
C_{OUT}		A0 – A15, R/W, VMA	—	—	12	pF
f	Frequency of Operation	S68A00	0.1	—	1.5	MHz
		S68B00	0.1	—	2.0	
t_{CYC}	Clock Timing (Figure 1)	S68A00	0.666	—	10	
	Cycle Time	S68B00	0.50	—	10	μs
$PW_{\phi H}$	Clock Pulse Width	$\phi 1, \phi 2$ – S68A00	230	—	9500	ns
	Measured at $V_{CC} - 0.6V$	$\phi 1, \phi 2$ – S68B00	180	—	9500	
t_{UT}	Total $\phi 1$ and $\phi 2$ Up Time	S68A00	600	—	—	ns
		S68B00	440	—	—	
$t_{\phi r}, t_{\phi f}$	Rise and Fall Times		5.0	—	100	ns
	Measured between $V_{SS} + 0.4$ and $V_{CC} - 0.6$					
t_d	Delay Time or Clock separation		0	—	9100	ns
	Measured at $V_{OV} = V_{SS} + 0.6$					

Except $\overline{IRQ}$ and $\overline{NMI}$, which require $K\Omega$ pullup load resistor for wire-OR capability at optimum operation.

#Capacitances are periodically sampled rather than 100% tested.

READ/WRITE TIMING

Symbol	Parameter	S6800			S68A00			S68B00			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{AD}	Address Delay										ns
	$\quad\quad\quad$ C = 90pF		100	300			180			150	
	$\quad\quad\quad$ C = 30pF						165			135	
t_{ACC}	Peripheral Read Access Time $t_{AC} = t_{UT} - (t_{AD} + t_{DSR})$			575			360			250	ns
t_{DSR}	Data Setup Time (Read)	100			60			40			ns
t_H	Input Data Hold Time	10	30		10			10			ns
t_H	Output Data Hold Time	10	25		10	25		10	25		ns
t_{AH}	Address Hold Time (Address, R/W, VMA)				10	75		10	75		ns
t_{EH}	Enable High Time for DBE Input	470			280			220			ns
t_{DDW}	Data Delay Time (Write)					165	200			160	ns
t_{PCS}	Processor Controls Processor Control Setup Time			200	200			200			ns
t_{PC_r}; t_{PC_f}	Processor Control Rise and Fall Time						100			100	ns
t_{BA}	Bus Available Delay						270			270	ns
t_{TSE}	Three-State Enable						40			40	ns
t_{TSD}	Three-State Delay						270			270	ns
$t_{\overline{DBE}}$	Data Bus Enable Down Time During $\phi1$ Up Time				150			70			ns
t_{DBE_r}, t_{DBE_f}	Data Bus Enable Rise and Fall Times						25			25	ns

FIGURE 1   CLOCK TIMING WAVEFORM

Measurement point for $\phi1$ and $\phi2$ are shown below. Other measurements are the same as for MC6800.

FIGURE 2   READ/WRITE TIMING WAVEFORM

FIGURE 3   READ DATA FROM MEMORY OR PERIPHERALS

FIGURE 4   WRITE DATA IN MEMORY OR PERIPHERALS
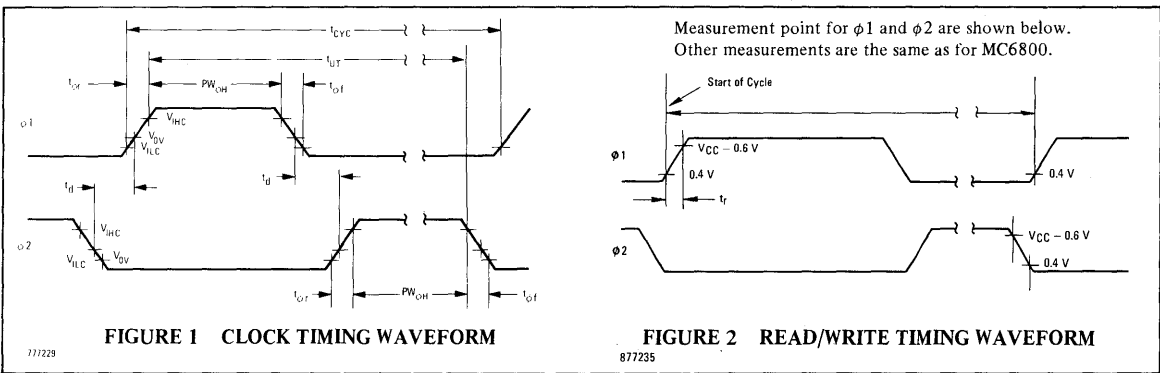
INTERFACE DESCRIPTION

Label	Pin	Function
ϕ1 ϕ2	(3) (37)	**Clocks Phase One and Phase Two** — Two pins are used for a two-phase non-overlapping clock that runs at the V_{CC} voltage level.
$\overline{RESET}$	(40)	**Reset** — This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{IRQ}$. $\overline{Reset}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts (Figure 4). If $\overline{Reset}$ goes high prior to the leading edge of ϕ2, on the next ϕ1 the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

FIGURE 5
INITIALIZATION OF MPU AFTER RESTART
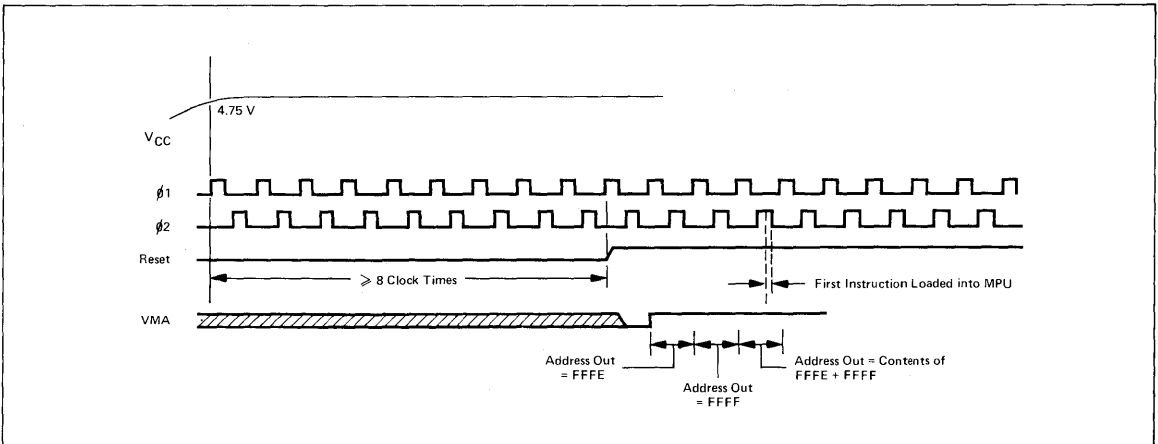
VMA	(5)	**Valid Memory Address** — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 30 pF may be directly driven by this active high signal.

Label	Pin	Function
A0 • • • A15	(9) (25)	**Address Bus** — Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130 pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.
TSC	(39)	**Three-State Control** — This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 500 ns after TSC = 2.4 V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The $\phi1$ clock must be held in the high state and the $\phi2$ in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 5.0 μs or destruction of data will occur in the MPU.
D0 • • D7	(33) (26)	**Data Bus** — Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load at 130 pF.
DBE	(36)	**Data Bus Enable** — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it can be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.
R/W	(34)	**Read/Write** — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the off (high-impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 130 pF.
$\overline{\text{HALT}}$	(2).	$\overline{\text{Halt}}$ — When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode. Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250 ns of phase one. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one Phase One Clock cycle.
BA	(7)	**Bus Available** — The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0)or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

Label	Pin	Function
$\overline{\text{IRQ}}$	(4)	**Interrupt Request** -- This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be recognized.

The $\overline{\text{IRQ}}$ has a high impedance pullup device internal to the chip; however a 3 kΩ external resistor to V$_{CC}$ should be used for wire-OR and optimum control of interrupts.

Label	Pin	Function
$\overline{\text{NMI}}$	(6)	**Non-Maskable Interrupt** — A low-going edge on this input requests that a non-mask interrupt sequence be generated within the processor. As with the $\overline{\text{Interrupt Request}}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away in the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{\text{NMI}}$ has a high impedance pullup resistor internal to the chip; however a 3 kΩ external resistor to V$_{CC}$ should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are acknowledged during $\phi2$ and will start the interrupt routine on the $\phi1$ following the completion of an instruction.
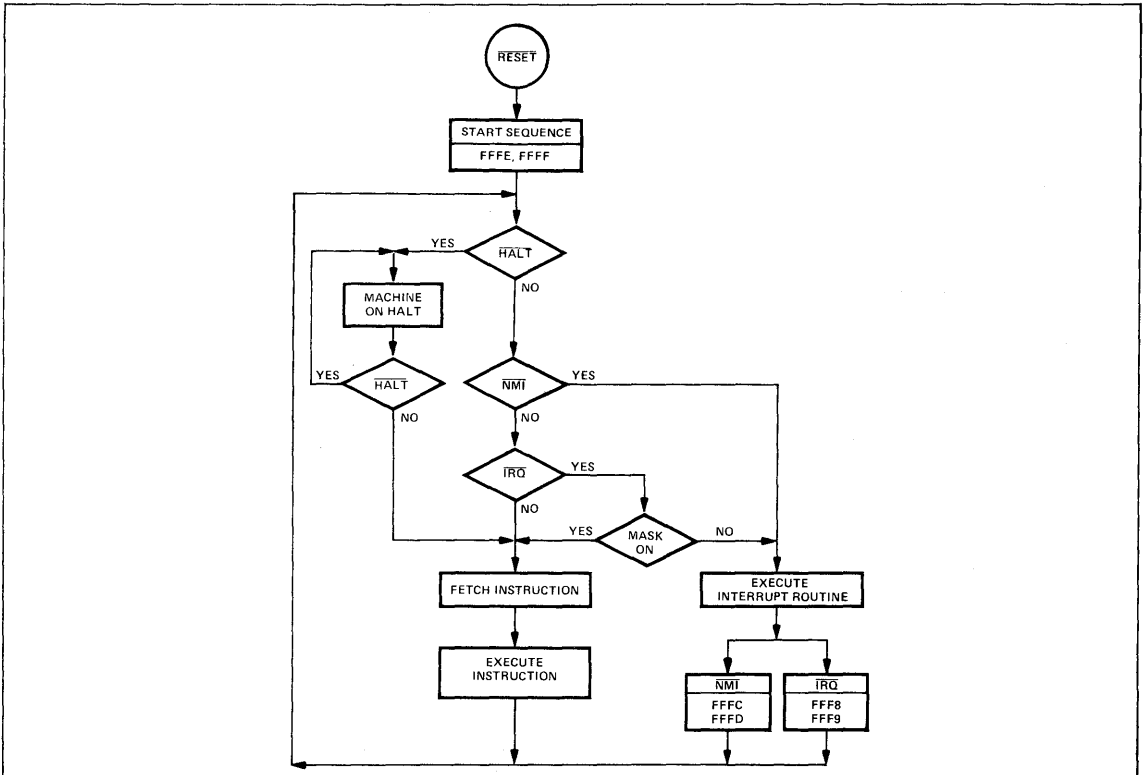
S6800

INTERRUPTS — As outlined in the interface description the S6800 requires a 16-bit vector address to indicate the location of routines for Restart, Non-maskable Interrupt, and Maskable Interrupt. Additionally an address is required for the Software Interrupt Instruction (SWI). The processor assumes the uppermost eight memory locations, FFF8 — FFFF, are assigned as interrupt vector addresses as defined in Figure 6.

After completing the current instruction execution the processor checks for an allowable interrupt request via the $\overline{\text{IRQ}}$ or $\overline{\text{NMI}}$ inputs as shown by the simplified flow chart in Figure 7. Recognition of either external interrupt request or a Wait for Interrupt (WAI) or Software Interrupt (SWI) instruction causes the contents of the Index Register, Program Counter, Accumulators and Condition Code Register to be tranferred to the stack as shown in Figure 8.

FIGURE 6   **MEMORY MAP FOR INTERRUPT VECTORS**

Vector		Description
MS	LS	
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request

FIGURE 7   MPU FLOW CHART

```
                              ( RESET )
                                 │
                         ┌───────────────┐
                         │ START SEQUENCE │
                         │   FFFE, FFFF   │
                         └───────────────┘
                                 │
                  YES           ◇ HALT
          ┌──────────────────────│
          │                      │ NO
    ┌───────────┐                │
    │  MACHINE  │                │
    │  ON HALT  │                │
    └───────────┘                │
          │                      │
   YES    │              YES     │
  ┌───────◇ HALT      ┌──────────◇ NMI
  │       │ NO        │          │ NO
  │       │           │          │
  │       │           │    YES   ◇ IRQ
  │       │           │   ┌──────│
  │       │           │   │      │ NO
  │       │   YES     │   │      │
  │       │  ┌────────│───│──────◇ MASK    NO
  │       │  │        │   │      │ ON ──────┐
  │       │  │        │   │                 │
  │  ┌─────────────┐  │   │       ┌──────────────────┐
  │  │   FETCH     │  │   │       │    EXECUTE       │
  │  │ INSTRUCTION │  │   │       │ INTERRUPT ROUTINE │
  │  └─────────────┘  │   │       └──────────────────┘
  │       │           │   │            │
  │  ┌─────────────┐  │   │      ┌──────┴──────┐
  │  │  EXECUTE    │  │   │   ┌──────┐    ┌──────┐
  │  │ INSTRUCTION │  │   │   │  NMI │    │  IRQ │
  │  └─────────────┘  │   │   │ FFFC │    │ FFF8 │
  │       │           │   │   │ FFFD │    │ FFF9 │
  │       │           │   │   └──────┘    └──────┘
  └───────┴───────────┘
```

FIGURE 8   SAVING THE STATUS OF THE MICROPROCESSOR IN THE STACK

SP = Stack Pointer
CC = Condition Codes (Also called the Processor Status Byte)
ACCB = Accumulator B
ACCA = Accumulator A
IXH = Index Register, Higher Order 8 Bits
IXL = Index Register, Lower Order 8 Bits
PCH = Program Counter, Higher Order 8 Bits
PCL = Program Counter, Lower Order 8 Bits

BEFORE		AFTER	
		m − 9	
		m − 8	
		m − 7	← SP
		m − 6	CC
		m − 5	ACCB
		m − 4	ACCA
		m − 3	IXH
m − 2		m − 2	IXL
m − 1		m − 1	PCH
m	← SP	m	PCL
m + 1		m + 1	
m + 2		m + 2	

3.11

MPU REGISTERS

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer.

Program Counter — The program counter is a two byte (16-bits) register that points to the current program address.

Stack Pointer — The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register — The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

Accumulators — The MPU contains two 8-bit accumulators that are used to hold operands and results from the arithmetic logic unit (ALU).

Condition Code Register — The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

FIGURE 9   PROGRAMMING MODEL OF THE MICROPROCESSOR

3.12
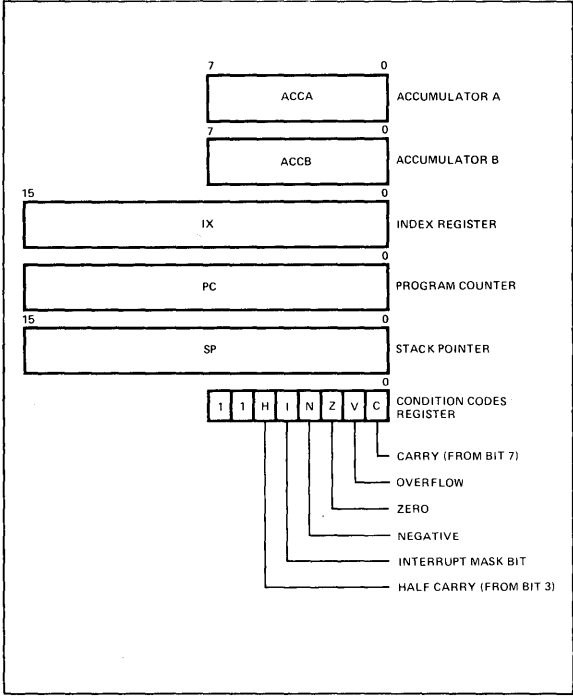
MPU ADDRESSING MODES

The S6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Figure 9 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

ACCUMULATOR ADDRESSING (ACCX)

OP CODE
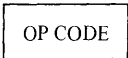
A single byte instruction addressing operands only in accumulator A or accumulator B.

IMPLIED ADDRESSING

OP CODE
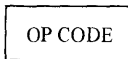
Single byte instruction where the operand address is implied by the instruction definition (i.e., Stack Pointer, Index Register or Condition Register).

IMMEDIATE ADDRESSING

HIGHER	OPERAND	OPERAND LOWER
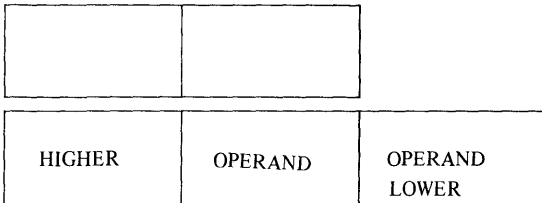
Two or three byte instructions with an eight or sixteen bit operand respectively. For accumulator operations the eight bit operand is contained in the second byte of a two byte instruction. For Index Register operations (e.g. LDX) sixteen bit operand is contained in the second and third byte of a three byte instruction.

DIRECT ADDRESSING

OP CODE	ADDRESS 0-255
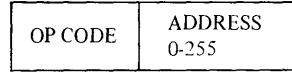
Two byte instructions with the address of the operand contained in the second byte of the instruction. This format allows direct addressing of operands within the first 256 memory locations.

EXTENDED ADDRESSING

OP CODE	ADDRESS HIGHER	ADDRESS LOWER
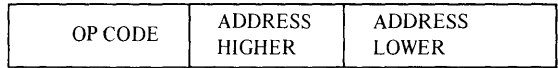
Three byte instructions with the higher eight bits of the operand address contained in the second byte and the lower eight bits of address contained in the third byte of the instruction. This format allows direct addressing of all 65,536 memory locations.

INDEXED ADDRESSING

OP CODE	INDEX ADDRESS
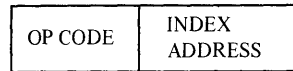
Two byte instructions where the 8 bit unsigned address contained in the second byte of the instruction is added to the sixteen bit Index Register resulting in a sixteen bit effective address. The effective address is stored in a temporary register and the contents of the Index Register are unchanged.

RELATIVE ADDRESSING

OP CODE	RELATIVE ADDRESS
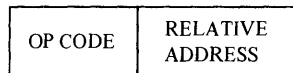
Two byte instructions where the relative address contained in the second byte of the instruction is added to the sixteen bit program counter plus two. The relative address is interpreted as a two's complement number allowing relative addressing within a range of −126 to +129 bytes of the present instruction.

S6800

FIGURE 10   S6800 INSTRUCTION SET

Instruction	Mnemonic	Implied OP MC PB	Immediate OP MC PB	Direct OP MC PB	Extended OP MC PB	Indexed OP MC PB	Relative OP MC PB	Boolean/Arith Operation	H	I	N	Z	V	C
Load accumulator	LDAA		86 2 2	96 3 2	B6 4 3	A6 5 2		M → A	•	•	↕	↕	R	•
	LDAB		C6 2 2	D6 3 2	F6 4 3	E6 5 2		M → B	•	•	↕	↕	R	•
Load stack pointer	LDS		8E 3 3	9E 4 2	BE 5 3	AE 6 2		M → SP$_H$, (M + 1) → SP$_L$	•	•	9	↕	R	•
Load index register	LDX		CE 3 3	DE 4 2	FE 5 3	EE 6 2		M → X$_H$, (M + 1) → X$_L$	•	•	9	↕	R	•
Store accumulator	STAA			97 4 2	B7 5 3	A7 6 2		A → M	•	•	↕	↕	R	•
	STAB			D7 4 2	F7 5 3	E7 6 2		B → M	•	•	↕	↕	R	•
Store stack pointer	STS			9F 5 2	BF 6 3	AF 7 2		SP$_H$ → M, SP$_L$ → (M + 1)	•	•	9	↕	R	•
Store index register	STX			DF 5 2	FF 6 3	EF 7 2		X$_H$ → M, X$_L$ → (M + 1)	•	•	9	↕	R	•
Transfer accumulators	TAB	16 2 1						A → B	•	•	↕	↕	R	•
	TBA	17 2 1						B → A	•	•	↕	↕	R	•
Transfer Acc. to cond. reg.	TAP	06 2 1						A → CCR	Note 12					
Transfer cond. reg. to Acc.	TPA	07 2 1						CCR → A	•	•	•	•	•	•
Transfer stck ptr to index	TSX	30 4 1						SP + 1 → X	•	•	•	•	•	•
Transfer index to stck ptr	TXS	35 4 1						X - 1 → SP	•	•	•	•	•	•
Pull data	PULA	32 4 1						SP + 1 → SP, M$_{SP}$ → A	•	•	•	•	•	•
	PULB	33 4 1						SP + 1 → SP, M$_{SP}$ → B	•	•	•	•	•	•
Push data	PSHA	36 4 1						A → M$_{SP}$, SP - 1 → SP	•	•	•	•	•	•
	PSHB	37 4 1						B → M$_{SP}$, SP - 1 → SP	•	•	•	•	•	•
Add accumulators	ABA	1B 2 1						A + B → A	↕	•	↕	↕	↕	↕
Add	ADDA		8B 2 2	9B 3 2	BB 4 3	AB 5 2		A + M → A	↕	•	↕	↕	↕	↕
	ADDB		CB 2 2	DB 3 2	FB 4 3	EB 5 2		B + M → B	↕	•	↕	↕	↕	↕
Add with carry	ADCA		89 2 2	99 3 2	B9 4 3	A9 5 2		A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB		C9 2 2	D9 3 2	F9 4 3	E9 5 2		B + M + C → B	↕	•	↕	↕	↕	↕
Subtract accumulators	SBA	10 2 1						A − B → A	•	•	↕	↕	↕	↕
Subtract	SUBA		80 2 2	90 3 2	B0 4 3	A0 5 2		A − M → A	•	•	↕	↕	↕	↕
	SUBB		C0 2 2	D0 3 2	F0 4 3	E0 5 2		B − M → B	•	•	↕	↕	↕	↕
Subtract with carry	SBCA		82 2 2	92 3 2	B2 4 3	A2 5 2		A − M − C → A	•	•	↕	↕	↕	↕
	SBCB		C2 2 2	D2 3 2	F2 4 3	E2 5 2		B − M − C → B	•	•	↕	↕	↕	↕
Increment	INCA	4C 2 1						A + 1 → A	•	•	↕	↕	5	•
	INCB	5C 2 1						B + 1 → B	•	•	↕	↕	5	•
	INC				7C 6 3	6C 7 2		M + 1 → M	•	•	↕	↕	5	•
Increment stack pointer	INS	31 4 1						SP + 1 → SP	•	•	•	•	•	•
Increment index reg.	INX	08 4 1						X + 1 → X	•	•	•	↕	•	•
Decrement	DECA	4A 2 1						A − 1 → A	•	•	↕	↕	4	•
	DECB	5A 2 1						B − 1 → B	•	•	↕	↕	4	•
	DEC				7A 6 3	6A 7 2		M − 1 → M	•	•	↕	↕	4	•
Decrement stack pointer	DES	34 4 1						SP − 1 → SP	•	•	•	•	•	•
Decrement index register	DEX	09 4 1						X − 1 → X	•	•	•	↕	•	•
Complement (1's)	COMA	43 2 1						Ā → A	•	•	↕	↕	R	S
	COMB	53 2 1						B̄ → B	•	•	↕	↕	R	S
	COM				73 6 3	63 7 2		M̄ → M	•	•	↕	↕	R	S
Complement (2's)	NEGA	40 2 1						00 − A → A	•	•	↕	↕	1	2
	NEGB	50 2 1						00 − B → B	•	•	↕	↕	1	2
	NEG				70 6 3	60 7 2		00 − M → M	•	•	↕	↕	1	2
Decimal adjust accumulator	DAA	19 2 1							•	•	↕	↕	↕	3

OP = Operation Code   MC = Number of MPU Cycles   PB = Number of Program Bytes

FIGURE 10   S6800 INSTRUCTION SET (CONT'D.)

Instruction	Mnemonic	Implied OP MC PB	Immediate OP MC PB	Direct OP MC PB	Extended OP MC PB	Indexed OP MC PB	Relative OP MC PB	Boolean/Arith Operation	H I N Z V C
Logical and	ANDA		84 2 2	94 3 2	B4 4 3	A4 5 2		A • M → A	• • ‡ ‡ R •
	ANDB		C4 2 2	D4 3 2	F4 4 3	E4 5 2		B • M → B	• • ‡ ‡ R •
Inclusive or	ORAA		8A 2 2	9A 3 2	BA 4 3	AA 5 2		A + M → A	• • ‡ ‡ R •
	ORAB		CA 2 2	DA 3 2	FA 4 3	EA 5 2		B + M → B	• • ‡ ‡ R •
Exclusive or	EORA		88 2 2	98 3 2	B8 4 3	A8 5 2		A ⊕ M → A	• • ‡ ‡ R •
	EORB		C8 2 2	D8 3 2	F8 4 3	E8 5 2		B ⊕ M → B	• • ‡ ‡ R •
Shift left arithmetic	ASLA	48 2 1							• • ‡ ‡ 6 ‡
	ASLB	58 2 1							• • ‡ ‡ 6 ‡
	ASL				78 6 3	68 7 2			• • ‡ ‡ 6 ‡
Shift right arithmetic	ASRA	47 2 1							• • ‡ ‡ 6 ‡
	ASRB	57 2 1							• • ‡ ‡ 6 ‡
	ASR				77 6 3	67 7 2			• • ‡ ‡ 6 ‡
Shift right logical	LSRA	44 2 1							• • R ‡ 6 ‡
	LSRB	54 2 1							• • R ‡ 6 ‡
	LSR				74 6 3	64 7 2			• • R ‡ 6 ‡
Rotate left	ROLA	49 2 1							• • ‡ ‡ 6 ‡
	ROLB	59 2 1							• • ‡ ‡ 6 ‡
	ROL				79 6 3	69 7 2			• • ‡ ‡ 6 ‡
Rotate right	RORA	46 2 1							• • ‡ ‡ 6 ‡
	RORB	56 2 1							• • ‡ ‡ 6 ‡
	ROR				76 6 3	66 7 2			• • ‡ ‡ 6 ‡
Compare accumulators	CBA	11 2 1						A − B	• • ‡ ‡ ‡ ‡
Compare	CMPA		81 2 2	91 3 2	B1 4 3	A1 5 2		A − M	• • ‡ ‡ ‡ ‡
	CMPB		C1 2 2	D1 3 2	F1 4 3	E1 5 2		B − M	• • ‡ ‡ ‡ ‡
Compare index register	CPX		8C 3 3	9C 4 2	BC 5 3	AC 6 2		$X_H − M, X_L − (M+1)$	• • 7 ‡ 8 •
Test (zero or minus)	TSTA	4D 2 1						A − 00	• • ‡ ‡ R R
	TSTB	5D 2 1						B − 00	• • ‡ ‡ R R
	TST				7D 6 3	6D 7 2		M − 00	• • ‡ ‡ R R
Bit test	BITA		85 2 2	95 3 2	B5 4 3	A5 5 2		A • M	• • ‡ ‡ R •
	BITB		C5 2 2	D5 3 2	F5 4 3	E5 5 2		B • M TEST	• • ‡ ‡ R •
Branch	BRA						20 4 2		• • • • • •
Branch if carry clear	BCC						24 4 2	C = 0	• • • • • •
Branch if carry set	BCS						25 4 2	C = 1	• • • • • •
Branch if overflow clear	BVC						28 4 2	V = 0	• • • • • •
Branch if overflow set	BVS						29 4 2	V = 1	• • • • • •
Branch if equal to zero	BEQ						27 4 2	Z = 1	• • • • • •
Branch if greater or equal to zero	BGE						2C 4 2	N ⊕ V = 0	• • • • • •
Branch if greater than zero	BGT						2E 4 2	Z + (N ⊕ V) = 0	• • • • • •
Branch if less than zero	BLT						2D 4 2	N ⊕ V = 1	• • • • • •
Branch if less than or equal to zero	BLE						2F 4 2	Z + (N ⊕ V) = 1	• • • • • •
Branch if not equal to zero	BNE						26 4 2	Z = 0	• • • • • •
Branch if minus	BMI						2B 4 2	N = 1	• • • • • •
Branch if plus	BPL						2A 4 2	N = 0	• • • • • •
Branch if higher	BHI						22 4 2	C + Z = 0	• • • • • •
Branch if lower or same	BLS						23 4 2	C + Z = 1	• • • • • •

OP = Operation Code   MC = Number of MPU Cycles   PB = Number of Program Bytes

FIGURE 10   S6800 INSTRUCTION SET (CONT'D.)

Instruction	Mnemonic	Implied OP MC PB	Direct OP MC PB	Immediate OP MC PB	Extended OP MC PB	Indexed OP MC PB	Relative OP MC PB	Boolean/Arith Operation	H I N Z V C
Branch to subroutine	BSR						8D 8 2	⎫ See Special Operations	• • • • • •
Jump to subroutine	JSR				BD 9 3	AD 8 2			• • • • • •
Jump	JMP				7E 3 3	6E 4 2			• • • • • •
Return from subroutine	RTS	39 5 1							• • • • • •
Return from interrupt	RTI	3B 10 1						⎭	Note 10
Software interrupt	SWI	3F 12 1							• S • • • •
Wait for interrupt	WAI	3E 9 1							• 11 • • • •
No operation	NOP	02 2 1						PC + 1 → PC	• • • • • •
Clear	CLRA	4F 2 1						00 → A	• • R S R R
	CLRB	5F 2 1						00 → B	• • R S R R
	CLR				7F 6 3	6F 7 2		00 → M	• • R S R R
Clear carry	CLC	0C 2 1						0 → C	• • • • • R
Clear interrupt mask	CLI	0E 2 1						0 → I	• R • • • •
Clear overflow	CLV	0A 2 1						0 → V	• • • • R •
Set carry	SEC	0D 2 1						1 → C	• • • • • S
Set interrupt mask	SEI	0F 2 1						1 → I	• S • • • •
Set overflow	SEV	0B 2 1						1 → V	• • • • S •

CONDITION CODE SYMBOLS:

H   Half-carry from bit 3;
I   Interrupt mask
N   Negative (sign bit)
Z   Zero (byte)
V   Overflow, 2's complement
C   Carry from bit 7
R   Reset Always
S   Set Always
‡   Test and set if true, cleared otherwise
•   Not Affected

LEGEND:

OP   Operation Code (Hexadecimal):
MC   Number of MPU Cycles;
PB   Number of Program Bytes;
+   Arithmetic Plus;
–   Arithmetic Minus;
•   Boolean AND;
M_{SP} Contents of memory location pointed to by Stack Pointer;
+   Boolean Inclusive OR;
⊕   Boolean Exclusive OR;
$\overline{M}$ Complement of M;
→   Transfer Into;
0   Bit = Zero;
00   Byte = Zero;

Note – Accumulator addressing mode instructions are included in the IMPLIED addressing.

CONDITION CODE REGISTER NOTES:

(Bit set if test is true and cleared otherwise)

1	(Bit V)	Test: Result = 10000000?
2	(Bit C)	Test: Result = 00000000?
3	(Bit C)	Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4	(Bit V)	Test: Operand = 10000000 prior to execution?
5	(Bit V)	Test: Operand = 01111111 prior to execution?
6	(Bit V)	Test: Set equal to result of N ⊕ C after shift has occurred.
7	(Bit N)	Test: Sign bit of most significant (MS) byte = 1?
8	(Bit V)	Test: 2's complement overflow from subtraction of MS bytes?
9	(Bit N)	Test: Result less than zero? (Bit 15 = 1)
10	(All)	Load Condition Code Register from Stack. (See Special Operations)
11	(Bit I)	Set when interrupt occurs, if previously set, a Non-Maskable Interrupt is required to exit the wait state.
12	(ALL)	Set according to the contents of Accumulator A

SPECIAL OPERATIONS

JMP, JUMP;

PC	MAIN PROGRAM
n	6E = JMP
n + 1	K = OFFSET

INDXD

X + K | NEXT INSTRUCTION

PC	MAIN PROGRAM
n	7E = JMP
n + 1	K_H = NEXT ADDRESS
n + 2	K_L = NEXT ADDRESS

EXTENDED

K | NEXT INSTRUCTION

JSR, JUMP TO SUBROUTINE:

INDXD

PC	MAIN PROGRAM
n	AD = JSR
n + 1	K = OFFSET*
n + 2	NEXT MAIN INSTR.

*K = 8-BIT UNSIGNED VALUE

SP	STACK
SP − 2	
SP − 1	(n + 2) H
SP	(n + 2) L

(n + 2) $_H$ AND (n + 2) $_L$ FORM n + 2

PC	SUBROUTINE
INX + K	1st SUBR. INSTR.

EXTND

PC	MAIN PROGRAM
n	BD = JSR
n + 1	SH = SUBR. ADDR.
n + 2	SL = SUBR. ADDR.
n + 3	NEXT MAIN INSTR.

SP	STACK
SP − 2	
SP − 1	(n + 3) H
SP	(n + 3) L

➤ = STACK POINTER AFTER EXECUTION.

PC	SUBROUTINE
S	1st SUBR. INSTR.

(S FORMED FROM S_H AND S_L)

BSR, BRANCH TO SUBROUTINE:

PC	MAIN PROGRAM
n	8D = BSR
n + 1	± K = OFFSET*
n + 2	NEXT MAIN INSTR.

*K = 7-BIT SIGNED VALUE;

SP	STACK
SP − 2	
SP − 1	(n + 2) H
SP	(n + 2) L

n + 2 FORMED FROM (n + 2)$_H$ AND (n + 2)$_L$

PC	SUBROUTINE
n + 2 ± K	1st SUBR. INSTR.

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SPECIAL OPERATIONS

RTS, RETURN FROM SUBROUTINE:

PC	SUBROUTINE
S	39 = RTS

SP	STACK
SP	
SP + 1	n_H
SP + 2	n_L

PC	MAIN PROGRAM
n	NEXT MAIN INSTR.

SWI, SOFTWARE INTERRUPT

PC	MAIN PROGRAM
n	3F = SWI

SP	STACK
SP − 7	
SP − 6	CC
SP − 5	ACCB
SP − 4	ACCA
SP − 3	X_H
SP − 2	X_L
SP − 1	$(n + 1)_H$
SP	$(n + 1)_L$

PC	INTERRUPT PROGRAM
m	INT. ROUTINE

$m_H = (H - 0005)$
$m_L = (H - 0004)$
H = ADDRESS WITH
 ALL ADDRESS LINES
 IN HIGH STATE

WAI, WAIT FOR INTERRUPT

PC	MAIN PROGRAM
n	3E = WAI

SP	STACK
SP − 7	
SP − 6	CC
SP − 5	ACCB
SP − 4	ACCA
SP − 3	X_H
SP − 2	X_L
SP − 1	$(n + 1)_H$
SP	$(n + 1)_L$

PC	INTERRUPT PROGRAM
m	INT. ROUTINE

$m_H = (H - 0007)$
$m_L = (H - 0006)$
H = ADDRESS WITH
 ALL ADDRESS LINES
 IN HIGH STATE

PROGRAM PROCEEDS AT m ONLY AFTER
EXTERNAL INTERRUPT REQUEST

RTI, RETURN FROM INTERRUPT:

PC	INTERRUPT PROGRAM
S	3B = RTI

SP	STACK
SP	
SP + 1	CC
SP + 2	ACCA
SP + 3	ACCB
SP + 4	X_H
SP + 5	X_L
SP + 6	n_H
SP + 7	n_L

PC	MAIN PROGRAM
n	NEXT MAIN INSTR.

SYSTEMS OPERATION

To demonstrate the great versatility of the functional building block concept, a typical system configuration is shown. This configuration will demonstrate how easily a basic system may be upgraded and expanded for a number of different applications.

The Microprocessing Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system (Figure 10). Such a system can easily be adapted for a number of small scale applications by simply changing the content of the ROM.

TWO-PHASE CLOCK CIRCUITRY AND TIMING—The MPU requires a two-phase non-overlapping clock which has a frequency range as high as 1 MHz for the S6800, 1.5 MHz for the S68A00, and 2.0 MHz for the S68B00. In addition to the two phases, this circuit should also generate an enable signal E, and its complement $\overline{E}$, to enable ROMs, RAMs, PIAs and ACIAs. This Enable signal and its complement is obtained by ANDing $\phi2$ and VMA (Valid Memory Address).

CHIP SELECTION AND ADDRESSING—The minimum system configuration permits direct selection of the ROM, RAM, ACIA and PIA without the use of special TTL select logic. This is accomplished by simply wiring the address lines A13 and A14 to the Enable or chip select lines on the memories and PIA. This permits the devices to be addressed as follows:

Device	A14	A13	Hex Addresses
RAM	0	0	0000–007F
PIA	0	1	2004–2007 (Registers)
ROM	1	1	6000–63FF

Other addressing schemes can be utilized which use any combination of two of the lines A10 through A14 for chip selection.

PERIPHERAL CONTROL—All control and timing for the peripherals that are connected to the PIA is accomplished by software routines under the control of the MPU.

RESTART AND NON-MASKABLE INTERRUPT—Since this basic system does not have a nonvolatile RAM, special circuitry to handle loss of power using NMI is not required. Circuitry is, however, required to insure proper initialization of the MPU when power is turned on. This circuit should insure that the Restart signal is held low for eight $\phi1$ clock cycles after the V_{CC} power supply reaches a voltage of approximately 4.75 volts DC. Also, in order to insure that a PIA or ACIA is not inadvertently selected during the power-on sequence, Three-State Control (TSC) should be held high until the positive transition of Restart.

$\overline{HALT}$—The $\overline{Halt}$ line is tied to V_{CC} and will automatically place the MPU in the run state when power is turned on. This signal may be used to halt the MPU if a switch is used to tie the line to ground for HALT and to V_{CC} for RUN.

S6800

FIGURE 11 MINIMUM SYSTEM CONFIGURATION

AMI ®
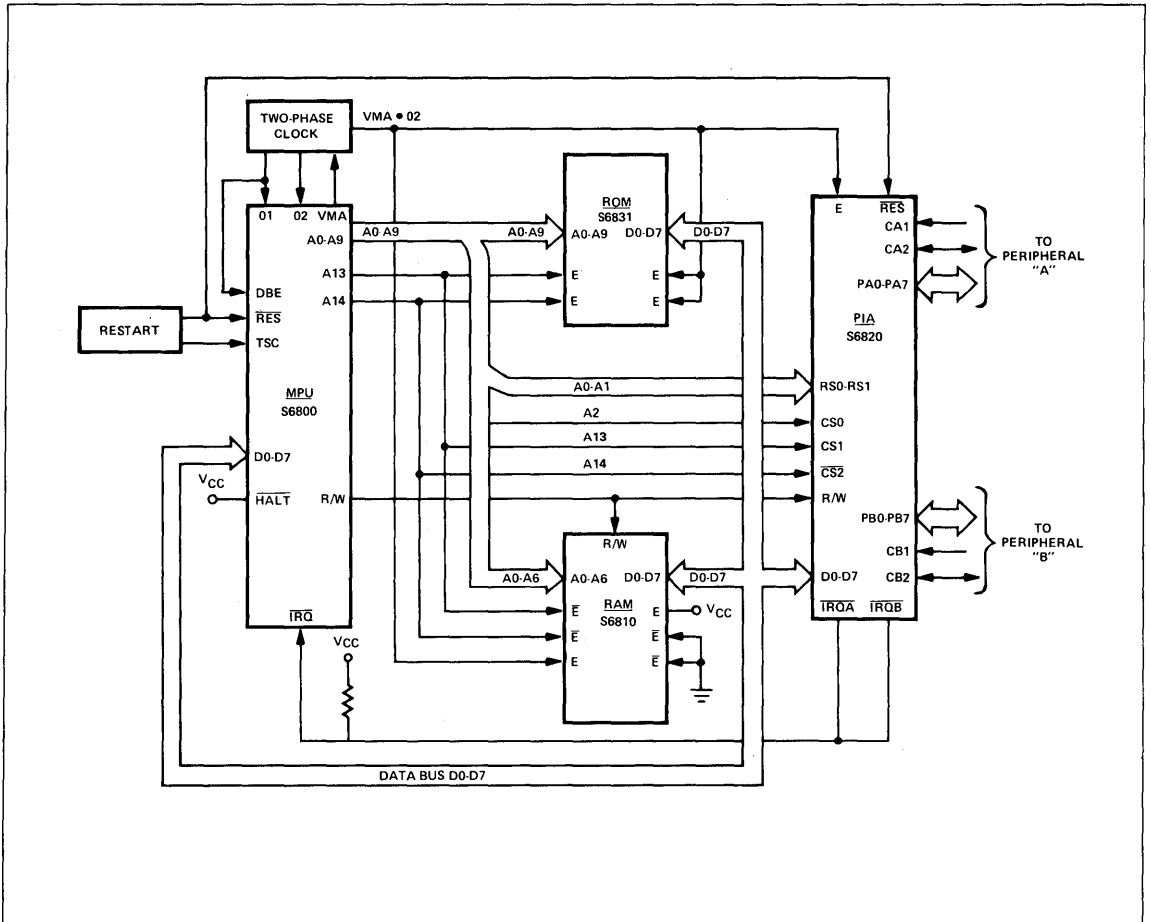
MICROCOMPUTER UNIT (MCU)*

Features

- Expanded S6800 instruction set

- Object code compatible with S6800

- Single chip or expandable to 65K words.

- 2K bytes of ROM

- 128 bytes of RAM (64 bytes retainable)

- 31 parallel I/O lines

- Internal Clock/Divide-by-Four mask option (S6801)

- External Clock/Divide-by-One mask option (S6801E)

- TTL compatible inputs and outputs

- Interrupt capability

- Hardware Multiply

General Description

The S6801 MCU is an 8-bit microcomputer system which is expandable, using the S6800 microprocessor family. The S6801 MCU is object code compatible with the S6800 instruction set with improved execution times of key instructions plus several new 16-bit and 8-bit instructions. The S6801 MCU can operate single chip or be expanded to 65K words. The S6801 MCU is TTL compatible and requires one + 5.0 volt power supply. The S6801 MCU has 2K bytes of ROM and 128 bytes of RAM on board. In addition, the S6801 MCU has on board serial and parallel I/O and three 16 stage timer function.

*Available 1st Quarter 1979

S6800

Block Diagram

AMI®
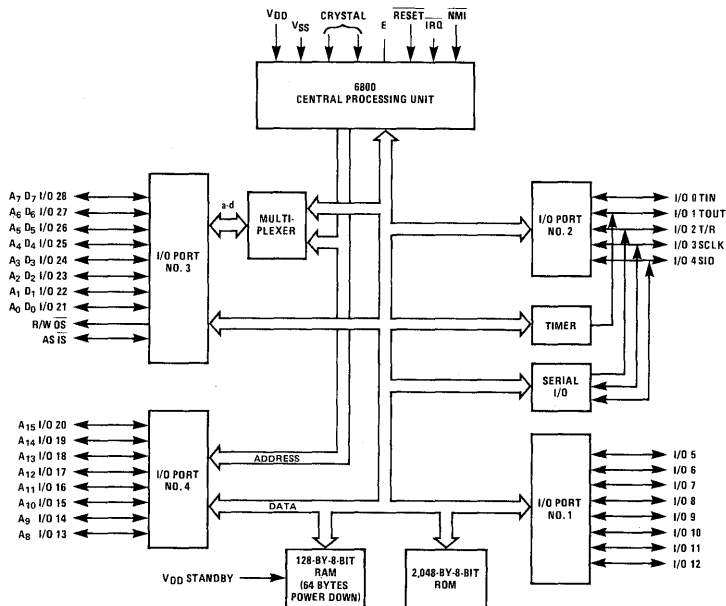
MICROPROCESSOR WITH CLOCK AND RAM

Features

☐ On-Chip Clock Circuit

☐ 128 x 8 Bit On-Chip RAM

☐ 32 Bytes of RAM Are Retainable

☐ Software-Compatible with the S6800

☐ Expandable to 65K Words

☐ Standard TTL-Compatible Inputs and Outputs

☐ 8-Bit Word Size

☐ 16-Bit Memory Addressing

☐ Interrupt Capability

General Description

The S6802 is a monolithic 8-bit microprocessor that contains all the registers and accumulators of the present S6800 plus an internal clock oscillator and driver on the same chip. In addition, the S6802 has 128 bytes of RAM on board located at hex addresses 0000 to 007F. The first 32 bytes of RAM, at hex addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation.

The S6802 is completely software compatible with the S6800 as well as the entire S6800 family of parts. Hence, the S6802 is expandable to 65K words. When the S6802 is interfaced with the S6846 ROM — I/O — Timer chip, as shown in the Block Diagram below, a basic 2-chip microcomputer system is realized.
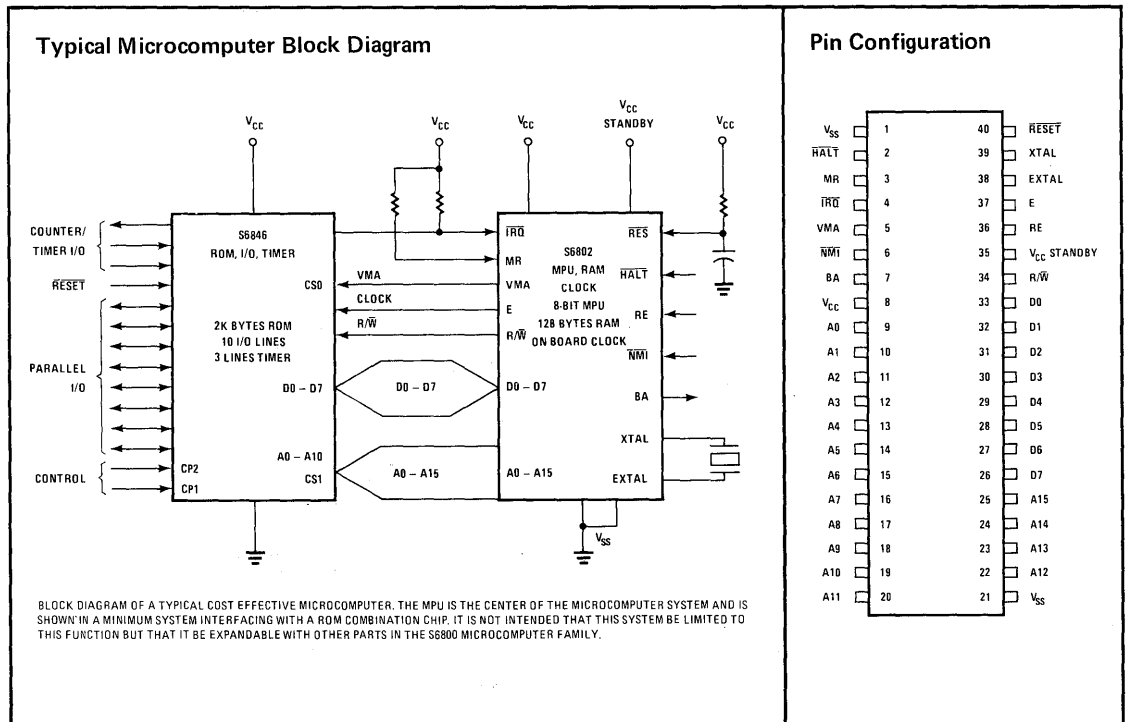
Typical Microcomputer Block Diagram

BLOCK DIAGRAM OF A TYPICAL COST EFFECTIVE MICROCOMPUTER. THE MPU IS THE CENTER OF THE MICROCOMPUTER SYSTEM AND IS SHOWN IN A MINIMUM SYSTEM INTERFACING WITH A ROM COMBINATION CHIP. IT IS NOT INTENDED THAT THIS SYSTEM BE LIMITED TO THIS FUNCTION BUT THAT IT BE EXPANDABLE WITH OTHER PARTS IN THE S6800 MICROCOMPUTER FAMILY.

Pin Configuration

This is advance information and specifications are subject to change without notice

Absolute Maximum Ratings

Supply Voltage	−0.3V to + 7.0V
Input Voltage	−0.3V to + 7.0V
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to + 150°C
Thermal Resistance	70°C/W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0$, $T_A = 0°C$ to $+70°C$ unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	Logic, EXtal	V_{SS} +2.0	—	V_{CC}	V
		$\overline{Reset}$	V_{SS} +4.0	—	V_{CC}	
V_{IL}	Input Leakage Voltage	Logic, EXtal, $\overline{Reset}$	V_{SS} − 0.3	—	V_{SS} + 0.8	V
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max)	Logic*	—	1.0	2.5	μA
V_{OH}	Output High Voltage					V
	(I_{LOAD} = − 205μA, V_{CC} = Min)	D0 — D7	V_{SS} +2.4	—	—	V
	(I_{LOAD} = − 145μA, V_{CC} = Min)	A0—A15, R/$\overline{W}$, VMA,E	V_{SS} +2.4	—	—	V
	(I_{LOAD} = − 100μA, V_{CC} = Min)	BA	V_{SS} +2.4	—	—	V
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mA, V_{CC} = Min)		—	—	V_{SS} + 0.4	V
P_D **	Power Dissipation		—	0.600	1.2	W
C_{IN}	Capacitance #					pF
	(V_{IN} = 0, T_A =25°C, f=1.0MHz	D0 — D7	—	10	12.5	
		Logic Inputs, EXtal	—	6.5	10	
C_{OUT}		A0 — A15, R/$\overline{W}$, VMA	—	—	12	pF

Clock Timing ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0$, $T_A = 0°C$ to $+70°C$ unless otherwise noted)

Symbol	Parameter		Min.	Typ.	Max.	Unit
f	Frequency of Operation	Input Clock÷4	0.1	—	1.0	MHz
f_{Xtal}		Crystal Frequency	1.0	—	4.0	
t_{CYC}	Cycle Time		1.0	—	10	μs
PW$_{\phi Hs}$ PW$_{\phi L}$	Clock Pulse Width Measured at 2.4V		450	—	4500	ns
t_ϕ	Fall Time Measured between V_{SS} + 0.4V and V_{SS} −2.4V		—	—	25	ns

*Except $\overline{IRQ}$ and $\overline{NMI}$, which require 3KΩ pullup load resistors for wire-OR capability at optimum operation. Does not include EXtal and Xtal, which are crystal inputs.
**In power-down mode, maximum power dissipation is less than 40mW.
#Capacitances are periodically sampled rather than 100% tested.

Read/Write Timing (Figures 1 through 5; Load Circuit of Figure 3).

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

Symbol	Parameters	Min.	Typ.	Max.	Unit
t_{AD}	Address Delay	—	—	270	ns
t_{ACC}	Peripheral Read Access Time $\quad t_{ACC} = t_{ut} - t_{DSR}$)	—	—	530	ns
t_{DSR}	Data Setup Time (Read)	100	—	—	ns
t_H	Input Data Hold Time	10	—	—	ns
t_{AH}	Address Hold Time (Address, R/$\overline{W}$, VMA)	20	—	—	ns
t_{DDW}	Data Delay Time (Write)	—	165	225	ns
t_{PCS}	Processor Controls: Processor Control Setup Time	200	—	—	ns
t_{PCr}, t_{PCf}	Processor Control Rise and Fall Time (Measured between 0.8V and 2.0V)	—	—	100	ns

Figure 1. Read Data From Memory or Peripherals
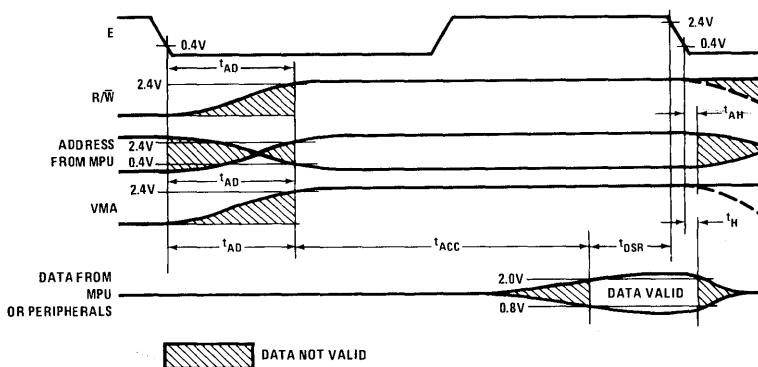
Figure 2. Write Data In Memory or Peripherals
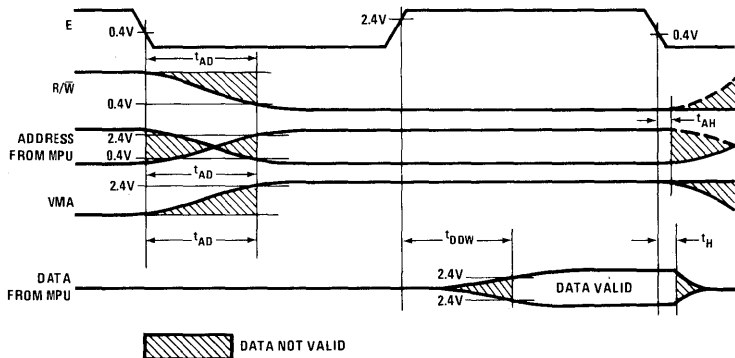
Figure 3. Bus Timing Test Load
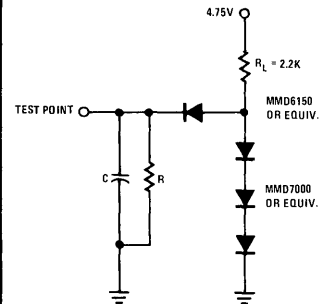
C = 130pF FOR D0 – D7, E
= 90pF FOR A0 – A15, R/$\overline{W}$, AND VMA
= 30pF FOR BA
R = 11.7 KΩ FOR D0 – D7, E
= 16.5KΩ FOR A0 – A15, R/$\overline{W}$, AND VMA
= 24KΩ FOR BA

Figure 4. Typical Data Bus Output Delay Versus Capacitive Loading

I_{OH} = −205 μA MAX @ 2.4V
I_{OL} = 1.6mA MAX @ 0.4V
V_{CC} = 5.0V
T_A = 25°C

C_L INCLUDES STRAY CAPACITANCE

C_L, LOAD CAPACITANCE (pF)

DELAY TIME (ns)
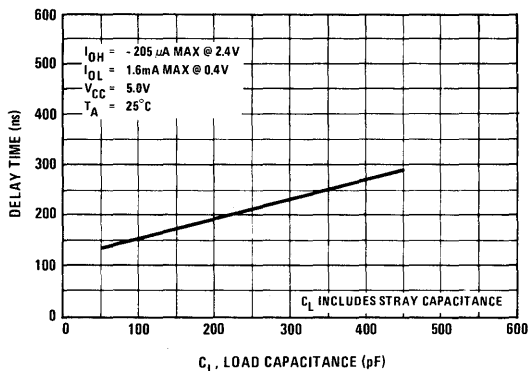
Figure 5. Typical Read/Write, VMA, and Address Output Delay Versus Capacitive Loading

I_{OH} = −145 μA MAX @ 2.4V
I_{OL} = 1.6mA MAX @ 0.4V
V_{CC} = 5.0V
T_A = 25°C

ADDRESS, VMA

R/W

C_L INCLUDES STRAY CAPACITANCE

C_L LOAD CAPACITANCE (pF)

DELAY TIME (ns)
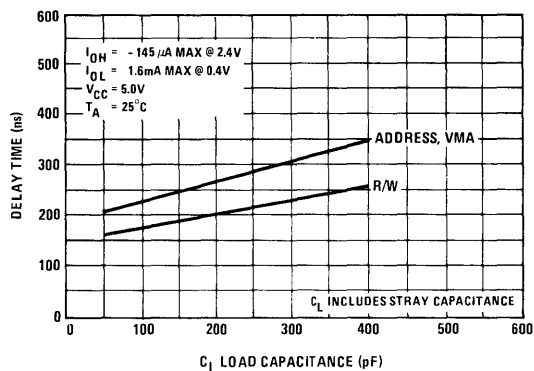
S6800

Figure 6. S6802 Expanded Block Diagram

V_{CC} = PIN 8, 35
V_{SS} = PIN 1, 21
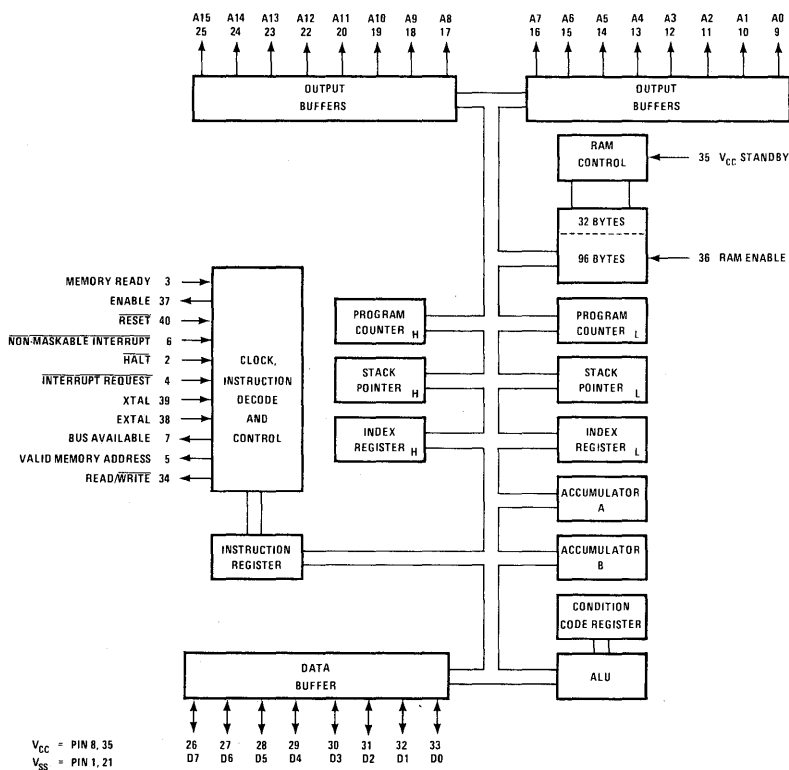
Functional Description

MPU Registers

A general block diagram of the S6802 is shown in Figure 6. As shown, the number and configuration of the registers are the same as for the S6800. The 128 x 8 bit RAM has been added to the basic MPU. The first 32 bytes may be operated in a low power mode via a V_{CC} standby. These 32 bytes can be retained during power-up and power-down conditions via the RE signal.

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer (Figure 7).

Program Counter — The program counter is a two byte (16-bits) register that points to the current program address.

Stack Pointer — The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register — The index register is a two byte register that is used to store data or a sixteen-bit memory address for the Indexed mode of memory addressing.

Accumulators — The MPU contains two 8-bit accumulators that are used to hold operands and results from an arithmetic logic unit (ALU).

Condition Code Register — The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and Half Carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The used bits of the Condition Code Register (b6 and b7) are ones.

Figure 8 shows the order of saving the microprocessor status within the stack.

Figure 7. Programming Model of the Microprocessing Unit
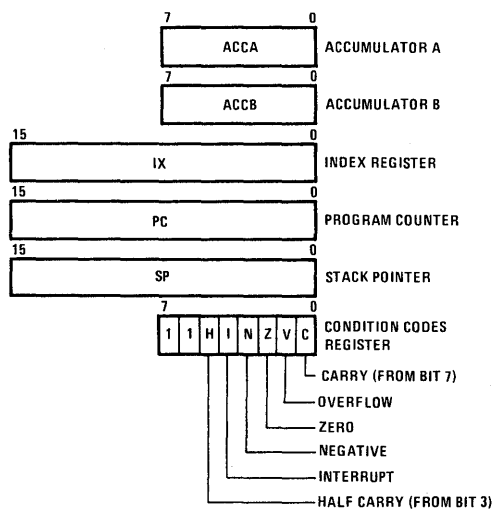
Figure 8. Saving the Status of the Microprocessor in the Stack
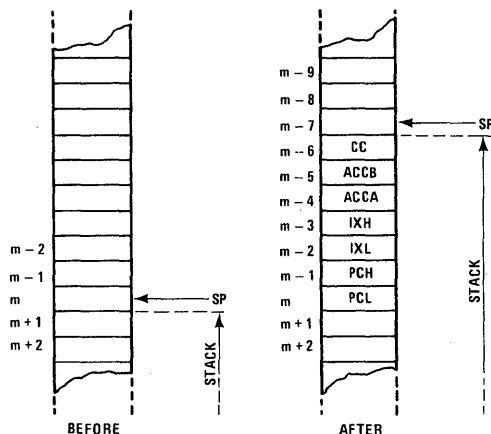
SP = STACK POINTER
CC = CONDITION CODES (ALSO CALLED THE PROCESSOR STATUS BYTE)
ACCB = ACCUMULATOR B
ACCA = ACCUMULATOR A
IXH = INDEX REGISTER, HIGHER ORDER 8 BITS
IXL = INDEX REGISTER, LOWER ORDER 8 BITS
PCH = PROGRAM COUNTER, HIGHER ORDER 8 BITS
PCL = PROGRAM COUNTER, LOWER ORDER 8 BITS

S6800

S6802 MPU Signal Description

Proper operation of the MPU requires that certain control and timing signals be provided to accomplish specific functions and that other signal lines be monitored to determine the state of the processor. These control and timing signals for the S6802 are identical to those of the S6800 except that TSC, DBE, $\phi1$, $\phi2$ input, and two unused pins have been eliminated, and the following signal and timing lines have been added:

    RAM Enable (RE)

    Crystal Connections EXtal and Xtal

    Memory Ready (MR)

    V$_{CC}$ Standby

    Enable $\phi2$ Output (E)

The following is a summary of the S6802 MPU signals:

Address Bus (A0 — A15) — Sixteen pins are used for the address bus. The outputs are capable of driving one standard TTL load and 130pF.

Data Bus (D0 — D7) — Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state-output buffers capable of driving one standard TTL load and 130pF.

Halt — When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a high state, Valid Memory Address will be at a low state, and all other three-state lines will be in the three-state mode. The address bus will display the address of the next instruction.

To insure single instruction operation, transition of the Halt line must not occur during the last 250ns of E and the Halt line must go high for one Clock cycle.

Read/Write (R/W) — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high).

Figure 9. Power-up and Reset Timing
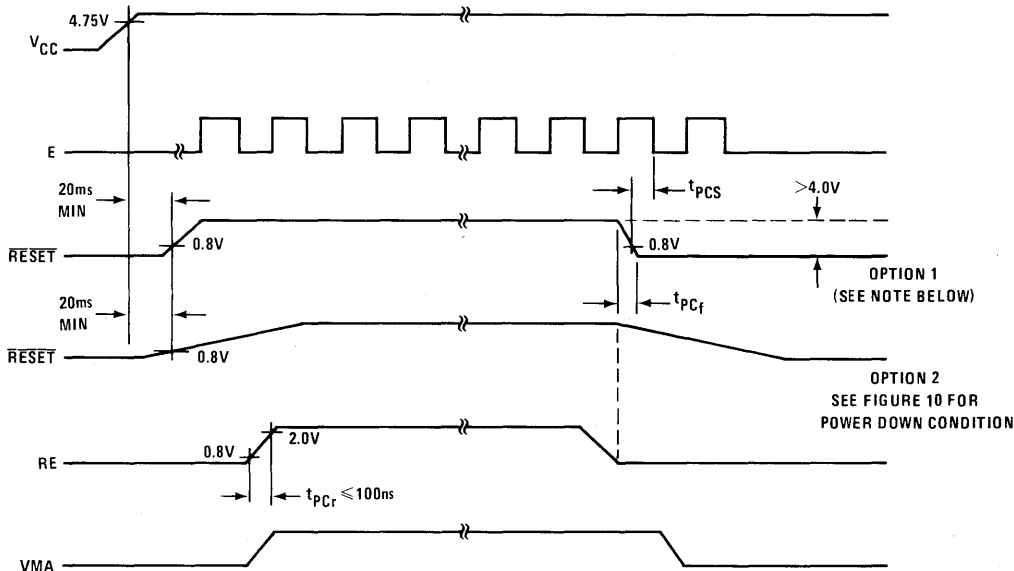
NOTE: IF OPTION 1 IS CHOSEN, RESET AND RE PINS CAN BE TIED TOGETHER.

When the processor is halted, it will be in the logical one state. This output is capable of driving one standard TTL load and 90pF.

Valid Memory Address (VMA) — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 90pF may be directly driven by this active high signal.

Bus Available (BA) — The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the Halt line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or non-maskable interrupt. This output is capable of driving one standard TTL load and 30pF.

Interrupt Request (IRQ) — This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The Halt line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while Halt is low.

The IRQ has a high impedance pull-up device internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrrupts.

Reset — This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. When this line is low, the MPU is inactive and the informa-

tion in the registers will be lost. If a high level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by IRQ. Power-up and reset timing and power-down sequences are shown in Figures 9 and 10, respectively.

Figure 10. Power-Down Sequence
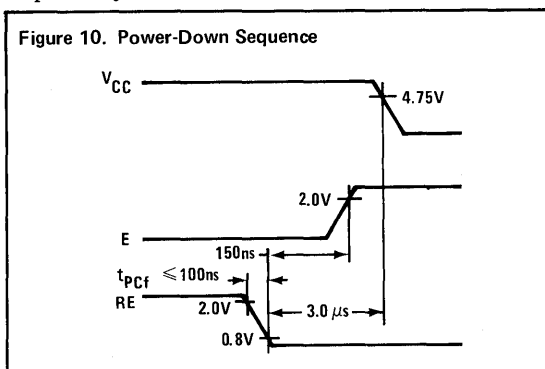
Non-Maskable Interrupt (NMI) — A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the NMI signal. The interrupt mask bit in the Condition Code Register has no effect on NMI.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations caused the MPU to branch to a non-maskable interrupt routine in memory.

NMI has a high impedance pull-up resistor internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs IRQ and NMI are hardware interrupt lines that are sampled when E is high and will start the interrupt routine on a low E following the completion of an instruction.

Figure 11 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 1 gives the memory map for interrupt vectors.

RAM Enable (RE) — A TTL-compatible RAM enable input controls the on-chip RAM of the S6802. When placed in the high state, the on-chip memory is enabled to respond to the MPU controls. In the low state, RAM is disabled. This pin may also be utilized to disable reading and writing the on-chip RAM during power-down situation. RAM enable must be low three μs before V_{CC} goes below 4.75V during power-down.

EXtal and Xtal — The S6802 has an internal oscillator that may be crystal controlled. These connections are for a series resonant fundamental crystal. (AT out.) A divide-by four circuit has been added to the S6802 so that a 4MHz crystal may be used in lieu of a 1MHz crystal for a more cost effective system. Pin 38 of the S6802 may be driven externally by a TTL input signal if a separate clock is required. Pin 39 is to be left open in this mode.

Memory Ready (MR) — MR is a TTL compatible input control signal which allows stretching of E. When MR is high, E will be in normal operation.

When MR is low, it may be stretched integral multiples of half periods, thus allowing interface to slow memories. Memory Ready timing is shown in Figure 12.

Enable (E) — This pin supplies the clock for the MPU and the rest of the system. This is a single phase, TTL compatible clock. This clock may be conditioned by a Memory Ready Signal. This is equivalent to $\phi2$ on the S6800.

V_{CC} Standby — This pin supplies the dc voltage to the first 32 bytes of RAM as well as the RAM Enable (RE) control logic. Thus retention of data in this portion of the RAM on a power-up, power-down, or standby condition is guaranteed. Maximum current drain at 5.25V is 8mA.

Table 1. Memory Map for Interrupt Vectors

VECTOR		DESCRIPTION
MS	LS	
FFFE	FFFF	RESTART
FFFC	FFFD	NON-MASKABLE INTERRUPT
FFFA	FFFB	SOFTWARE INTERRUPT
FFF8	FFF9	INTERRUPT REQUEST

Figure 11. MPU Flow Chart

RESET

START SEQUENCE
FFFE, FFFF

HALT — YES

MACHINE
ON HALT

HALT — YES — NO

NMI — YES — NO

IRQ — YES — NO

MASK ON — YES — NO

FETCH INSTRUCTION

EXECUTE
INSTRUCTION

EXECUTE
INTERRUPT ROUTINE

NMI	IRQ
FFFC	FFF8
FFFD	FFF9
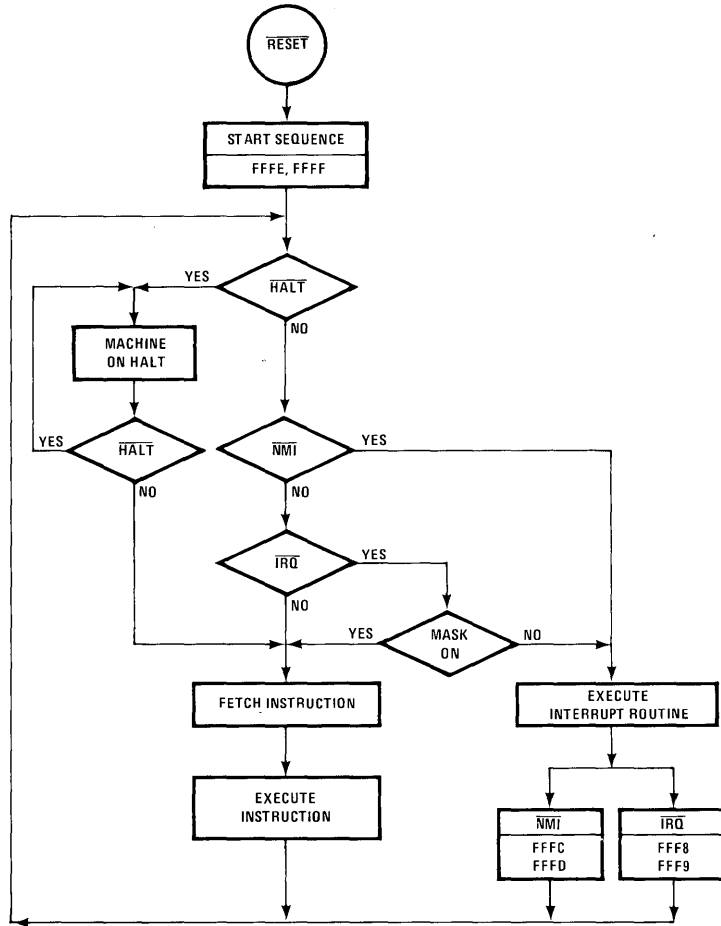
Figure 12. Memory Ready Control Function

A – SETUP

B – RELEASE

E

2.4V

0.4V

≤200NS

t_{PCf} ≤100NS

≥300NS

≤100NS

MR

2.0V

0.8V

2.0V

0.8V

Contact AMI for complete product description.

3.30

AMI ®
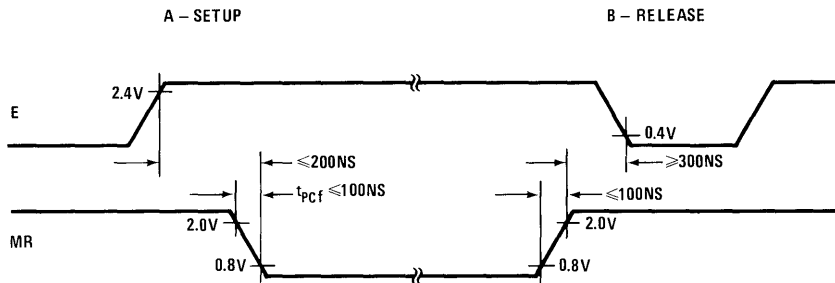
HIGH PERFORMANCE
MICROPROCESSOR*

Features

- Upward source compatible with S6800
- Bus compatible with S6800 family
- 2MHz Bus operation
- Pin-out compatible with S6800/S6802
- On-chip Oscillation/Clock Driver
- TTL compatible I/O
- 3 priority Interrupts
- Fast Interrupt — Cuts Response Time
- Interrupt acknowledge allows vectoring by device
- Memory Ready Signal for slow memory
- +5V Power Supply
- Expandable to 64 K words

Block Diagram
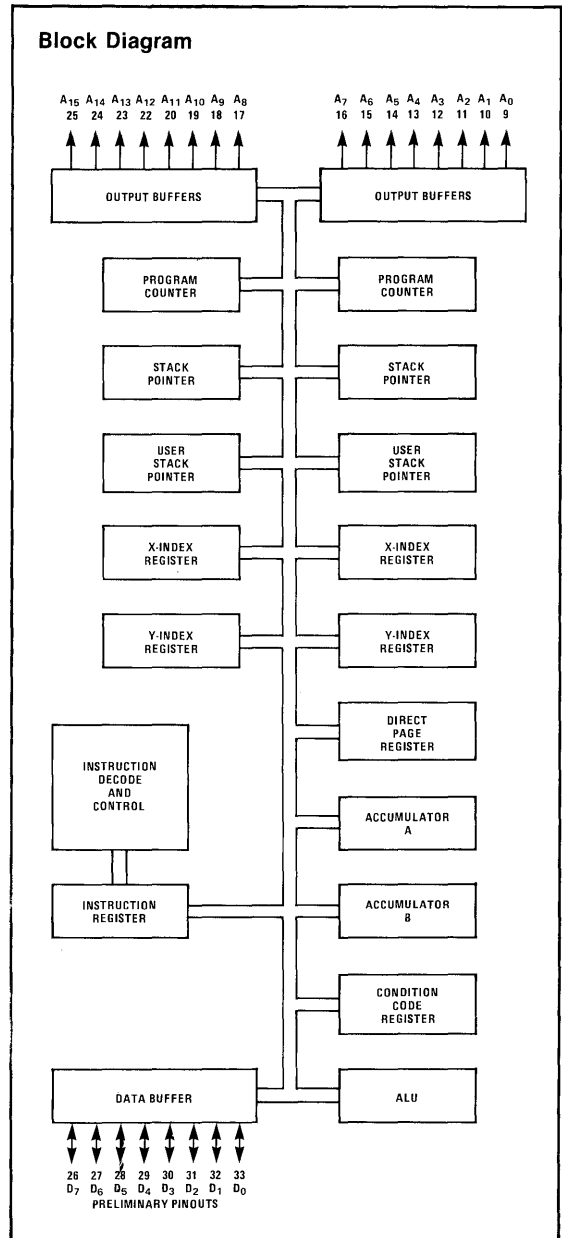
General Description

The S6809 is a monolithic microprocessor that contains all the registers of the S6800 plus an additional clock oscillator and driver on chip.

The S6809 gives the user 8- and 16-bit word capability, while retaining software compatibility with the basic S6800 family. Four 8-bit-wide registers and five 16-bit-wide ones process the data, with the 8-bit accumulators supplying routing computation.

The S6809 is compatible with the complete set of S6800 peripheral and memory devices. It is designed for the middle and high end of the microprocessor scale.

*Available 1st Quarter 1979

AMI®

128x8 STATIC READ/WRITE MEMORY

Features

☐ Organized as 128 Bytes of 8 Bits
☐ Static Operation
☐ Bi-Directional Three-State Data Input/Output
☐ Six Chip Enable Inputs (Four Active Low, Two Active High)
☐ Single 5-Volt Power Supply
☐ TTL Compatible
☐ Maximum Access Time = 450ns for S6810A 350ns for S6810A – 1

General Description

The S6810A is a static 128 x 8 Read/Write Memory designed and organized to be compatible with the S6800 Microprocessor. Interfacing to the S6810A consists of an 8-Bit Bidirectional Data Bus, Seven Address Lines, a single Read/Write Control line, and six Chip Enable lines — four negative and two positive.

For ease of use, the S6810A is a totally static memory requiring no clocks or cell refresh. The S6810A is fabricated with N-channel silicon gate depletion mode technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

Block Diagram

Pin Configuration

S6800
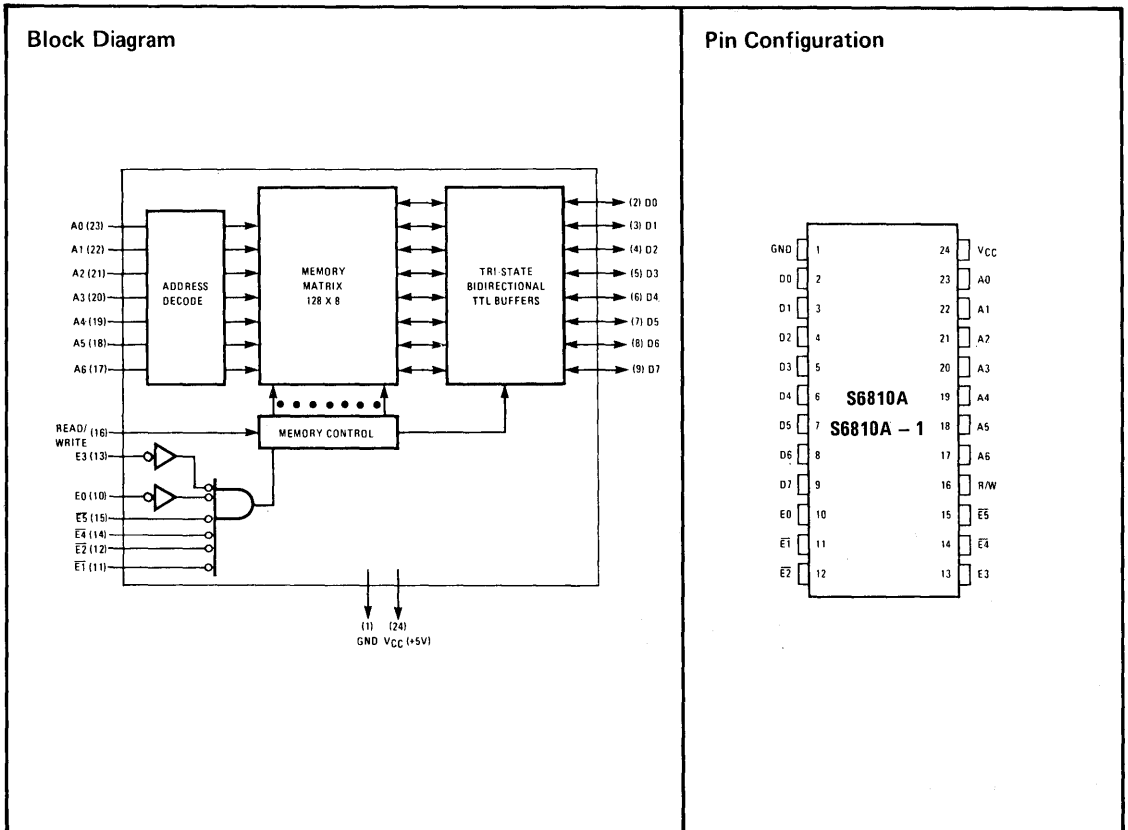
Absolute Maximum Ratings

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Supply Voltage V_{CC} .... − 0.3 to +7.0V
Input Voltage V_{IN} .... − 0.3 to +7.0V
Operating Temperature Range T_A .... $0°C$ to $+70°C$
Storage Temperature Range T_{stg} .... − $55°C$ to $+150°C$

DC (Static) Characteristics

V_{CC} = 5.0V ± 5%; T_A = $0°C$ to $+70°C$ unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0	—	5.25	V	
V_{IL}	Input Low Voltage	− 0.3	—	0.8	V	
I_{IN}	Input Current (A_n, R/W, E_n, $\overline{E}_n$) (V_{IN} = 0 to 5.25V)	—	—	2.5	μA	
V_{OH}	Output High Voltage (I_{OH} = 205 μA)	2.4	—	—	V	
V_{OL}	Output Low Voltage (I_{OL} = 1.6mA)	—	—	0.4	V	
I_{LIH}	Output Leakage Current (D0 − D7) (V_0 = 2.4V, E = 0.8V, $\overline{E}$ = 2.0V)	—	—	10	μA	
I_{LOL}	Output Leakage Current (D0 − D7) (V_0 = 0.4V, E = 0.8V, $\overline{E}$ = 2.0V)	—	—	10	μA	
I_{CC}	Supply Current (V_{CC} = 5.25V, T_A = $0°C$) S6810A S6810A − 1	— —	— —	70 80	mA mA	
C_{IN}	Input Capacitance*	—	—	7.5	pF	f=1.0MHz, T_A=$25°C$
C_{OUT}	Output Capacitance*	—	—	—	—	f=1.0MHz, T_A=$25°C$

*This parameter periodically sampled rather than 100% tested.

AC (Dynamic) Characteristics

V_{CC} = 5.0V ± 5%, T_A = $0°C$ to $+70°C$

Symbol	Parameter	Min.	Max.	Unit
t_{AS}	Address Setup Time	20	—	ns
t_{AH}	Address Hold Time	0	—	ns
t_{CS}	Chip Enable Pulse Width S6810A	230	—	ns
	S6810A − 1	180	—	ns

Read Cycle

(All timing with low input pulse 0.8V, high input pulse 2.0V, t_r = t_f = 20ns, Load of Figure 1)

Symbol	Parameter		Min.	Max.	Unit
$t_{CYC\ (R)}$	Read Cycle Time	S6810A	450	—	ns
		S6810A − 1	350	—	ns
t_{DD}	Output Disable Delay Time	S6810A	10	—	ns
		S6810A − 1	10	—	ns
t_{ACC}	Read Access Time	S6810A	—	450	ns
		S6810A − 1	—	350	ns
t_{RCS}	Read to Select Delay Time	S6810A	0	—	ns
		S6810A − 1	0	—	ns

Write Cycle

(All timing with low input pulse 0.80, high input pulse 2.0V, t_r = t_f = 20ns, Load of Figure 1)

Symbol	Parameter		Min.	Max.	Unit
$t_{CYC\ (W)}$	Write Cycle Time	S6810A	450	—	ns
		S6810A − 1	350	—	ns
t_{WP}	Write Pulse Width	S6810A	300	—	ns
		S6810A − 1	250	—	ns
t_{DS}	Data Setup Time	S6810A	190	—	ns
		S6810A − 1	150	—	ns
t_{WCS}	Write to Select Delay Time	S6810A	0	—	ns
		S6810A − 1	0	—	ns

Figure 1. AC Test Load

TEST POINT

5.0V

R_L = 2.5k

MMD6150
OR EQUIV

130 pF*   11.7k

MMD7000
OR EQUIV

1176162

*Includes Jig Capacitance
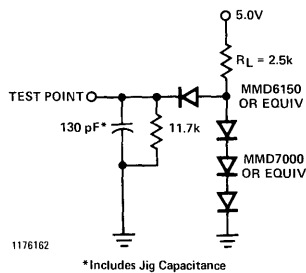
Timing Characteristics

Figure 2. Read Cycle Timing
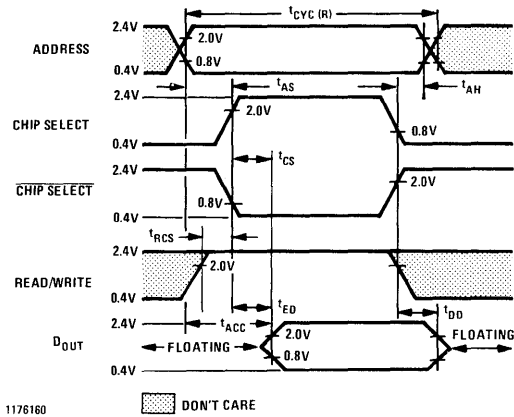
1176160

Figure 3. Write Cycle Timing
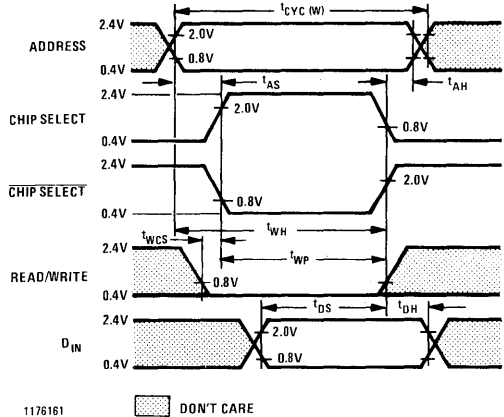
1176161

Physical Dimensions
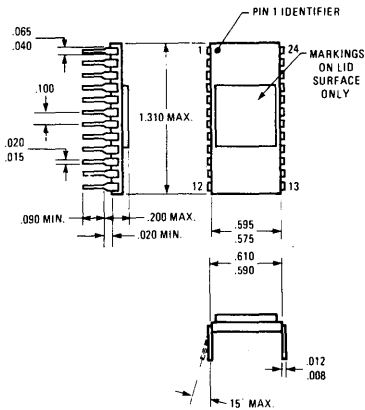
Ordering Information

Order No.	No. Pins	Package	Temp. Range	Description
S6810AP	40	Plastic	$0 - 70°C$	NMOS 128 x 8 Static RAM, T_{AA}=450ns Max
S6810A	24	Ceramic	$0 - 70°C$	NMOS 128 x 8 Static RAM, T_{AA}=450ns Max
S6810A-1P	24	Plastic	$0 - 70°C$	NMOS 128 x 8 Static RAM, T_{AA}=350ns Max
S6810A-1	24	Ceramic	$0 - 70°C$	NMOS 128 x 8 Static RAM, T_{AA}=350ns Max

AMI®

128 × 8 STATIC READ/WRITE MEMORY

Features

☐ Organized as 128 Bytes of 8 Bits

☐ Static Operation

☐ Bidirectional Three-State Data Input/Output

☐ Six Chip Enable Inputs (Four Active Low, Two Active High)

☐ Single 5 Volt Power Supply

☐ TTL Compatible

☐ Maximum Access Time:
—360ns for S68A10
—250ns for S68B10

General Description

The S68A10 and S68B10 are static 128x8 Read/Write Memories designed and organized to be compatible with the S68A00 and S68B00 Microprocessors. Interfacing to the S68A10 and S68B10 consists of an 8-bit bidirectional data bus, seven address lines, a single Read/Write control line, and six chip enable lines, four negative and two positive.

For ease of use, the S68A10 and S68B10 are a totally static memory requiring no clocks or cell refresh. The S68A10 and S68B10 are fabricated with N-channel silicon gate depletion load technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.
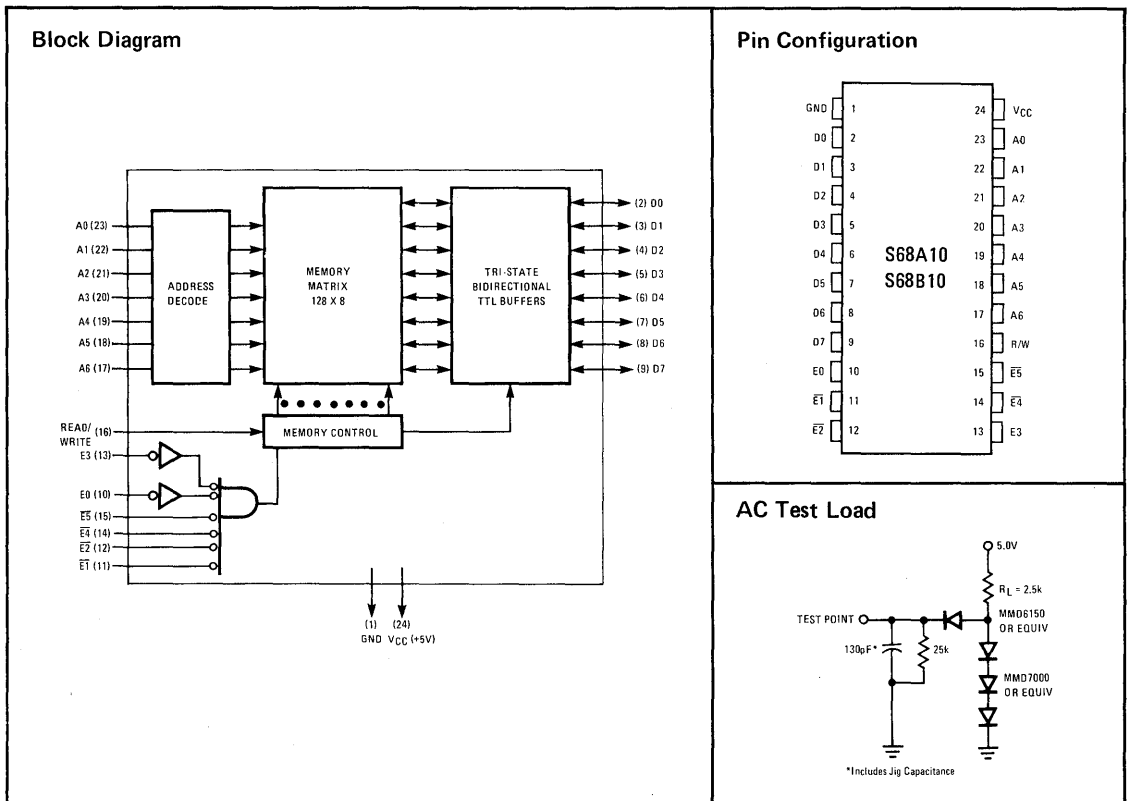
Block Diagram

Pin Configuration

AC Test Load

*Includes Jig Capacitance

Absolute Maximum Ratings

Supply Voltage	$-0.3V$ to $+7.0V$
Input Voltage	$-0.3V$ to $+7.0V$
Operating Temperature Range	$0°C$ to $+70°C$
Industrial Temperature Range	$-40°C$ to $+85°C$
Military Temperature Range	$-55°C$ to $+125°C$
Storage Temperature Range	$-55°C$ to $+150°C$

DC Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{IN}	Input Current (A_n, R/W, CS_n, $\overline{CS_n}$)			2.5	μAdc	V_{IN} = 0V to 5.25V
V_{OR}	Output High Voltage	2.4			Vdc	I_{OH} = -205μA
V_{OL}	Output Low Voltage			0.4	Vdc	I_{OL} = 1.0mA
I_{LO}	Output Leakage Current (Three-State)			10	μAdc	CS = 0.8V or $\overline{CS}$ = 2.0V, V_{OUT} = 0.4V to 2.4V
I_{CC}	Supply Current			80	mAdc	V_{CC} = 5.25V, all other pins grounded, T_A = 0°C

AC Characteristics

Read Cycle (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	S68A10		S68B10		Units
		Min.	Max.	Min.	Max.	
$t_{cyc(R)}$	Read Cycle Time	360		250		ns
t_{acc}	Access Time		360		250	ns
t_{AS}	Address Setup Time	20		20		ns
t_{AH}	Address Hold Time	0		0		ns
t_{DDR}	Data Delay Time (Read)		220		180	ns
t_{RCS}	Read to Select Delay Time	0		0		ns
t_{DHA}	Data Hold from Address	10		10		ns
t_H	Output Hold Time	10		10		ns
t_{DHW}	Data Hold from Write	10	60	10	60	ns

Write Cycle (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	S68A10		S68B10		Units
		Min.	Max.	Min.	Max.	
$t_{cyc(W)}$	Write Cycle Time	360		250		ns
t_{AS}	Address Setup Time	20		20		ns
t_{AH}	Address Hold Time	0		0		ns
t_{CS}	Chip Select Pulse Width	250		210		ns
t_{WCS}	Write to Chip Select Delay Time	0		0		ns
t_{DSW}	Data Setup Time (Write)	80		60		ns
t_H	Input Hold Time	10		10		ns

S6800

Read Cycle Timing

$t_{cyc(R)}$

t_{acc}

ADDRESS
2.0V
0.8V

t_{AS}

t_{AH}

CS
0.8V
2.0V

t_{DDR}

$\overline{CS}$
2.0V
0.8V

t_{RCS}

R/W
2.0V

t_{DHA}

t_{H}

t_{DHW}

DATA OUT
2.0
0.8
DATA VALID

DON'T CARE

Note: CS and $\overline{CS}$ can be enabled for consecutive read cycles provided R/W remains at V_{IH}.

Write Cycle Timing

$t_{cyc(W)}$

ADDRESS
2.0V
0.8V

t_{AS}

t_{CS}

t_{AH}

CS
0.8V
2.0V

$\overline{CS}$
2.0V
0.8V

t_{WCS}

R/W
0.8V

t_{DSW}

t_{H}

DATA IN
2.0V
0.8V
DATA IN STABLE

DON'T CARE

Note: CS and $\overline{CS}$ can be enabled for consecutive write cycles provided R/W is strobed to V_{IH} before or coincident with the Address change, and remains high for time t_{AS}.

3.38

AMI®

PERIPHERAL INTERFACE ADAPTER (PIA)

Features

- ☐ 8-Bit Bidirectional Data Bus for Communication with the MPU
- ☐ Two Bidirectional 8-Bit Buses for Interface to Peripherals
- ☐ Two Programmable Control Registers
- ☐ Two Programmable Data Direction Registers
- ☐ Four Individually-Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs
- ☐ Handshake Control Logic for Input and Output Peripheral Operation
- ☐ High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- ☐ Program Controlled Interrupt and Interrupt Disable Capability
- ☐ CMOS Compatible Peripheral Lines

General Description

The S6821/S68A21/S68B21 are peripheral Interface Adapters that provide the universal means of interfacing peripheral equipment to the S6800, S68A00 and S68B00 Microprocessing Units (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The PIA interfaces to the S6800/S68A00/S68B00 MPUs with an eight-bit bidirectional data bus, three

S6800

Block Diagram

Pin Configuration

877255
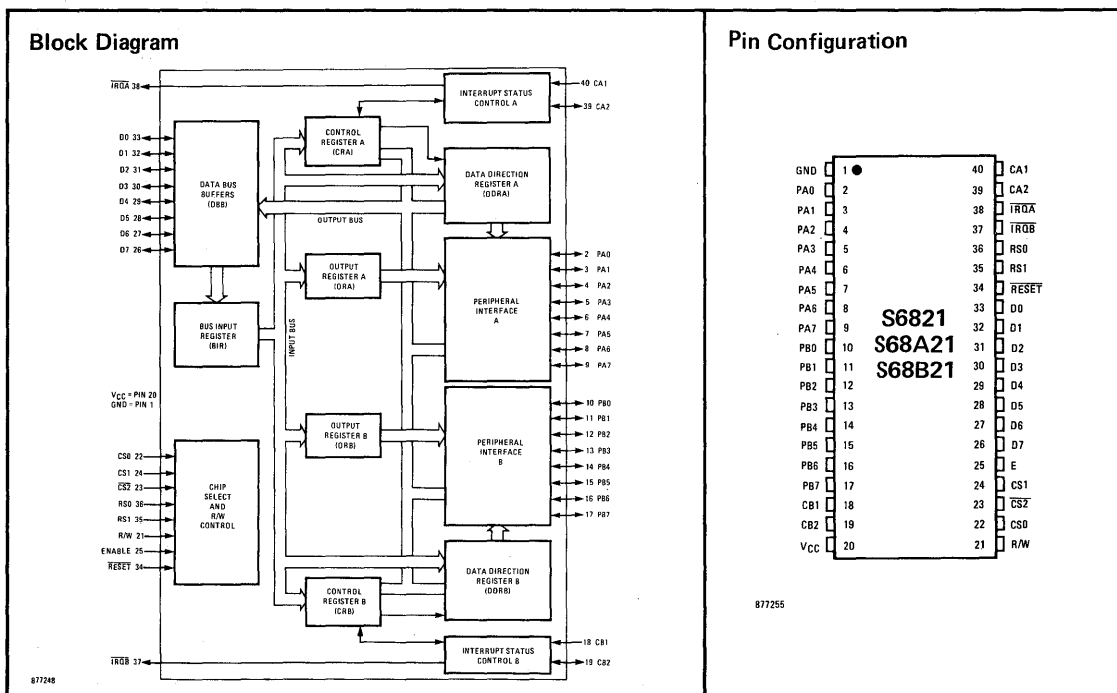
General Description (Continued)

chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the S6800/S68A00/S68B00 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

Absolute Maximum Ratings

Supply Voltage	-0.3V to $+7.0$V
Input Voltage	-0.3V to $+7.0$V
Operating Temperature Range	$0°$C to $+70°$C
Industrial Temperature Range	$-40°$C to $+85°$C
Military Temperature Range	$-55°$C to $+125°$C

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage		V_{SS}+2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage		V_{SS}- 0.3		V_{SS}+0.8	Vdc	
I_{in}	Input Leakage Current R/W, Reset, RS0, RS1, CS0, $\overline{CS2}$, CS1, CA1, CB1, Enable			1.0	2.5	μAdc	V_{in} = 0Vdc to +5.25Vdc
I_{TSI}	Three-State (Off State) Input Current D0-D7, PB0-PB7, CB2			2.0	10	μAdc	V_{in} = 0.4Vdc to 2.4Vdc
I_{IH}	Input High Current PA0-PA7, CA2		- 200	-400		μAdc	V_{IH} = 2.4Vdc
I_{IL}	Input Low Current PA0-PA7, CA2			- 1.3	- 2.4	mAdc	V_{IL} = 0.4Vdc
V_{OH}	Output High Voltage						
		D0-D7	V_{SS}+2.4			Vdc	I_{Load} = - 205μAdc
		Other Outputs	V_{SS}+2.4			Vdc	I_{Load} = - 200μAdc
V_{OL}	Output Low Voltage						
		D0-D7			V_{SS}+0.4	Vdc	I_{Load} = 1.6mAdc
		Other Outputs			V_{SS}+0.4	Vdc	I_{Load} = 3.2mAdc
I_{OH}	Output High Current (Sourcing)						
		D0-D7	- 205			μAdc	V_{OH} = 2.4Vdc
		Other Outputs	- 100			μAdc	
		PB0-PB7, CB2	- 1.0	- 2.5	- 10	mAdc	V_O = 1.5Vdc, the current for driving other than TTL, e.g., Darlington Base
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQA}$, $\overline{IRQB}$			1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation				550	mW	
C_{in}	Capacitance						
		D0-D7			12.5	pF	V_{in} = 0, T_A = +25°C,
	PA0-PA7, PB0-PB7, CA2, CB2				10	pF	f = 1.0MHz
	Enable, R/W, Reset, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1				7.5	pF	
C_{out}		$\overline{IRQA}$, $\overline{IRQB}$			5.0	pF	

Note: The PA0-PA7 Peripheral Data lines and the CA2 Peripheral Control line can drive two standard TTL loads. In the input mode, the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

A.C. (Dynamic) Characteristics Loading = 30pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2
= 130pF and one TTL load for D0-D7, $\overline{IRQA}$, $\overline{IRQB}$
(V_{CC} = +5.0V ±5%, T_A = 0°C to +70°C unless otherwise noted.)

Read Timing Characteristics (Figure 1)

Timing Characteristics (V_{CC} = + 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

Symbol	Parameter	S6821 Min.	S6821 Max.	S68A21 Min.	S68A21 Max.	S68B21 Min.	S68B21 Max.	Units	Conditions
t_{PDSU}	Peripheral Data Setup Time	200		135		100		ns	
t_{PDH}	Peripheral Data Hold Time	0		0		0		ns	
t_{CA2}	Delay Time, Enable Negative Transition to CA2 Negative Transition		1.0		0.670		0.5	μs	
t_{RS1}	Delay Time, Enable Negative Transition to CA2 Positive Transition		1.0		0.670		0.5	μs	
t_r, t_f	Rise and Fall Times for CA1 and CA2 Input Signals		1.0		1.0		1.0	μs	
t_{RS2}	Delay Time from CA1 Active Transition to CA2 Positive Transition		2.0		1.35		1.0	μs	
t_{PDW}	Delay Time, Enable Negative Transition to Peripheral Data Valid		1.0		0.670		0.5	μs	
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral CMOS PA0-PA7, CA2 Data Valid		2.0		1.35		1.0	μs	$V_{CC} - 30\%$ V_{CC}; Figure 6, Load C
t_{CB2}	Delay Time, Enable Positive Transition to CB2 Negative Transition		1.0		0.670		0.5	μs	
t_{DC}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	20		20		20		ns	
t_{RS1}	Delay Time, Enable Positive Transition to CB2 Positive Transition		1.0		0.670		0.5	μs	
PW_{CT}	Peripheral Control Output Pulse Width, CA2/CB2	550		550		550		ns	
t_r, t_f	Rise and Fall Time for CB1 and CB2 Input Signals		1.0		1.0		1.0	μs	
t_{RS2}	Delay Time, CB1 Active Transition to CB2 Positive Transition		2.0		1.35		1.0	μs	
t_{IR}	Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$		1.6		1.1		0.85	μs	
t_{RS3}	Interrupt Response Time		1.0		1.0		1.0	μs	
PW_I	Interrupt Input Pulse Width	500		500		500		ns	
t_{RL}	Reset Low Time*	1.0		0.66		0.5		μs	

*The Reset line must be high a minimum of 1.0μs before addressing the PIA.

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Bus Timing Characteristics ($V_{CC} = +5.0V \pm 5\%$, $V_{SS} = 0V$, $T_A = 0°C$ to $+70°C$ unless otherwise noted.)

Read

Symbol	Parameter	S6821		S68A21		S68B21		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{cycE}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.280		0.22		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Write

Symbol	Parameter	S6821		S68A21		S68B21		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{cycE}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.280		0.22		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Data Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Figure 1. Peripheral Data Setup Time (Read Mode)
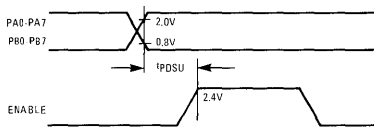
Figure 2. CA2 Delay Time (Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

*Assumes part was deselected during the previous E pulse.

877259
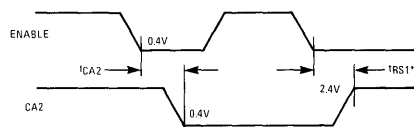
877260

Figure 3. CA2 Delay Time
   (Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)
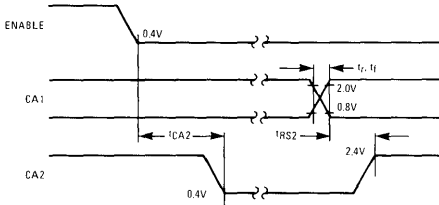
877261

Figure 4. Peripheral CMOS Data Delay Times
   (Write Mode: CRA-5 = CRA-3 = 1, CRA-4 = 0)
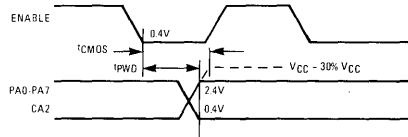
877262

Figure 5. Peripheral Data and CB2 Delay Times
   (Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)
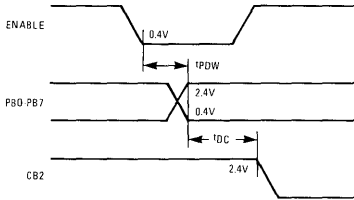
CB2 Note:
   CB2 goes low as a result of the positive transition of Enable.

877263

Figure 6. CB2 Delay Time
   (Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)
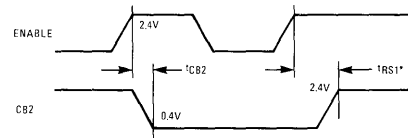
*Assumes part was deselected during the previous E pulse.

877264

Figure 7. CB2 Delay Time
   (Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)
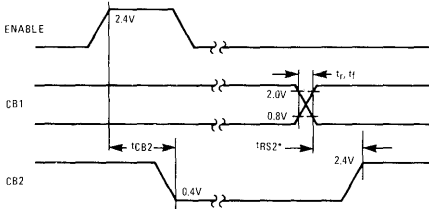
*Assumes part was deselected during any previous E pulse.

877265

Figure 8. IRQ Release Time
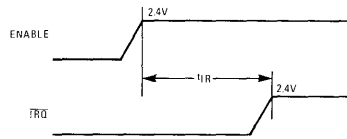
877266

Figure 9. RESET Low Time
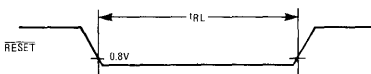
*The Reset line must be a V_IH for a minimum of 1.0μs
before addressing the PIA.

877267

Figure 10. Bus Read Timing Characteristics
   (Read Information from PIA)

877268

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3.43
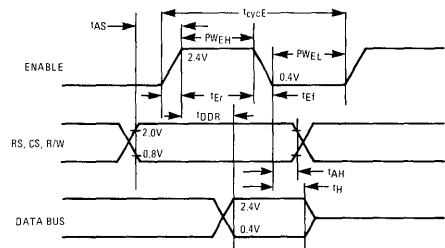
Figure 11. Bus Write Timing Characteristics
(Write Information into PIA)
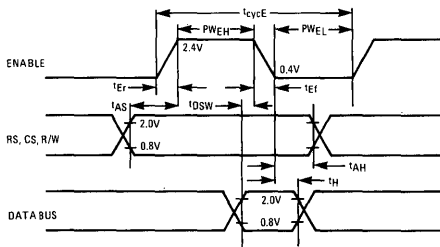
877269

Figure 12. Peripheral Data Hold Time
(Read Mode)
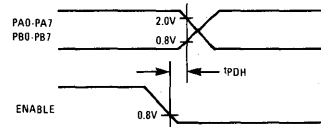
877270

Figure 13. Peripheral Control Output Pulse Width
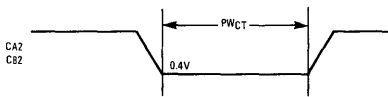
877271

Figure 14. Interrupt Pulse Width and IRQ Response
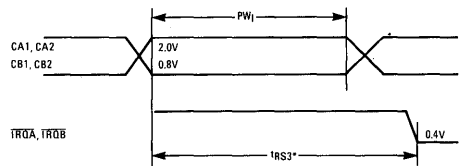
*Assumes Interrupt Enable Bits are set.

877272

Figure 15. Bus Timing Test Loads

LOAD B
(IRQ ONLY)

LOAD A
(D0-D7)
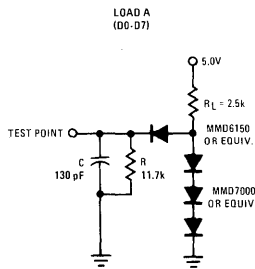
LOAD C
(CMOS LOAD)
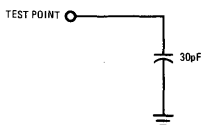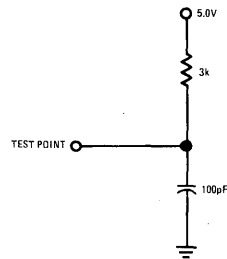
LOAD D
(PA0-PA7, PB0-PB7, CA2, CB2)
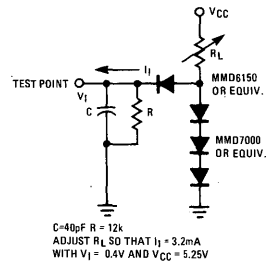
C=40pF R = 12k
ADJUST R$_L$ SO THAT I$_1$ = 3.2mA
WITH V$_1$ = 0.4V AND V$_{CC}$ = 5.25V

877257

Interface Description

MPU/PIA Interface

Pin	Label	Function
(33)	D0	**Bidirectional Data** — The bidirectional data lines (D0-D7) allow the transfer of data
(32)	D1	between the MPU and the PIA. The data bus output drivers are three-state devices that
(31)	D2	remain in the high-impedance (off) state except when the MPU performs a PIA read
(30)	D3	operation. The Read/Write line is in the Read (high) state when the PIA is selected for
(29)	D4	a Read operation.
(28)	D5	
(27)	D6	
(26)	D7	

(25)   E   **Enable** — The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the S6800 $\phi 2$ Clock.

The E pulse is used to condition the interrupt/control lines CA1, CA2, CB1 and CB2. At least one E pulse must occur from the inactive edge to the active edge of the input signal to set the interrupt flag, when the lines are used as inputs.

(21)   R/W   **Read/Write** — This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

(34) $\overline{\text{RESET}}$ **Reset** — The active low $\overline{\text{Reset}}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

(22)   CS0   **Chip Select** — These three input signals are used to select the PIA. CS0 and CS1 must
(24)   CS1   be high and $\overline{\text{CS2}}$ must be low for selection of the device. Data transfers are then per-
(23) $\overline{\text{CS2}}$ formed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse.

(36)   RS0   **PIA Register Select** — The two register select lines are used to select the various registers
(35)   RS1   inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The Register select lines should be stable for the duration of the E pulse while in the read or write cycle.

| (38) | $\overline{IRQA}$ | **Interrupt Request** — The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to |
| (37) | $\overline{IRQB}$ | interrupt the MPU either directly or through interrupt priority circuitry. These lines |

are "open source" (no load device on the chip) and are capable of sinking a current of 1.6mA from an external source. This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that will cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also, four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU is accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The Interrupt Flag is cleared (zeroed) as a result of an MPU Read Peripheral Data Operation.

PIA/Peripheral Interface

Pin	Label	Function
(2)	PA0	**Section A Peripheral Data** — Each of the peripheral data lines can be programmed to
(3)	PA1	act as an input or output. This is accomplished by setting a "1" in the corresponding
(4)	PA2	Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of
(5)	PA3	the Data Direction Register causes the corresponding peripheral data line to act as an
(6)	PA4	input. During an MPU Read Peripheral Data Operation, the data on peripheral lines
(7)	PA5	programmed to act as inputs appears directly on the corresponding MPU Data Bus
(8)	PA6	lines. In the input mode the internal pullup resistor on these lines represents a maxi-
(9)	PA7	mum of one standard TTL load.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low." Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volts for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

(10)	PB0	**Section B Peripheral Data** — The peripheral data lines in the B Section of the PIA can
(11)	PB1	be programmed to act as either inputs or outputs in a similar manner to PA0-PA7.
(12)	PB2	However, the output buffers driving these lines differ from those driving lines PA0-PA7.
(13)	PB3	They have three-state capability, allowing them to enter a high impedance state when
(14)	PB4	the peripheral data line is used as an input. In addition, data on the peripheral data
(15)	PB5	lines PB0-PB7 will be read properly from those lines programmed as outputs even if
(16)	PB6	the voltages are below 2.0 volts for a "high." As outputs, these lines are compatible
(17)	PB7	with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts

to directly drive the base of a transistor switch.

(40)   CA1   **Interrupt Input** — Peripheral Input lines CA1 and CB1 are input-only lines that set the
(18)   CB1   interrupt flags of the control registers. The active transition for these signals is also pro-
grammed by the two control registers.

(39)   CA2   **Peripheral Control** — The peripheral control line CA2 can be programmed to act as an
interrupt input or as a peripheral control output. As an output, this line is compatible
with standard TTL; as an input the internal pullup resistor on this line represents one
standard TTL load. The function of this signal line is programmed with Control
Register A.

(19)   CB2   **Peripheral Control** — Peripheral Control line CB2 may also be programmed to act as an
interrupt input or peripheral control output. As an input, this line has high input im-
pedance and is compatible with standard TTL. As an output, it is compatible with stan-
dard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly
drive the base of a transistor switch. This line is programmed by Control Register B.

(1)   GND   **Ground**

(20) V_{CC} +5Volts ±5%

S6800

Application Information

Initialization

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

Register Addressing

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

Table 1. Internal Addressing

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

Data Direction Registers (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. All Data Direction Register bits set at "0" configure the corresponding peripheral data line as an input; all "1's" result in an output.

Control Registers (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines, CA1, CA2, CB1 and CB2. In addition, they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

Table 2. Control Word Format

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	

	7	6	5	4	3	2	1	0
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

Data Direction Access Control Bit (CRA-2 and CRB-2) — Bit 2 in each Control Register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1 and CRB-1) — The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4 and CRB-5) — Bits 3, 4 and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CBR-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

Interrupt Flags (CRA-6, CRA-7, CRB-6 and CRB-7) — The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Status lines when those lines are programmed to be interrupt inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

Table 3. Control of Interrupt Inputs CA1 and CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high

Notes:
1. ↑ indicates positive transition (low to high).
2. ↓ indicates negative transition (high to low).
3. The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.
4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs on the positive transition of CRA-0 (CRB-0).

Table 4. Control of CA2 and CB2 as Interrupt Inputs
CRA-5 (CRB-5) is Low

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled — $\overline{IRQ}$ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled — $\overline{IRQ}$ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high

Notes:
1. ↑ indicates positive transition (low to high).
2. ↓ indicates negative transition (high to low).
3. The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.
4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs on the positive transition of CRA-3 (CRB-3).

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Table 5. Control of CA2 as an Output
       CRA-5 is High

CRA-5	CRA-4	CRA-3	CA2	
			Cleared	Set
1	0	0	Low on negative transition of E after an MPU Read "A" Data operation.	High on an active transition of the CA1 signal.
1	0	1	Low immediately after an MPU Read "A" Data operation.	High on the negative edge of the next "E" pulse.
1	1	0	Low when CRA-3 goes low as a result of an MPU Write in Control Register "A."	Always low as long as CRA-3 is low.
1	1	1	Always high as long as CRA-3 is high.	High when CRA-3 goes high as a result of a Write in Control Register "A."

Table 6. Control of CB2 as an Output
       CRB-5 is High

CRB-5	CRB-4	CRB-3	CB2	
			Cleared	Set
1	0	0	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal.
1	0	1	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High on the positive transition of the next "E" pulse.
1	1	0	Low when CRB-3 goes low as a result of an MPU Write in Control Register "B."	Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register "B" that changes CRB-3 to "one."
1	1	1	Always high as long as CRB-3 is high Will be cleared when an MPU Write Control Register "B" results in clearing CRB-3 to "zero."	High when CRB-3 goes high as a result of an MPU write into Control Register "B."

Basic System Configuration

The Microprocessing Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system (Figure 16). Such a system can easily be adapted for a number of small scale applications by simply changing the content of the ROM.

Two-Phase Clock Circuitry and Timing — The MPU requires a two-phase non-overlapping clock which has a frequency range as high as 1MHz. In addition to the two phases, this circuit should also generate an enable Signal E, and its complement E, to enable ROMs, RAMs, PIAs and ACIAs. This Enable signal and its complement are obtained by ANDing $\phi 2$ and VMA (Valid Memory Address).

Chip Selection and Addressing — The minimum system configuration permits direct selection of the ROM,

RAM, ACIA and PIA without the use of special TTL select logic. This is accomplished by simply wiring the address lines A13, A14 to the Enable or chip select lines on the memories and PIA. This permits the devices to be addressed as follows:

Device	A14	A13	Hex Addresses
RAM	0	0	0000-007F
PIA	0	1	2004-2007 (Registers)
ROM	1	1	6000-63FF

Other addressing schemes can be utilized which use any combination of two of the lines A10 through A14 for chip selection.

Peripheral Control — All control and timing for the peripherals that are connected to the PIA is accomplished by software routines under the control of the MPU.

Figure 16. Minimum System Implementation

877258
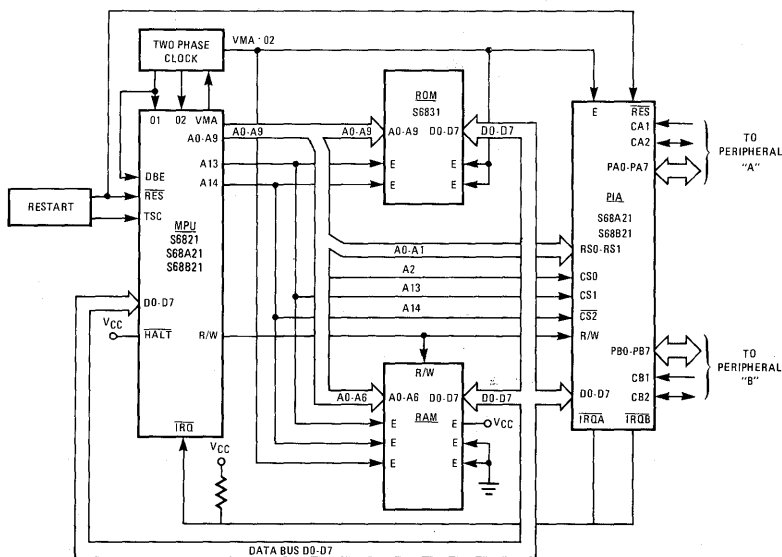
Expanded Block Diagram

877248

3.52

A M I ®
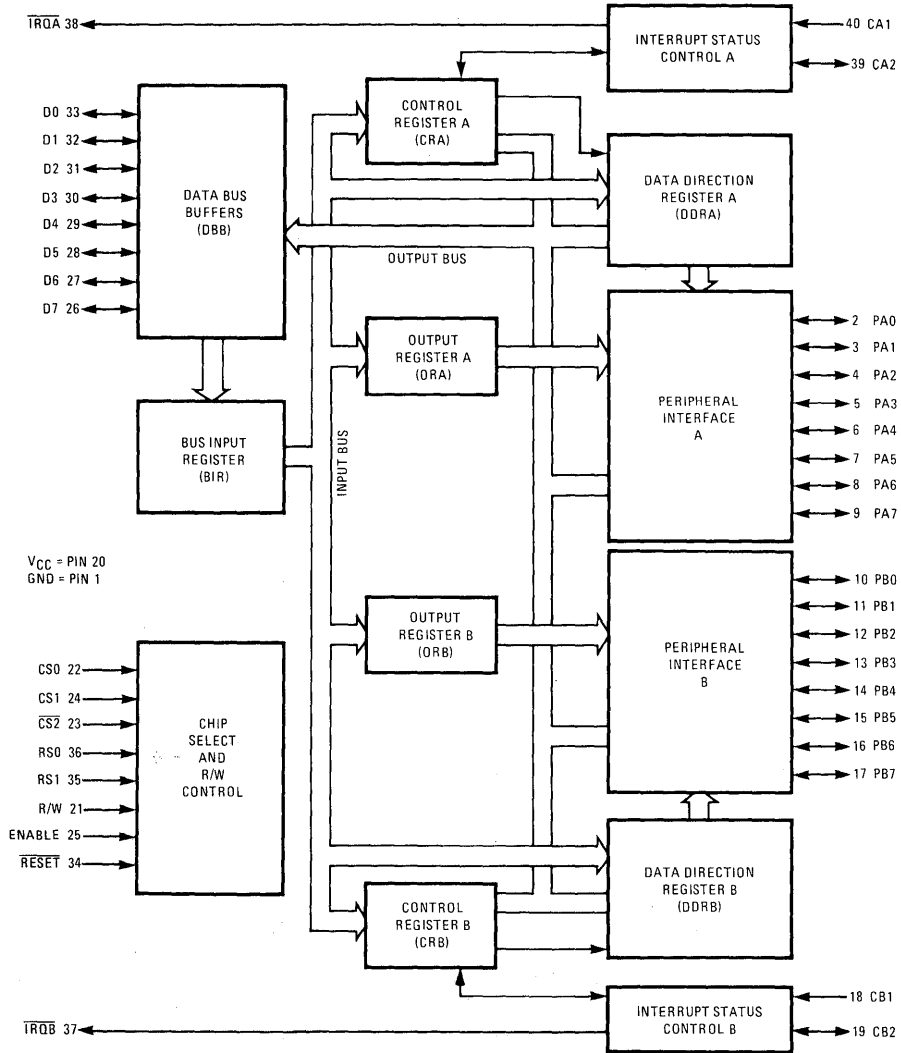
PROGRAMMABLE TIMER

Features

☐ Operates from a Single 5 Volt Power Supply
☐ Fully TTL Compatible
☐ Single System Clock Required (Enable)
☐ Selectable Prescaler on Timer 3 Capable of a 4MHz Input
☐ Programmable Interrupts ($\overline{IRQ}$) Output to MPU
☐ Readable Down Counter Indicates Counts to Go to Time-Out
☐ Selectable Gating for Frequency or Pulse-Width Comparison
☐ $\overline{RESET}$ Input
☐ Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized
☐ Three Maskable Outputs

General Description

The S6840 is a programmable subsystem component of the S6800 family designed to provide variable system time intervals.

The S6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The S6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

S6800
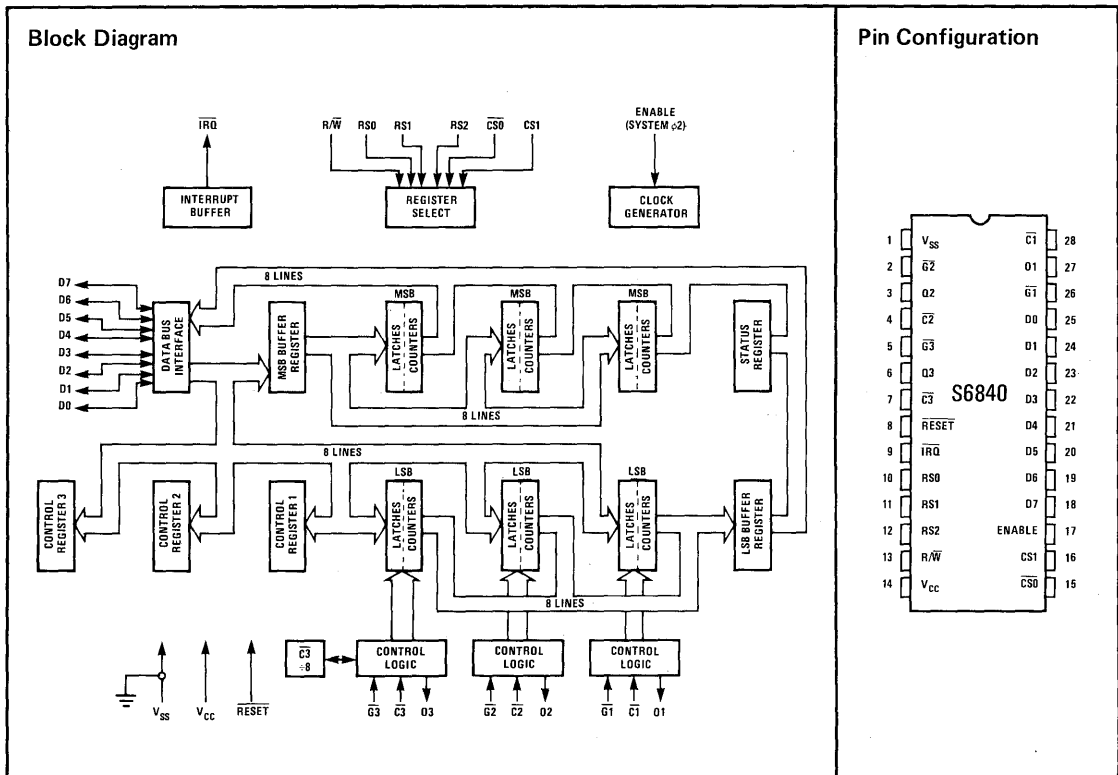
Block Diagram

Pin Configuration

Absolute Maximum Ratings

Supply Voltage V_{CC}	-0.3 to $+7.0$V
Input Voltage V_{IN}	-0.3 to $+7.0$V
Operating Temperature Range T_A	$0°$C to $+70°$C
Storage Temperature Range T_{stg}	$-55°$C to $+150°$C
Thermal Resistance θ_{JA}	$82.5°$C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics ($V_{CC} = 5.0$V $\pm$ 5%, $V_{SS} = 0$, $T_A = 0°$C to $+70°$C unless otherwise noted)

Symbol	Characteristic		Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage		$V_{SS} +2.0$		V_{CC}	V	
V_{IL}	Input Low Voltage		$V_{SS} -0.3$		$V_{SS} +0.8$	μA	
I_{IN}	Input Leakage Current			1.0	2.5	μA	V_{IN}=0 to 5.25V
I_{TSI}	Three-State (Off State) Input Current	D0 — D7		2.0	10	μA	V_{IN} = 0.4 to 2.4V
V_{OH}	Output High Voltage					V	
		D0 — D7	$V_{SS} +2.4$				$I_{LOAD} = -205\mu$A
		Other Outputs	$V_{SS} +2.4$				$I_{LOAD} = -200\mu$A
V_{OL}	Output Low Voltage					V	
		D0 — D7			$V_{SS} +0.4$		$I_{LOAD} = 1.6$mA
		01 — 03, $\overline{IRQ}$			$V_{SS} +0.4$		$I_{LOAD} = 3.2$mA
I_{LOH}	Output Leakage Current (Off State)	$\overline{IRQ}$		1.0	10	μA	$V_{OH} = 2.4$V
P_D	Power Dissipation				550	mW	
C_{IN}	Input Capacitance					pF	V_{IN}=0, T_A=25°C, f = 1.0MHz
		D0 — D7			12.5		
		All Others			7.5		
C_{OUT}	Output Capacitance					pF	
		$\overline{IRQ}$			5.0		V_{IN}=0, T_A=25°C, f = 1.0MHz
		01, 02, 03			10		

Bus Timing Characteristics
Read (See Figures 1 and 7)

Symbol	Characteristic	Min.	Max.	Unit	Condition
t_{CYCE}	Enable Cycle Time	1.0	1.0	μs	
PW_{EH}	Enable Pulse Width, High	0.45	4.5	μs	
PW_{EL}	Enable Pulse Width, Low	0.43		μs	
t_{AS}	Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	160		ns	
t_{DDR}	Data Delay Time		320	ns	
t_H	Data Hold Time	10		ns	
t_{AH}	Address Hold Time	10		ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input		25	ns	

Bus Timing Characteristics (Continued)
Write (See Figures 2 and 7)

Symbol	Characteristic	Min.	Max.	Unit	Condition
t_{CYCE}	Enable Cycle Time	1.0	10	μs	
PW_{EH}	Enable Pulse Width, High	0.45	4.5	μs	
PW_{EL}	Enable Pulse Width, Low	0.43		μs	
t_{AS}	Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	160		ns	
t_{DSW}	Data Setup Time	195		ns	
t_H	Data Hold Time	10		ns	
t_{AH}	Address Hold Time	10		ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input		25	ns	

AC Operating Characteristics

Symbol	Characteristic	Min.	Max.	Unit	Condition
t_r, t_f	Input Rise and Fall Times $\overline{C}, \overline{G}$ and $\overline{Reset}$		1.0*	μs	
PW_L	Input Pulse Width Low (Figure 3) $\overline{C}, \overline{G}$ and $\overline{Reset}$	$t_{CYCE} + t_{su} + t_{hd}$		ns	
PW_H	Input Pulse Width High (Figure 4) $\overline{C}, \overline{G}$	$t_{CYCE} + t_{su} + t_{hd}$		ns	
t_{su}	Input Setup Time (Figure 5) (Synchronous Mode) $\overline{C}, \overline{G}$ and $\overline{Reset}$ $\overline{C3}$ ($\div 8$ Prescaler Mode only)	200		ns	
t_{hd}	Input Hold Time (Figure 5) (Synchronous Mode) $\overline{C}, \overline{G}$ and $\overline{Reset}$ $\overline{C3}$ ($\div 8$ Prescaler Mode only)	50		ns	
t_{co}	Load A TTL		700	ns	$V_{OH}=2.4V$
t_{cm}	Load C MOS		450	ns	$V_{OH}=2.4V$
t_{cmos}	Load C CMOS		2.0	μs	$V_{OH}=0.7V_{DD}$
t_{IR}	Interrupt Release Time		1.6	μs	

*t_r and $t_f \leqslant 1$ x Pulse Width or 1.0μs, whichever is smaller.

Figure 1. Bus Read Timing Characteristics
(Read Information from PTM)
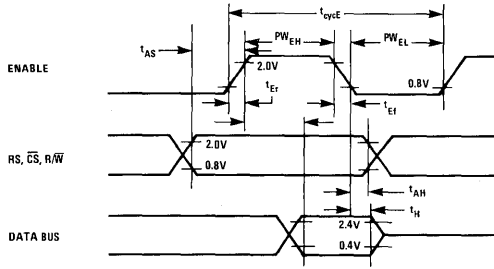
Figure 2. Bus Write Timing Characteristics
(Write Information into PTM)
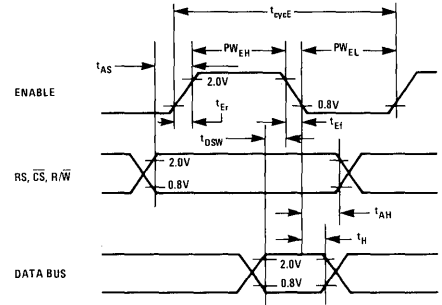
Figure 3. Input Pulse Width Low
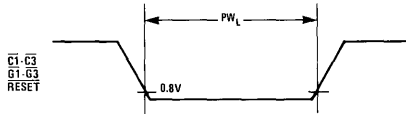
Figure 4. Input Pulse Width High
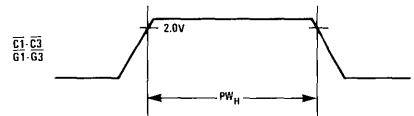
Figure 5. Input Setup and Hold Times
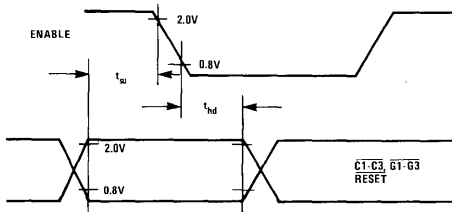
Figure 6. Output Delay
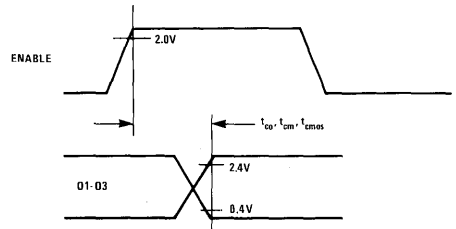
Figure 7. $\overline{\text{IRQ}}$ Release Time
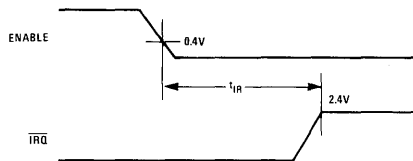
Figure 8. Bus Timing Test Loads
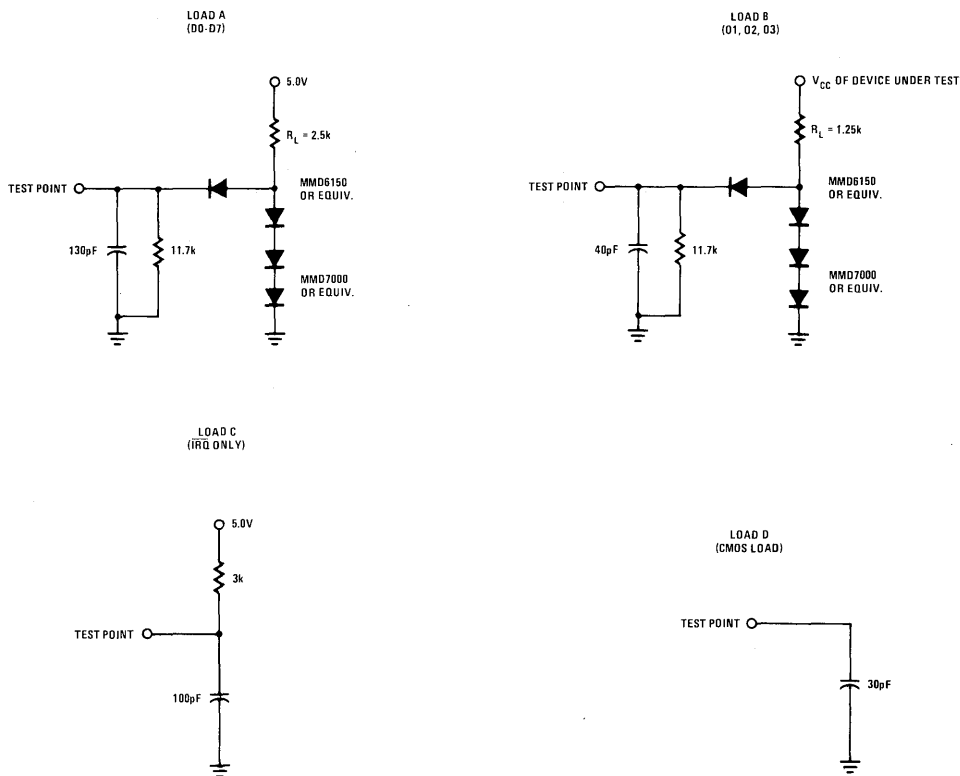
Device Operation

The three timers in the S6840 may be independently programmed to operate in modes which fit a wide variety of applications. The device is fully bus compatible with S6800 systems and is accessed by load and store operations from the MPU in much the same manner as a memory device. In a typical application, a Timer will be loaded by first storing two bytes of data into an associated Counter Latch. This data is then transferred into the counter via a Counter Initialization cycle. The counter decrements on each subsequent clock period which may be an external clock or Enable (System $\phi 2$) until one of several predetermined conditions causes it to halt or recycle. The timers are thus programmable, cyclic in nature, controllable by external inputs or the MPU program, and accessible by the MPU at any time.

Bus Interface

The Programmable Timer Module (PTM) interfaces to the S6800 Bus with an eight-bit bidirectional data bus, two Chip Select lines, a Read/Write line, an Enable (System $\phi 2$) line, an Interrupt Request line, an external Reset line, and three Register Select lines. These signals, in conjunction with the S6800 VMA output, permit the MPU to control the PTM. VMA should be utilized in conjunction with an MPU address line into a Chip Select of the PTM.

Bidirectional Data (D0 — D7) — The bidirectional data lines (D0 — D7) allow the transfer of data between the MPU and PTM. The data bus output drivers are three-state devices which remain in the high-impedance (off) state except when the MPU performs a PTM read operation (Read/Write and Enable lines high and PTM Chip Selects activated).

Chip Select (CS0, CS1) — These two signals are used to activate the Data Bus interface and allow transfer of data from the PTM. With CS0=0 and CS1=1, the device is selected and data transfer will occur.

Read/Write (R/W) — This signal is generated by the MPU to control the direction of data transfer on the Data Bus. With the PTM selected, a low state on the PTM R/W line enables the input buffers and data is transferred from the MPU to the PTM on the trailing edge of the Enable (System $\phi 2$) signal. Alternately, (under the same conditions) R/W = 1 and Enable high allows data in the PTM to be read by the MPU.

Enable (System $\phi 2$) — This signal synchronizes data transfer between the MPU and the PTM. It also performs an equivalent synchronization function on the external clock, reset, and gate inputs of the PTM.

Interrupt Request (IRQ) — The active low Interrupt Request signal is normally tied directly (or through priority interrupt circuitry) to the IRQ input of the MPU. This is an "open drain" output (no load device on the chip) which permits other similar interrupt request lines to be tied together in a wire-OR configuration.

The IRQ line is activated if, and only if, the Composite Interrupt Flag (Bit 7 of the Internal Status Register) is asserted. The conditions under which the IRQ line is activated are discussed in conjunction with the Status Register.

External Reset — A low level at this input is clocked into the PTM by the Enable (System $\phi 2$) input. Two Enable pulses are required to synchronize and process the signal. The PTM then recognizes the active "low" or inactive "high" on the third Enable pulse. If the Reset signal is asynchronous, an additional Enable period is required if setup times are not met. The Reset input must be stable High/Low for the minimum time stated in the AC Operating Characteristics.

Recognition of a low level at this input by the PTM causes the following action to occur:

a. All counter latches are preset to their maximal count values.

b. All Control Register bits are cleared with the exception of CR10 (internal reset bit) which is set.

c. All counters are preset to the contents of the latches.

d. All counter outputs are reset and all counter clocks are disabled.

e. All Status Register bits (interrupt flags) are cleared.

Register Select Lines (RS0, RS1, RS2) — These inputs are used in conjunction with the $R/\overline{W}$ line to select the internal registers, counters and latches as shown in Table 1.

It has been previously stated that the PTM is accessed via MPU Load and Store operations in much the same manner as a memory device. The instructions available with the S6800 family of MPUs which perform operations directly on memory should not be used when the PTM is accessed. These instructions actually fetch a byte from memory, perform an operation, then restore it to the same address location. Since the PTM used the $R/\overline{W}$ line as an additional register select input, the modified data may not be restored to the same register if these instructions are used.

Table 1. Register Selection

REGISTER SELECT INPUTS			OPERATIONS	
RS2	RS1	RS0	$R/\overline{W} = 0$	$R/\overline{W} = 1$
0	0	0	CR20 = 0　　WRITE CONTROL REGISTER #3 CR20 = 1　　WRITE CONTROL REGISTER #1	NO OPERATION
0	0	1	WRITE CONTROL REGISTER #2	READ STATUS REGISTER
0	1	0	WRITE MSB BUFFER REGISTER	READ TIMER #1 COUNTER
0	1	1	WRITE TIMER #1 LATCHES	READ LSB BUFFER REGISTER
1	0	0	WRITE MSB BUFFER REGISTER	READ TIMER #2 COUNTER
1	0	1	WRITE TIMER #2 LATCHES	READ LSB BUFFER REGISTER
1	1	0	WRITE MSB BUFFER REGISTER	READ TIMER #3 COUNTER
1	1	1	WRITE TIMER #3 LATCHES	READ LSB BUFFER REGISTER

Control Register

Three Write-Only registers in the S6840 are used to modify timer operation to suit a variety of applications. Control Register #2 has a unique address space (RS0 = 1, RS1 = 0, RS2 = 0) and therefore may be written into at any time. The remaining Control Registers (#1 and #3) share the Address Space selected by a logic zero on all Register Select inputs. The least significant bit of Control Register #2 (CR20) is used as an additional addressing bit for Control Registers #1 and #3. Thus, with all Register Selects and R/$\overline{\text{W}}$ inputs at logic zero, Control Register #1 will be written into if CR20 is a logic one. Under the same conditions, Control Register #3 will be written into if CR20 is a logic zero. Control Register #3 can also be written into after a $\overline{\text{Reset}}$ low condition has occurred, since all control register bits (except CR10) are cleared. Therefore, one may write in the sequence CR3, CR2, CR1.

The least significant bit of Control Register #1 is used as an Internal Reset bit. When this bit is a logic zero, all timers are allowed to operate in the modes prescribed by the remaining bits of the control

Table 2. Control Register Bits

CR10 INTERNAL RESET BIT		CR20 CONTROL REGISTER ADDRESS BIT		CR30 TIMER #3 CLOCK CONTROL	
0	ALL TIMERS ALLOWED TO OPERATE	0	CR#3 MAY BE WRITTEN	0	T3 $\overline{\text{CLOCK}}$ IS NOT PRESCALED
1	ALL TIMERS HELD IN PRESET STATE	1	CR#1 MAY BE WRITTEN	1	T3 $\overline{\text{CLOCK}}$ IS PRESCALED BY ÷ 8
CRX1*		TIMER #X $\overline{\text{CLOCK}}$ SOURCE			
0		TX USES EXTERNAL CLOCK SOURCE ON $\overline{\text{CX}}$ INPUT			
1		TX USES ENABLE CLOCK			
CRX2		TIMER #X COUNTING MODE CONTROL			
0		TX CONFIGURED FOR NORMAL (16-BIT) COUNTING MODE			
1		TX CONFIGURED FOR DUAL 8-BIT COUNTING MODE			
CRX3 CRX4 CRX5		TIMER #X COUNTER MODE AND INTERRUPT CONTROL (See Table 3)			
CRX6		TIMER #X INTERRUPT ENABLE			
0		INTERRUPT FLAG MASKED ON $\overline{\text{IRQ}}$			
1		INTERRUPT FLAG ENABLED TO $\overline{\text{IRQ}}$			
CRX7		TIMER #X COUNTER OUTPUT ENABLE			
0		TX OUTPUT MASKED ON OUTPUT OX			
1		TX OUTPUT ENABLED ON OUTPUT OX			

*Control Register for Timer 1, 2 or 3, Bit 1.

Control Register (Continued)

registers. Writing a "one" into CR10 causes all counters to be preset with the contents of the corresponding counter latches, all counter clocks to be disabled, and the timer outputs and interrupt flags (Status Register) to be reset. Counter Latches and Control Registers are undisturbed by an Internal Reset and may be written into regardless of the state of CR10.

The least significant bit of Control Register # 3 is used as a selector for a ÷ 8 prescaler which is available with Timer # 3 only. The prescaler, if selected, is effectively placed between the clock input circuitry and the input to Counter # 3. It can therefore be used with either the internal clock (Enable) or an external clock source.

The functions depicted in the foregoing discussions are tabulated on the first row in Table 2 for ease of reference.

Control Register Bits CR10, CR20, and CR30 are unique in that each selects a different function. The remaining bits (1 through 7) of each Control Register select common functions, with a particular Control Register affecting only its corresponding timer. For example, Bit 1 of Control Register # 1 (CR11) selects whether an internal or external clock source is to be used with Timer # 1. Similarly, CR21 selects the clock source for Timer # 2, and CR31 performs this function for Timer # 3. The function of each bit of Control Register "X" can therefore be defined as shown in the remaining section of Table 2.

Control Register Bit 2 selects whether the binary information contained in the Counter Latches (and subsequently loaded into the Counter) is to be treated as a single 16-bit word or two 8-bit bytes. In the single 16-bit Counter Mode (CRX2 = 0) the counter will decrement to zero after N+1 enabled ($\overline{G}$ = 0) clock periods, where N is defined as the 16-bit number in the Counter Latches. With CRX2 = 1, a similar Time Out will occur after (L+1) • (M+1) enabled clock periods, where L and M respectively, refer to the LSB and MSB bytes in the Counter Latches.

Control Register Bits 3, 4, and 5 are explained in detail in the Timer Operating Mode section. Bit 6 is an interrupt mask bit which will be explained more fully in conjunction with the Status Register, and bit 7 is used to enable the corresponding Timer Output.

Status Register/Interrupt Flags

The S6840 has an internal Read-Only Status Register which contains four Interrupt Flags. (The remaining four bits of the register are not used, and default to zeros when being read.) Bits 0, 1, and 2 are assigned to Timers 1, 2, and 3, respectively, as individual flag bits, while Bit 7 is a Composite Interrupt Flag. This flag bit will be asserted if any of the individual flag bits is set while Bit 6 of the corresponding Control Register is at a logic one. The conditions for asserting the Composite Interrupt Flag bit can therefore be expressed as:

$$INT = I1 \cdot CR16 + I2 \cdot CR26 + I3 \cdot CR36$$

where INT = Composite Interrupt Flag (Bit 7)

$$I1 = \text{Timer \#1 Interrupt Flag (Bit 0)}$$
$$I2 = \text{Timer \#2 Interrupt Flag (Bit 1)}$$
$$I3 = \text{Timer \#3 Interrupt Flag (Bit 2)}$$

An interrupt flag is cleared by a Timer Reset condition, i.e., External $\overline{Reset}$ = 0 or Internal Reset Bit (CR10) = 1. It will also be cleared by a Read Timer Counter Command provided that the Status Register has previously been read while the interrupt flag was set. This condition on the Read Status Register — Read Timer Counter (RS — RT) sequence is designed to prevent missing interrupts which might occur after the status register is read, but prior to reading the Timer Counter.

An individual Interrupt Flag is also cleared by a Write Timer Latches (W) command or a Counter Initialization (CI) sequence, provided that W or CI affects the Timer corresponding to the individual Interrupt Flag.

Counter Latch Initialization

Each of the three independent timers consists of a 16-bit addressable counter and 16 bits of addressable latches. The counters are preset to the binary numbers stored in the latches. Counter initialization results in the transfer of the latch contents to the counter. See notes in Table 4 regarding the binary number N, L, or M placed into the Latches and their relationship to the output waveforms and counter Time-Outs.

Counter Latch Initialization (Continued)

Since the PTM data bus is 8-bits wide and the counters are 16-bits wide, a temporary register (MSB Buffer Register) is provided. This "write only" register is for the Most Significant Byte of the desired latch data. Three addresses are provided for the MSB Buffer Register (as indicated in Table 1), but they all lead to the same Buffer. Data from the MSB Buffer will automatically be transferred into the Most Significant Byte of Timer # X when a Write Timer # X Latches Command is performed. So it can be seen that the S6840 has been designed to allow transfer of two bytes of data into the counter latches provided that the MSB is transferred first.

In many applications, the source of the data will be an S6800 MPU. It should be noted that the 16-bit store operations of the S6800 family microprocessors (STS and STX) transfer data in the order required by the PTM. A Store Index Register Instruction, for example, results in the MSB of the X register being transferred to the selected address, then the LSB of the X register being written into the next higher location. Thus, either the index register or stack pointer may be transferred directly into a selected counter latch with a single instruction.

A logic zero at the $\overline{\text{Reset}}$ input also initializes the counter latches. In this case, all latches will assume a maximum count of $65,536_{10}$. It is important to note that an Internal Reset (Bit zero of Control Register 1 Set) has no effect on the counter latches.

Counter Initialization

Counter Initialization is defined as the transfer of data from the latches to the counter with subsequent clearing of the Individual Interrupt Flag associated with the counter. Counter Initialization always occurs when a reset condition ($\overline{\text{Reset}}$ = 0 or CR10 = 1) is recognized. It can also occur — depending on Timer Mode — with a Write Timer Latches command or recognition of a negative transition of the $\overline{\text{Gate}}$ input.

Counter recycling or re-initialization occurs when a negative transition of the clock input is recognized after the counter has reached an all-zero state. In this case, data is transferred from the Latches to the Counter.

Asynchronous Input/Output Lines

Each of the three timers within the PTM has external

clock and gate inputs as well as a counter output line. The inputs are high impedance, TTL compatible lines and outputs are capable of driving two standard TTL loads.

$\overline{\text{Clock}}$ Inputs ($\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{C3}}$) — Input pins $\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{C3}}$ will accept asynchronous TTL voltage level signals to decrement Timers 1, 2, and 3, respectively. The high and low levels of the external clocks must each be stable for at least one system clock period plus the sum of the setup and hold times for the inputs. The asynchronous clock rate can vary from dc to the limit imposed by Enable (System ϕ 2) Setup, and Hold time.

The external clock inputs are clocked in by Enable (System ϕ 2) pulses. Three Enable periods are used to synchronize and process the external clock. The fourth Enable pulse decrements the internal counter. This does not affect the input frequency, it merely creates a delay between a clock input transition and internal recognition of that transition by the PTM. All references to $\overline{\text{C}}$ inputs in this document relate to internal recognition of the input transition. Note that a clock high or low level which does not meet setup and hold time specifications may require an additional Enable pulse for recognition. When observing recurring events, a lack of synchronization will result in "jitter" being observed on the output of the PTM when using asynchronous clocks and gate input signals. There are two types of jitter. "System jitter" is the result of the input signals being out of synchronization with the Enable (System ϕ 2), permitting signals with marginal setup and hold time to be recognized by either the bit time nearest the input transition or the subsequent bit time.
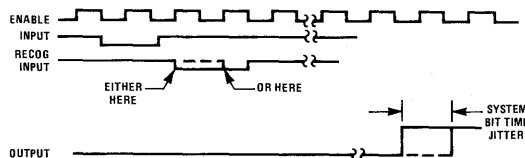
"Input jitter" can be as great as the time between input signal negative going transitions plus the system jitter, if the first transition is recognized during one system cycle, and not recognized the next cycle, or vice versa.

Asynchronous Input/Output Lines (Continued)


```
ENABLE ‾|_|‾|_|‾|_|‾|_|‾|_|‾|_|‾|_|‾|_|‾|_|‾|_
INPUT     t₀ INPUT        OR THIS ONE
C3 ‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾
         PTM          |          |
         RECOGNIZES  t₀  PTM  OR  t₀  PTM
         THIS EDGE
```
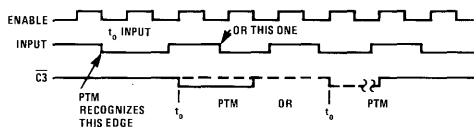
External clock input $\overline{C3}$ represents a special case when Timer #3 is programmed to utilize its optional ÷ 8 prescaler mode. The maximum input frequency and allowable duty cycles for this case are specified under the AC Operating Characteristics. The output of the ÷ 8 prescaler is treated in the same manner as the previously discussed clock inputs. That is, it is clocked into the counter by Enable pulses, is recognized on the fourth Enable pulse (provided setup and hold time requirements are met), and must produce an output pulse at least as wide as the sum of an Enable period, setup, and hold times.

$\overline{Gate}$ Inputs ($\overline{G1}$, $\overline{G2}$, $\overline{G3}$) — Input pins $\overline{G1}$, $\overline{G2}$, and $\overline{G3}$ accept asynchronous TTL-compatible signals which are used as triggers or clock gating functions to Timers 1, 2, and 3, respectively. The gating inputs are clocked into the PTM by the Enable (System $\phi2$) signal in the same manner as the previously discussed clock inputs. That is, a $\overline{Gate}$ transition is recognized by the PTM on the fourth Enable pulse (provided setup and hold time requirements are met), and the high or low levels of the $\overline{Gate}$ input must be stable for at least one system clock period plus the sum of setup and hold times. All references to $\overline{G}$ transition in this document relate to internal recognition of the input transition.

The $\overline{Gate}$ inputs of all timers directly affect the internal 16-bit counter. The operation of $\overline{G3}$ is therefore independent of the ÷ 8 prescaler selection.

Timer Outputs (O1, O2, O3) — Timer outputs O1, O2, and O3 are capable of driving up to two TTL loads and produce a defined output waveform for either Continuous or Single-Shot Timer modes. Output waveform definition is accomplished by selecting either Single 16-bit or Dual 8-bit operating modes. The single 16-bit mode will produce a square-wave output in the continuous timer mode and will produce a single pulse in the Single-Shot Timer mode. The Dual 8-bit mode will produce a variable duty cycle pulse in both the continuous and single shot Timer modes. One bit of each Control Register (CRX7) is used to enable the corresponding output. If this bit is cleared, the output will remain low

(V_{OL}) regardless of the operating mode.

The Continuous and Single-Shot Timer Modes are the only ones for which output response is defined. Signals appear at the outputs (unless CRX7 = 0) during Frequency and Pulse Width comparison modes, but the actual waveform is not predictable in typical applications.

Timer Operating Modes

The S6840 has been designed to operate effectively in a wide variety of applications. This is accomplished by using three bits of each control register (CRX3, CRX4, and CRX5) to define different operating modes of the Timers. These modes are outlined in Table 3.

Table 3. Operating Modes

CONTROL REGISTER			TIMER OPERATING MODE
CRX3	CRX4	CRX5	
0	*	0	CONTINUOUS
0	*	1	SINGLE-SHOT
1	0	*	FREQUENCY COMPARISON
1	1	*	PULSE WIDTH COMPARISON

*Defines Additional Timer Functions

In addition to the four timer modes in Table 3, the remaining control register bit is used to modify counter initialization and enabling or interrupt conditions.

Continuous Operating Mode (Table 4) — Any of the timers in the PTM may be programmed to operate in a continuous mode by writing zeroes into bits 3 and 5 of the corresponding control register. Assuming that the timer output is enabled (CRX7 = 1), either a square wave or a variable duty cycle waveform will be generated at the Timer Output, OX. The type of output is selected via Control Register Bit 2.

Either a Timer Reset (CR10 = 1 or External $\overline{Reset}$ = 0) condition or internal recognition of a negative transition of the $\overline{Gate}$ input results in Counter Intialization. A Write Timer Latches command can be selected as a Counter Initialization signal by clearing CRX4.

In the dual 8-bit mode (CRX2 = 1) [Refer to the example in Figure 10] the MSB decrements once for every full countdown of the LSB + 1. When the LSB = 0, the MSB is unchanged; on the next clock pulse the LSB is reset to the count in the LSB Latches and
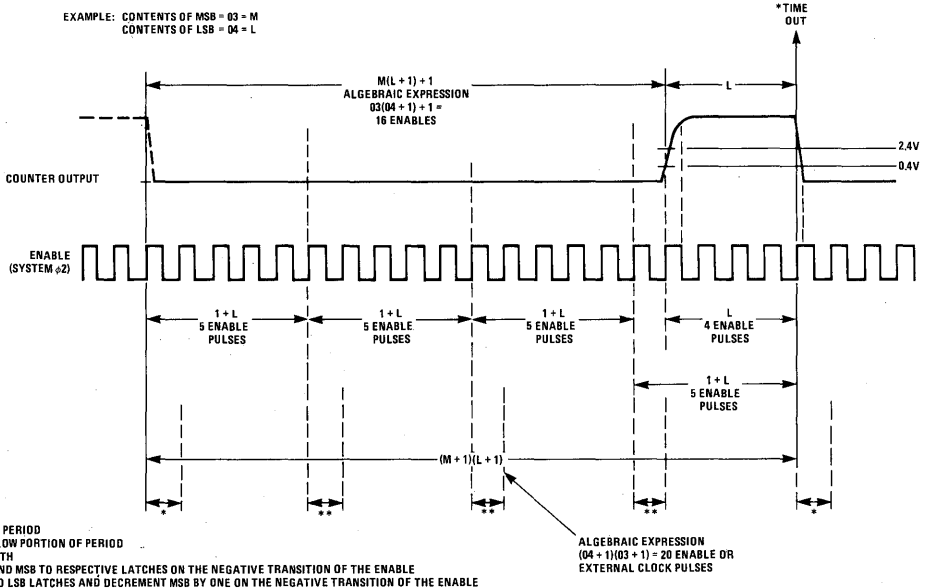
Table 4. Continuous Operating Modes

**CONTINUOUS MODE
(CRX3 = 0, CRX5 = 0)**

CONTROL REGISTER		INITIALIZATION/OUTPUT WAVEFORMS	
CRX2	CRX4	COUNTER INITIALIZATION	*TIMER OUTPUT (OX) (CRX7 = 1)
0	0	$G\downarrow + W + R$	
0	1	$G\downarrow + R$	
1	0	$G\downarrow + W + R$	
1	1	$G\downarrow + R$	

$G\downarrow$ = NEGATIVE TRANSITION OF GATE INPUT.
W = WRITE TIMER LATCHES COMMAND.
R = TIMER RESET (CR10 = 1 OR EXTERNAL RESET = 0).
N = 16-BIT NUMBER IN COUNTER LATCH.
L = 8-BIT NUMBER IN LSB COUNTER LATCH.
M = 8-BIT NUMBER IN MSB COUNTER LATCH.
T = CLOCK INPUT NEGATIVE TRANSITIONS TO COUNTER.
t_0 = COUNTER INITIALIZATION CYCLE.
TO = COUNTER TIME OUT (ALL ZERO CONDITION).

*All time intervals shown above assume that the Gate (G) and Clock (C) signals are synchronized to enable (System $\phi2$) with the specified setup and hold time requirements.

Figure 9. Timer Output Waveform Example
(Continuous Dual 8-Bit Mode using Internal Enable)

EXAMPLE: CONTENTS OF MSB = 03 = M
CONTENTS OF LSB = 04 = L

*TIME OUT

M(L + 1) + 1
ALGEBRAIC EXPRESSION
03(04 + 1) + 1 =
16 ENABLES

L

2.4V
0.4V

COUNTER OUTPUT

ENABLE (SYSTEM $\phi2$)

1 + L
5 ENABLE PULSES

1 + L
5 ENABLE PULSES

1 + L
5 ENABLE PULSES

L
4 ENABLE PULSES

1 + L
5 ENABLE PULSES

(M + 1)(L + 1)

ALGEBRAIC EXPRESSION
(04 + 1)(03 + 1) = 20 ENABLE OR
EXTERNAL CLOCK PULSES

(M + 1)(L + 1) = PERIOD
M(L + 1) + 1 = LOW PORTION OF PERIOD
L = PULSE WIDTH
*PRESET LSB AND MSB TO RESPECTIVE LATCHES ON THE NEGATIVE TRANSITION OF THE ENABLE
**PRESET LSB TO LSB LATCHES AND DECREMENT MSB BY ONE ON THE NEGATIVE TRANSITION OF THE ENABLE

Timer Operating Modes (Continued)

the MSB is decremented by 1 (one). The output, if enabled, remains low during and after initialization and will remain low until the counter MSB is all zeroes. The output remains high until both the LSB and MSB of the counter are all zeroes. At the beginning of the next clock pulse the defined Time Out (TO) will occur and the output will go low. In the normal 16-bit mode the period of the output of the example in Figure 9 would span 1546 clock pulses as opposed to the 20 clock pulses using the Dual 8-bit mode.

The counter is enabled by an absence of a Timer Reset condition and a logic zero at the $\overline{\text{Gate}}$ input. The counter will then decrement on the first clock signal recognized during or after the counter initialization cycle. It continues to decrement on each clock signal so long as $\overline{\text{G}}$ remains low and no reset condition exists. A Counter Time Out (the first clock after all counter bits = 0) results in the Individual Interrupt Flag being set and re-initialization of the counter.

A special condition exists for the dual 8-bit mode (CRX2 = 1) if L = 0. In this case, the counter will revert to a mode similar to the single 16-bit mode, except Time Out occurs after M + 1 clock pulses. The output, if enabled, goes low during the Counter Initialization cycle and reverses state at each Time Out. The counter remains cyclical (is re-initialized at each Time Out) and the Individual Interrupt Flag is set when Time Out occurs. If M = L = 0, the internal counters do not change, but the output toggles at a rate of ½ the clock frequency.

The discussion of the Continuous Mode has assumed that the application requires an output signal. It should be noted that the Timer operates in the same manner with the output disabled (CRX7 = 0). A Read Timer Counter command is valid regardless of the state of CRX7.

Single-Shot Timer Mode — This mode is identical to the Continuous Mode with three exceptions. The first of these is obvious from the name — the output returns to a low level after the initial Time Out and remains low until another Counter Initialization cycle occurs. The waveforms available are shown in Table 5.

As indicated in Table 5, the internal counting mechanism remains cyclical in the Single-Shot Mode. Each Time Out of the counter results in the setting of an Individual Interrupt Flag and re-initialization of the counter.

The second major difference between the Single-Shot and Continuous modes is that the internal counter

enable is not dependent on the $\overline{\text{Gate}}$ input level remaining in the low state for the Single-Shot mode.

Another special condition is introduced in the Single-Shot mode. If L = M = 0 (Dual 8-bit) or N = 0 (Single 16-bit), the output goes low on the first clock received during or after Counter Initialization. The output remains low until the Operating Mode is changed or non-zero data is written into the Counter Latches. Time Outs continue to occur at the end of each clock period.

The three differences between Single-Shot and Continuous Timer Modes can be summarized as attributes of the Single-Shot mode:

1. Output is enabled for only one pulse until it is reinitialized.

2. Counter Enable is independent of $\overline{\text{Gate}}$.

3. L = M = 0 or N = 0 disables output.

Aside from these differences, the two modes are identical.

Time Interval Modes — The Time Interval Modes are provided for those applications which require more flexibility of interrupt generation and Counter Initialization. Individual Interrupt Flags are set in these modes as a function of both Counter Time Out and transitions of the $\overline{\text{Gate}}$ input. Counter Initialization is also affected by Interrupt Flag status.

The output signal is not defined in any of these modes, but the counter does operate in either Single 16-bit or Dual 8-bit modes as programmed by CRX2. Other features of the Time Interval Modes are outlined in Table 6.

Frequency Comparison or Period Measurement Mode (CRX3 = 1, CRX4 = 0) — The Frequency Comparison Mode with CRX5 = 1 is straightforward. If Time Out occurs prior to the first negative transition of the $\overline{\text{Gate}}$ input after a Counter Initialization cycle, an Individual Interrupt Flag is set. The counter is disabled, and a Counter Initialization cycle cannot begin until the interrupt flag is cleared and a negative transition on $\overline{\text{G}}$ is detected.

If CRX5 = 0, as shown in Table 6 and Table 7, an interrupt is generated if $\overline{\text{Gate}}$ input returns low prior to a Time Out. If Counter Time-Out occurs first, the counter is recycled and continues to decrement. A bit is set within the timer on the initial Time Out which precludes further individual interrupt generation until a new Counter Initialization cycle has been completed. When this internal bit is set, a negative

Timer Operating Modes (Continued)

transition of the $\overline{\text{Gate}}$ input starts a new Counter Initialization cycle. (The condition of $\overline{\text{G}} \downarrow \cdot \overline{\text{I}} \cdot \text{TO}$ is satisfied, since a Time Out has occurred and no individual Interrupt has been generated.)

Any of the timers within the PTM may be programmed to compare the period of a pulse (giving the frequency after calculations) at the $\overline{\text{Gate}}$ input with the time period required for Counter Time-Out. A negative transition of the $\overline{\text{Gate}}$ input enables the counter and starts a Counter Initialization cycle — provided that other conditions as noted in Table 7 are satisfied. The counter decrements on each clock signal recognized during or after Counter Initialization until an Interrupt is generated, a Write Timer Latches command is issued, or a Timer Reset condition occurs. It can be seen from Table 7 that an interrupt condition will be generated if CRX5 = 0 and the period of the pulse (single pulse or measured separately repetitive pulses) at the $\overline{\text{Gate}}$ input is less than the Counter Time Out period. If CRX5 = 1, an interrupt is generated if the reverse is true.

Assume now with CRX5 = 1 that a Counter Initialization has occurred and that the $\overline{\text{Gate}}$ input has returned low prior to Counter Time Out. Since there is no Individual Interrupt Flag generated, this automatically starts a new Counter Initialization Cycle. The process will continue with frequency comparison being performed on each $\overline{\text{Gate}}$ input cycle until the mode is changed, or a cycle is determined to be above the predetermined limit.

Pulse Width Comparison Mode (CRX3 = 1, CRX4 = 1)
This mode is similar to the Frequency Comparison Mode except for a positive, rather than negative, transition of the $\overline{\text{Gate}}$ input terminates the count. With CRX5 = 0, an Individual Interrupt Flag will be generated if the zero level pulse applied to the $\overline{\text{Gate}}$ input is less than the time period required for Counter Time Out. With CRX5 = 1, the interrupt is generated when the reverse condition is true.

As can be seen in Table 8, a positive transition of the $\overline{\text{Gate}}$ input disables the counter. With CRX5 = 0, it is therefore possible to directly obtain the width of any pulse causing an interrupt. Similar data for other Time Interval Modes and conditions can be obtained, if two sections of the PTM are dedicated to the purpose.

Table 5. Single-Shot Operating Modes

SINGLE-SHOT OPERATING MODES (CRX3 = 0, CRX7 = 1, CRX5 = 1)			
CONTROL REGISTER		INITIALIZATION/OUTPUT WAVEFORMS	
CRX2	CRX4	COUNTER INITIALIZATION	TIMER OUTPUT (0X)
0	0	$G\downarrow + W + R$	
0	1	$G\downarrow + R$	
1	0	$G\downarrow + W + R$	
1	1	$G\downarrow + R$	

Symbols are as defined in Table 4.

Table 6. Time Interval Modes

CRX4	CRX5	APPLICATION	CONDITION FOR SETTING INDIVIDUAL INTERRUPT FLAG
			CRX3 = 1
0	0	FREQUENCY COMPARISON	INTERRUPT GENERATED IF $\overline{GATE}$ INPUT PERIOD (1/F) IS LESS THAN COUNTER TIME OUT (TO)
0	1	FREQUENCY COMPARISON	INTERRUPT GENERATED IF $\overline{GATE}$ INPUT PERIOD (1/F) IS GREATER THAN COUNTER TIME OUT (TO)
1	0	PULSE WIDTH COMPARISON	INTERRUPT GENERATED IF $\overline{GATE}$ INPUT "DOWN TIME" IS LESS THAN COUNTER TIME OUT (TO)
1	1	PULSE WIDTH COMPARISON	INTERRUPT GENERATED IF $\overline{GATE}$ INPUT "DOWN TIME" IS GREATER THAN COUNTER TIME OUT (TO)

Table 7. Frequency Comparison Mode

CONTROL REG BIT 5 (CRX5)	COUNTER INITIALIZATION	COUNTER ENABLE FLIP-FLOP SET (CE)	COUNTER ENABLE FLIP-FLOP RESET (CE)	INTERRUPT FLAG SET (1)
		CRX3 = 1, CRX4 = 0		
0	$\overline{G}\downarrow \cdot \overline{I} \cdot (\overline{CE} + TO \cdot CE) + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	$W + R + 1$	$\overline{G}\downarrow$ BEFORE TO
1	$\overline{G}\downarrow \cdot \overline{I} + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	$W + R + 1$	TO BEFORE $\overline{G}\downarrow$

$\overline{I}$ represents the interrupt for a given timer.

Table 8. Pulse Width Comparison Mode

CONTROL REG BIT 5 (CRX5)	COUNTER INITIALIZATION	COUNTER ENABLE FLIP-FLOP SET (CE)	COUNTER ENABLE FLIP-FLOP RESET (CE)	INTERRUPT FLAG SET (1)
		CRX3 = 1, CRX4 = 1		
0	$\overline{G}\downarrow \cdot \overline{I} + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	$W + R + \overline{I} + G$	$G\uparrow$ BEFORE TO
1	$\overline{G}\downarrow \cdot \overline{I} + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	$W + R + \overline{I} + G$	TO BEFORE $G\uparrow$

Package Dimensions

28-Pin Ceramic Package

28-Pin Plastic Package

AMI®
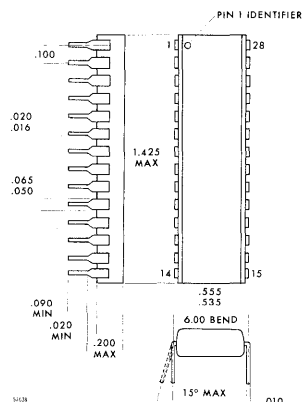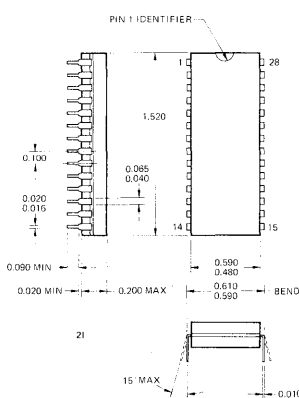
ROM-I/O-TIMER

Features

☐ 2048x8-Bit Bytes of Mask-Programmable ROM

☐ 8-Bit Bidirectional Data Port for Parallel Interface Plus Two Control Lines

☐ Programmable Interval Timer-Counter Functions

☐ Programmable I/O Peripheral Data, Control and Direction Registers

☐ Compatible with the Complete S6800 Microcomputer Product Family

☐ TTL-Compatible Data and Peripheral Lines

☐ Single 5 Volt Power Supply

General Description

The S6846 combination chip provides the means, in conjunction with the S6802, to develop a basic 2-chip microcomputer system. The S6846 consists of 2048 bytes of mask-programmable ROM, an 8-bit bidirectional data port with control lines, and a 16-bit programmable timer-counter.

This device is capable of interfacing with the S6802 (basic S6800, clock and 128 bytes of RAM) as well as the S6800 if desired. No external logic is required to interface with most peripheral devices.

The S6846 combination chip may be partitioned into three functional operating sections: programmed storage, timer-counter functions, and a parallel I/O port.

Block Diagram

*MASK PROGRAMMABLE

Pin Configuration

	S6846 ROM I/O TIMER	
1 VSS		A8 40
2 A7		A9 39
3 A6		A10 38
4 A5		RST 37
5 A4		IRQ 36
6 CS0		CP2 35
7 R/W		CP1 34
8 D0		A0 33
9 D1		A1 32
10 D2		A2 31
11 D3		A3 30
12 D4		VCC 29
13 D5		P7 28
14 D6		P6 27
15 D7		P5 26
16 CS1		P4 25
17 CTG		P3 24
18 CTC		P2 23
19 CTO		P1 22
20 E		P0 21
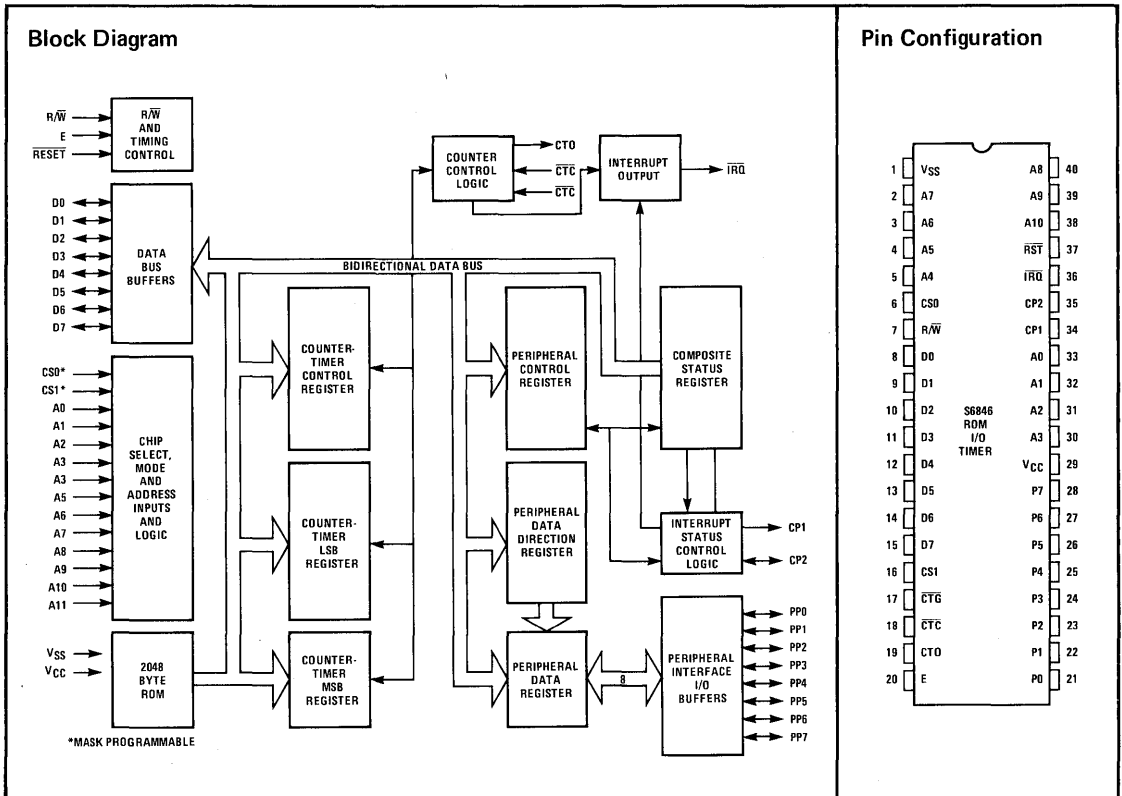
General Description (Continued)

Programmed Storage

The mask-programmable ROM section is similar to other AMI ROM products. The ROM is organized in a 2048 by 8-bit array to provide read only storage for a minimum microcomputer system. Two mask-programmable chip selects are available for user definition.

Address inputs A0-A10 allow any of the 2048 bytes of ROM to be uniquely addressed. Internal registers associated with the I/O functions may be selected with A0, A1 and A2. Bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the S6846.

Timer-Counter Functions

Under software control this 16-bit binary counter may be programmed to count events, measure frequencies and time intervals, or similar tasks. It may also be used for square wave generation, single pulses of controlled duration, and gated delayed signals. Interrupts may be generated from a number of conditions selectable by software programming.

The timer-counter control register allows control of the interrupt enables, output enables, and selection of an internal or external clock source. Input pin $\overline{CTC}$ (counter-timer clock) will accept an asynchronous pulse to be used as a clock to decrement the internal register for the counter-timer. If the divide-by-8 prescaler is used, the maximum clock rate can be four times the master clock frequency with a maximum of 4 MHz. Gate input ($\overline{CTG}$) accepts an asynchronous TTL-compatible signal which may be used as a trigger or gating function to the counter-timer. A counter-timer output ($\overline{CTO}$) is also available and is under software control via selected bits in the timer-counter control register. This mode of operation is dependent on the control register, the gate input, and the external clock.

Parallel I/O Port

The parallel bidirectional I/O port has functional operational characteristics similar to the B port on the S6821 PIA. This includes 8 bidirectional data lines and two handshake control signals. The control and operation of these lines are completely software programmable.

The interrupt input (CP1) will set the interrupt flags of the peripheral control register. The peripheral control (CP2) may be programmed to act as an interrupt input or as a peripheral control output.

S6800

Figure 1. Typical Microcomputer
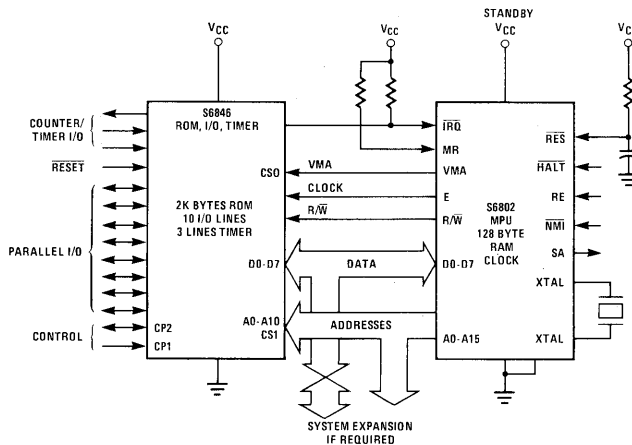
Figure 1 is a block diagram of a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the S6800 Microcomputer family if desired.

Absolute Maximum Ratings

Supply Voltage .... –0.3Vdc to +7.0Vdc

Input Voltage .... –0.3Vdc to +7.0Vdc

Operating Temperature Range .... 0°C to +70°C

Storage Temperature Range .... –55°C to +150°C

Thermal Resistance .... 70°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	All Inputs	V_{SS} + 2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	All Inputs	V_{SS} –0.3		V_{SS} + 0.8	Vdc	
V_{OS}	Clock Overshoot/Undershoot — Input High Level — Input Low Level		V_{CC} –0.5 V_{SS} –0.5		V_{CC} + 0.5 V_{SS} + 0.5	Vdc	
I_{in}	Input Leakage Current	R/$\overline{W}$, $\overline{Reset}$, CS0, CS1 CP1, $\overline{CTG}$, $\overline{CTC}$, E, A0-A11		1.0	2.5 100	µAdc	V_{in} = 0 to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current	D0-D7 PP0-PP7, CR2		2.0	10 100	µAdc	V_{in} 0.4 to 2.4Vdc
V_{OH}	Output High Voltage	D0-D7 CP2, PP0-PP7 Other Outputs	V_{SS} + 2.4 V_{SS} + 2.4 V_{SS} + 2.4			Vdc Vdc	I_{Load} = –205µAdc, I_{Load} = –145µAdc, I_{Load} = –100µAdc
V_{OL}	Output Low Voltage	D0-D7 Other Outputs			V_{SS} + 0.4 V_{SS} + 0.4	Vdc	I_{Load} = 1.6mAdc I_{Load} = 3.2mAdc
I_{OH}	Output High Current (Sourcing)	D0-D7 Other Outputs CP2, PP0-PP7	–205 –200 –1.0		–10	µAdc mADC	V_{OH} = 2.4Vdc V_O = 1.5Vdc, the current for driving other than TTL, e.g., Darlington Base
I_{OL}	Output Low Current (Sinking)	D0-D7 Other Outputs	1.6 3.2			mAdc	V_{OL} = 0.4Vdc
I_{LOH}	Output Leakage Current (Off State)	$\overline{IRQ}$			10	µAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation				1000	mW	
C_{in}	Capacitance	D0-D7 PP0-PP7, CP2 A0-A10, R/$\overline{W}$, $\overline{Reset}$, CS0, CS1, CP1, $\overline{CTC}$, $\overline{CTG}$ $\overline{IRQ}$			20 12.5 10 7.5	pF	V_{in} = 0, T_A = 25°C, f = 1.0MHz
C_{out}		PP0-PP7, CP2, CTO			5.0 10	pF	
f	Frequency of Operation		0.1		1.0	MHz	
t_{cycE} t_{RL} t_{IR}	Clock Timing Cycle Time Reset Low Time Interrupt Release		1.0 2		 1.6	µs µs µs	

Read/Write Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
PW_{EL}	Enable Pulse Width, Low	430			ns	
PW_{EH}	Enable Pulse Width, High	430			ns	
t_{AS}	Set Up Time (Address CS0, CS1, R/W)	160			ns	
t_{DDR}	Data Delay Time			320	ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Ef}, t_{Er}	Rise and Fall Time			25	ns	
t_{DSW}	Data Set Up Time	195			ns	

Bus Timing
Peripheral I/O Lines

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PDSU}	Peripheral Data Setup	200			ns	
t_{Pr}, t_{Pc}	Rise and Fall Times CP1, CP2			1.0	μs	
t_{CP2}	Delay Time E to CP2 Fall			1.0	μs	
t_{DC}	Delay Time I/O Data CP2 Fall	20			μs	
t_{RS1}	Delay Time E to CP2 Rise			1.0	μs	
t_{RS2}	Delay Time CP1 to CP2 Rise			2.0	μs	
t_{PDW}	Peripheral Data Delay			1.0	μs	

Timer-Counter Lines

t_{CR}, t_{CF}	Input Rise and Fall Time CTC and CTG			100	ns	
t_{PWH}	Input Pulse Width High (Asynchronous Mode)	$t_{cyc} + 250$			ns	
t_{PWL}	Input Pulse Width Low (Asynchronous Mode)	$t_{cyc} + 250$			ns	
t_{su}	Input Setup Time (Synchronous Mode)	200			ns	
t_{hd}	Input Hold Time (Synchronous Mode)	50			ns	
t_{CTO}	Output Delay			1.0	μs	

Figure 2. Bus Read Timing
(Read Information from S6846)
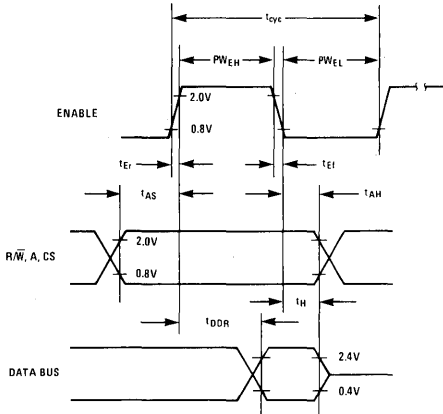
Figure 3. Bus Write Timing
(Write Information from MPU)
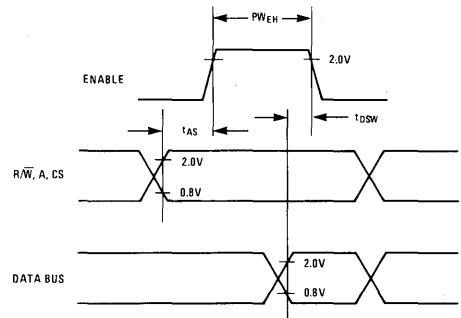
Figure 4. Peripheral Data and CP2 Delay
(Control Mode PCR5 = 1, PCR4 = 0, PCR3 = 1)
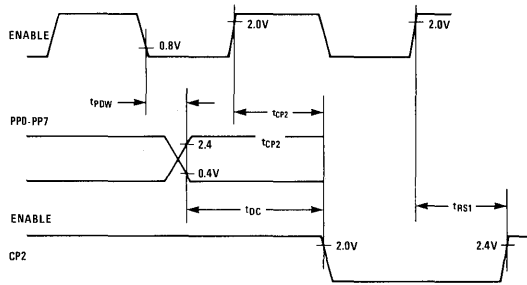
Figure 5. IRQ Release Time
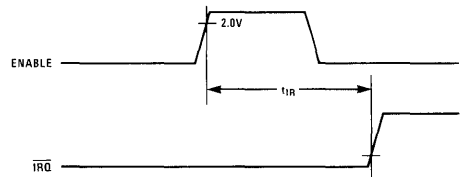
Figure 6. Peripheral Port Setup Time
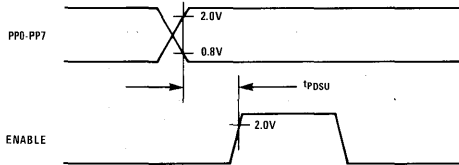
Figure 7. CP2 Delay Time
(PCR5 = 1, PCR4 = 0, PCR3 = 0)
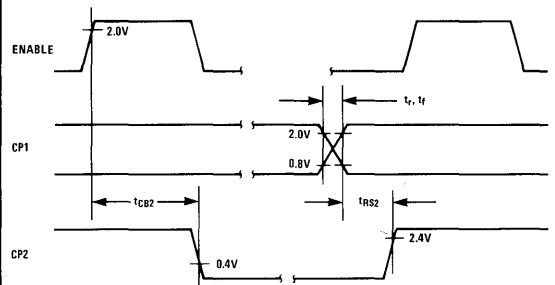
Figure 8. Input Pulse Widths
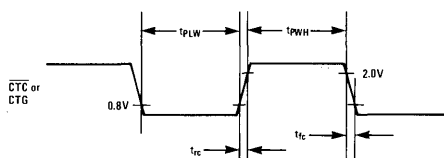
Figure 9. Input Setup and Hold Times
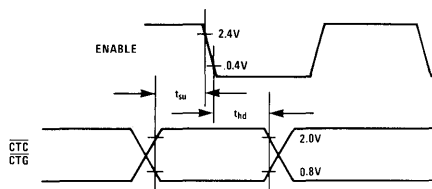
NOTE: This mode is valid only for synchronous operation.

Figure 10. Output Delay
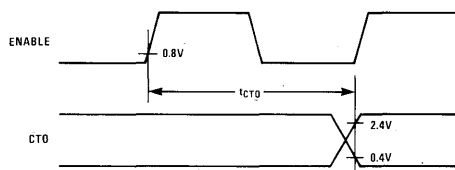
Figure 11. Bus Timing Test Loads

LOAD A
(D0-D7, CTO, CP2, PP0-PP7)

LOAD B
(IRQ ONLY)

TEST POINT

R_L = 2.5k

S6150
OR EQUIV.

S7000
OR EQUIV.

TEST POINT

C = 130pF for D0-D7
  = 30pF for CTO, CP2, PP0-PP7
R = 11.7kΩ for D0-D7
  = 24kΩ for CTO, CP2, PP0-PP7
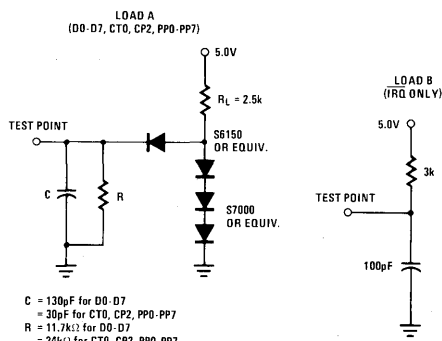
S6800

Signal Description

Bus Interface — The S6846 interfaces to the S6802 or S6800 Bus via an eight-bit bidirectional data bus, two Chip Select lines, a Read/Write line, and eleven address lines. These signals, in conjunction with the S6800/02 VMA output, permit the MPU to control the S6846.

Bidirectional Data Bus (D0-D7) — The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the S6846. The data bus output drivers are three-state devices which remain in the high-impedance (Off) state except when the MPU performs an S6846 register or ROM read (R/W = 1 and I/O Registers or ROM selected).

Chip Select (CS0, CS1) — The CS0 and CS1 inputs are used to select the two major sections of the S6846. They are mask programmed to be active high or active low as chosen by the user.

Address Inputs (A0-A10) — The Address Inputs allow any of the 2048 bytes of ROM to be uniquely selected when the circuit is operating in the ROM mode. In the I/O-Timer mode, address inputs A0, A1, and A2 select the proper I/O Register, while A3 through A10 (together with CS0 and CS1) can be used as additional qualifiers in the I/O Select circuitry. (See the section on I/O-Timer Select for additional details.)

Reset — The active low state of the Reset input is used to initialize all register bits in the I/O section of the device to their proper values. (See the section on Initialization for Reset conditons for timer and peripheral registers.)

Enable (φ2) — This signal synchronized data transfer between the MPU and the S6846. It also performs an equivalent synchronization function on the external clock, reset, and gate inputs of the S6846 Timer section.

Read/Write (R/W) — This signal is generated by the MPU and is used to control the direction of data transfer on the bidirectional data pins. A low level on the R/W input enables the S6846 input buffers and data is transferred to the circuit during the φ2 pulse when the part has been selected. A high level on the R/W input enables the output buffers and data is transferred to the MPU during φ2 when the part is selected.

Interrupt Request (IRQ) — The active low IRQ output acts to interrupt the MPU through logic included on the S6846. This output utilizes an open chain configuration and permits other interrupt request outputs from other circuits to be connected in a wire-OR configuration.

Peripheral Data (P0-P7) — The peripheral data lines can be individually programmed as either inputs or outputs via the Data Direction Register. When programmed as outputs, these lines will drive two standard TTL loads (3.2 mA). They are also capable of sourcing up to 1.0 mA at 1.5 Volts (Logic "1" output.)

When programmed as inputs, the output drives associated with these lines enter a three-state (high impedance) mode. Since there is no internal pull-up for these lines, they represent a maximum 10μA load to the circuitry driving them — regardless of logic state.

A logic zero at the $\overline{\text{Reset}}$ input forces the peripheral data lines to the input configuration by clearing the Data Direction Register. This allows the system designer to preclude the possibility of having a peripheral data output connected to an external driver output during power-up sequence.

Interrupt Input (CP1) — Peripheral input line CP1 is an input-only that sets the Interrupt Flags of the Peripheral Control register. The active transition for this signal is programmed by the control register for the parallel port. CP1 may also act as a strobe for the peripheral data register when it is used as an input latch. Details for programming CP1 are in the section on the parallel peripheral port.

Peripheral Control (CP2) — Peripheral Control line CP2 may be programmed to act as an Interrupt input or Peripheral Control output. As an input, this line has high impedance and is compatible with standard TTL voltage levels. As an output, it is also TTL compatible and may be used as a source of 1 mA at 1.5V to directly drive the base of a Darlington transistor switch. This line is programmed by the Control Register for the parallel port.

Counter Timer Output (CTO) — The Counter Timer Output is software programmable by selected bits in the timer counter control register. The mode of op-

eration is dependent on the Timer control register, the gate input, and the external clock. The output is TTL compatible.

External Clock Input ($\overline{\text{CTC}}$) — Input pin $\overline{\text{CTC}}$ will accept asynchronous TTL voltage level signals to be used as a clock to decrement the Timer. The high and low levels of the external clock must be stable for at least one system clock period plus the sum of the setup and hold times for the inputs. The asynchronous clock rate can vary from dc to the limit imposed by System ϕ2, setup, and hold times.

The external clock input is clocked in by Enable (System ϕ2) pulses. Three Enable periods are used to synchronize and process the external clock. The fourth Enable pulse decrements the internal counter. This does not affect the input frequency; it merely creates a delay between a clock input transition and internal recognition of that transition by the S6846. All references to $\overline{\text{CTC}}$ inputs in this document relate to internal recognition of the input transition. Note that a clock transition which does not meet setup and hold time specifications may require an additional Enable pulse for recognition.

When observing recurring events, a lack of synchronization will result in either "System jitter" or "Input jitter" being observed on the output of the S6846 when using an asynchronous clock and gate input signal. "System jitter" is the result of the input signals being out of synchronization with the system ϕ2 clock (Enable), permitting signals with marginal set-up and hold time to be recognized by either the bit time nearest the input transition or subsequent bit time. "Input jitter" can be as great as the time between the negative going transitions of the input signal plus the system jitter if the first transition is recognized during one system cycle, and not recognized the next cycle or vice-versa.

Figure 12.

3.74
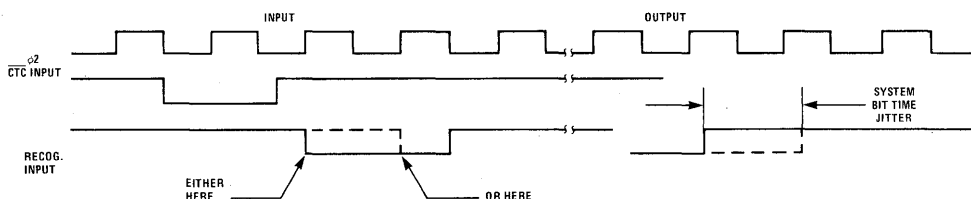
Gate Input ($\overline{\text{CTG}}$) — The input pin $\overline{\text{CTG}}$ accepts as asynchronous TTL-compatible signal which is used as a trigger or a clock gating function to the Timer. The gating input is clocked into the S6846 by the Enable (System $\phi2$) signal in the same manner as the previously discussed clock inputs. That is, a $\overline{\text{CTG}}$ transition is recognized on the fourth Enable pulse (provided set-up and hold time requirements are met), and the high or low levels of the $\overline{\text{CTG}}$ input must be stable for at least one system clock period plus the sum of setup and hold times. All references to $\overline{\text{CTG}}$ transition in this document relate to internal recognition of the input transition.

The $\overline{\text{CTG}}$ input of the timer directly affects the internal 16-bit counter. The operation of $\overline{\text{CTG}}$ is therefore independent of the ÷ 8 prescaler selection.

Functional Select Circuitry

I/O Timer Select Circuitry — Two chip select inputs are provided with the S6846, and are programmed active high or low simultaneously with the ROM pattern. The I/O-Timer selection can therefore be made to correspond to any one of the four possible state combinations of the two chip select inputs. ($\overline{\text{CS0}}$-$\overline{\text{CS1}}$, CS0-$\overline{\text{CS1}}$, $\overline{\text{CS0}}$-CS1, or CS0-CS1)

Address lines A3, A4, and A5 are also used as I/O-Timer Select inputs. Specifically, these lines must be at a logic zero (low) for the I/O-Timer section to be selected. Address line A6 can also be used as a qualifier for I/O-Timer selection, as can any one of the four high Address lines (A7 through A10). A6 is unique among these selector inputs in that it is possible to program either the high or low state of A6 as an I/O-Timer select input.

The circuit of Figure 13 is representative of the I/O-Timer select circuitry on the S6846. The mask programmable options are represented by switches.

Internal Addressing — Seven I/O Register locations within the S6846 combination circuit are accessible to the MPU data bus. Selection of these registers is controlled by A0, A1, and A2 as shown in Table 1. CS0 and CS1 must be in the I/O state and the proper register address must be applied to access a particular register. The combination status register is Read-only; all other Registers are Read/Write.

Figure 13. I/O-Timer Select Circuitry

*SWITCHES REPRESENT MASK PROGRAMMABLE INTERCONNECTS.
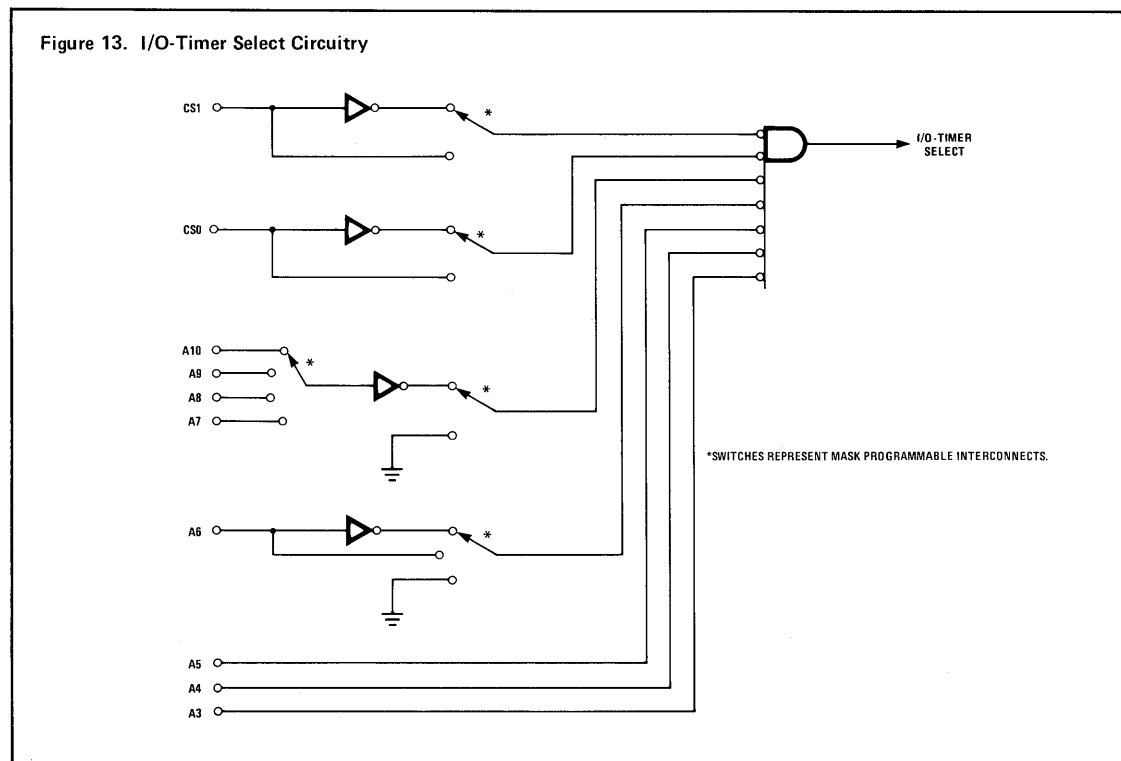
Table 1. Internal Register Addresses

Registered Selected	A2	A1	A0
Combination Status Register	0	0	0
Peripheral Control Register	0	0	1
Data Direction Register	0	1	0
Peripheral Data Register	0	1	1
Combination Status Register	1	0	0
Timer Control Register	1	0	1
Timer MSB Register	1	1	0
Timer LSB Register	1	1	1
ROM Address	X	X	X

Initialization — When the $\overline{\text{Reset}}$ input has accepted a low signal, all registers are initialized to the $\overline{\text{Reset}}$ state. The data direction and data registers are cleared. The Peripheral Control Register is cleared except for bit 7 (the $\overline{\text{Reset}}$ bit). This forces the parallel port to the input mode with Interrupts disabled. To remove the $\overline{\text{Reset}}$ condition from a parallel port, an "0" must be written into the Peripheral Control Register bit 7 (PCR7).

The counter latches are preset to their maximal count, the Timer control register bits are reset to zero except for Bit 0 (CCR0) (which is set), the counter ouput is cleared, and the counter clock disabled. This state forces the timer counter to remain in an inactive state. The combination status register is cleared of all interrupt flags. During timer initialization, the reset bit (CCR0) must be cleared.

ROM — The Mask Programmable ROM section is similar in operation to other AMI ROM products. The ROM is organized as 2048 words of 8-bits to provide read-only storage for a minimum microcomputer system. The ROM is active when selected by the unique combination of the chip select inputs.

ROM Select — The active levels of CS0 and CS1 for ROM and I/O select are a user programmable option. Either CS0 or CS1 may be programmed active high or active low, but different codes must be used for ROM or I/O select. CS0 and CS1 are mask programmed simultaneously with the ROM pattern. The ROM Select Circuitry is shown in Figure 14.

Timer Operation

The Timer may be programmed to operate in modes which fit a wide variety of applications. The device is fully bus compatible with the S6800 system, and is accessed by Load and Store operations from the MPU.

In a typical application, the timer will be loaded by storing two bytes of data into the counter latch. This data is then transferred into the counter during a Counter Initialization cycle. The counter decrements on each subsequent clock cycle (which may be system $\phi2$ or an external clock) until one of several predetermined conditions causes it to halt or recycle. Thus the timer is programmable, cyclic in nature, controllable by external inputs or MPU program, and accessible to the MPU at any time.

Counter Latch Initialization — The Timer consists of a 16-bit addressable counter and 16 bits of addressable latches. The function of the latches is to store a binary equivalent of the desired count value minus one. Counter initialization results in the transfer of the latch contents of the counter. It should be noted that data transfer to the counters is always accomplished via the latches. Thus, the counter latches may be accurately described as a 16-bit "counter initialization data" storage register.

In some modes of operation, the initialization of the latches will cause simultaneous counter initialization (i.e., immediate transfer of the new latch data into the counters). It is, therefore, necessary to insure that

Figure 14. ROM Select Circuitry

CS1

CS0

ROM SELECT

*SWITCHES REPRESENT MASK PROGRAMMABLE INTERCONNECTS.
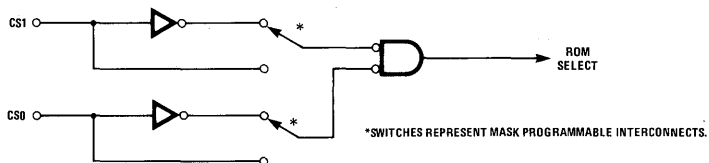
all 16 bits of the latches are updated simultaneously. Since the S6846 data bus is 8 bits wide, a temporary register (MSB Buffer Register) is provided for in the Most Significant Byte of the desired latch data. This is a "write-only" register selected via address lines A0, A1, and A2. Data is transferred directly from the data bus to the MSB Buffer when the chip is selected, R/$\overline{\text{W}}$ is low, and the timer MSB register is selected (A0 = "0"; A1 = A2 = "1").

The lower 8 bits of the counter latch can also be referred to as a "write-only" register. Data Bus information will be transferred directly to the LSB of a counter latch when the chip is selected, R/$\overline{\text{W}}$ is low and the Timer LSB Register is selected (A0 = A1 = A2 = "1"). Data from the MSB Buffer will automatically be transferred into the Most Significant Byte of the counter latches simultaneously with the transfer of the Data Bus information to the Least Significant Byte of the Counter Latch. For brevity, the conditions for this operation will be referred to henceforth as a "Write Timer Latches Command."

The S6846 has been designed to allow transfer of two bytes of data into the counter latches from any source, provided the MSB is transferred first. In many applications, the source of data will be an S6802 or S6800 MPU. It should therefore be noted that the 16-bit store operations of the S6800 family of microprocessors (STS and STX) transfer data in the order required by the S6846. A Store Index Register instruction, for example, results in the MSB of the X register being transferred to the selected address, then the LSB of the X register being written into the next higher location. Thus, either the index register or stack pointer may be transferred directly into a selected counter latch with a single instruction.

A logic zero at the $\overline{\text{Reset}}$ input also initializes the counter latches. All latches will assume maximum count (65, 536) values. It is important to note that an internal $\overline{\text{Reset}}$ (Bit zero of the Timer Control Register Set) has no effect on the counter latches.

Counter Initialization — Counter Initialization is defined as the transfer of data from the latches to the counter with attendant clearing of the Individual Interrupt Flag associated with the counter. Counter Initialization always occurs when a reset condition (external $\overline{\text{Reset}}$ = 0 or TCRO = 1) is recognized. It can also occur (dependent on the Timer Mode) with a Write Timer Latches command or recognition of a negative transition of the $\overline{\text{Gate}}$ input.

Counter recycling or reinitialization occurs when a clock input is recognized after the counter has reached an all-zero state. In this case, data is transferred from the Latches to the Counter, but the Interrupt Flag is unaffected.

Timer Control Register — The Timer Control register (see Table 2) in the S6846 is used to modify timer operation to suit a variety of applications. The Control

Table 2. Format for Timer/Counter Control Register

Control Register Bit	State	Bit Definition	State Definition
TCR0	0	Internal Reset	Timer Enabled
	1		Timer in Preset State
TCR1	0	Clock Source	Timer uses External Clock ($\overline{\text{CTC}}$)
	1		Timer uses $\phi2$ System Clock
TCR2	0	÷ 8 Prescaler	Clock is not Prescaled
	1	Enabler	Clock is Prescaled by ÷ 8 Counter
TCR3	X		
TCR4	X	Operating Mode Selection	See Table 3
TCR5	X		
TCR6	0	Timer Interrupt Enable	$\overline{\text{IRQ}}$ Masked from Timer
	1		$\overline{\text{IRQ}}$ Enabled from Timer
TCR7	0	Timer Output Enable	Counter Output (CTO) Set LOW
	1		Counter Output Enabled

Register has a unique address space (A0 = 1, A1 = 0, A2 = 1) and therefore may be written into at any time. The least significant bit of the Control Register is used as an Internal Reset bit. When this bit is a logic zero, all timers are allowed to operate in the modes prescribed by the remaining bits of the control registers.

Writing "one" into Timer Control Register Bit 0 (TCR0) causes the counter to be preset with the contents of the counter latches, all counter clocks to be disabled, and the timer output and interrupt flag (Status Register) to be reset. The Counter Latch and Control Register are undisturbed by an Internal Reset and may be written into regardless of the state of TCR0.

Timer Control Register Bit 1 (TCR1) is used to select the clock source. When TCR1 = 0, the external clock input $\overline{CTC}$ is selected, and when TCR1 = "1", the timer uses system $\phi 2$.

Timer Control Register Bit 2 (TCR2) enables the $\div 8$ prescaler (TCR1 = "1"). In this mode, the clock frequency is divided by eight before being applied to the counter. When TCR2 = "0" the clock is applied directly to the counter.

TCR3, 4, 5 select the Timer Operating Mode, and are discussed in the next section.

Timer Control Register Bit 6 (TCR6) is used to mask or enable the Timer Interrupt Request. When TCR6 = 0, the Interrupt Flag is masked from the timer. When TCR6 = 1, the Interrupt Flag is enabled into Bit 7 of the Composite Status Register (Composite IRQ Bit), which appears on the $\overline{IRQ}$ output pin.

Timer Control Register Bit 7 (TCR7) has a special function when the timer is in the Cascaded Single Shot mode. (This function is explained in detail in the section describing the mode.) In all other modes, TCR7 merely acts as an output enable bit. If TCR7 = 0, the Counter Timer Output (CTO) is forced low. Writing a logic one into TCR7 enables CTO.

Timer Operating Modes — The S6846 has been designed to operate effectively in a wide variety of applications. This is accomplished by using three bits of the control register (TCR3, TCR4, and TCR5) to define different operating modes of the Timer, outlined in Table 3.

Continuous Operating Mode (TCR3 = 0, TCR5 = 0) — The timer may be programmed to operate in a continuous counting mode by writing zeros into bits 3 and 5 of the timer control register. Assuming that the timer output is enabled (TCR7 = 1), a square wave will be generated at the Timer Output CTO (see Table 4).

Either a Timer Reset (TCR0 = 1 or External $\overline{Reset}$ = 0) condition or internal recognition of a negative transition of the $\overline{CTG}$ input results in Counter Initialization. A Write Timer Latches command can be selected as a Counter Initialization signal by clearing TCR4.

Table 3. Operating Modes

TCR5	TCR4	TCR3	Timer Operating Mode	Counter Initialization	Interrupt Flag Set
0	0	0	Continuous	$\overline{CTG}\downarrow + W + R$	T.O.
0	0	1	Cascaded Single Shot	$\overline{CTG}\downarrow + R$	T.O.
0	1	0	Continuous	$\overline{CTG}\downarrow + R$	T.O.
0	1	1	Normal Single Shot	$\overline{CTG}\downarrow + R$	T.O.
1	0	0	Frequency Comparison	$\overline{CTG}\downarrow \cdot \overline{I} \cdot (W + T.O.) + R$	$\overline{CTG}\downarrow$ Before T.O.
1	0	1		$\overline{CTG}\downarrow \cdot \overline{I} + R$	T.O. Before $\overline{CTG}\downarrow$
1	1	0	Pulse Width Comparison	$\overline{CTG}\downarrow \cdot \overline{I} + R$	$\overline{CTG}\uparrow$ Before T.O.
1	1	1			T.O. Before $\overline{CTG}\uparrow$

R = Reset Condition
W = Write Time Latches
T.O. = Counter Time Out

$\overline{CTG}\downarrow$ = Negative Transition of Pin 17
$\overline{CTG}\uparrow$ = Positive Transition of Pin 17
$\overline{I}$ = Interrupt Flag (CSR0) = 0

Table 4. Continuous Operating Modes

Continuous Mode (TCR3 = 0, TCR7 = 1, TCR5 = 0)			
Control Register Register			Initialization/Output Waveforms
TCR2	TCR4	Counter	Timer Output (2X)
0	0	Initialization $\overline{G} + \overline{W} + R$	$\leftarrow(N+1)\,(T) \rightarrow$ $\leftarrow(N+1)\,(T)\rightarrow$ $\leftarrow(N+1)\,(T)\rightarrow$ — V_{OH} — V_{OL}
0	1	$\overline{G} + R$	to T.O. T.O. T.O.

$\overline{G}$ = Negative transition of $\overline{GATE}$ input.

$\overline{W}$ = Write Timer Latches Command.

R = Timer Reset (TCR0 = 1 or External $\overline{RESET}$ = 0)

N = 16 Bit Number in Counter Latch.

T = Period of Clock input to Counter.

to = Counter initialization Cycle.

T.O. = Counter Time Out (All Zero Condition).

The discussion of the Continuous Mode has assumed the application requires an output signal. It should be noted the Timer operates in the same manner with the output disabled (TCR7 = 0). A Read Timer Counter command is valid regardless of the state of TCR7.

Normal Single-Shot Timed Mode (TCR3 = 0, TCR4 = 1, TCR5 = 1) — This mode is identical to the Continuous Mode with two exceptions. The first of these is obvious from the name — the output returns to a low-level after the initial Time Out and remains low until another Counter Initialization cycle occurs. The output waveform (CTO) is shown in Figure 15.

As indicated in Figure 15, the internal counting mechanism remains cyclical in the Single-Shot Mode. Each Time Out of the counter results in the setting of an Individual Interrupt Flag and reinitialization of the counter.

The second major difference between the Single-Shot and Continuous modes is that the internal counter enable is not dependent on the $\overline{CTG}$ input level remaining in the low state for the Single-Shot mode. Aside from these differences, the two modes are identical.

Figure 15. Single-Shot Modes

(A) NORMAL SINGLE-SHOT MODE OUTPUT WAVEFORM

(B) CASCADED SINGLE-SHOT MODE OUTPUT WAVEFORM

1 = WRITE A "1" INTO TCR-7
0 = WRITE A "0" INTO TCR-7

*POINT AT WHICH AN INTERRUPT MAY OCCUR

Note: All time intervals shown above assume the Gate ($\overline{CTG}$) and Clock (CTC) signals are synchronized to system φ2 with specified setup and hold time requirements.
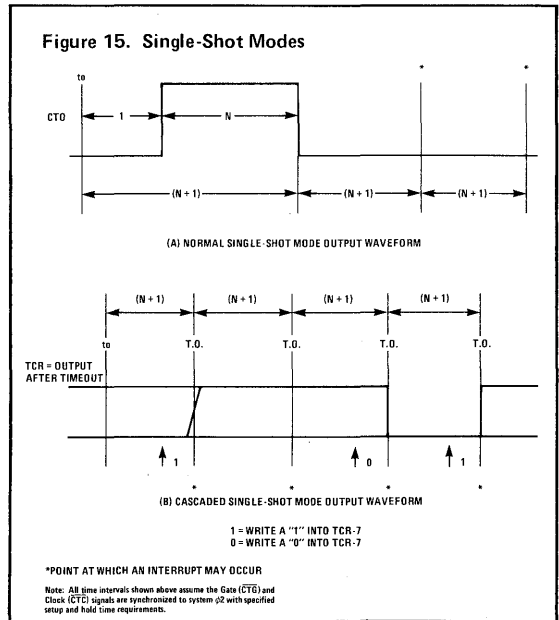
Time Interval Modes (TCR3 = 1) — The Time Interval Modes are provided for applications requiring more flexibility of interrupt generation and Counter Initialization. Individual Interrupt Flags are set in these modes as a function of both Counter Time Out and transitions of the $\overline{\text{CTG}}$ input. Counter Initialization is also affected by Interrupt Flag status. The output signal is not defined in any of these modes. Other features of the Time Interval Modes are outlined in Table 5.

Cascaded Single-Shot Mode (TCR3 = 0, TCR4 - 0, TCR5 = 1) — This mode is identical to the single-shot mode with two exceptions. First, the output waveform does not return to a low level and remain low after timeout. Instead, the output level remains at its initialized level until it is reprogrammed and changed by timeout. The output level may be changed at any timeout or may have any number of timeouts between changes.

The second difference is the method used to change the output level. Timer Control Register Bit 7 (TCR7) has a special function in this mode. The timer output (CTO) is equal to TCR7 clocked by timeout. At every timeout, the content of TCR7 is clocked to and held at the CTO output. Thus, output pulses of length greater than one timer cycle can be generated by cascading timer cycles and counting timeouts with a software program. (See Figure 15).

An interrupt is generated at each timeout. To cascade timer cycles, the MPU would need an interrupt routine to: 1) count each timeout and determine when to change TCR7; 2) write into TCR7 the state corresponding to the next desired state of the output waveform (only necessary during the last timer cycle before the output is to change state); and 3) clear the interrupt flag by reading the combination status register. It is also possible, if desired, to change the length of the timer cycle by reinitializing the timer latches. This allows more flexibility for obtaining desired times.

Table 5. Time Interval Modes

TCR3 = 1			
TCR4	TCR5	Application	Condition for Setting Individual Interrupt Flag
0	0	Frequency Comparison	Interrupt Generated if $\overline{\text{CTG}}$ Input Period (1/F) is Less Than Counter Time Out (T.O.)
0	1	Frequency Comparison	Interrupt Generated if $\overline{\text{CTG}}$ Input Period (1/F) is Greater Than Counter Time Out (T.O.)
1	0	Pulse Width Comparison	Interrupt Generated if $\overline{\text{CTG}}$ Input "Down Time" is Less Than Counter Time Out (T.O.)
1	1	Pulse Width Comparison	Interrupt Generated if $\overline{\text{CTG}}$ Input "Down Time" is Greater Than Counter Time Out (T.O.)

Frequency Comparison Mode (TCR3 = 1, TCR4 = 0) — The timer within the S6846 may be programmed to compare the period of a pulse (giving the frequency after calculations) at the $\overline{\text{CTG}}$ input with the time period required for Counter Time Out. A negative of the $\overline{\text{CTG}}$ input enables the counter and starts a Counter Initialization cycle — provided that other conditions as noted in Table 6 are satisfied. The counter decrements on each clock signal recognized during or after Counter Initialization until an Interrupt is generated, a Write Timer Latches command is issued, or a Timer Reset condition occurs. It can be seen from Table 6 that an interrupt condition will be generated if TCR5 = 0 and the period of the pulse (single pulse or measured separately repetitive pulses) at the $\overline{\text{CTG}}$ input is less than the Counter Time Out period. If TCR5 = 1, an interrupt is generated if the reverse is true.

Assume now with TCR5 = 1 that a Counter Initialization has occurred and that the $\overline{\text{CTG}}$ input has returned low prior to Counter Time Out. Since there is no individual Interrupt Flag generated, this automatically starts a new Counter Initialization Cycle. The process will continue with frequency comparison being performed on each $\overline{\text{CTG}}$ input cycle until the mode is changed, or a cycle is determined to be above the predetermined limit.

Pulse Width Comparison Mode (TCR3 = 1, TCR4 = 1) — This mode is similar to the Frequency Comparison Mode except for the limiting factor being a positive, rather than negative, transition of the $\overline{\text{CTG}}$ input. With TCR5 = 0, an Individual Interrupt Flag will be generated if the zero level pulse applied to the $\overline{\text{CTG}}$ input is less than the time period required for Counter Time Out. With TCR5 = 1, the interrupt is generated when the reverse condition is true.

As can be seen in Table 7, a positive transition of the $\overline{\text{CTG}}$ input disables the counter. With TCR5 = 0, it is therefore possible to directly obtain the width of any pulse causing an interrupt.

Table 6. Frequency Comparison Mode

CRX3 = 1, CRX4 = 0				
Control Reg Bit 5 (CRX5)	Counter Initialization	Counter Enable Flip-Flop Set (CE)	Counter Enable Flip-Flop Reset (CE)	Interrupt Flag Set (1)
0	$\overline{\text{G}}{\downarrow}\cdot\overline{\text{I}}\cdot(\overline{\text{CE}}+\text{TO}\cdot\text{CE})+\text{R}$	$\overline{\text{G}}{\downarrow}\cdot\overline{\text{W}}\cdot\overline{\text{R}}\cdot\overline{\text{I}}$	$\text{W}+\text{R}+\text{I}$	$\overline{\text{G}}{\downarrow}$ Before TO
1	$\overline{\text{G}}{\downarrow}\cdot\overline{\text{I}}+\text{R}$	$\overline{\text{G}}{\downarrow}\cdot\overline{\text{W}}\cdot\overline{\text{R}}\cdot\overline{\text{I}}$	$\text{W}+\text{R}+\text{I}$	TO Before $\overline{\text{G}}{\downarrow}$

I represents the interrupt for the timer.

Table 7. Pulse Width Comparison Mode

CRX3 = 1, CRX4 = 1				
Control Reg Bit 5 (CRX5)	Counter Initialization	Counter Enable Flip-Flop Set (CE)	Counter Enable Flip-Flop Reset (CE)	Interrupt Flag Set (1)
0	$\overline{\text{G}}{\downarrow}\cdot\overline{\text{I}}+\text{R}$	$\overline{\text{G}}{\downarrow}\cdot\overline{\text{W}}\cdot\overline{\text{R}}\cdot\overline{\text{I}}$	$\text{W}+\text{R}+\text{I}+\text{G}$	$\overline{\text{G}}{\uparrow}$ Before TO
1	$\overline{\text{G}}{\downarrow}\cdot\overline{\text{I}}+\text{R}$	$\overline{\text{G}}{\downarrow}\cdot\overline{\text{W}}\cdot\overline{\text{R}}\cdot\overline{\text{I}}$	$\text{W}+\text{R}+\text{I}+\text{G}$	TO Before $\overline{\text{G}}{\uparrow}$

S6800

Differences Between the S6840 and the S6846 Timers

1) Control registers 1 and 3 are buried (access through control register 2 only) in the S6840 timer. In the S6846, all registers are directly accessible.

2) The S6840 has a dual 8 bit continuous mode for generating non-symmetrical waveforms. The S6846, instead, has a cascaded one shot mode which can accomplish the same function, but also allows the user to generate waveforms longer than one timeout.

3) Because of the different modes, there is a difference in the control registers between the S6840 and the S6846.

Control Register Bit	S6840	S6846
2	16 bit or dual 8 bit mode control	÷8 prescale enable
7	output enable (all modes)	output next state (cascaded one shot mode only), output enable all other modes
0	R_1 internal reset R_2 control register select R_3 timer 3 clock control	internal reset

Composite Status Register — The Composite Status Register (CSR) is a read-only register which is shared by the Timer and the Peripheral Data Port (of the S6846.) Three individual interrupt flags in the register are set directly via the appropriate conditions in the timer or peripheral port. The composite interrupt flag — and the $\overline{IRQ}$ Output — respond to these individual interrupts only if corresponding enable bits are set in the appropriate Control Registers. (See Figure 16). The sequence of assertion is not detected. Setting TCR6 while CSR0 is high will cause CSR7 to be set, for example.

The Composite Interrupt Flag (CSR7) is clear only if all enabled Individual Interrupt Flags are clear. The conditions for clearing CSR1 and CSR2 are detailed in a later section. The Timer Interrupt Flag (CSR0) is cleared under the following conditions:

1) Timer Reset — Internal Reset Bit (TCR0) = 1 or External $\overline{Reset}$ = 0.

2) Any Counter Initialization condition.

3) A Write Timer Latches command if Time Interval (TCR3 = 1) are being used.

4) A Read Timer Counter command, provided this is preceded by a Read Composite Status Register while CSR0 is set. This latter condition prevents missing an Interrupt Request generated after reading the Status Register and prior to reading the counter.

5) The remaining bits of the Composite Status Register (CR3-CSR6) are unused. They default to a logic zero when read.

Figure 16. Composite Status Register and Associated Logic
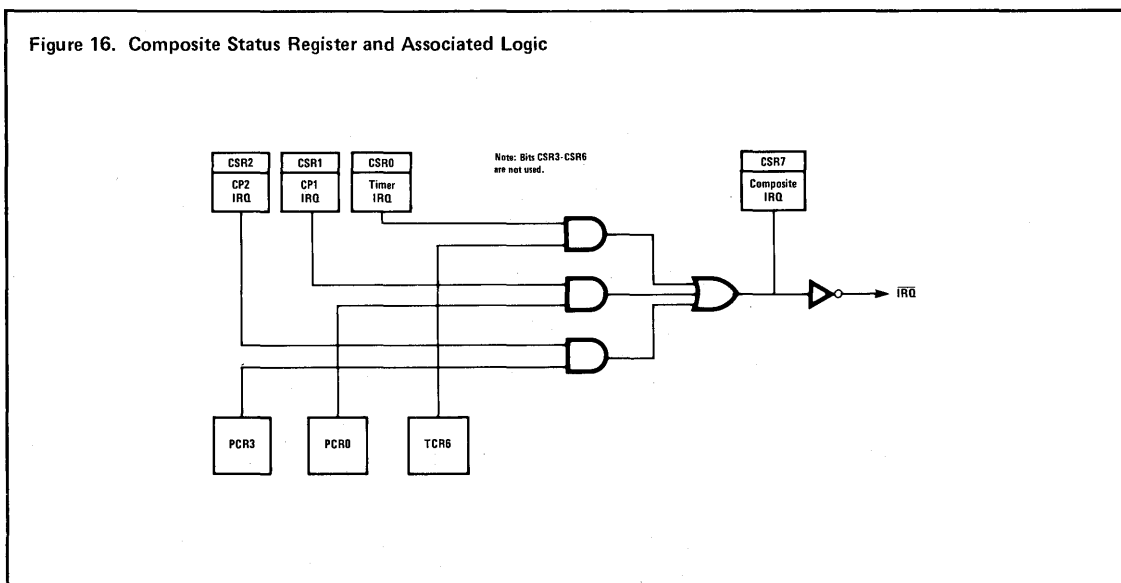
I/O Operation

Parallel Peripheral Port — The peripheral port of the S6846 contains 8 Peripheral Data lines (P0-P7), two Peripheral Control lines (CP1 and CP2), a Data Direction Register, a Peripheral Data Register, and a Peripheral Control Register. The port also directly affects two bits (CSR1 and CSR2) of the Composite Status Register.

The Peripheral Port is similar to the "B" side of a PIA (S6820 or S6821) with the following exceptions:

1) All registers are directly accessible in the S6846. Data Direction and Peripheral Data in the S6820/6821 are located at the same address, with Bit Two of the Control Register used for register selection.
2) Peripheral Control Register Bit Two (PCR2) of the S6846 is used to select an optional input latch function. This option is not available with S6820/6821 PIA's.
3) Interrupt Flags are located in the S6846 composite status register rather than Bits 6 and 7 of the Control Register as used in the S6820/6821.
4) Interrupt Flags are cleared in the S6820/6821 by reading data from the Peripheral Data Register. S6846 Interrupt Flags are cleared by either reading or writing to the Peripheral Data Register — provided that a sequence of a) Flag Set, b) Read Composite Status Register, c) Read/Write Peripheral Data Register is followed.
5) Bit 6 of the S6846 Peripheral Control Register is not used. Bit 7 (PCR7) is an Internal Reset Bit not available on the S6820/6821.

6) The Peripheral Data lines (and CP2) of the S6846 feature internal current limiting which allows them to directly drive the base of Darlington NPN transistors.

Data Direction Register — The MPU can write directly to this eight-bit register to configure the Peripheral Data lines as either inputs or outputs. A particular bit within the register (DDRN) is used to control the corresponding Peripheral Data line (PN). With DDRN = 0, PN becomes an input; if DDRN = 1, PN is an output. As an example, writing Hex SOF into the Data Direction Register results in P0 through P3 becoming outputs and P4 through P7 being inputs. Hex S35 is the Data Direction Register results in alternate outputs and inputs at the parallel port.

Peripheral Data Register — This eight-bit register is used for transferring data between the peripheral data port and the MPU. Any bit corresponding to an output line will be used to drive the output buffer associated with that line. Data in these output bits is normally provided by an MPU Write function (Input bits — those associated with input lines — are unchanged by a Write Command.) Any input bit will reflect the state of the associated input line if the input latch function is deselected. If the Control Register is programmed to provide input latching, the input bit will retain the state at the time CP1 was activated until the Peripheral Data Register is read by the MPU.

Peripheral Control Register — This eight-bit register is used to control the reset function as well as for selection of optional functions of the two peripheral control lines (CP1 and CP2). The peripheral Control Register functions are outlined in Table 8.

Table 8. Peripheral Control Register Format (Expanded)

3.83
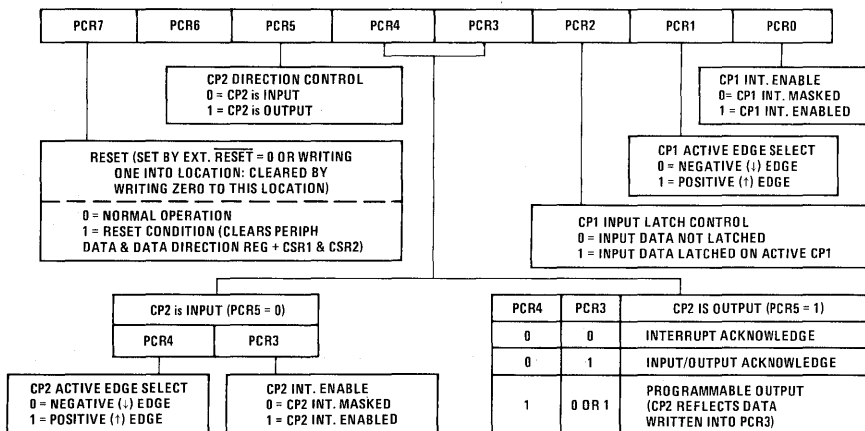
Peripheral Port Reset (PCR7) — Bit 7 of the Peripheral Control Register (PCR7) may be used to initialize the peripheral section of the S6846. When this bit is set high, the peripheral data register, the peripheral data direction register, and the interrupt flags associated with the peripheral port (CSR1 and CSR2) are all cleared. Other bits in the peripheral control register are not affected by PCR7.

PCR7 is set by either a logic zero at the External $\overline{\text{RESET}}$ input or under program control by writing a "one" into the location. In any case, PCR7 may be cleared only by writing a zero into the location while $\overline{\text{RESET}}$ is high. The bit must be cleared to activate the port.

Control of CP1 Peripheral Control Line — CP1 may be used as an interrupt request to the S6846, as a strobe to allow latching of input data, or both. In any case, the input can be programmed to be activated by either a positive or negative transition of the signal. These options are selected via Control Register Bits PCR0, PCR1 & PCR2.

Control Register Bit 0 (PCR0) is used to enable the interrupt transfer circuitry of the S6846. Regardless of the state of PCR0, an active transition of CP1 causes the Composite Status Register Bit One (CSR1) to be set. If PCR0 = 1, this interrupt will be reflected in the Composite Interrupt Flag (CSR7), and thus at the $\overline{\text{IRQ}}$ output. CSR1 is cleared by a Timer Reset condition or by either reading or writing to the peripheral data register after the Composite Status Register is read. The latter alternative is conditional — CSR1 must have been a logic one when the Composite Status Register was last read. This precludes inadvertent clearing of interrupt flags generated between the time the Status Register is read and the manipulation of peripheral data.

Control Register Bit One (PCR1) is used to select the edge which activates CP1. When PCR1 = 0, CP1 is active on negative transitions (high to low). Low to High transitions are sensed by CP1 when PCR1 = 1.

In addition to its use as an interrupt input, CP1 can be used as a strobe to capture input data in an internal latch. This option is selected by writing a one into Peripheral Control Register Bit Two (PCR2). In operation, the data at the pins designated by the Data Direction Register as inputs will be captured by an active transition of CP1. An MPU Read of the Peripheral Data Register will result in the captured data being transferred to the MPU — and it also releases the latch to allow capture of new data. Note that successive active transitions with no Read Peripheral Data Command between does not update the input latch. Also, it should be noted that use of the input latch function (which can be deselected by writing a zero into PCR2) has no effect on output data. It also does not affect Interrupt function of CP1.

Control of CP2 Peripheral Control Line — CP2 may be used as an input by writing a zero into PCR5. In this configuration, CP2 becomes a dual of CP1 in regard to generation of interrupts. An active transition (as selected by PCR4) causes Bit Two of the Composite Status Register to be set. PCR3 is then used to select whether the CP2 transition is to cause CSR2 to be set — and thereby cause $\overline{\text{IRQ}}$ to go low. CP2 has no effect on the input latch function of the S6846.

Writing a one into PCR5 causes CP2 to function as an output. PCR4 then determines whether CP2 is to be used in a handshake or programmable output mode. With PCR4 = 1, CP2 will merely reflect the data written into PCR3. Since this can readily be changed under program control, this mode allows CP2 to be a programmable output line in much the same manner as those lines selected as outputs by the Data Direction Register.

The handshaking mode (PCR5 = 1, PCR4 = 0) allows CP2 to perform one of two functions as selected by PCR3. With PCR3 = 1, CP2 will go low on the first Enable (System $\phi2$) positive transition after a Read or Write to the Peripheral Data Register. This $\overline{\text{Input/}}$ $\overline{\text{Output Acknowledge}}$ signal is released (returns high) on the next positive transition of the Enable signal.

In the $\overline{\text{Interrupt Acknowledge}}$ mode (PCR5 = 1, PCR4 = PCR3 = 0), CP2 is set when CSR1 is set by an active transition of CP1. It is released (goes low) on the first positive transition of Enable after CSR1 has been cleared via an MPU Read or Write to the Peripheral Data Register. (Note that the previously described conditions for clearing CSR1 still apply.)

Restart Sequence — A typical restart sequence for the S6846 will include initialization of both the Peripheral Control and Data Direction Registers of the parallel port. It is necessary to set up the Peripheral Control Register first, since PCR7 = 0 is a condition for writing data into the Data Direction Register. (A logic zero at the external $\overline{\text{Reset}}$ input automatically sets PCR7.)

Summary — The S6846 has several optional modes of operation which allow it to be used in a variety of applications. The following tables are provided for reference in selecting these modes.

Table 9. S6846 Internal Register Addresses

A2	A1	A0	Register Selected
0	0	0	Combination Status Register
0	0	1	Peripheral Control Register
0	1	0	Data Direction Register
0	1	1	Peripheral Data Register
1	0	0	Combination Status Register
1	0	1	Timer Control Register
1	1	0	Timer MSB Register
1	1	1	Timer LSB Register
X	X	X	ROM Address

Table 10. Composite Status Register

CSR7	CSR3-CSR6 NOT USED. DEFAULT TO ZERO WHEN READ	CSR2	CSR1	CSR0

COMPOSITE INTERRUPT FLAG
0 = NO ENABLED INTERRUPT FLAG SET
1 = ONE OR MORE ENABLED INTERRUPT FLAGS SET.

INVERSE OF THIS BIT APPEARS AT $\overline{IRQ}$ OUTPUT

STATUS OF THIS BIT CAN BE EXPRESSED AS:
CSR7 = CSR0 · TCR6 + CSR1 · PCR0 + CSR2 · PCR3

CP2 INTERRUPT FLAG
0 = NO INT REQ
1 = INT REQUESTED

TIMER INTERRUPT FLAG
0 = NO INT REQ
1 = INT REQUESTED

CP1 INTERRUPT
0 = NO INT REQ
1 = INT REQUESTED

Table 11. Timer Control Register

TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0

INTERRUP ENABLE
0 = $\overline{IRQ}$ MASKED
1 = $\overline{IRQ}$ ENABLED

INTERNAL RESET
0 = TIMER ENABLED
1 = RESET STATE

TIMER OUTPUT ENABLE
0 = OUTPUT DISABLED (LOW)
1 = OUTPUT ENABLED

CLOCK SOURCE
0 = EXTERNAL CLOCK (CTC)
1 = INTERNAL CLOCK (ϕ2)

FOR CASCADED SINGLE SHOT
0 = OUTPUT GOES LOW AT TIME OUT
1 = OUTPUT GOES HIGH AT TIME OUT

÷ 8 PRESCALE ENABLE
0 = CLOCK NOT PRESCALED
1 = CLOCK PRESCALED (÷ 8)

TCR5	TCR4	TCR3	TIMER OPERATING MODE	COUNTER INITIALIZATION	INTERRUPT FLAG SET
0	0	0	CONTINUOUS	$\overline{CTG}\downarrow$ + W + R	T.O.
0	0	1	CASCADED SINGLE SHOT	$\overline{CTG}\downarrow$ + R	T.O.
0	1	0	CONTINUOUS	$\overline{CTG}\downarrow$ + R	T.O.
0	1	1	NORMAL SINGLE SHOT	$\overline{CTG}\downarrow$ + R	T.O.
1	0	0	FREQUENCY COMPARISON	$\overline{CTG}\downarrow$ · I · (W + T.O.) + R	$\overline{CTG}\downarrow$ BEFORE T.O.
1	0	1		$\overline{CTG}\downarrow$ · I + R	T.O. BEFORE $\overline{CTG}\downarrow$
1	1	0	PULSE WIDTH COMPARISON	$\overline{CTG}\downarrow$ · I + R	$\overline{CTG}\uparrow$ BEFORE T.O.
1	1	1			T.O. BEFORE $\overline{CRG}\uparrow$

R = RESET CONDITION
W = WRITE TIMER LATCHES
T.O. = COUNTER TIME OUT

$\overline{CTG}\downarrow$ = NEG TRANSITION OF PIN 17
$\overline{CTG}\uparrow$ = POS TRANSITION OF PIN 17
I = INTERRUPT FLAG (CSR0) = 0

Table 12. Peripheral Control Register

PCR7	PCR6	PCR5	PCR4	PCR3	PCR2	PCR1	PCR0

CP2 DIRECTION CONTROL
0 = CP2 is INPUT
1 = CP2 is OUTPUT

CP1 INT. ENABLE
0 = CP1 INT. MASKED
1 = CP1 INT. ENABLED

RESET (SET BY EXT. RESET = 0 OR WRITING ONE INTO LOCATION: CLEARED BY WRITING ZERO TO THIS LOCATION)
0 = NORMAL OPERATION
1 = RESET CONDITION (CLEARS PERIPH DATA & DATA DIRECTION REG + CSR1 & CSR2)

CP1 ACTIVE EDGE SELECT
0 = NEGATIVE (↓) EDGE
1 = POSITIVE (↑) EDGE

CP1 INPUT LATCH CONTROL
0 = INPUT DATA NOT LATCHED
1 = INPUT DATA LATCHED ON ACTIVE CP1

CP2 is INPUT (PCR5 = 0)

PCR4	PCR3

CP2 ACTIVE EDGE SELECT
0 = NEGATIVE (↓) EDGE
1 = POSITIVE (↑) EDGE

CP2 INT. ENABLE
0 = CP2 INT. MASKED
1 = CP2 INT. ENABLED

PCR4	PCR3	CP2 IS OUTPUT (PCR5 = 1)
0	0	INTERRUPT ACKNOWLEDGE
0	1	INPUT/OUTPUT ACKNOWLEDGE
1	0 OR 1	PROGRAMMABLE OUTPUT (CP2 REFLECTS DATA WRITTEN INTO PCR3)

S6846 Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler/Loader. The format is as follows and may be on paper tape, punched card or other media readable by AMI. In addition the value for E_0, E_1, E_2* is required to program the mask.

ASCII

Character	Description
1	Start of record (S)
2	Type of record
	0 — Header record
	1 — Data record
	9 — End of file record
3 — 4	Byte Count

Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length being defined in each record by the byte count.

5, 6, 7, 8	Address Value

The memory location where this record is to be stored.

9, . . . , N	Data

Each data byte is represented by two hex characters. Most significant character first.

N + 1, N + 2	Checksum

The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

EXAMPLE:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 1 D
S 9 0 3 0 0 0 0 F C
```

START OF RECORD
TYPE OF RECORD
BYTE COUNT (HEX)
START ADDRESS
DATA
CHECK SUM

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
```

*Notes:
1. Only positive logic formats for E_0, E_1, E_2 are accepted. $1 = V_{HIGH}$; $0 = V_{LOW}$.
2. A "0" indicates the chip is enabled by a logic 0. A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should **not** be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

Package Dimensions

40-Pin Plastic

40-Pin Ceramic

S6800
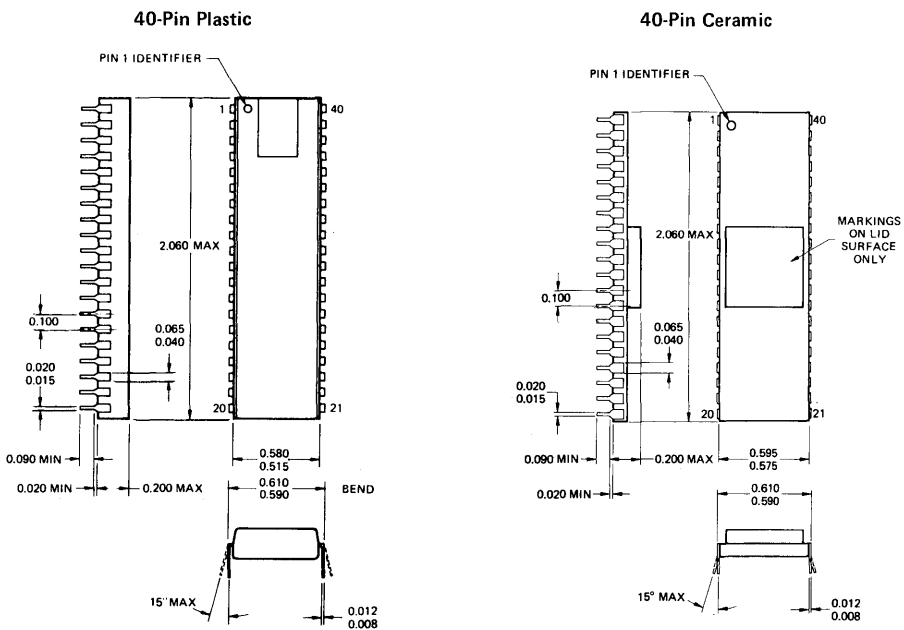
Ordering Information (see note)

Order No.	No. Pins	Package	Temp. Range	Description
S6846P	40	Plastic	0°C — +70°C	NMOS Combination ROM, I/O, Timer
S6846	40	Ceramic	0°C — +70°C	NMOS Combination ROM, I/O, Timer

Note: Because the S6846 has a ROM in chip for which the bit pattern is customer defined, the part marking will be S6846 — XXX where S6846 is the basic die and XXX is the customer bit pattern identification number. This number is issued at the time of ordering. Special part marking is also available upon request.

AMI®

ASYNCHRONOUS COMMUNICATION
INTERFACE ADAPTER (ACIA)

ADVANCE PRODUCT DESCRIPTION

Vcc = PIN 12
GROUND = PIN 1
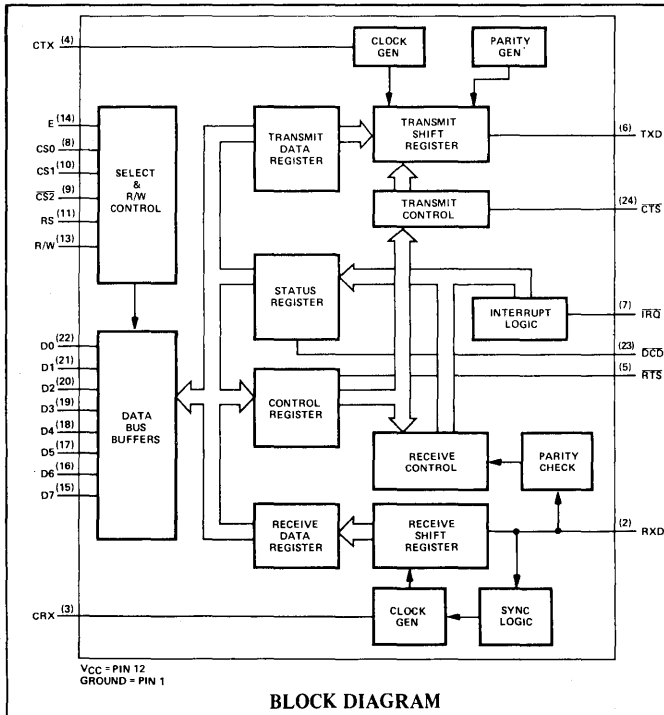
BLOCK DIAGRAM
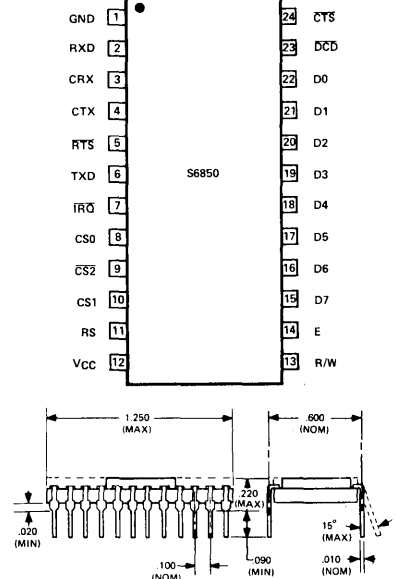
PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2L, 1W - see Sec. 1)

FEATURES

- 8 Bit Bidirectional Data Bus for Communication with MPU.

- False start bit deletion.

- Peripheral/modem control functions.

- Double buffered Receiver and Transmitter

- One or two stop bit operation.

- Eight and nine-bit transmission with optional even and odd parity.

- Parity, overrun and framing error checking.

- Programmable control register.

- Optional ÷1, ÷16, and ÷64 clock modes.

- Up to 500,000 bps transmission.

FUNCTIONAL DESCRIPTION

The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	−0.3 to +7.0V	Operating Temperature Range T_A	0 to +70°C
Input Voltage V_{in}	−0.3 to +7.0V	Storage Temperature Range T_{stg}	−55 to +150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS
(V_{CC} = 5.0V ± 5%, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.4	–	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	–	+0.4	Vdc
Input High Threshold Voltage All Inputs Except Enable	V_{IHT}	+2.0	–	–	Vdc
Input Low Threshold Voltage All Inputs Except Enable	V_{ILT}	–	–	+0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.0 Vdc) R/W, RS, CS0, CS1, $\overline{CS2}$, Enable	I_{in}	–	1.0	2.5	µAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) D0-D7,	I_{TSI}	–	2.0	10	µAdc
Output High Voltage (I_{Load} = −100 µAdc, Enable Pulse Width < 25 µs) All Outputs Except $\overline{IRQ}$	V_{OH}	+2.4	–	–	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc) Enable Pulse Width < 25 µs	V_{OL}	–	–	+0.4	Vdc
Output Leakage Current (Off State) $\overline{IRQ}$	I_{LOH}	–	1.0	10	µAdc
Power Dissipation	P_D	–	300	525	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) D0-D7 R/W, RS, CS0, CS1, $\overline{CS2}$, RXD, $\overline{CTS}$, $\overline{DCD}$, CTX, CRX Enable.	C_{in}	– – –	– – –	10 10	pF
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	10	pF

AC (DYNAMIC) CHARACTERISTICS

Loading = 130 pF and one TTL load for D0-D7 = 20pF and 1 TTL load for $\overline{RTS}$ and TXD = 100pF and 3KΩ to V_{CC} for $\overline{IRQ}$.

READ TIMING CHARACTERISTICS (Figure 1)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Setup Time, Address valid to Enable positive transition	T_{AEW}	180	—	—	ns
Setup Time, Enable positive transition to Data valid on bus	T_{EDR}	—	—	395	ns
Data Bus Hold Time	T_{HR}	10	—	—	ns
Rise and Fall Time for Enable input	t_{rE}, t_{fE}	—	—	25	μs

FIGURE 1 – READ TIMING CHARACTERISTICS
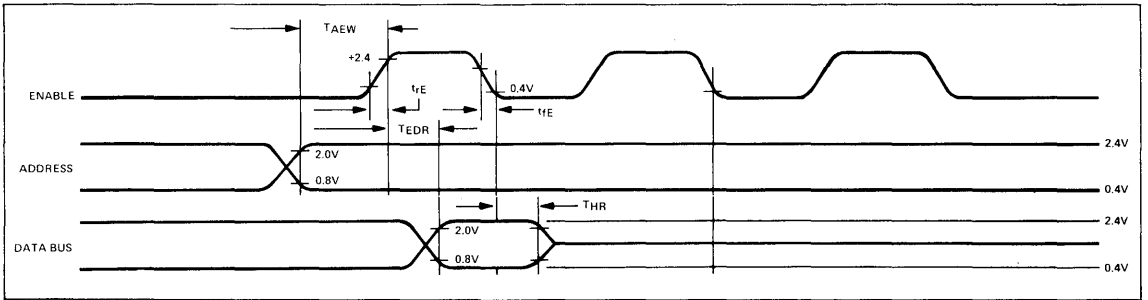
WRITE TIMING CHARACTERISTICS (Figure 2)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Enable Pulse Width	T_E	0.470	—	25	μs
Setup Time, Address valid to Enable positive transition	T_{AEW}	180	—	—	ns
Setup Time, Data valid to Enable netative transition	T_{DSU}	300	—	—	ns
Setup time, Read/Write negative transition to Enable positive transition	T_{WE}	130	—	—	ns
Data Bus Hold Time	T_{HW}	10	—	—	ns

FIGURE 2 – WRITE TIMING CHARACTERISTICS
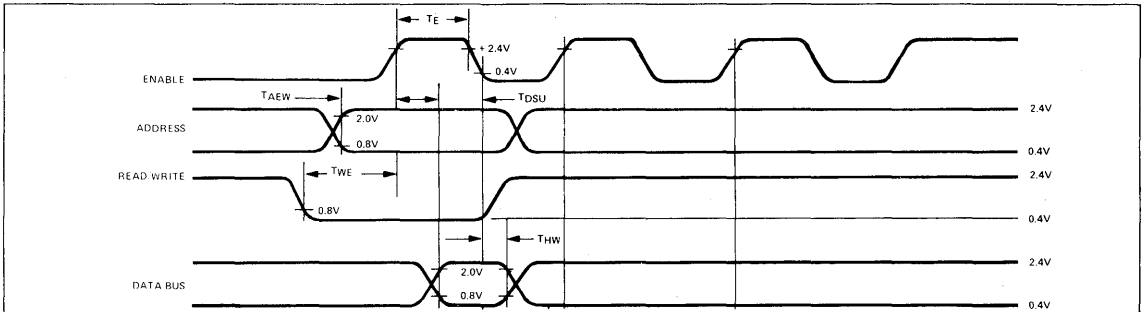
TRANSMIT/RECEIVE CHARACTERISTICS (Figure 3)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency ÷ 1 mode ÷ 16 mode ÷ 64 mode	f_C			500 800 800	KHz KHz KHz
Clock Pulse Width, Low State	PW_{CL}	600			nsec
Clock Pulse Width, High State	PW_{CH}	600			nsec
Delay Time, Transmit Clock to Data Out	T_{TDD}			1.0	μsec
Set up Time, Receive Data	T_{RDSU}	500			nsec
Hold Time, Receive Data	T_{RDH}	500			nsec
Delay Time, Enable to $\overline{IRQ}$ Reset	T_{IRQR}			1.2	μsec
Delay Time, Enable to $\overline{RTS}$	T_{RTS}			1.0	μsec

FIGURE 3 – TRANSMIT/RECEIVE TIMING

MPU/ACIA INTERFACE

Pin	Label	FUNCTION
(22)	D0	**ACIA BI-DIRECTIONAL DATA LINES**–The bi-directional data lines (D0-D7) allow for
(21)	D1	data transfer between the ACIA and the MPU. The data bus output drivers are three-state
(20)	D2	devices that remain in the high-impedance (off) state except when the MPU performs an
(19)	D3	ACIA read operation. The Read/Write line is in the read (high) state when the ACIA is
(18)	D4	selected for a read operation.
(17)	D5	
(16)	D6	
(15)	D7	
(14)	E	**ACIA ENABLE SIGNAL**–The Enable signal (E) is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the S6800 $\phi2$ clock.
(13)	R/W	**READ/WRITE CONTROL SIGNAL**–The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), the ACIA output driver is turned on and a selected register is read. When it is low, the ACIA output driver is turned off and the MPU writes into a selected register. Thus, the Read/Write signal is used to select the Read Only or Write Only registers within the ACIA.
(8)	CS0	
(10)	CS1	
(9)	$\overline{CS2}$	**CHIP SELECT SIGNALS**–These three high impedance TTL compatible input lines are used to address an ACIA. A particular ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from ACIA are then performed under the control of Enable, Read/Write, and Register Select.
(11)	RS	**REGISTER SELECT SIGNAL**–The Register Select line is a high impedance input that is TTL compatible and is used to select the Transmit/Receive Data or Control/Status registers in the ACIA. The Read/Write signal line is used in conjunction with Register Select to select the Read Only or Write Only register in each register pair.
(7)	$\overline{IRQ}$	**INTERRUPT REQUEST SIGNAL**–Interrupt request is a TTL compatible, open drain active low output that is used to interrupt the MPU. The Interrupt Request remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

ACIA/MODEM OR PERIPHERAL INTERFACE

Pin	Label	FUNCTION
(4)	CTX	**TRANSMIT CLOCK**–The Transmit Clock is a high impedance TTL compatible input used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.

Pin	Label	FUNCTION
(3)	CRX	**RECEIVE CLOCK**—The Receive Clock is a high impedance TTL compatible input used for synchronization of received data. (In the $\div$ 1 mode, the clock and data must be synchronized externally.) The receiver strobes the data on the positive transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(2)	RXD	**RECEIVED DATA**—The Received Data line is a high impedance TTL compatible input through which data is received in a serial NRZ(Non Return to Zero) format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 Kbps when external synchronization is utilized.
(6)	TXD	**TRANSMIT DATA**—The Transmit Data output line transfers serial NRZ data to a modem or other peripheral device. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.
(24)	$\overline{\text{CTS}}$	**CLEAR-TO-SEND**—This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem's "clear-to-send" active low output by inhibiting the Transmitter Data Register Empty status bit (TDRE).
(5)	$\overline{\text{RTS}}$	**REQUEST-TO-SEND**—The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The active state is low. The Request-to-Send output is controlled by the contents of the ACIA control register.
(23)	$\overline{\text{DCD}}$	**DATA CARRIER DETECTED**—This high impedance TTL compatible input provides automatic control of the receiving end of a communications link by means of the modem "Data-Carrier-Detect" or "Received-Line-Signal Detect" output. The $\overline{\text{DCD}}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receiver Interrupt Enable (RIE) is set.
(12)	V$_{CC}$	**+5 volts $\pm$ 5%**
(1)	GND	**GROUND**

APPLICATION INFORMATION

INTERNAL REGISTERS—The ACIA has four internal registers utilized for status, control, receiving data, and transmitting data. The register addressing by the R/W and RS lines and the bit definitions for each register are shown in Figure 4.

FIGURE 4 – DEFINITION OF ACIA REGISTERS

	BUFFER ADDRESS			
	RS • $\overline{\text{R/W}}$	RS • R/W	$\overline{\text{RS}}$ • $\overline{\text{R/W}}$	$\overline{\text{RS}}$ • R/W
Data Bus Line Number	Transmit Data Register	Receiver Date Register	Control Register	Status Register
	(Write Only)	(Read Only)	(Write Only)	(Read Only)
0	Data Bit 0*	Data Bit 0*	Clk. Divide Sel. 1 (CR0)	Rx Data Reg. Full (RDRF)
1	Data Bit 1	Data Bit 1	Clk. Divide Sel. 2 (CR1)	Tx Data Reg. Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Sel. 1 (CR2)	Data Carrier Det. ($\overline{\text{DCD}}$)
3	Data Bit 3	Data Bit 3	Word Sel. 2 (CR3)	Clear-to-Send ($\overline{\text{CTS}}$)
4	Data Bit 4	Data Bit 4	Word Sel. 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Tx Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Tx Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Rx Interrupt. Enable (CR7)	Interrupt Request (IRQ)

Notes:
*   Leading bit = LSB = Bit 0
** Unused data bits in received character will be "0's."
*** Unused data bits for transmission are "don't care's."

ACIA STATUS REGISTER—Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This Read Only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of: transmitting data register, the receiving data register and error status and the modem status inputs of the ACIA.

Receiver Data Register Full (RDRF) [Bit 0] — Receiver Data Register Full indicates that received data has been transferred to the Receiver Data Register. RDRF is cleared after an MPU read of the Receiver Data Register or by a Master Reset. The cleared or empty state indicates that the contents of the Receiver Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE) [Bit 1]—The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{\text{DCD}}$) [Bit 2] — The Data Carrier Detect bit will be high when the $\overline{\text{DCD}}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated if the Receiver Interrupt Enable (RIE) is set. It remains high until the interrupt is cleared by reading the Status Register and the data register or a Master Reset occurs. If the $\overline{\text{DCD}}$ input remains high after Read Status and Read Data or Master Reset have occurred, the $\overline{\text{DCD}}$ Status bit remains high and will follow the $\overline{\text{DCD}}$ input.

Clear-to-Send ($\overline{\text{CTS}}$) [Bit 3] — The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{\text{CTS}}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master Reset does not affect the Clear-to-Send status bit.

Framing Error (FE) [Bit 4] — Framing error indicates that the received character is improperly framed by the start and stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receiver data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN) [Bit 5] — Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receiver Data Register

(RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until Overrun is reset. Character synchronization is maintained during the Overrun condition. The overrun indication is reset after the reading of data from the Receive Data Register. Overrun is also reset by the Master Reset.

Parity Error (PE) [Bit 6]—The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{\text{IRQ}}$) [Bit 7]—The IRQ bit indicates the state of the $\overline{\text{IRQ}}$ output. Any interrupt that is set and enabled will be indicated in the status register. Any time the $\overline{\text{IRQ}}$ output is low the IRQ bit will be high to indicate the interrupt or service request status.

CONTROL REGISTER—The ACIA control Register consists of eight bits of write only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send modem control output.

Counter Divide Select Bits (CR0 and CR1)—The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a Master Reset for the ACIA which clears the Status Register and initializes both the receiver and transmitter. Note that after a power-on or a power-fail restart, these bits must be set High to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	$\div 1$
0	1	$\div 16$
1	0	$\div 64$
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4)–The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bit
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not double-buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6)–Two Transmitter Control bits provide for the control of the Transmitter Buffer Empty interrupt output, the Request-to-Send output and the transmission of a BREAK level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled
1	1	$\overline{RTS}$ = low, Transmitting Interrupt Disabled and Transmits a BREAK level on the Transmit Data Output.

Receiver Interrupt Enable Bit (RIE) (CR7)–Interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Interrupts caused by the Receiver Data Register Full being high or by a low to high transition on the Data Carrier Detect signal line are enabled or disabled by the Receiver Interrupt Enable Bit.

TRANSMIT DATA REGISTER (TDR)–Data is written in the Transmit Data Register *during* the peripheral enable time (E) when the ACIA has been addressed and RS • R/W is selected. Writing data into the register causes the Transmit Data Register Empty bit in the status register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)–Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receiver Data Register Full bit (RDRF) (in the status buffer) to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receiver Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receiver Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

OPERATIONAL DESCRIPTION

From the MPU Bus interface the ACIA appears as two addressable RAM memory locations. Internally, there are four registers; two read-only and two write-only registers. The read-only registers are status and receive data, and the write only registers are control and transmit data. The serial interface consists of serial transmit and receive lines and three modem/peripheral control lines.

During a power-on sequence, the ACIA is internally latched in a reset condition to prevent erroneous output transitions. This power-on reset latch can only be released by the master reset function via the control register; bits b_0 and b_1 are set "high" for a master reset. After master resetting the ACIA, the programmable control register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none) and etc.

TRANSMITTER–A typical transmitting sequence consists of reading the ACIA status register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmitter Data Register if the status read operation has indicated that the Transmit Data

Register is empty. This character is transferred to a shift register where it is serialized and transmitted from the Tx Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the data register, the status register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted. This second character will be automatically transferred into the shift register when the first character transmission is completed. The above sequence continues until all the characters have been transmitted.

RECEIVER—Data is received from a peripheral by means of the Rx Data input. A divide by one clock ratio is provided for an externally synchronized clock (to its data) while the divide by 16 and 64 ratios are provided for internal synchronization.

Bit synchronization in the divide by 16 and 64 modes is obtained by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the status register along with framing error, overrun error, and receiver data register full. In a typical receiving sequence, the status register is read to determine if a character has been received from a peripheral. If the receiver data register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. The status register can be read again to determine if another character is available in the receiver data register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

AMI®

ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER (ACIA)

Features

☐ 8 Bit Bidirectional Data Bus for Communication with MPU

☐ False Start Bit Deletion

☐ Peripheral/Modem Control Functions

☐ Double Buffered Receiver and Transmitter

☐ One or Two Stop Bit Operation

☐ Eight and Nine-Bit Transmission with Optional Even and Odd Parity

☐ Parity, Overrun and Framing Error Checking

☐ Programmable Control Register

☐ Optional ÷1, ÷16, and ÷64 Clock Modes

☐ Up to 500,000 bps Transmission

General Description

The S68A50/S68B50 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S68A00/S68B00 Microprocessing Units.

The S68A50/S68B50 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided.

Block Diagram

Pin Configuration

3.98

Absolute Maximum Ratings

Supply Voltage	$-0.3V$ to $+7.0V$
Input Voltage	$-0.3V$ to $+7.0V$
Operating Temperature Range	$0°C$ to $+70°C$
Storage Temperature Range	$-55°C$ to $+150°C$

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage (normal operating level)	$V_{SS}+2.0$		V_{CC}	Vdc	
V_{IL}	Input Low Voltage (normal operating level)	$V_{SS}-0.3$		$V_{SS}+0.8$	Vdc	
I_{IN}	Input Leakage Current R/W, ES, CS0, CS1, $\overline{CS2}$, Enable		1.0	2.5	μAdc	V_{IN} = 0Vdc to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current D0-D7		2.0	10	μAdc	V_{IN} = 0.4Vdc to 2.4Vdc
V_{OH}	Output High Voltage (all outputs except IRQ) D0-D7	$V_{SS}+2.4$			Vdc	I_{LOAD} = -205μAdc, Enable Pulse Width <25μs
	Tx Data, $\overline{RTS}$	$V_{SS}+2.4$			Vdc	I_{LOAD} = -100μAdc, Enable Pulse Width <25μs
V_{OL}	Output Low Voltage (Enable pulse width < 25μs)			$V_{SS}+0.4$	Vdc	I_{LOAD} = 1.6mAdc, Enable Pulse Width <25μs
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation		300	525	mW	
C_{IN}	Input Capacitance D0-D7		10	12.5	pF	
	E,Tx,CLK,Rx Clk,R/W,RS,Rx Data, CS0,$\overline{CS1}$,$\overline{CS2}$,RXD,CTS,$\overline{DCD}$,CTX,CRX		7.0	7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
C_{OUT}	Output Capacitance $\overline{RTS}$,Tx Data			10	pF	
	$\overline{IRQ}$			5.0	pF	
PW_{CL}	Minimum Clock Pulse Width, Low ÷16, ÷64 Modes	600			ns	
PW_{CH}	Minimum Clock Pulse Width, High ÷16, ÷64 Modes	600			ns	
f_C	Clock Frequency ÷1 Mode			500	kHz	
	÷16, ÷64 Modes			800	kHz	
t_{TDD}	Clock-to-Data Delay for Transmitter			1.0	μs	
t_{RDSU}	Receive Data Setup Time ÷1 Mode	500			ns	
t_{RDH}	Receive Data Hold Time ÷1 Mode	500			ns	
t_{IR}	Interrupt Request Release Time			1.2	μs	
t_{RTS}	Request-to-Send Delay Time			1.0	μs	
t_r,t_f	Input Transition Times (Except Enable)			1.0*	μs	

*1.0μ or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Read

Symbol	Parameter	S68A50		S68B50		Units
		Min.	Max.	Min.	Max.	
t_{cycF}	Enable Cycle Time	0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.28	25	0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	140		70		ns
t_{DDR}	Data Delay Time		220		180	ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25	ns

Write

Symbol	Parameter	S68A50		S68B50		Units
		Min.	Max.	Min.	Max.	
t_{cycE}	Enable Cycle Time	0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.28	25	0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	140		70		ns
t_{DSW}	Data Setup Time	80		60		ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Fr}, t_{Ef}	Rise and Fall Time for Enable Input		25		25	ns

Figure 1. Clock Pulse Width, Low State
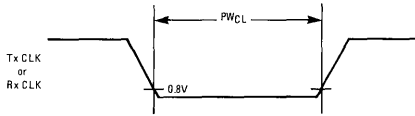
Tx CLK or Rx CLK — PW_{CL}, 0.8V

Figure 2. Clock Pulse Width, High State

Tx CLK or Rx CLK — 2.0V, PW_{CH}

Figure 3. Transmit Data Output Delay

Tx CLK — 0.8V, t_{TDD}
Tx DATA — 2.4V, 0.4V
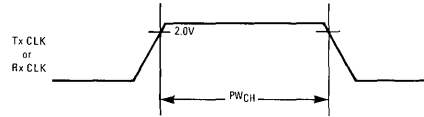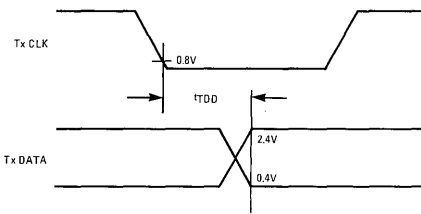
Figure 4. Receive Data Setup Time (÷1 Mode)

Rx DATA — 2.0V, 0.8V, t_{RDSU}
Rx CLOCK — 0.8V
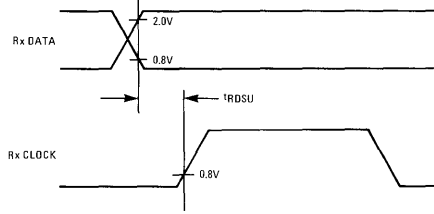
Figure 5. Receive Data Hold Time (÷1 Mode)

Rx CLK — 2.0V, t_{RDH}
Rx DATA — 2.0V, 0.8V

Figure 6. Request-to Send Delay and Interrupt-Request Release Times

ENABLE — 0.8V, t_{RTS}
$\overline{RTS}$ — 2.4V, 0.4V, t_{IR}
$\overline{IRQ}$ — 2.4V
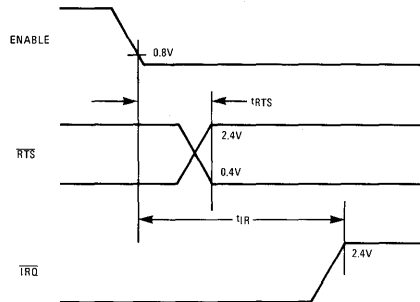
Figure 7. Bus Read Timing Characteristics (Read Information from ACIA)

ENABLE — t_{AS}, PW_{EH}, PW_{EL}, t_{cycE}, 2.0V, 0.8V, t_{Er}, t_{Ef}, t_{DDR}
RS, CS, R/W — 2.0V, 0.8V
DATA BUS — 2.4V, 0.4V, t_{AH}, t_{H}
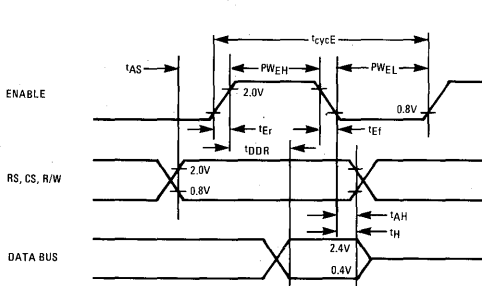
Figure 8. Bus Write Timing Characteristics (Write Information into ACIA)

ENABLE — t_{AS}, PW_{EH}, PW_{EL}, t_{cycE}, 2.0V, 0.8V, t_{Er}, t_{Ef}, t_{DSW}
RS, CS, R/W — 2.0V, 0.8V
DATA BUS — 2.0V, 0.8V, t_{AH}, t_{H}

S6800

Bus Timing Test Loads

LOAD A
(D0-D7, RTS, Tx DATA)

LOAD B
(IRQ ONLY)

5.0V

R_L = 2.5k

TEST POINT

MMD6150
OR EQUIV.

C

R

MMD7000
OR EQUIV.

5.0V

3k

TEST POINT

100pF

C = 130pF FOR D0-D7
= 30pF FOR RTS AND Tx DATA

R = 11.7kΩ FOR D0-D7
= 24kΩ FOR RTS AND Tx DATA

877251

Expanded Block Diagram

TRANSMIT CLOCK 4

ENABLE 14

READ/WRITE 13
CHIP SELECT 0 8
CHIP SELECT 1 10
CHIP SELECT 2 9
REGISTER SELECT 11

CHIP
SELECT
AND
READ/WRITE
CONTROL

CLOCK
GEN

PARITY
GEN

TRANSMIT
DATA
REGISTER

TRANSMIT
SHIFT
REGISTER

6 TRANSMIT DATA

TRANSMIT
CONTROL

24 CLEAR-TO-SEND

D0 22
D1 21
D2 20
D3 19
D4 18
D5 17
D6 16
D7 15

DATA
BUS
BUFFERS

STATUS
REGISTER

INTERRUPT
LOGIC

7 INTERRUPT REQUEST

23 DATA CARRIER DETECT

CONTROL
REGISTER

5 REQUEST-TO-SEND

RECEIVE
CONTROL

PARITY
CHECK

V_{DD} = PIN 12
V_{SS} = PIN 1

RECEIVE
DATA
REGISTER

RECEIVE
SHIFT
REGISTER

2 RECEIVE DATA

CLOCK
GEN

SYNC
LOGIC

RECEIVE CLOCK 3

877252

3.102

MPU/ACIA Interface

Pin	Label	Function
(22)	D0	**ACIA Bidirectional Data Lines** — The bidirectional data lines (D0-D7) allow for data
(21)	D1	transfer between the ACIA and the MPU. The data bus output drivers are three-state
(20)	D2	devices that remain in the high impedance (off) state except when the MPU performs
(19)	D3	an ACIA read operation. The Read/Write line is in the read (high) state when the ACIA
(18)	D4	is selected for a read operation.
(17)	D5	
(16)	D6	
(15)	D7	

(14)   E   **ACIA Enable Signal** — The Enable signal (E) is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the S6800 $\phi2$ clock.

(13)   R/W   **Read/Write Control Signal** — The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), the ACIA output driver is turned on and a selected register is read. When it is low, the ACIA output driver is turned off and the MPU writes into a selected register. Thus, the Read/Write signal is used to select the Read Only or Write Only registers within the ACIA.

(8)   CS0   **Chip Select Signals** — These three high impedance TTL compatible input lines are used
(10)   CS1   to address an ACIA. A particular ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$
(9) $\overline{CS2}$ is low. Transfers of data to and from ACIA are then performed under the control of Enable, Read/Write and Register Select.

(11)   RS   **Register Select Signal** — The Register Select line is a high impedance input that is TTL compatible and is used to select the Transmit/Receive Data or Control/Status registers in the ACIA. The Read/Write signal line is used in conjunction with Register Select to select the Read Only or Write Only register in each register pair.

(7) $\overline{IRQ}$ **Interrupt Request Signal** — Interrupt request is a TTL compatible, open drain active low output that is used to interrupt the MPU. The Interrupt Request remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

S6800

ACIA/Modem or Peripheral Interface

Pin	Label	Function
(4)	CTX	**Transmit Clock** — The Transmit Clock is a high impedance TTL compatible input used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(3)	CRX	**Receive Clock** — The Receive Clock is a high impedance TTL compatible input used for synchronization of received data. (In the ÷1 mode, the clock and data must be synchronized externally.) The receiver strobes the data on the positive transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(2)	RXD	**Received Data** — The Received Data line is a high impedance TTL compatible input through which data is received in a serial NRZ (Non Return to Zero) format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.
(6)	TXD	**Transmit Data** — The Transmit Data output line transfers serial NRZ data to a modem or other peripheral device. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.
(24)	$\overline{\text{CTS}}$	**Clear-to-Send** — This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem's "clear-to-send" active low output by inhibiting the Transmitter Data Register Empty status bit (TDRE).
(5)	$\overline{\text{RTS}}$	**Request-to-Send** — The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The active state is low. The Request-to-Send output is controlled by the contents of the ACIA control register.
(23)	$\overline{\text{DCD}}$	**Data Carrier Detected** — This high impedance TTL compatible input provides automatic control of the receiving end of a communications link by means of the modem "Data-Carrier-Detect" or "Received-Line-Signal Detect" output. The $\overline{\text{DCD}}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receiver Interrupt Enable (RIE) is set.
(12)	V_{CC}	+5volts ±5%
(1)	GND	Ground

Application Information

Internal Registers — The ACIA has four internal registers utilized for status, control, receiving data and transmitting data. The register addressing by the R/W and RS lines and the bit definitions for each register are shown in Figure 4.

Figure 4 — Definition of ACIA Registers

Data Bus Line Number	Buffer Address			
	RS • $\overline{\text{R/W}}$ Transmit Data Register (Write Only)	RS • R/W Received Data Register (Read Only)	$\overline{\text{RS}}$ • $\overline{\text{R/W}}$ Control Register (Write Only)	$\overline{\text{RS}}$ • R/W Status Register (Read Only)
0	Data Bit 0*	Data Bit 0*	Clk. Divide Sel. (CR0)	Rx Data Reg. Full (RDRF)
1	Data Bit 1	Data Bit 1	Clk. Divide Sel. (CR1)	Tx Data Reg. Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Sel. 1 (CR2)	Data Carrier Det. Loss ($\overline{\text{DCD}}$)
3	Data Bit 3	Data Bit 3	Word Sel. 2 (CR3)	Clear-to-Send (CTS)
4	Data Bit 4	Data Bit 4	Word Sel. 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Tx Control 1 (CR5)	Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Tx Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Rx Interrupt Enable (CR7)	Interrupt Request (IRQ)

Notes:
*   Leading bit = LSB = Bit 0
**   Unused data bits in received character will be "0's"
***   Unused data bits for transmission are "don't care's"

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ACIA Status Register — Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This Read Only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of: transmitting data register, the receiving data register and error status and the modem status inputs of the ACIA.

Receiver Data Register Full (RDRF) [Bit 0] — Receiver Data Register Full indicates that received data has been transferred to the Receiver Data Register. RDRF is cleared after an MPU read of the Receiver Data Register or by a Master Reset. The cleared or empty state indicates that the contents of the Receiver Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE) [Bit 1] — The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{\text{DCD}}$) [Bit 2] — The Data Carrier Detect bit will be high when the $\overline{\text{DCD}}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated if the Receiver Interrupt Enable (RIE) is set. It remains high until the interrupt is cleared by reading the Status Register and the data register or a Master Reset occurs. If the $\overline{\text{DCD}}$ input remains high after Read Status and Read Data or Master Reset have occurred, the $\overline{\text{DCD}}$ Status bit remains high and will follow the $\overline{\text{DCD}}$ input.

Clear-to-Send ($\overline{\text{CTS}}$) [Bit 3] — The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{\text{CTS}}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master Reset does not affect the Clear-to-Send status bit.

Framing Error (FE) [Bit 4] — Framing error indicates that the received character is improperly framed by the start and stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receiver data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN) [Bit 5] — Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receiver Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until Overrun is reset. Character synchronization is maintained during the Overrun condition. The overrun indication is reset after the reading of data from the Receiver Data Register. Overrun is also reset by the Master Reset.

Parity Error (PE) [Bit 6] — The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{\text{IRQ}}$) [Bit 7] — The IRQ bit indicates the state of the $\overline{\text{IRQ}}$ output. Any interrupt that is set and enabled will be indicated in the status register. Any time the $\overline{\text{IRQ}}$ output is low the IRQ bit will be high to indicate the interrupt or service request status.

Control Register — The ACIA Control Register consists of eight bits of write only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send modem control output.

Counter Divide Select Bits (CR0 and CR1) — The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a Master Reset for the ACIA which clears the Status Register and initializes both the receiver and transmitter. Note that after a power-on or a power-fail restart, these bits must be set High to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) — The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not double-buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) — Two Transmitter Control bits provide for the control of the Transmitter Buffer Empty interrupt output, the Request-to-Send output and the transmission of a BREAK level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled
1	1	$\overline{RTS}$ = low, Transmitting Interrupt Disabled and Transmits a BREAK level on the Transmit Data Output.

Receiver Interrupt Enable Bit (RIE) (CR7) — The Interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Interrupts caused by the Receiver Data Register Full being high or by a low to high transition on the Data Carrier Detect signal line are enabled or disabled by the Receiver Interrupt Enable Bit.

Transmit Data Register (TDR) — Data is written in the Transmit Data Register *during* the peripheral enable time (E) when the ACIA has been addressed and RS • R/W is selected. Writing data into the register causes the Transmit Data Register Empty bit in the status register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

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Receive Data Register (RDR) — Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receiver Data Register Full bit (RDRF) (in the status buffer) to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receiver Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receiver Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

Operational Description

From the MPU Bus interface the ACIA appears as two addressable RAM memory locations. Internally, there are four registers; two read-only and two write-only registers. The read-only registers are status and receive data, and the write-only registers are control and transmit data. The serial interface consists of serial transmit and receive lines and three modem/peripheral control lines.

During a power-on sequence, the ACIA is internally latched in a reset condition to prevent erroneous output transitions. This power-on reset latch can only be released by the master reset function via the control register: bits b_0 and b_1 are set "high" for a master reset. After master resetting the ACIA, the programmable control register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none) and etc.

Transmitter — A typical transmitting sequence consists of reading the ACIA status register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmitter Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a shift register where it is serialized and transmitted from the Tx Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the data register, the status register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted. This second character will be automatically transferred into the shift register when the first character transmission is completed. The above sequence continues until all the characters have been transmitted.

Receiver — Data is received from a peripheral by means of the Rx Data input. A divide by one clock ratio is provided for an externally synchronized clock (to its data) while the divide by 16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide by 16 and 64 modes is obtained by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the status register along with framing error, overrun error, and receiver data register full. In a typical receiving sequence, the status register is read to determine if a character has been received from a peripheral. If the receiver data register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. The status register can be read again to determine if another character is available in the receiver data register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

AMI®

SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

Features

- ☐ Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- ☐ Character Synchronization on One or Two Sync Codes
- ☐ External Synchronization Available for Parallel-Serial Operation
- ☐ Programmable Sync Code Register
- ☐ Up to 600kbps Transmission
- ☐ Peripheral/Modem Control Functions
- ☐ Three Bytes of FIFO Buffering on Both Transmit and Receive
- ☐ Seven, Eight, or Nine Bit Transmission
- ☐ Optional Even and Odd Parity
- ☐ Parity, Overrun, and Underflow Status

General Description

The S6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the S6800 Microprocessor systems.

The bus interface of the S6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

S6800

Block Diagram

Pin Configuration

1	V_{SS}	CTS	24
2	Rx DATA	DCD	23
3	Rx Clk	D0	22
4	Tx Clk	D1	21
5	SM/$\overline{DTR}$	D2	20
6	Tx DATA	D3	19
7	$\overline{IRQ}$ S6852	D4	18
8	TUF	D5	17
9	$\overline{RESET}$	D6	16
10	$\overline{CS}$	D7	15
11	RS	E	14
12	V_{DD}	R/W	13

Maximum Ratings

Supply Voltage .... − 0.3V to +7.0V
Input Voltage .... − 0.3V to +7.0V
Operating Temperature Range .... 0°C to +70°C
Storage Temperature Range .... − 55°C to +150°C
Thermal Resistance .... +70°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage		V_{SS} + 2.0			Vdc	
V_{IL}	Input Low Voltage				V_{SS} + 0.8	Vdc	
I_{in}	Input Leakage Current	Tx Clk, Rx Clk, Rx Data, Enable, $\overline{Reset}$, RS, R/W, $\overline{CS}$, $\overline{DCD}$, $\overline{CTS}$		1.0	2.5	μAdc	V_{in} = 0Vdc to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current	D0-D7		2.0	10	μAdc	V_{in} = 0.4Vdc to 2.4Vdc, V_{CC} = 5.25Vdc
V_{OH}	Output High Voltage	D0-D7	V_{SS} + 2.4			Vdc	I_{Load} = − 205μAdc, Enable Pulse Width <25μs
		Tx Data, $\overline{DTR}$, TUF	V_{SS} + 2.4				I_{Load} = − 100μAdc, Enable Pulse Width <25μs
V_{OL}	Output Low Voltage				V_{SS} + 0.4	Vdc	I_{Load} = 1.6mAdc, Enable Pulse Width <25μs
I_{LOH}	Output Leakage Current (Off State)	$\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation			300	525	mW	
C_{in}	Input Capacitance	D0-D7			12.5	pF	V_{in} = 0, T_A = 25°C, f = 1.0MHz
		Other Inputs			7.5		
C_{out}	Output Capacitance	Tx Data, SM/$\overline{DTR}$, TUF, $\overline{IRQ}$			10	pF	V_{in} = 0, T_A = 25°C, f = 1.0MHz
					5.0		
PW_{CL}	Minimum Clock Pulse Width, Low		700			ns	Figure 1
PW_{CH}	Minimum Clock Pulse Width, High		700			ns	Figure 2
f_C	Clock Frequency				600	kHz	
t_{RDSU}	Receive Data Setup Time		350			ns	Figure 3, 7
t_{RDH}	Receive Data Hold Time		350			ns	Figure 3
t_{SM}	Sync Match Delay Time				1.0	μs	Figure 3
t_{TDD}	Clock-to-Data Delay for Transmitter				1.0	μs	Figure 4
t_{TUF}	Transmitter Underflow				1.0	μs	Figure 4, 6
t_{DTR}	$\overline{DTR}$ Delay Time				1.0	μs	Figure 5
t_{IR}	Interrupt Request Release Time				1.2	μs	Figure 5
t_{Res}	$\overline{Reset}$ Minimum Pulse Width		1.0			μs	
t_{CTS}	$\overline{CTS}$ Setup Time				200	ns	Figure 6
t_{DCD}	$\overline{DCD}$ Setup Time				500	ns	Figure 7
t_r, t_f	Input Rise and Fall Times (except Enable)				1.0*	μs	0.8V to 2.0V

*1.0μs or 10% of the pulse width, whichever is smaller.

Figure 1. Clock Pulse Width, Low-State
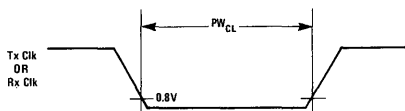
Figure 2. Clock Pulse Width, High-State
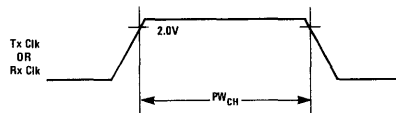
Bus Timing Characteristics

Read

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{cycE}	Enable Cycle Time	1.0			μs	
PW_{EH}	Enable Pulse Width, High	0.45		25	μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, Address and R/W valid to Enable positive transition	160			ns	Figures 8 and 10
t_{DDR}	Data Delay Time			320	ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input			25	ns	

Write

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{cycE}	Enable Cycle Time	1.0			μs	
PW_{EH}	Enable Pulse Width, High	0.45		25	μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, Address and R/W valid to Enable positive transition	160			ns	Figures 9 and 10
t_{DSW}	Data Setup Time	195			ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input			25	ns	

Figure 3. Receive Data Setup and Hold Times and Sync Delay Time

3.111

Figure 4. Transmit Data Output Delay and Transmitter Underflow Delay Time

n = NUMBER OF BITS IN CHARACTER
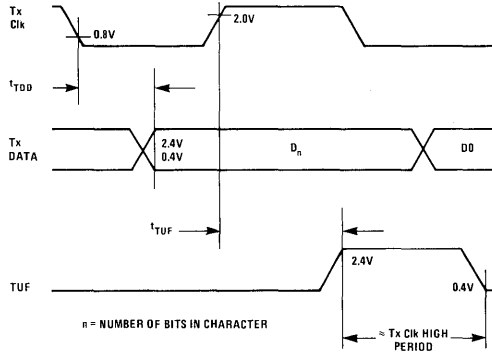
Figure 5. Data Terminal Ready and Interrupt Request Release Times
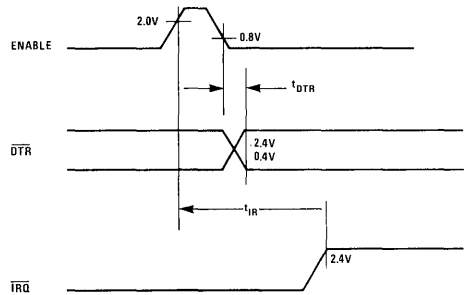
Figure 6. Clear-To-Send Setup Time
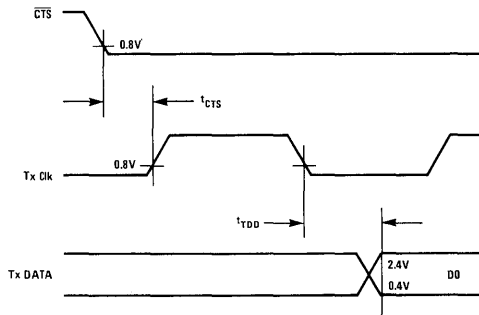
Figure 7. Data Carrier Detect Setup Time
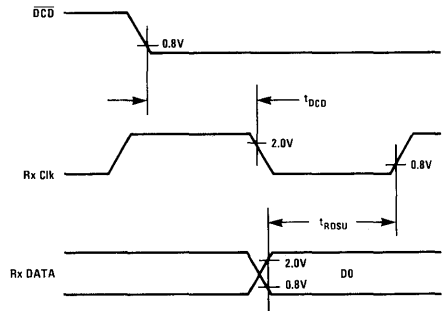
Figure 8. Bus Read Timing Characteristics (Read Information from SSDA)
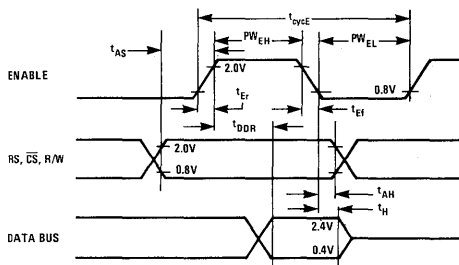
Figure 9. Bus Write Timing Characteristics (Write Information into SSDA)
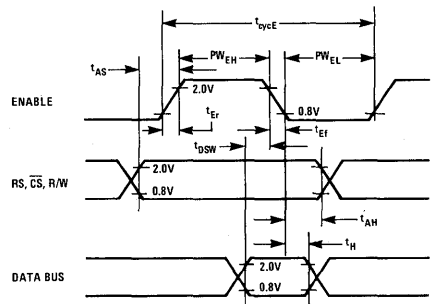
Figure 10. Bus Timing Test Loads

LOAD A
(DO-D7, DTR, Tx DATA, TUF)

LOAD B
(IRQ ONLY)

TEST POINT

5.0V

R_L = 2.5k

MMD6150
OR EQUIV.

MMD7000
OR EQUIV.

C

R

TEST POINT

5.0V

3k

100pF

C = 130pF FOR DO-D7
= 30pF FOR DTR, Tx DATA, AND TUF

R = 11.7kΩ FOR DO-D7
= 24kΩ FOR DTR, Tx DATA, AND TUF

Expanded Block Diagram

ENABLE 14

READ/WRITE 13

CHIP SELECT 10

REGISTER SELECT 11

ADDRESS
LOGIC

TRANSMIT CLOCK 4

PARITY
GENERATOR

TRANSMIT
DATA FIFO
REGISTER
(3 BYTES)
#1

#2

#3

TRANSMITTER
SHIFT
REGISTER

6 TRANSMIT
DATA

8 TRANSMITTER
UNDERFLOW

TRANSMIT
CONTROL

24 CLEAR-TO-SEND

23 DATA CARRIER
DETECT

D0 22

D1 21

D2 20

D3 19

D4 18

D5 17

D6 16

D7 15

DATA
BUS
BUFFERS

STATUS
REGISTER

INTERRUPT
LOGIC

7 INTERRUPT
REQUEST

RESET 9

CONTROL
REGISTER
1

CONTROL
REGISTER
3

CONTROL
REGISTER
2

RECEIVE
CONTROL

PARITY
CHECK

V_{DD} = PIN 12
V_{SS} = PIN 1

RECEIVE
DATA FIFO
REGISTER
(3 BYTES)
#1

#2

#3

SYNC
CODE
REGISTER

RECEIVER
SHIFT
REGISTER

COMPARATOR

COMPARE
LOGIC

2 RECEIVE
DATA

3 RECEIVE
CLOCK

5 SYNC
MATCH/
DATA TERMINAL
READY

Device Operation

At the bus interface, the SSDA appears as two addressable memory locations. Internally, there are seven registers: two read-only and five write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control 1, Control 2, Control 3, Sync Code and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and four peripheral/modem control lines.

Data to be transmitted is transferred directly into the 3-byte Transmit Data First-In First-Out (FIFO) Register from the data bus. Availability of the input to the FIFO is indicated by a bit in the Status Register; once data is entered, it moves through the FIFO to the last empty location. Data at the output of the FIFO is automatically transferred from the FIFO to the Transmitter Shift Register as the shift register becomes available to transmit the next character. If data is not available from the FIFO (underflow condition), the Transmitter Shift Register is automatically loaded with either a sync code or an all "1"s character. The transmit section may be programmed to append loaded with either a sync code or an all "1"s character. The transmit section may be programmed to append even, odd, or no parity to the transmitted word. An external control line (Clear-to-Send) is provided to inhibit the transmitter without clearing the FIFO.

Serial data is accumulated in the receiver based on the synchronization mode selected. In the external sync mode, used for parallel-serial operation, the receiver is synchronized by the $\overline{DCD}$ (Data Carrier Detect) input and transfers successive bytes of data to the input of the Receiver FIFO. The single-sync-character mode requires that a match occur between the Sync Code Register and one incoming character before data transfer to the FIFO begins. The two-sync-character mode requires that two sync codes be received in sequence to establish synchronization. Subsequent to synchronization in any mode, data is accumulated in the shift register, and parity is optionally checked. An indication of parity error is carried through the Receiver FIFO with each character to the last empty location. Availability of a word at the FIFO output is indicated by a bit in the Status Register, as is a parity error.

The SSDA and its internal registers are selected by the address bus, Read/Write (R/W) and Enable control lines. To configure the SSDA, Control Registers are selected and the appropriate bits set. The Status Register is addressable for reading status.

Other I/O lines, in addition to Clear-to-Send ($\overline{CTS}$) and Data Carrier Detect ($\overline{DCD}$), include SM/$\overline{DTR}$ (Sync Match/Data Terminal Ready) and Transmitter Underflow (TUF). The transmitter and receiver each have individual clock inputs allowing simultaneous operation under separate clock control. Signals to the microprocessor are the Data bus and Interrupt Request ($\overline{IRQ}$).

Initialization

During a power-on sequence, the SSDA is reset via the $\overline{Reset}$ input and internally latched in a reset condition to prevent erroneous output transitions. The Sync Code Register, Control Register 2, and Control Register 3 should be programmed prior to the programmed release of the Transmitter and/or Receiver Reset bits; these bits in Control Register 1 should be cleared after the Reset line has gone high.

Transmitter Operation

Data is transferred to the transmitter section in parallel form by means of the data bus and Transmit Data FIFO. The Transmit Data FIFO is a 3-byte register whose status is indicated by the Transmitter Data Register Available status bit (TDRA) and its associated interrupt enable bit. Data is transferred through the FIFO on Enable (E) pulses. Two data transfer modes are provided in the SSDA. The 1-byte transfer mode provides for writing data to the transmitter section (and reading from the receiver section) one byte at a time. The 2-byte transfer mode provides for writing two data characters in succession.

Data will automatically transfer from the last register location in the Transmit Data FIFO (when it contains data) to the Transmitter Shift Register during the last half of the last bit of the previous character. A character is transferred into the Shift Register by the Transmitter Clock. Data is transmitted *LSB first*, and odd or even parity can be optionally appended. The unused bit positions in short word length characters from the data bus are "don't cares." (Note: The data bus inputs may be reversed for applications requiring the MSB to be transferred first, e.g., IBM format for floppy disks; however, care must be taken to properly program the control registers — Table 1 will have its bit positions reversed.)

When the Shift Register becomes empty and data is *not* available for transfer from the Transmit Data FIFO, an "underflow" occurs, and a character is inserted into the transmitter data stream to maintain

character synchronization. The character transmitted on underflow will be either a "Mark" (all "1"s) or the contents of the Sync Code Register, depending upon the state of the Transmit Sync Code on Underflow control bit. The underflow condition is indicated by a pulse (≈1 Tx Clk high period) on the Underflow output (when in Tx Sync on underflow mode). The Underflow output occurs coincident with the transfer of the last half of the last bit preceding the underflow character. The Underflow status bit is set until cleared by means of the Clear Underflow control bit. This output may be used in floppy disk systems to synchronize write operations and for appending CRCC.

Transmission is initiated by clearing the Transmitter Reset bit in Control Register 1. When the Transmitter Reset bit is cleared, the first *full* positive half-cycle of the Transmit Clock will initiate the transmit cycle, with the transmission of data or underflow characters beginning on the negative edge of the Transmit Clock pulse which started the cycle. If the Transmit Data FIFO was not loaded, an underflow character will be transmitted (see Figure 4).

.The $\overline{\text{Clear-to-Send}}$ ($\overline{\text{CTS}}$) input provides for automatic control of the transmitter by means of external system hardware; e.g., the modem $\overline{\text{CTS}}$ output provides the control in a data communications system. The $\overline{\text{CTS}}$ input resets and inhibits the transmitter section when high, but does not reset the Transmit Data FIFO. The TDRA status bit is inhibited by $\overline{\text{CTS}}$ being high in either the one-sync-character or two-sync-character mode of operation. In the external sync mode, TDRA is unaffected by $\overline{\text{CTS}}$ in order to provide Transmit Data FIFO status for preloading and operating the transmitter under the control of the $\overline{\text{CTS}}$ input. When the Transmitter Reset bit (Tx Rx) is set, the Transmit Data FIFO becomes available for new data with TDRA inhibited.

Receiver Operation

Data and a presynchronized clock are provided to the SSDA receiver section by means of the Receive Data (Rx Data) and Receive Clock (Rx Clk) inputs. The data is a continuous stream of binary data bits without means for identifying character boundaries within the stream. It is, therefore, necessary to achieve character synchronization for the data at the *beginning* of the data block. Once synchronization is achieved, it is assumed to be retained for all successive characters within the block.

Data communications systems utilize the detection of sync codes during the initial portion of the preamble to establish character synchronization. This requires the detection of a single code or two successive sync codes. Floppy disk and cartridge tape units require sixteen bits of defined preamble and cassettes require eight bits of preamble to establish the reference for the start of record. All three are functionally equivalent to the detection of sync codes. Systems which do not utilize code detection techniques require custom logic external to the SSDA for character synchronization and use of the parallel-to-serial (external sync) mode. (Note: The Receiver Shift Register is set to ones when reset.)

Synchronization

The SSDA provides three operating modes with respect to character synchronization: - one-sync-character mode, two-sync-character mode, and external sync mode. The external sync mode requires synchronization and control of the receiving section through the Data Carrier Detect ($\overline{\text{DCD}}$) input (see Figure 7). This external synchronization could consist of direct line control from the transmitting end of the serial data link or from external logic designed to detect the start of the message block. The one-sync-character mode searches on a bit-by-bit basis until a match is achieved between the data in the Shift Register and the Sync Code Register. The match indicates character synchronization is complete and will be retained in message block. In the two-sync-character mode, the receiver searches for the first sync code match on a bit-by-bit basis and then looks for a second *successive* sync code character prior to establishing character synchronization. If the second sync code character is not received, the bit-by-bit search for the first sync code is resumed.

Sync codes received prior to the completion of synchronization (one or two character) are not transferred to the Receive Data FIFO. Redundant sync codes during the preamble or sync codes which occur as "fill characters" can automatically be stripped from the data, when the Strip Sync control bit is set, to minimize system loading. The character synchronization will be retained until cleared by means of the Clear Sync bit, which also inhibits synchronization search when set.

Receiving Data

Once synchronization has been achieved, subsequent characters are automatically transferred into the Receive Data FIFO and clocked through the FIFO to the last empty location by E pulses (MPU System $\phi2$).

The Receiver Data Available status bit (RDA) indicates when data is available to be read from the last FIFO location (#3) when in the 1-byte transfer mode. The 2-byte transfer mode causes the RDA status bit to indicate data is available when the last two FIFO register locations are full. Data being available in the Receive Data FIFO causes an interrupt request if the Receiver Interrupt Enable (RIE) bit is set. The MPU will then read the SSDA Status Register, which will indicate that data is available for the MPU read from the Receive Data FIFO register. The IRQ and RDA status bits are reset by a read from the FIFO. If more than one character has been received and is resident in the Receive Data FIFO, subsequent E clocks will cause the FIFO to update and the RDA and IRQ status bits will again be set. The read data operation for the 2-byte transfer mode requires an intervening E clock between reads to allow the FIFO data to shift. Optional parity is automatically checked as data is received, and the parity status condition is maintained with each character until the data is read from the Receive Data FIFO. Parity errors will cause an interrupt request if the Error Interrupt Enable (EIE) has been set. The parity bit is not transferred to the data bus but must be checked in the Status Register. NOTE: In the 2-byte transfer mode, parity should be checked prior to reading the second byte, since a FIFO read clears the error bit.

Other status bits which pertain to the receiver section are Receiver Overrun and $\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$). The Overrun status bit is automatically set when a transfer of a character to the Receive Data FIFO occurs and the first register of the Receive Data FIFO is full. Overrun causes an interrupt if Error Interrupt Enable (EIE) has been set. The transfer of the over-running character into the FIFO causes the previous character in the FIFO input register location to be lost The Overrun status bit is cleared by reading the Status Register (when the overrun condition is present), followed by a Receive Data FIFO Register read. Overrun cannot occur and be cleared without providing an opportunity to detect its occurrence via the Status Register.

A positive transition on the $\overline{\text{DCD}}$ input causes an interrupt if the EIE control bit has been set. The interrupt caused by $\overline{\text{DCD}}$ is cleared by reading the Status Register when the $\overline{\text{DCD}}$ status bit is high, followed by a Receive Data FIFO read. The $\overline{\text{DCD}}$ status bit will subsequently follow the state of the $\overline{\text{DCD}}$ input when it goes low.

Input/Output Functions

SSDA Interface Signals for MPU

The SSDA interfaces to the S6800 MPU with an 8-bit bi-directional data bus, a chip select line, a register select line, an interrupt request line, read/write line, an enable line, and a reset line. These signals, in conjunction with the S6800 VMA output, permit the MPU to have complete control over the SSDA.

SSDA Bi-Directional Data (D0-D7)—The bi-directional data lines (D0-D7) allow for data transfer between the SSDA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an SSDA read operation.

SSDA Enable (E) — The Enable signal, E, is a high impedance TTL compatible input that enables the bus input/output data buffers, clocks data to and from the SSDA, and moves data through the FIFO Registers. This signal is normally the continuous S6800 System $\phi2$ clock, so that incoming data characters are shifted through the FIFO.

Read/Write (R/W) — The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the SSDA's input/output data bus interface. When Read/Write is high (MPU read cycle), SSDA output drivers are turned on if the chip is selected and a selected register is read. When it is low, the SSDA output drivers are turned off and the MPU writes into a selected register. The Read/Write signal is also used to select read-only or write-only registers within the SSDA.

Chip Select ($\overline{\text{CS}}$) — This high impedance TTL compatible input line is used to address the SSDA. The SSDA is selected when $\overline{\text{CS}}$ is low. VMA should be used in generating the $\overline{\text{CS}}$ input to insure that false selects will not occur. Transfers of data to and from the SSDA are then performed under the control of the Enable signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high impedance input that is TTL compatible. A high level is used to select Control Registers C2 and C3, the Sync Code Register, and the Transmit/Receive Data Registers. A low level selects the Control 1 and Status Registers (see Table 1).

Table 1. SSDA Programming Model

REGISTER	CONTROL INPUTS		ADDRESS CONTROL		REGISTER CONTENT							
	RS	R/W	AC2	AC1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STATUS (S)	0	1	X	X	INTERRUPT REQUEST (IRQ)	RECEIVER PARITY ERROR (PE)	RECEIVER OVERRUN (Rx Ovrn)	TRANS-MITTER UNDERFLOW (TUF)	CLEAR-TO-SEND (CTS)	DATA CARRIER DETECT (DCD)	TRANS-MITTER DATA REGISTER AVAILABLE (TDRA)	RECEIVER DATA AVAILABLE (RDA)
CONTROL 1 (C1)	0	0	X	X	ADDRESS CONTROL 2 (AC2)	ADDRESS CONTROL 1 (AC1)	RECEIVER INTERRUPT ENABLE (RIE)	TRANS-MITTER INTERRUPT ENABLE (TIE)	CLEAR SYNC	STRIP SYNC CHARACTERS (STRIP SYNC)	TRANS-MITTER RESET (Tx Rs)	RECEIVER RESET (Rx Rs)
RECEIVE DATA FIFO	1	1	X	X	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL 2 (C2)	1	0	0	0	ERROR INTERRUPT ENABLE (EIE)	TRANSMIT SYNC CODE ON UNDERFLOW (Tx Sync)	WORD LENGTH SELECT 3 (WS3)	WORD LENGTH SELECT 2 (WS2)	WORD LENGTH SELECT 1 (WS1)	1-BYTE/2-BYTE TRANSFER (1-BYTE/2-BYTE)	PERIPHERAL CONTROL 2 (PC2)	PERIPHERAL CONTROL 1 (PC1)
CONTROL 3 (C3)	1	0	0	1	NOT USED	NOT USED	NOT USED	NOT USED	CLEAR TRANS-MITTER UNDERFLOW STATUS (CTUF)	CLEAR CTS STATUS (CLEAR CTS)	ONE-SYNC-CHARACTER/TWO-SYNC-CHARACTER MODE CONTROL (1 Sync/2 Sync)	EXTERNAL/INTERNAL SYNC MODE CONTROL (E/I Sync)
SYNC CODE	1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
TRANSMIT DATA FIFO	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

X = DON'T CARE

Status Register

IRQ Bit 7 — The IRQ flag is cleared when the source of the IRQ is cleared. The source is determined by the enables in the Control Registers: TIE, RIE, EIE.

Bits 6-0 — indicate the SSDA status at a point in time, and can be *reset* as follows:

PE — Bit 6 — Read Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).

Rx Ovrn — Bit 5 — Read Status and then Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).

TUF — Bit 4 — A "1" into CTUF (C3 Bit 3) or into Tx Rs (C1 Bit 1).

CTS — Bit 3 — A "1" into Clear CTS (C3 Bit 2) or a "1" into Tx Rs (C1 Bit 1)

DCD — Bit 2 — Read Status and then Rx Data FIFO or a "1" into Rx Rs (C1 Bit 0)

TDRA — Bit 1 — Write into Tx Data FIFO.

RDA — Bit 0 — Read Rx Data FIFO.

Control Register 1

AC2, AC1 — Bits 7, 6 — Used to access other registers, as shown above.

RIE — Bit 5 — When "1", enables interrupt on RDA (S Bit 0).

TIE — Bit 4 — When "1", enables interrupt on TDRA (S Bit 1).

Clear Sync — Bit 3 — When "1", clears receiver character synchronization.

Strip Sync — Bit 2 — When "1", strips all sync codes from the received data stream.

Tx Rs — Bit 1 — When "1", resets and inhibits the transmitter section.

Rx Rs — Bit 0 — When "1", resets and inhibits the receiver section.

Control Register 3

CTUF — Bit 3 — When "1", clears TUF (S Bit 4), and IRQ if enabled.

Clear CTS — Bit 2 — When "1", clears CTS (S Bit 3), and IRQ if enabled.

1 Sync/2 Sync — Bit 1 — When "1", selects the one-sync-character mode; when "0", selects the two-sync-character mode.

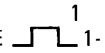E/I Sync — Bit 0 — When "1", selects the external sync mode; when "0", selects the internal sync mode.

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Control Register 2

EIE Bit 7 When "1", enables the PE, Rx Ovrn, TUF, $\overline{CTS}$, and $\overline{DCD}$ interrupt flags (S Bits 6 through 2).

Tx Sync Bit 6 When "1", allows sync code contents to be transferred on underflow, and enables the TUF Status bit and output. When "0", an all mark character is transmitted on underflow.

WS3, 2, 1 Bits 5-3 Word Length Select

BIT 5 WS3	BIT 4 WS2	BIT 3 WS1	WORD LENGTH
0	0	0	6 BITS + EVEN PARITY
0	0	1	6 BITS + ODD PARITY
0	1	0	7 BITS
0	1	1	8 BITS
1	0	0	7 BITS + EVEN PARITY
1	0	1	7 BITS + ODD PARITY
1	1	0	8 BITS + EVEN PARITY
1	1	1	8 BITS + ODD PARITY

1-Byte/ 2-Byte Bit 2 When "1", enables the TDRA and RDA bits to indicate when a 1-byte transfer can occur; when "0", the TDRA and RDA bits indicate when a 2-byte transfer can occur.

PC2, PC1 Bits 1-0 SM/$\overline{DTR}$ Output Control

BIT 1 PC2	BIT 0 PC1	SM/$\overline{DTR}$ OUTPUT AT PIN 5
0	0	1
0	1	PULSE ⎍ 1-BIT WIDE ON SM
1	0	0
1	1	SM INHIBITED, 0

Note: When the SSDA is used in applications requiring the MSB of data to be received and transmitted first, the data bus inputs to the SSDA may be reversed (D0 to D7, etc.) Caution must be used when this is done since the bit positions in this table will be reversed, and the parity should not be selected.

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The Interrupt Request remains low until cleared by the MPU.

Reset Input — The $\overline{Reset}$ input provides a means of resetting the SSDA from an external source. In the low state, the $\overline{Reset}$ input causes the following:

1. Receiver Reset (Rx Rs) and Transmitter Reset (Tx Rs) bits are set causing both the receiver and transmitter sections to be held in a reset condition.

2. Peripheral Control bits PC1 and PC2 are reset to zero, causing the SM/$\overline{DTR}$ output to be high.

3. The Error Interrupt Enable (EIE) bit is reset.

4. An internal synchronization mode is selected.

5. The Transmitter Data Register Available (TDRA) status bit is cleared and inhibited.

When $\overline{Reset}$ returns high (the inactive state), the transmitter and receiver sections will remain in the reset state until the Receiver Reset and Transmitter Reset bits are cleared via the bus under software control. The control Register bits affected by $\overline{Reset}$ (Rx Rs, Tx Rs, PC1, PC2, EIE, and E/I Sync) cannot be changed when $\overline{Reset}$ is low.

Clock Inputs

Separate high impedance TTL compatible inputs are provided for clocking of transmitted and received data.

Transmit Clock (Tx Clk) — The Transmit Clock input is used for the clocking of transmitted data. The transmitter shifts data on the negative transition of the clock.

Receive Clock (Rx Clk) — The Receive Clock input is used for clocking in received data. The clock and data must be synchronized externally. The receiver samples the data on the positive transition of the clock.

Serial Input/Output Lines

Receive Data (Rx Data) — The Receive Data line is a high impedance TTL compatible input through which data is received in a serial format. Data rates are from 0 to 600 kbps.

Transmit Data (Tx Data) — The Transmit Data output line transfers serial data to a modem or other peripheral. Data rates are from 0 to 600 kbps.

Peripheral/Modem Control

The SSDA includes several functions that permit limited control of a peripheral or modem. The functions included are $\overline{Clear-to-Send}$, Sync Match/$\overline{Data}$

Terminal Ready, Data Carrier Detect, and Transmitter Underflow.

Clear-to-Send ($\overline{\text{CTS}}$) — The $\overline{\text{CTS}}$ input provides a real-time inhibit to the transmitter section (the Tx Data FIFO is not disturbed). A positive $\overline{\text{CTS}}$ transition resets the Tx Shift Register and inhibits the TDRA status bit and its associated interrupt in both the one-sync-character and two-sync-character modes of operation. TDRA is not affected by the $\overline{\text{CTS}}$ input in the external sync mode.

The positive transition of $\overline{\text{CTS}}$ is stored within the SSDA to insure that its occurrence will be acknowledged by the system. The stored $\overline{\text{CTS}}$ information and its associated $\overline{\text{IRQ}}$ (if enabled) are cleared by writing a "1" in the Clear $\overline{\text{CTS}}$ bit in Control Register 3 or in the Transmitter Reset bit. The $\overline{\text{CTS}}$ status bit subsequently follows the $\overline{\text{CTS}}$ input when it goes low.

The $\overline{\text{CTS}}$ input provides character timing for transmitter data when in the external sync mode. Transmission is initiated on the negative transition of the first *full* positive clock pulse of the transmitter clock (Tx Clk) after the release of $\overline{\text{CTS}}$ (see Figure 6).

Data Carrier Detect ($\overline{\text{DCD}}$) — The $\overline{\text{DCD}}$ input provides a real-time inhibit to the receiver section (the Rx FIFO is not disturbed). A positive $\overline{\text{DCD}}$ transition resets and inhibits the receiver section except for the Receive FIFO and the RDRA status bit and its associated $\overline{\text{IRQ}}$.

The positive transition of $\overline{\text{DCD}}$ is stored within the SSDA to insure that its occurrence will be acknowledged by the system. The stored $\overline{\text{DCD}}$ information and its associated $\overline{\text{IRQ}}$ (if enabled) are cleared by reading the Status Register and then the Receiver FIFO, or by writing a "1" into the Receiver Reset bit. The $\overline{\text{DCD}}$ status bit subsequently follows the $\overline{\text{DCD}}$ input when it goes low. The $\overline{\text{DCD}}$ input provides character synchronization timing for the receiver during the external sync mode of operation. The receiver will be initialized and data will be sampled on the positive transition of the first *full* Receive Clock cycle after release of $\overline{\text{DCD}}$ (see Figure 7).

Sync Match/$\overline{\text{Data Terminal Ready}}$ (SM/$\overline{\text{DTR}}$) — The SM/$\overline{\text{DTR}}$ output provides four functions (see Table 1) depending on the state of the PC1 and PC2 control bits. When the Sync Match mode is selected (PC1 = "1", PC2 = "0"), the output provides a one-bit-wide pulse when a sync code is detected. The SM output is inhibited when PC2 = "1". The $\overline{\text{DTR}}$ mode (PC1 = "0") provides an output level corresponding to the complement of PC2 ($\overline{\text{DTR}}$ = "0" when PC2 = "1"). (See Table 1.)

Transmitter Underflow (TUF) — The Underflow output indicates the occurrence of a transfer of a "fill

character" to the Transmitter Shift Register when the last location (#3) in the Transmit Data FIFO is empty. The Underflow output pulse is approximately a Tx Clk high period wide and occurs during the last half of the last bit of the character preceding the "Underflow" (see Figure 4). The Underflow output does not respond to underflow conditions when the Tx Sync bit is in the reset state.

SSDA Registers

Seven registers in the SSDA can be accessed by means of the bus. The registers are defined as read-only or write-only according to the direction of information flow. The Register Select input (RS) selects two registers in each state, one being read-only and the other write-only. The Read/Write input (R/W) defines which of the two selected registers will actually be accessed. Four registers (two read-only and two write-only) can be addressed via the bus at any particular time. These registers and the required addressing are defined in Table 1.

Control Register 1 (C1)

Control Register 1 is an 8-bit write-only register that can be directly addressed from the data bus. Control Register 1 is addressed when RS = "0" and R/W = "0".

Receiver Reset (Rx Rs), C1 Bit 0 — The Receiver Reset control bit provides both a reset and inhibit function to the receiver section. When Rx Rs is set, it clears the receiver control logic, sync logic, error logic, Rx Data FIFO, Parity Error status bit, and $\overline{\text{DCD}}$ interrupt. The Receiver Shift Register is set to ones. The Rx Rs bit must be cleared after the occurrence of a low level on $\overline{\text{Reset}}$ in order to enable the receiver section of the SSDA.

Transmitter Reset (Tx Rs), C1 Bit 1 — The Transmitter Reset control bit provides both a reset and inhibit to the transmitter section. When Tx Rs is set, it clears the transmitter control section, Transmitter Shift Register, Tx Data FIFO (which can be reloaded after one E clock pulse), the Transmitter Underflow status bit, and the $\overline{\text{CTS}}$ interrupt, and inhibits the TDRA status bit (in the one-sync-character and two-sync-character modes). The Tx Rs bit must be cleared after the occurrence of a low level on $\overline{\text{Reset}}$ in order to enable the transmitter section of the SSDA.

Strip Synchronization Characters (Strip Sync), C1 Bit 2 — If the Strip Sync bit is set, the SSDA will automatically strip all received characters which match the contents of the Sync Code Register. The characters used for synchronization (one or two characters of sync) are always stripped from the received data stream.

Clear Synchronization (Clear Sync), C1 Bit 3 — The Clear Sync control bit provides the capability of dropping receiver character synchronization and inhibiting resynchronization. The Clear Sync bit is set to clear and inhibit receiver synchronization in *all* modes and is reset to zero to enable resynchronization.

Transmitter Interrupt Enable (TIE), C1 Bit 4 — TIE enables both the $\overline{\text{Interrupt Request}}$ output ($\overline{\text{IRQ}}$) and Interrupt Request status bit to indicate a transmitter service request. When TIE is set and the TDRA status bit is high, the $\overline{\text{IRQ}}$ output will go low (the active state) and the $\overline{\text{IRQ}}$ status bit will go high.

Receiver Interrupt Enable (RIE), C1 Bit 5 — RIE enables both the $\overline{\text{Interrupt Request}}$ output ($\overline{\text{IRQ}}$) and the Interrupt Request status bit to indicate a receiver service request. When RIE is set and the RDA status bit is high, the $\overline{\text{IRQ}}$ output will go low (the active state) and the IRQ status bit will go high.

Address Control 1 (AC1) and Address Control 2 (AC2), C1 Bits 6 and 7 — AC1 and AC2 select one of the write-only registers — Control 2, Control 3, Sync Code, or Tx Data FIFO — as shown in Table 1, when RS = "1" and R/W = "0".

Control Register 2 (C2)

Control Register 2 is an 8-bit write-only register which can be programmed from the bus when the Address Control bits in Control Register 1 (AC1 and AC2) are reset, RS = "1" and R/W = "0".

Peripheral Control 1 (PC1) and Peripheral Control 2 (PC2), C2 Bits 0 and 1 — Two control bits, PC1 and PC2, determine the operating characteristics of the Sync Match/$\overline{\text{DTR}}$ output. PC1, when high, selects the Sync Match mode. PC2 provides the inhibit/enable control for the SM/$\overline{\text{DTR}}$ output in the Sync Match mode. A one-bit-wide pulse is generated at the output when PC2 is "0", and a match occurs between the contents of the Sync Code Register and the incoming data even if sync is inhibited (Clear Sync bit = "1"). The Sync Match pulse is referenced to the negative edge of Rx Clk pulse causing the match (see Figure 3).

The $\overline{\text{Data Terminal Ready}}$ ($\overline{\text{DTR}}$) mode is selected when PC1 is low. When PC2 = "1" the SM/$\overline{\text{DTR}}$ output = "0" and vice versa. The operation of PC2 and PC1 is summarized in Table 1.

1-Byte/2-Byte Transfer (1-Byte/2-Byte), C2 Bit 2 — When 1-Byte/2-Byte is set, the TDRA and RDA status bits will indicate the availability of their respective data FIFO registers for a single byte data transfer.

Alternately, if 1-Byte/2-Byte is reset, the TDRA and RDA status bits indicate when two bytes of data can be moved without a second status read. An intervening Enable pulse must occur between data transfers.

Word Length Selects (WS1, WS2, WS3), C2 Bits 3, 4, 5 — Word Length Select bits WS1, WS2, and WS3 select word length of 7, 8, or 9 bits including parity as shown in Table 1.

Transmit Sync Code on Underflow (Tx Sync), C2 Bit 6 — When Tx Sync is set, the transmitter will automatically send a sync character when data is not available for transmission. If Tx Sync is reset, the transmitter will transmit a Mark character (including the parity bit position) on underflow. When the underflow is detected, a pulse approximately a Tx Clk high period wide will occur on the underflow output if the Tx Sync bit is set. Internal parity generation is inhibited during underflow except for sync code fill character transmission in 8-bit plus parity word lengths.

Error Interrupt Enable (EIE), C2 Bit 7 — When EIE is set, the IRQ status bit will go high and the $\overline{\text{IRQ}}$ output will go low if:

1. A receiver overrun occurs. The interrupt is cleared by reading the Status Register and reading the Rx Data FIFO.

2. $\overline{\text{DCD}}$ input has gone to a "1". The interrupt is cleared by reading the Status Register and reading the Rx Data FIFO.

3. A parity error exists for the character in the last location (#3) of the Rx Data FIFO. The interrupt is cleared by reading the Rx Data FIFO.

4. The $\overline{\text{CTS}}$ input has gone to a "1". The interrupt is cleared by writing a "1" in the Clear $\overline{\text{CTS}}$ bit, C3 bit 2, or by a TX Reset.

5. The transmitter has underflowed (in the Tx Sync on Underflow mode). The interrupt is cleared by writing a "1" into the Clear Underflow, C3 bit 3, or Tx Reset.

When EIE is a "0", the IRQ status bit and the $\overline{\text{IRQ}}$ output are disabled for the above error conditions. A low level on the $\overline{\text{Reset}}$ input resets EIE to "0".

Control Register 3 (C3)

Control Register 3 is a 4-bit write-only register which can be programmed from the bus when RS = "1" and R/W = "0" and Address Control bit AC1 = "1" and AC2 = "0".

External/Internal Sync Mode Control (E/I Sync), C3 Bit 0 — When the E/I Sync Mode bit is high, the SSDA is in the external sync mode and the receiver synchronization logic is disabled. Synchronization can be achieved by means of the $\overline{DCD}$ input or by starting Rx Clk at the midpoint of data bit 0 of a character with $\overline{DCD}$ low. Both the transmitter and receiver sections operate as parallel — serial converters in the External Sync mode. The Clear Sync bit in Control Register 1 acts as a receiver sync inhibit when high to provide a bus controllable inhibit. The Sync Code Register can serve as a transmitter fill character register and a receiver match register in this mode. A "low" on the $\overline{Reset}$ input resets the E/I Sync Mode bit placing the SSDA in the internal sync mode.

One-Sync-Character/Two-Sync-Character Mode Control (1 Sync/2 Sync), C3 Bit 1 — When the 1 Sync/2 Sync bit is set, the SSDA will synchronize on a single match between the received data and the contents of the Sync Code Register. When the 1 Sync/2 Sync bit is reset, two *successive* sync characters must be received prior to receiver synchronization. If the second sync character is not detected, the bit by bit search resumes from the first bit in the second character. See the description of the Sync Code Register for more details.

Clear $\overline{CTS}$ Status (Clear $\overline{CTS}$), C3 Bit 2 — When a "1" is written into the Clear $\overline{CTS}$ bit, the stored status and interrupt are cleared. Subsequently, the $\overline{CTS}$ status bit reflects the state of the $\overline{CTS}$ input. The Clear $\overline{CTS}$ control bit does not affect the $\overline{CTS}$ input nor its inhibit of the transmitter section. The Clear $\overline{CTS}$ command bit is self-clearing, and writing a "0" into this bit is a nonfunctional operation.

Clear Transmit Underflow Status (CTUF), C3 Bit 3 — When a "1" is written into the CTUF status bit, the CTUF bit and its associated interrupt are reset. The CTUF command bit is self-clearing and writing a "0" into this bit is a nonfunctional operation.

Sync Code Register

The Sync Code Register is an 8-bit register for storing the programmable sync code required for received data character synchronization in the one-sync-character and two-sync-character modes. The Sync Code Register also provides for stripping the sync/fill characters from the received data (a programmable option) as well as automatic insertion of fill characters in the transmitted data stream. The Sync Code Register is

not utilized for receiver character synchronization in the external sync mode; however, it provides storage of receiver match and transmit fill characters.

The Sync Code Register can be loaded when AC2 and AC1 are a "1" and "0", respectively, and R/W = "0" and RS - "1".

The Sync Code Register may be changed after the detection of a match with the received data (the first sync code having been detected) to synchronize with a double-word sync pattern. (This sync code change must occur prior to the completion of the second character.) The sync match (SM) output can be used to interrupt the MPU system to indicate that the first eight bits have matched. The service routine would then change the sync match register to the second half of the pattern. Alternately, the one-sync-character mode can be used for sync codes for 16 or more bits by using software to check the second and subsequent bytes after reading them from the FIFO.

The detection of the sync code can be programmed to appear on the Sync Match/$\overline{DTR}$ output by writing a "1" in PC1 (C2 bit 0) and a "0" in PC2 (C2 bit 1). The Sync Match output will go high for one bit time beginning at the character interface between the sync code and the next character (see Figure 3).

Receive Data First-In First-Out Register (Rx Data FIFO)

The Receive Data FIFO Register consists of three 8-bit registers which are used for buffer storage of received data. Each 8-bit register has an internal status bit which monitors its full or empty condition. Data is always transferred from a full register to an adjacent empty register. The transfer from register to register occurs on E pulses. The RDA status bit will be high when data is available in the last location of the Rx Data FIFO.

In an Overrun condition, the overrunning character will be transferred into the full first stage of the FIFO register and will cause the loss of that data character. Successive overruns continue to overwrite the first register of the FIFO. This destruction of data is indicated by means of the Overrun status bit. The Overrun bit will be set when the overrun occurs and remains set until the Status Register is read, followed by a read of the Rx Data FIFO.

Unused data bits for short word lengths (including the parity bit) will appear as "0"s on the data bus when the Rx Data FIFO is read.

Transmit Data First-In First-Out Register (Tx Data FIFO)

The Transmit Data FIFO Register consists of three 8-bit registers which are used for buffer storage of data to be transmitted. Each 8-bit register has an internal status bit which monitors its full or empty condition. Data is always transferred from a full register to an adjacent empty register. The transfer is clocked by E pulses.

The TDRA status bit will be high if the Tx Data FIFO is available for data.

Unused data bits for short word lengths will be handled as "don't cares". The parity bit is not transferred over the data bus since the SSDA generates parity at transmission.

When an Underflow occurs, the Underflow character will be either the contents of the Sync Code Register or an all "1"s character. The underflow will be stored in the Status Register until cleared and will appear on the Underflow output as a pulse approximately a Tx Clk high period wide.

Status Register

The Status Register is an 8-bit read-only register which provides the real-time status of the SSDA and the associated serial data channel. Reading the Status Register is a non-destructive process. The method of clearing status bits depends upon the function each bit represents and is discussed for each bit in the register.

Receiver Data Available (RDA), S Bit 0 — The Receiver Data Available status bit indicates when receiver data can be read from the Rx Data FIFO. The receiver data being present in the last register (#3) of the FIFO causes RDA to be high for the 1-byte transfer mode. The RDA bit being high indicates that the last two registers (#2 and #3) are full when in the 2-byte transfer mode. The second character can be read without a second status read (to determine that the character is available). An E pulse must occur between reads of the Rx Data FIFO to allow the FIFO to shift. Status must be read on a word-by-word basis if receiver data error checking is important. The RDA status bit is reset automatically when data is not available.

Transmitter Data Register Available (TDRA), S Bit 1 — The TDRA status bit indicates that data can be loaded into the Tx Data FIFO Register. The first register (#1) of the Tx Data FIFO being empty will be indicated by a high level in the TDRA status bit in the 1-byte transfer mode. The first two registers (#1 and #2) must be empty for TDRA to be high when in the 2-byte transfer mode. The Tx Data FIFO can be loaded with two bytes without an intervening status read; however, one E pulse must occur between loads. TDRA is inhibited by the Tx Reset or $\overline{\text{Reset}}$. When Tx Reset is set, the Tx Data FIFO is cleared and then released on the next E clock pulse. The Tx Data FIFO can then be loaded with up to three characters of data, even though TDRA is inhibited. This feature allows preloading data prior to the release of Tx Reset. A high level on the $\overline{\text{CTS}}$ input inhibits the TDRA status bit in either sync mode of operation (one-sync-character or two-sync-character). $\overline{\text{CTS}}$ does not affect TDRA in the external sync mode. This enables the SSDA to operate under the control of the $\overline{\text{CTS}}$ input with TDRA indicating the status of the Tx Data FIFO. The $\overline{\text{CTS}}$ input does not clear the Tx Data FIFO in any operating mode.

Data Carrier Detect ($\overline{\text{DCD}}$), S Bit 2 — A positive transition on the $\overline{\text{DCD}}$ input is stored in the SSDA until cleared by reading both Status and Rx Data FIFO. A "1" written into Rx Rs also clears the stored $\overline{\text{DCD}}$ status. The $\overline{\text{DCD}}$ status bit, when set, indicates that the $\overline{\text{DCD}}$ input has gone high. The reading of both Status and Receive Data FIFO allows Bit 2 of subsequent Status reads to indicate the state of the $\overline{\text{DCD}}$ input until the next positive transition.

Clear-to-Send ($\overline{\text{CTS}}$), S Bit 3 — A positive transition on the $\overline{\text{CTS}}$ input is stored in the SSDA until cleared by writing a "1" into the Clear $\overline{\text{CTS}}$ control bit or the Tx Rs bit. The $\overline{\text{CTS}}$ status bit, when set, indicates that the $\overline{\text{CTS}}$ input has gone high. The Clear $\overline{\text{CTS}}$ command (a "1" into C3 Bit 2) allows Bit 3 of subsequent Status reads to indicate the state of the $\overline{\text{CTS}}$ input until the next positive transition.

Transmitter Underflow (TUF), S Bit 4 — When data is not available for the transmitter, an underflow occurs and is so indicated in the Status Register (in the Tx Sync on underflow mode). The underflow status bit is cleared by writing a "1" into the Clear Underflow (CTUF) control bit or the Tx Rs bit. TUF indicates that a sync character will be transmitted as the next character. A TUF is indicated on the output *only* when the contents of the Sync Code Register is to be transferred (transmit sync code on underflow = "1").

Receiver Overrun (Rx Ovrn), S Bit 5 — Overrun indicates data has been received when the Rx Data FIFO is full, resulting in data loss. The Rx Ovrn status bit is set when Overrun occurs. The Rx Ovrn status bit is cleared by reading Status followed by reading the Rx Data FIFO or by setting the Rx Rs control bit.

Receiver Parity Error (PE), S Bit 6 — The parity error status bit indicates that parity for the character in the last register of the Rx Data FIFO did not agree with selected parity. The parity error is cleared when the character to which it pertains is read from the Rx Data FIFO or when Rx Rs occurs. The $\overline{DCD}$ input does not clear the Parity Error or Rx Data FIFO status bits.

Interrupt Request (IRQ), S Bit 7 — The Interrupt Request status bit indicates when the $\overline{IRQ}$ output is in the active state ($\overline{IRQ}$ output = "0"). The IRQ status bit is subject to the same interrupt enables (RIE, TIE, and EIE) as the $\overline{IRQ}$ output. The IRQ status bit simplifies status inquiries for polling systems by providing single bit indication of service requests.

Physical Dimensions

24-PIN CERAMIC
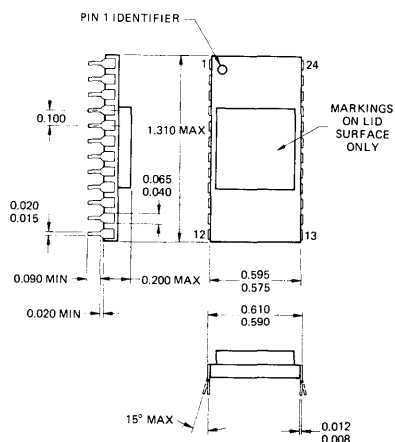
24-PIN PLASTIC

NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA. (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
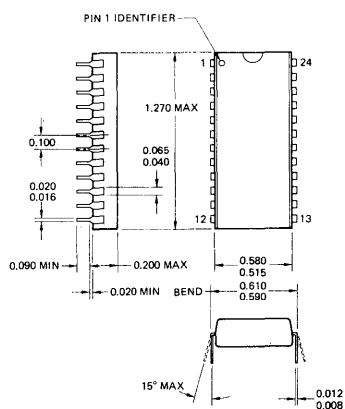
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA. AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (DIM. "D").
2. DIM. "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

S6800

AMI®

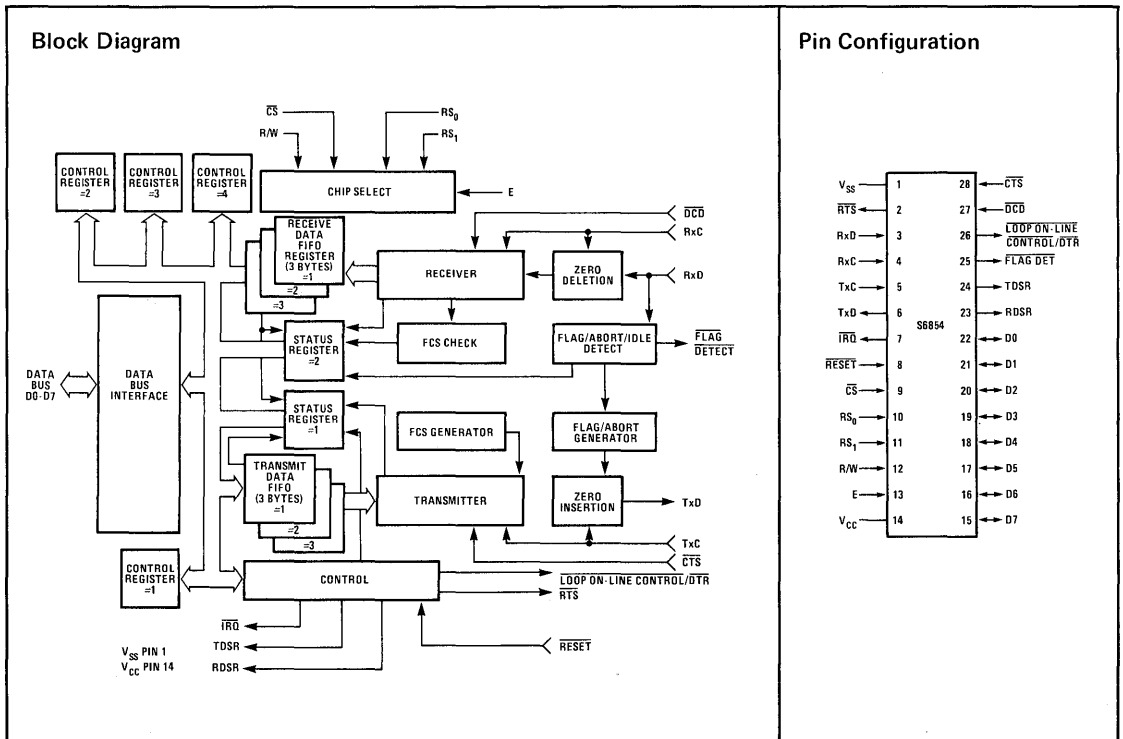# ADVANCED DATA LINK CONTROLLER

Features

☐ S6800 Compatible
☐ Protocol Features
  ☐ Automatic Flag Detection and Synchronization
  ☐ Zero Insertion and Deletion
  ☐ Extendable Address, Control and Logical Control Fields (Optional)
  ☐ Variable Word Length Info Field — 5, 6, 7, or 8-bits
  ☐ Automatic Frame Check Sequence Generation and Check
  ☐ Abort Detection and Transmission
  ☐ Idle Detection and Transmission
☐ Loop Mode Operation
☐ Loop Back Self-Test Mode
☐ NRZ/NRZI Modes

☐ Quad Data Buffers for Each Rx and Tx
☐ Prioritized Status Register (Optional)
☐ MODEM/DMA/Loop Interface
☐ MIL-STD-883, Class B and C Devices Available

General Description

The S6854 ADLC performs the complex MPU/data communication link function for the "Advanced Data Communication Control Procedure" (ADCCP). High Level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations.

Block Diagram

Pin Configuration

Absolute Maximum Ratings*

Supply Voltage	$-0.3V$ to $+7.0V$
Input Voltage	$-0.3V$ to $+7.0V$
Operating Temperature Range	$0°C$ to $+70°C$
Industrial Temperature Range	$-40°C$ to $+85°C$
Military Temperature Range	$-55°C$ to $+125°C$
Storage Temperature Range	$-55°C$ to $+150°C$
Thermal Resistance	$+70°C/W$

*This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0$, $T_A = 0°C$ to $70°C$ unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	$V_{SS}+2.0$			Vdc	
V_{IL}	Input Low Voltage			$V_{SS}+0.8$	Vdc	
I_{IN}	Input Leakage Current All Inputs Except D0 — D7		1.0	2.5	μAdc	$V_{IN} = 0$ to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current D0 — D7		2.0	10	μAdc	$V_{IN} = 0.4$ to 2.4Vdc $V_{CC} = 5.25$Vdc
V_{OH}	Output High Voltage D0 — D7 All Others	$V_{SS}+2.4$ $V_{SS}+2.4$			Vdc	$I_{LOAD} = -205\mu Adc$ $I_{LOAD} = -100\mu Adc$
V_{OL}	Output Low Voltage			$V_{SS}+0.4$	Vdc	$I_{LOAD} = 1.6$mAdc
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	$V_{OH} = 2.4$Vdc
P_D	Power Dissipation			850	mW	
C_{IN}	Capacitance D0 — D7 All Other Inputs			12.5 7.5	pF	$V_{IN} = 0$, $T_A = 25°C$, $f = 1.0$MHz
C_{OUT}	$\overline{IRQ}$ All Others			5.0 10	pF	

Symbol	Parameter	S6854 Min.	S6854 Max.	S68A54 Min.	S68A54 Max.	Unit	Conditions
PW_{CL}	Minimum Clock Pulse Width, Low	700		450		ns	
PW_{CH}	Minimum Clock Pulse Width, High	700		450		ns	
f_C	Clock Frequency		0.66		1.0	MHz	
t_{RDSU}	Receive Data Setup Time	250		200		ns	
t_{RDH}	Receive Data Hold Time	120		100		ns	
t_{RTS}	Request-to-Send Delay Time		680		460	ns	
t_{TDD}	Clock-to-Data Delay for Transmitter		460		320	ns	
t_{FD}	Flag Detect Delay Time		680		460	ns	
t_{DTR}	DTR Delay Time		680		460	ns	
t_{LOC}	Loop On-Line Control Delay Time		680		460	ns	
t_{RDSR}	RDSR Delay Time		540		400	ns	
t_{TDSR}	TDSR Delay Time		540		400	ns	
t_{IR}	Interrupt Request Release Time		1.2		0.9	μs	
t_{RES}	Reset Minimum Pulse Width	1.0		0.65		μs	
t_r, t_f	Input Rise and Fall Times Except Enable		1.0*		1.0*	μs	0.8V to 2.0V

*1.0μs or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Read

Symbol	Parameter	S6854 Min.	S6854 Max.	S68A54 Min.	S68A54 Max.	Unit
t_{CYC}	Enable Cycle Time	1.0		0.666		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable positive transition	160		140		ns
t_{DDR}	Data Delay Time		320		220	ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input		25		25	ns

Write

Symbol	Parameter	S6854 Min.	S6854 Max.	S68A54 Min.	S68A54 Max.	Unit
t_{CYCE}	Enable Cycle Time	1.0		0.666		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable positive transition	160		140		ns
t_{DSW}	Data Setup Time	195		80		ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input		25		25	ns

Figure 1. Bus Timing Test Loads
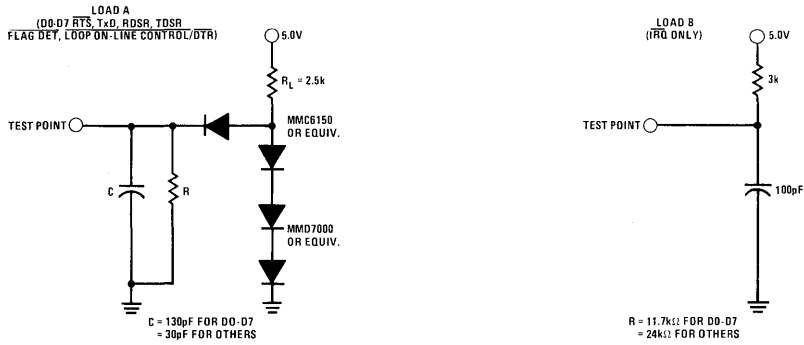
Figure 2. Receiver Data Setup/Hold, Flag Detect and Loop On-Line Control Delay Timing
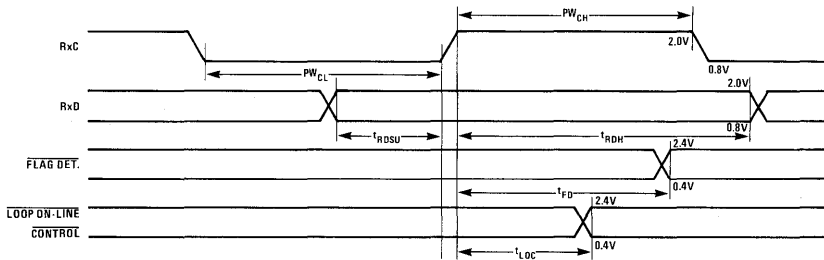
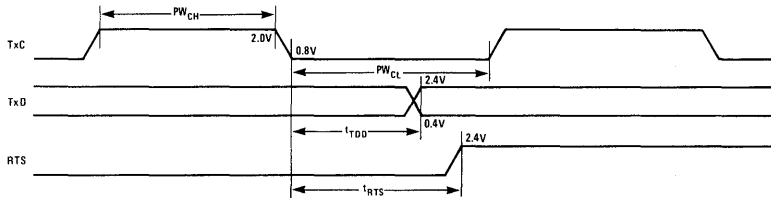Figure 3. Transmit Data Output Delay and Request to Send Delay Timing

Figure 4. TDSR/RDSR Delays, IRQ Release Delay, RTS and DTR Delay Timing
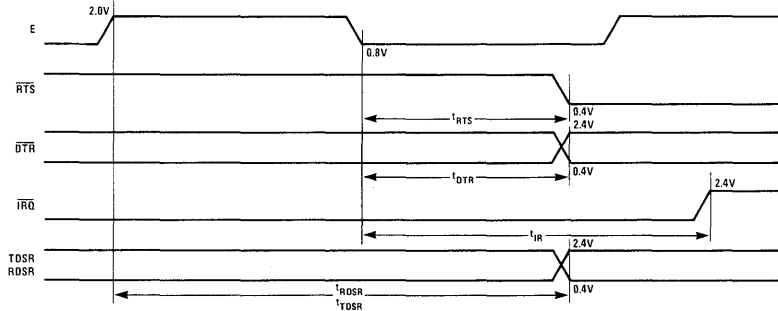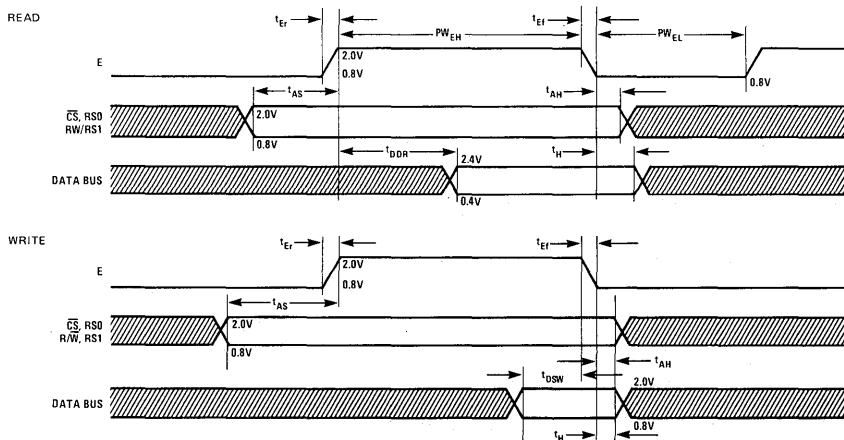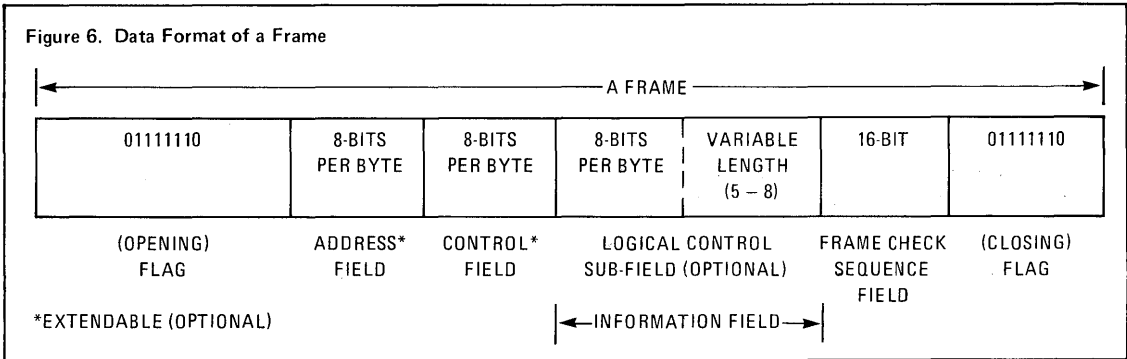

Figure 5. Bus Read/Write Timing Characteristics

Frame Format

The ADLC transmits and receives data (information or control) in a format called a frame. All frames start with an opening flag (F) and end with a closing flag (F). Between the opening flag and closing flag, a frame contains an address field, control field, information field, and frame check sequence field.

Figure 6. Data Format of a Frame

01111110	8-BITS PER BYTE	8-BITS PER BYTE	8-BITS PER BYTE	VARIABLE LENGTH (5 – 8)	16-BIT	01111110
(OPENING) FLAG	ADDRESS* FIELD	CONTROL* FIELD	LOGICAL CONTROL SUB-FIELD (OPTIONAL)		FRAME CHECK SEQUENCE FIELD	(CLOSING) FLAG

A FRAME

*EXTENDABLE (OPTIONAL)

←INFORMATION FIELD→

Flag (F) — The flag is the unique binary pattern (01111110). It provides the frame boundary and a reference for the position of each field of the frame.

The ADLC transmitter generates a flag pattern internally and the opening flag and closing flags are appended to a frame automatically. Two successive frames can share one flag for a closing flag of the first frame and for the opening flag of the next frame, if the "FF/F" control bit in the control register is reset.

The receiver searches for a flag on a bit by bit basis and recognizes a flag at any time. The receiver establishes the frame synchronization with every flag. The flags mark the frame boundary and reference for each field but they are not transferred to the Rx FIFO. The detection of a flag is indicated by the Flag Detect output and by a status bit in the status register.

Order of Bit Transmission — Address, control and information field bytes are transferred between the MPU and the ADLC in parallel by means of the data bus. The bit on D0 (data bus bit 0, pin 22) is serially transmitted first, and the first serially received bit is transferred to the MPU on D0. The FCS field is transmitted and receives MSB first.

Address (A) Field — The 8 bits following the opening flag are the address (A) field. The A-field can be extendable if the Auto-Address Extend Mode is selected in control register #3. In the Address Extend Mode, the first bit (bit 0) in every address octet becomes the extend control bit. When the bit is "0", the ADLC assumes another address octet will follow, and when the bit is "1", the address extension is terminated. A "null" address (all "0's") does not extend. In the receiver, the Address Present status

bit distinguishes the address field from other fields. When an address byte is available to be read in the receive FIFO register, the Address Present status bit is set and causes an interrupt (if enabled). The Address Present bit is set for every address octet when the Address Extend Mode is used.

Control (C) Field — The 8 bits following the address field is the control (link control) field. When the Extended Control Field bit in control register #3 is selected, the C-field is extended to 16 bits.

Information (I) Field — The I-field follows the C-field and precedes the FCS field. The I-field contains "data" to be transferred but is not always necessarily contained in every frame. The word length of the I-field can be selected from 5 to 8 bits per byte by control bits in control register #4. The I-field will continue until it is terminated by the FCS and closing flag. The receiver has the capability to handle a "partial" last byte. The last information byte can be any word length between 1 and 8 bits. If the last byte in the I-field is less than the selected word length, the receiver will right justify the received bits, fill the remaining bits of the receiver shift register with zeros, and transfer a full byte to the Rx FIFO. Regardless of selected byte length, the ADLC will transfer 8 bits of data to the data bus. Unused bits for word lengths of 5, 6, and 7 will be zeroed.

Logical Control (LC) Field — When the Logical control Field Select bit in control register #3 is selected, the ADLC separates the I-field into two sub-fields. The first sub-field is the Logical Control field and the following sub-field is the "data" portion of the I-field. The logical control field is 8 bits and

follows the C-field, which is extendable by octets, if it is selected. The last bit (bit 7) is the extend control bit, and if it is a "1", the LC-field is extended one octet.

Note: Hereafter the word "Information Field" or "I-field" is used as the data portion of the information field, and excludes the logical control field. This is done in order to keep the consistency of the meaning of "Information Field" as specified in SDLC, HDLC, and ADCCP standards.

Frame Check Sequence (FCS) Field — The 16 bits preceding the closing flag is the FCS field. The FCS is the "cyclic redundancy check character (CRCC)". The poly-nomial $x^{16} + x^{12} + x^5 + 1$ is used both for the transmitter and receiver. Both the transmitter and receiver poly-nominal registers are initialized to all "1"s prior to calculation of the FCS. The transmitter calculates the FCS on all bits of the address, control, logical control (if selected), and information fields, and transmits the complement of the resulting remainder as FCS. The receiver performs the similar computation on all bits of the address, control, logical control (if selected), information, and received FCS fields and compares the result to F0B8 (Hexadecimal). When the result matches F0B8, the Frame Valid status bit is set in the status register. If the result does not match, the Error status bit is set. The FCS generation, transmission, and checking are performed automatically by the ADLC transmitter and receiver. The FCS field is not transferred to the Rx FIFO.

Invalid Frame — Any valid frames should have at least the A-field, C-field and FCS field between the opening flag and the closing flag. When invalid frames are received, the ADLC handles them as follows:

1) A short frame which has less than 25 bits between flags — The ADLC ignores the short frame and its reception is not reported to the MPU.

2) A frame less than 32 bits between the flags, or a frame 32 bits or more with an extended A-field or C-field that is not completed. — This frame is transferred into the Rx FIFO. The FCS/IF Error status bit indicates the reception of the invalid frame at the end of the frame.

3) Aborted Frame— The frame which is aborted by receiving an abort or DCD failure is also an invalid frame. Refer to "Abort" and "DCD status bit."

Zero Insertion and Zero Deletion — The Zero insertion and deletion, which allows the content of the frame to be transparent, are performed by the ADLC automatically. A binary 0 is inserted by the transmitter after any succession of 5 1's within a frame (A, C, LC, I, and FCS field). The receiver deletes a binary 0 that follows successive 5 continuous 1's within a frame.

Abort — The function of prematurely terminating a data link is called "abort". The transmitter aborts a frame by sending at least 8 consecutive 1's immediately after the Tx Abort control bit in control register #4 is set to a "1". (Tx FIFO is also cleared by the Tx Abort control bit at the same time.) The abort can be extended up to (at least) 16 consecutive 1's, if the Abort Extend control bit in the control register #4 is set when an abort is sent. This feature is useful to force mark idle transmission. Reception of 7 or more consecutive 1's is interpreted as an abort by the receiver. The receiver responds to a received abort as follows:

1) An abort in an "out of frame" condition — An abort during the idle or time fill has no meaning. The abort reception is indicated in the status register as long as the abort condition continues; but neither an interrupt nor a stored condition occurs. The abort indication is suppressed after 15 or more consecutive 1's are received (Received Idle status is set).

2) An abort "in frame" after less than 26 bits are received after an opening flag — Under this condition, any field of the aborted frame has not transferred to the MPU yet. The ADLC clears the aborted frame data in the FIFO and clears flag synchronization. Neither an interrupt nor a stored status occurs. The status indication is the same as (1) above.

3) An abort "in frame" after 26 bits or more are received after an opening flag — Under this condition, some fields of the aborted frame might have been transferred onto the data bus. The abort status is stored in the receiver status register and the data of the aborted frame in the ADLC is cleared. The synchronization is also cleared.

Idle and Time Fill — When the transmitter is in an "out of frame" condition (the transmitter is not transmitting a frame), it is in an idle state. Either a series of contiguous flags (time fill) or a mark idle

(consecutive 1's on a bit by bit basis) is selected for the transmission in an idle state by the Flag/Mark Idle control bit. When the receiver receives 15 or more consecutive 1's, the Receive Idle status bit is set and causes an interrupt. The flags and mark idle are not transferred to the Rx FIFO.

Operation

Initialization — During a power-on sequence, the ADLC is reset via the $\overline{RESET}$ input and internally latched in a reset condition to prevent erroneous output transitions. The four control registers must be programmed prior to the release of the reset condition. The release of the reset condition is performed via software by writing a "0" into the Rx RS control bit (receiver) and/or Tx RS control bit (transmitter). The release of the reset condition must be done after the $\overline{RESET}$ input has gone high.

At any time during operation, writing a "1" into the Rx RS control bit or TX RS control causes the reset condition of the receiver or the transmitter.

Transmitter Operation — The Tx FIFO register cannot be pre-loaded when the transmitter is in a reset state. After the reset release, the Flag/Mark Idle control bit selects either the mark idle state (inactive idle) or the Flag "time fill' (active idle) state. This active or inactive mark idle state will continue until data is loaded into the Tx FIFO.

The availability of the Tx FIFO is indicated by the TDRA status bit under the control of the 2-Byte/1-Byte control bit. TDRA status is inhibited by the Tx RS bit or $\overline{CTS}$ input being high. When the 1-Byte mode is selected, one byte of the FIFO is available for data transfer when TDRA goes high. When the 2-Byte mode is selected, two successive bytes can be transferred when TDRA goes high.

The first byte (Address field) should be written into the Tx FIFO at the "Frame Continue" address. Then the transmission of a frame automatically starts. If the transmitter is in a mark idle state, the transfer of an address causes an opening flag within two or three transmitter clock cycles. If the transmitter has been in a time fill state, the current time fill flag being transmitted is assumed as an opening flag and the address field will follow it.

A frame continues as long as data is written into the Tx FIFO at the "Frame Continue" address. The ADLC internally keeps track of the field sequence in the frame. The frame format is described in the "FRAME FORMAT" section.

The frame is terminated by one of two methods. The most efficient way to terminate the frames from a software standpoint is to write the last data character into the Transmit FIFO "Frame Terminate" address (RS1, RS0 = 11) rather than the Transmit FIFO "Frame Continue" address (RS1, RS0 = 10). An alternate method is to follow the last write of data in the Tx FIFO "Frame Continue" address with the setting of the Transmit Last Data control bit. Either method causes the last character to be transmitted and the FCS field to automatically be appended along with a closing flag. Data for a new frame can be loaded into the Tx FIFO immediately after the old frame data, if TDRA is high. The closing Flag can serve as the opening Flag of the next frame or separate opening and closing Flags may be transmitted. If a new frame is not ready to be transmitted, the ADLC will automatically transmit the Active (Flag) or Inactive (Mark) Idle condition.

If the Tx FIFO becomes empty at any time during frame transmission (the FIFO has no data to transfer into transmitter shift register during transmission of the last half of the next to last bit of a word), an underrun will occur and the transmitter automatically terminates the frame by transmitting an abort. The underrun state is indicated by the Tx Underrun status bit.

Any time the Tx ABORT Control bit is set, the transmitter immediately aborts the frame (transmits at least 8 consecutive 1's) and clears the Tx FIFO. If the abort Extend Control bit is set at the time, an idle (at least 16 consecutive 1's) is transmitted. An abort or idle in an "out of frame" condition can be useful to gain 8 or 16 bits of delay. (For an example, see "Programming Considerations.")

The $\overline{CTS}$ ($\overline{Clear-To-Send}$) input and $\overline{RTS}$ ($\overline{Request-To-Send}$) output are provided for a MODEM or other hardware interface.

The TDRA/FC status bit (when selected to be Frame Complete Status) can cause an interrupt upon frame completion (i.e., a flag or abort completion).

Details regarding the inputs and outputs, status bits, control bits, and FIFO operation are described in their respective sections.

Receiver Operation — Data and a pre-synchronized clock are provided to the ADLC receiver section by means of the Receive Data (RxD) and Receive Clock (RxC) inputs. The data is a continuous stream of binary bits with the characteristic that a maximum of five "1's" can occur in succession unless Abort, Flag,

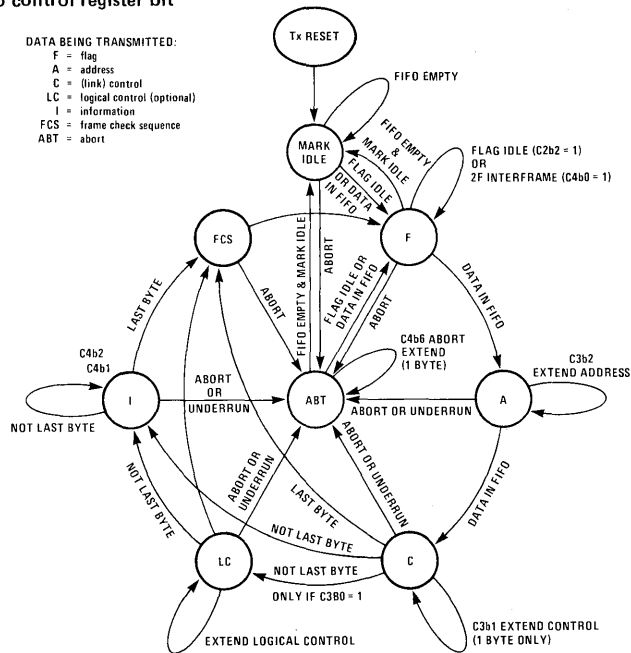Figure 7A. ADLC Transmitter State Diagram
C₁b₁ refers to control register bit

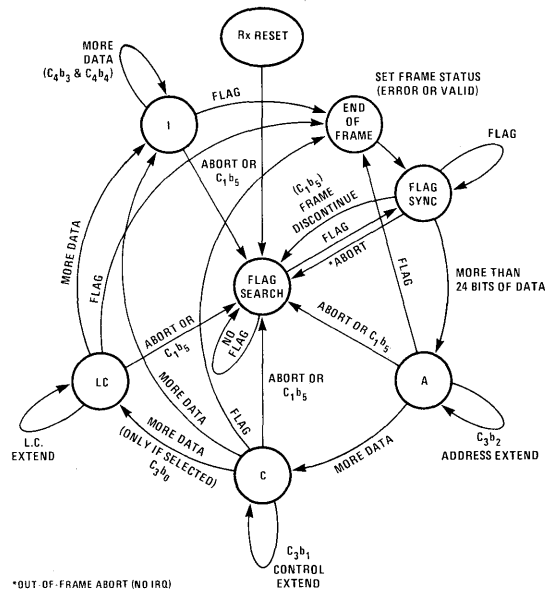DATA BEING TRANSMITTED:
F = flag
A = address
C = (link) control
LC = logical control (optional)
I = information
FCS = frame check sequence
ABT = abort

Figure 7B. ADLC Receiver State Diagram

*OUT-OF-FRAME ABORT (NO IRQ)

Operation (Continued)

or Idling condition occurs. The receiver continuously (on a bit-by-bit basis) searches for Flags and Aborts.

When a flag is detected, the receiver establishes frame synchronization to the flag timing. If a series of flags is received, the receiver resynchronizes to each flag.

If the frame is terminated before the internal buffer time expires (the frame data is less than 25 bits after an opening flag), the frame is simply ignored. Noise on the data input (RxD) during time fill can cause this kind of invalid frame.

Once synchronization has been achieved and the internal buffer time (24 bit times) expires data will automatically transfer to the Rx Data FIFO. The Rx Data FIFO is clocked by E to cause received data to move through the FIFO to the last empty register location. The Receiver Data Available status bit (RDA) indicates when data is present in the last register (Reg. #3) for the 1 Byte Transfer Mode. The 2 Byte Transfer Mode causes the RDA status bit to indicate data is available when the last two FIFO register locations (Reg. #2 and #3) are full. If the data character present in the FIFO is an address octet the status register will exhibit an Address Present status condition. Data being available in the Rx Data FIFO causes an interrupt to be initiated (assuming the receiver interrupt is enabled, RIE = "1"). The MPU will read the ADLC Status Register as a result of the interrupt or in its turn in a polling sequence. RDA or Address Present will indicate that receiver data is available and the MPU should subsequently read the Rx Data FIFO register. The interrupt and status bit will then be reset automatically. If more than one character had been received and was resident in the Rx Data FIFO, subsequent E clocks will cause the FIFO to update and the RDA status bit and interrupt will again be SET. In the two byte transfer mode both data bytes may be read on consecutive E cycles. Address Present provides for 1 byte transfers only.

The sequence of each field in the received frame is automatically handled by the ADLC. The frame format is described in the "FRAME FORMAT" section.

When a closing flag is received, the frame is terminated. The 16 bits preceding the closing flag are regarded as the FCS and are not transferred to the MPU. Whatever data is present in the most significant byte portion of the receiver buffer register is right justified and transferred to the Rx FIFO. The frame boundary pointer, which is explained in the "Rx FIFO REGISTER" section, is set simultaneously in the Rx FIFO. The frame boundary pointer sets the Frame Valid

status bit (when the frame was completed with no error) or the FCS/IF Error Status bit (when the frame was completed with error) when the last byte of the frame appears at the last location of the Rx FIFO. As long as the Frame Valid or FCS/IF Error status bit is set, the data transfer from the second location of the Rx FIFO to the last location of the Rx FIFO is inhibited.

Any time the Frame Discontinue control bit is set, the ADLC discards the current frame data in the ADLC without dropping flag synchronization. This feature can be used to ignore a frame which is addressed to another station.

The reception of an abort or idle is explained in the "FRAME FORMAT" section. The details regarding the inputs, outputs, status bits, control bits, and Rx FIFO operation are described in their respective sections.

Loop Mode Operation — The ADLC in the loop mode not only performs the transmission and receiving of data frames in the manner previously described but also has additional features for gaining and relinquishing loop control. In Figure 8a, a configuration is shown which depicts loop mode operation. The system configuration shows a primary station and several secondary stations. The loop is always under control of the primary station. When the primary wants to receive data, it transmits a Poll sequence and allows frame transmission to secondary stations on the loop. Each secondary is in series and adds one bit of delay to the loop. Secondary A in the figure receives data from the primary via its Rx Data Input, delays the data 1 bit, and transmits it to secondary B via its Tx Data Output. Secondaries B, C, and D operate in a similar manner. Therefore, data passes through each secondary and is received back by the primary controller.

Certain protocol rules must be followed in the manner by which the secondary station places itself on-loop (connects its transmitter output to the loop), goes active on the loop (starts transmitting its own stations' data on the loop), and goes off the loop (disconnects its transmitter output). Otherwise loop data to other stations down loop would be interfered. The data stream always flows the same way and the order in which secondary terminals are serviced is determined by the hardware configuration. The primary controller times the delay through the loop. Should it exceed n + 1 bit times, where n is the number of secondary terminals on the loop, it will indicate a loop failure. Control is transferred to a secondary by transmitting
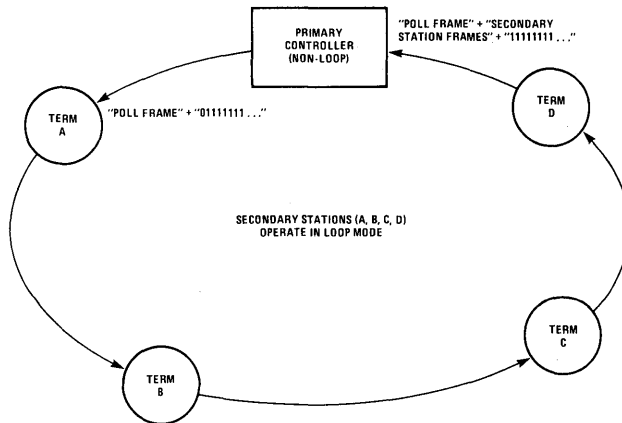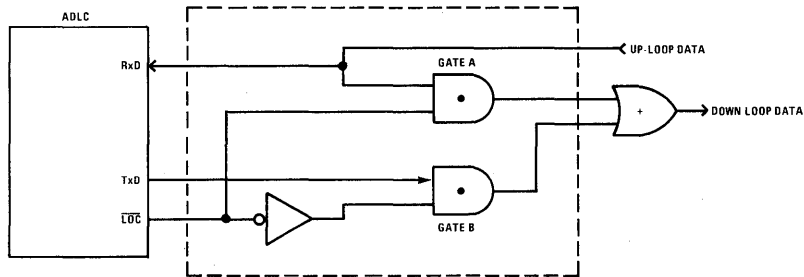
Figure 8A. Typical Loop Configuration

Figure 8B. Example of External Loop Logic

a "Go Ahead" signal following the closing Flag of a polling frame (request for a response from the secondary) from the primary station. The "Go Ahead" from the primary is a "0" and 7 "1's" followed by mark idling. The primary can abort its response request by interrupting its idle with flags. The secondary should immediately stop transmission and return control back to the primary. When the secondary completes its frame, a closing flag is transmitted followed by all "1"s. The primary detects the final 01111111 . . . ("Go Ahead" to the primary) and control is given back to the primary. Note that, if a down-loop secondary (e.g., station D) needs to insert

information following an up-loop station (e.g., station A), the go ahead to station D is the last "0" of the closing flag from station A followed by "1's".

The ADLC in the primary station should operate in a non-loop, full duplex mode. The ADLC in the secondaries should operate in a loop mode, monitoring up-loop data on its receiver data input. The ADLC can recognize the necessary sequences in the data stream to automatically go on/off the loop and to insert its own station data. The procedure is the following and is summarized in Table 1.

Table 1. Summary of Loop Mode Operation

STATE	RX SECTION	TX SECTION	LOOP STATUS BIT

OFF-LOOP	Rx section receives data from loop and searches for 7 "1's" (when On-Loop Control bit set) to go ON-LOOP.	Inactive
		1) NRZ MODE
		    Tx data output is maintained "high" (mark).
		2) NRZI MODE
		    Tx data output reflects the Rx data input state delayed by one bit time. (Not normally connected to loop.) The NRZI data is internally decoded to provide error-free transitions to On-Loop mode.
			"0"

ON-LOOP	1) When Go-Active on poll bit is set, Rx section searches for 01111111 pattern (the EOP or 'Go Ahead') to become the active terminal on the loop.
	2) When On-Loop control bit is reset, Rx section searches of 8 "1's" to go OFF-LOOP.
		Inactive
		1) NRZ MODE
		    Tx data output reflects Rx data input state delayed one bit time.
		2) NRZI MODE
		    Tx data output reflects Rx data input state delayed 2 bit times.
			"1"

ACTIVE	Rx section searches for flag (an interrupt from the loop controller) at Rx data input. Received flag causes $\overline{FD}$ output to go low. IRQ is generated if $\overline{RIE}$ and FDSE control bits are set.	Tx data originates within ADLC until Go Active on Poll bit is reset and a flag or Abort is completed. Then returns to ON-LOOP state.	"0"

(1) Go On-loop — when the ADLC powers up, the terminal station will be off line. The first task is to become an active terminal on the loop. The ADLC must be connected to a Loop Link via an external switch as shown in Figure 8b. After hardware reset, the ADLC $\overline{LOC}/\overline{DTR}$ Output will be in the high state and the up-loop receive data repeated through gate A to the down Loop stations. Any Up-Loop transmission will be received by the ADLC. The Loop/Non-Loop Mode Control bit (bit 5 in Control Register 3) must be set to place the ADLC in the Loop Mode. The ADLC now monitors its Rx Data input for a string of seven consecutive "1's" which will allow a station to go on line. The Loop operation may be monitored by use of the Loop Status bit in Status Register 1. After power up and reset, this bit is a zero. When seven consecutive ones are received by the ADLC the $\overline{LOC}/\overline{DTR}$ output will go to a low level, disabling gate A (refer to Figure 8b), enabling gate B and connecting the ADLC Tx Data output to the down Loop stations. The up Loop data is now repeated to the down Loop stations via the ADLC. A one bit delay is inserted in the data (in NRZI mode, there will be a 2 bit delay) as it circulates through the ADLC. The ADLC is now on-line and the Loop Status bit in Status Register 1 will be at a one.

(2) Go Active after Poll — The receiver section will monitor the up link data for a general or addressed poll command and the Tx FIFO should be loaded with data so that when the go-ahead sequence of a zero followed by seven ones (01111111 ---) is detected, transmission can be initiated immediately. When the polling frame is detected, the Go-Active-On-Poll control bit must be set (bit 6 in Control Register 3). A minimum of seven bit times are available to set this control bit after the closing flag of the poll. When the Go-Ahead is detected by the receiver, the ADLC will automatically change the seventh one to a zero so that repeated sequence out gate B in Figure 8b is now opening flag sequence (01111110). Transmission now continues from the Tx FIFO with data (address, control, etc.) as previously described. When the ADLC has gone active-on-poll, the Loop Status bit in Status Register 1 will go to a zero. The receiver searches for a flag, which indicates that the primary station is interrupting the current operation.

(3) Go Inactive when On-Loop — The Go-Active-On Poll control bit may be RESET at any time during transmission. When the frame is complete (the closing Flag or abort is transmitted), the Loop is automatically released and the station reverts back to being

just a one bit delay in the Loop, repeating up link data. If the Go-Active-On-Poll control bit is not reset by software and the final frame is transmitted (Flag/Mark Idle bit = 0), then the transmitter will mark idle and will not release the loop to up-loop data. A Tx Abort command would have to be used in this case in order to go inactive when on the loop. Also, if the Tx FIFO was not preloaded with data (address, control, etc.) prior to changing the "Go Ahead Character" to a Flag, the ADLC will either transmit flags (active idle character) until data is loaded (when Flag/Mark Idle Control bit is high) or will go into an underrun condition and transmit an Abort (when Flag/Mark Idle control bit is low). When an abort is transmitted, the Go-Active-on-Poll control bit is reset automatically and the ADLC reverts to its repeating mode, (TxD = delayed RxD). When the ADLC transmitter lets go of the loop, the Loop Status bit will return to a "1", indicating normal on-loop retransmission of up-loop data.

4) Go Off-Loop — The ADLC can drop-off the Loop (go off-line) similar to the way it went on-line. When the Loop On-Line control bit is reset the ADLC receiver section looks for 8 successive "1's" before allowing the $\overline{\text{LOC}/\text{DTR}}$ output to return high (the inactive state). Gate A in Figure 8b will be enabled and Gate B disabled allowing the loop to maintain continuity without disturbance. The Loop Status bit will show an off-line condition (logical zero).

Input/Output Functions

All inputs of ADLC are high impedance and TTL compatible level inputs. All outputs of the ADLC are compatible with standard TTL. Interrupt Request (IRQ), however, is an open drain output (no internal pull-up).

Interface for MPU

D0-D7

Bidirectional Data Bus — These data bus I/O ports allow the data transfer between ADLC and system bus. The data bus drivers are three-state devices that remain in the high impedance (off) state except when the MPU performs an ADLC read operation.

E

Enable Clock — E activates the address inputs ($\overline{\text{CS}}$, RS0 and RS1) and R/W input and enables the data transfer on the data bus. E also move data through the Tx FIFO and Rx FIFO. E should be a free running clock such as the S6800 MPU system clock.

$\overline{\text{CS}}$

Chip Select — An ADLC read or write operation is enabled only when the $\overline{\text{CS}}$ input is low and the E clock input is high. (E • $\overline{\text{CS}}$).

RS0
RS1
Register Selects — When the Register Select inputs are enabled by (E • $\overline{\text{CS}}$), they select internal registers in conjunction with the Read/Write input and Address Control bit (control register 1, bit 0). Register addressing is defined in Table 2.

R/W

Read/Write Control Line — The R/W input controls the direction of data flow on the data bus when it is enabled by (E • CS). When R/W is high, the I/O Buffer acts as an output driver and as an input buffer when low. It also selects the Read Only and Write Only registers within the ADLC.

$\overline{\text{RESET}}$

Reset Input — The $\overline{\text{RESET}}$ Input provides a means of resetting the ADLC from a hardware source. In the "low state," the $\overline{\text{RESET}}$ Input causes the following:

☐ Rx Reset and Tx Reset are SET causing both the Receiver and Transmitter sections to be held in a reset condition.

☐ Resets the following control bits: Transmit Abort, RTS, Loop Mode, and Loop On-Line/DTR.

☐ Clears all stored status condition of the status registers.

☐ Outputs: $\overline{\text{RTS}}$ and $\overline{\text{LOC}/\text{DTR}}$ go high. TxD goes to the mark state ("1's" are transmitted).

When $\overline{\text{RESET}}$ returns "high" (the inactive state) the transmitter and receiver sections will remain in the reset state until Tx Reset and Rx Reset are cleared via the data bus under software control. The Control Register bits affected by $\overline{\text{RESET}}$ cannot be changed when $\overline{\text{RESET}}$ is "low".

$\overline{\text{IRQ}}$

Interrupt Request Output — $\overline{\text{IRQ}}$ will be low if an interrupt situation exists and the appropriate interrupt enable has been set. The interrupt remains as long as the cause for the interrupt is present and the enable is set.

Clock and Data of Transmitter and Receiver

TxC

Transmitter Clock Input — The transmitter shifts data

on the negative transition of the TxC clock input. When the Loop Mode or Test Mode is selected, TxC should be the same frequency and phase as the RxC clock. The data rate of the transmitter should not exceed the E frequency.

RxC

Receiver Clock Input — The receiver samples the data on the positive transition of the TxC clock. RxC should be synchronized with receive data externally.

TxD

Transmit Data Output — The serial data from the transmitter is coded in NRZ or NRZI (Zero Complement) data format.

RxD

Receiver Data Input — The serial data to be received by the ADLC can be coded in NRZ or NRZI (Zero Complement) data format. The data rate of the receiver should not exceed the E frequency. If a partial byte reception is possible at the end of a frame, the maximum data rate of the receiver is indicated by the following relationship:

$$f_{RxC} \leqslant \frac{1}{2t_E + 300ns}$$

where t_E is the period of E.

Peripheral/Modem Control

$\overline{RTS}$

Request to Send Output — The Request-to-Send output is controlled by the Request-to-Send control bit in conjunction with the state of the transmitter section. When the RTS bit goes high, the $\overline{RTS}$ output is forced low. When the RTS bit returns low, the $\overline{RTS}$ output remains low until the end of the frame. The positive transition of $\overline{RTS}$ occurs after the completion of a Flag, an Abort, or when the RTS control bit is reset during a mark idling state. When the $\overline{RESET}$ input is low, the $\overline{RTS}$ output goes high.

$\overline{CTS}$

Clear to Send Input — The $\overline{CTS}$ input provides a real-time inhibit to the TDRA status bit and its associated interrupt. The positive transition of $\overline{CTS}$ is stored within the ADLC to insure its occurrence will be acknowledged by the system. The stored CTS information and its associated IRQ (if enabled) are cleared by writing a "1" in the Clear Tx Status bit or in the Transmitter Reset bit.

$\overline{DCD}$

Data Carrier Detect Input — The $\overline{DCD}$ input provides a real-time inhibit to the receiver section. A high level on the $\overline{DCD}$ input resets and inhibits the receiver register, but data in the Rx FIFO from a previous frame is not disturbed. The positive transition of $\overline{DCD}$ is stored within the ADLC to insure that its occurrence will be acknowledged by the system. The stored DCD information and its associated IRQ (if enabled) are cleared by means of the Clear Rx Status Control bit or by the Rx Reset bit.

$\overline{LOC}/\overline{DTR}$

Loop On Line Control/Data Terminal Ready output — The $\overline{LOC}/\overline{DTR}$ output serves as a $\overline{DTR}$ output in the non-loop mode or as a Loop Control output in the loop mode. When $\overline{LOC}/\overline{DTR}$ output performs the $\overline{DTR}$ function, it is turned on and off by means of the LOC/DTR control bit. When the Loc/DTR control bit is high the $\overline{DTR}$ output will be low. In the loop mode the $\overline{LOC}/\overline{DTR}$ output provides the means of controlling the external loop interface hardware to go On-line or Off-line. When the LOC/DTR control bit is SET and the loop has "idled" for 7 bit times or more (RxD) = 01111111 . . .), the $\overline{LOC}/\overline{DTR}$ output will go low (on-line). When the LOC/DTR control bit is low and the loop has "idled" for 8 bit times or more, the $\overline{LOC}/\overline{DTR}$ output will return high (off-line). The $\overline{RESET}$ input being low will cause the $\overline{LOC}/\overline{DTR}$ output to be high.

$\overline{FD}$

Flag Detect Output — An output to indicate the reception of a flag and initiate an external time-out counter for the loop mode operation. The $\overline{FD}$ output goes low for one bit time beginning at the last bit of the flag character, as sampled by the receiver clock (RxC).

DMA Interface

RDSR

Receiver Data Service Request Output — The RDSR Output is provided primarily for use in DMA Mode operation and indicates (when high) that the Rx FIFO requests service (RSDR output reflects the RDA status bit). If the prioritized Status Mode is selected, RDSR will be inhibited when any other receiver status conditions are present. RDSR goes low when the Rx FIFO is read.

TDSR

Transmitter Data Service Request Output — The TDSR Output is proivded for DMA mode operation and indicates (when high) that the Tx FIFO requests

service (TDSR reflects the TDRA status bit). TDSR goes low when the Tx FIFO is loaded. TDSR is inhibited by: The Tx Rs control bit being SET, $\overline{\text{RESET}}$ being low, or $\overline{\text{CTS}}$ being high. If the prioritized status mode is used, Tx underrun also inhibits TDSR.

ADLC Registers

Eight registers in the ADLC can be accessed by means of the MPU data and address buses. The registers are defined as read only or write only according to the direction of information flow. The addresses of these registers are defined in Table 2. The transmitter FIFO register can be accessed by two different addresses, the "Frame Terminate" address and the "Frame Continue" address. (The function of these addresses are discussed in the FIFO section.)

Table 2. Register Addressing

Register Selected	R/W	RS1	RS0	Address Control Bit (C_1b_0)
Write Control Register #1	0	0	0	X
Write Control Register #2	0	0	1	0
Write Control Register #3	0	0	1	1
Write Transmit FIFO (Frame Terminate)	0	1	1	0
Write Control Register #4	0	1	1	1
Read Status Register #1	1	0	0	X
Read Status Register #2	1	0	1	X
Read Receiver FIFO	1	1	X	X

Receiver Data First-In First-Out Register

Rx FIFO

The Rx FIFO consists of three 8-bit registers which are used for the buffer storage of received data. Data bytes are always transferred from a full register to an adjacent empty register; and both phases of the E input clock are used for the data transfer. Each register has pointer bits which point the frame boundary. When these pointers appear at the last FIFO location, they update the Address Present, Frame Valid or FCS/IF Error status bits.

The RDA status bit indicates the state of the Rx

FIFO. When RDA status bit is "1", the Rx FIFO is ready to be read. The RDA status is controlled by the 2 Byte/1 Byte control bit. When overrun occurs, the data in the first byte of the Rx FIFO are no longer valid.

Both the Rx Reset bit and $\overline{\text{Reset}}$ input clear the Rx FIFO. Abort ("In Frame") and a high level on the $\overline{\text{DCD}}$ input also clears the Rx FIFO, but the last bytes of the previous frame, which are separated by the frame boundary pointer, are not disturbed.

Transmitter Data First-In First-Out Register

Tx FIFO

The Tx FIFO consists of three 8-bit registers which are used for buffer storage of data to be transmitted. Data is always transferred from a full register to an empty adjacent register; the transfer occurs on both phases of the E input clock. The Tx FIFO can be addressed by two different register addresses, the "Frame Continue" address and the "Frame Terminate" address. Each register has pointer bits which point to the frame boundary. When a data byte is written at the "Frame Continue" address, the pointer of the first FIFO register is set. When a data byte is written at the "Frame Terminate" address, the pointer of the first FIFO register is reset. RxRs control bit or Tx Abort control bit resets all pointers. The pointer will shift through the FIFO. When positive transition is detected at the third location of FIFO, the transmitter initiates a frame with an open flag. When the negative transition is detected at the third location of FIFO, the transmitter closes a frame, appending the FCS and closing Flag to the last byte.

The Tx last control bit can be used instead of using the "Frame Terminate" address. When the Tx last control bit is written by a "1", the logic searches the last byte location in the FIFO and resets the pointer in the FIFO register.

The status of Tx FIFO is indicated by the TDRA status bit. When TDRA is "1", the Tx FIFO is available for loading data. The TDRA status is controlled by the 2BYTE/1BYTE control bit. The Tx FIFO is reset by both Tx Reset and $\overline{\text{RESET}}$ input. During this reset condition or when $\overline{\text{CTS}}$ input is high, the TDRA status bit is suppressed and data loading is inhibited.

Table 3. ADLC Internal Register Structure

	Bit #	RS1 RS0 = 00 Status Register #1	RS1 RS0 = 01 Status Register #2	RS1 RS0 = 10 Receiver Data Register	RS1 RS0 = 11
Read Only Registers	0	RDA	Address Present	Bit 0	
	1	Status #2 Read Request	Frame Valid	Bit 1	
	2	Loop On Line	Inactive Idle Received	Bit 2	
	3	Flag Detected (When Enabled)	Abort Received	Bit 3	Not Used
	4	$\overline{\text{CTS}}$	FCS Error	Bit 4	
	5	Tx Underrun	$\overline{\text{DCD}}$	Bit 5	
	6	TDRA/Frame Complete	Tx Overrun	Bit 6	
	7	IRQ Present	RDA (Receiver Data Available)	Bit 7	

	Bit #	Control Register #1	Control Register #2 ($C_1 b_0 = 0$)	Control Register #3 ($C_1 b_0 = 1$)	Transmitter Data (Continue Data)	Transmitter Data (Last Data) ($C_1 b_0 = 0$)	Control Register #4 $C_1 b_0 = 1$
Write Only Registers	0	Address Control (AC)	Prioritized Status Enable	Logical Control Field Select	Bit 0	Bit 0	Double Flag/Single Flag Interframe Control
	1	Receiver Interrupt Enable (RIE)	2 Byte/1 Byte Transfer	Extended Control Field Select	Bit 1	Bit 1	Word Length Select Transmit #1
	2	Transmitter Interrupt Enable (TIE)	Flag/Mark Idle	Auto, Address Extension Mode	Bit 2	Bit 2	Word Length Select Transmit #2
	3	RDSR Mode (DMA)	Frame Complete/ TDRA Select	01/11 Idle	Bit 3	Bit 3	Word Length Select Receive #1
	4	TDSR Mode (DMA)	Transmit Last Data	Flag Detected Status Enable	Bit 4	Bit 4	Word Length Select Receive #2
	5	Rx Frame Discontinue	CLR Rx Status	Loop/Non-Loop Mode	Bit 5	Bit 5	Transmit Abort
	6	Rx RESET	CLR Tx Status	Go Active on Poll/Test	Bit 6	Bit 6	Abort Extend
	7	Tx RESET	RTS Control	Loop On-Line Control DTR	Bit 7	Bit 7	NRZI/NRZ

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Control Registers

Control Register 1 (CR1)

RS1 RS0 R/W AC	7	6	5	4	3	2	1	0
0 0 0 X	TxRS	RxRS	Discontinue	TDSR Mode	RDSR Mode	TIE	RIE	AC

b_0 Address Control (AC) — AC provides another RS (Register Select) signal internally. The AC bit is used in conjunction with RS0, RS1 and R/W inputs to select particular registers, as shown in Table 2.

b_1 Receiver Interrupt Enable (RIE) — RIE enables/ disables the interrupt request caused by the receiver section. 1 . . . enable, 0 . . . disable.

b_2 Transmitter Interrupt Enable (TIE) — TIE enables/ disables the interrupt request caused by the transmitter. 1 . . . enable, 0 . . . disable.

b_3 Receiver Data Service Request Mode (RDSR Mode) — The RDSR Mode bit provides the capability of operation with a bus system in the DMA mode when used in conjunction with the prioritized status mode. When RDSR MODE is set, and interrupt request caused by RDA status is inhibited, and the ADLC does not request data transfer via the $\overline{IRQ}$ output.

b_4 Transmitter Data Service Request Mode (TDSR MODE) — The TDSR MODE bit provides the capability of operation with a bus system in the DMA mode when used in conjunction with the prioritized status mode. When TDSR MODE is set, and interrupt request caused by TDRA status is inhibited, and the ADLC does not request a data transfer via the $\overline{IRQ}$ output.

b_5 Rx Frame Discontinue (DISCONTINUE) — When the DISCONTINUE bit is set, the currently re-ceived frame is ignored and the ADLC discards the data of the current frame. The DISCONTINUE bit is automatically reset when the last byte of the frame is discarded. When the ignored frame is aborted by receiving an Abort or DCD failure, the DISCONTINUE bit is also reset.

b_6 Receiver Reset (Rx Rs) — When the Rx Rs bit is "1", the receiver section stays in the reset condition. All receiver sections including the Rx FIFO register and the receiver status bits in both status registers, are reset. (During reset, the stored DCD status is reset but the DCD status bit follows the $\overline{DCD}$ input. Rx Rs is set by forcing a low level on the $\overline{RESET}$ input or by writing a "1" into this bit from the data bus. Rx Rs must be reset by writing a "0" from the data bus after $\overline{RESET}$ has gone high.

b_7 Transmitter Reset (Tx Rs) — when the Tx Rs bit is "1", the transmitter section stays in the reset condition and transmits marks ("1's"). All transmitter sections, including the Tx FIFO and the transmitter status bits in both status registers, are reset (FIFO cannot be loaded). During reset, the stored $\overline{CTS}$ status is reset but the CTS status bit follows the $\overline{CTS}$ input. Tx Rs is set by forcing a low level on the $\overline{RESET}$ input or by writing a "1" from the data bus. It must be reset by writing a "0" after $\overline{RESET}$ has gone high.

Control Register 2 (CR2)

			7	6	5	4	3	2	1	0
RS1 RS0 R/W AC			RTS	CLR	CLR	Tx	FC/TDRA	F/M	2/1	PSE
0 1 0 0				TxST	RxST	Last	Select	Idle	Byte	

b0 Prioritized Status Enable (PSE) — When the PSE bit is SET, the status bits in both status registers are prioritized as defined in the Status Register section. When PSE is low, the status bits indicate current status without bit suppression by other status bits. The exception to this rule is the $\overline{CTS}$ status bit which always suppresses the TDRA status.

b1 2 Byte/1 Byte Transfer (2/1 Byte) — When the 2/1 Byte bit is RESET the TDRA and RDA status bits then will indicate the availability of their respective data FIFO registers for a single byte data transfer. Similarly, if 2/1 Byte is set, the TDRA and RDA status bits indicate when two bytes of data can be moved without a second status read.

b2 Flag/Mark Idle Select (F/M Idle) — The F/M Idle bit selects Flag characters or bit by bit Mark Idle for the time fill or the idle state of the transmitter. When Mark Idle is selected, Go-Ahead code can be generated for loop operation in conjunction with the 01/11 Idle control bit (C3b3). 1 . . . Flag time fill, 0 . . . Mark Idle.

b3 Frame Complete/TDRA Select (FC/TDRA Select) — The FC/TDRA Select bit selects TDRA status or FC status for the TDRA/FC status bit indication. 1 . . . FC status, 0 . . . TDRA status.

b4 Transmit Last Data (Tx Last) — Tx Last bit provides another method to terminate a frame. When the Tx Last bit is set just after loading a data byte,

the ADLC assumes the byte is the last byte and terminates the frame by appending CRCC and a closing Flag. This control bit is useful for DMA operation. Tx Last bit automatically returns to the "0" state.

b5 Clear Receiver Status (CLR Rx ST) — When a "1" is written into the CLR Rx ST bit, a reset signal is generated for the receiver status bits in status register # 1 and # 2 (except AP and RDA bits). The reset signal is enabled only for the bits which have been present during the last "read status" operation. The CLR Rx ST bit automatically returns to the "0" state.

b6 Clear Transmitter Status (CLR TxST) — When a "1" is written into CLR TxST bit, a reset signal is generated for the transmitter status bits in status register # 1 (except TDRA). The reset signal is enabled for the bits which have been present during the last "read status" operation. The CLR TxST bit automatically returns to the "0" state.

b7 Request to Send Control (RTS) — The RTS bit when high causes the $\overline{RTS}$ output to be low (the active state). When the RTS bit returns low and data is being transmitted, the $\overline{RTS}$ output remains low until the last character of the frame (the closing Flag or Abort) has been completed. If the transmitter is idling when the RTS bit return low, the $\overline{RTS}$ output will go high (the inactive state) within two bit times.

Control Register 3 (CR3)

RS1 RS0 R/W AC	7	6	5	4	3	2	1	0
	LOC/	GAP/	Loop	FDSE	01/11	AEX	CEX	LCF
0 1 0 1	DTR	TST			Idle			

b_0 Logical Control Field Select (LCF) — The LCF select bit causes the first byte(s) of data belonging to the information field to remain 8 bit characters until the logical control field is complete. The logical control field (when selected) is an automatically extendable field which is extended when bit 7 of a logical control character is a "1". When the LCF Select bit is reset the ADLC assumes no logical control field is present for either the transmit or received data channels. When the logical control field is terminated, the word length of the information data is then defined by WLS_1 and WLS_2.

b_1 Extended Control Field Select (C_{EX}) — When the C_{EX} bit is a "1", the control field is extended and assumed to be 16 bits. When C_{EX} is "0", the control field is assumed to be 8 bits.

b_2 Auto/Address Extend Mode (A_{EX}) — The A_{EX} bit when "low" allows full 8 bits of the address octet to be utilized for addressing because address extension is inhibited. When the A_{EX} bit is "high", bit 0 of address octet equal to "0" causes the Address field to be extended by one octet. The exception to this automatic address field extension is when the first address octet is all "0's" (the Null Address).

b_3 01/11 Idle (01/11 Idle) — The 01/11 Idle Control bit determines whether the inactive (Mark) idle condition begins with a "0" or not. If the 01/11 Idle Control is SET, the closing flag (or Abort) will be followed by a 011111 ... pattern. This is required of the controller for the "Go Ahead" character in the Loop Mode. When 01/11 is RESET, the idling condition will be all "1's".

b_4 Flag Detect Status Enable (FDSE) — The FDSE bit enables the FD status bit in Status Register #1 to indicate the occurrence of a received Flag character. The status indication will be accompanied by an interrupt if RIE is SET. Flag detection will cause the Flag Detect output to go low for one bit time regardless of the state of FDSE.

b_5 LOOP/NON-LOOP Mode (LOOP) — When the LOOP bit is set, loop mode operation is selected and the GAP/TST control bit, LOC/DTR control bit and $\overline{\text{LOC/DTR}}$ output are selected to perform the loop control functions. When LOOP is reset, the ADLC operates in the point to point data communications mode.

b_6 Go Active On Poll/Test (GAP/TST) — In the Loop Mode — The GAP/TST bit is used to respond to the poll sequence and to begin transmission. When GAP/TST is set, the receiver searches for the "Go Ahead" (or End of Poll, EOP). The receiver "Go Ahead" is converted to an opening Flag and the ADLC starts its own transmission. When GAP/TST is reset during the transmission; the end of the frame (the completion of Flag or Abort) causes the termination of the "go-active-on-poll" operation and the Rx Data to Tx Data link is re-established. The ADLC then returns to the "loop-on-line" state.

In the Non-loop Mode — The GAP/TST bit is used for self-test purposes. If GAP/TST bit is set, the TxD output is connected to the RxD input internally, and provides a "loop-back" feature. For normal operation, the GAP/TST bit should be reset.

b_7 Loop On-Line Control/DTR Control (LOC/DTR) — In the Loop Mode — The LOC/DTR bit is used to go on-line or to go off-line. When LOC/DTR is set, the ADLC goes to the on-line state after 7 consecutive "1's" occur at the RxD input. When LOC/DTR is reset, the ADLC goes to the "off-line" state after eight consecutive "1's" occur at the RxD input.

In the Non-Loop Mode — The LOC/DTR bit directly controls the Loop On-Line/DTR output state. 1 ... DTR output goes to low level. 0 ... $\overline{\text{DTR}}$ output goes to high level.

Control Register 4 (CR4)

	7	6	5	4	3	2	1	0
RS1 RS0 R/W AC	NRZI/NRZ	ABT$_{EX}$	ABT	Rx		Tx		"FF"/F
1 1 0 1				WLS$_2$ WLS$_1$		WLS$_2$ WLS$_1$		

b0 Double Flag/Single Flag Interframe Control ("FF" /"F") — The "FF"/"F" Control bit determines whether the transmitter will transmit separate closing and opening Flags when frames are transmitted successively. When the "FF"/"F" control bit is low, the closing flag of the first frame will serve as the opening flag of the second frame. When the bit is high, independent opening and closing flags will be transmitted.

b1 Transmitter Word Length Select (Tx WLS1 and WLS2).

b2 — Tx WLS1 and WLS2 are used to select the word length of the transmitter information field. The encoding format is shown in Table 4.

Table 4. I-Field Character Length Select

WLS$_1$	WLS$_2$	I-Field Character Length Length
0	0	5 bits
1	0	6 bits
0	1	7 bits
1	1	8 bits

b3 Receiver Word Length Select (Rx WLS1 and WLS2)

b4 Rx WLS1 and WLS2 are used to select the word length of the receiver information field. The encoding format is shown in Table 4.

b5 Transmit Abort (ABT) — The ABT bit causes an Abort (at least 8 bits of "1" in succession) to be transmitted. The Abort is initiated and the Tx FIFO is cleared when the control bit goes high. Once Abort begins, the Tx Abort control bit assumes the low state.

b6 Abort Extend (ABT$_{EX}$) — If ABT$_{EX}$ is set, the abort code initiated by ABT or the underrun condition is extended up to at least 16 bits of

consecutive "1's", the mark Idle State.

b7 NRZI (Zero Complement)/NRZ Select (NRZI/ NRZ) — NRZI/NRZ bit selects the transmit/ receive data format to be NRZI or NRZ in both Loop Mode or Non-Loop mode operation. When the NRZI Mode is selected, a 1 bit delay is added to the transmitted data (TxD) to allow for NRZI encoding. 1 . . . NRZI, 0 . . . NRZ.

NOTE: NRZI coding — The serial data remains in the same state to send a binary "1" and switches to the opposite state to send a binary "0".

Status Register

The Status Register # 1 is the main status register. The IRQ bit indicates whether the ADLC requests service or not. The S2RQ bit indicates whether any bits in status register # 2 request any service. TDRA and RDA, because they are most often used, are located in bit positions that are more convenient to test, RDA reflects the state of the RDA bit in status register # 2.

The Status Register # 2 provides the detailed status information contained in the S2RQ bit and these bits reflect receiver status. The FD bit is the only receiver status, which is not indicated in status register # 2.

The prioritized status mode provides maximum efficiency in searching the status bits and indicates only the most important action required to service the ADLC. The priority trees of both status registers are provided in Figure 9.

Reading the status register is a non-destructive process. The method of clearing status depends upon the bit's function and is discussed for each bit in the register.

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Status Register 1 (SR1)

		7	6	5	4	3	2	1	0
RS1 RS0 R/W AC		IRQ	TDRA/FC	TXU	CTS	FD	LOOP	S2RQ	RDA
0 0 1 X									

b0 Receiver Data Available (RDA) — The RDA status bit reflects the state of the RDA status bit in status Register # 2. It provides the means of achieving data transfers of received data in the full Duplex Mode without having to read both status registers.

b1 Status Register #2 Read Request (S2RQ) — All the status bits (stored conditions) of status register # 2 (except RDA bit) are logically OR-ed and indicated at by the S2RQ status bit. Therefore S2RQ indicated that status register #2 needs to be read. When S2RQ is "0", it is not necessary to read status register #2. The bit is cleared when the appropriate bits in Status Register #2 are cleared or when Rx Reset is used.

b2 Loop Status (LOOP) — The LOOP status bit is used to monitor the loop operation of the ADLC. This bit does not cause an IRQ. When Non-Loop Mode is selected, LOOP bit stays "0". When Loop Mode is selected, the LOOP status bit goes to "1" during "On-Loop" condition. When ADLC is in an "Off-Loop" condition or "Go-Active-On-Poll" condition, the LOOP status bit is a "0".

b3 Flag Detected (FD) — the FD Status bit indicates that a flag has been received if the Flag Detect Enable control bit has been set. The bit goes high at the last bit of the Flag Character received (when the Flag Detect Output goes low) and is stored until cleared by Clear Rx Status or Rx Reset.

b4 Clear To Send (CTS) — The $\overline{CTS}$ input positive transition is stored in the status register and causes an IRQ (if Enabled). The stored CTS condition and its IRQ are cleard by Clear Tx Status control bit or Tx Reset bit. After the stored status is reset, the CTS status bit reflects the state of the $\overline{CTS}$ input.

b5 Transmitter Underrun (TxU) — When the transmitter runs out of data during a frame transmission, an underrun occurs and the frame is automatically terminated by transmitting an Abort. The underrun condition is indicated by the TxU status bit. TxU can be cleared by means of the Clear Tx Status Control bit or by Tx Reset.

b6 Transmitter Data Register Available/Frame Complete (TDRA/FC) — The TDRA Status bit serves two purposes depending upon the state of the Frame Complete/TDRA Select control bit. When this bit serves as a TDRA status bit, it indicates that data (to be transmitted) can be loaded into the Tx Data FIFO register. The first register (Reg. #1) of the Tx Data FIFO being empty (TDRA = "1") will be indicated by the TDRA Status bit in the "1-Byte Transfer Mode". The first two registers (Reg. #1 and #2) must be empty for TDRA to be high and when in the "2-Byte Transfer Mode". TDRA is inhibited by Tx Reset, or $\overline{CTS}$ being high.

When the Frame Complete Mode of operation is selected, the TDRA/FC status bit goes high when a Flag or Abort has been transmitted. The bit remains high until cleared by resetting the TDRA/FC control bit or setting the Tx Reset bit.

b7 Interrupt Request (IRQ) — The Interrupt Request status bit indicates when the $\overline{IRQ}$ output is in the active state ($\overline{IRQ}$ Output = "0"). The IRQ status bit is subject to the same interrupt enables (RIE, TIE) as the $\overline{IRQ}$ output. The IRQ status bit simplifies status inquiries for polling systems by providing single bit indication of service requests.

Figure 9. Status Register Priority Tree (PSE = 1)
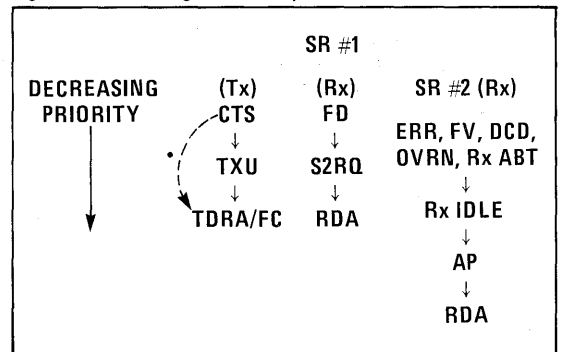
*Prioritized even when PSE = 0
NOTE: Status bit above will inhibit one below it.

Status Register 2 (SR2)

		7	6	5	4	3	2	1	0
RS1 RS0 R/W AC		RDA	OVRN	DCD	ERR	Rx	Rx	FV	AP
0 1 1 X						ABT	Idle		

b0 Address Present (AP) — The AP status bit provides the frame boundary and indicates an Address octet is available in the Rx Data FIFO register. In the Extended Addressing Mode, the AP bit continues to indicate addresses until the Address field is complete. The Address present status bit is cleared by reading data or by Rx Reset.

b1 Frame Valid (FV) — The FV status bit provides the frame boundary indication to the MPU and also indicates that a frame is complete with no error. The FV status bit is set when the last data byte of a frame is transferred into the last location of the Tx FIFO (available to be read by MPU). Once FV status is set, the ADLC stops further data transfer into the last location of the Rx FIFO (in order to prevent the mixing of two frames) until the status bit is cleared by the Clear Rx Status bit or Rx Reset.

b2 Inactive Idle Received (Rx Idle) — The Rx Idle status bit indicates that a minimum of 15 consecutive "1's" have been received. The event is stored within the status register and can cause an interrupt. The interrupt and stored condition are cleared by the Clear Rx Status Control bit. The Status bit is the Logical OR of the receiver idling detector (which continues to reflect idling until a "0" is received) and the stored inactive idle condition.

b3 Abort Received (RxABT) — The RxABT status bit indicates that 7 or more consecutive "1's" have been received. Abort has no meaning under out-of-frame conditions; therefore, no interrupt nor storing of the status will occur unless a Flag has been detected prior to the Abort. An Abort Received when "in frame" is stored in the status register and causes an IRQ. The status bit is the logical OR of the stored conditions and the Rx Abort detect logic, which is cleared after 15 consecutive "1's" have occurred. The stored

Abort condition is cleared by the Clear Rx Status Control bit or Rx Reset.

b4 Frame Check Sequence/Invalid Frame Error (ERR) — When a frame is complete with a cyclic redundancy check (CRC) error or a short frame error (the frame does not have complete Address and Control fields), the ERR status bit is set instead of the Frame Valid status bit. Other functions, frame boundary indication and control function, are exactly the same as for the Frame Valid status bit. Refer to the FV status bit.

b5 Data Carrier Detect (DCD) — A positive transition on the $\overline{DCD}$ input is stored in the status register and causes an IRQ (if enabled). The stored DCD condition and its IRQ are cleared by the Clear Rx Status Control bit or RX Reset. After stored status is reset, the DCD status bit follows the state of the input. Both the stored $\overline{DCD}$ condition and the $\overline{DCD}$ input cause the reset of the receiver section when they are high.

b6 Receiver Overrun (OVRN) — OVRN status indicates that receiver data has been transferred into the Rx FIFO when it is full, resulting in data loss. The OVRN status is cleared by the Clear Rx Status bit or Rx Reset. Continued overrunning only destroys data in the first FIFO register.

b7 Receiver Data Available (RDA) — The Receiver Data Available status bit indicates when receiver data can be read from the Rx Data FIFO. When the prioritized status mode is used, the RDA bit indicates that non-Address and non-last data are available in the Rx FIFO. The receiver data being present in the last register of the FIFO causes RDA to be high for the "1 Byte Transfer Mode". The RDA bit being high indicates that the last two registers are full when in the "2 Byte Transfer Mode". The RDA status bit is reset automatically when data is not available.

Programming Considerations

1. **Status Priority** — When the prioritized status mode is used, it is best to test for the lowest priority conditions first. The lowest priority conditions typically occur more frequently and are the most likely conditions to exist when the processor is interrupted.

2. **Stored vs Present Status** — Certain status bits (DCD, CTS, Rx Abort, and Rx Idle) indicate a status which is the logical OR of a stored and a present condition. It is the stored status that causes an interrupt and which is cleared by a Status Clear control bit. After being cleared, the status register will reflect the present condition of an input or a receiver input sequence.

3. **Clearing Status Registers** — In order to clear an interrupt with the two Status Clear control bits, a particular status condition must be read before it can be cleared. In the prioritized mode, clearing a higher priority condition might result in another $\overline{\text{IRQ}}$ caused by a lower priority condition whose status was suppressed when a status register was first read. This guarantees that a status condition is never inadvertently cleared.

4. **Clearing the Rx FIFO** — An Rx Reset will effectively clear the contents of all 3 Rx FIFO bytes. However, the FIFO may contain data from 2 different frames when an overrun, abort, or DCD failure occurs. When this happens, the data from a previously closed frame (a frame whose closing flag has been received) will not be destroyed.

5. **Servicing the Rx FIFO in a 2 Byte Mode** — The procedure for reading the last bytes of data is the same, regardless of whether the frame contains an even or an odd number of bytes. Continue to read 2 bytes until an interrupt occurs that is caused by an end of frame status (FV or ERR). When this occurs, indicating the last byte either has been read or is ready to be read, switch temporarily to the 1-byte mode with no prioritized status (control register 2). Test RDA to indicate whether a 1-byte read should be performed. Then clear the frame and status.

6. **Frame Complete Status and $\overline{\text{RTS}}$ Release** — In many cases, a MODEM will require a delay for releasing $\overline{\text{RTS}}$. An 8-bit or 16-bit delay can be added to the ADLC $\overline{\text{RTS}}$ output by using an Abort. At the end of a transmission, frame complete status will indicate the frame completion. After frame complete status goes high, write "1" into the Abt control bit (and Abt Extend bit if a 16-bit delay is required). After the Abt control bit is set, write "0" into the RTS control bit. The transmitter will transmit eight or sixteen 1's and the $\overline{\text{RTS}}$ output will then go high (inactive).

7. **Note to users not using the S6800** — (a) Care should be taken when performing a write followed by a read on successive E pulses at a high frequency rate. Time must be allowed for status changes to occur. If this is done, the time that E is low between successive write/read E pulses should be at least 500ns. (b) The ADLC is a completely static part. However, the E frequency should be high enough to move data through the FIFO's and to service the peripheral requirements. Also, the period between successive E pulses should be less than the period of RxC or TxC in order to maintain synchronization between the data bus and the peripherals.

AMI.

VIDEO DISPLAY GENERATOR

August 1978

Features

- ☐ 32 x 16 (512 total) Alphanumeric Two Color Display on Black Background with Internal or External Character Generator ROM.
- ☐ Two Semigraphics Modes with Display Densities Ranging from 64 x 32 to 64 x 48 in 8 and 4 Color Sets Respectively, plus Black.
- ☐ Full Graphics Modes with Display Densities Ranging from 64 x 64 to 256 x 192 in 2 and 4 Colors.
- ☐ Full NTSC Compatible Composite Video with Choice of Interlaced and Non-interlaced Display Versions.
- ☐ Provides Microprocessor Compatible Interface Signals.
- ☐ Generates Display Refresh RAM Addresses.
- ☐ NMOS Device, Single 5V Supply, TTL Compatible Logic Levels.
- ☐ Color Set Select Pin Can Give 8 Color Displays in Full Graphics Mode.

General Description

The S68047 Video Display Generator (VDG) is designed to produce composite video suitable for display on a standard American NTSC compatible black/white television or color televison or monitor.

There are three major types of display which the S68047 can generate. These include an alphanumerics mode of which there are two types, each with normal or inverted video; a semigraphics mode of which there are also two types; and full graphics mode of which there are eight types.

Alphanumeric Modes

The alphanumeric modes, internal and external, enable the S68047 to display a matrix of 32 x 16 (512 total) characters. The internal mode utilizes an on-chip 64 ASCII character ROM to display each character in a 5 x 7 dot matrix font. In the external alphanumeric

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Block Diagram

Pin Configuration
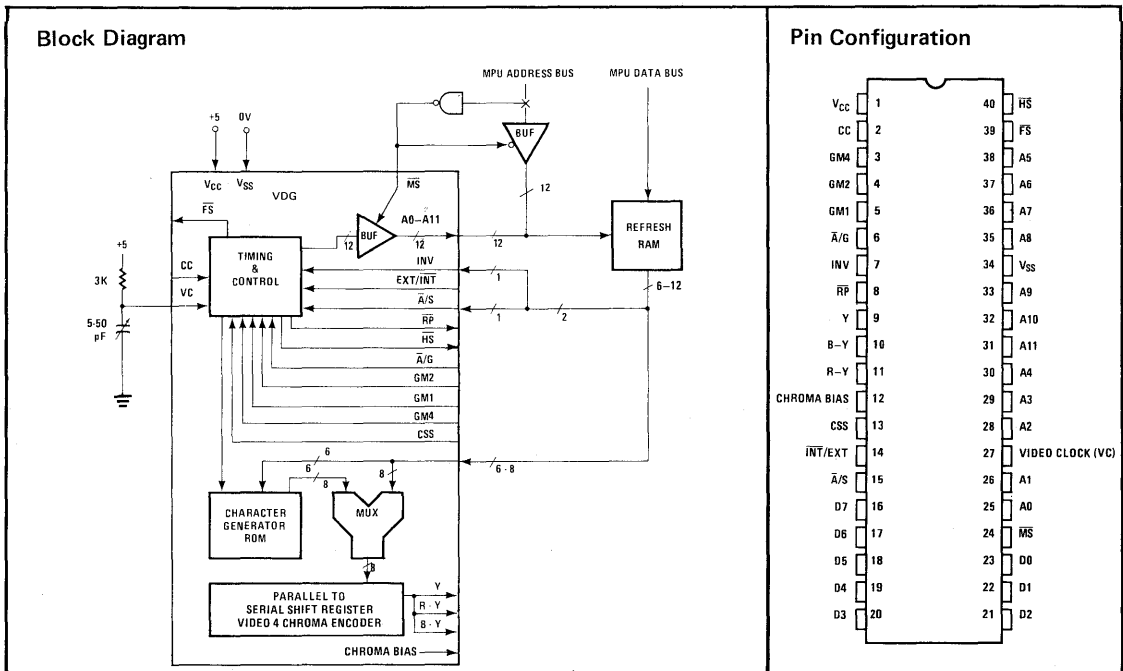
General Description (Continued)

mode, an external memory is required, either ROM or RAM, which is used to display the 32 x 16 character matrix with each character located within an 8 x 12 dot matrix of customized font. Switching between internal and external alphanumerics modes and normal and inverted video can be accomplished on a character by character basis.

Semigraphic Modes

The two semigraphic modes, semigraphic 4 (SG4) and semigraphic 6 (SG6), subdivide each of the 512 (32 x 16) character blocks of 8 x 12 dots each into 2 x 2 and 2 x 3 smaller blocks respectively. In SG4 each block is created from 4 x 6 dots and in SG6 each block consists of 4 x 4 dots. In addition the SG4 and SG6 modes can each be displayed in 8 and 4 colors plus black.

Display switching from alphanumerics to semigraphics modes or vice versa during a raster display is called minor mode switching and can take place on a character basis.

Graphics Modes

The eight full graphics modes are divided into two major groups, 4 color and 2 color. The 4 color graphics provide 4 display densities ranging from 64 x 64 for Graphics 0 through to 128 x 192 elements for Graphics 6. The 2 color graphics also provide 4 display densities ranging from 128 x 64 for Graphics 1 through to 256 x 192 elements for Graphics 7. The latter display has the highest density of the eight graphics modes. The amount of display memory increases proportionately with increasing density of display to a maximum of 6K bytes for Graphics 7. Switching between either the alphanumeric modes or semigraphics modes and any of the full graphics modes is called major mode switching. Major mode switching can only occur at the end of every twelfth raster line scan.

Applications

Anywhere data can be more usefully presented graphically on a CRT and for a minimum cost, the VDG in conjunction with a microprocessor based controller can utilize a standard American NTSC compatible TV or monitor for such a purpose. Applications are extremely broad ranging from educational systems, video games, small low cost business/home computers to process control monitors and medical diagnostic displays.

The different modes of operation permit various cost/ display presentation tradeoffs. The alphanumerics modes allow use of the TV screen as a video teletype at the most limited level of operation. Only 512 bytes, one for each character, need to be stored, each byte being a minimum of six bits wide per the ASCII code. If video inversion switching or alpha to semigraphics switching is required per character then two extra bits are required in the display RAM as shown in Fig. 5. The semigraphics modes each offer an intermediate range of graphics densities with tradeoffs in density versus color. Typical semigraphics display capabilities are bar graphs, charts, mini displays, etc. which with minor mode switching to alphanumerics modes allow annotation or captioning of the resultant display. The various graphics modes provide greater density displays with greater freedom of display presentations. The tradeoffs in increasing density are with increasing display memory size and color versus density. A minimum Graphics 0 provides a display density of 64 x 64 (4096) elements, each element being composed of a matrix of 12 (4 x 3) dots with a selection of four colors per element. Since each of the even numbered 4 color graphics modes map two bits of the data word to one picture element, each data word of memory provides four picture elements. Thus Graphics 0 requires 4096/4 = 1024 bytes of display RAM, Graphics 2 requires 8192/4 = 2048 and so on. Graphics 1, like all the odd numbered 2 color graphics modes, maps one bit of data word to one picture element. Each data word therefore maps eight elements. Graphics 1 density of 128 x 8 (8192) elements therefore requires 8192/8 = 1024 bytes of display RAM and Graphics 7, the densest display, requires 49, 152/8 = 6144 bytes of RAM. At the higher density graphics displays, the rate of change of elements approaches the maximum dot frequency of 6MHz. This video rate taxes the capabilities of most commercially available television sets and thus the quality of the display system (television or monitor) should be commensurate with the highest video rate to be used.

Electrical Specifications
Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

DC (Static) Characteristics ($V_{CC} = 5.0V \pm 5\%$; $T_A = 25°C$, unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input Voltage High	2.0		V_{CC}	V	
V_{IH}	Input Voltage High (Color Clock only)	4.0		V_{CC}	V	
V_{IL}	Input Voltage Low	−0.3		+0.6	V	
I_{IN}	Input Leakage Current (all inputs)		1.0	2.5	μA	$V_{IN} = 0 - 5.25V$; $V_{CC} = 0V$
$I_{L(TS)}$	Tri-State Output Leakage Current (A0 − A11)			10	μA	$V_{CC} = 5.25V$; $\overline{MS} = 0V$; $V_{IN} = 0.4 - 2.4V$
I_{LO}	Output Leakage Current ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$)			10	μA	$V_{IN} = 2.4V$; $V_{CC} = 0V$
V_{OH}	Output Voltage High (A0 − A11, $\overline{HS}$, $\overline{FS}$, $\overline{RP}$)	2.4			V	$I_{OH} = -100\mu A$ ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$); $0\mu A$ ($A_0 - A_{11}$); $CL = 30pF$
V_{OL}	Output Voltage Low (A0 − A11, $\overline{HS}$, $\overline{FS}$, $\overline{RP}$)			0.4	V	$I_{OL} = 1.6mA$ ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$); $0mA$ ($A_0 - A_{11}$); $CL = 30pF$
I_{CC}	V_{CC} Supply Current		45		mA	$V_{CC} = 5V$; $T_A = 25°C$
C_{IN}	Input Capacitance			10	pF	$V_{IN} = 0$, $T_A = 25°C$; $f = 1.0MHz$
C_{OUT}	Output Capacitance			12	pF	$V_{IN} = 0$, $T_A = 25°C$; $f = 1.0MHz$

AC Electrical Characteristics ($V_{CC} = 5.0V \pm 5\%$; $T_A = 0 - 70°C$ except where noted).

Alpha Internal Mode (Figure 1)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
f_{VC}	Video Clock Frequency	5.6	6.0	6.4	MHz	
t_{ch}	Character Time	1.43	1.33	1.25	μs	
t_{ACC}	Access-Time of External Refresh RAM			0.7	μs	
t_{dot}	Dot Time	178	166	156	ns	

Alpha External Mode (Figure 1)
NOTE: All parameters are the same as in Alpha Internal Mode except t_{ACC}

t_{ACC}	Access-time of Refresh RAM + Access-time of External ROM			0.7	μs	

Semigraphics Mode (Figure 1)

t_{pic}	Picture Element Duration	712	664	624	ns	

NOTE: All other parameters are the same as in Alpha Internal Mode.

Color Sub-carrier Input

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{CC}	Frequency		3.579545 ±10 Hz		MHz	
t_r	Rise Time			10	ns	
t_f	Fall Time			10	ns	
PW_{CC}	Pulse Width		140		ns	
V_{IL}	Zero Level			0.6	V	
V_{IH}	One Level	4.0			V	
DR	Duty Ratio	40%	50%	60%		

Figure 1. Refresh RAM Interface Timing
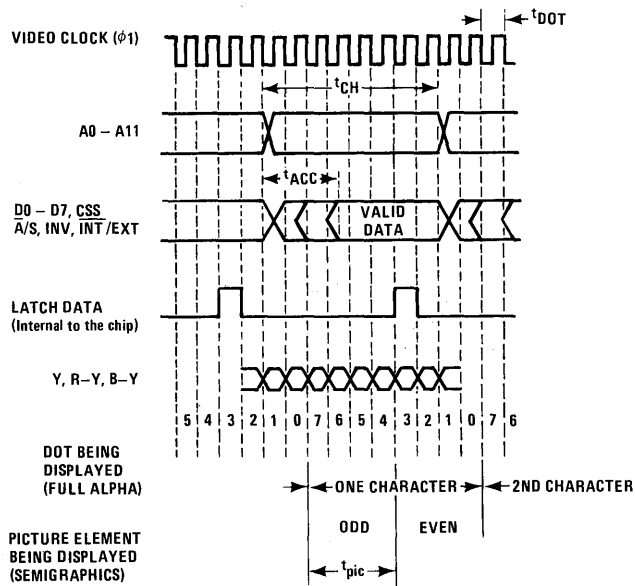
Composite Video Timing (Figure 2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{SYNC}	Sync duration		4.888889		μs	
t_{fp}	Front Porch duration		1.536508		μs	
t_{BLANK}	Horizontal Blank Duration			11.44	μs	
t_{rs}, t_{fs}	Rise time and Fall time of Horizontal Sync			250	ns	
t_{rv}, t_{fv}	Rise time and Fall time of Horizontal Blank			340	ns	

Figure 2. Composite Video Timing on Y Pin
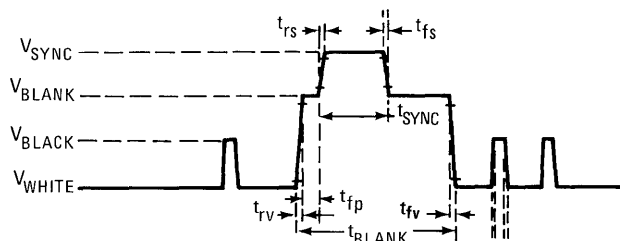
Chroma R and Chroma B Output Timing; C_L = 10pF; 1K Load (Figure 3.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{rB}, t_{fB} t_{rR}, t_{fR}	Color Signals rise and fall time		50		ns	Load = R-Y, B-Y input of LM1889
t_{scB}	Color Burst to Sync lag		410		ns	
t_{BURST}	Color Burst Duration		2.45		μs	
t_{fcB}, t_{rcB}	Color Burst rise and fall times		175		ns	
t_{cL1}, t_{cL2}	Video to color signals lag		75		ns	

Voltage Levels

Video (Y) and Chroma (R—Y, B—Y) Output Levels (Figure 3.) C_L = 10pF; Video Clock = 5.6MHz; T_A = 25°C; V_{CC} = 5V ± 5%

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{SYNC}	Sync Voltage	0	0.1	0.5	V	
V_{BLANK}	Blanking Level		1.5		V	
V_{BLACK}	Black Level		1.7		V	
V_{WHITE}	White level	2.4	4.0	V_{CC}	V	
V_{B1}, V_{R1}		2.4	4.0	V_{CC}	V	
V_{B0}, V_{R0}			2.0		V	
V_{B3}, V_{R3}		0	0.1	0.5	V	
V_{BURST}			0.4		V	
$V_{CHROMA\ BIAS}$			2.0		V	

Figure 3. Chroma Timing
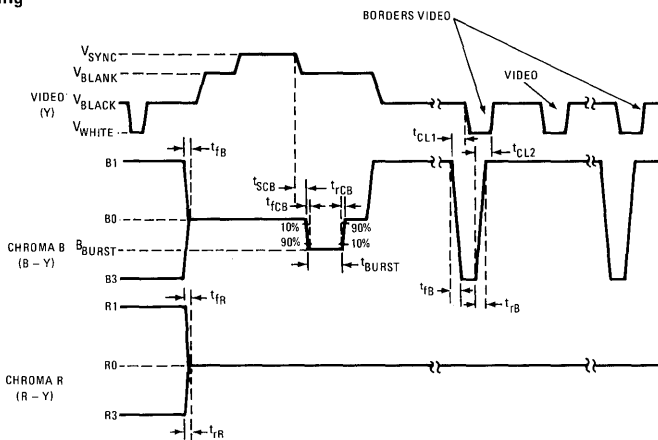
Video Display Format Timing (Figure 4.)

Symbol	Parameter	Typ.	Units	Conditions
H	Horizontal Scan Time	63.55557	μs	
V	Field Time	16.683337	ms	
F	Frame Time	33.366674	ms	
I/V	Field Rate	59.94004	$\sec^{-1}$	
t_{ACTIVE}	Active Display Duration	41	μs	
t_{VIDEO}	Active Display + Border Duration	52.8	μs	
t_{RP}	Row Preset Period (12 Horizontal Scans)	762.66684	μs	

Figure 4. Video Display Format
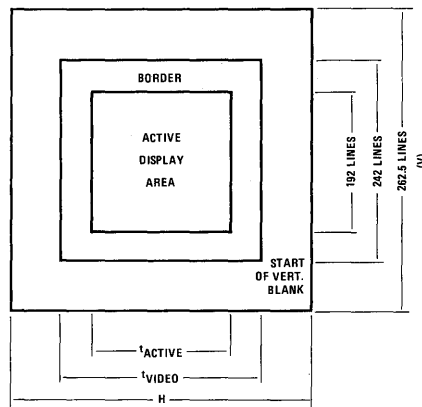
Pin Description (Figure 2.)

V_{CC}	+5V
V_{SS}	0V
CC	(Color Burst Clock 3.579545 MHz)
VC	(Video Clock Oscillator $\cong$ 6MHz)
A0 — A11	(Address Lines to Display Memory; high-impedance during $\overline{MS}$ low)
D0 — D5	(Data from Display Memory RAM or ROM; D4 — D6 — Color Data in Semigraphics)
D6, D7	(Data from Display Memory in GRAPHIC Mode; Data also in ALPHANUMERIC Mode; Color Data in ALPHA SEMIGRAPHIC — 6)
R — Y, B — Y, Y	(Color and Composite Video)
CHB	(Chroma Bias; References R — Y and B — Y Levels)
$\overline{RP}$	(Row Preset in any ALPHA Mode; goes low in all modes every 12 lines)
$\overline{HS}$	(Horizontal Sync)
INV	(Inverts Video in all FULL ALPHA Modes; no effect in Semigraphics or Graphics Mode)
EXT/$\overline{INT}$	(Switches to External ROM in ALPHA Mode; between SEMIG — 4 and SEMIG — 6 in Semigraphics; no effect in all Graphics Modes)
$\overline{A}$/S	(Alpha/Semigraphics: Selects between FULL ALPHA and SEMIGRAPHICS in ALPHA Modes; no effect in all Graphics Modes)
$\overline{MS}$	(Memory Select; forces VDG Address Buffers to high-impedance state; also used as a strobe in TEST and RESET functions). The TV screen is forced black when $\overline{MS}$ = low
$\overline{A}$/G	(Switches between ALPHA and GRAPHIC Modes)
$\overline{FS}$	(Field Synchronization; LOW during vertical blanking time)
CSS	(Color Set Select: Selects between two ALPHA Display Colors; between two Color Sets in SEMIGRAPHICS — 6 and FULL GRAPHICS: selects Border Color in 8 Graphic Modes)
GM1, GM2 GM4	(Graphics Mode Select; select one of eight Graphic Modes; no affect in Alpha and Semigraphic Modes; GM1, GM2 select TEST and RESET mode when $\overline{A}$/G = 0 and $\overline{MS}$ pin is strobed low)

Internal Description

Internally the VDG is the combination of four integrated subsystems (timing and control, MUX, address buffers and shift registers to form the VDG function. A block diagram of the VDG is shown on Page 1. Each subsystem is described below.

Timing and Control

The timing and control subsystem of the VDG uses the 3.58MHz color frequency to generate timing information. It accepts the color clock (generated off-chip) (CC) input and generates timing for the horizontal sync, horizontal blank, field sync, vertical blank and row preset signal ($\overline{RP}$) for external character generator ROM. The video clock is generated on-chip by external RC and generates addresses A0 — A11 to address the external refresh RAM.

The color-set-select (CSS) input to the Timing and Control subsystem of the VDG is used to determine the color-set of the display.

The EXT/$\overline{INT}$ input has two functions. In the full alphanumeric mode, it is used to select either internal ROM or external ROM. It is also used to select between semigraphic 4 and semigraphic 6 mode in semigraphic modes ($\overline{A}$/S = 1).

The INV input is utilized by the timing and control subsystem to invert the display while in full alpha mode.

Internal Description (Continued)

$\overline{A}/G$, $\overline{A}/S$, GM1, GM2, GM4 inputs to the timing and control subsystem determine which of the fourteen VDG modes is to be used (Table 1).

MUX

The MUX provides the function of selecting the data source to be displayed. The source can be either internal ROM or external ROM or RAM. For the internal alphanumeric mode, the data source is the internal ROM. For all other modes (semigraphic and graphics) the data source is external ROM/RAM.

Address Buffers

The address buffers provide the buffering required for external drive (ROM/RAM). The buffers are tristated when the $\overline{MS}$ pin goes low and tri-states the buffers so that VDG does not interfere with the MPU operation. The $\overline{FS}$ pin (output) from the VDG signals to the MPU that the TV is in the vertical retrace mode and the MPU can directly change the data in the display memory during that time with no interruption to displayed data.

Shift Registers

The two shift registers serialize bytes coming from internal/external ROM/RAM for conversion to data

on the TV screen. The shift registers output also goes to the chroma encoder circuitry to determine the color of each individual dot. Each shift register has 4-bits.

VDG

The VDG has fourteen modes, grouped in three sets. They are:

4 Alphanumerics Modes   2 Semigraphics Modes

☐ Normal internal alpha   ☐ Semigraphics 4
☐ Inverted internal alpha   ☐ Semigraphics 6
☐ Normal external alpha
☐ Inverted external alpha

8 Full-graphics Modes

☐ 4 Graphics four-color modes
☐ 4 Graphics two-color modes

The six alphanumeric modes can be switched among themselves on a character-by-character basis. Switching within the six alphanumeric modes is referred to as minor-mode switching. All other mode switching is referred to as major-mode switching.

The display can be major-mode switched on after any multiple of twelve rows have been completed. This is signalled to the MPU by $\overline{RP}$ output going low. Switching among the full-graphics modes is permitted at the end of every twelfth row just as in major-mode switching.

Table 1 tabulates the modes of the VDG. The data structures for each mode are listed in Table 7. Table 2 and Table 3 show the Alpha Select Mode and Graphic Select Mode configurations respectively. Table 4 gives the Two-color Graphics and Full-alpha Color Specification. Table 5 shows the semigraphics and Four-color Graphics Color Specification.

Table 1. VDG Modes

	Mode	Description	Memory
I.	ALPHA INTERNAL	32 x 16 BOXES: 5 x 7 CHARACTER	512 x 7 — 8
II.	ALPHA INTERNAL INVERTED	IN 8 x 12 BOX	
III.	ALPHA EXTERNAL	32 x 16 BOXES: 5 x 7 OR 7 x 9 CHARACTERS	512 x 7 — 8
IV.	ALPHA EXTERNAL INVERTED	IN 8 x 12 BOX OR FULL 8 x 12 LIMITED GRAPHICS	
V.	ALPHA SEMIGRAPHICS 4	32 x 16 BOXES: 2 x 2 ELEMENTS PER BOX; EIGHT COLORS PLUS BLACK	512 x 4 — 7
VI.	ALPHA SEMIGRAPHICS 6	32 x 16 BOXES 2 x 3 ELEMENTS PER BOX; FOUR COLORS PLUS BLACK	512 x 6 — 8
VII.	GRAPHICS 0	64 x 64 ELEMENTS: FOUR COLORS PER ELEMENT	1K x 8
VIII.	GRAPHICS 1	128 x 64 ELEMENTS: TWO COLORS PER ELEMENT	1K x 8
IX.	GRAPHICS 2	128 x 64 ELEMENTS: FOUR COLORS PER ELEMENT	2K x 8
X.	GRAPHICS 3	128 x 96 ELEMENTS: TWO COLORS PER ELEMENT	1.5K x 8
XI.	GRAPHICS 4	128 x 96 ELEMENTS: FOUR COLORS PER ELEMENT	3K x 8
XII.	GRAPHICS 5	256 x 96 ELEMENTS: TWO COLORS PER ELEMENT	3K x 8
XIII.	GRAPHICS 6	128 x 192 ELEMENTS: FOUR COLORS PER ELEMENT	6K x 8
XIV.	GRAPHICS 7	256 x 192 ELEMENTS: TWO COLORS PER ELEMENT	6K x 8

Table 7. Detailed Description of VDG Model

VDG PINS								COLOR			TV SCREEN		VDG DATA BUS	COMMENTS
A/G	A/S	INT/EXT	GM4	GM2	GM1	CSS	INV	CHARACTER COLOR	BACK-GROUND	BORDER	DISPLAY MODE	DETAIL		
0	0	0	X	0	0	0 / 1	0 / 1	Green / Black / Blue / Black	Black / Green / Black / Blue	Black / Black	32 Characters in columns; 16 Characters in rows	8 DOTS / 12 DOTS / 7 / 5	NOT USED — ASCII INPUT	ALPHANUMERIC INTERNAL mode uses internal character generator with on-chip 64 ASCII character ROM to display each character in 5x7 dot matrix font.
0	0	1	X	0	0	0 / 1	0 / 1	Green / Black / Green / Black	Black / Green / Black / Green	Black / Black	32 Characters in columns; 16 Characters in rows		ONE ROW OF CUSTOM CHARACTERS	ALPHANUMERIC EXTERNAL mode uses external ROM or RAM to display 512 characters in custom fonts each in 8x12 dot matrix.
0	1	0	X	0	0	X	X	$L_x\ C_2\ C_1\ C_0$ Color: 0 X X X Black; 1 0 0 0 Yellow; 1 0 0 1 Cyan; 1 0 1 0 Red; 1 0 1 1 Blue; 1 1 0 0 Cyan/Blue; 1 1 1 0 Magenta; 1 1 1 1 Orange		Black	64 Display elements in columns; 32 Display elements in rows	L1 L0 / L3 L2	NOT USED — COLOR — LUMINANCE (C2 C1 C0 L3 L2 L1 L0)	SEMIGRAPHICS 4 mode subdivides each of the 512 (32x16) character blocks of 8x12 dots into four equal parts. The dominance of each block is determined by the corresponding bit (L0-L3) on the VDG data bus. Color of each block is determined by 3 bits (C0-C3).
0	1	1	X	0	0	0 / X	X	$L_x\ C_1\ C_0$ Color: 0 0 0 Black; 1 0 0 Green; 1 0 1 Yellow; 1 1 1 Red; 1 0 0 Blue; 1 0 1 Cyan/Blue; 1 1 0 Magenta; 1 1 1 Orange		Black	64 Display elements in columns; 48 Display elements in rows	L1 L0 / L3 L2 / L5 L4	COLOR — LUMINENCE (C1 C0 L5 L4 L3 L2 L1 L0)	SEMIGRAPHICS 6 mode subdivides each of the 512 (32x16) character blocks of 8x12 dots into six equal parts. The luminance of each part is determined by the corresponding bits (L0-L5) on the VDG bus. Color of each block is determined by 2 bits (C0, C1).
1	X	X	0	0	0	0 / 1	X	$C_1\ C_0$: 0 0 Green; 0 1 Yellow; 1 0 Cyan; 1 1 Red; 0 0 Blue; 0 1 Cyan/Blue; 1 0 Magenta; 1 1 Orange		Green / Cyan/Blue	64 Display elements in columns; 64 Display elements in rows	E3 E2 E1 E0 WHERE EX = C1C0	C1 C0 C1 C0 C1 C0 C1 C0	GRAPHICS 0 mode uses a maximum of 1024 bytes of display RAM in which one pair of bits (C0, C1) specifies on picture element. (Ex.).
1	X	X	0	0	1	0 / 1	X	L_x : 0 Black, Color; 1 Green; 0 Black; 1 Cyan/Blue		Green / Cyan/Blue	128 Display elements in columns; 64 Display elements in rows	L7 L6 L5 L4 L3 L2 L1 L0	L7 L6 L5 L4 L3 L2 L1 L0	GRAPHICS 1 mode uses a maximum of 1024 bytes of display RAM in which one bit (Lx) specifies one picture element.
1	X	X	0	1	0	0 / 1	X	Same color as Graphics 0		Green / Cyan/Blue	128 Display elements in columns; 64 Display elements in rows	E3 E2 E1 E0	C1 C0 C1 C0 C1 C0 C1 C0	GRAPHICS 2 mode uses a maximum of 2048 bytes of display RAM in which one pair of bits (C0, C1) specifies one picture element (Ex.).
1	X	X	0	1	1	0 / 1	X	Same color as Graphics 1		Green / Cyan/Blue	128 Display elements in columns; 96 Display elements in rows	L7 L6 L5 L4 L3 L2 L1 L0	L7 L6 L5 L4 L3 L2 L1 L0	GRAPHICS 3 mode uses a maximum of 1536 bytes of display RAM in which one bit (Lx) specifies one picture element.
1	X	X	0	1	0	0 / 1	X	Same color as Graphics 0		Green / Cyan/Blue	128 Display elements in columns; 96 Display elements in rows	E3 E2 E1 E0	C1 C0 C1 C0 C1 C0 C1 C0	GRAPHICS 4 mode uses a maximum of 3072 bytes of display RAM in which one pair of bits (C0, C1) specifies one picture element (Ex.)
1	X	X	1	0	1	0 / 1	X	Same color as Graphics 1		Green / Cyan/Blue	256 Display elements in columns; 96 Display elements in rows	L7 L6 L5 L4 L3 L2 L1 L0	L7 L6 L5 L4 L3 L2 L1 L0	GRAPHICS 5 mode uses a maximum of 3072 bytes of display RAM in which one bit (Lx) specifies one picture element.
1	X	X	1	1	0	0 / 1	X	Same color as Graphics 0		Green / Cyan/Blue	128 Display elements in columns; 192 Display elements in rows	E3 E2 E1 E0	C1 C0 C1 C0 C1 C0 C1 C0	GRAPHICS 6 mode uses a maximum of 6144 bytes of display RAM in which one pair of bits (C0, C1) specifies one picture element (Ex.).
1	X	X	1	1	1	0 / 1	X	Same color as Graphics 1		Green / Cyan/Blue	256 Display elements in columns; 192 Display elements in rows	L7 L6 L5 L4 L3 L2 L1 L0	L7 L6 L5 L4 L3 L2 L1 L0	GRAPHICS 7 mode uses a maximum of 6144 bytes of display RAM in which one bit (Lx) specifies one picture element.

Table 2. Alpha Mode Select

GM2	GM1	$\overline{A}/G$	$\overline{A}/S$	$\overline{INT}/EXT$	INV	$\overline{MS}$	MODE
X	0	0	0	0	0		INTERNAL ALPHANUMERICS
X	0	0	0	0	1		INTERNAL INV. ALPHA
X	0	0	0	1	0		EXTERNAL ALPHA
X	0	0	0	1	1		EXTERNAL INV. ALPHA
X	0	0	1	0	X		SEMIGRAPHICS – 4
X	0	0	1	1	X		SEMIGRAPHICS – 6
0	1	0	X	X	X	STROBED LOW	TEST ROM
1	1	0	X	X	X	STROBED LOW	RESET

NOTES:
1) GM4 pin has no effect when $\overline{A}/G = 0$.
2) Invert pin has no effect except in Internal Alpha or External Alpha.
3) Under normal operation, care should be taken not to take GM1 pin HIGH, when $\overline{A}/G$ pin is LOW. If this happens, any of the following conditions will occur depending on the status of $\overline{MS}$ and GM2 pin:
   a) The VDG might go to TEST mode.
   b) The VDG might be reset.
   The VDG will not return to normal operation unless $\overline{A}/G$ and GM1 pins are returned to LOW level and $\overline{MS}$ pin is strobed.
4) X = Don't care.

Table 3. Graphic Mode Select

	$\overline{A}/G$	GM4	GM2	GM1	MODE
GRAPHICS 0	1	0	0	0	64 x 64 4 – COLOR
GRAPHICS 1	1	0	0	1	128 x 64 2 – COLOR
GRAPHICS 2	1	0	1	0	128 x 64 4 – COLOR
GRAPHICS 3	1	0	1	1	128 x 96 2 – COLOR
GRAPHICS 4	1	1	0	0	128 x 96 4 – COLOR
GRAPHICS 5	1	1	0	1	256 x 96 2 – COLOR
GRAPHICS 6	1	1	1	0	128 x 192 4 – COLOR
GRAPHICS 7	1	1	1	1	256 x 192 2 – COLOR

NOTE: $\overline{A}/S$, $\overline{INT}/EXT$, INV pins have no effect when $\overline{A}/G = 1$.

Table 4. Two-Color Graphics and Full-Alpha Color Specification

CSS PIN	COLOR OF 'ON' DOTS
0	GREEN
1	CYAN-BLUE

Table 5. Semigraphics and Four-Color Graphics Color Specification

4-COLOR GRAPHICS	SEMI-GRAPHICS – 6	SEMI-GRAPHICS – 4
EVEN BIT	D6	D4
ODD BIT	D7	D5
CSS	CSS	D6

COLOR SET 1	0	0	0	GREEN
	0	0	1	YELLOW
	0	1	0	CYAN
	0	1	1	RED
COLOR SET 2	1	0	0	BLUE
	1	0	1	CYAN/BLUE
	1	1	0	MAGENTA
	1	1	1	ORANGE

NOTE: In Semigraphics – 6, if any bit D0 – D5 is '0', then picture element corresponding to that bit would be black. In Semigraphics – 4, if any bit D0 – D3 is zero, then the picture element corresponding to that dot will be black.

Table 6. Two-Color Graphics and Four-Color Graphics Border Color Specification

CSS PIN	BORDER COLOR
0	GREEN
1	CYAN-BLUE

Typical System: A typical S6800 microprocessor based S68047 system is shown on Figure 5. This system has the capability of displaying internally and externally generated characters, semigraphics 4 and 6 modes with mode switching control from the microcomputer input/output ports. A full graphics system configuration would be similar in complexity with possibly additional display RAM for the denser graphics modes. The National Semiconductor LM1889 RF modulator shown, has an on chip 3.58 MHz oscillator which can provide the microcomputer system clock as well as the color burst reference for the S68047. Other RF modulators are available through various commercial channels. Only 512 bytes are needed to display the 512 character blocks on a TV screen. However, because of current static RAM configurations (ie. 1Kx1 & 1Kx4) the extra 512 bytes available in the 1Kx9 RAM shown can be used as scratchpad by the host microcomputer system.

Ordering Information

Ordering No.	No. Pins	Package	Temp. Range	Description
S68047	40	Ceramic	0-70°C	VDG non-interlaced
S68047P	40	Plastic	0-70°C	VDG non-interlaced
S68047Y	40	Ceramic	0-70°C	VDG interlaced
S68047YP	40	Plastic	0-70°C	VDG interlaced

Figure 5. Typical System (Alphanumeric Internal/External & Semigraphics 4 and 6 Modes.)
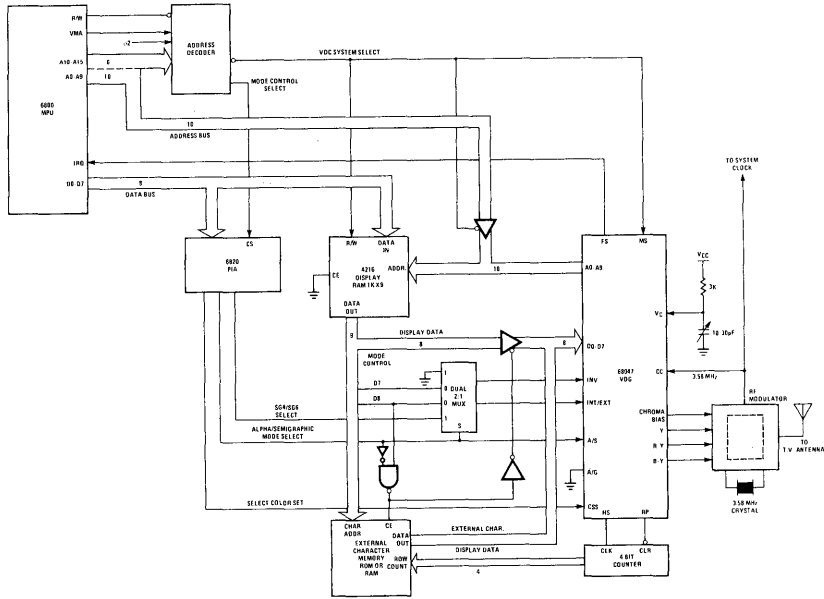
Physical Dimensions

40-Pin Plastic

40-Pin SLAM

AMI ®
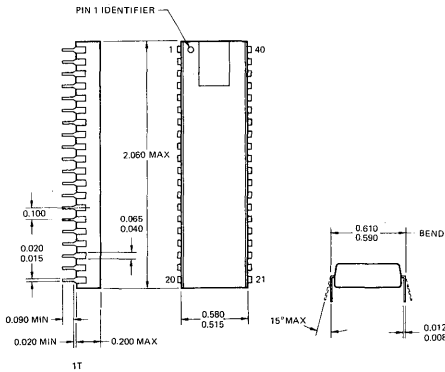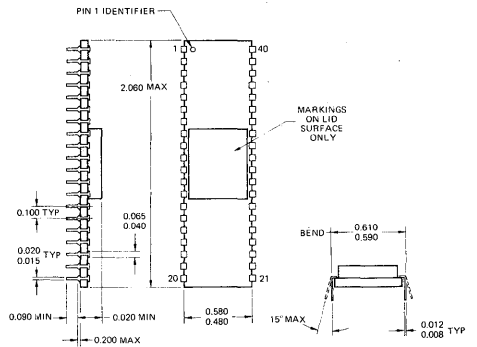
GENERAL PURPOSE INTERFACE ADAPTER

Features

☐ Single or Dual Primary Address Recognition
☐ Secondary Address Capability
☐ Complete Source and Acceptor Handshakes
☐ Programmable Interrupts
☐ RFD Holdoff to Prevent Data Overrun
☐ Operates with DMA Controller
☐ Serial and Parallel Polling Capability
☐ Talk-Only or Listen-Only Capability
☐ Selectable Automatic Features to Minimize Software
☐ Synchronization Trigger Output
☐ S6800 Bus Compatible

General Description

The S68488 GPIA provides the means to interface between the IEEE488 standard instrument bus and the S6800. The 488 instrument bus provides a means for controlling and moving data from complex systems of multiple instruments.

The S68488 will automatically handle all handshake protocol needed on the instrument bus.

S6800

Block Diagram

NOTE 1:

TYP 16 PLACES
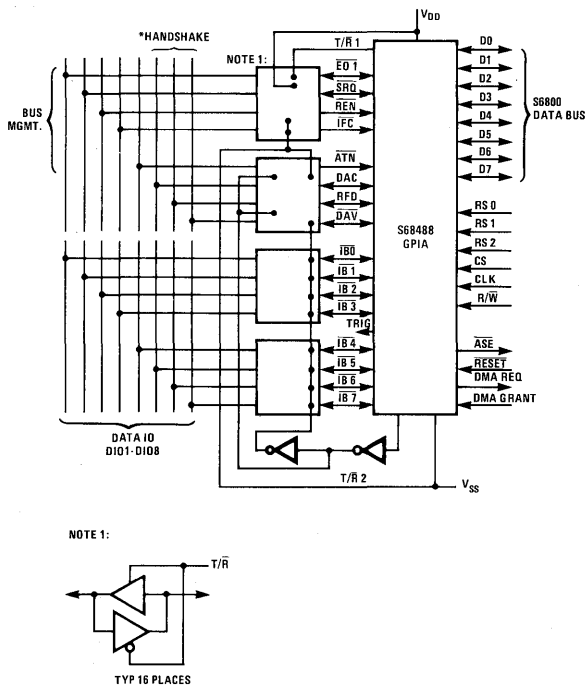
*The 3-wire handshake described is the subject of patents owned by Hewlett-Packard Co.

Pin Configuration
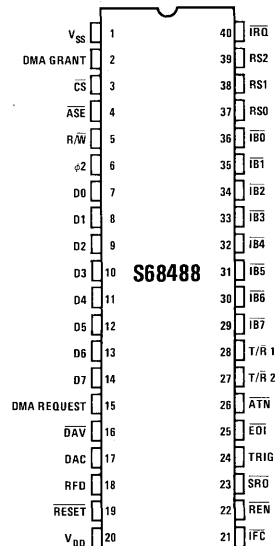
Functional Description

The IEEE 488 instrument bus standard is a bit-parallel, byte-serial bus structure designed for communiation to and from intelligent instruments. Using this standard, many instruments may be interconnected and remotely and automatically controlled or programmed. Data may be taken from, sent to, or transferred between instruments. A bus controller dictates the role of each device by making the attention line true and sending talk or listen addresses on the instrument bus data lines; those devices which have matching addresses are activated. Device addresses are set into each GPIA from switches or jumpers on a PC board by a microprocessor as a part of the initialization sequence.

When the controller makes the attention line true, instrument bus commands may also be sent to single or multiple GPIAs.

Information is transmitted on the instrument bus data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as the devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices of different speeds to receive the same data concurrently.

The GPIA is designed to work with standard 488 bus driver Ics (S3448As) to meet the complete electrical specifications of the IEEE488 bus. Additionally, a powered-off instrument may be powered-on without disturbing the 488 bus. With some additional logic, the GPIA could be used with other microprocessors.

The S68488 GPIA has been designed to interface between the S6800 microprocessor and the complex protocol of the IEEE488 instrument bus. Many instrument bus protocol functions are handled automatically by the GPIA and require no additional MPU action. Other functions require minimum MPU response due to a large number of internal registers conveying information on the state of the GPIA and the instrument bus.
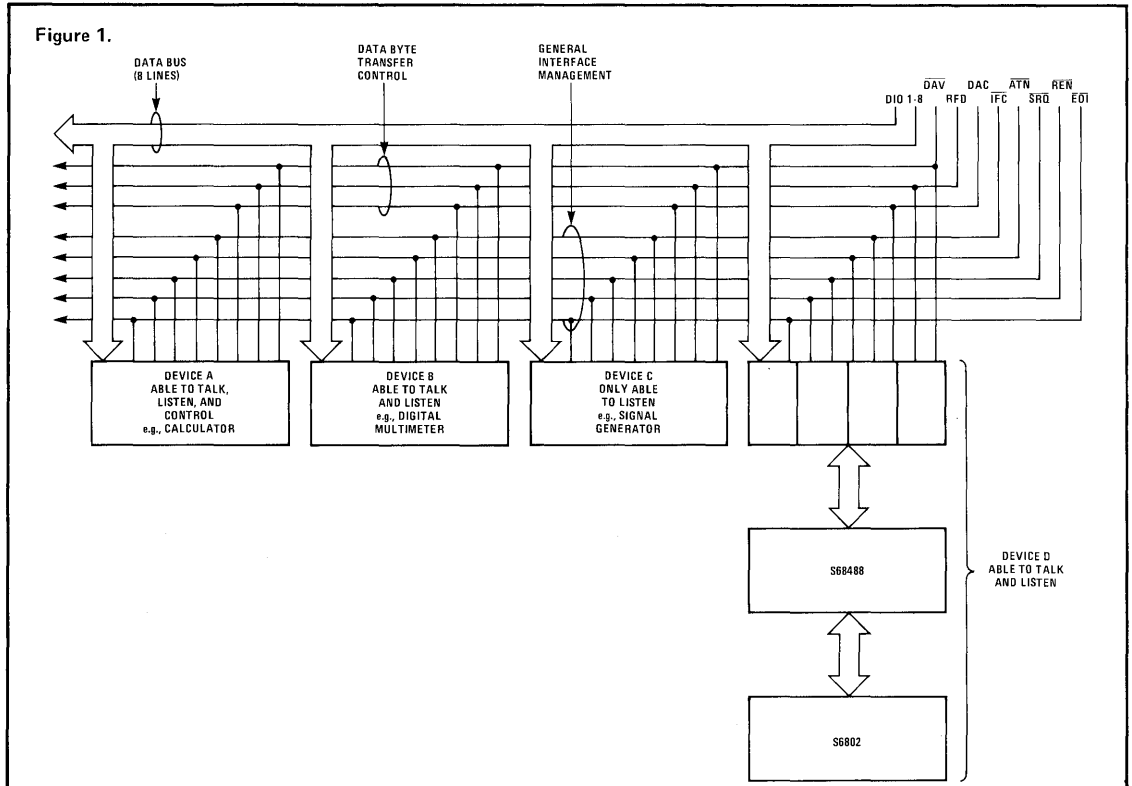
Figure 1.

Maximum Ratings

Supply Voltage .... -0.3Vdc to $+7.0$Vdc

Input Voltage .... -0.3Vdc to $+7.0$Vdc

Operating Temperature Range .... $0°$C to $+70°$C

Storage Temperature Range .... $-55°$C to $+150°$C

Thermal Resistance .... $+82.5°$C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V $\pm5\%$, V_{SS} = 0, T_A = $0°$C to $+70°$C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	V_{SS} + 2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} - 0.3		V_{SS} + 0.8		
I_{IN}	Input Leakage Current		1.0	2.5	μAdc	V_{IN} = 0 to 5.25V
I_{TSI}	Three-State (Off State) Input Current D0-D7		2.0	10	μAdc	V_{IN} = 0.4 to 2.4V
V_{OH}	Output High Voltage D0-D7	V_{SS} + 2.4			Vdc	I_{load} = -205μA
V_{OL}	Output Low Voltage D0-D7 $\overline{IRQ}$			V_{SS} + 0.4 V_{SS} + 0.4	Vdc	I_{load} = 1.6mA I_{load} = 3.2mA
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation		600		mW	
C_{IN}	Input Capacitance D0-D7 All Others			12.5 7.5	pF	V_{IN} = 0, T_A = $25°$C, f = 1.0MHz

Figure 2. Source and Acceptor Handshake
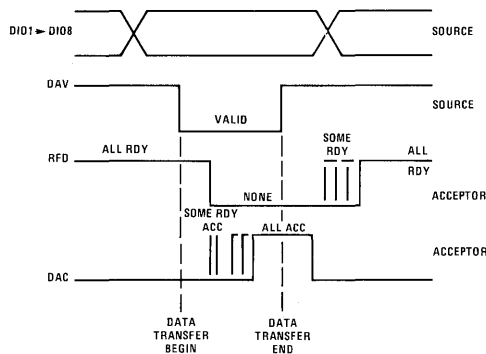
Bus Timing Characteristics
Read (See Figure 3)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{cycE}	Enable Cycle Time	1.0			μs	
PW_{EH}	Enable Pulse Width, High	0.45			μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, Address and $R/\overline{W}$ valid to enable positive transition	160			ns	See Figure 3
t_{DDR}	Data Delay Time			320	ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input			25	ns	

Write (See Figure 4)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{cycE}	Enable Cycle Time	1.0			μs	
PW_{EH}	Enable Pulse Width, High	0.45			μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, Address and $R/\overline{W}$ valid to enable positive transition	160			ns	See Figure 4
t_{DSW}	Data Setup Time	195			ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input			25	ns	

Output (See Figure 5)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{HD}	Output Delay Time			400	ns	$\overline{DAV}$, DAC, RFD, $\overline{EOI}$, $\overline{ATN}$ valid
$t_{T/\overline{R}1, 2D}$				400	ns	T/$\overline{R}$1, T/$\overline{R}$2 valid

Figure 3. Bus Read Timing Characteristics (Read Information from GPIA)

Figure 4. Bus Write Timing Characteristics (Write Information into GPIA)
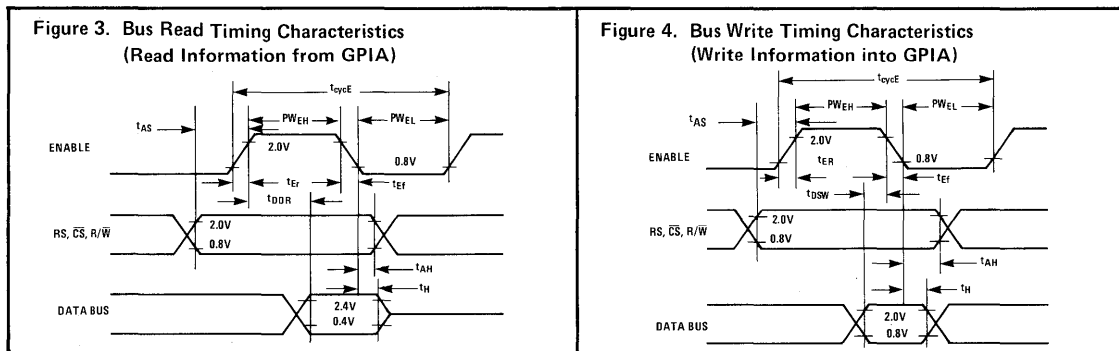
Figure 5. Output Bus Timing
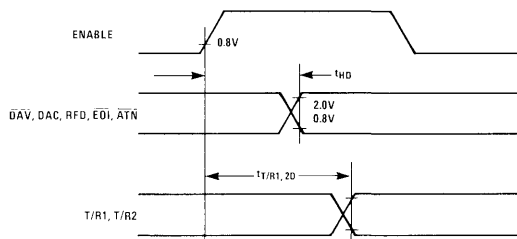
A.C. Time Values

Symbol*	Parameter		Min.	Typ.	Max.	Unit	Conditions
T_1	Settling Time for Multiple Message	SH		$\geqslant 2$		μs**	
t_2	Response to $\overline{ATN}$	SH, AH, T, L		$\leqslant 200$		ns	
T_3	Interface Message Accept Time †	AH		>0		ϕ	
t_4	Response to $\overline{IFC}$ or $\overline{REN}$ False	T, TE, L, LE		<100		μs	
t_5	Response to $\overline{ATN} \bullet \overline{EOI}$	PP		$\leqslant 200$		ns	

* Time values specified by a lower case t indicate the maximum time allowed to make a state transition. Time values specified by an upper case T indicate the minimum time that a function must remain in a state before exiting.

** If three-state drivers are used on the $\overline{DIO} - \overline{DAV}$ and $\overline{EOI}$ lines, T_1 may be:
 (1) $\geqslant 1100$ns
 (2) Or $\geqslant 700$ns if it is known that within the controller $\overline{ATN}$ is driven by a three-state driver.
 (3) Or $\geqslant 500$ns for all subsequent bytes following the first sent after each false transition of $\overline{ATN}$ [the first byte must be sent in accordance with (1) or (2)].

† Time required for interface functions to accept, not necessarily respond to interface messages.

ϕ Implementation dependent.

MPU bus clock rate — The current 6800 bus clock is $\leqslant$ 1MHz but part should operate at 1.5MHz (design goal), with appropriate settling times (T1).

GPIA/MPU Interface Signals

The S68488 interfaces to the S6800 MPU with an eight-bit bidirectional data bus, a chip select, Read/$\overline{Write}$ line, $\overline{reset}$ line, three register select lines, an interrupt request line, two DMA control lines, and an address switch enable line.

Bidirectional Data (D0-D7) — The bidirectional data lines allow the transfer of data between the MPU and the GPIA. The data bus output drives are three-state devices that remain in the high impedance (off) state except when the MPU performs a GPIA read operation.

Chip Select ($\overline{CS}$) — This input signal is used to select the GPIA. $\overline{CS}$ must be low for selection of the device. Chip select decoding is normally accomplished with logic external to the chip.

Read/$\overline{Write}$ Line (R/$\overline{W}$) — This signal is generated by the MPU to control register access and direction of data transfer on the data bus. A low state on the GPIA Read/$\overline{Write}$ allows for the selection of one of seven write-only registers when used in conjunction with the register select lines RS0, RS1, RS2. A high

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state on the GPIA Read/$\overline{\text{Write}}$ allows for the selection of one of eight read-only registers when used in conjunction with register select lines RS0, RS1, RS2.

Register Select (RS0, RS1, RS2) — The three register select lines are used to select the various registers inside the GPIA. These three lines are used in conjunction with the Read/Write line to select a particular register that is to be written or read. Table 1 shows the register select coding.

Table 1. Register Access

RS2	RS1	RS0	R/W	REGISTER TITLE	REGISTER SYMBOL
0	0	0	1	INTERRUPT STATUS	R0R
0	0	0	0	INTERRUPT MASK	R0W
0	0	1	1	COMMAND STATUS	R1R
0	0	1	0	UNUSED	–
0	1	0	1	ADDRESS STATUS	R2R
0	1	0	0	ADDRESS MODE	R2W
0	1	1	1	AUXILIARY COMMAND	R3R
0	1	1	0	AUXILIARY COMMAND	R3W
1	0	0	1	ADDRESS SWITCH*	R4R
1	0	0	0	ADDRESS	R4W
1	0	1	1	SERIAL POLL	R5R
1	0	1	0	SERIAL POLL	R5W
1	1	0	1	COMMAND PASS-THROUGH	R6R
1	1	0	0	PARALLEL POLL	R6W
1	1	1	1	DATA IN	R7R
1	1	1	0	DATA OUT	R7W

*External to S68488

Interrupt Request ($\overline{\text{IRQ}}$) — The $\overline{\text{IRQ}}$ output goes to the common interrupt bus for the MPU. This is an open drain output which is wire-ORed to the $\overline{\text{IRQ}}$ bus. The IRQ is set false (low) when an enabled interrupt occurs and stays false until the MPU reads from the interrupt status register.

$\overline{\text{Reset}}$ — The active low $\overline{\text{Reset}}$ line is used to initialize the chip during power on start up. $\overline{\text{Reset}}$ will be driven by an external power-up reset circuit.

DMA Control Lines (DMA Grant, DMA Request) — The DMA request line is used to signal waiting data when Byte In (BI) or Byte Out (BO) is set high for a DMA controller. The DMA request line is set high if either the BI or BO interrupt flags are set in the Interrupt Status Register (ROW) and the corresponding bits in the Interrupt Mask Register (ROR) are set true.

The DMA request line is cleared when the DMA grant is made true. The DMA grant line is used to signal the GPIA that the DMA controller has control of the MPU data and address lines.* *DMA Grant must be grounded when not in use!*

Address Switch Enable ($\overline{\text{ASE}}$) — The $\overline{\text{ASE}}$ output is used to enable the device address switch three-state buffers to allow the instrument address switch to be read on the MPU bus.

Clock Input (Clk) — The clock input is normally a derivative of the MPU ϕ2 clock.

GPIA/488 Interface Bus Signals

The GPIA provides a set of eighteen interface signal lines between the S6800 and the IEEE Standard 488 bus.

Signal Lines ($\overline{\text{IB0}}$-$\overline{\text{IB7}}$) — These bidirectional lines allow for the flow of seven bit ASCII interface messages and device-dependent messages. Data appears on these lines in a bit-parallel byte-serial form. These lines are buffered by the transceivers and applied to the 488 but (DIO1-DIO8).

Byte Transfer Lines (DAC, RFD, $\overline{\text{DAV}}$) — These lines allow for proper transfer of each data byte on the bus between sources and acceptors. RFD goes passively true, indicating that all acceptors are "ready for data." A source will indicate the "data is valid" by pulling $\overline{\text{DAV}}$ low. Upon the reception of valid data by all acceptors, DAC will go passively true, indicating that the "data has been accepted" by all acceptors.

Bus Management Lines ($\overline{\text{ATN}}$, $\overline{\text{IFC}}$, $\overline{\text{SRQ}}$, EOI, $\overline{\text{REN}}$) — These lines are used to manage an orderly flow of information across the interface lines.

Attention ($\overline{\text{ATN}}$) — This is sent true over the interface to disable current talker and listeners, freeing the signal lines ($\overline{\text{IB0}}$-$\overline{\text{IB7}}$). During the $\overline{\text{ATN}}$, active state devices monitor the DIO1 for addressing or an interface command. Data flows on the DIO1 lines when $\overline{\text{ATN}}$ is inactive (high).

Interface Clear ($\overline{\text{IFC}}$) — This is used to put the interface system into a known quiescent state.

Service Request ($\overline{\text{SRQ}}$) — This is used to indicate a need for attention in addition to requesting an interruption in the current sequence of events. This indicates to the controller that a device on the bus is in need of service.

Remote Enable ($\overline{\text{REN}}$) — This is used to select one of two alternate sources of device programming data, local or remote control.

End of Identify ($\overline{\text{EOI}}$) — This is used to signal the end of a multiple byte transfer sequence and, in conjunction with $\overline{\text{ATN}}$, executes a parallel polling sequence.

Transmit/Receive Control Signals (T/$\overline{\text{R}}$1, T/$\overline{\text{R}}$2) — These two signals are used to control the quad transceivers which drive the interface bus. It is assumed that appropriate transceivers will be used where each transceiver has a separate transmit/receive control pin. These pins can support one TTL load each. The outputs can then be grouped as shown in the Block Diagram with $\overline{\text{SRQ}}$ hardwired high to transmit. The transmit/receive inputs of $\overline{\text{REN}}$, $\overline{\text{IFC}}$, and $\overline{\text{ATN}}$ are hardwired low to receive. ROI is controlled by T/$\overline{\text{R}}$1 through the S3448A (or an equivalent), allowing it to transmit or receive. T/$\overline{\text{R}}$1 operates exactly as T/$\overline{\text{R}}$2 except dur-

ing the parallel polling sequence. During parallel poll, $\overline{\text{EOI}}$ will be made an input by T/$\overline{\text{R}}$1 while $\overline{\text{DAV}}$ and IB0-IB7 lines are outputs.

GPIA INTERNAL CONTROLS AND REGISTERS*

There are fifteen locations accessible to the MPU data bus which are used for transferring data to control the various functions on the chip and provide current chip status. Seven of these registers are write only and eight registers are read only. The various registers are accessed according to the three least significant bits of the MPU address bus and the status of the Read/Write line. One of the fifteen registers is external to the IC but an address switch register is provided for reading the address switches. Table 2 shows actual bit contents of each of the registers.

*Note: Upper and lower case type designations will be used with the register bits to indicate remote or local messages, respectively.

Table 2

	7	6	5	4	3	2	1	0	
R0W	IRQ	BO	GET		APT	CMD	END	BI	Interrupt "Mask" Reg.
R0R	INT	BO	GET		APT	CMD	END	BI	Interrupt Status Reg.
R1R	UACG	REM	LOK		RLC	SPAS	DCAS	UUCG	Command Status Reg.
R1W									Unused
R2R	ma	to	lo	ATN	TACS	LACS	LPAS	TPAS	Address Status Reg.
R2W	dsel	to	lo		hide	hlda		apte	Address Mode Reg.
R3R	Reset	DAC	$\overline{\text{DAV}}$	RFD	msa	rtl	ulpa	fget	Auxiliary Command Reg.
R3W		rfdr	feoi	dacr			dacd		
R4R	UD3	UD2	UD1	AD5	AD4	AD3	AD2	AD1	Address Switch Reg.
R4W	lsbe	dal	dat	AD5	AD4	AD3	AD2	AD1	Address Register
R5R	S8	SRQS	S6	S5	S4	S3	S2	S1	Serial Poll Reg.
R5W		rsv							
R6R	B7	B6	B5	B4	B3	B2	B1	B0	Command Pass-thru Reg.
R6W	PPR8	PPR7	PPR6	PPR5	PPR4	PPR3	PPR2	PPR1	Parallel Poll Reg.
R7R	D17	D16	D15	D14	D13	D12	D11	D10	Data In Register
R7W	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	Data Out Register

Data-In Register R7R — The data-in register is an actual eight-bit storage register used to move data from the interface bus when the chip is a listener. Reading the register does not destroy information in the data-out register. DAC (data accepted) will remain low until the MPU removes the byte from the data-in register. The chip will automatically finish the handshake by allowing DAC to go high. In RFD (ready for data) holdoff mode, a new handshake is not initiated until a command is sent allowing the chip to release holdoff. This will delay a talker until the available information has been processed.

Data-In Register (Read Only)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

DI0-DI7 correspond to DIO1-DIO8 of the 488-1975 Standard and $\overline{IB0}$-$\overline{IB7}$ of the S68488.

Data Out Register R7W — The data-out register is an actual eight-bit storage register used to move data out of the chip onto the interface bus. Reading from the data-in register has no effect on the information in the data-out register. Writing to the data-out register has no effect on the information in the data-in register.

Data Out Register (Write Only)

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

DO0-DO7 correspond to the DIO1-DIO8 of the 488-1975 Standard and $\overline{IB0}$-$\overline{IB7}$ of the S68488.

Interrupt Mask Register ROW — The Interrupt Mask Register is a seven-bit storage register used to select the particular events that will cause an interrupt to be sent to the MPU. The seven control bits may be set independently of each other. If dsel (bit 7 of the Address Mode Register) is set high, CMD bit 2 will interrupt on SPAS or RLC. If dsel is set low, CMD will interrupt on UACG, UUCG, and DCAS in addition to RLC and SPAS. The Command Status Register R1R may then be used to determine which command caused the interrupt. Setting GET bit 5 allows an interrupt to occur on Group Execute Trigger Command. END bit 1 allows an interrupt to occur if $\overline{EOI}$ is true (low) and $\overline{ATN}$ is false (high). APT bit 3 allows an interrupt to occur, indicating that a secondary address is available to be examined by the MPU if apte (bit 0 of Address Mode Register) is enabled and listener or talker primary address is received and a Secondary Command Group is received. A typical response for a valid secondary address would be to set msa (bit 3 of Auxiliary Command Register) true and dacr (bit 4 Auxiliary Command Register) true, releasing the DAC handshake. BI indicates that a data byte is waiting in the data-in register. BI is set high when data-in register is full. BO indicates that a byte from the data-out register has been accepted. BO is set when the data-out register is empty. IRQ enabled high allows any interrupt to be passed to the MPU.

Interrupt Mask Register (Write Only)

IRQ	BO	GET	X	APT	CMD	END	BI

IRQ — Mask bit for IRQ pin
BO — Interrupt on byte output
GET — Interrupt on Group Execute Trigger
APT — Interrupt on Secondary Address Pass-Through
CMD — Interrupt on SPAS + RLC + $\overline{dsel}$ (DCAS + UUCG + UACG)
END — Interrupt on EOI and $\overline{ATN}$
BI — Interrupt on byte input

Interrupt Status Register R0R — The Interrupt Status Register is a seven-bit storage register which corresponds to the interrupt mask register with an additional bit INT bit 7. Except for the INT bit, the other bits in the status register are set regardless of the state of the interrupt mask register when the corresponding event occurs. The $\overline{IRQ}$ (MPU interrupt) is cleared when the MPU reads from the register. INT bit 7 is the logical OR of the other six bits ANDed with the respective bit of ROW.

Interrupt Status Register (Read Only)

INT	BO	GET	X	APT	CMD	END	BI

INT — Logical OR of all other bits in this register ANDed with the respective bits in the interrupt mask register
BO — A byte of data has been output
GET — A Group Execute Trigger has occurred
APT — An Address Pass-Through has occurred
CMD — SPAS + RLC + $\overline{dsel}$ (DCAS + UUCG + UACG) has occurred
END — An EOI has occurred with $\overline{ATN}$ = 0
BI — A byte has been received

Serial Poll Register R5R/W — The Serial Poll Register is an eight-bit storage regiter which can be both written into and read by the MPU. It is used for establishing the status byte that the chip sends out when it is serial poll enabled. Status may be placed in bits 0 through 5 and bit 7. Bit 6 rsv (request for service) is used to drive the logic which controls the $\overline{SRQ}$ line on the bus telling the controller that service is needed. This same logic generated the signal SRQS which is substituted in bit 6 position when the status byte is read by the MPU $\overline{IB0}$-$\overline{IB7}$. In order to initiate a rsv (request for service), the MPU sets bit 6 true (generating rsv signal) and this in turn causes the chip to pull down the $\overline{SRQ}$ line. SRQS is the same as rsv when SPAS is false. Bit 6 as read by the MPU will be the SPQS (Service Request State).

Serial Poll Register (Read)

S8	SRQS	S6	S5	S4	S3	S2	S1

S1-S8 — Status bits
SRQS — Bus in Service Request State

Serial Poll Register (Write)

S8	rsv	S6	S5	S4	S3	S2	S1

S1-S8 — Status bits
rsv — Generate a service request

Parallel Poll Register R6W — This register will be loaded by the MPU and the bits in this register will be delivered to the instrument but IB0-IB7 during PPAS (Parallel Poll Active State). This register powers up in the PPO (Parallel Poll No Capability) state. The reset bit (Auxiliary Command Register bit 7) will clear this register to the PPO state.

The parallel poll interface function is executed by this chip using the PP2 subset (Omit Controller Configuration Capability). The controller cannot directly configure the parallel poll output of this chip. This must be done by the MPU. The controller will be able to indirectly configure the parallel poll by issuing an addressed command which has been defined in the MPU software.

Parallel Poll Register (Write Only)

PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1

Bits delivered to bus during Parallel-Poll Active State (PPAS)
Register powers up in the PPO state
Parallel Poll is executed using the PP2 subset

Address Mode Register R2W — The address mode register is a storage register with six bits for control: to, lo, hlde, hlda, dsel, and apte. The to bit 6 selects the talker/listener and addresses the chip to talk only. The lo bit 5 selects the talker/listener and sets the chip to listen only. The apte bit 0 is used to enable the extended addressing mode. If apte is set low, the device goes from the TPAS (Talker Primary Address State) directly to the TADS (Talker Addressed State). The hlda bit 2 holds off RFD (Ready for Data) on ALL DATA until rfdr is set true. The hlde bit 3 holds off RFD on EOI enabled (low) and ATN not enabled (high). This allows the last byte in a block of data to be continually read as needed. Writing rfdr true (high) will allow the next handshake to proceed.

Address Mode Register (Write Only)

dsel	to	lo	X	hdle	hdla	X	apte

dsel — Configure for automatic completion of handshake sequence on occurrence of GET, UACG, UUCG, SDC, or DCL commands.
to — Set to talk-only mode.
lo — Set to listen-only mode.
hdle — Hold-off RFD on end.
hdla — Hold-off RFD on all data.
apte — Enable the address pass-through feature.

Address Status Register R2R — The address status register is not a storage register but simply an eight-bit port used to couple internal signal nodes to the MPU bus. The status flags represented here are stored internally in the logic of the chip. These status bits indicate the addressed state of the talker/listener as well as flags that specify whether the chip is in the talk only or listen only mode. The ATN, bit 4, contains the condition of the Attention Line. The ma signal is true when the chip is in:

TACS — Talker Active State
TADS — Talker Addressed State
LACS — Listener Active State
LADS — Listener Addressed State
SPAS — Serial Poll Active State

Address Status Register (Read Only)

ma	to	lo	ATN	TACS	LACS	LPAS	TPAS

ma — My address has occurred.
to — The talk-only mode is enabled.
lo — The listen-only mode is enabled.
ATN — The Attention command is asserted.
TACS — GPIA is in the Talker Active State.
LACS — GPIA is in the Listener Active State.
LPAS — GPIA is in the Listener Primary Addressed State.
TPAS — GPIA is in the Talker Primary Addressed State.

Address Switch Register R4R — The address switch register is external to the chip. There is an enable line (ASE) to be used to enable three-state drivers connected between the address switches and the MPU. When the MPU addresses the address switch register, the enable line directs the switch information to be sent to the MPU. The five least significant bits of the eight-bit register are used to specify the bus address of the device, and the remaining three bits may be used at the discretion of the user. The most probable use of one or two of the bits is for controlling the listener only or talk only functions.

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Address Switch Register (Read Only)

UD3	UD2	UD1	AD5	AD4	AD3	AD2	AD1

AD1-AD5 — Device address.
UD1-UD3 — User definable bits.

When this "register" is addressed, the $\overline{\text{ASE}}$ pin is set, allowing external address switch information from bus device to be read.

Address Register R4W — The Address Register is an eight-bit storage register. The purpose of this register is to carry the primary address of the device. The primary address is placed in the five least significant bits of the register. If external switches are used for device addressing, these are normally read from the Address Switch Register and then placed in the Address Register by the MPU.

AD1 through AD5 bits 0-5 are for the device's address. The lsbe bit 7 is set to enable the Dual Primary Addressing Mode. During this mode, the device will respond to two consecutive addresses, one address with AD1 equal to 0 and the other address with AD1 equal to 1. For example, if the device's address is HEX 0F, the Dual Primary Addressing Mode would allow the device to be addressed at both HEX 0F and HEX 0E. The dal bit 6 is set to disable the listener and the dat bit 5 is set to disable the talker.

This register is cleared by the $\overline{\text{Reset}}$ input only (not by the reset bit of the Auxiliary Command Register bit 7).

When $\overline{\text{ATN}}$ is enabled and the primary address is received on the $\overline{\text{IB0-7}}$ lines, the S68488 will set bit 7 of the address status register (ma). This places the S68488 in the TPAS or LPAS.

When $\overline{\text{ATN}}$ is disabled, the GPIA may go to one of three states: TACS, LACS or SPAS.

Address Register (Write Only)

lsbe	dal	dat	AD5	AD4	AD3	AD2	AD1

lsbe — Enable dual primary addressing mode.
dal — Disable the listener.
dat — Disable the talker.
AD1-AD5 — Primary device address, usually read from address switch register.

Register is cleared by the $\overline{\text{Reset}}$ input pin only.

Auxiliary Command Register R3R/W — Bit 7, reset, initializes the chip to the following states: (Reset is set true by external $\overline{\text{Reset}}$ input pin and by writing into the register from the MPU.)

SIDS — Source Idle State
AIDS — Acceptor Idle State
TIDS — Talker Idle State
LIDS — Listener Idle State
LOCS — Local State
NPRS — Negative Poll Response State
PPIS — Parallel Poll Idle State
PUCS — Parallel Poll Unaddressed to Configure State
PPO — Parallel Poll No Capability

rfdr (release RFD handshake) bit 6 allows for completion of the handshake that was stopped by RFD (Ready for Data) holdoff commands hlda and hlde.

fget (force group execute trigger) bit 0 has the same effect as the GET (Group Execute Trigger) command from the controller.

rtl (return to local) bit 2 allows the device to respond to local controls and the associated device functions are operative.

dacr (release DAC handshake) bit 4 is set high to allow DAC to go passively true. This bit is set to indicate that the MPU has examined a secondary address or an undefined command.

ulpa (upper/lower primary address) bit 1 will indicate the state of the LSB of the address received on the DIO1-8 bus lines at the time the last Primary Address was received. This bit can be read but not written by the MPU.

msa (valid secondary address) bit 3 is set true (high) when TPAS (Talker Primary Addressed State) or LPAS (Listener Primary Addressed State) is true. The chip will become addressed to listen or talk. The primary address must have been previously received.

RFD, $\overline{\text{DAV}}$, DAC (Ready for Data, Data Valid, Data Accepted) bits assume the same state as the corresponding signal on the S68488 package pins. The MPU may only read these bits. These signals are not synchronized with the MPU clock.

dacd (data accept disable) bit 1 set high by the MPU will prevent completion of the automatic handshake on Addresses or Commands. dacr is used to complete the handshake.

feoi (forced end or identify) bit 5 tells the chip to send $\overline{\text{EOI}}$ low. The $\overline{\text{EOI}}$ line is then returned high after the next byte is transmitted. NOTE: The following signals are not stored but revert to a false (low) level one clock cycle (MPUϕ2) after they are set true (high):

1. rfdr
2. feoi
3. dacr

These signals can be written but not read by the MPU.

Auxiliary Command Register

RESET	rfdr	feoi	dacr	msa	rtl	dacd	fget	WRITE
	DAC	DAV	RFE			ulpa		READ

reset — initialize the chip to the following status:
       (1) all interrupts cleared
       (2) following bus states are in effect: SIDS, AIDS, TIDS, LIDS,
          LOCS, PPIS, PUCS, and PPO
       (3) bit is set by $\overline{\text{Reset}}$ input pin
msa — if GPIA is in LPAS or TDAS, setting msa will force GPIA to
       LADS or TADS
rtl — return to local if local lockout is disabled
ulpa — state of LSB of bus at-last-primary-address receive time
fget — Force group execute trigger command from the MPU has
       occurred
rfdr — continue handshake stopped by RFD holdoff
feoi — set EOI true, clears after next byte transmitted
dacr — MPU has examined an undefined command or secondary
       address
dacd — prevents completion of automatic handshake on Addresses or
       Commands

Command Status Register R1R — The command status register flags commands or states as they occur. These flags or states are simply coupled onto the MPU bus. There are five major address commands. REM shows the remote/local state of the talker/listener. RLC bit 3 is set when a change of state of the remote/local flip-flop occurs and reset when the command status register is read. DCAS bit 1 indicates that either the device clear or selected device clear has been received activating the device clear function. SPAS bit 2 indicates that the SPE command has been received activating the device serial poll function. UACG bit 7 indicates that an undefined address command has been received and depending on programming the MPU decides whether to execute or ignore it. UUCG bit 0 indicates that an undefined universal command has been received.

Command Status Register
(Read)

UACG	REM	LOK	X	RLC	SPAS	DCAS	UUCG

UACG — Undefined Addressed Command
REM — Remote Enabled
LOK — Local Lockout Enabled
RLC — Remote/Local State Changed
SPAS — Serial Poll Active State is in effect
DCAS — Device Clear Active State is in effect
UUCG — Undefined Universal Command

Command Pass-Through Register R6R — The command pass-through is an eight-bit port with no storage. When this port is addressed by MPU it connects the instrument data bus ($\overline{\text{IB0}}$-$\overline{\text{IB7}}$) to the MPU data bus D0-D7. This port can be used to pass commands and secondary addresses that aren't automatically interpreted through to the MPU for inspection.

Command Pass-Through Register
(Read Only)

B7	B6	B5	B4	B3	B2	B1	B0

An eight-bit input port used to pass commands and secondary addresses to MPU which are not automatically interpreted by the GPIA.

AMI®

S1883 BLOCK DIAGRAM

PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 3M, 1T - see Sec. 1)

FEATURES

- 12.5 K Baud Data Rates
- 5-8 Bit Word Length
- Parity Generation/Checking Odd, Even, None
- Framing and Overflow Error Detection
- 1, 1.5, or 2 Stop Bits

- Double Buffered Input/Output
- Independent Transmit/Receive Rates
- Start and Stop Bits Generated and Detected
- Interchangeable with TMS6011, COM2017, TR1602, AY-5-1013
- Tri-State Outputs

FUNCTIONAL DESCRIPTION

The S1883 Universal Asynchronous Receiver Transmitter (UART) is a single chip MOS/LSI device that totally replaces the asynchronous parallel to serial and serial to parallel conversion logic required to interface a word parallel controller or data terminal to a bit serial communication network.

For asynchronous data transmission with a non-contiguous data bit stream, the UART automatically inserts a START bit preceding each character and under program control 1, 1.5, or 2 stop bits at the end of each character. To detect incoming characters in a noisy environment the UART employs a START bit detection network and allows errorless recovery of data with up to 42% distortion.

The UART will transmit or receive data characters of 5, 6, 7, or 8 bit length. Options allow the generation and checking of odd, even parity or no parity. The odd or even parity bit is automatically added to the character length for transmission.

BLOCK DIAGRAM

PIN/PACKAGE CONFIGURATION

FEATURES

- 500 KHz Data Rates
- Internal Sync Detection
- Fill Character Register
- Double Buffered Input/Output
- Bus Oriented Outputs

- 5–8 Bit Characters
- Odd/Even or No Parity
- Error Status Flags
- Single Power Supply (+5v)
- Input/Output TTL Compatible

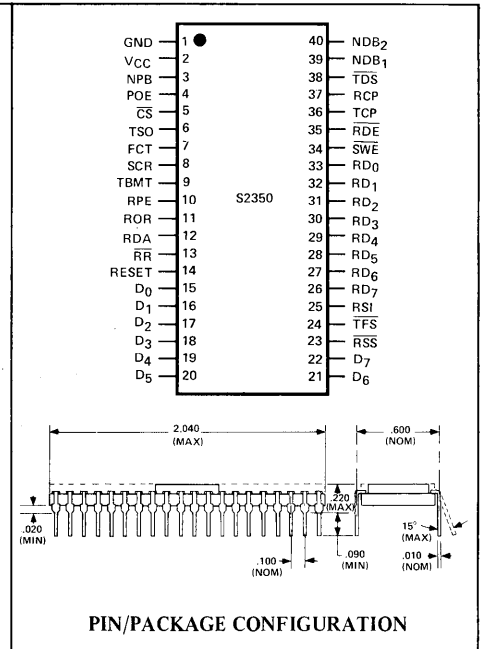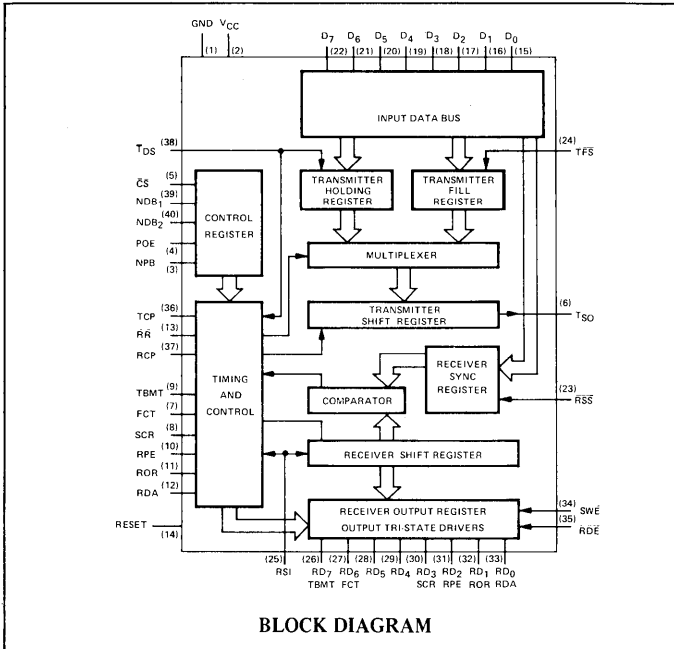## FUNCTIONAL DESCRIPTION

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8 bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character

3.171

AMI Microcomputer Development Center

An intelligent stand-alone software debugging station, serving completely the combined needs of the design engineer and the programmer. It consists of a S6800 based CRT/keyboard microcomputer terminal, a dual drive floppy disk memory, and an optional hard copy printer.

A program in development (or in operation) can be viewed on the CRT and edited on the keyboard. Program files can be assembled and stored in the floppy disk memory, under control of the disk memory operating system software. The modular bus oriented card cage in the CRT terminal provides versatile facilities for developing and testing 6800 hardware.
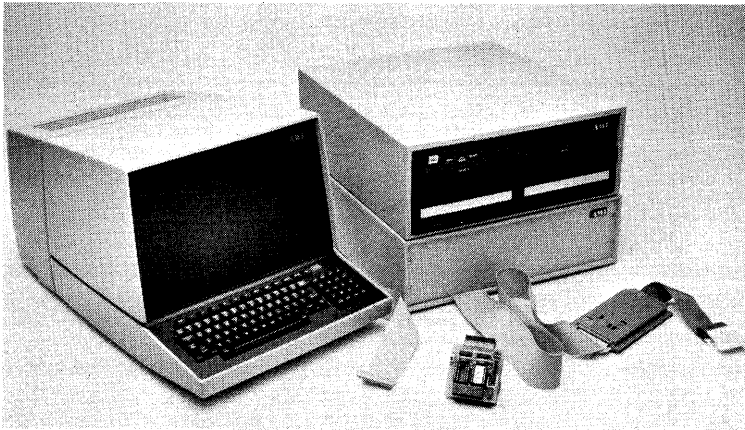
CRT/Keyboard Terminal

☐ Capability for generating 256 unique ASCII input characters

☐ 12-inch diagonal CRT display — 25 lines of 80 characters

☐ 16K bytes of user available RAM, expandable to 48K

☐ Full cursor and editing controls

☐ Special function controls

☐ Peripheral interconnects

Logic Analyzer

☐ General-purpose logic analyzer

☐ Plugs into MDC-100

☐ Trace memory hold 1024 steps

☐ All patterns 40 channels wide

☐ Two separate event qualifiers

☐ Data-dependent clock

☐ Outbound trigger

Floppy Disk Memory

☐ IBM 3740 data format compatible

☐ Data storage capacity of 256,256 bytes per diskette

☐ Fully supported by FDOS-II Disk Operating and File Management System software

Optional Matrix Printer

☐ 132 column

☐ Dot matrix, impact printing

☐ 120 or 180 characters per second

S2000 Support

S2000 Designers can use the DEV-2000 Development Board to provide a direct link between the MDC and the user's prototype. As stand-alone systems, the S2000 designer can use the capabilities of either the low-cost SES-2000 hardware emulator — which is a pin-for-pin substitute for an S2000 microcomputer chip and contains its own EPROM memory — or the TES-S2000 functional go/no-go tester.

MDC Hardware Capabilities

The AMI MDC is a multifunction development center that single-handedly satisfies your requirements for software development, hardware development, and prototype checkout. The MDC can also double as a stand-alone communications terminal, a general purpose data processing system, or as an incoming parts tester.

Software Development — write, debug and operate S6800 and S2000 programs on the CRT terminal, using its internal RAM and the dual drive floppy disk for storage. The MDC comes with a full complement of support software, including the FDOS-II Disk Operating and File Management System, a Text Editor, an Assembler, Debugger, Trace, Telecommunications and Utilities.

Hardware Development — breadboard such cicruitry as interfaces or memories right on the MDC wirewrap prototyping board and plug into the CRT terminal card cage to operate with the MDC's S6800-based central processor in solving development problems. Use the control panel type functions of the CRT terminal for single step, stop-on-address, display, alter, and other similar program operations. The bus oriented card cage, position interchangeable plug-in card modules, and an extender card provide the flexibility to make hardware development easy. There is also a complete keyboard control led PROM programmer within the CRT terminal.

Prototype Checkout — with the advantages of a real-time test environment, rapid test program retrieval, single or multiple step execution, and hardware as well as software breakpoints, the checkout of prototype S2000 and S6800 circuitry is easy and efficient.

Stand-alone Communications Terminal — the CRT terminal has both RS-232 and current loop interfaces, supported by telecommunications firmware, for operation as a general purpose stand-alone intelligent terminal.

MDC Software Capabilities

The AMI MDC offers total facilities for rapidly developing applications and systems software. The entire MDC software system is at the user's instant disposal — a few simple keystrokes are needed to instantly access and execute any program. The FDOS-II disk based operating system provides complete system resource control to the programmer.

FDOS-II Disk Operating and File Management System — contains a resident module for bootstrapping the floppy disk memory and for disk I/O handling. It also contains an executive that performs all of the disk memory command line interpretations, file management and operational functions of the dual disk system. In addition, there are utility I/O and EPROM programming routines in FDOS-II.

The Text Editor — program provides the means for rapidly creating, examining and modifying stored files. The total capability of MDC's Text Editor exceeds that of many large minicomputer systems, and includes such features as storing searches and string substitutions.

The Symbolic Assembler — translates assembler language statements into executable machine language code. In conjunction with FDOS-II Operating and File Management Systems, assembling has been reduced to a series of simple operator keystrokes. Results of the assembly, automatically stored on disk, are immediately available for reference or execution.

MDC's Extensive Debug Program — effectively automates the functions of a computer control panel. Given control by simply pressing the DEBUG key or via program traps, Debug immediately responds with the display of machine and program status. Addition functions include:

    Register/data display and modification
    Instruction/subroutine step
    User definable debug macros
    Snapshot debug data of a running program
    Breakpoints (stop-on-address compare)
    Comment and header line displays

MDC's Trace Package — gives Debug the ability to display a trace of machine register contents, instruction mnemonics and operands before execution of any instruction or subroutine in the user's program. Microprocessor debugging has never been made easier.

MDC's Test Programs — are a set of self-test and diagnostics which verify that the hardware associated with the MDC is operating correctly. The programs are also helpful in isolating malfunctioning components. The program for testing the basic hardware is resident in EPROM and is activated by the keyboard TEST key.

AMI®

MICROCOMPUTER BOARDS/KITS

Features

- ☐ **Expandable to 4K Bytes ROM**
- ☐ **Expandable to 2K Bytes EPROM**
- ☐ **Expandble to 1K Bytes RAM**
- ☐ **EPROM Programming for S6834**
- ☐ **Expandable to 3 PIA's = 58 I/O Lines**
- ☐ **TTY Current Loop or RS232 Interface**
- ☐ **ROM Subroutine Program Library**
- ☐ **Selectable DMA Mode**

General Description

The EVK Series Board is a single PCB, hardware/ software system that can be used as a general purpose microcomputer. It allows system development using a functionally compatible system and reduced development time. With this system the basic 6800 family of parts can also be evaluated. The 10-1/2"x12" card has two edge connectors, one for the MPU Bus and one for the I/O. The EVK 300 is a fully assembled and tested board, while the EVK 200, EVK 100 and EVK 99 are in kit form. All kits are fully expandable to EVK 300 capabilities.

Series Block Diagram
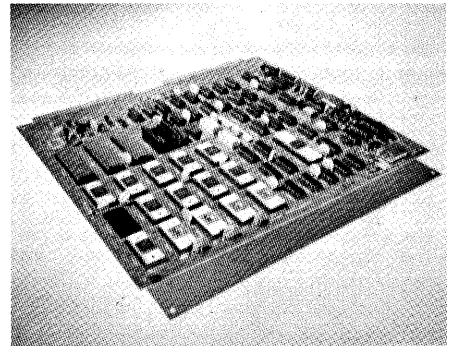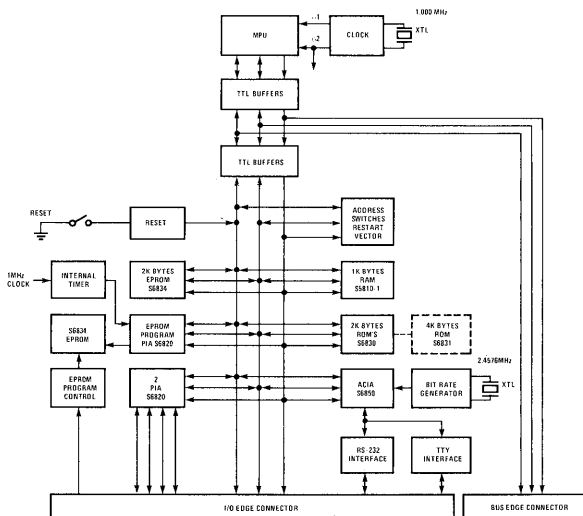
Address Assignment Map
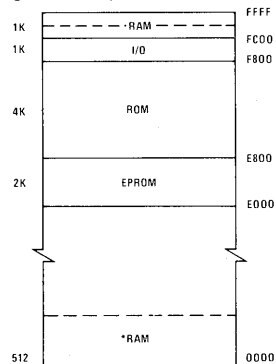
System Specifications

All of the S6800 microprocessor lines are available at the bus edge connector and are buffered to allow 40mA of drive capacity for expanding the development system. The standard system clock is adjustable from 300kHz to 1MHz by using the potentiometers on the board. An optional 1MHz crystal may be selected to control the accuracy for those applications requiring critical timings.

An on-board interval timer gives 1ms and 100μs timing marks for general use and for EPROM programming. Three types of DMA operation are possible using the EVK Board: Halt Processor, Cycle Steal or Multiplexing.

Memory

Memory and I/O addresses are assigned to the upper 8K bytes of the available memory space. (See memory map for address assignments.) This gives the system developer the flexibility to use the remaining 56K bytes as he wishes. All of the memory and I/O on the board may be disabled externally by an edge connector line called MEMORY DISABLE, leaving the MPU free to operate totally in an external memory.

The S6830 ROMs contain the Prototype Operating Library (PROTO) and a ROM Subroutine Library (RS)[3]. An optional Assembler/Disassembler (M/AD) S6831 ROM is available to operate with PROTO. The 2K of EPROM locations may also be used for program verification.

The RAM is assigned to the upper 1K of available memory space. The PROTO and (RS)[3] programs require about 256 bytes of this RAM so the rest is available for general programming. With all restart vectors automatically assigned to the upper memory addresses, restart vectoring is forced from a set of 16 switches. This allows the restart address to be vectored to any memory location.

The RAM has further been divided into two 512 byte sections such that the upper 512 bytes remain fixed in the assigned address block and the lower 512 bytes are moveable through a switch selection option. 512 bytes of RAM are relocatable to the lowest address space to take advantage of the S6800's direct addressing mode. This is only recommended if no external memory is added. When adding external memory, it is advisable to use the RAM in the upper address space and the external memory as the low addresses.

I/O

An S6850 ACIA is used to provide a 20mA current loop interface to a TTY or RS232 terminal. A 20mA current loop interface and an EIA RS232 interface are both available on the board. A bit rate generator allows operation using any of the standard communication frequencies (see table) so a large variety of terminal types can be used.

Three S6820 PIAs allow up to 58 I/O lines, giving flexibility in I/O through the parallel interfaces.

EPROM Programming

Unique to the AMI EVK Board is the ability to program S6834 EPROMs (512 x 8) on the board. The programming software can program an EPROM from any memory location, RAM, ROM or EPROM. It can verify a word and, if desired, change a single bit in the EPROM, provided that the change is from LOW to HIGH.

Software

The EVK Board Software is comprised of a TTY Operating Program (PROTO) and is supported by a ROM Subroutine Library (RS)[3].

EVK Capabilities

	ROM	RAM	EPROM	PIA	TTY CURR LOOP	ROM SUB-ROUTINE PROG. LIBRARY	TOTALLY BUFFERED MPU LINES	SGL +5V P.S.	RESTART ADDRESS SELECTION	SELECTABLE DMA MODE	INTERVAL TIMER	TINY BASIC
EVK 99	2K bytes	512 bytes	—	1	✔		✔	✔	✔			
EVK 100	2K bytes	512 bytes	—	—	✔	✔	✔	✔	✔			
EVK 200	4K bytes	1K bytes	512 bytes	3	✔	✔	✔	✔	✔	✔	✔	
EVK 300	4K bytes	1K bytes	2K bytes	3	✔	✔	✔	✔	✔	✔	✔	*✔

*AMI 6800 Tiny BASIC

— A high-level interpretive language derived from the standard Dartmouth BASIC. Furnished to EVK 300 users at no charge upon submittal of warranty registration.

The Proof from AMI

AMI's S2000 Family Compared to Other Major Low-End Single-Chip Microcomputers

Mfr	Device	MEMORY						INPUT/OUTPUT											HARDWARE THAT SAVES ROM SPACE							DEVELOPMENT SYSTEMS ($8K - $15K)					
		ROM X 8	RAM	EXPANDABLE ROM	CYCLE TIME (μSEC)	ANALOG TO DIGITAL CONVERTER	CONVERSION TIME (μSEC)	NUMBER OF MULTIPLEXED INPUTS	DIGITAL TO ANALOG CONVERTER	ZERO CROSSING DETECTOR	POWER FAIL DETECT	INTERNAL TIMER	INPUTS	OUTPUTS	BI-DIRECTIONAL I/O	TOUCH CONTROL	DIRECT LED AND HIGH CURRENT TRIAC DRIVE	VACUUM FLUORESCENT DISPLAY	INTERRUPTS	7-SEGMENT — HARDWARE DECODE	SUBROUTINE STACK LEVELS	FLAGS (DISCRETE)	RAM TEST BITS	TABLE — LOOK UP	NUMBER OF INSTRUCTIONS	FLOPPY DISK/CRT BASED DEVELOPMENT SYSTEM	EPROM PROGRAMMER	ASSEMBLER LOADER	TEXT EDITOR	SOFTWARE SIMULATOR	LOGIC ANALYZER
AMI	S2000	1K	64x4	YES	4.5	—	—	—	—	YES	—	50/60	9	13	8	YES	YES	2000A	—	YES	3	2	256	—	49	YES	YES	YES	YES	YES	YES
AMI	S2150	1.5K	80x4	YES	4.5	—	—	—	—	YES	—	50/60	9	13	8	YES	YES	2150A	—	YES	3	2	320	—	49	YES	YES	YES	YES	YES	YES
AMI	S2200	2K	128x4	YES	4.5	8 BIT	45	8	YES	YES	YES	8 BIT PROG	0	13	24	YES	YES	2200A	3	YES	5	6	512	YES	59	YES	YES	YES	YES	YES	YES
AMI	S2400	4K	128x4	YES	4.5	8 BIT	45	8	YES	YES	YES	8 BIT PROG	0	13	24	YES	YES	2400A	3	YES	5	6	512	YES	59	YES	YES	YES	YES	YES	YES
INTEL	8021	1K	64x8	NO	10.0	—	—	—	—	YES	—	8 BIT	0	0	20	—	—	—	—	—	8	0	0	YES	65+	YES	YES	YES	YES	YES	—
INTEL	8022	2K	64x8	NO	10.0	8 BIT	40	2	—	YES	—	8 BIT	0	0	24	—	—	—	—	—	8	0	0	YES	65+	YES	YES	YES	YES	YES	—
MOTOROLA	MK 3870	2K	64x8	NO	2.0	—	—	—	—	—	—	8 BIT	0	0	32	—	YES	—	—	—	1	4	0	YES	60+	—	YES	YES	YES	YES	—
MOTOROLA	MK 3876	2K		NO	2.0	—	—	—	—	—	—	8 BIT	0	0	32	—	YES	—	—	—	1	4	0	YES	60+	—	YES	YES	YES	YES	—
MOTOROLA	MK 3872	4K	128x8	NO	2.0	—	—	—	—	—	—	8 BIT	0	0	32	—	YES	—	—	—	1	4	0	YES	60+	—	YES	YES	YES	YES	—
MOTOROLA	6805	1.1K	64x8	NO	2.0	—	—	—	—	—	—	8 BIT	0	0	20	—	—	—	—	—	RAM	5	YES	—	58	YES	YES	YES	YES	YES	—
NATIONAL	COP 410L	512	32x4	NO	16.0	—	—	—	—	—	—	—	0	4	12	—	YES	—	1	—	2	0	128	NO	43	YES	YES	YES	YES	—	—
NATIONAL	COP 420	1K	64x4	NO	4.0	—	—	—	—	—	—	—	4	4	12	—	YES	—	1	—	3	0	256	NO	57	YES	YES	YES	YES	—	—
NATIONAL	COP 440	2K	128x4	NO	4.0	—	—	—	—	—	—	—	8	8	16	—	YES	—	1	—	3	0	512	NO	TBA	YES	YES	YES	YES	—	—
ROCKWELL	MM 75	640	48x4	NO	12.5	—	—	—	—	—	—	—	5	0	17	—	—	YES	—	YES	1	0	192	YES	69	NO/CRT	YES	YES	YES	YES	—
ROCKWELL	MM 76E	1K	48x4	NO	12.5	—	—	—	—	—	—	—	11	2	18	—	—	YES	—	YES	1	0	192	YES	69	NO/CRT	YES	YES	YES	YES	—
ROCKWELL	MM 77	1.3K	96x4	NO	12.5	—	—	—	—	—	—	—	11	2	18	—	—	YES	—	—	2	0	384	YES	69	NO/CRT	YES	YES	YES	YES	—
ROCKWELL	MM 78	2K	128x4	NO	12.5	—	—	—	—	—	—	—	11	2	18	—	—	YES	—	—	2	0	512	YES	69	NO/CRT	YES	YES	YES	YES	—
TEXAS INSTRUMENTS	TMS 1000	1K	64x4	NO	15.0	—	—	—	—	—	—	—	4	19	0	—	YES	—	—	PLA	1	0	256	NO	43	—	PAPER TAPE	YES	—	—	—
TEXAS INSTRUMENTS	TMS 1270	1K	64x4	NO	15.0	—	—	—	—	—	—	—	4	23	0	—	—	YES	—	PLA	1	0	256	NO	43	—	PAPER TAPE	YES	—	—	—
TEXAS INSTRUMENTS	TMS 1300	2K	128x4	NO	15.0	—	—	—	—	—	—	—	4	24	0	—	YES	—	—	PLA	1	0	512	NO	55	—	PAPER TAPE	YES	—	—	—

S2000 FAMILY DESIGN SUPPORT

The S2000 single-chip microcomputer is fully supported by a proven array of development aids. This includes AMI's Microcomputer Development Center, development software, SES-2000 Emulator Board, MDC-140 Logic Analyzer and customer assistance by AMI Applications Engineering staff.

Microcomputer Development Center (MDC)
AMI's MDC is a fully equipped, disk-based microcomputer development facility, complete with FDOS-II Floppy-Disk-Operating and File Management System. Controlled from its CRT terminal, MDC provides instant access to program and data files resident on removable diskettes. For use with the S2000, special interface boards are provided that permit debug and checkout of S2000-based prototype systems totally under MDC control.

Development Software
MDC's standard software includes a comprehensive Text Editor and PROM Programmer package that support S2000 software development. In addition, specialized S2000 software includes a MACRO-Assembler, Loader, and a sophisticated Instruction Simulator.
Cross-assemblers, editor and simulator/debug software are also available on a major timesharing service.

SES-2000 Emulator Board
The SES-2000/2150 Emulator Board is a pin-for-pin substitute for an S2000 microcomputer chip which uses conventional UV-erasable PROMs for program storage. The SES-2000 thus provides the equivalent of an S2000 microcomputer with erasable program memory. For high voltage output, the SES-2000A/2150A provides buffering suitable for use with fluorescent displays.

Customer Assistance
AMI's S2000 Applications Engineering staff are available for consultation regarding all aspects of S2000 usage. AMI'S staff is also available to discuss any special modifications to the S2000 for high volume applications.

MDC-140 Logic Analyzer
The MDC-140 Logic Analyzer is an advanced debug tool connected as a peripheral device of the AMI Microcomputer Development Center (MDC). Features include:

☐ Captures 1024 Events of 40 Parallel Inputs
☐ Captures Data Under Control of Programmable Start on Data Content
☐ Delay of −1024 to +64K Clock Periods
☐ Setup and Display of Captured Data Under Control of MDC Software
☐ Display Format is User-Definable; Captured Data Can Be Displayed in a Mix of Hex, Octal, Binary, ASCII and Special Formats for Support of S6800, S6820, S2000, 8080, etc.
☐ Four Clock Sources
☐ Input Voltage Range = −15 to +15 volts
☐ Adjustable Input Thresholds
☐ Data-Dependent Output for Triggering an Oscilloscope

AMI's MDC and SES-2000 Emulator Board provide a complete software development center and hardware prototyping facility.

AMI®

S2000
SINGLE-CHIP
MICROCOMPUTER
FAMILY

S2000

S2000 Single-Chip Microcomputer Family

AMI's S2000 family of single-chip microcomputers offers a wide range of capability to the user seeking flexible, adaptable system(s) at low cost. The S2000 family provides the ideal solution to appliance and industrial/process-control applications. With versatile keyboard-oriented inputs, and outputs which can drive either LED or fluorescent displays directly, the S2000 family is designed specifically to minimize system parts count and cost.

Table I. S2000 Family Features

	S2000	S2150	S2200	S2400
ROM (x8)	1K	1.5K	2K	4K
RAM (x4)	64	80	128	128
Interrupts	—	—	3	3
A/D CONV (8 Channel)	—	—	8-Bit	8-Bit
Counter/Timer	÷50/÷60	÷50/÷60	8-Bit	8-Bit
Max Subroutine Levels	3	3	5	5
Instructions	51	51	59	59
Cycle Time (μs)	4.5	4.5	4.5	4.5
High Voltage (Fluorescent Display Drive Version)	S2000A	S2150A	S2200A	S2400A

The S2000 family provides the advantages of computer architecture to low cost, minimum-parts-count display/keyboard oriented control systems.

S2000/2150 Features

☐ **1024 x 8 Program ROM On-Chip; Externally Expandable to 8192 x 8 — S2000**

☐ **1536 x 8 Program ROM On-Chip; Externally Expandable to 8192 x 8 — S2150**

☐ **64 x 4 Scratchpad RAM On Chip — S2000**

☐ **80 x 4 Scratchpad RAM On-Chip — S2150**

☐ **13 Outputs and Inputs, Plus 8 Bi-Directional Three-State Lines**

☐ **Touch Control™ Capacitive Touchplate Interface**

☐ **Seconds Timer for Both 60Hz and 50Hz Lines**

☐ **7-Segment Decoder and LED Display Drivers On Chip**

☐ **Single 9.0 Volt Supply**

☐ **Fast 4.5μs Execution Cycle**

☐ **Three-Level Subroutine Stack**

☐ **TTL-Compatible Outputs**

☐ **Reset, Test, and Single Step Modes**

☐ **Access to All Internal Registers and Memory for Debug and Test**

☐ **Crystal Input for Accurate Clocking — S2150**

☐ **Low Power RAM Retention, 20μA/Bit Typ @ 4V — S2150**

S2000A/2150A Vacuum Fluorescent Display

The S2000A/2150A are identical to the S2000/2150 but provide high voltage fluorescent display capability. The output buffer drive (V_{DD}) is changed to a vacuum fluorescent drive (V_{FD}) and typically tied to 32 volts. The D_0 through D_7 and A_0 through A_4 are changed from LED drivers (nominal 5 volts) to vacuum fluorescent drivers (nominal 26 volts).

S2200/2400 Features

The S2200/2400 provide a quantum jump in chip features beyond the S2000. In addition to all the features the S2000 offers, the S2200 gives the added flexibility of interrupts and the sophistication of an on-chip A/D or D/A converter capable of multiplexing 8 channels of analog data making it suitable for a wide range of applications.

☐ **2048 x 8 Program ROM On Chip Expandable to 8192 x 8 — S2200**

☐ **4096 x 8 Program ROM On-Chip; Externally Expandable to 8192 x 8 — S2400**

☐ **128 x 4 Scratchpad RAM On Chip**

☐ **RAM Save Power Down Mode (Mask Option)**

☐ **Two-Level Maskable Priority Interrupt System with Provision for Software Interrupt**

☐ **Programmable 8-Bit Timer/Event Counter On Chip**

☐ **13 Outputs, 9 Inputs, Plus 8 Bi-Directional Three-State Lines**

☐ **Touch Control™ Capacitive Switch Interface**

☐ **7-Segment Display Decoders and LED Drivers**

☐ **TTL-Compatible Outputs**

☐ **Single + 9V Power Supply**

☐ **4.5μs Cycle Time**

☐ **59 Instructions — 52 Single Byte and Single Cycle**

☐ **3-Level Subroutine Stack**

☐ **2-Level Interrupt Stack**

☐ **Built-In Production Test Mode**

☐ **Single-Step Capability**

☐ **Power-Fail Detect, RAM Keep-Alive and Power-On Reset Circuitry**

☐ **8-Bit A/D Converter (Up to 8 Channels)**

☐ **D/A Converter Capability (Mask Option)**

☐ **Up to 256 General Purpose Flags**

☐ **6 Special Flags**

☐ **Table Look-Up Capability**

☐ **S2200A/2400A Vacuum Fluorescent Display Capability**

S2000 Family

	S2000	S2000A	S2150	S2150A	S2200	S2200A	S2400	S2400A
Product Characteristics								
ROM (Bytes)	1K	1K	1.5K	1.5K	2K	2K	4K	4K
RAM (Nibbles)	64	64	80	80	128	128	128	128
A/D Converter (8-Bit)	—	—	—	—	YES	YES	YES	YES
Timer	50/60Hz	50/60Hz	50/60Hz	50/60Hz	PROG 8BIT	PROG 8BIT	PROG 8BIT	PROG 8BIT
Interrupts	—	—	—	—	3	3	3	3
Power Fail Detect	—	—	—	—	YES	YES	YES	YES
High Voltage Outputs	—	YES	—	YES	—	YES	—	YES
Crystal Clock Option	—	—	YES	YES	YES	YES	YES	YES
TouchControl Inputs	YES	YES	YES	YES	YES	YES	YES	YES
Levels of Subroutine	3	3	3	3	5	5	5	5
# of Flags	2	2	2	2	262	262	262	262
Power-Down RAM Option	—	—	YES	YES	YES	YES	YES	YES
D/A Converter Option	—	—	—	—	YES	YES	YES	YES
Zero — Crossing Detect	YES	YES	YES	YES	YES	YES	YES	YES
Cycle Time (μsec)	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5
Instructions — Total	51	51	51	51	59	59	59	59
Single Cycle & Byte	49	49	49	49	52	52	52	52

Development Support

Microcomputer Development Center	YES	YES	YES	YES	YES	YES	YES	YES
Logic Analyzer	YES	YES	YES	YES	YES	YES	YES	YES
Hardware Emulator	#2150	#2150A	#2150	#2150A	#2400	#2400A	#2400	#2400A

S2000

S2000 Family Support

The S2000 single-chip microcomputer family, unlike many microprocessors, does not leave the designer or industrial OEM unsupported. The S2000 Family features a proven array of development aids:

Microcomputer Development Center (MDC) — AMI's MDC is a fully equipped, dual-floppy disk-based microcomputer development facility, complete with FDOS-II Floppy-Disk-Operating and File Management System. Controlled from its CRT terminal, MDC provides instant access to program and data files resident on removable diskettes.

Development Software — The MDC's software includes self-diagnostics and a comprehensive Text Editor and PROM programmer package that support S2000 software development. In addition, S2000 software includes a MACRO Assembler, Loader, and Instruction Simulator.

Cross-Assemblers editor and simulator debug — Available on a major timesharing service.

Logic Analyzer — The MDC-140 Logic Analyzer is an advanced debug tool connected as a peripheral device of the AMI Microcomputer Development Center (MDC). Features include:

— Captures 1024 Events of 40 Parallel Inputs
— Captures Data Under Control of Programmable Start on Data Content
— Delay of – 1024 to + 64K Clock Periods
— Setup and Display of Captured Data Under Control of MDC Software
— Display Format is User-Definable; Captured Data Can Be Displayed in a Mix of Hex, Octal, Binary, ASCII and Special Formats for Support of S6800, S6820, S2000, 8080, etc.
— Four Clock Sources
— Input Voltage Range = – 15 to + 15 volts
— Adjustable Input Thresholds
— Data-Dependent Output for Triggering an Oscilloscope

SES-2150(A)/SES-2400(A) — The SES-2150/2400 Emulator boards are pin-for-pin substitutes for S2000 microcomputer family chips. The Emulator Boards use conventional UV erasable PROMs for program storage.

In addition, a specialized module is used to provide emulation of the S2150A/S2400A high voltage vacuum fluorescent display drivers.

Customer Assistance — AMI's S2000 Family Applications Engineering Staff is readily available for consultation regarding any aspects of S2000 Family usage. The AMI staff is also available to discuss any special modifications to the S2000 for high volume applications.

S2000 Family Instruction Set Summary

The S2000 and S2150 contain 51 instructions, all single byte, with 49 that are single cycle. The S2200 and S2400 contain 59 instructions, of which 52 are single cycle and single byte.

Nearly all S2000/2150 instructions are common to the entire family, which allows the programmer to develop software expertise and easily move up the S2000 product line.

Register Instructions

S2000/2150	S2200/2400	
LAI X	LAI X	X→ACC, 0≤X≤15; (In S2000/2150 Select I and K Inputs also)
LAB	LAB	BL→ACC
LAE	LAE	E→ACC
XAB	XAB	BL↔ACC
XABU	XABU	BU↔ACC, (IN S2150, BITS 2, 1, AND 0; IN OTHERS, BITS 1 AND 0 ONLY)
XAE	XAE	ACC↔E
LBE Y	LBE Y	Y→BU, E→BL, 0≤Y≤3
LBZ Y	LBZ Y	Y→BU, 0→BL, 0≤Y≤3
LBF Y		Y→BU, 15→BL, 0≤Y≤3
LBEP Y		Y→BU, E+1→BL, 0≤Y≤3
	SRB	1→BA
	RRB	0→BA
	LMDI X+	X(6)→BA, X(5−4)→BU, X(3−0)→BL
	RAR	ACC(I)→ACC(I−1), ACC(0)→CARRY, CARRY→ACC(3)
	XAK	KSR↔ACC
	LANG	ACC→AR(3−0), RAM→AR(7−4)
	LNMA	ACC→NR(3−0), RAM→NR(7−4), THEN NR→BIN
	MOD	ACC→MOD(3−0), RAM→MOD(7−4)
	RBIN	BIN(3−0)→ACC; BIN(7−4)→RAM

RAM Instructions

S2000/2150	S2200/2400	
LAM Y*	LAM Y*	RAM→ACC, BU ⊕ Y→BU
XC Y*	XC Y*	RAM↔ACC, BU ⊕ Y→BU
XCI Y*	XCI Y*	ACC↔RAM, BL+1→BL, BU ⊕ Y→BU SKIP IF BL=0 (AFTER INCREMENT)
XCD Y*	XCD Y*	ACC↔RAM, BL−1→BL, BU ⊕ Y→BU SKIP IF BL=0 (BEFORE DECREMENT)
STM Z	STM Z	1→RAM BIT Z, 0≤Z≤3
RSM Z	RSM Z	0→RAM BIT Z, 0≤Z≤3
	LMA	ACC→RAM
	STMI Z+	1→RAM BIT Z, 0≤Z≤255, (RAM BANK 1)
	RSMI Z+	0→RAM BIT Z, 0≤Z≤255, (RAM BANK 1)

Input/Output Instructions

S2000/2150	S2200/2400	
INP	IND	D3-D0→ACC, D7-D4→RAM
OUT	OUT	ACC→D3-D0, RAM→D7-D4 (NOT LATCHED)
DISN	DISN	ACC→SEGMENT DECODER→DISPLAY LATCH→D6-D0, CARRY→DISPLAY LATCH→D7
DISB	DISB	ACC→DISPLAY LATCH→D3-D0, RAM→DISPLAY LATCH→D7-D4
MVS	MVS	A-LINE MASTER STROBE LATCH→A LINES
PSH	PSH	PRESET HIGH [BL]→MASTER STROBE LATCH
PSL	PSL	PRESET LOW [BL]→MASTER STROBE LATCH
EUR		(EUROPEAN) SET 50/60Hz AND DISPLAY LATCH POLARITY
	INK	K3-K0→ACC, K7-K4→RAM

+8 bits in the second byte of an instruction.
*Assembled code contains complement of those arguments (the assembler does it automatically).

S2000/S2150 and S2200/S2400 Instruction Set Summary

Program Control Instructions

S2000/2150	S2200/2400	
PP X*	PP X*	IF PREVIOUS INSTRUCTION = PP, X→PPR $(0 \leq X \leq 15)$
		IF PREVIOUS INSTRUCTION = PP, X→PBR $(0 \leq X \leq 7)$
JMP X	JMP X	JUMP TO LOCATION X, X→LR $(0 \leq X \leq 15)$
		EXCEPT IF PREVIOUS INSTRUCTION = PP
JMS X	JMS X	JUMP TO SUBROUTINE AT X, LR + 1→L STACK, PR→P STACK,
		X→LR, 15→PR EXCEPT IF PREVIOUS INSTRUCTION = PP
RT	RT	L STACK→LR, P STACK→PR
RTS	RTS	L STACK→LR, P STACK→PR, SKIP INSTR.
NOP	NOP	NO OPERATION
	RTI	RETURN FROM INTERRUPT, RESTORE REGISTERS
	TLU	IF PREVIOUS INSTRUCTION WAS A PP, DO A TABLE LOOK-UP
		SEQUENCE:
		PC + 1→STACK
		RAM→PC(3 – 0), ACC→PC(7 – 4), PPR(3 – 2)→PC(9 – 8)
		ROM(7 – 4)→RAM, ROM(3 – 0)→ACC
		STACK→PC.
		IF PREVIOUS INSTRUCTION WAS NOT A PP, DO AN INDEXED
		SUBROUTINE CALL:
		PC + 1→STACK
		RAM→PC(3 – 0), ACC→PC(7 – 4)

Skip Instructions (Skip 1 Non-PP Instruction) (RAM = Memory at BU,BL)

S2000/2150	S2200/2400	
SZC	SZC	SKIP IF CARRY = 0
SZM Z	SZM Z	SKIP IF RAM BIT Z = 0, $0 \leq Z \leq 3$
SZK	SZK	SKIP IF K BIT(S) = 0, (BIT(S) IN LAST LAI)
SBE	SBE	SKIP IF BL = E
SAM	SAM	SKIP IF ACC = RAM
SZI		SKIP IF I BIT(S) = 0, (BIT(S) IN LAST LAI)
SOS		SKIP IF SF = 1, 0→SF. (SF = 'SECONDS' FLAG OUTPUT OF ÷50/÷60
		COUNTER)
TF1		SKIP IF FLAG 1 = 1
TF2		SKIP IF FLAG 2 = 1
	SZMI Z +	SKIP IF RAM BIT = 0, (IN RAM BANK 1) $0 \leq Z \leq 255$
	SKFL X +	SKIP IF FLAG = 1

Arithmetic and Logical Instructions

S2000/2150	S2200/2400	
ADCS	ADCS	RAM + ACC + CARRY→ACC + C, SKIP IF SUM ≤ 15
ADIS X	ADIS X	X + ACC→ACC, SKIP IF SUM ≤ 15, CARRY UNALTERED
ADD	ADD	ACC + RAM→ACC, CARRY UNALTERED
AND	AND	ACC & RAM→ACC
XOR	XOR	ACC ⊕ RAM→ACC
STC	STC	1→CARRY
RSC	RSC	0→CARRY
CMA	CMA	15 – ACC→ACC (LOGICAL 1's COMPLEMENT ACC)
SF1		1→FLAG 1
RF1		0→FLAG 1
SF2		1→FLAG 2
RF2		0→FLAG 2
	SFLG X +	1→FLAG X
	RFLG X +	0→FLAG X

+ 8 bits in the second byte of an instruction.
*Assembled code contains complement of those arguments (assembler does it for you).

AMI S2000/2150 Detailed Block Diagram

ADDRESS/CONTROL LINES
$A_0 ... _{11}$ AND A_{12}/RAM POWER

DATA/SEGMENT LINES (3-STATE)

$D_0 .. _3$ $D_4 .. _7$

TOUCH CONTROL $K_{1,2,4,8}$ KEY SWITCH $I_{1,2,4,8}$

KREF

SELECTOR — 3-LEVEL STACK*

SELECTOR   SELECTOR   KREF   ÷60 OR ÷50   SELECTOR

S2150 ROM 1.5K x 8 / S2000 ROM 1K x 8

DECODER

LATCH SELECT   LATCH SELECT

FLAGS

PROGRAM COUNTER — BANK / PAGE / LOC.   PREP

7-SEG DECODE

CARRY

CONTROL LOGIC

ROMS
RUN
POR
STATUS/XTAL2
EXT
SYNC

8 BIT BUS

SLAVE LATCH / MASTER LATCH   E   S2150 RAM 320 BITS 16 x 5 x 4 / S2000 RAM 16 x 4 x 4   DECODER   BU   SELECTOR   SELECTOR   ADDER   CARRY   OSC   CLK/XTAL1

INTERNAL CONTROLS

ACCUMULATOR

DECODER   BL

V_{GG} – LOGIC
V_{FD} or V_{DD} = OUTPUT BUFFERS
V_{SS} – GROUND

*S2150 – 11 BITS
S2000 – 10 BITS

S2000/S2150 Pin Configuration

Left	Pin	Pin	Right
(GRD) V_{SS}	1	40	D_3
D_2	2	39	D_4
D_1	3	38	D_5
D_0	4	37	D_6
ROMS	5	36	D_7
EXT	6	35	SYNC
(P.C. MSB) A_{12}	7	34	RUN
A_{11}	8	33	K_8
A_{10}	9	32	K_4
A_9	10	31	K_2
A_8	11	30	K_1
V_{DD}/V_{FD}	12	29	V_{GG} (+9V)
A_7	13	28	I_8 AND TIMER
A_6	14	27	I_4
A_5	15	26	I_2
A_4	16	25	I_1
A_3	17	24	K_{REF} TOUCH CONTROL
A_2	18	23	CLK*
A_1	19	22	POR
(P.C. LSB) A_0	20	21	STATUS*

*May be used for crystal input on S2150/2150A

Pin Descriptions — S2000/2150

PIN NO.	NAME	DESCRIPTION
1	V_{SS}	Most negative power-supply input. Typically grounded.
29	V_{GG}	Most positive power-supply input. Typically $+9V$.
12	V_{DD} (S2000) V_{FD} (S2000A)	Power supply input for all output buffers. Typically tied to V_{GG} or to a $+5V$ supply. Power supply input for HV drive. Typically $+32V$
4 — 2, 40 — 36	D0 — D7	D Lines for input and output. Output during instructions OUT, DISN, DISB. Input during INP. Float at reset time or after an MVS instruction; or if RUN pin is low; or after a PSL with BL = 14. Display Latch outputs (DISN, DISB) can be inverted using EUR.
20 — 13 11 — 7	A0 — A12	A Lines for addressing and control. Changed by MVS as set up by PSH/PSL. When external program ROM is used, these lines output the contents of the Program Counter during the first half of each instruction cycle.
5	ROMS	ROM source control. Tied to a logic 1 or 0 to indicate internal ROM only, or internal plus external. Tied to SYNC to override Bank 0 with an external program, and to inverted SYNC to verify internal ROM contents.
6	$\overline{EXT}$	Active-low strobe output for D Lines. Generated by an OUT instruction during time T7.*
35	SYNC	Synchronization output for external devices or for external ROM control. Continuous square wave, low in T1 and T3, high in T5 and T7.* $f_{CLK} \div f_{SYNC} = 4$ for S2000, 8 for S2150.
34	RUN	Run/Wait control for prototyping and single-step testing. Logic 1 to run, logic 0 to wait with D Lines floating.
22	$\overline{POR}$	Power-On-Reset. Needs only an external capacitor, typically .05 microfarad. A pull-up to V_{GG} ($15\mu A$ nominal) is provided internally.
23	CLK	On-chip oscillator connection. Runs at $\sim 850kHz$ when connected to V_{SS} through 47pf and to V_{GG} through $30k\Omega$ on the S2000. Crystal control possible; consult AMI.
21	STATUS	Monitors internal status for special designs. Logic 1 vs. logic 0 indicates: (during T1)* D Lines floating or not floating; (T3) BL equal or not equal to 13 for multiplex control; (T5) Carry is 1 or 0; (T7) Next instruction will or won't be skipped. On the S2150 a mask option allows use as a crystal oscillator pin.
24	KREF	K Lines voltage comparator reference input. Typically $+3.0V$, supplied by an external resistor divider.
30 — 33	K1, K2 K4, K8	K Lines, tested by SZK instruction. Any combination of these lines, selected by the last executed LAI instruction, are gated into the signal input of the voltage comparator. Unselected K Lines are discharged to V_{SS}, at $160\mu A$ typical.
25 — 28	I1, I2, I4, I8	I Lines, with internal pull-ups of $100\mu A$ nominal. Any combination of these lines, selected by the last executed LAI instruction (S2000, S2150), are gated into a common node tested by the SZI instruction. I8 also clocks a seconds timer whose output is tested using SOS.

*T1 is the first quarter-cycle following the falling edge of the SYNC output, T3 is the second, T5 is the third, and T7 is the fourth.

S2000/2150

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	$-55°C$ to $+125°C$
Operating Temperature	$0°C$ to $+70°C$
Operating Temperature (special request)	$-40°C$ to $+85°C$
Maximum Positive Voltage	$+18V$
Maximum Negative Voltage	$-0.3V$
Maximum Output Currents	(See "Conditions" below)
I_{DD} Supply Current (depends on output loads)	$+75mA$
Total Average Power Dissipation	$+700mW$

S2000/2150

Electrical Characteristics

($V_{SS} = 0V$, $V_{GG} = +7.5V$ to $+10.0V$, $V_{DD} = 5V^*$, $T_A = 0°C$ to $+70°C$, $f_{SYNC} = 125kHz$ to $225kHz$)

	Parameter	Min.	Typ.	Max.	Units	Conditions
INPUTS	K_1 thru K_8					$2.8 < K_{REF} < 3.2V$
	Low Level	0		$K_{REF} - 0.5$	V	
	High Level	$K_{REF} + 0.5$		V_{GG}	V	
INPUTS	I_1 thru I_8, POR					(Note 1)
	Schmitt-trigger					
	Low Level	0		1.7	V	
	High Level	5.3		V_{GG}	V	
INPUTS	ROMs, RUN					
	Low Level	0		0.8	V	
	High Level	3.5		V_{GG}		
INPUTS	D_0 thru D_7					
	Low Level	0		0.8	V	
	High Level — Program	5.0		V_{GG}	V	
	High Level — Data	3.5		V_{GG}	V	
OUTPUTS	A_0 thru A_3					
	High Level	3.5		$^*V_{DD}$	V	$I = -5mA^{**}$
	Low Level	0		0.8	V	$I = +25mA^{**}$
OUTPUTS	A_4 thru A_{12}					
	$\overline{EXT}$, SYNC, & S					
	High Level	3.5		$^*V_{DD}$	V	$I = -5mA^{**}$
	Low Level	0		0.6	V	$I = +5mA^{**}$
OUTPUTS	D_0 thru D_7					
	High Level	3.5		$^*V_{DD}$	V	$I = -5mA^{**}$
	Low Level	0		1.0	V	$I = +12mA^{**}$
I_{GG}	Supply Current		28	50	mA	
Δ RAM	RAM "Keep Alive"		20		$\mu A/Bit$	$V_{RAM} = 4.0V$
			30		$\mu A/Bit$	$V_{RAM} = 9.0V$

NOTE 1: There is an internal pull-up of $100\mu A$ nominal ($15\mu A$ nominal on $\overline{POR}$) from each of these inputs to V_{GG}.

$^*V_{DD}$ may be connected to V_{GG} if single power supply operation is desired.

**At $V_{GG} \geq 8.5VDC$

Δ Available only on S2150/S2150A.

S2000A/S2150A

Preliminary Electrical Specifications

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	$-55°C$ to $+125°C$
Operating Temperature	$0°C$ to $+70°C$
Operating Temperature (special request)	$-40°C$ to $+85°C$
Maximum Positive Voltage, V_{FD}, A_0-A_4, D_0-D_7	$+33V$
All other pins	$+18V$
Maximum Negative Voltage, any pin	$-0.3V$
Maximum Output Currents	(See Conditions below)
Source Current, any pin	$-10mA$
Total Average Power Dissipation	$+700mW$
Rate of Rise of V_{FD}	1.6V/msec.
Maximum Voltage at V_{FD} with respect to V_{GG}	$+22V$

S2000A/S2150A

Electrical Characteristics — Specifications noted only for parameters which change from the S2000/2150 to the S2000A/2150A.
($V_{SS} = 0V$, $V_{GG} = 7.5$ to $10.0V$, $V_{FD} = V_{GG} + 22V$, $T_A = 0°C$ to $+70°C$. $f_{SYNC} = 125kHz$ to $225kHz$)

|	Parameter	Min.	Typ.	Max.	Units	Conditions
OUTPUTS	D_0 thru D_7, A_0 thru A_4 High Level Low Level	-3.5		0.6	mA V	$V_{OUT} = V_{FD} - 6V$** $I = 250\mu A$**
OUTPUTS	A_5 thru A_{12}, EXT, SYNC, & STATUS High Level Low Level	3.5		0.6	V V	$I = -5mA$** $I = +5mA$**
I_{GG}	Supply Current		28	50	mA	No Loads

NOTE 1: The output buffers for lines A_5-A_{12} are supplied from V_{GG}.

NOTE 2: The high voltage parts, when biased with normal V_{FD}, are not TTL-compatible; when using external program ROM, it is necessary to interpose buffers.

NOTE 3: When applying power, V_{FD} must rise with or after V_{GG} at a rate not to exceed 1.6V/msec.

**At $V_{GG} \geq 8.5VDC$

S2000
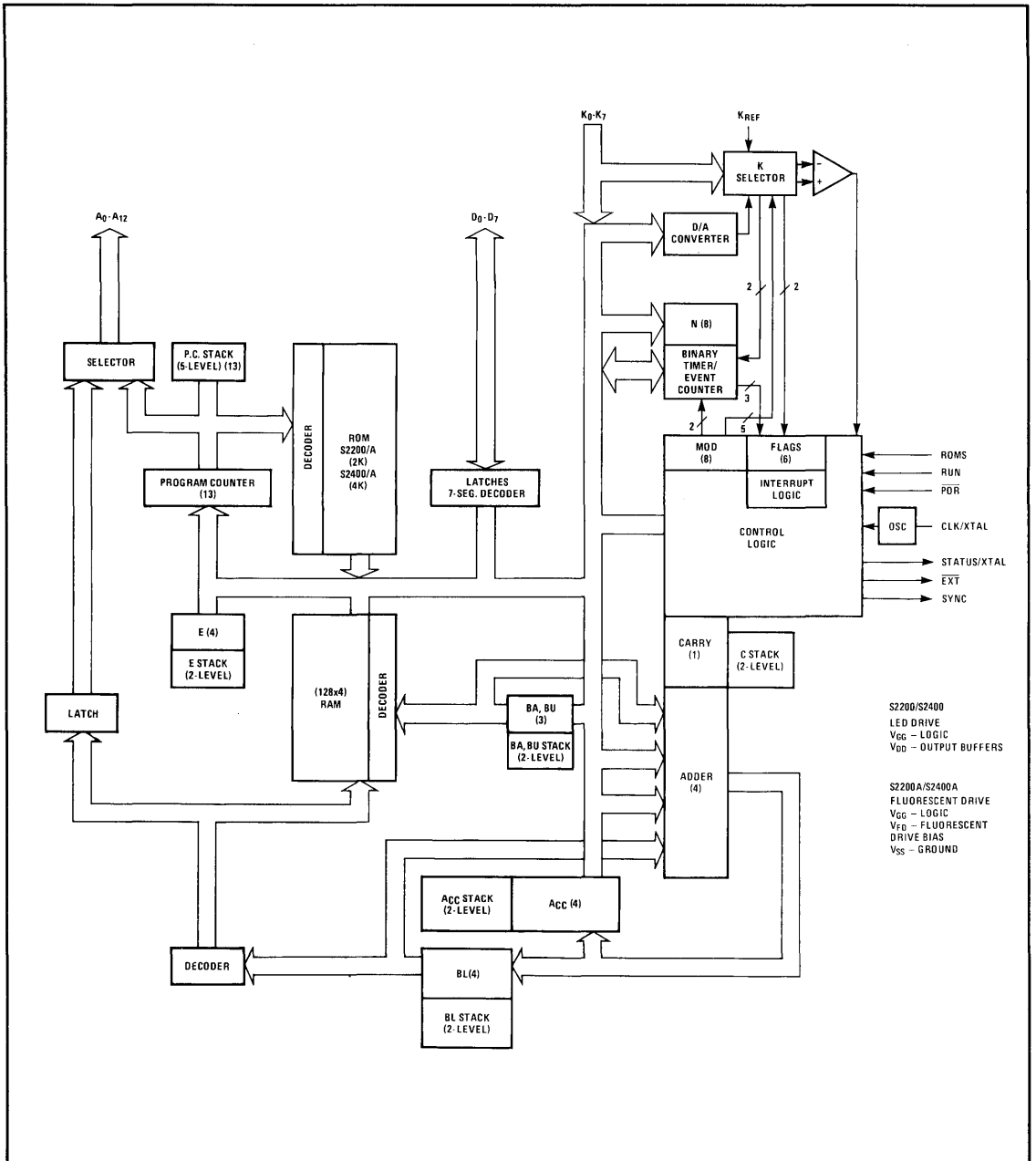
S2200/2400 Block Diagram

For applications such as pulse width measurement, interval timing and event counting, the S2200/2400 has an 8-bit binary down-counter which counts 256 distinct states. The number of states (1 to 256) is controlled by the (Modulo-) N Register.

Another register, the MOD Register, controls the selection of inputs and outputs for the Programmable Counter/Timer, as well as the Display Latch output polarity and the voltage comparator's noninverting-input source.

4.12

S2200/2400

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	$-55°C$ to $+125°C$
Operating Temperature	$0°C$ to $+70°C$
Operating Temperature (special request)	$-40°C$ to $+85°C$
Maximum Positive Voltage	$+18V$
Maximum Negative Voltage	$-0.3V$
Maximum Output Currents	(See Conditions p. 12)
I_{DD} Supply Current (depends upon output loads)	$+75mA$
Total Maximum Power Dissipation	$+700mW$

Electrical Characteristics
($V_{SS} = 0V$, $V_{GG} = +7.5V$ to $+10.0V$; $V_{DD} = +5V$*, $T_A = 0°C$ to $+70°C$, $f_{SYNC} = 125kHz$ to $225kHz$)

	Parameter	Min.	Typ.	Max.	Units	Conditions
INPUTS	K_0 thru K_7				V	For Touch-
	Low Level	0		$K_{REF} - 0.5$	V	Control and
	High Level	$K_{REF} + 0.5$		V_{GG}	V	Keyswitch
						Inputs
INPUT	K_{REF}	0		$2/3\ V_{GG}$	V	
INPUTS	K_0 thru K_7					For A/D
	For A/D Conversion	0		$2/3\ V_{GG}$	V	Conversion
	Logic Low Level			0.8	V	As Logic Inputs
	Logic High Level	3.5			V	
INPUT	$\overline{POR}$					
	Low Level ($\overline{POR}$ Reset)	0		1.0	V	
	High Level	$1/2\ V_{GG}$		V_{GG}	V	
	Power Fail					
	—No Interrupt			V_{GG}	V	
	—Interrupt	$V_{GG} + 1$			V	
INPUTS	ROMs, RUN					(Note 1)
	Low Level	0		0.8	V	
	High Level	3.5		V_{GG}	V	
INPUTS	D_0 thru D_7					
	Low Level	0		0.8	V	
	High Level	4.5		V_{GG}	V	
OUTPUTS	A_0 thru A_3					
	High Level	3.5		*V_{DD}	V	$I = -5mA$**
	Low Level	0		0.8	V	$I = +25mA$**
OUTPUTS	A_4 thru A_{12}					
	EXT, SYNC, & S					
	High Level	3.5		*V_{DD}	V	$I = -5mA$**
	Low Level	0		0.6	V	$I = +5mA$**
OUTPUTS	D_0 thru D_7					
	High Level	3.5		*V_{DD}	V	$I = -5mA$**
	Low Level	0		1.0	V	$I = +12mA$**
I_{GG}	Supply Current		28	50	mA	
I_{RAM}	RAM "Keep Alive" Current		20		μA/Bit	$V_{RAM} = 4.0V$

*V_{DD} may be connected to V_{GG} if single power supply operation is desired.
**At $V_{GG} \geq 8.5VDC$

Note 1: There is an internal pullup of $100\mu A$ nominal from each of these inputs to V_{GG}.

S2200A/S2400A Preliminary Electrical Specifications

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	$-55°C$ to $+125°C$
Operating Temperature	$0°C$ to $+70°C$
Operating Temperature (special request)	$-40°C$ to $+85°C$
Maximum Positive Voltage, V_{FD}, A_0-A_4, D_0-D_7	$+33V$
All other pins	$+18V$
Maximum Negative Voltage	$-0.3V$
Maximum Output Currents	(See Conditions below)
Source Current, any pin	$-10mA$
Total Average Power Dissipation	$+700mW$
Rate of Rise of V_{FD}	1.6V/msec.

Electrical Characteristics — Specifications noted only for parameters which change from the S2200/2400 to the S2200A/2400A

($V_{SS} = 0V$, $V_{GG} = 7.5 + 10.0V$, $V_{FD} = V_{GG} + 22V$, $T_A = 0°C$ to $+70°C$. $f_{SYNC} = 125kHz$ to $225kHz$)

|	Parameter	Min.	Typ.	Max.	Units	Conditions
OUTPUTS	D_0 thru D_7, A_0 thru A_4					
	High Level	-3.5			mA	$V_{OUT} = V_{FD} - 6V$**
	Low Level			0.6	V	$I = 250\mu A$**
OUTPUTS	A_5 thru A_{12}, EXT, SYNC, & STATUS					
	High Level	3.5			V	$I = -5mA$**
	Low Level			0.6	V	$I = +5mA$**
I_{GG}	Supply Current		28	50	mA	No Loads

**At $V_{GG} \geq 8.5VDC$

NOTE 1: The output buffers for lines A_5-A_{12} are supplied from V_{GG}.

NOTE 2: The high voltage parts, when biased with normal V_{FD}, are not TTL-compatible; when using external program ROM, it is necessary to interpose buffers.

NOTE 3: When applying power, V_{FD} must rise with or after V_{GG} at a rate not to exceed 1.6V/msec.

S2200A Typical Microwave/Standard Oven Application
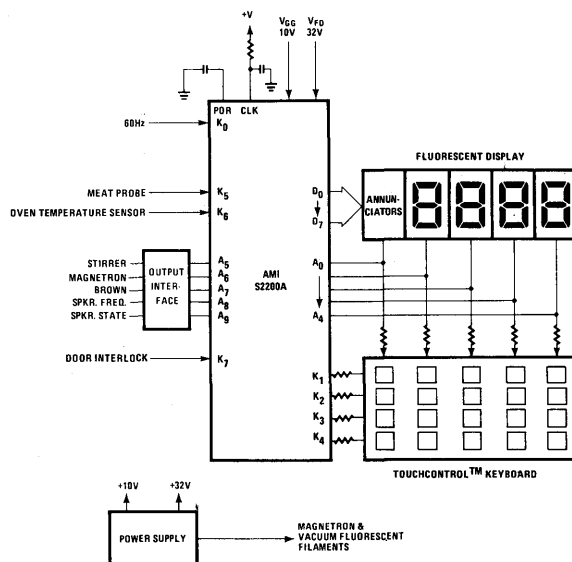
THE AMI S9900 MICROCOMPUTER SYSTEMS FAMILY

| PART NO.	DESCRIPTION	POWER SUPPLIES	INPUT/OUTPUT	PACKAGES
S9900	16-Bit Single Chip Microprocessor	+12V, ±5V	TTL	64 Pin
S9901	Programmable Systems Interface Circuit	+5V	TTL	40 Pin
S9902	Asynchronous Communications Controller (ACC)	+5V	TTL	18 Pin
S9903	Synchronous Communications Controller (SCC)	+5V	TTL	20 Pin
S9940	16-Bit Single Chip Microcomputer	+5V	TTL	18 Pin
S9980	16-Bit Single Chip Microcomputer	+5V	TTL	40 Pin
S9981	16-Bit Single Chip Microcomputer	+5V	TTL	40 Pin

AMI®

16-BIT MICROPROCESSOR

Features

- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability including Multiply and Divide
- ☐ Up to 65,536 Bytes of Memory
- ☐ 3.3MHz Speed
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 16 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ N-Channel Silicon-Gate Technology

General Description

The S9900 microprocessor is a single-chip 16-bit central processing unit (CPU) produced using N-channel silicon-gate MOS technology. The instruction set of the S9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. AMI provides a compatible set of MOS memory and support circuits to be used with an S9900 system. The system is fully supported by software and complete prototyping systems.

Block Diagram

Pin Configuration
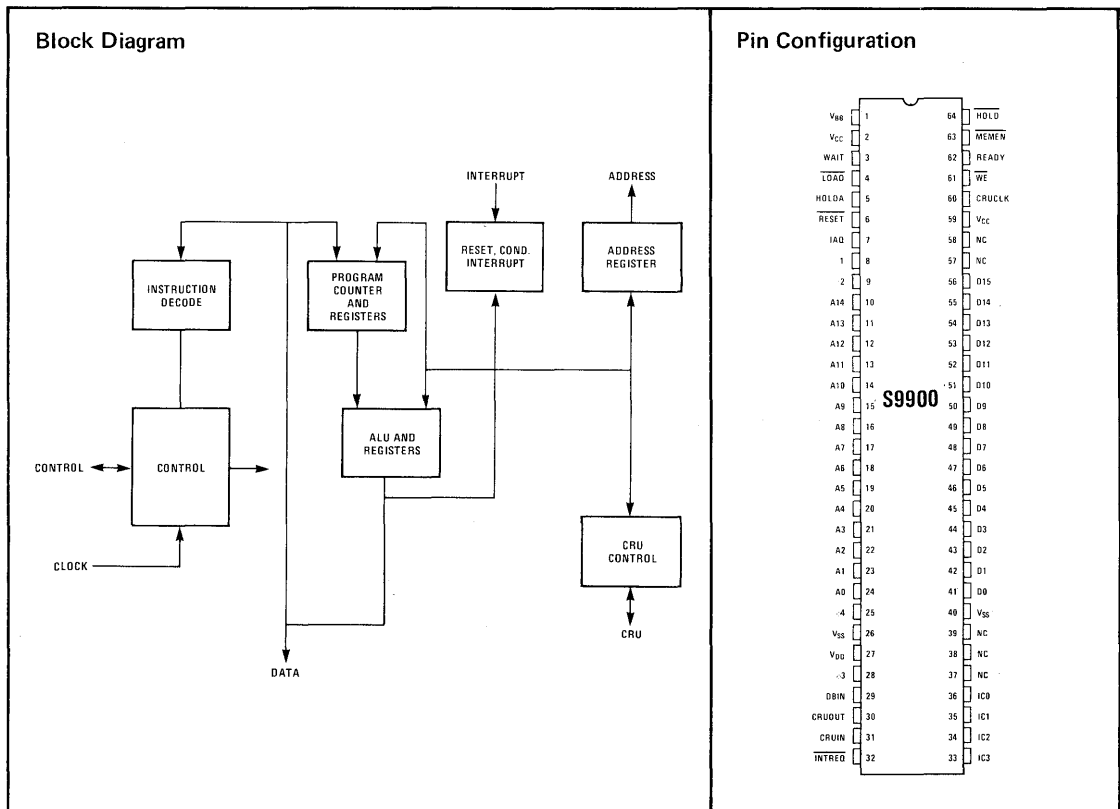
S9900

S9900 Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply Voltage, V_{CC} (See Note 1).. −0.3V to +20V
Supply Voltage, V_{DD} (See Note 1).. −0.3V to +20V
Supply Voltage, V_{SS} (See Note 1).. −0.3V to +20V
All Input Voltages (See Note 1).. −0.3V to +20V
Output Voltage (with Respect to V_{SS})... −2V to +7V
Continuous Power Dissipation .... +1.2W
Operating Free-Air Temperature Range... 0°C to +70°C
Storage Temperature Range.. −55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the most negative supply, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this section, voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage	−5.25	−5	−4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage (all inputs except clocks)	2.2	2.4	$V_{CC}+1$	V	
$V_{IH(\phi)}$	High-level clock input voltage	$V_{DD}-2$		V_{DD}	V	
V_{IL}	Low-level input voltage (all inputs except clocks)	−1	0.4	0.8	V	
$V_{IL(\phi)}$	Low-level clock input voltage	−0.3	0.3	0.6	V	
T_A	Operating free-air temperature	0		70	°C	

Timing Requirements Over Full Range of Recommended Operating Conditions (See Figures 1 and 2)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
$t_{c(\phi)}$	Clock cycle time	0.3	0.333	0.5	μs	
$t_{r(\phi)}$	Clock rise time	10	12		ns	
$t_{f(\phi)}$	Clock fall time	10	12		ns	
$t_{w(\phi)}$	Pulse width, any clock high	40	45	100	ns	
$t_{\phi1L, \phi2H}$	Delay time, clock 1 low to clock 2 high (time between clock pulses)	0	5		ns	
$t_{\phi2L, \phi3H}$	Delay time, clock 2 low to clock 3 high (time between clock pulses)	0	5		ns	
$t_{\phi3L, \phi4H}$	Delay time, clock 3 low to clock 4 high (time between clock pulses)	0	5		ns	
$t_{\phi4L, \phi1H}$	Delay time, clock 4 low to clock 1 high (time between clock pulses)	0	5		ns	
$t_{\phi1H, \phi2H}$	Delay time, clock 1 high to clock 2 high (time between leading edges)	70	80		ns	
$t_{\phi2H, \phi3H}$	Delay time, clock 2 high to clock 3 high (time between leading edges)	70	80		ns	
$t_{\phi3H, \phi4H}$	Delay time, clock 3 high to clock 4 high (time between leading edges)	70	80		ns	
$t_{\phi4H, \phi1H}$	Delay time, clock 4 high to clock 1 high (time between leading edges)	70	80		ns	
t_{su}	Data or control setup time before clock 1	30			ns	
t_h	Data hold time after clock 1	10			ns	

Electrical Characteristics Over Full Range of Recommended Operating Conditions (unless otherwise noted)

| Symbol	Parameter		Min.	Typ.†	Max.	Unit	Conditions
I_I	Input current	Data Bus during DBIN		±50	±100	μA	$V_I = V_{SS}$ to V_{CC}
		$\overline{WE}$, $\overline{MEMEN}$, DBIN, Address bus, Data bus during HOLDA		±50	±100		$V_I = V_{SS}$ to V_{CC}
		Clock*		±25	±75		$V_I = -0.3$ to $12.6V$
		Any other inputs		±1	±10		$V_I = V_{SS}$ to V_{CC}
V_{OH}	High-level output voltage		2.4		V_{CC}	V	$I_O = -0.4mA$
V_{OL}	Low-level output voltage				0.65	V	$I_O = 32.mA$
					0.50		$I_O = 2mA$
I_{BB}	Supply current from V_{BB}			0.1	1	mA	
I_{CC}	Supply current from V_{CC}			50	75	mA	
I_{DD}	Supply current from V_{DD}			25	45	mA	
C_i	Input capacitance (any inputs except clock and data bus)			10	15	pF	$V_{BB} = -5$, $f = 1MHz$, unmeasured pins at V_{SS}
$C_{i(\phi1)}$	Clock-1 input capacitance			100	150	pF	$V_{BB} = -5$, $f = 1MHz$, unmeasured pins at V_{SS}
$C_{i(\phi2)}$	Clock-2 input capacitance			150	200	pF	$V_{BB} = -5$, $f = 1MHz$ unmeasured pins at V_{SS}
$C_{i(\phi3)}$	Clock-3 input capacitance			100	150	pF	$V_{BB} = -5$, $f = 1MHz$, unmeasured pins at V_{SS}
$C_{i(\phi4)}$	Clock-4 input capacitance			100	150	pF	$V_{BB} = -5$, $f = 1MHz$, unmeasured pins at V_{SS}
C_{DB}	Data bus capacitance			15	25	pF	$V_{BB} = -5$, $f = 1MHz$, unmeasured pins at V_{SS}
C_o	Output capacitance (any output except data bus)			10	15	pF	$V_{BB} = -5$, $f = 1MHz$, unmeasured pins at V_{SS}

† All typical values are at $T_A = 25°C$ and nominal voltages.
*D.C. Component of Operating Clock.

Switching Characteristics Over Full Range of Recommended Operating Conditions (See Figure 2)
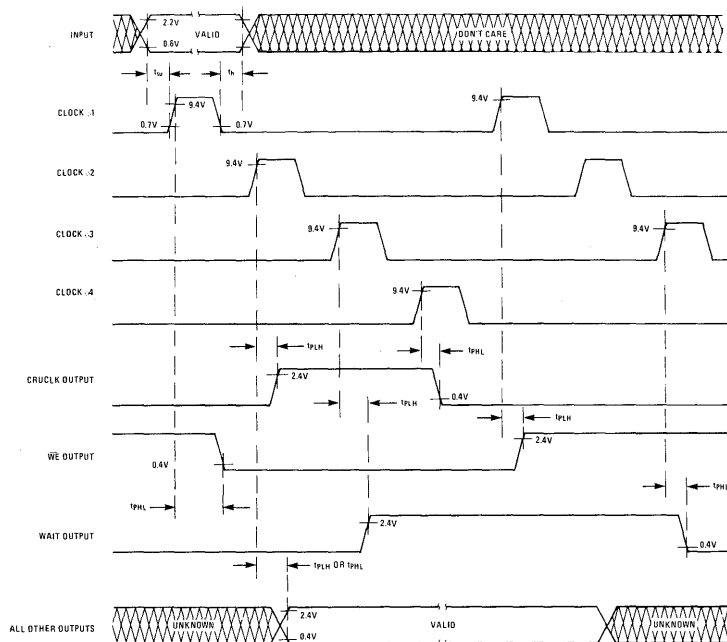
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PLH} or t_{PHL}	Propagation delay time, clocks to outputs		20	40	ns	$C_L = 200pF$

Figure 1. Clock Timing
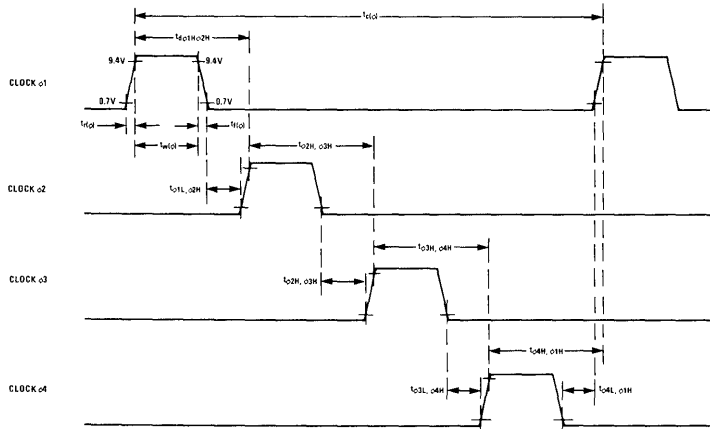
NOTE: All timing and voltage levels shown on $\phi1$ applies to $\phi2$, $\phi3$, and $\phi4$ in the same manner.

Figure 2. Signal Timing

†The number of cycles over which input/output data must/will remain valid can be determined from the number of wait states required for memory access. Note that in all cases data should not change during $\phi1$.

Pin Description

Table 1 defines the S9900 pin assignments and describes the function of each pin.

Table 1. S9900 Pin Assignments and Functions

Signature	Pin	I/O	Description
			ADDRESS BUS
A0 (MSB)	24	OUT	A0 through A14 comprise the address bus. This 3-state bus provides the memory-address vec-
A1	23	OUT	tor to the external-memory system when $\overline{\text{MEMEN}}$ is active and I/O-bit addresses and external-
A2	22	OUT	instruction addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. The address bus assumes the
A3	21	OUT	high-impedance state when HOLDA is active.
A4	20	OUT	
A5	19	OUT	
A6	18	OUT	
A7	17	OUT	
A8	16	OUT	
A9	15	OUT	
A10	14	OUT	
A11	13	OUT	
A12	12	OUT	
A13	11	OUT	
A14 (LSB)	10	OUT	
			DATA BUS
D0 (MSB)	41	I/O	D0 through D15 comprise the bidirectional 3-state data bus. This bus transfers memory data
D1	42	I/O	to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is
D2	43	I/O	active. The data bus assumes the high-impedance state when HOLDA is active.
D3	44	I/O	
D4	45	I/O	
D5	46	I/O	
D6	47	I/O	
D7	48	I/O	
D8	49	I/O	
D9	50	I/O	
D10	51	I/O	
D11	52	I/O	
D12	53	I/O	
D13	54	I/O	
D14	55	I/O	
D15 (LSB)	56	I/O	
			POWER SUPPLIES
V_{BB}	1		Supply voltage (–5V NOM)
V_{CC}	2,59		Supply voltage (5V NOM). Pins 2 and 59 must be connected in parallel.
V_{DD}	27		Supply volage (12V NOM)
V_{SS}	26,40		Ground reference. Pins 26 and 40 must be connected in parallel.
			CLOCKS
$\phi1$	8	IN	Phase-1 clock
$\phi2$	9	IN	Phase-2 clock
$\phi3$	28	IN	Phase-3 clock
$\phi4$	25	IN	Phase-4 clock

Table 1. S9900 Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
			BUS CONTROL
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the S9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains low in all other cases except when HOLDA is active.
$\overline{\text{MEMEN}}$	63	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	61	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the S9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0 through A2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	Interrupt request. When active (low), $\overline{\text{INTREQ}}$ indicates that an external-interrupt is requested. If $\overline{\text{INTREQ}}$ is active, the processor loads the data on the interrupt-code-input lines IC0 through IC3 into the internal interrupt-code-storage register. The code is compared to the interrupt mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15) the S9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. $\overline{\text{INTREQ}}$ should remain active and the processor will continue to sample IC0 through IC3 until the program enables a sufficiently low priority to accept the request interrupt.
IC0 (MSB) IC1 IC2 IC3 (LSB)	36 35 34 33	IN IN IN IN	Interrupt codes. IC0 is the MSB of the interrupt code, which is sampled when $\overline{\text{INTREQ}}$ is active. When IC0 through IC3 are LLLH, the highest external-priority interrupt is being requested and when HHHH, the lowest-priority interrupt is being requested.
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9900 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.

*If the cycle following the present memory cycle is also a memory cycle, it, too, is completed before the S9900 enters the hold state. The maximum number of consecutive memory cycles is three.

Table 1. S9900 Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{WE}$, $\overline{MEMEN}$, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the S9900 has entered a wait state because of a not-ready condition from memory.
			TIMING AND CONTROL
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9900 is acquiring an instruction. IAQ can be used to detect illegal op codes.
$\overline{LOAD}$	4	IN	Load. When active (low), $\overline{LOAD}$ causes the S9900 to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. $\overline{LOAD}$ will also terminate an idle state. If $\overline{LOAD}$ is active during the time $\overline{RESET}$ is released, then the $\overline{LOAD}$ trap will occur after the $\overline{RESET}$ fuction is completed. $\overline{LOAD}$ should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold-start ROM loaders. Additionally, front-panel routines can be implemented using CRU bits as front-panel-interface signals and software-control routines to control the panel operations.
$\overline{RESET}$	6	IN	Reset. When active (low), $\overline{RESET}$ causes the processor to be reset and inhibits $\overline{WE}$ and CRUCLK. When $\overline{RESET}$ is released, the S9900 then initiates a level-zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. $\overline{RESET}$ will also terminate an idle state. $\overline{RESET}$ must be held active for a minimum of three clock cycles.

*If the cycle following the present memory cycle is also a memory cycle it, too, is completed before the S9900 enters the hold state. The maximum number of consecutive memory cycles is three.

Timing

Memory

A basic memory read and write cycle is shown in Figure 3. The read cycle is shown with no wait states and the write cycle is shown with one wait state.

$\overline{MEMEN}$ goes active (low) during each memory cycle. At the same time that $\overline{MEMEN}$ is active, the memory address appears on the address bus bits A0 through A14. If the cycle is a memory-read-only cycle, DBIN will go active (high) at the same time $\overline{MEMEN}$ and A0 through A14 become valid. The memory-write signal $\overline{WE}$ will remain inactive (high) during a read cycle. If the read cycle is also an instruction acquisition cycle, IAQ will go active (high) during the cycle.

The READY signal, which allows extended memory cycles, is shown high during $\phi1$ of the second clock cycle of the read operation. This indicates to the S9900 that memory-read data will be valid during $\phi1$ of the next clock cycle. If READY is low during $\phi1$, then the S9900 enters a wait state suspending internal operation until a READY is sensed during a subsequent $\phi1$. The memory read data is then sampled by the S9900 during the next $\phi1$, which completes the memory-read cycle.

At the end of the read cycle, $\overline{MEMEN}$ and DBIN go inactive (high and low, respectively). The address bus may also change at this time; however, the data bus remains in the input mode for one clock cycle after the read cycle.

S9900

A write cycle is similar to the read cycle with the exception that $\overline{WE}$ goes active (low) as shown and valid write data appears on the data bus at the same time the address appears. The write cycle is shown as an example of a one-wait-state memory cycle. READY is low during $\phi1$ resulting in the WAIT signal shown.

Hold

Other interfaces may utilize the S9900 memory bus by using the hold operation (illustrated in Figure 4) of the S9900. When $\overline{HOLD}$ is active (low), the S9900 enters the hold state at the next available non-memory cycle. Considering that there can be a maximum of three consecutive memory cycles, the maximum delay between $\overline{HOLD}$ going active to HOLDA going active (high) could be $t_{c(\phi)}$ (for setup) + $(6 + 3W)\, t_{c(\phi)} + t_{c(\phi)}$ (delay for HOLDA), where W is the number of wait states per memory cycle and $t_{c(\phi)}$ is the clock cycle time. When the S9900 has entered the hold state, HOLDA goes active (high) and A0 through A15, D0 through D15 DBIN, $\overline{MEMEN}$, and $\overline{WE}$ go into a high-impedance state to allow other devices to use the memory buses. When $\overline{HOLD}$ goes inactive (high), the S9900 resumes processing as shown. If hold occurs during a CRU operation, the S9900 uses an extra clock cycle (after the removal of the $\overline{HOLD}$ signal) to reassert the CRU address providing the normal setup times for the CRU bit transfer that was interrupted.

CRU

CRU interface timing is shown in Figure 5. The timing for transferring two bits out and one bit in is shown. These transfers would occur during the execution of a CRU instruction. The other cycles of the instruction execution are not illustrated. To output a CRU bit, the CRU-bit address is placed on the address bus A0 through A14 and the actual bit data on CRUOUT. During the second clock cycle a CRU pulse is supplied by CRUCLK. This process is repeated until the number of bits specified by the instruction are completed.

The CRU input operation is similar in that the bit address appears on A0 through A14. During the subsequent cycle the S9900 accepts the bit input data as shown. No CRUCLK pulses occur during a CRU input operation.

Figure 3. S9900 Memory Bus Timing

MEMORY READ CYCLE WITH NO WAITS   MEMORY WRITE CYCLE WITH ONE WAIT
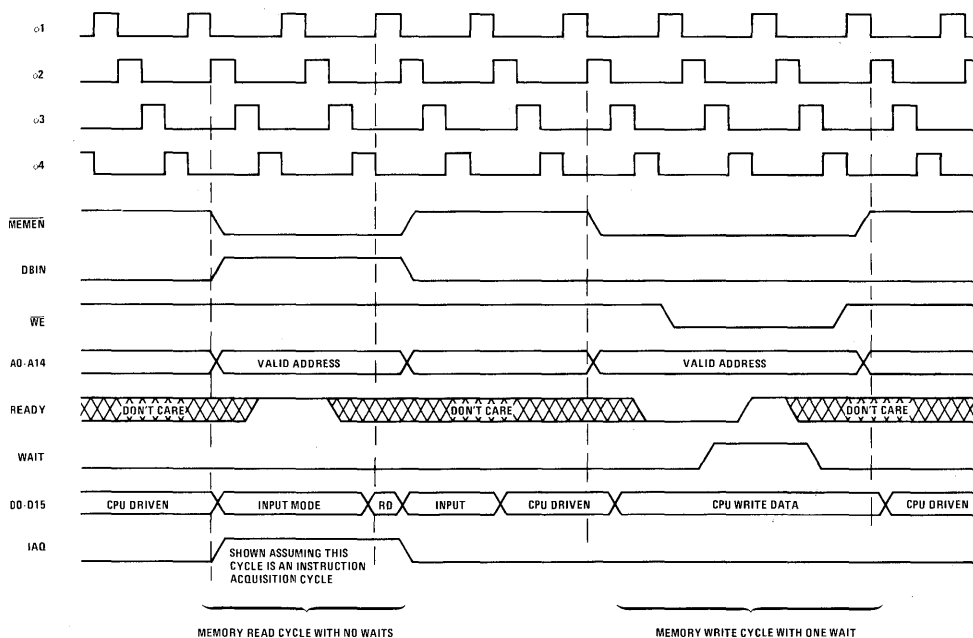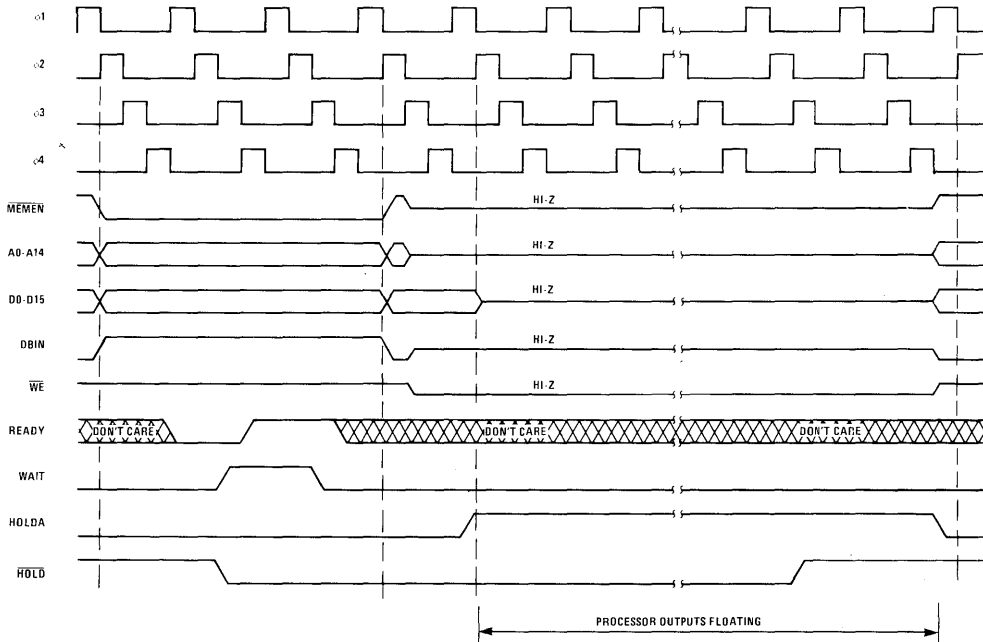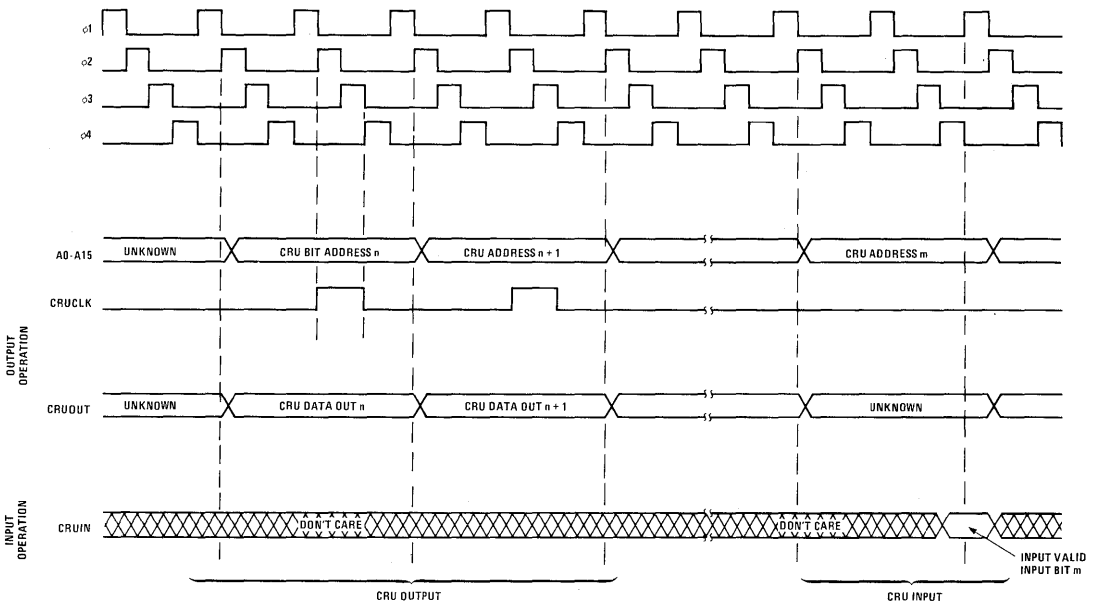
RD = READ DATA

Figure 4. S9900 Hold Timing

Figure 5. S9900 CRU Interface Timing

Architecture

The S9900 operation is shown in Figure 6 and its architecture illustrated by Figure 7.
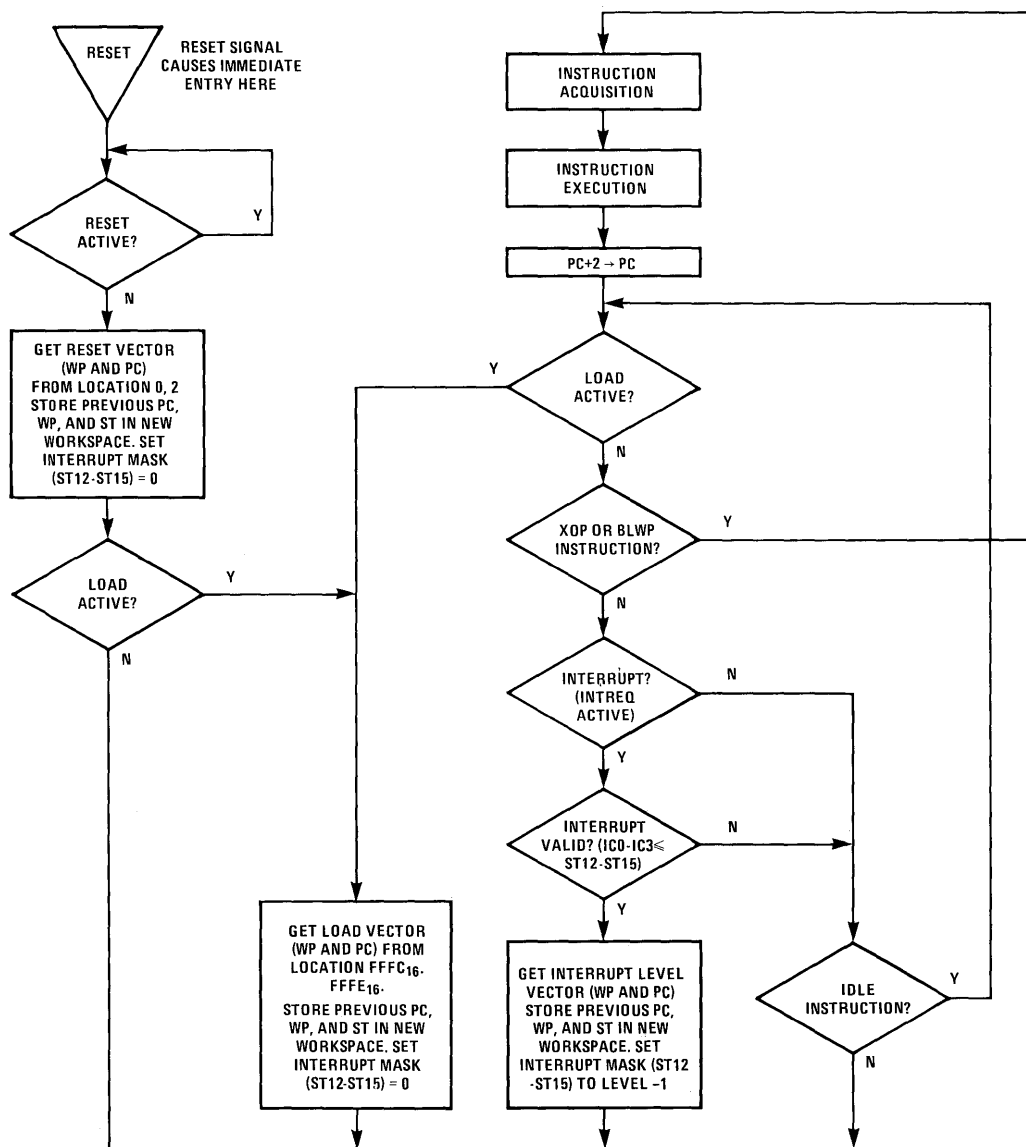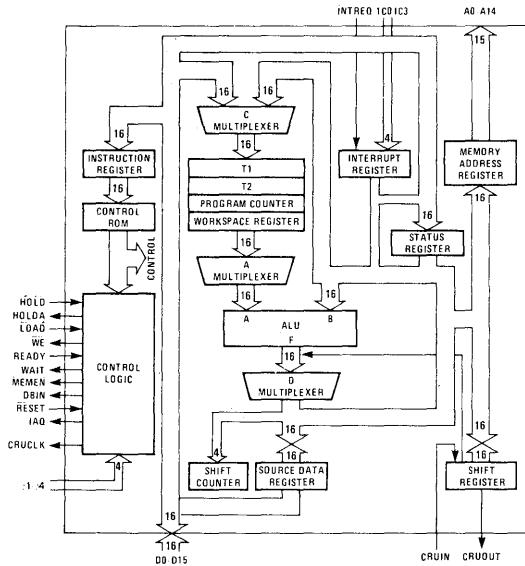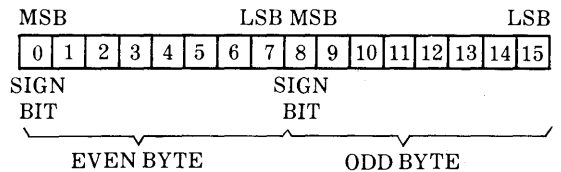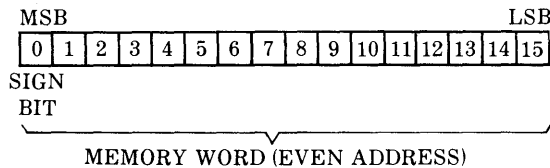
Figure 6. S9900 CPU Flow Chart

Figure 7. Architecture
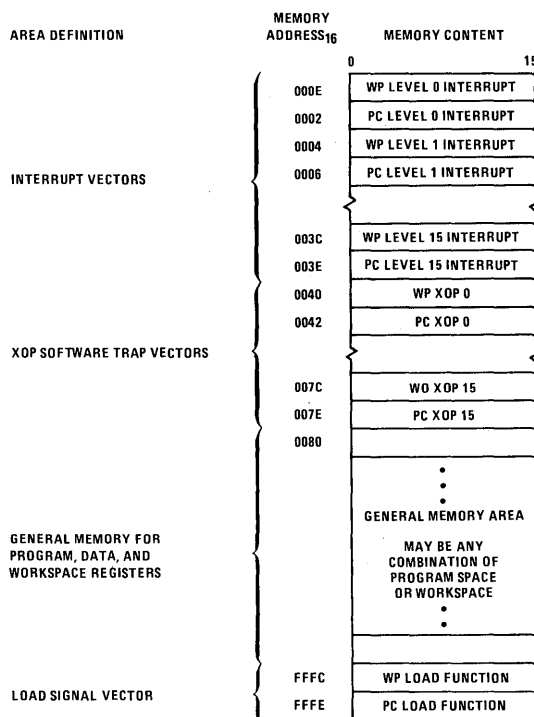

Registers and Memory

The S9900 employs an advanced memory-to-memory architecture. Blocks of memory designated as workspace replace internal-hardware registers with program-data registers. The memory word of the S9900 is 16 bits long. Each word is also defined as 2 bytes of 8 bits. The instruction set of the S9900 allows both word and byte operands. Thus, all memory locations are on even address boundaries and byte instructions can address either the even or odd byte. The memory space is 65,536 bytes or 32,768 words. The word and byte formats are shown below.

```
MSB                                              LSB
 0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15
SIGN
BIT
_____/
         MEMORY WORD (EVEN ADDRESS)
```

```
MSB              LSB MSB                    LSB
 0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15
SIGN                    SIGN
BIT                     BIT
_____/   _____/
    EVEN BYTE              ODD BYTE
```

The S9900 memory map is shown in Figure 8. The first 32 words are used for interrupt trap vectors. The next contiguous block of 32 memory words is used by the extended operation (XOP) instruction for trap vectors. The last two memory words, $FFFC_{16}$ and $FFFE_{16}$, are used for the trap vector of the LOAD signal. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory.

Figure 8. Memory Map

	AREA DEFINITION	MEMORY ADDRESS$_{16}$	MEMORY CONTENT

| AREA DEFINITION	MEMORY ADDRESS$_{16}$	MEMORY CONTENT (0 ... 15)
INTERRUPT VECTORS	000E	WP LEVEL 0 INTERRUPT
	0002	PC LEVEL 0 INTERRUPT
	0004	WP LEVEL 1 INTERRUPT
	0006	PC LEVEL 1 INTERRUPT
	003C	WP LEVEL 15 INTERRUPT
	003E	PC LEVEL 15 INTERRUPT
XOP SOFTWARE TRAP VECTORS	0040	WP XOP 0
	0042	PC XOP 0
	007C	WO XOP 15
	007E	PC XOP 15
	0080	
GENERAL MEMORY FOR PROGRAM, DATA, AND WORKSPACE REGISTERS		GENERAL MEMORY AREA MAY BE ANY COMBINATION OF PROGRAM SPACE OR WORKSPACE
LOAD SIGNAL VECTOR	FFFC	WP LOAD FUNCTION
	FFFE	PC LOAD FUNCTION

NOTE: 1 interrupt level 0 is reserved for RESET.

Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the present state of the processor. The workspace pointer (WP) contains the address of the first word in the currently active set of workspace registers.

A workspace-register file occupies 16 contiguous memory words in the general memory area (see Figure 2). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or index registers. During instruction execution, the processor addresses any register in the workspace by adding the register number to the contents of the workspace pointer and initiating a memory request for the word. The relation-

ship between the workspace pointer and its corresponding workspace is shown below.

GENERAL MEMORY		S9900
PROGRAM A		PC (A)
WORKSPACE REGISTER 0		WP (A)
WORKSPACE A		ST (A)
WORKSPACE REGISTER 15		
PROGRAM B		
WORKSPACE B		
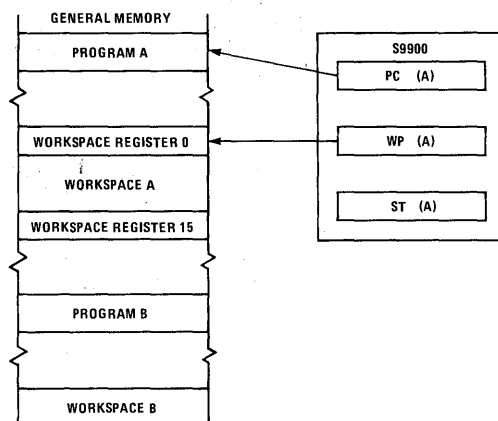
The workspace concept is particularly valuable during operations that require a context switch, which is a change from one program environment to another (as in the case of an interrupt) or to a subroutine. Such an operation, using a conventional multi-register arrangement, requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the program counter, status register, and workspace pointer, the S9900 accomplishes a complete context switch with only three store cycles and three fetch cycles. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine. A corresponding time saving occurs when the original context is restored. Instructions in the S9900 that result in a context switch include:

1. Branch and Load Workspace Pointer (BLWP)
2. Return from Subroutine (RTWP)
3. Extended Operation (XOP).

Device interrupts, $\overline{\text{RESET}}$, and $\overline{\text{LOAD}}$ also cause a context switch by forcing the processor to trap to a service subroutine.

Interrupts

The S9900 employs 16 interrupt levels with the highest priority level 0 and lowest level 15. Level 0 is reserved for the $\overline{\text{RESET}}$ function and all other levels may be used for external devices. The external levels may also be shared by several device interrupts, depending upon system requirements.

The S9900 continuously compares the interrupt code (IC0 through IC3) with the interrupt mask contained in status-register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the processor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. The, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15, respectively, of the new workspace. The S9900 then forces the interrupt mask to a value that is one less than the level of the interrupt being serviced, except for the level-zero interrupt, which loads zero into the mask. This allows only interrupts of higher priority to interrupt a service routine. The processor also inhibits interrupts until the first instruction of the service routine has been executed to preserve program linkage should a higher priority interrupt occur. All interrupt requests should remain active until recognized by the processor in the

device-service routine. The individual service routines must reset the interrupt requests before the routine is complete.

If a higher priority interrupt occurs, a second context switch occurs to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower-priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters. The interrupt-vector locations, device assignment, enabling-mask value, and the interrupt code are shown in Table 2.

Input/Output

The S9900 utilizes a versatile direct command-driven I/O interface designated as the communications-register unit (CRU). The CRU provides up to 4096 directly addressable input bits and 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields of from 1 to 16 bits. The S9900 employs three dedicated I/O pins (CRUIN, CRUOUT, and CRUCLK) and 12 bits (A3 through A14) of the address bus to interface with the CRU system. The processor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move between memory and CRU data fields.

Single-Bit CRU Operations

The S9900 performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the S9900 develops a CRU-bit address and places it on the address bus, A3 to A14.

For the two output operations (SBO and SBZ), the processor also generates a CRUCLK pulse, indicating an output operation to the CRU device, and places bit 7 of the instruction word on the CRUOUT line to accomplish the specified operation (bit 7 is a one for SBO and a zero for SBZ). A test-bit instruction transfers the addressed CRU bit from the CRUIN input line to bit 2 of the status register (EQUAL).

The S9900 develops a CRU-bit address for the single-bit operations from the CRU-base address contained in workspace register 12 and the signed displacement count contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from W12 is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 9 illustrates the development of a single-bit CRU address.

Table 2. Interrupt Level Data

Interrupt Level	Vector Location (Memory Address In Hex)	Device Assignment	Interrupt Mask Values to Enable Respective Interrupts (ST12 through ST15)	Interrupt Codes IC0 through IC3
(Highest priority) 0	00	Reset	0 through F*	0000
1	04	External device	1 through F	0001
2	08		2 through F	0010
3	0C		3 through F	0011
4	10		4 through F	0100
5	14		5 through F	0101
6	18		6 through F	0110
7	1C		7 through F	0111
8	20		8 through F	1000
9	24		9 through F	1001
10	28		A through F	1010
11	2C		B through F	1011
12	30		C through F	1100
13	34		D through F	1101
14	38		E and F	1110
(Lowest priority) 15	3C	External device	F only	1111

*Level 0 can not be disabled.

Figure 9. S9900 Single-Bit CRU Address Development
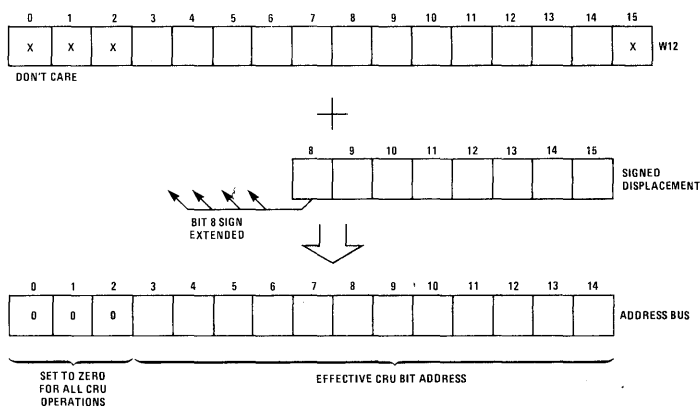
Multiple-Bit CRU Operations

The S9900 performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in Figure 10. Although the figure illustrates a full 16-bit transfer operation, any number of bits from 1 through 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves eight or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves nine or more bits, those bits come from the right-justified field within the whole memory word. When transferred to the CRU interface, each suc-cessive bit receives an address that is sequentially greater than the address for the previous bit. This addressing mechanism results in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressd bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves a byte or less transfer, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves from nine to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to zero.

When the input from CRU device is complete, the first bit from the CRU is the least-significant-bit position in the memory word or byte.

Figure 10. S9900 LDCR/STCR Data Transfers
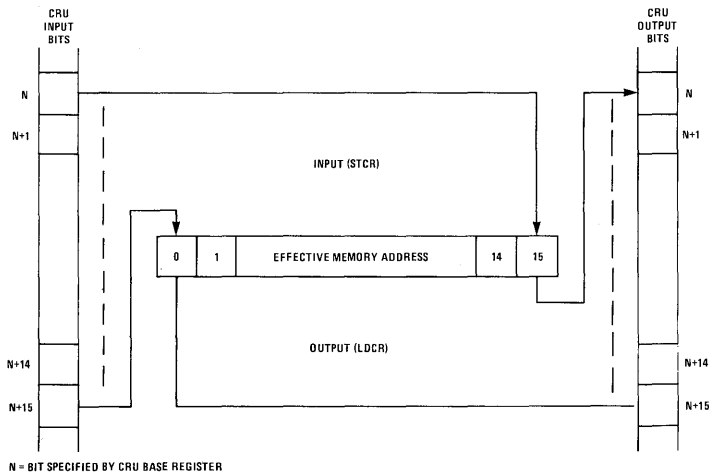
S9900 Instruction Set

Definition

Each S9900 instruction performs one of the following operations:

- [ ] Arithmetic, logical, comparison, or manipulation operations on data
- [ ] Loading or storage of internal registers (program counter, workspace pointer, or status)
- [ ] Data transfer between memory and external devices via the CRU
- [ ] Control functions.

Addressing Modes

S9900 instructions contain a variety of available modes for addressing random-memory data (e.g., program parameters and flags), or formatted memory data (character strings, data lists, etc.). The following figures graphically describe the derivation of the effective address for each addressing mode. The applicability of addressing modes to particular instructions is described later along with the description of the operations performed by the instruction. The symbols following the names of the addressing modes [R, *R, *R + ,@LABEL, or @TABLE (R)] are the general forms used by S9900 assemblers to select the addressing mode for register R.

Workspace Register Addressing R

Workspace Register R contains the operand.
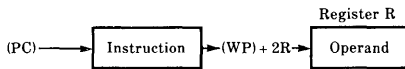
Workspace Register Indirect Addressing *R

Workspace Register R contains the address of the operand.
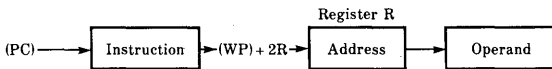
Workspace Register Indirect Auto Increment Addressing *R +

Workspace Register R contains the address of the operand. After acquiring the operand, the contents of workspace Register R are incremented.
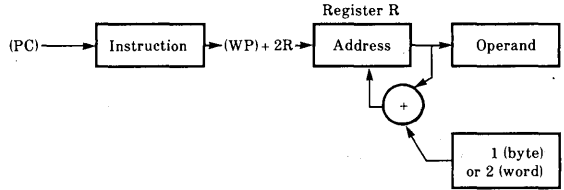
Symbolic (Direct) Addressing @LABEL

The word following the instruction contains the address of the operand.
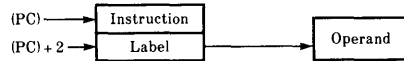
Indexed Addressing @TABLE (R)

The word following the instruction contains the base address. Workspace Register R contains the index value. The sum of the base address and the index value results in the effective address of the operand.

Immediate Addressing

The word following the instruction contains the operand.

```
(PC) ──────▶ | Instruction |
(PC)+2 ────▶ |   Operand    |
```

Program Counter Relative Addressing

The 8-bit signed displacement in the right byte (bits 8 through 15) of the instruction is multiplied by 2 and added to the updated contents of the program counter. The result is placed in the PC.

```
                    Jump Instruction
Program Counter    | OP CODE | DISP |──▶ 2 · DISP
| Address |        | next memory word |
                                        (+)
```

CRU Relative Addressing

The 8-bit signed displacement in the right byte of the instruction is added to the CRU base address (bits 3 through 14 of the workspace Register 12). The result is the CRU address of the selected CRU bit.

```
            Instruction
(PC)──────▶ | OP CODE | DISP |
            0      7 8     15
                                   CRU Bit
                              (+)──▶ Address
            Register 12
(WP)+2·12─▶ | | CRU Base Add | |
            0  2 3         14 15
```
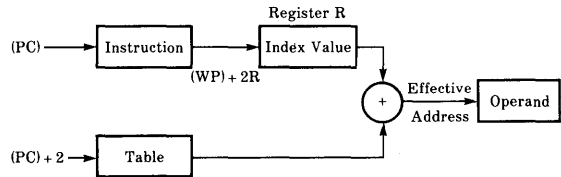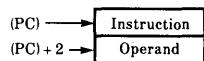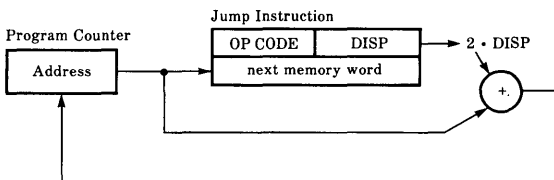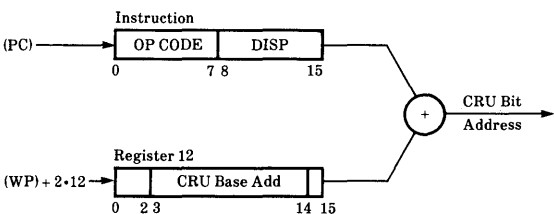
Terms and Definitions

The following terms are used in describing the instructions of the S9900:

TERM	DEFINITION
B	Byte indicator (1 = byte, 0 = word)
C	Bit count
D	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right most) bit of (n)
MSB(n)	Most significant (left most) bit of (n)
N	Don't care
PC	Program counter
Result	Result of operation performed by instruction
S	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination address modifier
T_S	Source address modifier
W	Workspace register
WRn	Workspace register n
(n)	Contents of n
a→b	a is transferred to b
|n|	Absolute value of n
+	Arithmetic addition
−	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
⊕	Logical exclusive OR
$\overline{n}$	Logical complement of n

Status Register

The status register contains the interrupt mask level and information pertaining to the instruction operation.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ST0	ST1	ST2	ST3	ST4	ST5	ST6		not used (=0)				ST12	ST13	ST14	ST15
L>	A>	=	C	O	P	X							Interrupt Mask		

Bit	Name	Instruction	Condition to Set Bit to 1
ST0	LOGICAL GREATER THAN	C, CB	If MSB(SA) = 1 and MSB(DA) = 0, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(W) = 1 and MSB of IOP = 0, or if MSB(W) = MSB of IOP and MSB of [IOP-(W)] = 1
		ABS	If (SA) ≠ 0
		All Others	If result ≠ 0
ST1	ARITHMETIC GREATER THAN	C, CB	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(W) = 0 and MSB of IOP = 1, or if MSB(W) = MSB of IOP and MSB of [IOP-(W)] = 1
		ABS	If MSB(SA) = 0 and (SA) ≠ 0
		All Others	If MSB of result = 0 and result ≠ 0
ST2	EQUAL	C, CB	If (SA) = (DA)
		CI	If (W) = IOP
		COC	If (SA) and $(\overline{DA})$ = 0
		CZC	If (SA) and (DA) = 0
		TB	If CRUIN = 1
		ABS	If (SA) = 0
		All Others	If result = 0
ST3	CARRY	A, AB, ABS, AI, DEC, DECT, INC, INCT, NEG S, SB	If CARRY OUT = 1
		SLA, SRA, SRC, SRL	If last bit shifted out = 1
ST4	OVERFLOW	A, AB	If MSB(SA) = MSB(DA) and MSB of result ≠ MSB(DA)
		AI	If MSB(W) = MSB of IOP and MSB of result ≠ MSB(W)
		S, SB	If MSB(SA) ≠ MSB(DA) and MSB of result ≠ MSB(DA)
		DEC, DECT	If MSB(SA) = 1 and MSB of result = 0
		INC, INCT	If MSB(SA) = 0 and MSB of result = 1
		SLA	If MSB changes during shift
		DIV	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 0
		ABS, NEG	If (SA) = 8000_{16}
ST5	PARITY	CB, MOVB	If (SA) has odd number of 1's
		LDCR, STCR	If $1 \leqslant C \leqslant 8$ and (SA) has odd number of 1's
		AB, SB, SOCB, SZCB	If result has odd number of 1's
ST6	XOP	XOP	If XOP instruction is executed
ST12-ST15	INTERRUPT MASK	LIMI	If corresponding bit of IOP is 1
		RTWP	If corresponding bit of WR15 is 1

Instructions

Dual Operand Instructions with Multiple Addressing Modes for Source and Destination Operand

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

General format:

OP CODE	B	T_D	D	T_S	S

If B = 1 the operands are bytes and the operand addresses are byte addresses. If B = 0 the operands are words and the operand addresses are word addresses.

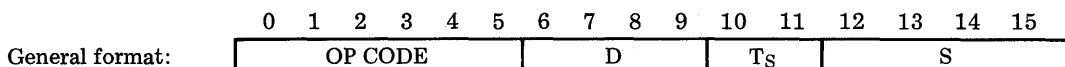The addressing mode for each operand is determined by the T field of that operand.

T_S or T_D	S or D	Addressing Mode	Notes
00	0, 1, . . . 15	Workspace register	1
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	4
10	1, 2, . . . 15	Indexed	2,4
11	0, 1, . . . 15	Workspace register indirect auto-increment	3

Notes:
1. When a workspace register is the operand of a byte instruction (bit 3 = 1), the left byte (bits 0 through 7) is the operand and the right byte (bits 8 through 15) is unchanged.
2. Workspace register 0 may not be used for indexing.
3. The workspace register is incremented by 1 for byte instructions (bit 3 = 1) and is incremented by 2 for word instructions (bit 3 = 0).
4. When $T_S = T_D = 10$, two words are required in addition to the instruction word. The first word is the source operand base address and the second word is the destination operand base address.

MNEMONIC	OP CODE 0 1 2	B 3	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
A	1 0 1	0	Add	Yes	0-4	$(SA)+(DA) \rightarrow (DA)$
AB	1 0 1	1	Add bytes	Yes	0-5	$(SA)+(DA) \rightarrow (DA)$
C	1 0 0	0	Compare	No	0-2	Compare (SA) to (DA) and set appropriate status bits
CB	1 0 0	1	Compare bytes	No	0-2,5	Compare (SA) to (DA) and set appropriate status bits
S	0 1 1	0	Subtract	Yes	0-4	$(DA) - (SA) \rightarrow (DA)$
SB	0 1 1	1	Subtract bytes	Yes	0-5	$(DA) - (SA) \rightarrow (DA)$
SOC	1 1 1	0	Set ones corresponding	Yes	0-2	$(DA) \text{ OR } (SA) \rightarrow (DA)$
SOCB	1 1 1	1	Set ones corresponding bytes	Yes	0-2,5	$(DA) \text{ OR } (SA) \rightarrow (DA)$
SZC	0 1 0	0	Set zeroes corresponding	Yes	0-2	$(DA) \text{ AND } (\overline{SA}) \rightarrow (DA)$
SZCB	0 1 0	1	Set zeroes corresponding bytes	Yes	0-2,5	$(DA) \text{ AND } (\overline{SA}) \rightarrow (DA)$
MOV	1 1 0	0	Move	Yes	0-2	$(SA) \rightarrow (DA)$
MOVB	1 1 0	1	Move bytes	Yes	0-2,5	$(SA) \rightarrow (DA)$

Dual Operand Instructions with Multiple Addressing Modes for the Source Operand and Workspace Register Addressing for the Destination

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

General format:

OP CODE						D			T_S		S				

The addressing mode for the source operand is determined by the T_S field.

T_S	S	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	
10	1, 2, . . . 15	Indexed	1
11	0, 1, . . . 15	Workspace register indirect auto increment	2

NOTES: 1. Workspace register 0 may not be used for indexing.
2. The workspace register is incremented by 2.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
COC	0 0 1 0 0 0	Compare ones corresponding	No	2	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set ST2.
CZC	0 0 1 0 0 1	Compare zeros corresponding	No	2	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set ST2.
XOR	0 0 1 0 1 0	Exclusive OR	Yes	0-2	(D)$\oplus$(SA)$\to$(D)
MPY	0 0 1 1 1 0	Multiply	No		Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D+1 (least significant). If WR15 is D, the next word in memory after WR15 will be used for the least significant half of the product.
DIV	0 0 1 1 1 1	Divide	No	4	If unsigned (SA) is less than or equal to unsigned (D), perform no operation and set ST4. Otherwise, divide unsigned (D) and (D+1) by unsigned (SA). Quotient $\to$ (D), remainder $\to$ (D+1). If D = 15, the next word in memory after WR15 will be used for the remainder.

Extended Operation (XOP) Instruction

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
General format:	0	0	1	0	1	1		D			T_S			S		

The T_S and S fields provide multiple mode addressing capability for the source operand. When the XOP is executed, ST6 is set and the following transfers occur:

$(40_{16} + 4D) \rightarrow (WP)$
$(42_{16} + 4D) \rightarrow (PC)$
SA $\rightarrow$ (new WR11)
(old WP) $\rightarrow$ (new WR13)
(old PC) $\rightarrow$ (new WR14)
(old ST) $\rightarrow$ (new WR15)

The S9900 does not test interrupt requests ($\overline{\text{INTREQ}}$) upon completion of the XOP instruction.

Single Operand Instructions

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
General format:					OP CODE						T_S			S		

The T_S and S fields provide multiple mode addressing capability for the source operand.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
B	0 0 0 0 0 1 0 0 0 1	Branch	No	—	SA→(PC)
BL	0 0 0 0 0 1 1 0 1 0	Branch and link	No	—	(PC)→(WR11); SA→(PC)
BLWP	0 0 0 0 0 1 0 0 0 0	Branch and load workspace pointer	No	—	(SA)→(WP); (SA+2)→(PC); (old WP)→(new WR13); (old PC)→(new WR14); (old ST)→(new WR15); the interrupt input ($\overline{\text{INTREQ}}$) is not tested upon completion of the BLWP instruction.
CLR	0 0 0 0 0 1 0 0 1 1	Clear operand	No	—	0→(SA)
SETO	0 0 0 0 0 1 1 1 0 0	Set to ones	No	—	$FFFF_{16}$→(SA)
INV	0 0 0 0 0 1 0 1 0 1	Invert	Yes	0-2	$(\overline{SA})$→(SA)
NEG	0 0 0 0 0 1 0 1 0 0	Negate	Yes	0-4	−(SA)→(SA)
ABS	0 0 0 0 0 1 1 1 0 1	Absolute value*	No	0-4	‖(SA)‖→(SA)
SWPB	0 0 0 0 0 1 1 0 1 1	Swap bytes	No	—	(SA), bits 9 thru 7→(SA), bits 8 thru 15; (SA), bits 8 thru 15 → (SA), bits 0 thru 7.
INC	0 0 0 0 0 1 0 1 1 0	Increment	Yes	0-4	(SA)+1→(SA)
INCT	0 0 0 0 0 1 0 1 1 1	Increment by two	Yes	0-4	(SA)+2→(SA)
DEC	0 0 0 0 0 1 1 0 0 0	Decrement	Yes	0-4	(SA)−1→(SA)
DECT	0 0 0 0 0 1 1 0 0 1	Decrement by two	Yes	0-4	(SA)−2→(SA)
X†	0 0 0 0 0 1 0 0 1 0	Execute	No	—	Execute the instruction at SA.

*Operand is compared to zero for status bit.
†If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the S9900 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

CRU Multiple-Bit Instructions

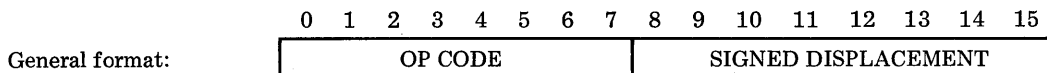|	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
General format:	OP CODE							C			T_S		S			
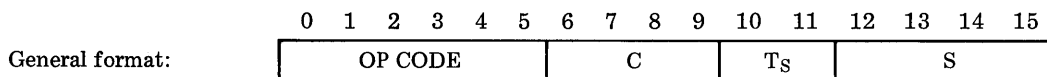
The C field specifies the number of bits to be transferred. If C = 0, 16 bits will be transferred. The CRU base register (WR12, bits 3 through 14) defines the starting CRU bit address. The bits are transferred serially and the CRU address is incremented with each bit transfer, although the contents of WR12 is not affected. T_S and S provide multiple mode addressing capability for the source operand. If 8 or fewer bits are transferred (C = 1 through 8), the source address is a byte address. If 9 or more bits are transferred (C = 0, 9 through 15), the source address is a word address. If the source is addressed in teh workspace register indirect auto increment mode, the workspace register is incremented by 1 if C = 1 through 8, and is incremented by 2 otherwise.

| MNEMONIC	OP CODE						MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
	0	1	2	3	4	5				
LDCR	0	0	1	1	0	0	Load communication register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from (SA) to the CRU.
STCR	0	0	1	1	0	1	Store communication register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from the CRU to (SA). Load unfilled bit positions with 0.

†ST5 is affected only if $1 \leqslant C \leqslant 8$.

CRU Single-Bit Instructions

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
General format:	OP CODE								SIGNED DISPLACEMENT							

CRU relative addressing is used to address the selected CRU bit.

MNEMONIC	OP CODE								MEANING	STATUS BITS AFFECTED	DESCRIPTION
	0	1	2	3	4	5	6	7			
SBO	0	0	0	1	1	1	0	1	Set bit to one	—	Set the selected CRU output bit to 1.
SBZ	0	0	0	1	1	1	1	0	Set bit to zero	—	Set the selected CRU output bit to 0.
TB	0	0	0	1	1	1	1	1	Test bit	2	If the selected CRU input bit=1, set ST2.

Jump Instructions

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

General format:

| OP CODE	DISPLACEMENT
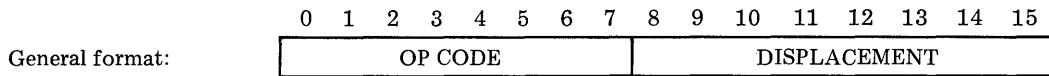
Jump instructions cause the PC to be loaded with the value selected by PC relative addressing if the bits of ST are at specified values. Otherwise, no operation occurs and the next instruction is executed since PC points to the next instruction. The displacement field is a word count to be added to PC. Thus, the jump instruction has a range of – 128 to 127 words from memory-word address following the jump instruction. No ST bits are affected by jump instruction.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	ST CONDITION TO LOAD PC
JEQ	0 0 0 1 0 0 1 1	Jump equal	ST2 = 1
JGT	0 0 0 1 0 1 0 1	Jump greater than	ST1 = 1
JH	0 0 0 1 1 0 1 1	Jump high	ST0 = 1 and ST2 = 0
JHE	0 0 0 1 0 1 0 0	Jump high or equal	ST0 = 1 or ST2 = 1
JL	0 0 0 1 1 0 1 0	Jump low	ST0 = 0 and ST2 = 0
JLE	0 0 0 1 0 0 1 0	Jump low or equal	ST0 = 0 or ST2 = 1
JLT	0 0 0 1 0 0 0 1	Jump less than	ST1 = 0 and ST2 = 0
JMP	0 0 0 1 0 0 0 0	Jump unconditional	unconditional
JNC	0 0 0 1 0 1 1 1	Jump no carry	ST3 = 0
JNE	0 0 0 1 0 1 1 0	Jump not equal	ST2 = 0
JNO	0 0 0 1 1 0 0 1	Jump no overflow	ST4 = 0
JOC	0 0 0 1 1 0 0 0	Jump on carry	ST3 = 1
JOP	0 0 0 1 1 1 0 0	Jump odd parity	ST5 = 1

Shift Instructions

| 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

General format:
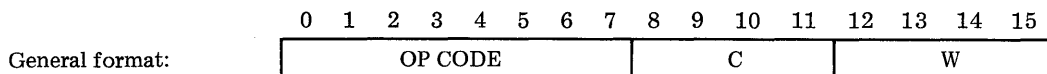
OP CODE	C	W

If C = 0, bits 12 through 15 of WR0 contain the shift count. If C = 0 and bits 12 through 15 of WR0 = 0, the shift count is 16.

| MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
SLA	0 0 0 0 1 0 1 0	Shift left arithmetic	Yes	0-4	Shift (W) left. Fill vacated bit positions with 0.
SRA	0 0 0 0 1 0 0 0	Shift right arithmetic	Yes	0-3	Shift (W) right. Fill vacated bit positions with original MSB of (W).
SRC	0 0 0 0 1 0 1 1	Shift right circular	Yes	0-3	Shift (W) right. Shift previous LSB into MSB.
SRL	0 0 0 0 1 0 0 1	Shift right logical	Yes	0-3	Shift (W) right. Fill vacated bit positions with 0's.

Immediate Register Instructions
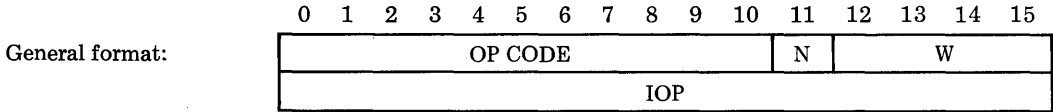
General format:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE											N	W			
IOP															

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
AI	0 0 0 0 0 0 1 0 0 0 1	Add immediate	Yes	0-4	(W)+IOP→(W)
ANDI	0 0 0 0 0 0 1 0 0 1 0	AND immediate	Yes	0-2	(W) AND IOP→(W)
CI	0 0 0 0 0 0 1 0 1 0 0	Compare immediate	Yes	0-2	Compare (W) to IOP and set appropriate status bits
LI	0 0 0 0 0 0 1 0 0 0 0	Load immediate	Yes	0-2	IOP→(W)
ORI	0 0 0 0 0 0 1 0 0 1 1	OR immediate	Yes	0-2	(W) OR IOP→(W)

Internal Register Load Immediate Instructions

General format:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE												N			
IOP															
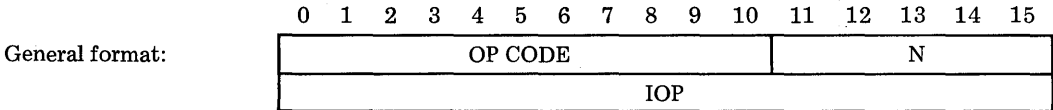
| MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
LWPI	0 0 0 0 0 0 1 0 1 1 1	Load workspace pointer immediate	IOP→(WP), no ST bits affected
LIMI	0 0 0 0 0 0 1 1 0 0 0	Load interrupt mask	IOP, bits 12 thru 15→ST12 thru ST15

Internal Register Store Instructions

General format:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE											N	W			
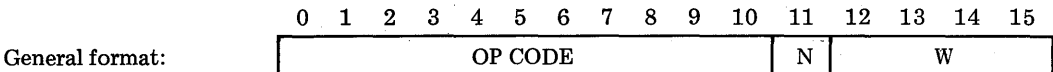
No ST bits are affected.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
STST	0 0 0 0 0 0 1 0 1 1 0	Store status register	(ST)→(W)
STWP	0 0 0 0 0 0 1 0 1 0 1	Store workspace pointer	(WP)→(W)

Return Workspace Pointer (RTWP) Instruction

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
General format:	0	0	0	0	0	0	1	1	1	0	0			N		
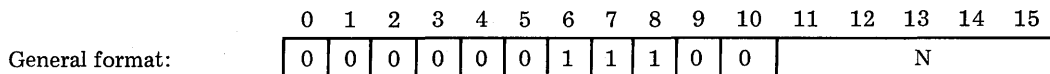
The RTWP instruction causes the following transfers to occur:

(WR15) → (ST)
(WR14) → (PC)
(WR13) → (WP)

External Instructions

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
General format:					OP CODE									N		
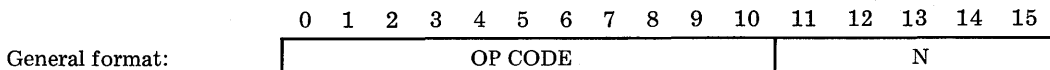
External instructions cause the three most-significant address lines (A0 through A2) to be set to the below described levels and the CRUCLK line to be pulsed, allowing external control functions to be initiated.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	STATUS BITS AFFECTED	DESCRIPTION	ADDRESS BUS A0 A1 A2
IDLE	0 0 0 0 0 0 1 1 0 1 0	Idle	—	Suspend S9900 instruction execution until an interrupt, $\overline{\text{LOAD}}$, or $\overline{\text{RESET}}$ occurs	L H L
RSET	0 0 0 0 0 0 1 1 0 1 1	Reset	12-15	0→ST12 through ST15	L H H
CKOF	0 0 0 0 0 0 1 1 1 1 0	User defined		—	H H L
CKON	0 0 0 0 0 0 1 1 1 0 1	User defined		—	H L H
LREX	0 0 0 0 0 0 1 1 1 1 1	User defined		—	H H H

S9900 Instruction Execution Times

Instruction execution times for the S9900 are a function of:

1) Clock cycle time, $t_{c(\phi)}$

2) Addressing mode used where operands have multiple addressing mode capability

3) Number of wait states required per memory access.

Table 3 lists the number of clock cycles and memory accesses required to execute each S9900 instruction. For instructions with multiple addressing modes for either or both operands, the table lists the number of clock cycles and memory accesses with all operands addressed in the workspace-register mode. To determine the additional number of clock cycles and memory accesses required for modified addressing, add the

Table 3. Instruction Execution Times

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION†		INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION†	
			SOURCE	DEST				SOURCE	DEST
A	14	4	A	A	LWPI	10	2	—	—
AB	14	4	B	B	MOV	14	4	A	A
ABS (MSB = 0)	12	2	A	—	MOVB	14	4	B	B
(MSB = 1)	14	4	A	—	MPY	52	5	A	—
AI	14	4	—	—	NEG	12	3	A	—
ANDI	14	4	—	—	ORI	14	4	—	—
B	8	2	A	—	RSET	12	1	—	—
BL	12	3	A	—	RTWP	14	4	—	—
BLWP	26	6	A	—	S	14	4	A	A
C	14	3	A	A	SB	14	4	B	B
CB	4	3	B	B	SBO	12	2	—	—
CI	14	3	—	—	SBZ	12	2	—	—
CKOF	12	1	—	—	SETO	10	3	A	—
CKON	12	1	—	—	Shift (C≠0)	12+2C	3	—	—
CLR	10	3	A	—	(C=0, Bits 12-15				
COC	14	3	A	—	of WR0=0)	52	4		
CZC	14	3	A	—	(C=0, Bits 12-15				
DEC	10	3	A	—	of WRP=N≠0)	20+2N	4	—	—
DECT	10	3	A	—	SOC	14	4	A	A
DIV (ST4 is set)	16	3	A	—	SOCB	14	4	B	B
DIV (ST4 is reset)*	92-124	6	A	—	STCR (C=0)	60	4	A	—
IDLE	12	1	—	—	(1≤C≤7)	42	4	B	—
INC	10	3	A	—	(C=8)	44	4	B	—
INCT	10	3	A	—	(9≤C≤15)	58	4	A	—
INV	10	3	A	—	STST	8	2	—	—
Jump (PC is					STWP	8	2	—	—
changed)	10	1	—	—	SWPB	10	3	A	—
(PC is not					SZC	14	4	A	A
changed)	8	1	—	—	SZCB	14	4	B	B
LDCR (C = 0)	52	3	A	—	TB	12	2	—	—
(1≤C≤8)	20+2C	3	B	—	X**	8	2	A	—
(9≤C≤15)	20+2C	3	A	—	XOP	36	8	A	—
LI	12	3	—	—	XOR	14	4	A	—
LIMI	16	2	—	—					
LREX	12	1	—	—					
RESET function	26	5	—	—	Undefined op codes 0000-01FF, 0320-033F, 0C00-0FFF, 0780-07FF	6	1	—	—
LOAD function	22	5	—	—					
Interrupt context switch	22	5	—	—					

*Execution time is dependent upon the partial quotient after each clock cycle during execution.

**Execution time is added to the execution time of the instruction located at the source address minus 4 clock cycles and 1 memory access time.

†The letters A and B refer to the respective tables that follow.

Table A Address Modification

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	8	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D $\neq$ 0)	8	2

Table B Address Modification

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	6	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D $\neq$ 0)	8	2

appropriate values from the referenced tables. The total instruction-execution time for an instruction is:

$$T = t_{c(\phi)} (C + W \cdot M)$$

where:

T = total instruction execution time;

$t_{c(\phi)}$ = clock cycle time;

C = number of clock cycles for instruction execution plus address modification;

W = number of required wait states per memory access for instruction execution plus address modification — no wait states used unless accessing slow memory;

M = number of memory accesses.

As an example, the instruction MOVB is used in a system with $t_{c(\phi)}$ = 0.333 μs and no wait states are required to access memory. Both operands are addressed in the workspace register mode:

$$T = t_{c(\phi)} (C + W \cdot M) = 0.333 (14 + 0 \cdot 4) \mu s = 4.662 \mu s.$$

If two wait states per memory access were required, the execution time is:

$$T = 0.333 (14 + 2 \cdot 4) \mu s = 7.326 \mu s.$$

If the source operand was addressed in the symbolic mode and two wait states were required:

$$T = t_{c(\phi)} (C + W \cdot M)$$
$$C = 14 + 8 = 22$$
$$M = 4 + 1 = 5$$
$$T = 0.333 (22 + 2 \cdot 5) \mu s = 10.656 \mu s.$$

System Design Examples

Figure 13 illustrates a typical minimum S9900 system. Eight bits of input and output interface are implemented. The memory system contains 1024x16 ROM and 1024x16 RAM memory blocks. The total package count for this system is 13 packages.

A maximum S9900 microprocessor system is illustrated in Figure 14. ROM and RAM are both shown for a total of 65,536 bytes of memory. The I/O interface supports 4096-output bits and 4096-input bits. Fifteen external interrupts are implemented in the interrupt interface. The clock generator and control section contains memory decode logic, synchronization logic, and the clock electronics. Bus buffers, required for this maximally configured system, are indicated on the system buses.
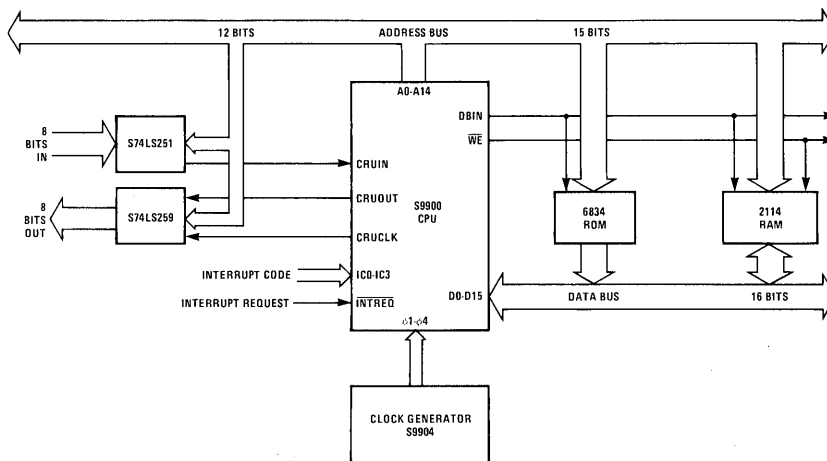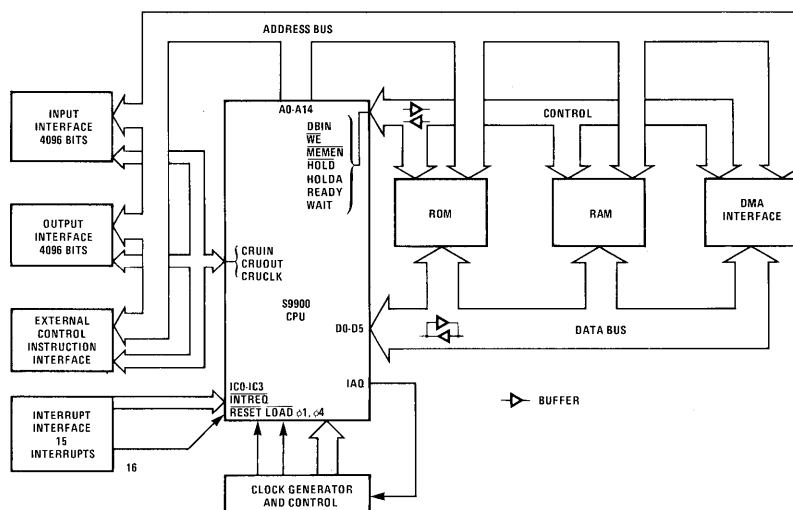
S9900

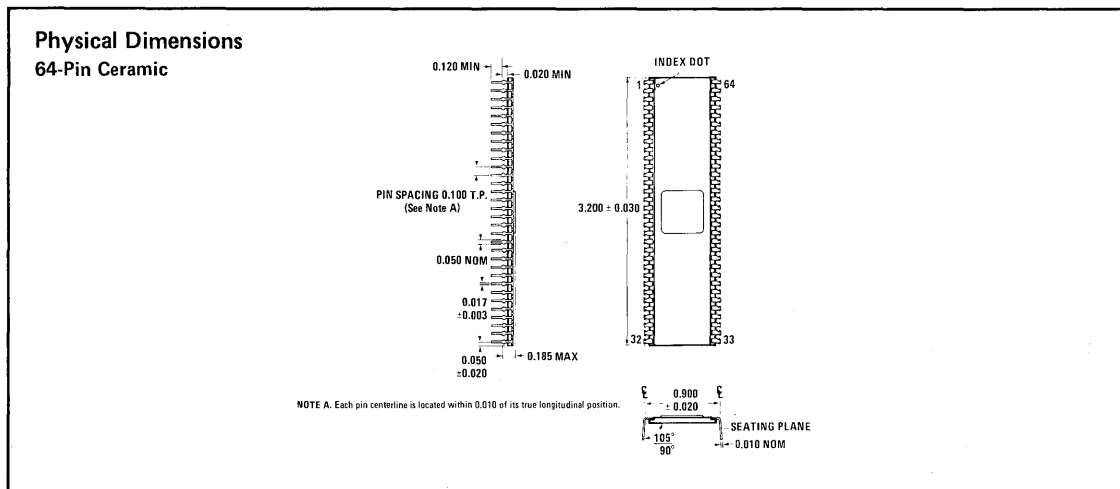Figure 13. Minimum S9900 System

Figure 14. Maximum S9900 System

Instruction Summary

MNEMONIC	OP CODE	FORMAT	RESULT COMPARED TO ZERO	STATUS AFFECTED	INSTRUCTIONS
A	A000	1	Y	0-4	ADD (WORD)
AB	B000	1	Y	0-5	ADD (BYTE)
ABS	0740	6	Y	0-4	ABSOLUTE VALUE
AI	0220	8	Y	0-4	ADD IMMEDIATE
ANDI	0240	8	Y	0-2	AND IMMEDIATE
B	0440	6	N	–	BRANCH
BL	0680	6	N	–	BRANCH AND LINE (W11)
BLWP	0400	6	N	–	BRANCH LOAD WORKSPACE POINTER
C	8000	1	N	0-2	COMPARE (WORD)
CB	9000	1	N	0-2,5	COMPARE (BYTE)
CI	0280	8	N	0-2	COMPARE IMMEDIATE
CKOF	03C0	7	N	–	EXTERNAL CONTROL
CKON	03A0	7	N	–	EXTERNAL CONTROL
CLR	04C0	6	N	–	CLEAR OPERAND
COC	2000	3	N	2	COMPARE ONES CORRESPONDING
CZC	2400	3	N	2	COMPARE ZEROES CORRESPONDING
DEC	0600	6	Y	0-4	DECREMENT (BY ONE)
DECT	0640	6	Y	0-4	DECREMENT (BY TWO)
DIV	3C00	9	N	4	DIVIDE
IDLE	0340	7	N	–	COMPUTER IDLE
INC	0580	6	Y	0-4	INCREMENT (BY ONE)
INCT	05C0	6	Y	0-4	INCREMENT (BY TWO)
INV	0540	6	Y	0-2	INVERT (ONES COMPLEMENT)
JEQ	1300	2	N	–	JUMP EQUAL (ST2=1)
JGT	1500	2	N	–	JUMP GREATER THAN (ST1=1)
JH	1800	2	N	–	JUMP HIGH (ST0=1 AND ST2=0)
JHE	1400	2	N	–	JUMP HIGH OR EQUAL (ST0 OR ST2=1)
JL	1A00	2	N	–	JUMP LOW (ST0 AND ST2=0)
JLE	1200	2	N	–	JUMP LOW OR EQUAL (ST0=0 OR ST2=1)
JLT	1100	2	N	–	JUMP LESS THAN (ST1 AND ST2=0)
JMP	1000	2	N	–	JUMP UNCONDITIONAL
JNC	1700	2	N	–	JUMP NO CARRY (ST3=0)
JNE	1600	2	N	–	JUMP NOT EQUAL (ST2=0)
JNO	1900	2	N	–	JUMP NO OVERFLOW (ST4=0)
JOC	1800	2	N	–	JUMP ON CARRY (ST3=1)
JOP	1C00	2	N	–	JUMP ODD PARITY (ST5=1)
LDCR	3000	4	Y	0-2,5	LOAD CRU
LI	0200	8	N	0-2	LOAD IMMEDIATE
LIMI	0300	8	N	12-15	LOAD IMMEDIATE TO INTERRUPT MASK
LREX	03E0	7	N	12-15	EXTERNAL CONTROL
LWPI	02E0	8	N	–	LOAD IMMEDIATE TO WORKSPACE POINTER
MOV	C000	1	Y	0-2	MOVE (WORD)
MOVB	D000	1	Y	0-2,5	MOVE (BYTE)
MPY	3800	9	N	–	MULTIPLY

Instruction Summary (Continued)

MNEMONIC	OP CODE	FORMAT	RESULT COMPARED TO ZERO	STATUS AFFECTED	INSTRUCTIONS
NEG	0500	6	Y	0-4	NEGATE (TWO'S COMPLEMENT)
ORI	0260	8	Y	0-2	OR IMMEDIATE
RSET	0360	7	N	12-15	EXTERNAL CONTROL
RTWP	0380	7	N	0-6, 12-15	RETURN WORKSPACE POINTER
S	6000	1	Y	0-4	SUBTRACT (WORD)
SB	7000	1	Y	0-5	SUBTRACT (BYTE)
SB0	1D00	2	N	–	SET CRU BIT TO ONE
SBZ	1E00	2	N	–	SET CRU BIT TO ZERO
SETO	0700	6	N	–	SET ONES
SLA	0A00	5	Y	0-4	SHIFT LEFT (ZERO FILL)
SOC	E000	1	Y	0-2	SET ONES CORRESPONDING (WORD)
SOCB	F000	1	Y	0-2,5	SET ONES CORRESPONDING (BYTE)
SRA	0800	5	Y	0-3	SHIFT RIGHT (MSB EXTENDED)
SRC	0B00	5	Y	0-3	SHIFT RIGHT CIRCULAR
SRL	0900	5	Y	0-3	SHIFT RIGHT (LEADING ZERO FILL)
STCR	3400	4	Y	0-2,5	STORE FROM CRU
STST	02C0	8	N	–	STORE STATUS REGISTER
STWP	02A0	8	N	–	STORE WORKSPACE POINTER
SWPB	06C0	6	N	–	SWAP BYTES
SZC	4000	1	Y	0-2	SET ZEROES CORRESPONDING (WORD)
SZCB	5000	1	Y	0-2,5	SET ZEROES CORRESPONDING (BYTE)
TB	1F00	2	N	2	TEST CRU BIT
X	0480	6	N	–	EXECUTE
XOP	2C00	9	N	6	EXTENDED OPERATION
XOR	2800	3	Y	0-2	EXCLUSIVE OR

ILLEGAL OP CODES 0000-01FF, 0320-033F, 0780-07FF, 0C00-0FFF

Physical Dimensions
64-Pin Ceramic

0.120 MIN
0.020 MIN
INDEX DOT
1
64
PIN SPACING 0.100 T.P. (See Note A)
3.200 ± 0.030
0.050 NOM
0.017 ±0.003
32
33
0.050 ±0.020
0.185 MAX
NOTE A. Each pin centerline is located within 0.010 of its true longitudinal position.
0.900 ± 0.020
SEATING PLANE
105°
90°
0.010 NOM

AMI®

Programmable Systems Interface Circuit

Features

- N-Channel Silicon-Gate Process
- 9900 Series CRU Peripheral
- Performs Interrupt and I/O Interface Functions
  - 6 Dedicated Interrupt Input Lines
  - 7 Dedicated I/O Ports
  - 9 Ports Programmable as Interrupts or I/O
- Easily Stacked for Interrupt and I/O Expansion
- Interval and Event Timer
- Single 5V Supply

General Description

The S9901 Programmable Systems Interface is a multifunctioned component designed to provide low cost interrupts and I/O ports in a 9900/9980 microprocessor system. It is fabricated with N-channel silicon-gate technology and is completely TTL compatible on all inputs including the power supply (+5V) and single-phase clock. Figure 1 is a block diagram of the S9901. The Programmable Systems Interface provides a 9900/9980 system with interrupt control, I/O ports, and a real-time clock as shown in Figure 2.

Figure 1. Block Diagram

S9901 Pin Configuration
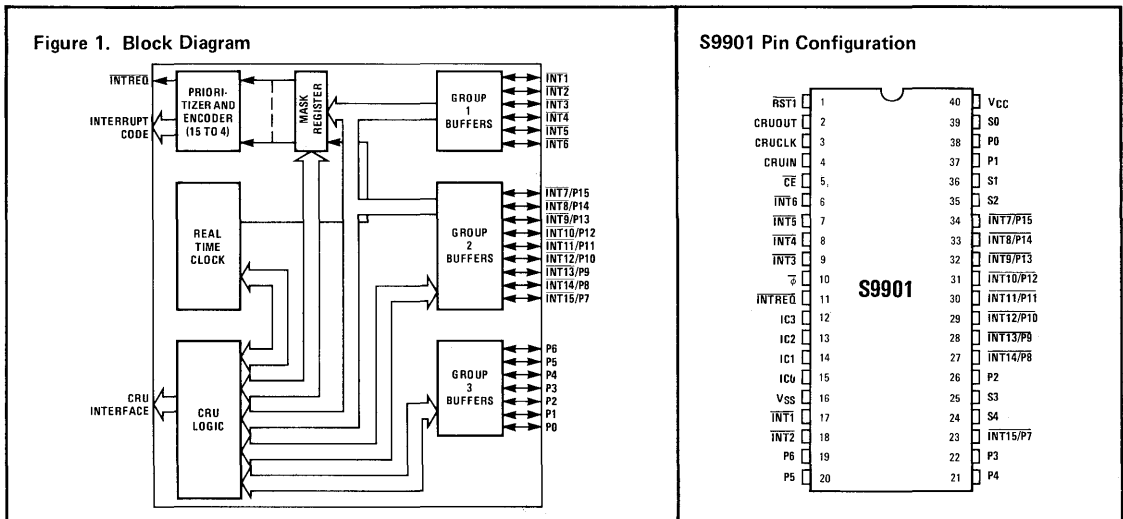
Figure 2. 9900/9980 System

S9900
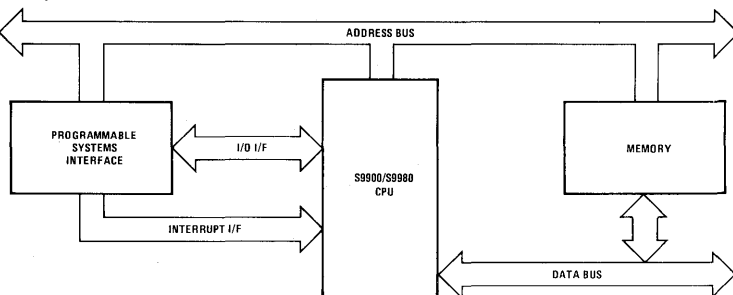
S9901 Electrical Specifications

Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply Voltages, V_{CC} and V_{SS}	−0.3V to +10V
All Input and Output Voltages	−0.3V to +10V
Continuous Power Dissipation	0.75W
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_{SS}		0		V
High-Level Input Voltage, V_{IH}		2		V
Low-Level Input Voltage, V_{IL}		0.8		V
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_I	Input Current (Any Input)		±10		μA	V_I = 0V to V_{CC}
V_{OH}	High Level Output Voltage		2.4		V	I_{OH} = 100μA
			2		V	I_{OH} = −400μA
V_{OL}	Low Level Output Voltage		0.4		V	I_{OL} = 3.2mA
I_{CC}	Supply Current from V_{CC}		100		mA	
I_{SS}	Supply Current from V_{SS}		200		mA	
$I_{CC(av)}$	Average Supply Current from V_{CC}		60		mA	$t_{c(\phi)}$ = 333ns, T_A = 25°C
C_i	Capacitance, Any Input		10		pF	f = 1MHz,
C_o	Capacitance, Any Output		20		pF	All Other Pins at 0V

Timing Requirements Over Full Range of Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit
$t_{c(\phi)}$	Clock Cycle Time		333		ns
$t_{r(\phi)}$	Clock Rise Time		10		ns
$t_{f(\phi)}$	Clock Fall Time		10		ns
$t_{w(\phi L)}$	Clock Pulse Low Width		55		ns
$t_{w(\phi H)}$	Clock Pulse High Width		240		ns
t_{su}	Setup Time for S0-S4, CE, or CRUOUT before CRUCLK		200		ns
t_{su}	Setup Time, Input Before Valid CRUIN		200		ns
t_{su}	Setup Time, Interrupt Before ϕ Low		40		ns
$t_{w(CRUCLK)}$	CRU Clock Pulse Width		100		ns
t_h	Address Hold Time		80		ns

Switching Characteristics Over Full Range of Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{PD}	Propagation Delay, $\overline{\phi}$ Low to Valid $\overline{\text{INTREQ}}$, I_{C0} - I_{C3}		80		ns	C_L = 100pF, 2 TTL Loads
t_{PD}	Propagation Delay, S0-S4 or $\overline{\text{CE}}$ to Valid CRUIN		400		ns	C_L = 100pF

Figure 3. Switching Characteristics
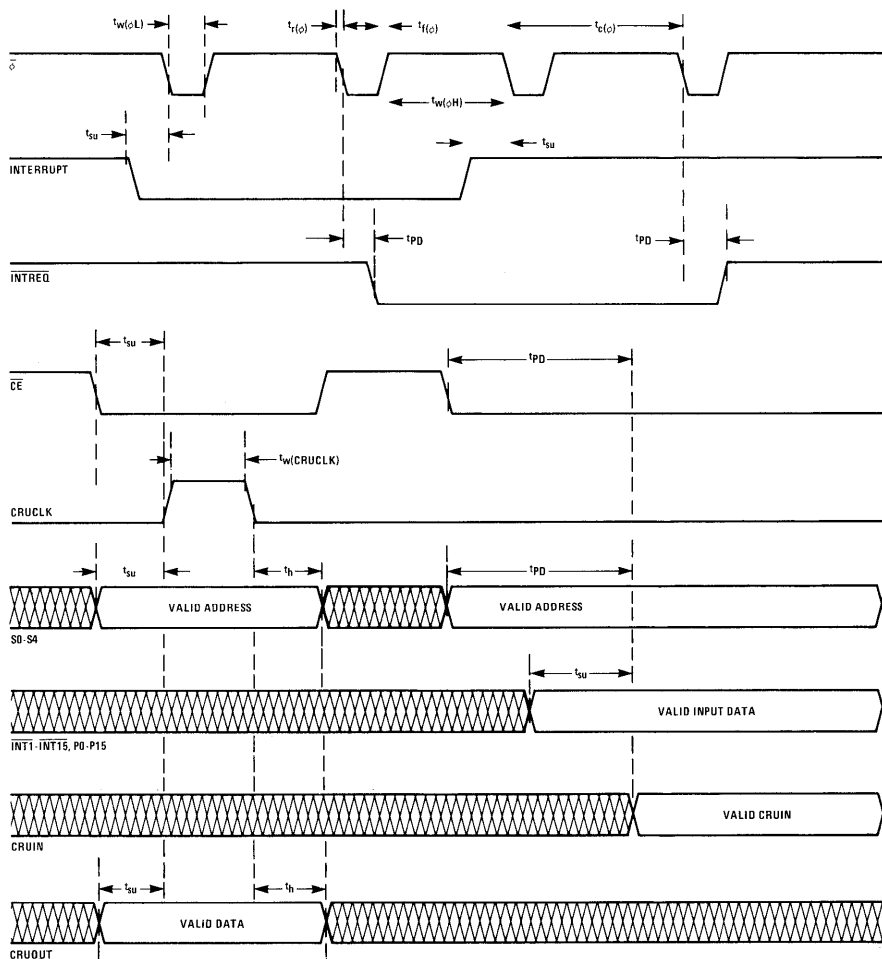
NOTE 1: ALL TIMING MEASUREMENTS ARE FROM 10% and 90% POINTS

S9900

Pin Definitions

Table 1 defines the S9901 pin assignments and describes the function of each pin.

Table 1. S9901 Pin Assignments and Functions

Signature	Pin	I/O	Description
$\overline{\text{INTREQ}}$	11	OUT	INTERRUPT Request. When active (low) $\overline{\text{INTREQ}}$ indicates that an enabled interrupt has been received. $\overline{\text{INTREQ}}$ will stay active until all enabled interrupt inputs are removed.
IC0 (MSB)	15	OUT	Interrupt Code lines. IC0-IC3 output the binary code corresponding to
IC1	14	OUT	the highest priority enabled interrupt. If no enabled interrupts are active
IC2	13	OUT	IC0-IC3 = (1,1,1,1).
IC3 (LSB)	12	OUT	
$\overline{\text{CE}}$	5	IN	Chip Enable. When active (low) data may be transferred through the CRU interface to the CPU. $\overline{\text{CE}}$ has no effect on the interrupt control section.
S0	39	IN	Address select lines. The data bit being accessed by the CRU interface is
S1	36	IN	specified by the 5-bit code appearing on S0-S4.
S2	35	IN	
S3	25	IN	
S4	24	IN	
CRUIN	4	OUT	CRU data in (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{\text{CE}}$ is not active CRUIN is in a high-impedance state.
CRUOUT	2	IN	CRU data out (from CPU). When $\overline{\text{CE}}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the command bit specified by S0-S4.
CRUCLK	3	IN	CRU Clock (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{\text{RST1}}$	1	IN	Power Up Reset. When active (low) $\overline{\text{RST1}}$ resets all interrupt masks to "0", disables the clock, and programs all I/O ports to inputs. $\overline{\text{RST1}}$ has a Schmitt-Trigger input to allow implementation with an RC circuit as shown in Figure 6.
V_{CC}	40		Supply Voltage. +5V nominal.
V_{SS}	16		Ground Reference
$\overline{\phi}$	10		System clock ($\overline{\phi}3$ in S9900 system, $\overline{\text{CKOUT}}$ in S9980 system).
$\overline{\text{INT1}}$	17	IN	Group 1, interrupt inputs. When active.
$\overline{\text{INT2}}$	18	IN	(Low) the signal is ANDed with its corresponding mask bit and if enabled
$\overline{\text{INT3}}$	9	IN	sent to the interrupt control section. INT1 has highest priority.
$\overline{\text{INT4}}$	8	IN	
$\overline{\text{INT5}}$	7	IN	
$\overline{\text{INT6}}$	6	IN	
$\overline{\text{INT7}}$/P15	34	I/O	Group 2, Programmable interrupt (active low) or I/O pins (true logic).
$\overline{\text{INT8}}$/P14	33	I/O	Each pin is individually programmable as an interrupt, an input port, or an
$\overline{\text{INT9}}$/P13	32	I/O	output port.
$\overline{\text{INT10}}$/P12	31	I/O	
$\overline{\text{INT11}}$/P11	30	I/O	
$\overline{\text{INT12}}$/P10	29	I/O	
$\overline{\text{INT13}}$/P9	28	I/O	
$\overline{\text{INT14}}$/P8	27	I/O	
$\overline{\text{INT15}}$/P7	23	I/O	
P0	38	I/O	Group 3, I/O ports (true logic). Each pin is individually programmable as
P1	37	I/O	an input port or an output port.
P2	26	I/O	
P3	22	I/O	
P4	21	I/O	
P5	20	I/O	
P6	19	I/O	

Functional Description

CPU Interface

The S9901 interfaces to the CPU through the Communications Register Unit (CRU) and the interrupt control lines as shown in Figure 1. The CRU interface consists of 5 address select lines (S0-S4), chip enable ($\overline{CE}$), and 3 CRU lines (CRUIN, CRUOUT, CRUCLK). When $\overline{CE}$ becomes active (low), the 5 select lines point to the CRU bit being accessed (see Table 2). In the case of a write, the datum is strobed off the CROUT line by the CRUCLK signal. For a read, the datum is sent to the CPU on the CRUIN line. The interrupt control lines consist of an interrupt request line ($\overline{INTREQ}$) and 4 code lines (IC0-IC3). The interrupt section of the S9901 prioritizes and encodes the highest priority active interrupt into the proper code to present to the CPU, and outputs this code on the IC0-IC3 code lines along with an active $\overline{INTREQ}$. Several S9901's can be used with the CPU by connecting all CRU and address lines in parallel and providing a unique chip select to each device.

System Interface

The system interface consists of 22 pins divided into 3 groups. The 6 pins in Group 1 ($\overline{INT1}$-$\overline{INT6}$) are normally dedicated to interrupt inputs (active low), but may also be used as input ports (true data in). Group 2 ($\overline{INT7}$/P15-$\overline{INT15}$/P7) consists of 9 pins which can be individually programmed as interrupt inputs (active low), input ports (true data in), or output ports (true data out). The remaining 7 pins which comprise Group 3 (P0-P6) are dedicated as individually programmable I/O ports (true data).

Interrupt Control

A block diagram of the interrupt control section is shown in Figure 4. The interrupt inputs (6 dedicated, 9 programmable) are sampled by $\bar{\phi}$ (active low) and are ANDED with their respective mask bits. If an interrupt input is active (low) and enabled (MASK=1), the signal is passed through to the priority encoder where the highest priority signal is encoded into a 4-bit binary code as shown in Table 3. The code along with the interrupt request is then output via the CPU interface on the leading edge of the next $\bar{\phi}$ to ensure proper synchronization to the processor.

The output signals will remain valid until the corresponding interrupt input is removed, the interrupt is disabled (MASK=0), or a higher priority enabled interrupt becomes active. When the highest priority enabled interrupt is removed, the code corresponding to the next highest priority enabled interrupt is output. If no enabled interrupt is active, all CPU interface lines ($\overline{INTREQ}$, IC0-IC3) are held high. $\overline{RST1}$ (power-up-reset) will force the output code to (0,0,0,0) with $\overline{INTREQ}$ held high and will reset all mask bits low (interrupts disabled). Individual interrupts can be subsequently enabled (disabled) by programming the appropriate command bits. Unused interrupt inputs may be used as datum inputs by disabling the interrupt (MASK=0).

Input/Output

A block diagram of the I/O section is shown in Figure 5. Up to 16 individually controlled I/O ports are available (7 dedicated, 9 programmable). $\overline{RST1}$ or $\overline{RST2}$ (a command bit) will program all ports to the input mode. Writing a datum to any port will program that port to the output mode and latch out the datum. The port will then remain in the output mode until either $\overline{RST1}$ or $\overline{RST2}$ is executed. Data present on the Group 2 pins can be read by either the Read Interrupt Commands or the Read Input Commands. Group 2 pins being used as input ports should have their respective Interrupt Mask values reset (low) to prevent false interrupts from occurring. In applications where Group 1 pins are not required as interrupt inputs, they may be used as input ports and read using the Read Input commands. As with Group 2 ports, any pins being used as input ports should have their respective Interrupt Masks disabled.

Table 2. CRU Bit Assignments

CRU Bit	S0	S1	S2	S3	S4	CRU Read Data	CRU Write Data
0	0	0	0	0	0	CONTROL BIT[1]	CONTROL BIT[1]
1	0	0	0	0	1	$\overline{INT}$1/CLK1[2]	Mask 1/CLK1[3]
2	0	0	0	1	0	$\overline{INT}$2/CLK2	Mask 2/CLK2
3	0	0	0	1	1	$\overline{INT}$3/CLK3	Mask 3/CLK3
4	0	0	1	0	0	$\overline{INT}$4/CLK4	Mask 4/CLK4
5	0	0	1	0	1	$\overline{INT}$5/CLK5	Mask 5/CLK5
6	0	0	1	1	0	$\overline{INT}$6/CLK6	Mask 6/CLK6
7	0	0	1	1	1	$\overline{INT}$7/CLK7	Mask 7/CLK7
8	0	1	0	0	0	$\overline{INT}$8/CLK8	Mask 8/CLK8
9	0	1	0	0	1	$\overline{INT}$9/CLK9	Mask 9/CLK9
10	0	1	0	1	0	$\overline{INT}$10/CLK10	Mask 10/CLK10
11	0	1	0	1	1	$\overline{INT}$11/CLK11	Mask 11/CLK11
12	0	1	1	0	0	$\overline{INT}$12/CLK12	Mask 12/CLK12
13	0	1	1	0	1	$\overline{INT}$13/CLK13	Mask 13/CLK13
14	0	1	1	1	0	$\overline{INT}$14/CLK14	Mask 14/CLK14
15	0	1	1	1	1	$\overline{INT}$15/$\overline{INTREQ}$	Mask 15/$\overline{RST2}$[4]
16	1	0	0	0	0	P0 INPUT[5]	P0 Output[6]
17	1	0	0	0	1	P1 Input	P1 Output
18	1	0	0	1	0	P2 Input	P2 Output
19	1	0	0	1	1	P3 Input	P3 Output
20	1	0	1	0	0	P4 Input	P4 Output
21	1	0	1	0	1	P5 Input	P5 Output
22	1	0	1	1	0	P6 Input	P6 Output
23	1	0	1	1	1	P7 Input	P7 Output
24	1	1	0	0	0	P8 Input	P8 Output
25	1	1	0	0	1	P9 Input	P9 Output
26	1	1	0	1	0	P10 Input	P10 Output
27	1	1	0	1	1	P11 Input	P11 Output
28	1	1	1	0	0	P12 Input	P12 Output
29	1	1	1	0	1	P13 Input	P13 Output
30	1	1	1	1	0	P14 Input	P14 Output
31	1	1	1	1	1	P15 Input	P15 Output

NOTES: (1) 0 = Interrupt Mode   1 = Clock Mode
(2) Data present on INT input pin (or clock value) will be read regardless of mask value.
(3) While in the Interrupt Mode (Control Bit = 0) writing a "1" into mask will enable interrupt; a "0" will disable.
(4) Writing a zero to bit 15 while in the clock mode (Control Bit = 1) executes a software reset of the I/O pins.
(5) Data present on the pin will be read. Output data can be read without affecting the data.
(6) Writing data to the port will program the port to the output mode and output the data.
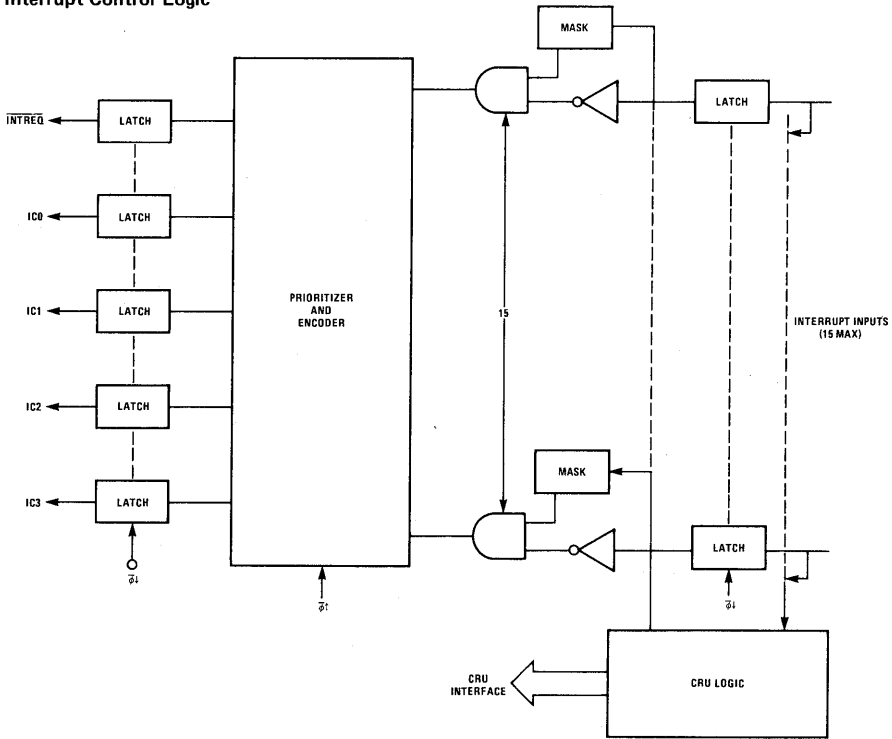
Figure 4. Interrupt Control Logic

Table 3 Interrupt Code Generation

Interrupt/State	Priority	IC0	IC1	IC2	IC3	$\overline{\text{INTREQ}}$
$\overline{\text{INT}}$1	1 (HIGHEST)	0	0	0	1	0
$\overline{\text{INT}}$2	2	0	0	1	0	0
$\overline{\text{INT}}$3/CLOCK	3	0	0	1	1	0
$\overline{\text{INT}}$4	4	0	1	0	0	0
$\overline{\text{INT}}$5	5	0	1	0	1	0
$\overline{\text{INT}}$6	6	0	1	1	0	0
$\overline{\text{INT}}$7	7	0	1	1	1	0
$\overline{\text{INT}}$8	8	1	0	0	0	0
$\overline{\text{INT}}$9	9	1	0	0	1	0
$\overline{\text{INT}}$10	10	1	0	1	0	0
$\overline{\text{INT}}$11	11	1	0	1	1	0
$\overline{\text{INT}}$12	12	1	1	0	0	0
$\overline{\text{INT}}$13	13	1	1	0	1	0
$\overline{\text{INT}}$14	14	1	1	1	0	0
$\overline{\text{INT}}$15	15 (LOWEST)	1	1	1	1	0
NO INTERRRUPT	—	1	1	1	1	1

Programmable Real Time Clock

A block diagram of the programmable real time clock section is shown in Figure 6. The clock consists of a 14-bit counter that decrements at a rate of $F(\phi)/64$ (at 3MHz this results in a maximum interval of 349ms with a resolution of $21.3\mu s$) and can be used as either an interval timer or as an event timer.

The clock is accessed by writing a one into the control bit (address 0) to force CRU bits 1-15 to clock mode. (See Table 1.) Writing a nonzero value into the clock register then enables the clock and sets its frequency. During system set up this entire operation can be accomplished with one additional I/O instruction (LCDR) as shown in Table 4. The clock functions as an interval timer by decrementing to zero, issuing an interrupt, and restarting at the programmed start value. When the clock interrupt is active, the clock mask (mask bit 3) must be written into (with either a "1" or a "0") to clear the interrupt.

If a value other than that initially programmed is required, a new 14-bit clock start value is similarly programmed by executing a CRU write operation to the same locations. During programming the decrementer

is restarted with the current start value after each start value bit is written. A timer restart can be easily implemented by writing a single bit to any of the clock bits.

The clock is disabled by $\overline{RST1}$ (power-up-clear) or by writing a zero value into the clock register. Enabling the clock programs the third priority interrupt ($\overline{INT3}$) as the clock interrupt and disables generation of interrupts from the $\overline{INT3}$ input pin. When accessing the clock all interrupts should be disabled to ensure that system integrity is maintained.

The clock can also function as an event timer since whenever the device is switched to the clock mode, by writing a one to the control bit, the current value of the clock is stored in the clock read register. Reading this value, and thus the elapsed event time, is accomplished by executing a 14-bit CRU read operation (addresses 1-14). The software example (Table 3) shows a read of the event timer.

The current status of the machine can always be obtained by reading the control (address zero) bit. A "0" indicates the machine is in an interrupt mode. Bits 1

Figure 5. I/O Interface
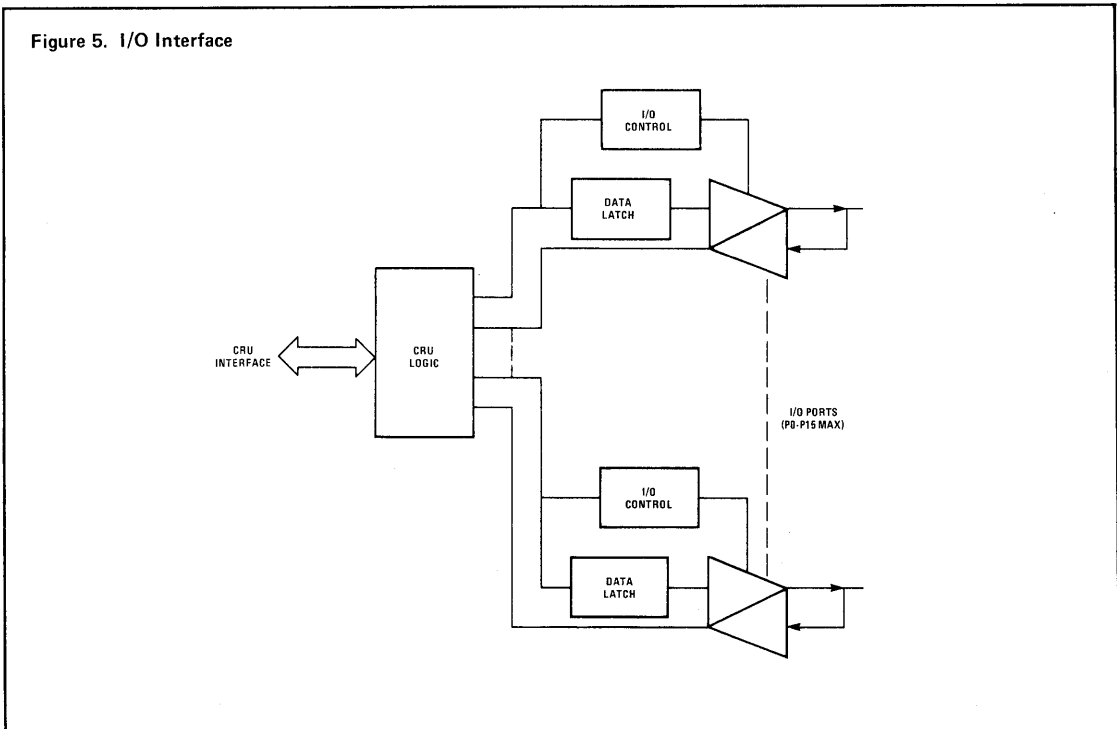
through 15 would normally be the interrupt input lines in this mode, but if any are not needed for interrupts they may also be read with a CRU input command and interpreted as normal data inputs. A "1" read on the control bit indicates that the 9901 is in the clock mode. Reading bits 1 through 14 completes the event timer operation as described above. Reading

bit 15 indicates whether the interrupt request line is active.

A software reset $\overline{RST2}$ can be performed by writing a "1" to the control bit followed by writing a "1" to bit 15, which forces all I/O ports to the input mode.

Table 4 Software Examples

Assumptions

   — System uses clock at maximum interval
   — Total of 6 interrupts are used
   — 8 bits are used as output port

   — 8 bits are used as input port
   — RST1 (power up reset) has already been applied

System Setup for Interrupt	LI	R12,PSIBAS	Setup CRU Base Address to point 9901
	LDCR	@X,0	Program Clock with maximum interval
	LDCR	@Y,7	Re-enter interrupt mode and enable top 6 interrupts

| System Setup for Output Ports | LI | R12,PSIBAS+ 16 | Move CRU Base to point I/O port |
| | LDCR | R1,8 | Move most significant byte of R1 to output port |

| Read Programmed Inputs | LI | R12,PSIBAS+ 24 | Move CRU Base to point to input ports |
| | STCR | R2,8 | Move input port to most significant byte of R2 |

(X) ——► FFFF

(Y) ——► 7FXX

Don't cares

	BLWP	CLKVCT	Save Interrupt Mask
	•		
	•		
	•		
CLKPC	LIMI	0	Disable INTERRUPTS
	LI	R12,PSIBAS+ 1	Set up CRU Base
	SB0	−1	Set 9901 into Clock Mode, Latch Clock Value
	STCR	R4,14	Store Read Register Latch Value into R4
	SBZ	−1	Reenter Interrupt Mode and Restarting Clock
	RTWP		Restore Interrupt Mask
	○		
	•		
	•		
CLKVCT	DATA	CLKWP, CLKPC	

Figure 6. Real Time Clock
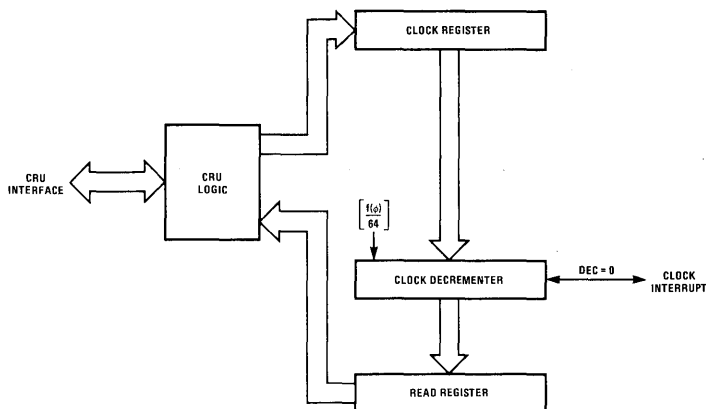
System Operation

During power up $\overline{RST1}$ must be activated (low) for a minimum of 2 clock cycles to force the S9901 into a known state. $\overline{RST1}$ will disable all interrupts, disable the clock, program all I/O ports to the mode, and force IC0-IC3 to (0,0,0,0) with $\overline{INTREQ}$ held high. System software must then enable the proper interrupts, program the clock (if used), and configure the I/O ports as required (see Table 4 for an example). After initial power up, the S9901 will be accessed only as needed to service the clock, enable (disable) interrupts, or

read (write) data to the I/O ports. The I/O ports can be reconfigured by use of the $\overline{RST2}$ command bit.

Figure 7 illustrates the use of an S9901 with an S9900. The S9904 is used to generate RST to reset the 9900 and the 9901 (connected to $\overline{RST1}$). Figure 8 shows an S9980 system using the S9901. The reset function, load interrupt, and 4 maskable interrupts allowed in a 9980 are encoded as shown in Table 5. Connecting the system as shown ensures that the proper reset will be applied to the 9980.

Table 5 9980 Interrupt Level Data

Interrupt Code (IC0-IC2)	Function	Vector Location (Memory Address In Hex)	Device Assignment	Interrupt Mask Values To Enable (ST12 through ST15)
1 1 0	Level 4	0 0 1 0	External Device	4 Through F
1 0 1	Level 3	0 0 0 C	External Device	3 Through F
1 0 0	Level 2	0 0 0 8	External Device	2 Through F
0 1 1	Level 1	0 0 0 4	External Device	1 Through F
0 0 1	Reset	0 0 0 0	Reset Stimulus	Don't Care
0 1 0	Load	3 F F C	Load Stimulus	Don't Care
0 0 0	Reset	0 0 0 0	Reset Stimulus	Don't Care
1 1 1	No-Op	—	—	Don't Care

Figure 7. S9900-S9901 Interface
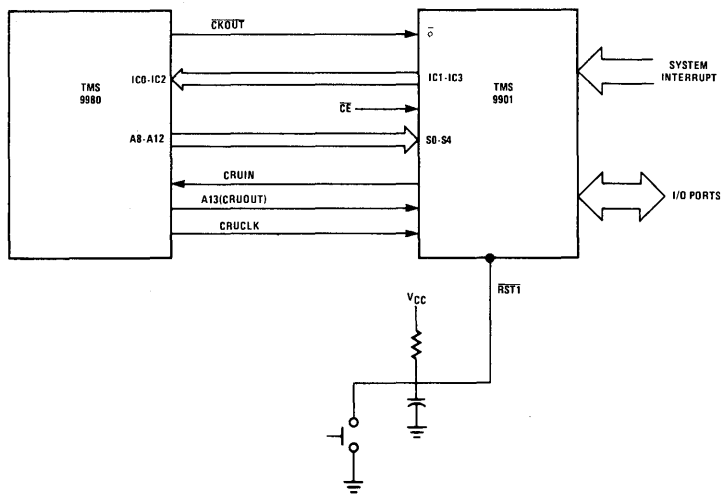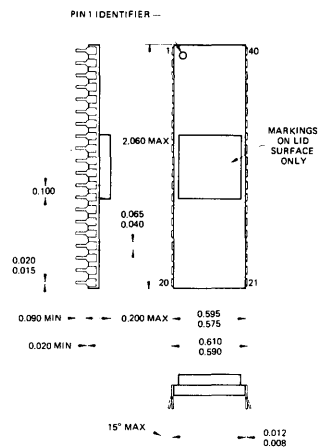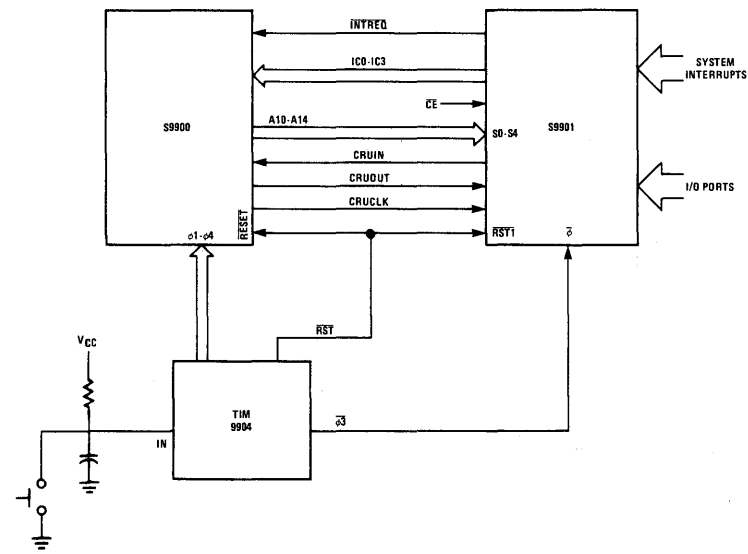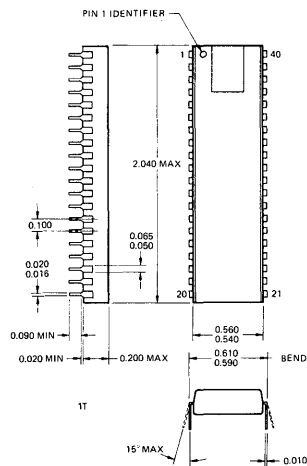

S9901 40 Pin Ceramic Package

Figure 8. S9980-S9901 Interface

S9901 40 Pin Plastic Package

S9900

AMI ®

Asynchronous Communications Controller (ACC)

Features

- 5- to 8-Bit Character Length
- 1, 1 1/2, or 2 Stop Bits
- Even, Odd, or No Parity
- Fully Programmable Data Rate Generation
- Interval Timer with Resolution from 64 to 16,320 μs
- Fully TTL Compatible, Including Single Power Supply.

General Description

The S9902 Asynchronous Communication Controller (ACC) is a peripheral device for the S9900 family of microprocessors. The ACC provides an interface between the microprocessor and a serial asynchronous communication channel, performing the timing and data serialization and deserialization, thus facilitating the control of the asynchronous channel by the microprocessor.

Figure 1. Block Diagram
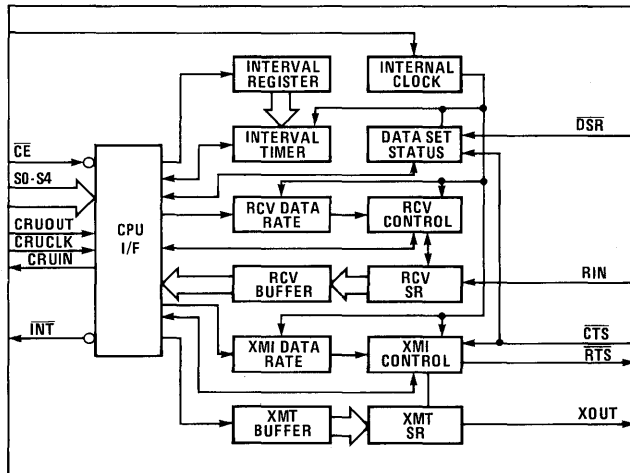
Figure 2. Pin Configuration
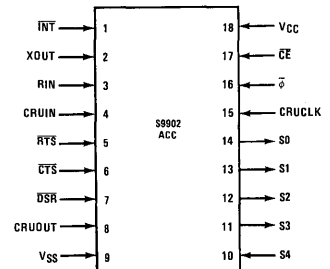
S9902 Electrical Specifications

Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply Voltage, V_{CC} .... -0.3V to +10V
All Inputs and Output Voltages .... -0.3V to +10V
Continuous Power Dissipation 0.7W
Operating Free-Air Temperature Range .... 0°C to +70°C
Storage Temperature Range .... -65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_{SS}		0		V
High-Level Input Voltage, V_{IH}	2.2	2.4	V_{CC}	V
Low-Level Input Voltage, V_{IL}		0.4	0.8	V
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_I	Input Current (Any Input)			±10	μA	$V_I = 0V$ to V_{CC}
V_{OH}	High-Level Output Voltage	2.2	3.0		V	$I_{OH} = -100\mu A$
		2.0	2.5			$I_{OH} = -400\mu A$
V_{OL}	Low-Level Output Voltage		0.4	0.85	V	$I_{OL} = 3.2mA$
$I_{CC(AV)}$	Average Supply Current from V_{CC}		2.5	100	mA	$t_{c(\phi)} = 250ns$, $T_A = 25°C$
C_i	Capacitance, Any Input		10		pF	f = 1 MHz,
C_o	Capacitance, Any Output		20			All other pins at 0V

Timing Requirements Over Full Range of Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{c(\phi)}$	Clock Cycle Time	300	333	2000	ns
$t_{r(\phi)}$	Clock Rise Time		10	12	ns
$t_{f(\phi)}$	Clock Fall Time		10	12	ns
$t_{H(\phi)}$	Clock Pulse Width (High Level)		225	240	ns
$t_{L(\phi)}$	Clock Pulse Width (Low Level)		45	55	ns
$t_{su(ad)}$	Setup Time for Address and CRUOUT Before CRUCLK		220		ns
$t_{su(CE)}$	Setup Time for CE Before CRUCLK		190		ns
t_{HD}	Hold Time for Address, CE and CRUOUT After CRUCLK		90		ns
t_{wcc}	CRUCLK Pulse Width		120		ns

Switching Characteristics Over Full Range of Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$T_{PCI(cd)}$	Propagation Delay, Address-to-Valid CRUIN			400	ns	$C_L = 100pF$
$T_{PCI(CE)}$	Propagation Delay, $\overline{CE}$-to-Valid CRUIN			400	ns	$C_L = 100pF$
t_H	CRUIN Hold Time After Address			20	ns	

Figure 3. Switching Characteristics
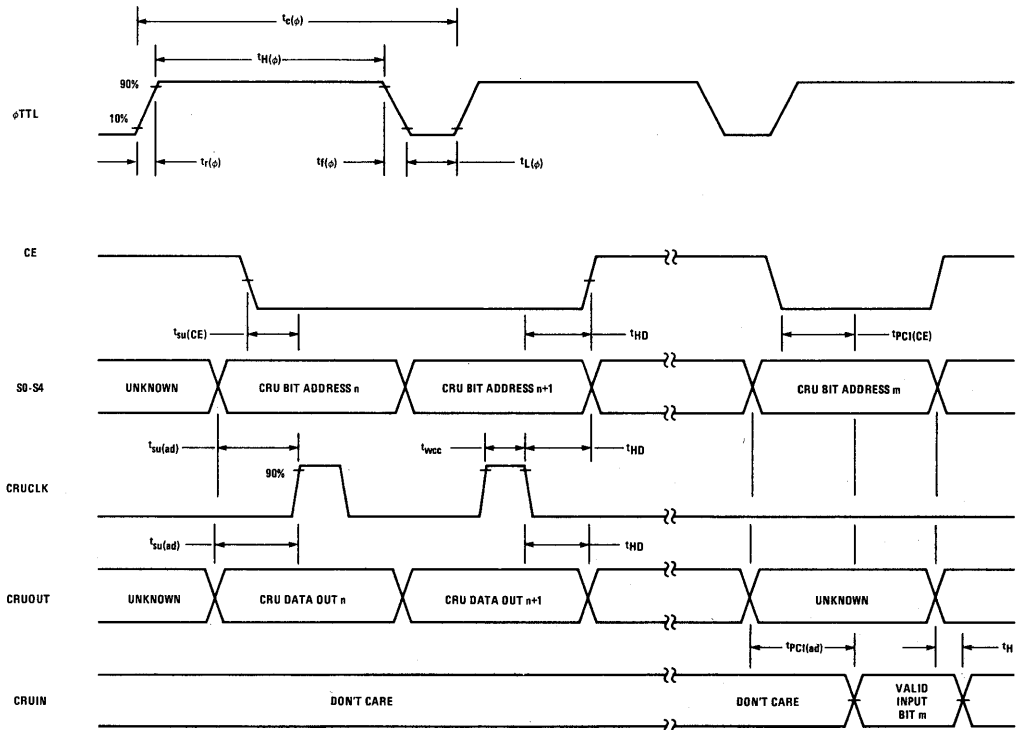
S9902 Pin Description

Table 1 defines the S9902 pin assignments and describes the function of each pin as shown in Figure 2.

Table 1

Signature	Pin	I/O	Description
$\overline{\text{INT}}$	1	O	Interrupt — when active (low), the $\overline{\text{INT}}$ output indicates that at least one of the interrupt conditions has occured.
XOUT	2	O	Transmitter serial data output line — XOUT remains inactive (high) when S9902 is not transmitting.
RIN	3	I	Receiver serial data input line — RCV — must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receiver circuitry.
CRUIN	4	O	Serial data output pin from S9902 to CRUIN input pin of the CPU.
$\overline{\text{RTS}}$	5	O	Request-to-send output from S9902 to modem. This output is enabled by the CPU and remains active (low) during transmission from the S9902.
$\overline{\text{CTS}}$	6	I	Clear-to-send input from modem to S9902. When active (low), it enables the transmitter section of S9902.
$\overline{\text{DSR}}$	7	I	Data set ready input from modem to S9902. This input generates an interrupt when going On or Off.
CRUOUT	8	I	Serial data input line to S9902 from CRUOUT line of the CPU.
V_{SS}	9	I	Ground reference voltage.
S4 (LSB)	10	I	
S3	11	I	
S2	12	I	
S1	13	I	Address bus S0-S4 are the lines that are addressed by the CPU to select a
S0	14	I	particular S9902 function.
CRUCLK	15	I	CRU Clock. When active (high), S9902 from CRUOUT line of the CPU.
$\overline{\phi}$	16	I	TTL Clock.
$\overline{\text{CE}}$	17	I	Chip enable — when CE is inactive (high), the S9902 address decoding is inhibited which prevents execution of any S9902 command function. CRUIN remains at high-impedance when $\overline{\text{CE}}$ is inactive (high).
V_{CC}	18	I	Supply voltage (+5V nominal).

S9900

Device Interface

The relationship of the ACC to other components in the system is shown in Figures 4 and 5. The ACC is connected to the asychronous channel through level shifters which translate the TTL inputs and outputs to the appropriate levels (e.g., RS-232C, TTY current loop, etc.). The microprocessor transfers data to and from the ACC via the Communication Register Unit (CRU).

CPU Interface

The ACC interfaces to the CPU through the Communication Register Unit (CRU). The CRU interface consists of five address-select lines (S0-S4), chip enable ($\overline{\text{CE}}$), and three CRU control lines (CRUIN, CRUOUT, and CRUCLK). When $\overline{\text{CE}}$ becomes active (low), the five select lines address the CRU bit being accessed. When data is being transferred to the ACC from the CPU, CRUOUT contains the valid datum which is strobed by CRUCLK. When ACC data is being read, CRUIN is the datum output by the ACC.
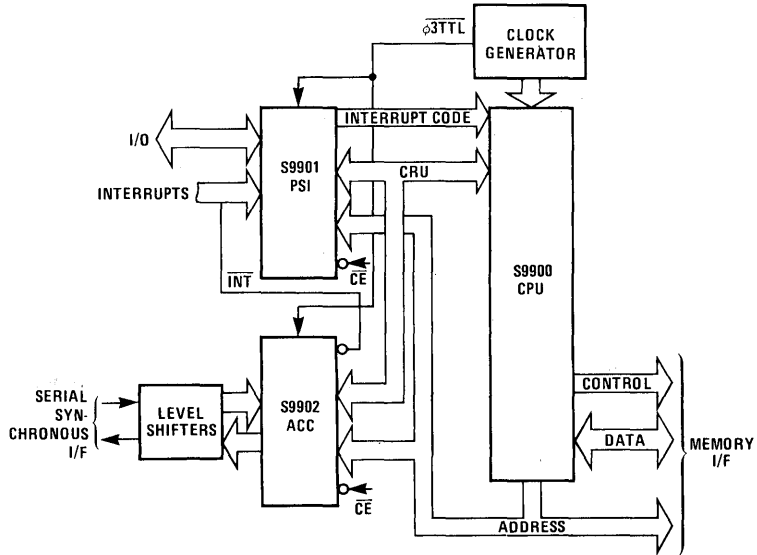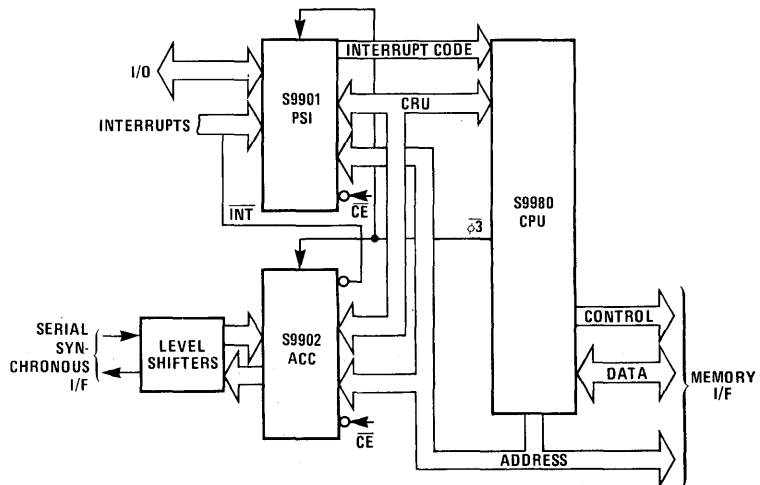
Figure 4. S9902 ACC in an S9900 System

Figure 5. S9902 ACC in an S9980 System

Asynchronous Communication Channel Interface

The interface to the asynchronous communication channel consists of an output control line ($\overline{\text{RTS}}$), two input status lines ($\overline{\text{DSR}}$ and $\overline{\text{CTS}}$), and serial transmit (XOUT) and receive (RIN) data lines. The request-to-send line ($\overline{\text{RTS}}$) is active (low) whenever the transmitter is activated. However, before data transmission begins, the clear-to-send ($\overline{\text{CTS}}$) input must be active. The data set ready ($\overline{\text{DSR}}$) input does not affect the receiver or transmitter. When $\overline{\text{DSR}}$ or $\overline{\text{CTS}}$ changes level, an interrupt is generated.

Interrupt Output

The interrupt output ($\overline{\text{INT}}$) is active (low) when any of the following conditions occurs and the corresponding interrupt has been enabled by the CPU:

(1) $\overline{\text{DSR}}$ or $\overline{\text{CTS}}$ changes levels (DSCH = 1);

(2) a character has been received and stored in the Receiver Buffer Register (RBRL = 1);

(3) the Transmit Buffer Register is empty (XBRE = 1); or

(4) the selected time interval has elapsed (TIMELP = 1).

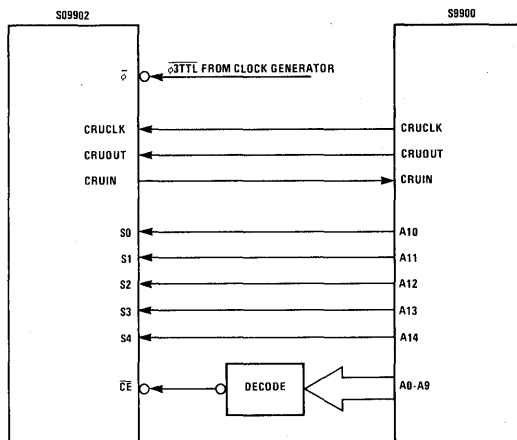The logical relationship of the interrupt output is shown below.

$\overline{\text{INT}}$ Output Generation

Device Operation
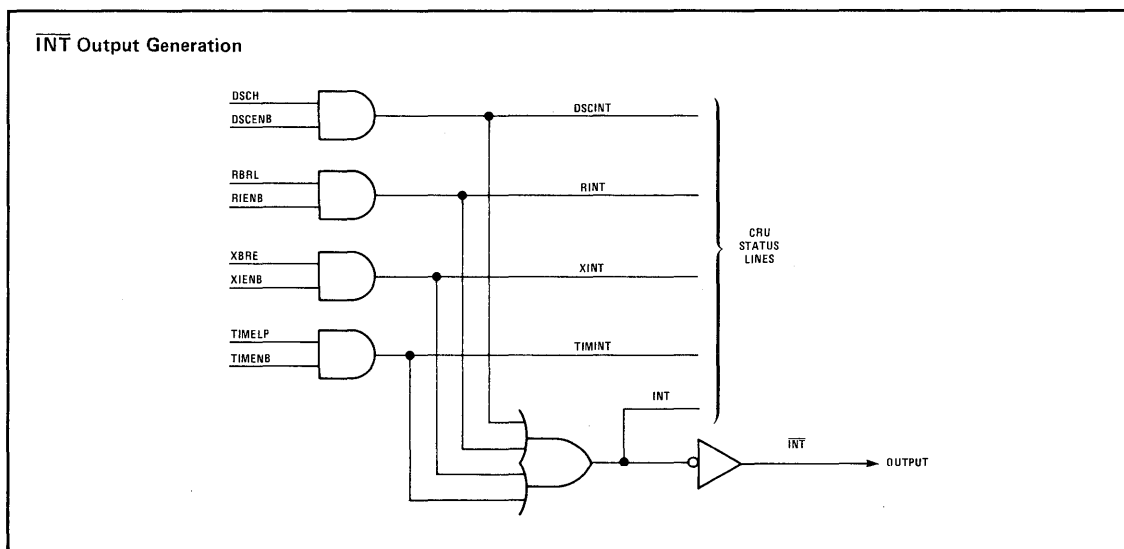
Clock Input

The clock input to the ACC ($\overline{\phi}$) is normally provided by the $\overline{\phi3}$ output of the clock generator (9900 systems) or the S9980 (9980 systems). This clock input is used to generate the internal device clock, which provides the time base for the transmitter, receiver, and interval timer of the ACC.

Control and Data Output

Data and control information is transferred to the ACC using $\overline{\text{CE}}$, S0-S4, CRUOUT, and CRUCLK. The diagrams below show the connection of the ACC to the S9900 and S9980 CPUs. The high-order CPU address lines are used to decode the $\overline{\text{CE}}$ signal when the device is being selected. The low-order address lines are connected to the five address-select lines (S0-S4). Table 2 describes the output bit address assignments for the ACC.

Connection of the ACC to the S9900

```
          S09902                                    S9900

              ø̄ ─o◁── ø̄3TTL FROM CLOCK GENERATOR

        CRUCLK ◁──────────────────────── CRUCLK
        CRUOUT ◁──────────────────────── CRUOUT
        CRUIN  ─────────────────────────▷ CRUIN

            S0 ◁──────────────────────── A10
            S1 ◁──────────────────────── A11
            S2 ◁──────────────────────── A12
            S3 ◁──────────────────────── A13
            S4 ◁──────────────────────── A14

            C̄Ē ─o◁── [ DECODE ] ◁═══ A0-A9
```

Connection of the ACC to the S9980 CPU's

```
          S9902                                     S9980

              ø̄ ─o◁──────────────────o─ ø̄

        CRUCLK ◁──────────────────────── CRUCLK
        CRUOUT ◁──────────────────────── A13
        CRUIN  ─────────────────────────▷ CRUIN

            S0 ◁──────────────────────── A8
            S1 ◁──────────────────────── A9
            S2 ◁──────────────────────── A10
            S3 ◁──────────────────────── A11
            S4 ◁──────────────────────── A12

            C̄Ē ─o◁──o [ DECODE ] ◁═══ A0-A7
```
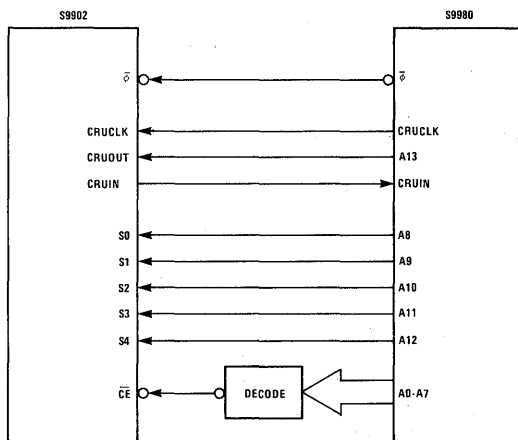
Table 2 S9902 ACC Output Bit Address Assignments

S0	S1	S2	S3	S4	Address$_{10}$	Name	Description
Address$_2$				
1	1	1	1	1	31	RESET	Reset device.
					30-22		Not used.
1	0	1	0	1	21	DSCENB	Data Set Status Change Interrupt Enable.
1	0	1	0	0	20	TIMENB	Timer Interrupt Enable
1	0	0	1	1	19	XBIENB	Transmitter Interrupt Enable
1	0	0	1	0	18	RIENB	Receiver Interrupt Enable
1	0	0	0	1	17	BRKON	Break On
1	0	0	0	0	16	RTSON	Request to Send On
0	1	1	1	1	15	TSTMD	Test Mode
0	1	1	1	0	14	LDCTRL	Load Control Register
0	1	1	0	1	13	LDIR	Load Interval Register
0	1	1	0	0	12	LRDR	Load Receiver Data Rate Register
0	1	0	1	1	11	LXDR	Load Transmit Data Rate Register
					10-0		Control, Interval, Receive Data Rate, Transmit Data Rate, and Transmit Buffer Registers

Bit 31 (RESET) — Writing a one or zero to Bit 31 causes the device to be reset, disabling all interrupts, initializing the transmitter and receiver, setting $\overline{RTS}$ inactive (high), setting all register load control flags (LDCTRL, LDIR, LRDR, and LXDR) to a logic one level, and resetting the BREAK flag. No other input or output operations should be performed for $11\overline{\phi}$ clock cycles after issuing the RESET command.

Bit 30-Bit 22 — Not used.

Bit 21 (DSCENB) — Data Set Change Interrupt Enable. Writing a one to Bit 21 causes the $\overline{INT}$ output to be active (low) whenever DSCH (Data Set Status Change) is a logic one. Writing a zero to Bit 21 causes DSCH interrupts to be disabled. Writing either a one or zero to Bit 21 causes DSCH to be reset.

Bit 20 (TIMENB) — Timer Interrupt Enable. Writing a one to Bit 20 causes the $\overline{INT}$ output to be active whenever TIMELP (Timer Elapsed) is a logic one. Writing a zero to Bit 20 causes TIMELP interrupts to be disabled. Writing either a one or zero to Bit 20 causes TIMELP and TIMERR (Timer Error) to be reset.

Bit 19 (XBIENB) — Transmit Buffer Interrupt Enable. Writing a one to Bit 19 causes the $\overline{INT}$ output to be active whenever XBRE (Transmit Buffer Register Empty) is a logic one. Writing a zero to Bit 19 causes XBRE interrupts to be disabled. The state of XBRE is not affected by writing to Bit 19.

Bit 18 (RIENB) — Receiver Interrupt Enable. Writing a one to Bit 18 causes the $\overline{INT}$ output to be active whenever RBRL (Receiver Buffer Register Loaded) is a logic one. Writing a zero to Bit 18 disables RBRL interrupts. Writing either a one or zero to Bit 18 causes RBRL to be reset.

Bit 17 (BRKON) — Break On. Writing a one to Bit 17 causes the XOUT (Transmitter Serial Data Output) to go to a logic zero whenever the transmitter is active and the Transmit Buffer Register (XBR) and the Transmit Shift Register (XSR) are empty. While BRKON is set, loading of characters into the XBR is inhibited. Writing a zero to Bit 17 causes BRKON to be reset and the transmitter to resume normal operation.

Bit 16 (RTSON) — Request-to-Send On. Writing a one to Bit 16 causes the $\overline{\text{RTS}}$ output to be active (low). Writing a zero to Bit 16 causes $\overline{\text{RTS}}$ to go to a logic one after the XSR and XBR are empty, and BRKON is reset. Thus, the $\overline{\text{RTS}}$ output does not become inactive (high) until after character transmission has been completed.

Bit 15 (TSTMD) — Test Mode. Writing a one to Bit 15 causes $\overline{\text{RTS}}$ to be internally connected to $\overline{\text{CTS}}$, XOUT to be internally connected to RIN, $\overline{\text{DSR}}$ to be internally held low, and the Interval Timer to operate at 32 times its normal rate. Writing a zero to Bit 15 re-enables normal device operation.

Bits 14-11 — Register Load Control Flags. Output Bits 14-11 control which of the five registers will be loaded by writing to Bits 10-0. The flags are prioritized as shown in Table 3.

Table 3 S9902 ACC Register Load Selection

Register Load Control Flag Status				Register Enabled
LDCTRL	LDIR	LRDR	LXDR	
1	X	X	X	Control Register
0	1	X	X	Interval Register
0	0	1	X	Receive Data Rate Register
0	0	X	1	Transmit Data Rate Register
0	0	0	0	Transmit Buffer Register

Bit 14 (LDCTRL) — Load Control Register. Writing a one to Bit 14 causes LDCTRL to be set to a logic one. When LDCTRL = 1, any data written to bits 0-7 are directed to the Control Register. Note that LDCTRL is also set to a logic one when a one or zero is written to Bit 31 (RESET). Writing a zero to Bit 14 causes LDCTRL to be reset to a logic zero, disabling loading of the Control Register. LDCTRL is also automatically reset to a logic zero when a datum is written to Bit 7 of the Control Register which normally occurs as the last bit written when loading the Control Register with a LDCR instruction.

Bit 13 (LDIR) — Load Interval Register. Writing a one to Bit 13 causes LDIR to be set to a logic one. When LDIR = 1 and LDCTRL = 0, any data written to Bits 0-7 are directed to the Interval Register. Note that LDIR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Interval Register loading is not enabled until LDCTRL is set to a logic zero. Writing a zero to Bit 13 causes LDIR to be reset to logic zero, disabling loading of the Internal Register. LDIR is also automatically reset to logic zero when a datum is written to Bit 7 of the Interval Register, which normally occurs as the last bit written when loading the Interval Register with a LDCR instruction.

Bit 12 (LRDR) — Load Receive Data Rate Register. Writing a one to Bit 12 causes LRDR to be set to a logic one. When LRDR = 1, LDIR = 0, and LDCTRL = 0, any data written to Bits 0-10 are directed to the Receive Data Rate Register. Note that LRDR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Receive Data Rate Register loading is not enabled until LDCTRL and LDIR have been set to a logic zero. Writing a zero to Bit 12 causes LRDR to be reset to a logic zero, disabling loading of the Receive Data Rate Register. LRDR is also automatically reset to logic zero when a datum is written to Bit 10 of the Receive Data Rate Register, which normally occurs as the last bit written when loading the Receive Data Rate Register with a LDCR instruction.

Bit 11 (LXDR) —   Load Transmit Data Rate Register. Writing a one to Bit 11 causes LXDR to be set to a logic one. When LXDR = 1, LDIR = 0, and LDCTRL = 0, any data written to Bits 0-10 are directed to the Transmit Data Rate Register. Note that loading of both the Receive and Transmit Data Rate Registers is enabled when LDCTRL = 0, LDIR = 0, LRDR = 1, and LXDR = 1; thus these two registers may be loaded simultaneously when data are received and transmitted at the same rate. LXDR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Transmit Data Rate Register loading is not enabled until LDCTRL and LDIR have been reset to logic zero. Writing a zero to Bit 11 causes LXDR to be reset to logic zero, disabling loading of the Transmit Data Rate Register. Since Bit 11 is the next bit addressed after loading the Transmit Data Rate Register, the register may be loaded and the LXDR flag reset with a single LDCR instruction where 12 bits (Bits 0-11) are written, with a zero written to Bit 11.

Control Register

The Control Register is loaded to select character length, device clock operation, parity, and the number of stop bits for the transmitter. Table 4 shows the bit address assignments for the Control Register.

Table 4 Control Register Bit Address Assignments

Address$_{10}$	Name	Description
7	SBS1	⎫
6	SBS2	⎬ ◄——— Stop Bit Select
5	PENB	Parity Enable
4	PODD	Odd Parity Select
3	CLK4M	ϕ Input Divide Select
2	—	Not Used
1	RCL1	⎫
0	RCL0	⎬ ◄——— Character Length Select

7	6	5	4	3	2	1	0
SBS1	SBS2	PENB	PODD	CLK4M	NOT USED	RCL1	RCL0
MSB							LSB
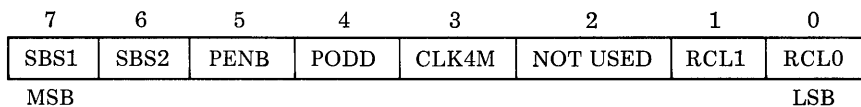
Bits 7 and 6
(SBS1 and SBS2) —   Stop Bit Selection. The number of stop bits to be appended to each transmitter character is selected by Bits 7 and 6 of the Control Register as shown below. The receiver only tests for a single stop bit, regardless of the status of Bits 7 and 6.

SBS1 Bit 7	SBS2 Bit 6	Number of Transmitted Stop Bits
0	0	1½
0	1	2
1	0	1
1	1	1

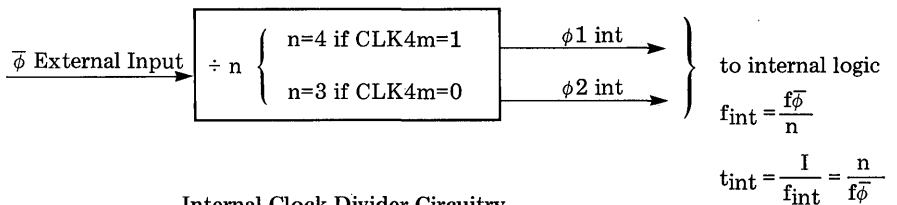Stop Bit Selection

Bits 5 and 4
PENB and PODD) — Parity Selection. The type of parity to be generated for transmission and detected for reception is selected by Bits 5 and 4 of the Control Register as shown below. When parity is enabled (PENB = 1), the parity bit is transmitted and received in addition to the number of bits selected for the character length. Odd parity is such that the total number of ones in the character and parity bit, exclusive of stop bit(s), will be odd. For even parity, the total number of ones will be even.

PENB Bit 5	PODD Bit 4	PARITY
0	0	None
0	1	None
1	0	Even
1	1	Odd

Parity Selection

Bit 3 (CLK4M) — $\overline{\phi}$ Input Divide Select. The $\overline{\phi}$ input to the S9902 ACC is used to generate internal dynamic logic clocking and to establish the time base for the Interval Timer, Transmitter, and Receiver. The $\overline{\phi}$ input is internally divided by either 3 or 4 to generate the two-phase internal clocks required for MOS logic, and to establish the basic internal operating frequency (f_{int}) and internal clock period (t_{int}). When Bit 3 of the Control Register is set to a logic one (CLK4M = 1), $\overline{\phi}$ is internally divided by 4, and when CLK4M = 0, $\overline{\phi}$ is divided by 3. For example, when $f\overline{\phi}$ = 3 MHz, as in a standard 3 MHz S9900 system, and CLK4M = 0, $\overline{\phi}$ is internally divided by 3 to generate an internal clock period t_{int} of $1\mu s$. The figure below shows the operation of the internal clock divider circuitry. The internal clock frequency should be no greater than 1.1 MHz; thus, when $f\overline{\phi} > 3.3$ MHz, CLK4M should be set to a logic one.

$$\overline{\phi}\ \text{External Input} \rightarrow \boxed{\div n \begin{cases} n=4\ \text{if CLK4m=1} \\ n=3\ \text{if CLK4m=0} \end{cases}} \begin{array}{l} \phi 1\ \text{int} \\ \phi 2\ \text{int} \end{array} \rightarrow \text{to internal logic}$$

$$f_{int} = \frac{f\overline{\phi}}{n}$$

$$t_{int} = \frac{I}{f_{int}} = \frac{n}{f\overline{\phi}}$$

Internal Clock Divider Circuitry

Bits 1 and 0
(RCL1 and RCL0) — Character Length Select. The number of data bits in each transmitted and received character is determined by Bits 1 and 0 of the Control Register as shown below.

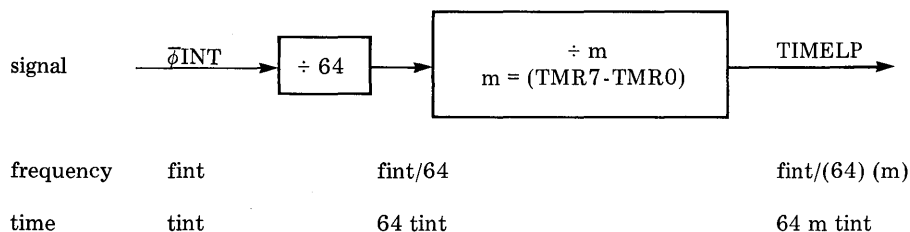| RCL1 Bit 1	RCL0 Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Character Length Selection

Interval Register

The Interval Register is enabled for loading whenever LDCTRL = 0 and LDIR = 1. The Interval Register is used for selecting the rate at which interrupts are generated by the Interval Timer of the ACC. The figure below shows the bit address assignments for the Interval Register when enabled for loading.

7	6	5	4	3	2	1	0
TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0

MSB   LSB
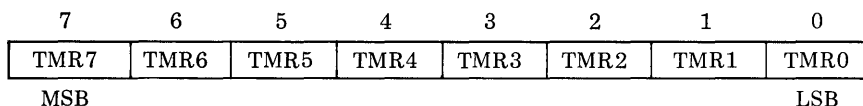
Interval Register Bit Address Assignments

The figure below illustrates the establishment of the interval for the Interval Timer. As an example, if the Interval Register is loaded with a value of 80_{16} (128_{10}) the interval at which Timer Interrupts are generated is $t_{ITVL} = t_{int} \cdot 64 \circ M = (1\mu s)\ (\cdot\ 64)\ (\cdot\ 128) = 8.192$ ms. when $t_{int} = 1\mu s$.

signal $\overline{\phi}INT$ → ÷ 64 → | ÷ m   m = (TMR7-TMR0) | → TIMELP

| frequency | fint | fint/64 | fint/(64) (m) |
| time | tint | 64 tint | 64 m tint |

Time Internal Selection

Receive Data Rate Register

The Receive Data Rate Register is enabled for loading whenever LDCTRL = 0, LDIR = 0, and LRDR = 1. The Receive Data Rate Register is used for selecting the bit rate at which data is received. The diagram shows the bit address assignments for the Receive Data Rate Register when enabled for loading.

10	9	8	7	6	5	4	3	2	1	0
RDV8	RDR9	RDR8	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0

MSB   LSB
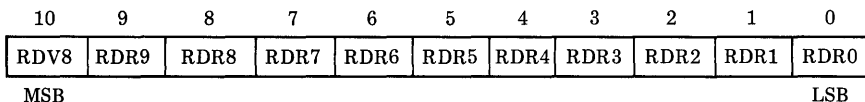
Receive Data Rate Register Bit Address Assignments

The following diagram describes the manner in which the receive data rate is established. Basically, two programmable counters are used to determine the interval for one-half the bit period of receive data. The first counter either divides the internal system clock frequency (f_{int}) by either 8 (RDV8 = 1) or 1 (RDV8 = 0). The second counter has ten stages and may be programmed to divide its input signal by any value from 1 (RDR9-RDR0 = 0000000001) to 1023 (RDR8-RDR0 = 1111111111). The frequency of the output of the second counter (f_{RHBT}) is double the receive-data rate. Register is loaded with a value of 11000111000, RDV8 = 1, and RDR9-RDR0 = 1000111000 = 238_{16} = 568 10. Thus, for f_{int} = 1 MHz, the receive-data rate = 1 X 10^6 ÷ 8 ÷ 568 ÷ 2 = 110.04 bits per second.

| signal	ϕINT $\rightarrow$	$\div$ m m = 8 (RDV8 = 1) or m = 1 (RDV8 = 0)	$\div$ n n = (RDR9-RDR0)	RHBT $\rightarrow$
frequency	fint		$\dfrac{\text{fint}}{\text{m}}$	$\dfrac{\text{fint}}{\text{m} \cdot \text{m}} = f_{RHBT}$

Receive Data Rate Selection
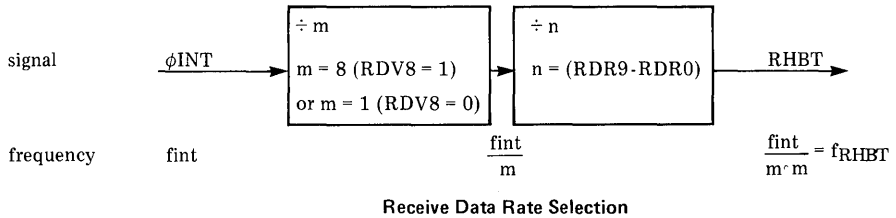
Quantitatively, the receive-data rate f_{RCV} may be described by the following algebraic expression:

$$f_{RCV} = \frac{f_{RHBT}}{2} = \frac{f_{int}}{2mn} = \frac{f_{int}}{(2)(8^{RDV8})(RDR9\text{-}RDR0)}$$

Transmit Data Rate Register

The Transmit Data Rate Register is enabled for loading whenever LDCTRL = 0, LDIR = 0, and LXDR = 1. The Transmit Data Rate Register is used for selecting the data rate for the transmitter. The figure below shows the bit address assignments for the Transmit Data Rate Register.

10	9	8	7	6	5	4	3	2	1	0
XDV8	XDR9	XDR8	XDR7	XDR6	XDR5	XDR4	XDR3	XDR2	XDR1	XDR0

MSB   LSB
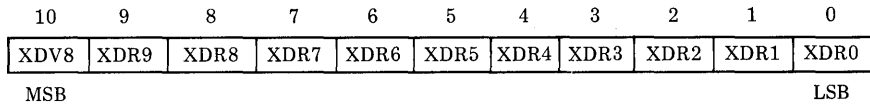
Selection of transmit data rate is accomplished with the Transmit Data Rate Register in the same way that the receive data rate is selected when the Receive Data Rate Register. The algebraic expression for the Transmit Data Rate f_{XMT} is:

$$f_{XMT} = \frac{f_{XHBT}}{2} = \frac{f_{int}}{(2)(8^{XDV8})(XDR9\text{-}XDR0)}$$

For example, if the Transmit Data Rate Register is loaded with a value of 00110100001, XDV8 = 0, and XDR9-XDR0 = $1A1_{16}$ = 417, the transmit data rate = $1 \times 10^{6} \div 2 \div 1 \div 417$ = 1199.04 bits per second.

Transmit Buffer Register

The Transmit Buffer Register is enabled for loading when LDCTRL = 0, LDIR = 0, LRDR = 0, LXDR = 0, and BRKON = 0. The Transmit Buffer Register is used for storage of the next character to be transmitted. When the transmitter is active, the contents of the Transmit Buffer Register are transferred to the Transmit Shift Register each time the previous character has been completely transmitted. The bit address assignments for the Transmit Buffer Register are shown below:

7	6	5	4	3	2	1	0
XBR7	XBR6	XBR5	XBR4	XBR3	XBR2	XBR1	XBR0

MSB   LSB

Transmit Buffer Register Bit Address Assignments

All 8 bits should be transferred into the register, regardless of the selected character length. The extraneous high-order bits will be ignored for transmission purposes; however, loading of bit 7 is internally detected to cause the Transmit Buffer Register Empty (XBRE) status flag to be reset.

Status and Data Input

Status and data information is read from the ACC using $\overline{CE}$, S0-S4, and CRUIN. The following figure illustrates the relationship of the signals used to access data from the ACC. Table 6 describes the input bit address assignments for the ACC.

CE	‾‾‾‾‾‾‾‾‾‾‾|_____|‾‾‾‾
S0 - S4	don't care | n | n + 1 | n + 2 | n + 3 | don't care
CRUIN	Hi - Z | bit n | bit n + 1 | bit n + 2 | bit n + 3 | Hi - Z

Table 5. CRU Output Bit Address Assignments

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET	NOT USED									DSCENB	TIMENB	XBIENB	RIENB	BRKON	RTSON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSTMD	LDCTRL	LDIR	LRDR	LXDR	CONTROL, INTERVAL, RECEIVE DATA RATE, TRANSMIT DATA RATE, AND TRANSMIT BUFFER REGISTERS										

CONTROL REGISTER

14	13	12	11	7	6	5	4	3	2	1	0
1	x	x	x	SBS1	SBS2	PENB	PODD	CLK4M	—	RCL1	RCL0

Stop Bits
00 1-1/2
01 2
1X 1

Party
0X none
10 even
11 odd

$f_{int} = f\overline{\phi}/(3+CLK4M)$

Character Length
00 5
01 6
10 7
11 8

INTERVAL REGISTER

14	13	12	11	7	6	5	4	3	2	1	0
0	1	x	x	TMR7	TMR 6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0

TMR
$T_{ITVL} = t_{int} \times 64 \times TMR$

RECEIVE DATA RATE REGISTER

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	x	RDV8	RDR9	RDR8	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0

RDR
$f_{rcv} = f_{int} \div 8^{RDV8} \div RDR \div 2$

TRANSMIT DATA RATE REGISTER

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	x	1	XDV8	XDR9	XDR8	XDR7	XDR6	XDR5	XDR4	XDR3	XDR2	XDR1	XDR0

XDR
$f_{xmt} = f_{int} \div 8^{XDV8} \div XDR \div 2$

TRANSMIT BUFFER REGISTER

14	13	12	11	7	6	5	4	3	2	1	0
0	0	0	0	XBR7	XBR6	XBR5	XBR4	XBR3	XBR2	XBR1	XBR0

NOTE 1: LOADING OF THE BIT INDICATED BY [ ] CAUSES THE LOAD CONTROL FLAG FOR THAT REGISTER TO BE AUTOMATICALLY RESET.

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Table 6. S9902 ACC Input Bit Address Assignments

S0	Address9 S1	S2	S3	S4	Address10	Name	Description
1	1	1	1	1	31	INT	Interrupt
1	1	1	1	0	30	FLAG	Register Load Control Flag Set
1	1	1	0	1	29	DSCH	Data Set Status Change
1	1	1	0	0	28	CTS	Clear to Send
1	1	0	1	1	27	DSR	Data Set Ready
1	1	0	1	0	26	RTS	Request to Send
1	1	0	0	1	25	TIMELP	Timer Elapsed
1	1	0	0	0	24	TIMERR	Timer Error
1	0	1	1	1	23	XSRE	Transmit Shift Register Empty
1	0	1	1	0	22	XBRE	Transmit Buffer Register Empty
1	0	1	0	1	21	RBRL	Receive Buffer Register Loaded
1	0	1	0	0	20	DSCINT	Data Set Status Charge Interrupt (DSCH · DSCENB)
1	0	0	1	1	19	TIMINT	Timer Interrupt (TIMELP · TIMENB)
1	0	0	1	0	18	—	Not used (always = 0)
1	0	0	0	1	17	XBINT	Transmitter Interrupt (XBRE · XBIENB)
1	0	0	0	0	16	RBINT	Receiver Interrupt (RBRL · RIENB)
0	1	1	1	1	15	RIN	Receive Input
0	1	1	1	0	14	RSBD	Receive Start Bit Detect
0	1	1	0	1	13	RFBD	Receive Full Bit Detect
0	1	1	0	0	12	RFER	Receive Framing Error
0	1	0	1	1	11	ROVER	Receive Overrun Error
0	1	0	1	0	10	RPER	Receive Parity Error
0	1	0	0	1	9	RCVERR	Receive Error
0	1	0	0	0	8	—	Not used (always = 0)
					7-0	RBR7-RBR0	Receive Buffer Register (Received Data)

Bit 31 (INT) — INT = DSCINT + TIMINT + XBINT + RBINT. The interrupt output ($\overline{INT}$) is active when this status signal is a logic 1.

Bit 30 (FLAG) — FLAG = LDCTRL + LDIR + LRDR + LXDR + BRKON. When any of the register load control flags or BRKON is set, FLAG = 1.

Bit 29 (DSCH) — Data Set Status Change Enable. DSCH is set when the $\overline{DSR}$ or $\overline{CTS}$ input changes state. To ensure recognition of the state change, $\overline{DSR}$ or $\overline{CTS}$ must remain stable in its new state for a minimum of two internal clock cycles. DSCH is reset by an output to bit 21 (DSCENB).

Bit 28 (CTS) — Clear to Send. The CTS signal indicates the inverted status of the $\overline{CTS}$ device input.

Bit 27 (DSR) — Data Set Ready. The DSR signal indicates the inverted status of the $\overline{DSR}$ device input.

Bit 26 (RTS) — Request to Send. The RTS signal indicates the inverted status of the $\overline{RTS}$ device output.

Bit 25 (TIMELP) — Timer Elapsed. TIMELP is set each time the Interval Timer decrements to 0. TIMELP is reset by an output to bit 20 (TIMENB).

Bit 24 (TIMERR) — Timer Error. TIMERR is set whenever the Interval timer decrements to 0 and TIMELP is already set, indicating that the occurrence of TIMELP was not recognized and cleared by the CPU before subsequent intervals elapsed. TIMERR is reset by an output to bit 20 (TIMENB).

Bit 23 (XSRE) — Transmit Shift Register Empty. When XSRE = 1, no data is currently being transmitted and the XOUT output is at logic 1 unless BRKON is set. When XSRE = 0, transmission of data is in progress.

Bit 22 (XBRE) — Transmit Buffer Register Empty. When XBRE = 1, the transmit buffer register does not contain the next character to be transmitted. XBRE is set each time the contents of the transmit buffer register are transferred to the transmit shift register, XBRE is reset by an output to bit 7 of the transmit buffer register (XBR7), indicating that a character has been loaded.

Bit 21 (RBRL) — Receive Buffer Register Loaded. RBRL is set when a complete character has been assembled in the receive shift register and the character is transferred to the receive buffer register. RBRL is reset by an output to bit 18 (RIENB).

Bit 20 (DSCINT) — Data Set Status Change Interrupt. DSCINT = DSCH (input bit 29) · DSCENB (output bit 21). DSCINT indicates the presence of an enabled interrupt caused by the changing of state of $\overline{DSR}$ or $\overline{CTS}$.

Bit 19 (TIMINT) — Timer Interrupt. TIMINT = TIMELP (input bit 25) · TIMENB (output bit 20). TIMINT indicates the presence of an enabled interrupt caused by the interval timer.

Bit 17 (XBINT) — Transmitter Interrupt. XBINT = XBRE (input bit 22) · XBIENB (output bit 19). XBINT indicates the presence of an enabled interrupt caused by the transmitter.

Bit 16 (RBINT) — Receiver Interrupt. RBINT = RBRL (input bit 21) · RIENB (output bit 18). RBINT indicates the presence of an enabled interrupt caused by the receiver.

Bit 15 (RIN) — Receive Input. RIN indicates the status of the RIN input to the device.

Bit 14 (RSBD) — Receive Start Bit Detect. RSBD is set one-half bit time after the 1-to-0 transition of RIN indicating the start bit of a character. If RIN is not still 0 at this point in time, RSBD is reset. Otherwise, RSBD remains true until the complete character has been received. This bit is normally used for testing purposes.

Bit 13 (RFBD) — Receive Full Bit Detect. RFBD is set one bit time after RSBD is set to indicate the sample point for the first data bit of the received character. RSBD is reset when the character has been completely received. This bit is normally used for testing purposes.

Bit 12 (RFER) — Receive Framing Error. RFER is set when a character is received in which the stop bit, which should be a logic 1, is a logic 0. RFER should only be read when RBRL (input bit 21) is a 1. RFER is reset when a character with the correct stop bit is received.

Bit 11 (ROVER) — Receive Overrun Error. ROVER is set when a new character is received before the RBRL flag (input bit 21) is reset, indicating that the CPU failed to read the previous character and reset RBRL before the present character is completely received. ROVER is reset when a character is received and RBRL is 0 when the character is transferred to the receive buffer register.

Bit 10 (RPER) — Receive Parity Error. RPER is set when a character is received in which the parity is incorrect. RPER is reset when a character with correct parity is received.

Bit 9 (RCVERR) — Receive Error. RCVERR = RFER + ROVER + RPER. RCVERR indicates the presence of an error in the most recently received character.

Bit 7-Bit 0 (RBR7-RBR0) — Receive Buffer Register. The receive buffer register contains the most recently received character. For character lengths of fewer than 8 bits the character is right justified, with unused most significant bit(s) all zero(es). The presence of valid data in the receive buffer register is indicated when RBRL is a logic 1.

Transmitter Operation

Transmitter Initialization

The operation of the transmitter is described in the following flowchart. The transmitter is initialized by issuing the RESET command (output to bit 31), which causes the internal signals XSRE and XBRE to be set, and BRKON to be reset. Device outputs $\overline{RTS}$ and XOUT are set, placing the transmitter in its idle state. When RTSON is set by the CPU, the $\overline{RTS}$ output becomes active and the transmitter becomes active when $\overline{CTS}$ goes low.

Data Transmission

If the Transmit Buffer Register contains a character, transmission begins. The contents of the Transmit Buffer Register are transferred to the Transmit Shift Register, causing XSRE to be reset and XBRE to be set. The first bit transmitted (start bit) is always a logic 0. Subsequently, the character is shifted out, LSB first. Only the number of bits specified by RCL1 and RCL0 (character length select) of the Control Register are shifted. If parity is enabled, the correct parity bit is next transmitted. Finally the stop bit(s) selected by SBS1 and SBS0 of the Control Register are transmitted. Stop bits are always logic one. XSRE is set to indicate that no transmission is in progress, and the transmitter again tests XBRE to determine if the CPU has yet loaded the next character. The waveform for a transmitted character is shown below.

```
                                              PARITY    STOP
                    |START|                   | BIT |   BIT(S)
                    | BIT |   TRANSMITTED CHARACTER           |
              1  ___         _____                        _____
    XOUT          |   |LSB |LSB+1|             |MSB|
              0       |___|_____|_____|___|    |     |
    NUMBER         |     |                        |     |     |
    OF BITS        |  1  |        5, 6, 7, OR 8    |0 OR 1| 1, 1-1/2, OR 2|

          t  ———————▶
              TRANSMITTED CHARACTER WAVEFORM
```
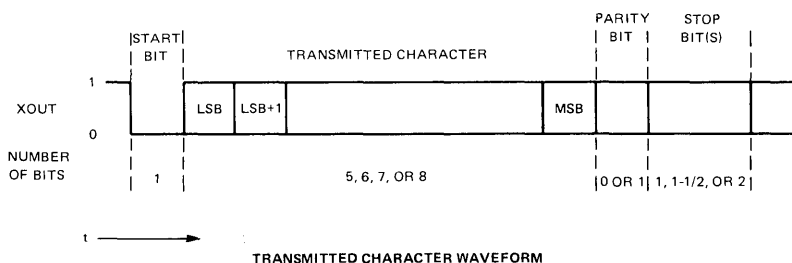
BREAK Transmission

The BREAK message is transmitted only if XBRE = 1, $\overline{CTS}$ = 9, and BRKON = 1. After transmission of the BREAK message begins, loading of the Transmit Buffer Register is inhibited and XOUT is reset. When BRKON is reset by the CPU, XOUT is set and normal operation continues. It is important to note that characters loaded into the Transmit Buffer Register are transmitted prior to the BREAK message regardless of whether the character has been loaded into the Transmit Shift Register before BRKON is set. Any character to be transmitted subsequent to transmission

of the BREAK message may not be loaded into the Transmit Buffer Regiser until after BRKON is reset.

Transmission Termination

Whenever XSRE = 1 and BRKON = 0, the transmitter is idle, with XOUT set to one. If RTSON is reset at this time, the $\overline{RTS}$ device output will go inactive, disabling further data transmission until RTSON is again set. $\overline{RTS}$ will not go inactive, however, until any characters loaded into the Transmit Buffer Register prior to resetting RTSON are transmitted and BRKON = 0.

S9902 Transmitter Operation
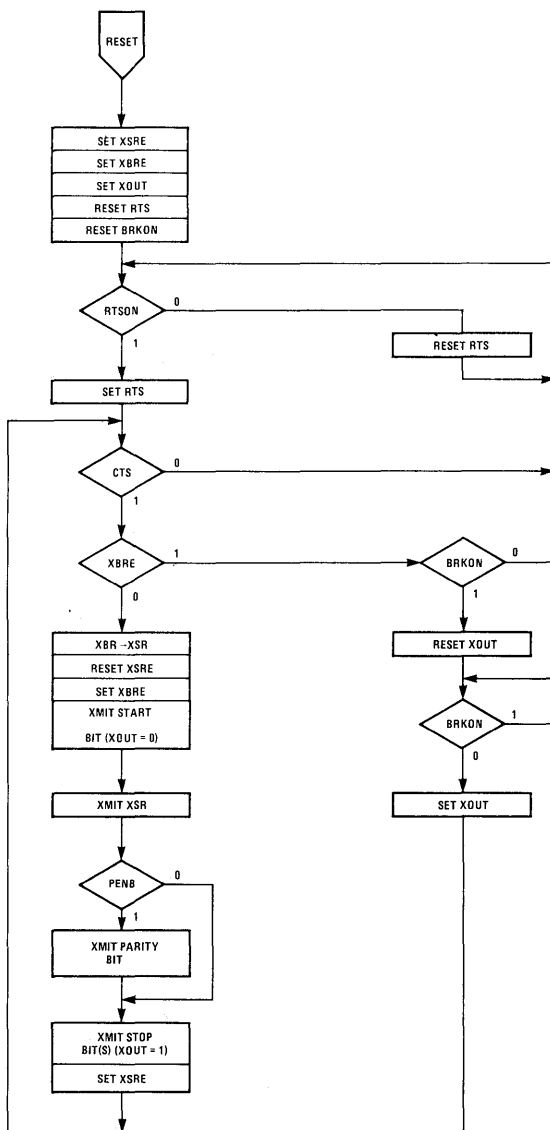
Receiver Operation

Receiver Initialization

Operation of the S9902 receiver is described in the following flowchart. The receiver is initialized any time the CPU issues the RESET command. The RBRL flag is reset to indicate that no character is currently in the Receive Buffer Register, and the RSBD and RFBD flags are reset. The receiver remains in the inactive state until a 1 to 0 transition is detected on the RIN device input.

Start Bit Detection

The receiver delays one-half bit time and again samples RIN to ensure that a valid start bit has been detected. If RIN = 0 after the half-bit delay, RSBD is set and data reception begins. If RIN = 1 no data reception occurs.

S9902 Receiver Operation
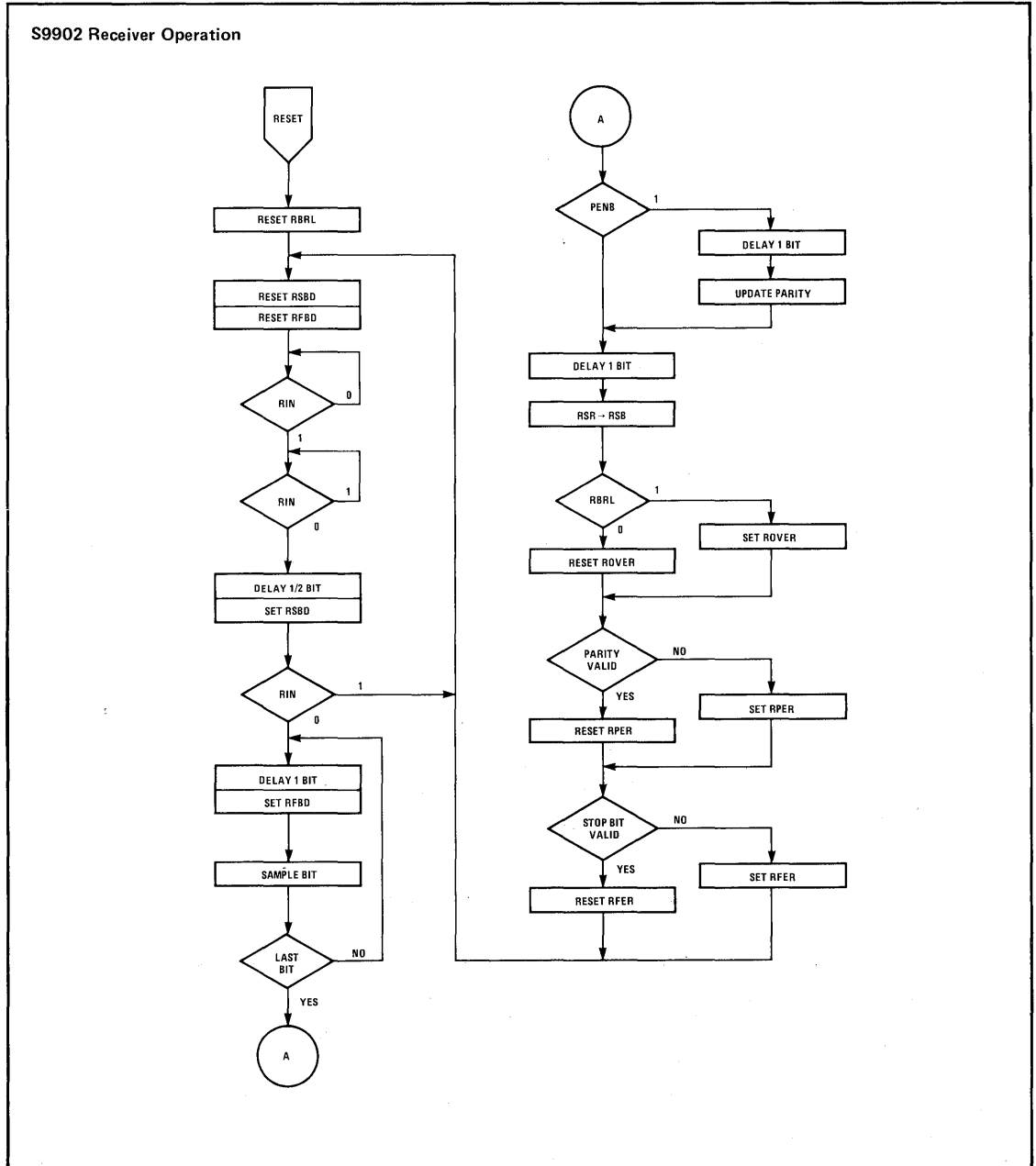
Data Reception

In addition to verifying the valid start bit, the half-bit delay after the 1-to-0 transition also establishes the sample point for all subsequent data bits in this character. Theoretically, the sample point is in the center of each bit cell, thus maximizing the limits of acceptable distortion of data cells. After the first full bit delay, the least significant data bit is received and RFBD is set. The receiver continues to delay one-bit intervals and sample RIN until the selected number of bits is received. If parity is enabled, one additional bit

is read for parity. After an additional bit delay, the received character is transferred to the Receive Buffer Register, RBRL is set, ROVER and RPER are loaded with appropriate values, and RIN is tested for a valid stop bit. If RIN = 1, the stop bit is valid. RFER, RSBD, and RFBD are reset and the receiver waits for the next start bit to begin reception of the next character.

If RIN = 0 when the stop bit is sampled, RFER is set to indicate the occurrence of a framing error. RSBD and RFBD are reset but sampling for the start bit of the next character does not begin until RIN = 1.

CHARACTER RECEPTION TIMING
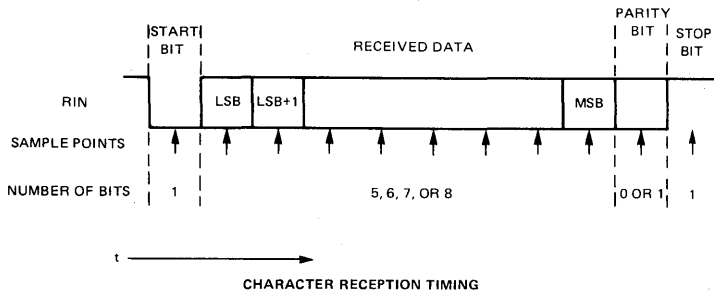
Interval Timer Operation

A flowchart of the operation of the Interval Timer is shown below. Execution of the RESET command by the CPU causes TIMELP and TIMERR to be reset and LDIR to be set. Resetting LDIR causes the contents of the Interval Register to be loaded into the Interval Timer, thus beginning the selected time interval. The timer is decremented every 64 internal clock cycles (every 2 internal clock cycles when in Test Mode) until it reaches zero, at which time the Interval Timer is reloaded by the Interval Register and TIMELP is set. If TIMELP was already set, TIMERR is set to indicate that TIMELP was not cleared by the CPU before the next time period elapsed. Each time LDIR is reset the contents of the Interval Register are loaded into the Interval Timer, thus restarting the time.

Interval Timer Operation
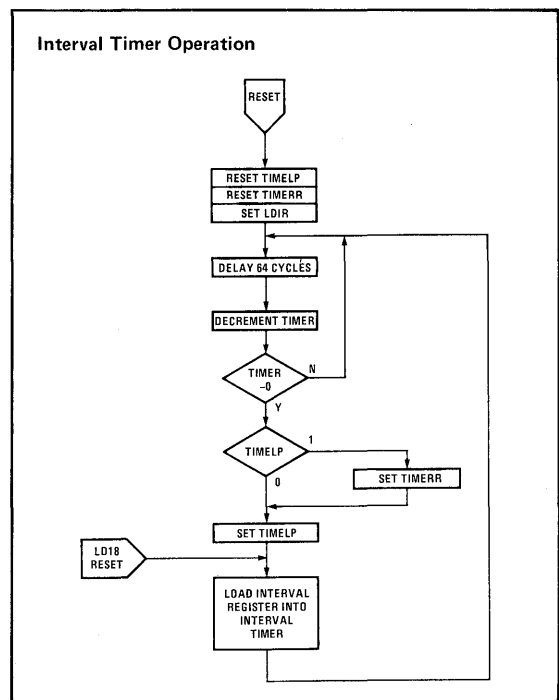
Device Application

This section describes the software interface between the CPU and the S9902 ACC and discusses some of the design considerations in the use of this device in asynchronous communications applications.

Device Initialization

The ACC is initialized by the CPU issuing the RESET command, followed by loading the Control, Interval, Receive Data Rate, and Trasmit Data Rate registers. Assume that the value to be loaded into the CRU Base Register (register 12) in order to point to bit 0 is 0040_{16}. In this application, characters will have 7 bits of data plus even parity and one stop bit. The ϕ input to the ACC is a 3MHz signal. The ACC will divide this signal frequency by 3 to generate an internal clock frequency of 1MHz. An interrupt will be generated by the Interval Timer every 1.6 milliseconds when timer interrupts are enabled. The transmitter will operate at a data rate of 300 bits per second and the receiver will operate at 1200 bits per second.

Had it been desired that both the transmitter and receiver operate at 300 bits per second, the "LDCR @RDR,11" instruction would have been deleted, and the "LDCR @XDR,12" instruction would have caused both data rate registers to be loaded and LRDR and LXDR to have been reset.

Initialization Program

The initialization program for the configuration previously described is as shown below. The RESET command disables all interrupts, initializes all controllers, sets the four register load control flags (LDCTRL, LDIR, LRDR, and LXDR). Loading the last bits of each of the registers causes the load control flag to be automatically reset.

```
        LI      R12, >40        INITIALIZE CRU BASE
        SBO     31              RESET COMMAND
        LDCR    @CNTRL, 8       LOAD CONTROL AND RESET LDCTRL
        LDCR    @INTVL, 8       LOAD INTERVAL AND RESET LDIR
        LDCR    @RDR, 11        LOAD RDR AND RESET LRDR
        LDCR    @XDR, 12        LOAD XDR AND RESET LXDR
                •
                •
                •
CNTRL   BYTE    >A2
INTVL   BYTE    1600/64
RDR     DATA    >1A1
XDR     DATA    >4DO
```

The RESET command initializes all subcontrollers, disables interrupts, and sets LDCTRL, LDIR, LRDR, and LXDR, enabling loading of the control register.

Control Register

The options described previously are selected by loading the value shown below.

5.64
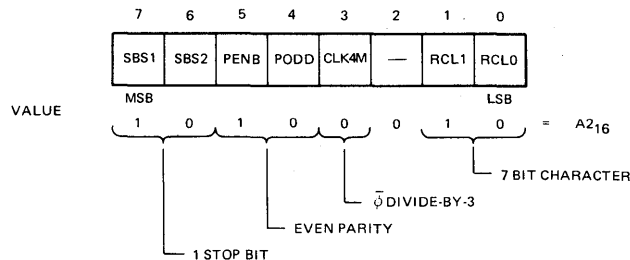
Interval Register

The interval register is to be set up to generate an interrupt every 1.6 milliseconds. The value loaded into the interval register specifies the number of 64 microsecond increments in the total interval.

7	6	5	4	3	2	1	0
TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
0	0	0	1	1	0	0	1
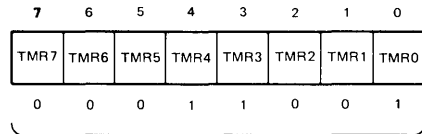
$19_{16} = 25_{10}$

25 X 64 MICROSECONDS = 1.6 MILLISECONDS

Receive Data Rate Register

The data rate for the receiver is to be 1200 bits per second. The value to be loaded into the Receive Data Rate Register is as shown:

10	9	8	7	6	5	4	3	2	1	0
RDV8	RDR9	RDR8	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
0	0	1	1	0	1	0	0	0	0	1
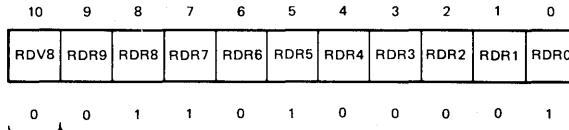
$_8RDV8 = 1$

$1A1_{16} = 417_{10}$

$10^6 \div 1 \div 417 \div 2 = 1199.04$ BITS PER SECOND

Transmit Data Rate Register

The data rate for the transmitter is to be 300 bits per second. The value to be loaded into the Transmit Data Rate Register is:

10	9	8	7	6	5	4	3	2	1	0
XDV8	XDR9	XDR8	XDR7	XDR6	XDR5	XDR4	XDR3	XDR2	XDR1	XDR0
1	0	0	1	1	0	1	0	0	0	0
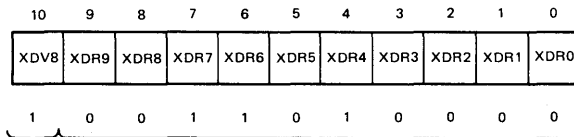
$_8XDV8 = 8$

$DO_{16} = 208$

$1 \times 10^6 \div 8 \div 208 \div 2 = 300.48$ BITS PER SECOND

Data Transmission

The subroutine shown below demonstrates a simple loop for the transmitting of a block of data.

```
        LI      R0, LISTAD      INITIALIZE LIST POINTER
        LI      R1, COUNT       INITIALIZE BLOCK COUNT
        LI      R12, CRUBAS     INITIALIZE CRU BASE
        SBO     16              TURN OFF TRANSMITTER
XMTLP   TB      22              WAIT FOR XBRE = 1
        JNE     XMTLP
        LDCR    *R0+,8          LOAD CHARACTER INCREMENT POINTER RESET XBRE
        DEC     R1              DECREMENT COUNT
        JNE     XMTLP           LOOP IF NOT COMPLETE
        SBZ     16              TURN OFF TRANSMITTER
```

After initializing the list pointer, block count, and CRU base address. RTSON is set to cause the transmitter and the RTS output to become active. Data transmission does not begin, however, until the CTS input becomes active. After the final character is loaded into the transmit buffer register, RTSON is reset. The transmitter and the RTS output do not become inactive until the final character has been completely transmitted.

Data Reception

The software shown below will cause a block of data to be received and stored in memory.

```
CARRET  BYTE    >OD
RCVBLK  LI      R2, RCVLST      INITIALIZE LIST COUNT
        LI      R3, MXRCNT      INITIALIZE MAX COUNT
        LI      R4, CARRET      SET UP END OF BLOCK CHARACTER
RCVLP   TB      21              WAIT FOR RBRL = 1
        JNE     RCVLP
        STCR    *R2,8           STORE CHARACTER
        SBZ     18              RESET RBRL
        DEC     R3              DECREMENT COUNT
        JEQ     RCVEND          END IF COUNT = 0
        CB      *R2+, R4        COMPARE TO EOB CHARACTER, INCREMENT POINTER
        JNE     RCVLP           LOOP IF NOT COMPLETE
RCVEND  RT                      END OF SUBROUTINE
```

Register Loading After Initialization

The control, interval, and data rate registers may be reloaded after initialization. For example, it may be desirable to change the interval of the timer. Assume, for sample, that the interval is to be changed to 10.24 milliseconds. The instruction sequence is as follows:

```
        SB0     13              SET LOAD CONTROL FLAG
        LDCR    @INTVL2,8       LOAD REGISTER, RESET FLAG
          •
          •
          •
INTVL2  BYTE    10240/64
```

Caution should be exercised when transmitter interrupts are enabled to ensure that the transmitter interrupt does not occur while the load control flag is set. For example, if the transmitter interrupts between execution of the "SBO 13" and the next instruction, the transmit buffer is not enabled for loading when the transmitter interrupt service routine is entered because the LDIR flag is set. This situation may be avoided by the following sequence:

```
          BLWP     @INTVCHG         CALL SUBROUTINE
            •
            •
            •
ITV CPC   LI MI    0                MASK ALL INTERRUPTS
          MOV      @24(R13), RIZ    LOAD CRU BASE ADDRESS
          SB0      13               SET FLAG
          LDCR     @INTVL2,8        LOAD REGISTER AND RESET FLAG
          RTWP                      RESTORE MASK AND RETURN
            •
            •
            •

ITVCHG    DATA     ACCWP, ITVCPC
INTVL2    BYTE     10240/64
```

In this case all interrupts are masked, ensuring that all interrupts are disabled while the load control flag is set.

Mechanical Data

18-Pin Plastic Dual-in-Line Package	18-Pin Ceramic Dual-in-Line Package

AMI ®
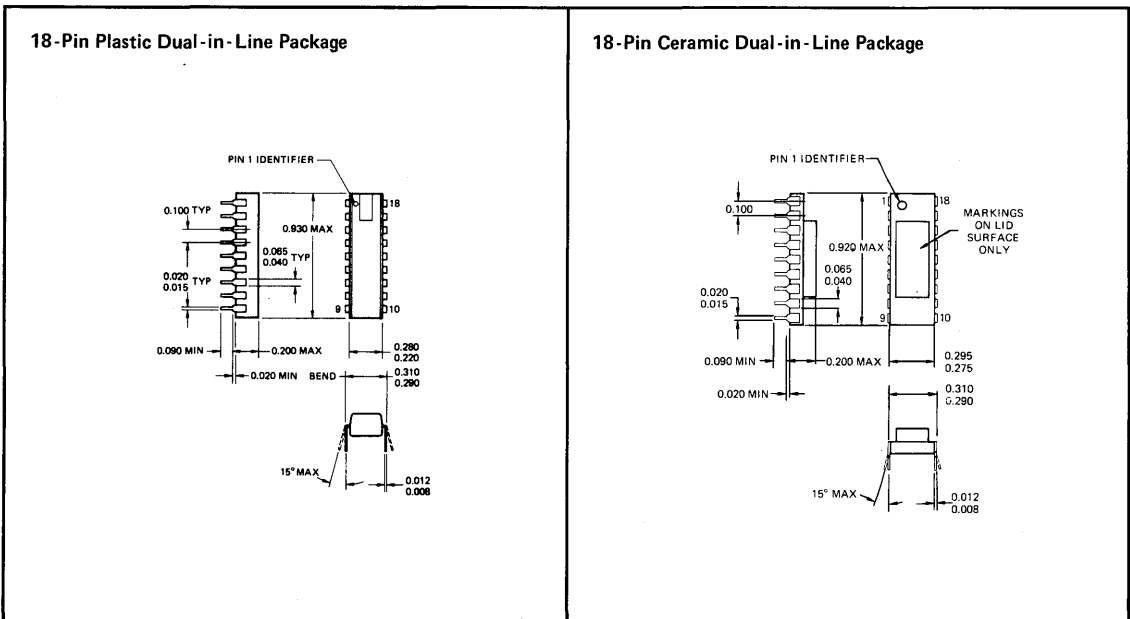
SYNCHRONOUS COMMUNICATIONS CONTROLLER

Features

- ☐ Versatile CRU interface to synchronous and asynchronous serial devices for the S99XX series of microprocessors
- ☐ DC to 250 KBPS data rate, half- or full-duplex
- ☐ Dynamic character length selection
- ☐ Line protocols include BI-SYNC, SDLC, and HDLC, as well as others
- ☐ Programmable-polynominal CRC generation and detection
- ☐ Interface to unclocked or NRZI data with 32x clocks
- ☐ Two programmable sync registers
- ☐ Interval timer [64μs to 16.32ms] on chip
- ☐ Automatic zero insert and delete for SDLC and HDLC
- ☐ Single +5V supply, 20-pin DIP, all inputs and outputs TTL compatible
- ☐ N-channel Silicon-Gate technology

General Description

The S9903 is a versatile device which provides the system designer with a wide range of capabilities in synchronous and asynchronous communications control. The S9903 operates in a multi-mode configuration that allows a broad range in the degree of active participation required in the control of high-speed serial communications. Most synchronous data-link control protocols can be supported through software control of sync and fill characters, timing, CRC generation and detection, etc. Established protocols such as BI-SYNC, SDLC, and HDLC are implemented directly in hardware, with others implemented through various combinations of hardware and software.

Universal applicability is further assured through the capability for dynamic character length selection from 5- to 9-bit data words plus parity. Definition and operation of all communications control is under software control and as such make upgrading to another protocol simply a matter of changing software with no hardware changes required.

Block Diagram

Pin Configuration

AMI®
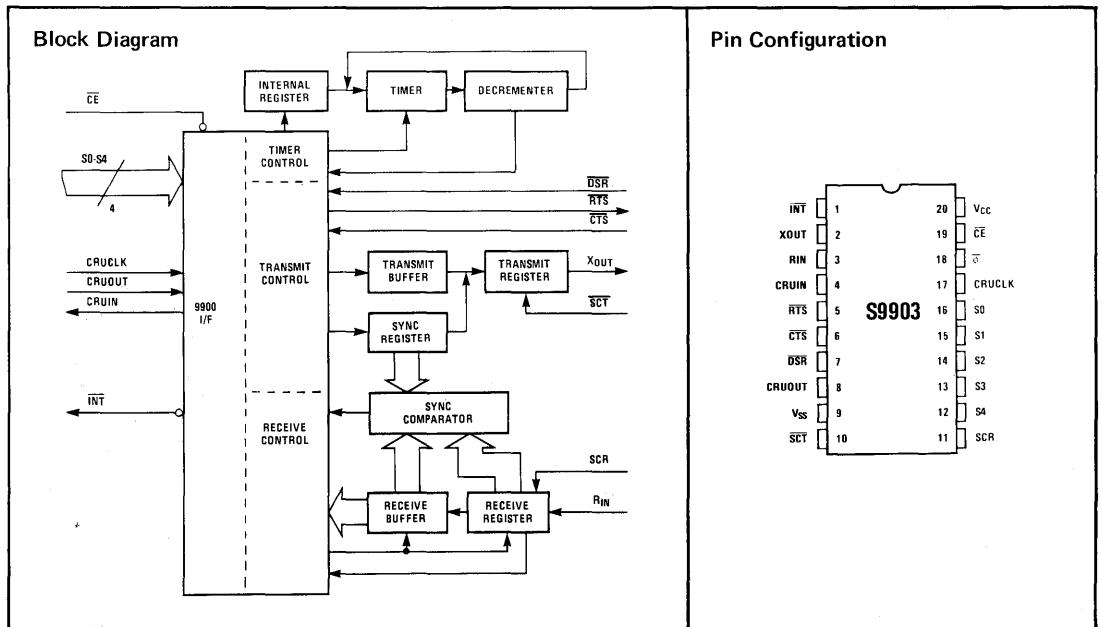
MICROPROCESSOR

Features

- ☐ **16-Bit Instruction Word**
- ☐ **Minicomputer Instruction Set Including Multiply and Divide**
- ☐ **2048 Bytes of ROM on Chip**
- ☐ **128 Bytes of RAM on Chip**
- ☐ **16 General Purpose Registers**
- ☐ **4 Prioritized Interrupts**
- ☐ **On Chip Timer/Event Counter**
- ☐ **32 Bits General Purpose I/O**
- ☐ **256 Bits I/O Expansion**
- ☐ **Multiprocessor System Interface**
- ☐ **Single 5 Volt Power Supply**
- ☐ **Power Down Capability for Low Stand-by Power**
- ☐ **N-Channel Silicon Gate MOS**

General Description

The S9940 is a single-chip, 16-bit microcomputer containing a CPU, memory (RAM and ROM), and extensive I/O. The instruction set of the S9940 is a subset of the S9900 instruction set and includes capabilities offered by minicomputers. The unique memory-to-memory architecture features multiple register files, resident in the RAM, which allow faster response to interrupts, and increased programming flexibility. The memory consists of 128 bytes of RAM and 2048 bytes of ROM. The S9940 implements four levels of interrupts, including an internal decrementer which can be programmed as a timer or an event counter. All members of the S9900 family of peripheral circuits are compatible with the S9940.
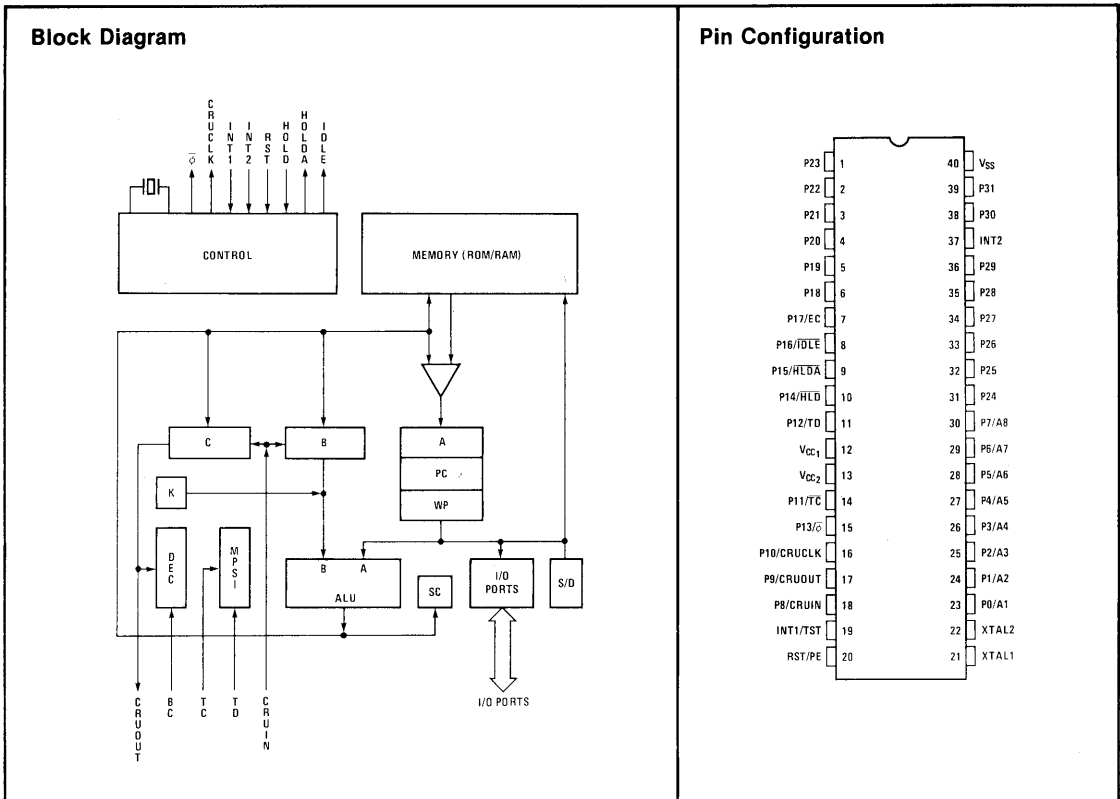
Block Diagram

Pin Configuration

P23	1	40	Vss
P22	2	39	P31
P21	3	38	P30
P20	4	37	INT2
P19	5	36	P29
P18	6	35	P28
P17/EC	7	34	P27
P16/IDLE	8	33	P26
P15/HLDA	9	32	P25
P14/HLD	10	31	P24
P12/TD	11	30	P7/A8
Vcc1	12	29	P6/A7
Vcc2	13	28	P5/A6
P11/TC	14	27	P4/A5
P13/φ	15	26	P3/A4
P10/CRUCLK	16	25	P2/A3
P9/CRUOUT	17	24	P1/A2
P8/CRUIN	18	23	P0/A1
INT1/TST	19	22	XTAL2
RST/PE	20	21	XTAL1

S9900

AMI ®

16-BIT MICROPROCESSOR

Features

☐ 16-Bit Instruction Word
☐ Full Minicomputer Instruction Set Capability Including Multiply and Divide
☐ Up to 16,384 Bytes of Memory
☐ 8-Bit Memory Data Bus
☐ Advanced Memory-to-Memory Architecture
☐ Separate Memory, I/O, and Interrupt-Bus Structures
☐ 16 General Registers
☐ 4 Prioritized Interrupts
☐ Programmed and DMA I/O Capability
☐ On-Chip 4-Phase Clock Generator
☐ 40-Pin Package
☐ N-Channel Silicon-Gate Technology

The S9980A and the S9981 although very similar, have several differences which are:

1. The S9980A requires a V_{BB} supply (pin 21) while the S9981 has an internal charge pump to generate V_{BB} from V_{CC} and V_{DD}.

2. The S9981 has an optional on-chip crystal oscillator in addition to the external clock mode of the S9980A.

3. The pin-outs are not compatible for D0-D7, INT0-INT2, and $\overline{\phi}3$.

Description

The S9980A/S9981 is a software-compatible member of AMI's 9900 family of microprocessors. Designed to minimize the system cost for smaller systems, the S9980A/S9981 is a single-chip 16-bit central processing unit (CPU) which has an 8-bit data bus, on-chip clock, and is packaged in a 40-pin package (see Figure 1). The instruction set of the S9980A/S9981 includes the capabilities offered by full minicomputers and is exactly the same as the 9900's. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort.

Block Diagram

Pin Configuration

			9980A	9981
$\overline{HOLD}$	1	40	$\overline{MEMEN}$	$\overline{MEMEN}$
HOLDA	2	39	READY	READY
IAQ	3	38	$\overline{WE}$	$\overline{WE}$
A13/CRUOUT	4	37	CRUCLK	CRUCLK
A12	5	36	V_{DD}	V_{DD}
A11	6	35	V_{SS}	V_{SS}
A10	7	34	CKIN	CKIN
A9	8	33	D7	OSCOUT
A8	9	32	D6	D7
A7	10	31	D5	D6
A6	11	30	D4	D5
A5	12	29	D3	D4
A4	13	28	D2	D3
A3	14	27	D1	D2
A2	15	26	D0	D1
A1	16	25	INT 0	D0
A0	17	24	INT 1	INT 0
DBIN	18	23	INT 2	INT 1
CRUIN	19	22	$\overline{\phi}3$	INT 2
V_{SS}	20	21	V_{BB}	$\phi3$

AMI ®

Telecommunications
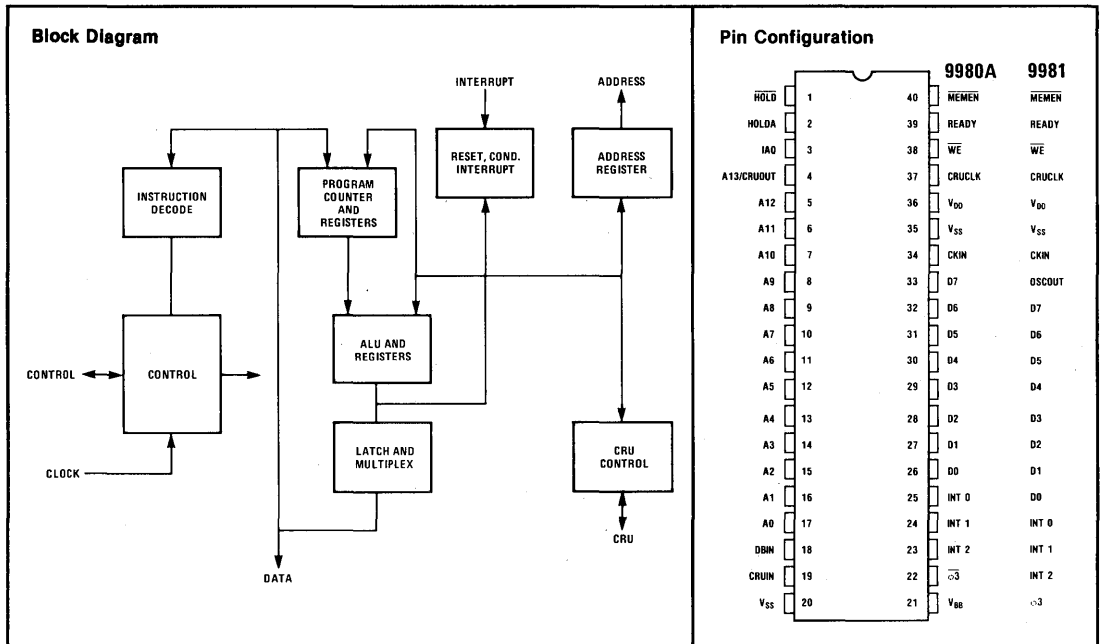
TELECOMMUNICATIONS

PART NO.	DESCRIPTION	PROCESS	POWER SUPPLIES	INPUT/OUTPUT	PACKAGES
S1883	Universal Asynchronous Receiver/Transmitter (UART)	P-I^2	$-12V, \pm 5V$	TTL	40 Pin
S2350	Universal Synchronous Receiver/Transmitter (USRT)	N-SiGate	$+5V$	TTL	40 Pin
S2559A/B	Digital Tone Generator	CMOS	$+3.5V$ to $+13V$	TTL/CMOS	16 Pin
S2559C/D	Digital Tone Generator	CMOS	$+2.75$ to $+10V$	TTL/CMOS	16 Pin
S2560A/B	Key Pulser	CMOS	$+12V$		18 Pin
S2561	Tone Ringer	CMOS	$+13.5V$	.	18 Pin
S2562	Repertory Dialer	CMOS			40 Pin

DIGITAL
TONE GENERATOR

Features

- [ ] Wide Operating Supply Voltage Range: 3.5 to 13 Volts (A, B) 2.75 to 10 Volts (C, D)
- [ ] Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V.
- [ ] Uses TV Crystal Standard (3.58MHz to Derive all Frequencies thus Providing Very High Accuracy and Stability
- [ ] MUTE and Transmitter Drivers On Chip
- [ ] Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- [ ] The Total Harmonic Distortion is Below Industry Specification
- [ ] On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range
- [ ] Dual Tone as well as Single Tone Capability
- [ ] Four Options Available:
  A: 3.5 to 13V Mode Select
  B: 3.5 to 13V Chip Disable
  C: 2.75 to 10V Mode Select
  D: 2.75 to 10V Chip Disable

General Description

The S2559 Digital Tone Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton telephone keyboard or calculator type X-Y keyboard and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2559 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, Point-of-Sale, and Credit Card Verification Terminals and process control.

Block Diagram
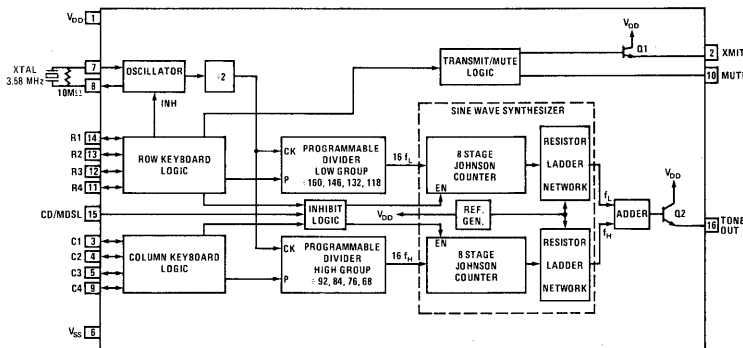
Pin Configuration
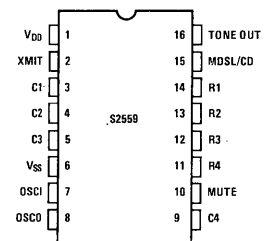
Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$) S2559 A, B .... +13.5V
DC Supply Voltage ($V_{DD} - V_{SS}$) S2559 C, D .... +10.5V
Operating Temperature .... −25°C to +70°C
Storage Temperature .... −55°C to +125°C
Power Dissipation at 25°C 500mW
Input Voltage .... $-0.6 \leqslant V_{in} \leqslant V_{DD} + 0.6$

S2559A & B Electrical Characteristics (Specifications apply over the operating temperature range of −25°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		(V_{DD}–V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode with One Valid Key Depressed			3.5		13.0	V
V_{DD}	Non Tone Out Mode (No Keys Depressed)			2.5		13.0	V
	Supply Current						
I_{DD}	Standby (No Keys Selected, Tone, MUTE and XMIT Outputs Unloaded)		13.0			130	μA
I_{OD}	Operating (One Key Selected, Tone, MUTE and XMIT Outputs Unloaded)		5.0			18	mA
	Tone Output[1]						
V_{OR}	Single Tone Mode, Output Voltage	Row Tone R_L = 600Ω	5.0	490		660	mVrms
		Row Tone R_L = 320Ω	12.0	440		600	mVrms
V_{OC}		Column Tone R_L = 600Ω	5.0	650		880	mVrms
		Column Tone R_L = 320Ω	12.0	590		790	mVrms
dB$_{CR}$	Ratio of Column to Row Tone		3.5-13.0	1.75	2.85	3.7	dB
% DIS	Distortion (Any Dual Tone)*		3.5-13.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage High (Pin 2) No Key Depressed	I_{OH} = 15mA	3.5	1.5			V
		I_{OH} = 50mA	10.0	8.0			V
V_{OL}	MUTE Output Voltage (Pin 10) Low No Key Depressed, No Load		3.5			0.4	V
			13.0			1.0	V
V_{OH}	One Key Depressed, No Load		3.5	2.6			V
			13.0	10.0			V
I_{OL}	MUTE Output Sink Current	V_{OL} = 0.5V	3.0	0.2			mA
			10.0	0.5			mA
I_{OH}	MUTE Output Source Current	V_{OH} = 2V	3.0	0.5			mA
		V_{OH} = 9V	10.0	0.5			mA
	Oscillator						
I_{OH}	Output Current	Sink V_{IL} = 0.5V	3.5	0.34			mA
		Source V_{IH} = 3.0V	3.5	0.23			mA
t_{SU}	Startup Time		3.5			6.0	mS
	Input Currents						
I_{IH}	Row, Column Inputs, Pull-up (Source) Current	V_{IH} = 3.0V	3.5			0.45	mA
		V_{IH} = 12.5V	13.0			1.48	mA
I_{IL}	Pull-down (Sink) Current	V_{IL} = 2.1V	3.5			0.1	mA
		V_{IL} = 9.1V	13.0			0.6	mA

*Distortion measured in accordance with the specification described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair."
[1]Amplitude specification limits apply at room temperature (+25°C) only.

S2559C & D Electrical Characteristics (Specifications apply over the operating temperature range of –25°C to +70°C unless otherwise noted. Absolute values of the measured parameters are specified.)

Symbol	Parameter/Conditions		$(V_{DD}-V_{SS})$ Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode with Valid Key Depressed			2.75		10.0	V
	Non Tone Out Mode (No Key Depressed)			2.25		10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		0.3	30	μA
			10.0		1.0	100	μA
	Operating (One Key Selected, Tone XMIT and MUTE Outputs Unloaded)		3.0		1.0	2.0	mA
			10.0		8.0	16.0	mA
	Tone Output[1]						
V_{OR}	Single Tone Mode Output Voltage	Row Tone, $R_L = 390\Omega$	5.0	424	546	667	mVrms
		Row Tone, $R_L = 240\Omega$	10.0	376	501	626	mVrms
V_{OC}		Column Tone, $R_L = 390\Omega$	5.0	573	731	889	mVrms
		Column Tone, $R_L = 240\Omega$	10.0	504	672	840	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.0-10.0	1.75	2.54	3.75	dB
% DIS	Distortion (Any Dual Tone)*		3.0-10.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High (No Key Depressed) (Pin 2)	$(I_{OH} = 15mA)$	3.0	1.5	1.8		V
		$(I_{OH} = 50mA)$	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, $V_{OF} = 0V$		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load		2.75		0	0.5	V
			10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed), No Load		2.75	2.25	2.75		V
			10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink Current	$V_{OL} = 0.5V$	3.0	0.53	1.3		mA
			10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source Current	$V_{OH} = 2.5V$	3.0	0.17	0.41		mA
		$V_{OH} = 9.5V$	10.0	0.57	1.5		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current One Key Selected	$V_{OL} = 0.5V$	3.0	0.21	0.52		mA
		$V_{OL} = 0.5V$	10.0	0.80	2.1		mA
I_{OH}	Output Source Current One Key Selected	$V_{OH} = 2.5V$	3.0	0.13	0.31		mA
		$V_{OH} = 9.5V$	10.0	0.42	1.1		mA
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	$V_{IL} = 10.0V$	10.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	$V_{IH} = 0.0V$	10.0			1.0	μA
I_{IL}	Sink Current No Key Selected	$V_{IL} = 0.5V$	3.0	47	93		μA
		$V_{IL} = 0.5V$	10.0	65	130		μA
t_{START}	Oscillator Startup Time		2.75		0.4	1.2	mS
			10.0		0.25	0.75	mS
$C_{I/O}$	Input/Output Capacitance		3.0		12	16	pF
			10.0		10	14	pF

[1] Amplitude specification limits apply at room temperature (+25°C) only.

S2559C & D Electrical Specifications (continued)

Symbol	Parameter/Conditions		$(V_{DD}-V_{SS})$ Volts	Min.	Typ.	Max.	Units
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, V_{IL} = 3.0V (Pull-down)	3.0	6.5	16		μA
		Sink Current, V_{IL} = 10.0V (Pull-down)	10.0	9.2	24		μA
I_{IH}		Source Current, V_{IH} = 2.5V (Pull-up)	3.0	85	210		μA
		Source Current, V_{IH} = 9.5V (Pull-up)	10.0	280	740		μA
I_{IH}	Mode Select Input (S2559C)	Source Current, V_{IH} = 0.0V (Pull-up)	3.0	1.4	3.3		μA
		Source Current, V_{IH} = 0.0V (Pull-up)	10.0	18	46		μA
I_{IL}	Chip Disable Input (S2559D)	Sink Current, V_{IL} = 3.0V (Pull-down)	3.0	3.9	9.5		μA
		Sink Current, V_{IL} = 10.0V (Pull-down)	10.0	55	143		μA

*Distortion measured in accordance with the specification described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair."

Table 1. Comparisons of Specified vs Actual Tone Frequencies Generated by S2559

Table 2. XMIT and MUTE Output Functional Relationship

ACTIVE INPUT	OUTPUT FREQUENCY Hz		% ERROR SEE NOTE
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	−0.32
C3	1,477	1,471.9	−0.35
C4	1,633	1,645.0	+0.73

OUTPUT	'DIGIT' KEY RELEASED	'DIGIT' KEY DEPRESSED	COMMENT
XMIT	V_{DD}	High Impedance	Can source at least 50mA at 10V with 1.5V max. drop
MUTE	V_{SS}	V_{DD}	Can source or sink current

NOTE: % Error does not include oscillator drift.

Circuit Description

The S2559 is designed so that it can be interfaced easily to the dual tone signaling telephone system and that it will more than adequately meet the recommended telephone industry specifications regarding the dual tone signaling scheme.

Design Objectives

The specifications that are important to the design of the Digital Tone Generator are summarized below: The dual tone signal consists of linear addition of two voice frequency signals. One of the two signals is selected from a group of frequencies called the "low group" and the other is selected from a group of frequencies called the "high group." The low group consists of four frequencies 697, 770, 852 and 941 Hz. The high group consists of four frequencies 1209, 1336, 1477 and 1633Hz. A keyboard arranged in a row, column format (4 rows x 3 or 4 columns) is used for number entry. When a push button corresponding to a digit (0 thru 9) is pushed, one appropriate row (R1 thru R4) and one appropriate column (C1 thru C4) is selected. The active row input selects one of the low group frequencies and the active column input selects one of the high group frequencies. In standard dual tone telephone systems, the highest high group frequency of 1633Hz (Col. 4) is not used. The frequency tolerance must be ±1.0%. However, the S2559 provides a better than .75% accuracy. The total harmonic and intermodulation distortion of the dual tone must be less than 10% as seen at the telephone terminals. (Ref. 1.) The high group to low group signal amplitude ratio should be 2.0 ±2dB and the absolute amplitude of the low group and high group tones must be within the allowed range. (Ref. 1.) These requirements apply when the telephone is used over a short loop or long loop and over the operating temperature range. The design of the S2559 takes into account these considerations.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the Osci and Osco terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Keyboard Interface

The S2559 employs a calculator type scanning circuitry to determine key closures. When no key is depressed, active pull-down resistors are "on" on the row inputs and active pull-up resistors are "on" on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull-up or pull-down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The advantage of the scanning technique is that a keyboard arrangement of SPST switches are shown in Figure 2 without the need for a common line, can be used. Conventional telephone push button keyboards as shown in Figure 1 or X-Y keyboards with common can also be used. The common line of these keyboards can be left unconnected or wired "high."

Logic Interface

The S2559 can interface with CMOS logic outputs directly. The S2559 requires active "high" logic levels. Since the active pull-up resistors present in the S2559 are fairly low value (500Ω typ), diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their "low" state.

Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stairstep waveform to approximate the sinewave function (See Figure 4.) This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak to peak amplitude V_P ($V_{DD} - V_{REF}$) of the stairstep function is fairly constant. V_{REF} is so chosen that V_P falls within the allowed range of the high group and low group tones.

Telecomunications

Figure 1. Standard Telephone Push Button Keyboard

RON (contact resistance) ≤ 1kΩ
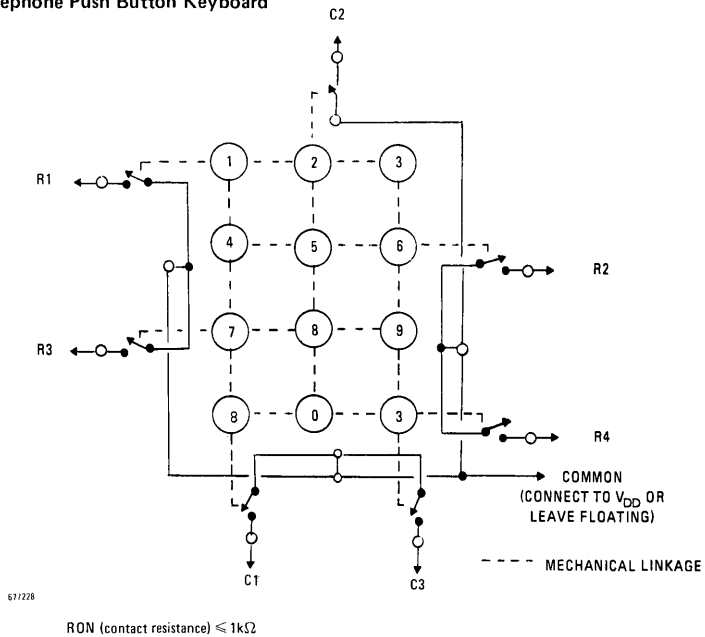
Figure 2. SPST Matrix Keyboard Arranged in the 2 of 8 Row, Column Format

SPST MATRIX KEYSORTED:

N.O.
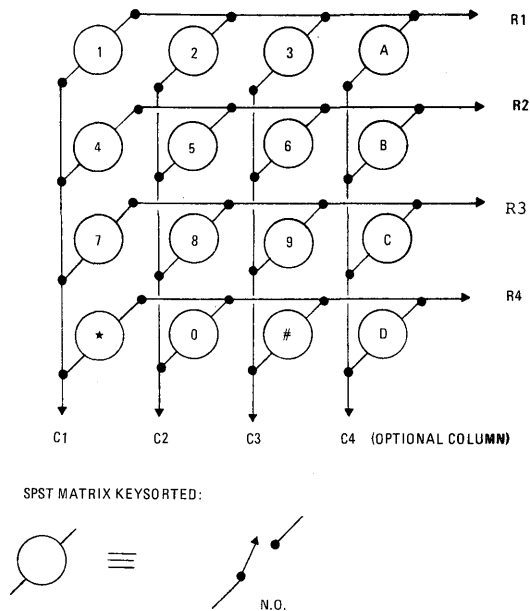
Figure 3. Logic Interface for Keyboard Inputs of the S2559

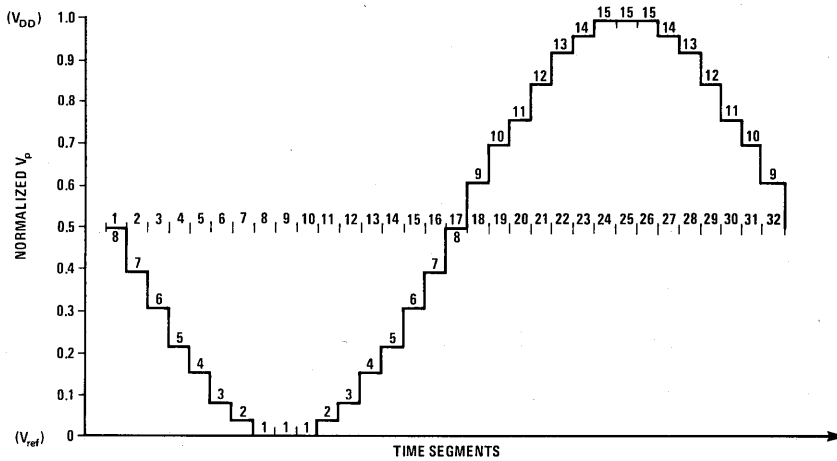677224 G1 THRU G8 ANY TYPE CMOS GATE
D1 THRU D8 DIODES TYPE IN914 (OPTIONAL)
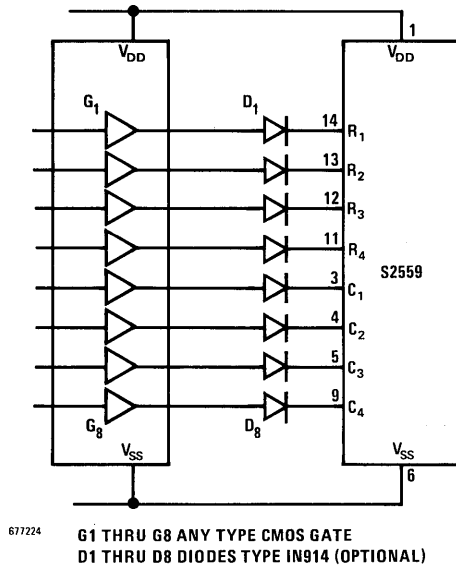
Figure 4. Stairstep Waveform of the Digitally Synthesized Sinewave

The individual tones generated by the sinewave synthesizer are then linearly added and drive a bipolar NPN transistor connected as emitter follower to allow proper impedance transformation, at the same time preserving signal level.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by activating the appropriate row input or by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Mode Select

S2559A and S2559C have a Mode Select (MDSL) input (Pin 15). When MDSL is left floating (unconnected) or connected to V_{DD}, both the dual tone and single tone modes are available. If MDSL is connected to V_{SS}, the single tone mode is disabled and no output tone is produced if an attempt for single tone is made. The S2559B and S2559D do not have the Mode Select option.

Chip Disable

The S2559B and S2559D have a Chip Disable input at Pin 15 instead of the Mode Select input. The chip disable for the S2559B and S2559D is active "high." When the chip disable is active, the tone output goes to V_{SS}, the row, column inputs go into a high impedance state, the oscillator is inhibited and the MUTE and XMIT outputs go into active states. The effect is the device essentially disconnects from the keyboard. This allows one keyboard to be shared among several devices.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ±0.02%
$R_S \leqslant 100\Omega$, L_M = 96MHY
C_M = 0.02pF C_h = 5pF

MUTE, XMIT Outputs

The S2559 A, B, C, D have a CMOS buffer for the MUTE output and a bipolar NPN transistor for the XMIT output. With no keys depressed, the MUTE output is "low" and the XMIT output is in the active state so that substantial current can be sourced to a load. When a key is depressed, the MUTE output goes high, while the XMIT output goes into a high impedance state. When Chip Disable is "high" the MUTE output is forced "low" and the XMIT output is in active state regardless of the state of the keyboard inputs.

Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the Digital Tone Generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the Tone Output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 5 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 5 volts. The load resistor value also controls the amplitude. If R_L is low the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than $5K\Omega$ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3581A) and amplitudes at the selected frequencies can be noted. This measurment also permits verification of the preemphasis between the individual frequency tones.

Distortion is defined as "the ratio of the *total* power of all extraneous frequencies in the *voiceband* above 500Hz accompanying the signal to the power of the frequency *pair*." This ratio must be less than 10% or when expressed in dB must be lower than −20dB. (Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

$$\text{Dist.} = \frac{\sqrt{(V_1)^2 + (V_2)^2 + \ldots + (V_n)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

where (V_1) ... (V_n) are extraneous frequency (i.e., intermodulation and harmonic) components in the 500Hz to 3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$\text{DIST}_{dB} = 20 \log \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots(V_n)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\left\{ \log\left[(V_1)^2+\ldots(V_n)^2\right] - \log\left[(V_L)^2+(V_H)^2\right]\right\} \ldots (1)$$

An accurate way of measuring distortion is to plot a spectrum of the signal by using a spectrum analyzer (H-P type 3580A) and an X-Y plotter (H-P type 7046A). Individual extraneous and signal frequency components are then noted and distortion is calculated by using the expression (1) above. Figure 6 shows a spectrum plot of a typical signal obtained from a S2559D device operating from a fixed supply of 4Vdc and R_L = 10kΩ in the test circuit of Figure 5. Mathematical analysis of the spectrum shows

distortion to be −30dB (3.2%). For quick estimate of distortion, a rule of thumb as outlined below can be used.

"As a first approximation distortion in dB equals the difference between the amplitude (dB) of the extraneous component that has the highest amplitude and the amplitude (dB) of the low frequency signal." This rule of thumb would give an estimate of ~28dB as distortion for the spectrum plot of Figure 6 which is close to the computed result of −30dB.

In a telephone application amplitude and distortion are affected by several factors that are interdependent. For detailed discussion of the telephone application and other applications of the 2559 Tone Generator, refer to the applications note "Applications of Digital Tone Generator."

Ref. 1: *Bell System Communications Technical Reference, PUB 47001,* "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment," August 1976.

Figure 5. Test Circuit for Distortion Measurement

Telecomuni-cations
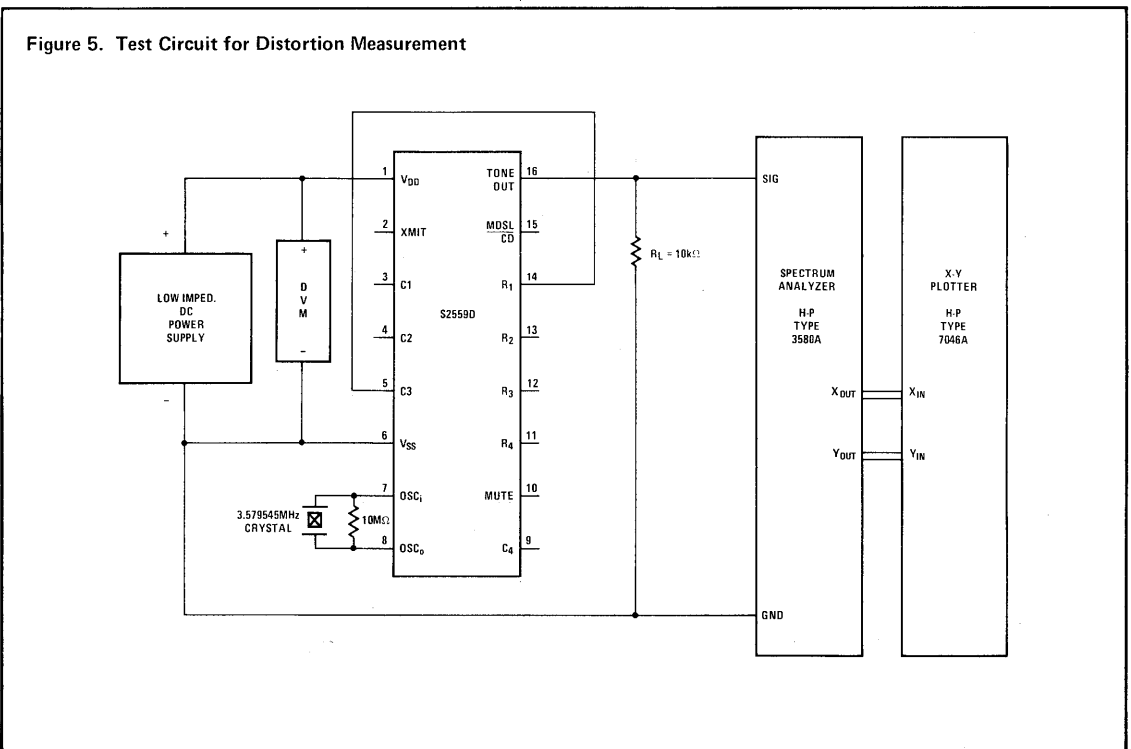
Figure 6. A Typical Spectrum Plot

DEVICE = S2559D
TEMP = ROOM
$(V_{DD} - V_{SS})$ = 4V DC FIXED
R_L = 10kΩ
TEST CKT = FIGURE 5
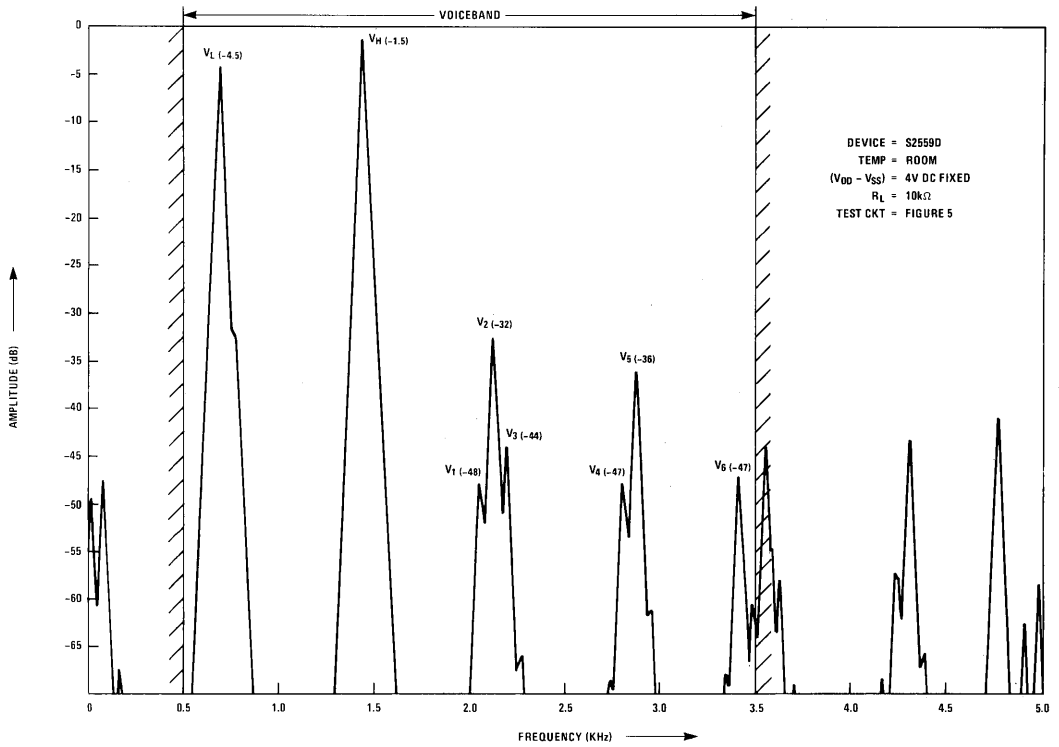
Physical Dimensions

16 Pin Plastic
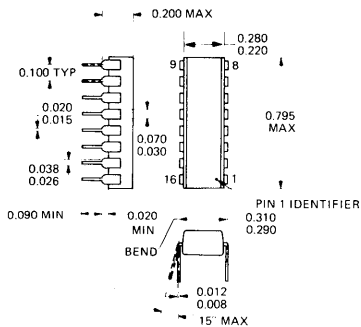
16 Pin Cer-DIP
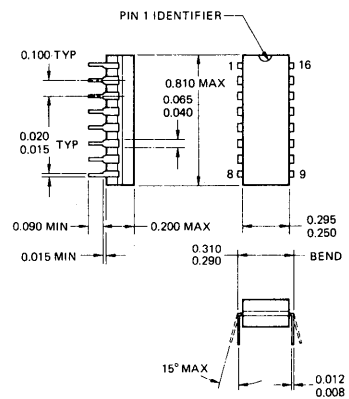
KEY PULSER

Features

- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines
- ☐ Inexpensive R-C Oscillator Design Provides Better than ±5% Accuracy Over Temperature and Unit to Unit Variations
- ☐ Dialing Rate Can Be Varied By Changing the Dial Rate Oscillator Frequency
- ☐ Dial Rate Select Input Allows Changing of the Dialing Rate by a 2:1 Factor Without the Need of Changing Oscillator Components
- ☐ Two Selections of Mark/Space Ratios (33-1/3 /66-2/3 or 40/60)
- ☐ Twenty Digit Memory for Input Buffering and for Redial With Access Pause Capability
- ☐ Mute and Dial Pulse Drivers on Chip
- ☐ Accepts Standard Telephone DPCT Keypad Arranged in a 2 of 7 Format; Also Capable of Logic Interface
- ☐ Ignores Multi Key Entries

General Description

The S2560 Key Pulser is a CMOS integrated circuit that converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone lines with minimum interface. Storage is provided for 20 digits, therefore, the last dialed number is available for redial until a new number is entered.

Unique Features of S2560A (18 Pin Package)

IDP scaled to the dialing rate such as to produce smaller IDP at higher dialing rates. Additionally, the IDP can be changed by a 2:1 factor at a given dialing rate by means of the IDP select input.

Unique Features of S2560B (24 Pin Package)

Separate IDP oscillator for selecting an IDP independent of the dialing rate. Provision for changing of the IDP by a 2:1 factor without the need of changing external components.

Alternating pacifier tone output simulates dual tone effects coincident with each keyboard number entry.

Data subject to change at any time without notice. These sheets transmitted for information only.

Block Diagram

Pin Configuration
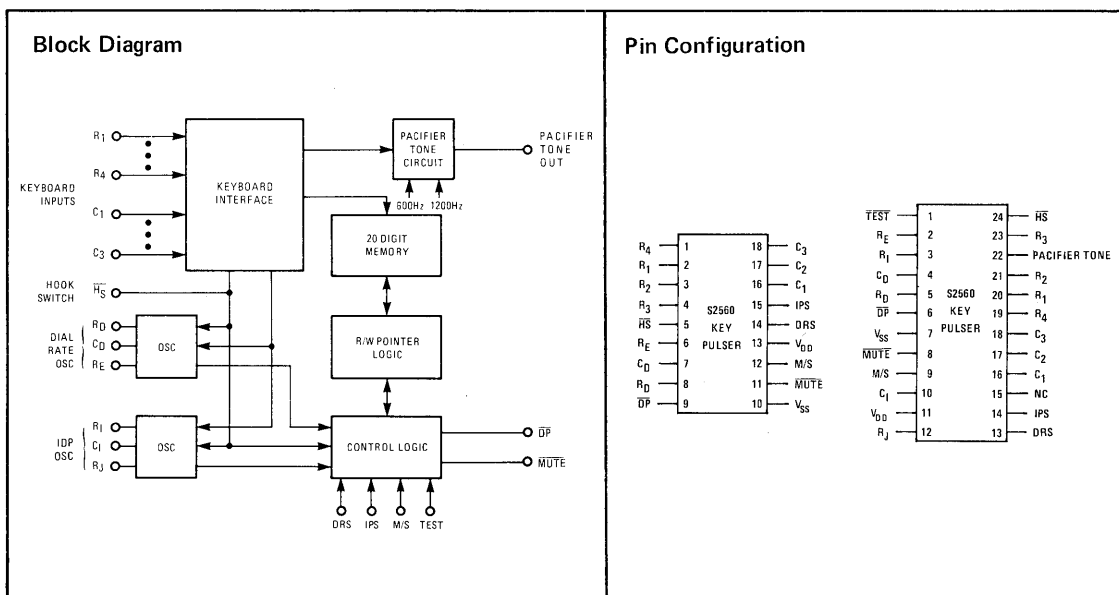
Absolute Maximum Ratings

Supply Voltage	+5.5V
Operating Temperature Range	$-40°$C to $+85°$C
Storage Temperature Range	$-40°$C to $+125°$C
Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Lead Temperature (Soldering, 10 Seconds)	$300°$C

Electrical Characteristics Specifications apply over the operating temperature range and $1.5V \leqslant V_{DD}$ to $V_{SS} \leqslant 3.5V$ unless otherwise specified. Absolute values of the measured parameters are specified.

Symbol	Parameter	$V_{DD} - V_{SS}$ (Volts)	Min.	Max.	Units	Conditions
	Output Current Levels					
I_{OLDP}	$\overline{DP}$ Output Low (Sink) Current	3.5	125		μA	$V_{OUT} = 0.4V$
I_{OHDP}	$\overline{DP}$ Output High (Source) Current	1.5 3.5	20 125		μA μA	$V_{OUT} = 1V$ $V_{OUT} = 2.5V$
I_{OLM}	$\overline{MUTE}$ Output Low (Sink) Current	3.5	125		μA	$V_{OUT} = 0.4V$
I_{OHM}	$\overline{MUTE}$ Output High (Source) Current	1.5 3.5	20 125		μA μA	$V_{OUT} = 1V$ $V_{OUT} = 2.5V$
I_{OLT}	Tone Output Low (Sink) Current	1.5	20		μA	$V_{OUT} = 0.4V$
I_{OHT}	Tone Output High (Source) Current	1.5	20		μA	$V_{OUT} = 1V$
I_{DD}	Quiescent Current	3.5		1	μA	"On Hook" $\overline{HS} = V_{DD}$
I_{IL}, I_{IH}	Input Current Any Pin (Keyboard Inputs)	3.5	1	10	μA	$V_{IN} = $ Open or V_{DD}
I_{IL}, I_{IH}	Input Current Any Other Pin	3.5		100	nA	$V_{IN} = V_{SS}$ or V_{DD}
I_{DD}	Operating Current	3.5 3.5		20 60	μA μA	$\overline{DP}$, $\overline{MUTE}$ open, $\overline{HS}=V_{SS}$ ("Off Hook") Keyboard processing and dial pulsing space fo = 2400Hz $\overline{DP}$, $\overline{MUTE}$ sourcing 20μA, other conditions as above
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	1.5 to 2.5 2.5 to 3.5	-5 -5	$+5$ $+5$	% %	Fixed R-C oscillator components $50k\Omega \leqslant R_D \leqslant 750k\Omega$; $100pF \leqslant C_D^* \leqslant 3000pF$; $1M\Omega \leqslant R_E \leqslant 5M\Omega$ *330pF most desirable value for C_D. Indicated and over the operating temperature range and unit to unit variations
	Input Voltage Levels					
V_{IH}	Logical "1"		$V_{DD} - 0.25$	V_{DD}	V	
V_{IL}	Logical "0"		V_{SS}	$V_{SS} + 0.25$	V	
C_{in}	Input Capacitance Any Pin			7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leqslant V_I \leqslant V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

Functional Description

The key pulser is available in two package configurations: 18 pin and 24 pin. The pin function designations for the two packages are outlined in Table 1.

18 Pin Configuration

This package is specifically designed for the most common telephone application where the rotary dial is to be replaced by a keypad to dial pulse conversion system. Figure 5 shows a typical telephone interface scheme.

OFF Hook Operation: The device is continuously powered through a 27kΩ resistor during OFF hook operation. The $\overline{DP}$ output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The $\overline{DP}$ output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during the pulse break. The $\overline{MUTE}$ output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 4.

ON Hook Operation: The device is continuously powered through a 10MΩ resistor during the ON hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20 pps can be achieved. Dialing rates of 7 and 14 pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20 pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14 pps, IDP's of 1143ms and 572ms

can be similarly obtained. If the IDP select pin is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10 pps an IDP of 800ms is obtained and at 20 pps an IDP of 400ms is obtained.

The user can enter a number up to 20 digits long from a standard 3 x 4 double contact keypad (Figure 1) or a matrix keyboard arranged out of 12 SPST switches to produce a 2 of 7 format (Figure 2). It is also possible to use a logic interface as shown in Figure 3 for number entry. Antibounce protection circuitry is provided on chip (min. 13ms) to prevent false entry.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is used to retain the memory.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20 pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed twenty.

Auto Dialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

24 Pin Configuration

All the functions previously described for the 18 pin package configuration can be performed in this configuration. Additionally, the following features are incorporated:

1. A separate IDP oscillator is provided. This allows generation of an IDP time independent of the

Telecommunications

24 Pin Configuration (Continued)

dialing rate. The IDP select input allows genera-tion of two IDP's with a 2:1 ratio without the need of changing oscillator components. Thus, for an oscillator frequency of 2400Hz, an IDP of 400ms is obtained with IDP select pin wired to V_{DD} and an IDP of 800ms is obtained with the IDP select pin connected to V_{SS}. Table 2 shows the relationship between the IDP and the IDP oscillator frequency. Typical resistance and capa-citor values are also provided. The IDP oscillator input can be driven by the dial rate oscillator out-put if scaling of IDP to dialing rate is desired.

2. A pacifier tone output is provided. As entries from the keyboard are made, the pacifier tone output alternates between two frequencies for successive digits. This provides simulation of the dual tone signaling in the user's earpiece. The tone frequency is derived from the dial rate oscillator and therefore depends on the dialing rate selected. The pacifier tone output alternates between a pair of audio frequencies.

3. A test input is provided to allow testing of the dial rate and IDP oscillators. With the test pin connected to V_{SS}, the dial rate and IDP oscil-lators can be gated on. This facilitates calibration of the required frequencies. In the normal opera-tion, the test input must be connected to V_{DD}.

Table 1. Pin/Function Descriptions

18 Pin Configuration

Pin	Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	7	These are 4 row and 3 column inputs from the key-board contacts. These inputs are open when the key-board is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD}. A logic interface is also possible as shown in Figure 3. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan be-gins when a key is pressed and starts the oscillator. De-bouncing is provided to avoid false entry (typ. 20ms).
Inter-Digit Pause Select (IPS)	1	One programmable line is available that allows selec-tion of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceding the first dialed pulse is an inter-digit time equal to the selected IDP. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Dial Rate Select (DRS)	1	A programmable line allows selection of two different output rates such as 7 or 14 pps, 10 or 20 pps, etc. See Tables 2 and 3.
Mark/Space (MS)	1	This input allows selection of the mark/space ratio, as per Table 3.
Mute Out ($\overline{MUTE}$)	1	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.

Table 1. (Continued)

Pin	Number	Function
Dial Pulse Out ($\overline{DP}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator	3	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	1	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 1.5V to 3.5V.
	18	

24 Pin Configuration

In addition to the 18 pins listed above, the following pins are provided:

Pacifier Tone Out (Tone)	1	Square wave output that alternates between two frequencies as defined in Table 3 when keypad buttons are depressed.
IDP Oscillator (R_I, R_J, C_I)	3	These pins are for connecting external resistors R_I, R_J and capacitor C_I to form an R-C oscillator that determines the duration of the inter-digit pause. This oscillator functions independently of the dial rate oscillator and thus permits the dialing rates and IDP to be independent of each other.
Test	1	This input when connected to V_{SS} turns the dial rate and IDP oscillators on to allow easy calibration of the frequencies desired. In normal operation it must be connected to V_{DD}.
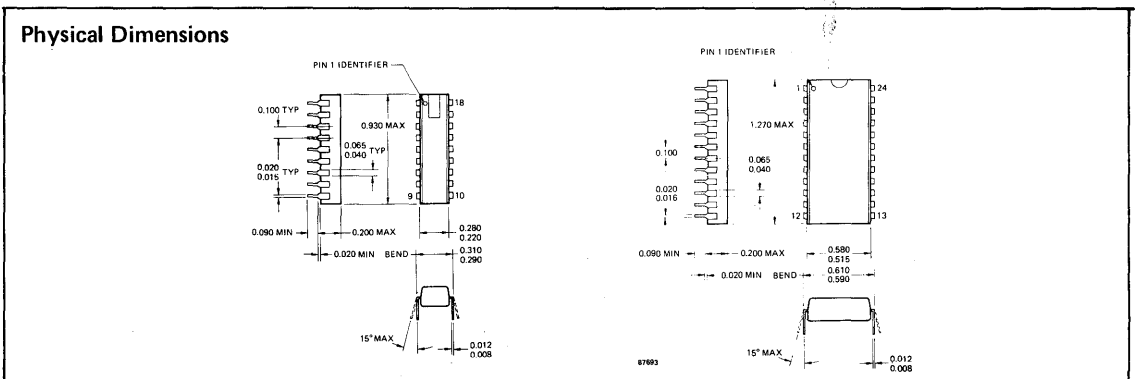
Telecomuni- cations

Physical Dimensions

Figure 1. Standard Telephone Pushbutton Keyboard

877284 R_{ON} (CONTACT RESISTANCE) ⩽ 1kΩ

COMMON
(CONNECT TO V_{DD} OR
LEAVE FLOATING)
——— MECHANICAL
LINKAGE
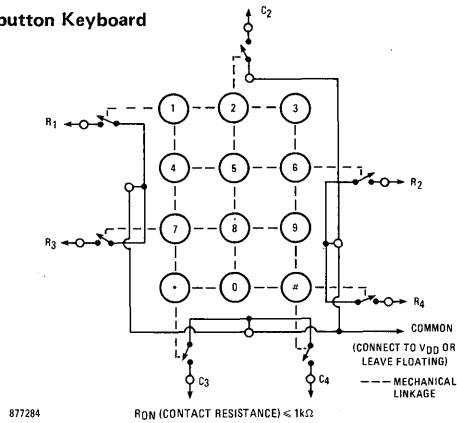
Figure 2. SPST Matrix Keyboard Arranged in the 2 of 7 Row, Column Format

SPST MATRIX KEYBOARD:

877291   140 R_{on} ⩽ 1kΩ

Figure 3. Logic Interface For the S2560

KEYBOARD
INPUTS

S2560

G1 through G7 any CMOS type logic gates

877292

6.18
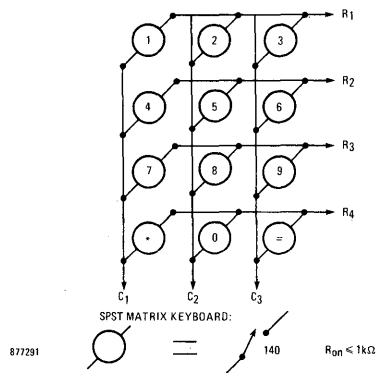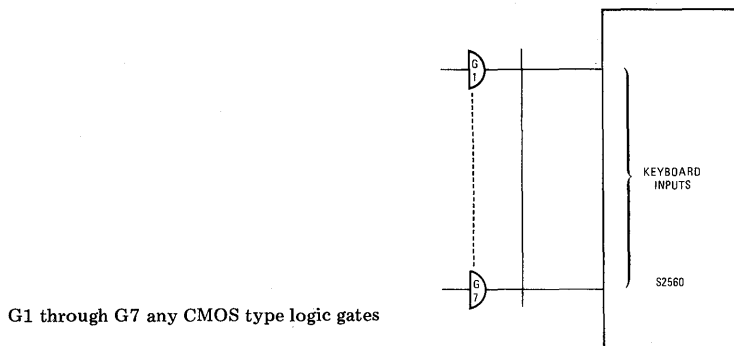
Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (R_I) (kΩ)	R_E (R_J) (kΩ)	C_D (C_I) (pF)	Dial Rate (pps)		IDP (ms)	
					DRS=V_{SS}	DRS=V_{DD}	IPS=V_{SS}	IPS=V_{DD}
5.5/11	1320				5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680				7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920	To Be Determined			8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400				10	20	800	400
(f_d/240)/ (f_d/120)	f_d				(f_d/240)	(f_d/120)	$\left(\frac{1920}{f_i} \times 10^3\right)$	$\left(\frac{960}{f_i} \times 10^3\right)$

Notes:
1. In the 18 pin package configuration, IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10 pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14 pps, an IDP of either 1142ms or 571ms can be selected.
2. In the 24 pin package configuration, the dialing rate and IDP can be independently selected of each other. The general formula outlined in the table may be used to figure out any IDP and dialing rate independent of each other where f_d = dial rate oscillator frequency in Hz as determined by components R_D, R_E and C_D and f_i = IDP oscillator frequency in Hz as determined by components R_I, R_J and C_I.

Table 3.

Function	Pin Designation	Input Logic Level	Selection
Dial Pulse Rate Selection	DRS	V_{SS} V_{DD}	(f/240) pps (f/120) pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	$\frac{960}{f}$ s $\frac{1920}{f}$ s
Mark/Space Ratio	M/S	V_{SS} V_{DD}	33-1/3/66-2/3 40/60
On Hook/Off Hook	$\overline{HS}$	V_{DD} V_{SS}	On Hook Off Hook

Note: f is the oscillator frequency and is determined as shown in Figure 5.

Figure 4. Timing

Figure 5. AMI Key Pulser Application

R_0: 10MΩ, R_1: 27kΩ, R_2: 2kΩ, R_3: 470kΩ
R_4, R_5: 10kΩ, R_{10}: 47kΩ, R_6, R_8: 2kΩ
R_7, R_9: 30kΩ, Z_1: 3.9V, D_1, D_5: 1V4004, C_1: 15μF
R_E, R_D: 750kΩ, C_D: 330pF, D_6: IN914
C_2: .01μF
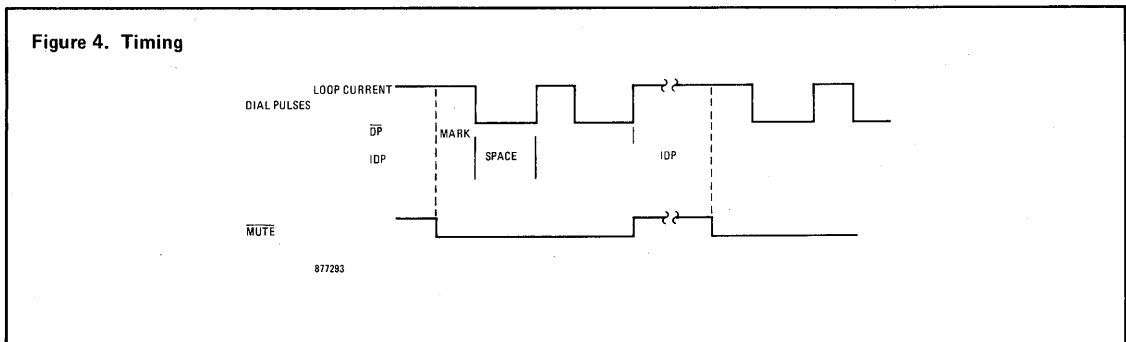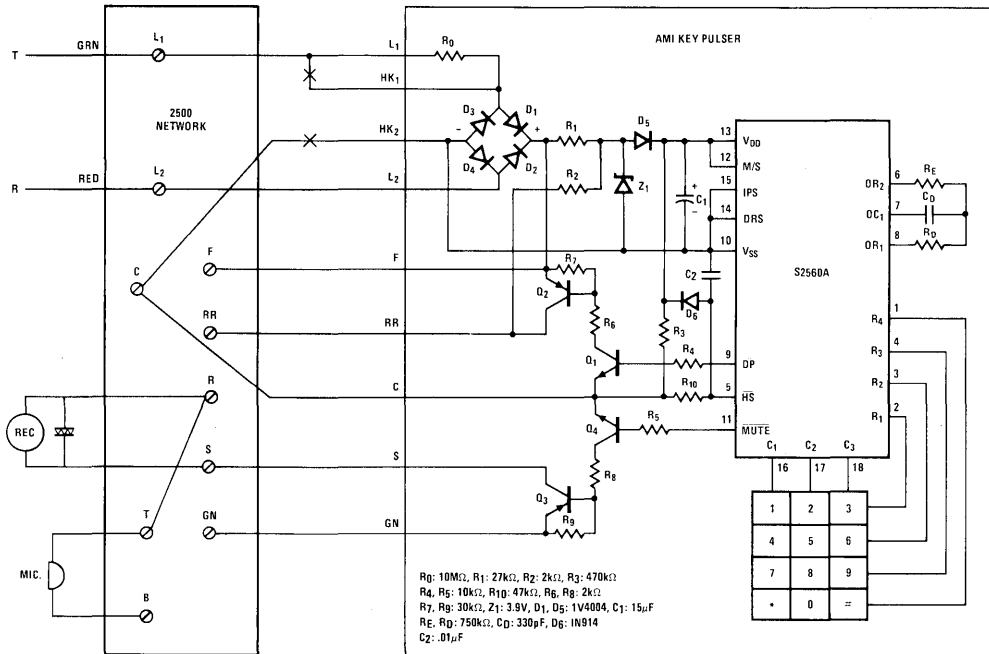
NOTE: INITIAL PARTS REQUIRE COMMON OF THE KEYBOARD CONNECTED TO V_{DD}

AMI®

TONE RINGER

Features

☐ CMOS Process for Low Power Operation
☐ Operates Directly from Telephone Lines with Simple Interface
☐ Also Capable of Logic Interface for Non-Telephone Applications
☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
☐ 50mW Output Drive Capability at 10V Operating Voltage

☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
☐ Single Frequency Tone Capability

General Description

The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

Data subject to change at any time without notice. These sheets transmitted for information only.

Block Diagram

Pin Configuration
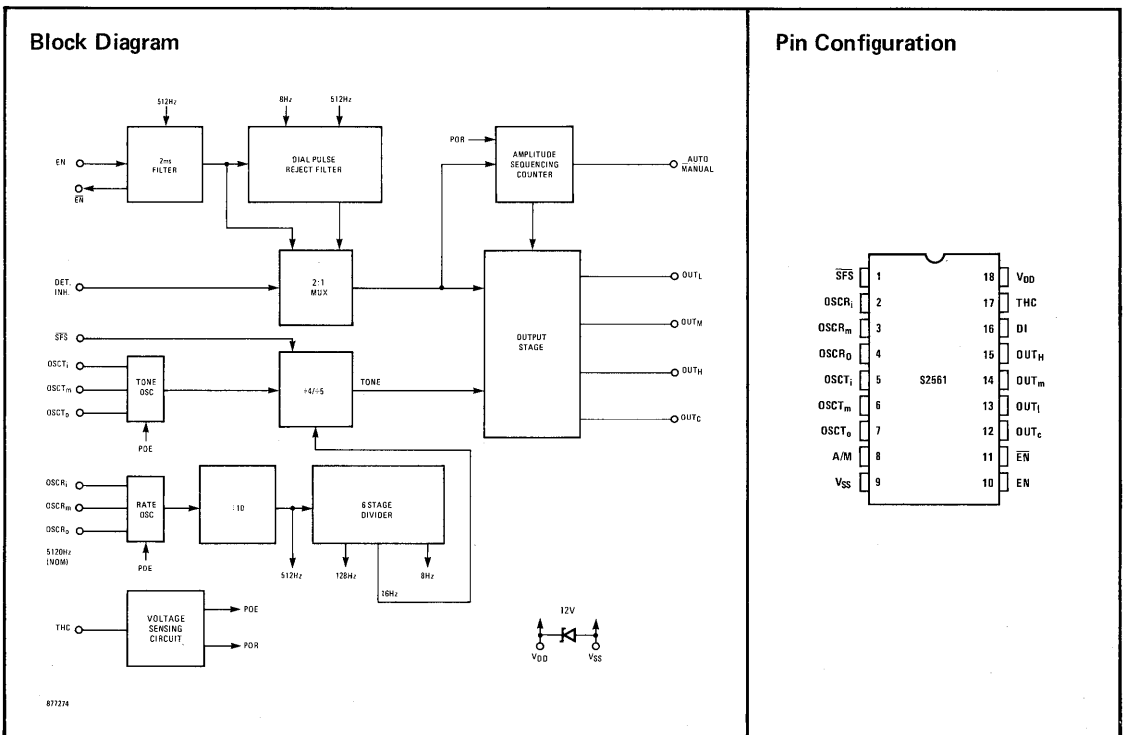
Absolute Maximum Ratings

Supply Voltage	+12V
Operating Temperature Range	$-25°C$ to $+70°C$
Storage Temperature Range	$-40°C$ to $+125°C$
Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Lead Temperature (Soldering, 10sec)	$300°C$

Electrical Characteristics Specifications apply over the operating temperature range and $3.5V \leqslant V_{DD}$ to V_{SS} $< 12V$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{DS}	Operating Voltage (V_{DD} to V_{SS})	8.0	13.5	V	Ringing, THC pin open
V_{DS}	Operating Voltage	4.0		V	"Auto" mode, non-ringing
I_{DS}	Operating Current		500	μA	Non-ringing, V_{DD} = 10V, THC pin open, DI pin open or V_{SS}
I_{DS}	Operating Current		25	μA	Non-ringing, V_{DD} = 6V, THC pin open
I_{OHC}	Output Drive Output Source Current (OUT_H, OUT_C outputs)	5		mA	V_{DD} = 10V, V_{OUT} = 9V
I_{OLC}	Output Sink Current (OUT_H, OUT_C outputs)	5		mA	V_{DD} = 10V, V_{OUT} = 0.5V
I_{OHM}	Output Source Current (OUT_M output)	2		mA	V_{DD} = 10V, V_{OUT} = 9V
I_{OLM}	Output Sink Current (OUT_M output)	2		mA	V_{DD} = 10V, V_{OUT} = 0.5V
I_{OHL}	Output Source Current (OUT_L output)	1		mA	V_{DD} = 10V, V_{OUT} = 9V
I_{OLL}	Output Sink Current (OUT_L output)	1		mA	V_{DD} = 10V, V_{OUT} = 0.5V
V_{IH}	CMOS to CMOS Input Logic "1" Level	$0.7\,V_{DD}$	$V_{DD} + 0.3$	V	All inputs
V_{IL}	Input Logic "0" Level	$V_{SS} - 0.3$	$0.3\,V_{DD}$	V	All inputs
V_{OHR}	Output Logic "1" Level (Rate output)	$0.9 V_{DD}$		V	I_O = $10\mu A$ (Source)
V_{OLR}	Output Logic "0" Level (Rate output)		0.5	V	I_O = $10\mu A$ (Sink)
V_{OZ}	Output Leakage Current (OUT_H, OUT_M outputs in high impedance state)		1 -1	μA μA	V_{DD} = 10V, V_{OUT} = 0V V_{DD} = 10V, V_{OUT} = 10V
C_{in}	Input Capacitance		7.5	pF	Any pin
$\Delta fo/fo$	Oscillator Frequency Deviation	-5	$+5$	%	Fixed RC component values $1M\Omega \leqslant R_{si}, R_{ti} \leqslant 5M\Omega$; $100k\Omega \leqslant R_{sm}, R_{tm} \leqslant 750k\Omega$ $150pF \leqslant C_{so}, C_{to} \leqslant 3000pF$ $330pF$ recommended value of C_{so} and C_{to}, supply voltage varied from $9V \pm 2V$ (over temperature and unit-unit variations)
R_{LOAD}	Output Load Impedance Connected Across OUT_H and OUT_C	600		Ω	Tone Frequency Range = 300Hz to 3400Hz
I_{IH}, I_{L}	Leakage Current, V_{in} = V_{DD} or V_{SS}		100	nA	Any input, except DI pin V_{DD} = 10V
V_{TH}	POE Threshold Voltage	6.5	8	V	
V_Z	Internal Zener Voltage	11	13	V	I_Z = 5mA

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leqslant V_I \leqslant V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

Functional Description

The S2561 is a CMOS device capable of simulating the effects of the telephone bell. This is achieved by producing a tone that shifts between two predetermined frequencies with a frequency ratio of 5:4 at approximately 16Hz rate.

Tone Generation: The output tone is derived from a tone oscillator that uses a 3 pin R-C oscillator design consisting of one capacitor and two resistors. The oscillator frequency is divided alternately by 4 or 5 at the shift rate. Thus, with the oscillator adjusted for 5120Hz, a tone signal is produced that alternates between 512Hz and 640Hz at the shift rate. The shift rate is derived from another 3 pin R-C oscillator which is adjusted for a nominal frequency of 5120Hz. It is divided down to 16Hz which is used to produce the shift in the tone frequency. It should be noted that in the special case where both oscillators are adjusted for 5120Hz, it is only necessary to have one external R-C network for one oscillator with the other oscillator driven from it. The oscillators are designed such that for fixed R-C component values an accuracy of ±5% can be obtained over the operating supply voltage, temperature and unit-unit variations. See Table 1 for component and frequency selections. In the single frequency mode, activated by connecting the $\overline{SFS}$ input to V_{SS} only the higher frequency continuous tone is produced by using a fixed divider ratio of 4 and by disabling the shift operation.

Ring Signal Detection: The incoming 20Hz ring signal can be applied to the "ENABLE" input after proper voltage limiting by diode clamping (see Figure 2). It is first squared up and then processed by an 2ms filter followed by a dial pulse reject filter. The 2ms filter removes undesirable noise transitions that may occur on the ring signal. The dial pulse reject filter is clocked by an 8Hz signal derived from the rate oscillator and insures that frequencies below 16Hz will not pass through. This helps eliminate dial pulse interference and insures that the tone ringer will not trigger during dial pulsing. Another benefit of the dial pulse reject filter is that an output tone is not produced unless the ring signal duration exceeds 125ms. This insures that the tone ringer will not respond to momentary bursts of ringing less than 125 milliseconds in duration (Ref. 1).

In logic interface applications, the 2ms filter and the dial pulse reject filter can be inhibited by wiring the Det. INHIBIT pin to V_{DD}. This allows the tone ringer to be enabled by a logic '1' level applied at the "ENABLE" input without the necessity of a 20Hz ring signal.

Voltage Sensing: The S2561 contains a voltage sensing circuit that enables the output stage and the rate and tone oscillators, only when the supply voltage exceeds a predetermined value. Typical value of this threshold is 7.3 volts. This produces two benefits. First, it insures that the audible intensity of the output tone is fairly constant throughout the ringing period; and secondly, it insures proper circuit operation during the "auto" mode operation by reducing the power consumption to a minimum when the supply voltage drops below 7.3 volts. This extends the supply voltage decay time beyond 4 seconds (off period of the ring signal) with an adequate filter capacitor and insures the proper functioning of the "amplitude sequencing" counter. It is important to note that the operating supply voltage should be well above the threshold value during the ringing period and that the filter capacitor should be large enough so that the ripple on the supply voltage does not fall below the threshold value. A supply voltage of 10 to 12 volts is recommended.

In applications where the tone ringer is continuously powered and below the threshold level, the internal threshold can be bypassed by connecting the THC pin to V_{DD}. The internal threshold can also be reduced by connecting an external zener diode between the THC and V_{DD} pins.

Auto Mode: In the "auto" mode, activated by wiring the "auto/manual" input to V_{SS}, an amplitude sequencing of the output tone can be achieved. Resistors R_L and R_M are inserted in series with the Out_L and Out_M outputs, respectively, and paralleled with the Out_H output (Figure 1). Load is connected across Out_H and Out_C pins. R_L is chosen to be higher than R_M. In this manner the first ring is of the lowest amplitude, second ring is of medium amplitude and the third and consecutive rings thereafter are at maximum amplitude. For the proper functioning of the "amplitude sequencing" counter the device must have at least 4.0 volts across it throughout the ring sequence. The filter capacitor is so chosen that the supply voltake will not drop below 4.0 volts during the off period. At the end of a ring sequence when the off period substantially exceeds the 4 second duration, the counter will be reset. This will insure that the amplitude sequencing will start correctly beginning a new ring sequence. The counter is held in reset during the "manual" mode operation. This produces a maximum ring amplitude at all times.

Output Stage: The output stage is of push-pull type

Functional Description (Continued)

consisting of buffers L, M, H and C. The load is connected across pins Out_H and Out_C (Figure 2). During ringing, the Out_H and Out_C outputs are out of phase with each other and pulse at the tone rate. During a non-ringing state, all outputs are forced to a known level such as ground which insures that there is no DC component in the load. Thus, direct coupling can be used for driving the load. The major benefit of the push-pull arrangement is increased power output. Four times as much power can be delivered to the load for the same operating voltage. Buffers M and H are three-state. In the "auto" mode buffer M is active only during the second ring and in the "high impe-dance" state at all other times. Buffer H is active beginning the third ring. In the "manual" mode buffers H, L and C are active at all times while buffer M is in a high impedance state. The output buffers are so designed that they can source or sink 5mA at a V_{DD} of 10 volts without appreciable voltage drop. Care has been taken to make them symmetrical in both source and sink configurations. Diode clamping is provided on all outputs to limit the voltage spikes associated with transformer drive in both directions V_{DD} and V_{SS}.

Normal protection circuits are present on all inputs.

Table 1. Pin/Function Descriptions

Pin	Number	Function
Power (V_{DD}, V_{SS})	2	These are the power supply pins. The device is designed to operate over the range of 3.5 to 13.5 volts. A range of 10 to 12 volts is recommended for the telephone application.
Ring Enable (EN, $\overline{EN}$)	2	These pins are to connect the 20Hz ring signal. EN can also be used for DC level enabling by wiring the DI pin to V_{DD}.
Auto/Manual (A/M)	1	"Auto" mode for amplitude sequencing is implemented by wiring this pin to V_{SS}. "Manual" mode results when connected to V_{DD}. The amplitude sequencing counter is held in reset during the "manual" mode.
Outputs (Out_L, Out_M, Out_H, Out_C)	4	These are the push-pull outputs. Load is directly connected across Out_H and Out_C outputs. In the "auto" mode, resistors R_L and R_M can be inserted in series with the Out_L and Out_M outputs for amplitude sequencing (see Figure 1).
Oscillators Rate Oscillator ($OSCR_i$, $OSCR_m$, $OSCR_o$)	3	These pins are provided to connect external resistors RR_i, RR_m and capacitor CR_o to form an R-C oscillator with a nominal frequency of 5120Hz. See Table 2 for components selection.
Tone Oscillator ($OSCT_i$, $OSCT_m$, $OSCT_o$)	3	These pins are provided to connect external resistors RT_i, RT_m and capacitor CT_o to form an R-C oscillator from which the tone signal is derived. With the oscillator adjusted to 5120Hz, a tone signal with frequencies of 512Hz and 640Hz results. See Table 2 for components selection.
Threshold Control (THC)	1	The internal threshold voltage is brought out to this pin for modification in non-telephone applications. It can be bypassed by wiring the THC pin to V_{DD}. It can be reduced by connecting a suitable zener diode between THC and V_{DD}.

Table 1 (Continued)

Pin	Number	Function
Detector Inhibit (DI)	1	When this pin is connected to V_{DD}, the dial pulse reject filter is disabled to allow DC level enabling of the tone ringer. This pin should be hardwired to V_{SS} in normal telephone-type applications.
Single Frequency Select ($\overline{SFS}$)	1	When this pin is connected to V_{SS}, only a single frequency continuous tone is produced as long as the tone ringer is enabled. In normal applications this pin should be hardwired to V_{DD}.

Table 2. Selection Chart for Oscillator Components and Output Frequencies

Tone/Rate Oscillator Frequency (Hz)	Oscillator Components			Rate (Hz)	Tone (Hz)
	R_I (kΩ)	R_M (kΩ)	C_O (pF)		
5120				16	512/640
6400				20	640/800
3200		To Be Determined		10	320/400
8000				25	800/1000
fo				$\dfrac{fo}{320}$	$\dfrac{fo}{10} \Big/ \dfrac{fo}{8}$

Applications

Typical Telephone Application: Figure 2 shows the schematic diagram of a typical telephone application for the S2561 tone ringer circuit. Power is derived from the telephone lines by the network formed by capacitor C_1, resistor R_1, diode bridge d_1 through d_4, and filter capacitor C_2. C_2 is chosen to be large enough so as to insure that the power supply ripple during ringing does not fall below the internal threshold level (typ. 7.3 volts) and to provide large enough decay time during the off period. A typical value of C_2 may be $47\mu F$. C_1 and R_1 are chosen to satisfy the Ringer Equivalence Number (REN) specification (Ref. 1). For REN = 1 the resistor should be a minimum of $8.2k\Omega$. It must be noted that the amount of power that can be delivered to the load depends upon the selection of C_1 and R_1.

The device is enabled by limiting the incoming ring signal through resistors R_2, R_3 and diodes d_5 and d_6. Zener diode Z_1 (typ. 9-27 volts) may be required in certain applications where large voltage transients may occur on the line during dial pulsing. The internal 2ms filter and the dial pulse reject filter will suppress any undesirable components of the signal and will only respond to the normal 20Hz ring signal. Ring signals with frequencies above 16Hz will be detected.

The configuration shown will produce a tone with frequency components of 512Hz and 640Hz with a shift rate of approximately 16Hz and deliver at least 50mW to an 8Ω speaker through a $2000\Omega{:}8\Omega$ transformer. If "manual" mode is used, a potentiometer may be inserted in series with the transformer primary to provide volume control. If "automatic" mode is used, resistors R_L and R_M can be chosen to provide desired amplitude sequencing. Typically, signal power will be down $20 \log \left(\dfrac{R_{LOAD}}{R_L + R_{LOAD}} \right)$ dB during the first ring, and down $20 \log \left(\dfrac{R_{LOAD}}{R_M + R_{LOAD}} \right)$ dB during the second ring with maximum power delivered to the load beginning the third and consecutive rings.

In applications where dial pulse rejection is not necessary, such as in DTMF telephone systems, the ENABLE pin may be connected directly to V_{DD}. Det. Inh pin must be connected to V_{DD} to allow DC level enabling of the ringer.

Non-Telephone Applications: The configuration shown in Figure 3-A may be used in non-telephone applications where it is desired to simulate the telephone bell. The internal threshold is bypassed by wiring THC to V_{DD}. The rate output (16Hz) is divided down by a 7 stage divider type 4024 to produce two signals: a 2 second on/2 second off signal and a 4 second on/4 second off signal. The first signal is connected to the EN pin and the second to the DI pin to produce a 2 second on/4 second off telephone-type ring signal. The ring sequence is initiated by removing the reset on the divider. If "auto" mode is used, a reset signal must be applied to the "amplitude sequencing" counter at the end of a ring sequence so that the circuit will respond correctly to a new ring sequence. This is done by temporarily connecting the "auto/manual" input to V_{SS}.

Figure 3-B shows a typical application for alarms, buzzers, etc. Single frequency mode is used by connecting the $\overline{SFS}$ input to V_{SS}. A suitable on/off rate can be determined by using the 7 stage divider circuit. If continuous tone is not desired, the 16Hz output can be used to gate the tone on and off by wiring it into the ENABLE input.

Many other configurations are possible depending upon the user's specific application.

Reference 1. Bell system communications technical reference:
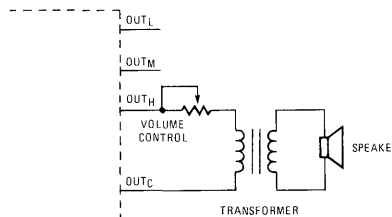
PUB 47001 of August 1976
"Electrical characteristics of Bell System Network Facilities at the interface with Voiceband Ancillary and Data Equipment" — Sections 2.6.1 and 2.6.3.

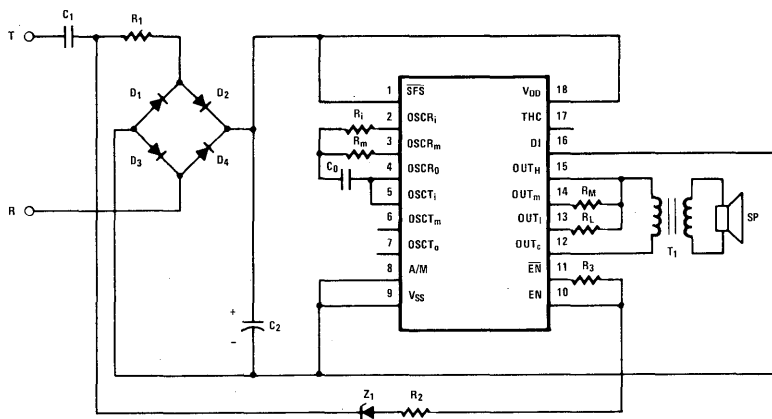**Figure 1-A. Output Stage Connected for Auto Mode Operation**
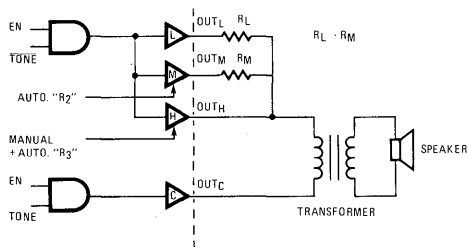
877276

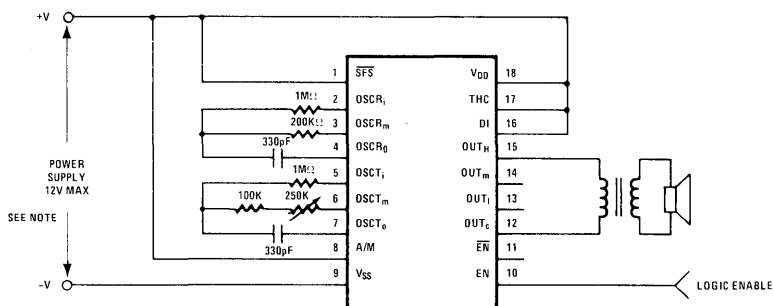**Figure 1-B. Output Stage Connected for Manual Mode Operation.**

877277

Figure 2. Typical Telephone Application of the S2561

C_1	.47μF/200V	R_1	2kΩ	R_i 1MΩ	R_L 18KΩ	SP 8ΩSPEAKER
C_2	47μF/25V	R_2	51kΩ	R_m 200kΩ	R_M 3.3KΩ	T_1 1000Ω/8Ω XFMR
D_1 - D_4	1N4004	R_3	10MΩ	C_o 330pF		Z_1 9 TO 27V ZENER

Figure 3-A. Simulation of the Telephone Bell in Non-Telephone Applications.

NOTE: THIS DEVICE INCORPORATES AN INTERNAL 12V ZENER DIODE ACROSS V_{DD} AND V_{SS} PINS. DO NOT CONNECT A LOW IMPEDANCE POWER SUPPLY DIRECTLY ACROSS THE DEVICE UNLESS THE SUPPLY VOLTAGE CAN BE MAINTAINED BELOW 12V OR SUPPLY CURRENT IS LIMITED TO 50mA.

Figure 3-B. Single Frequency Tone Application in Alarms, Buzzers, Etc.

AMI®
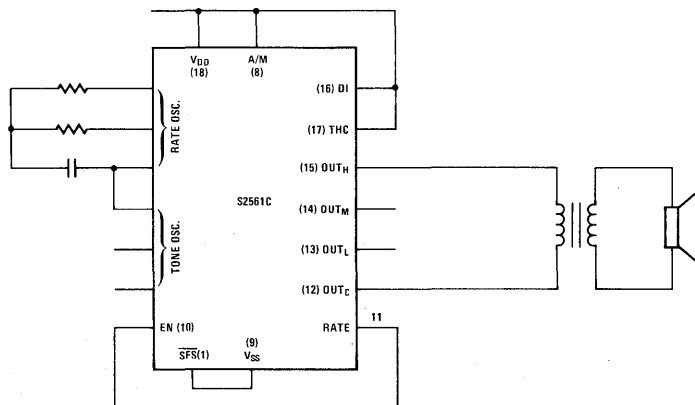
REPERTORY DIALER

Features

☐ CMOS Process Achieves Low Power Operation

☐ 8 or 16 Digit Number Capability
(Pin Programmable)

☐ Dial Pulse and Mute Output

☐ Tone Outputs Obtained by Interfacing with
Standard AMI S2559 Tone Generator

☐ Two Selections of Dial Pulse Rate

☐ Two Selections of Inter-Digit Pause

☐ Two Selections of Mark/Space Ratio
(33-1/3 / 66-2/3 or 40/60)

☐ Memory Storage of 32 8-Digit Numbers or
16 16-Digit Numbers with Standard
AMI S5101 RAM

☐ 16-Digit Memory for Input Buffering and for
Redial with Access Pause Capability

☐ Accepts the Standard Telephone DPCT
Keypad or SPST Switch X-Y Matrix
Keyboards; Also Capable of Logic Interface

☐ Ignores Multi Key Entries

☐ Inexpensive, but Accurate R-C Oscillator
Design Provides Better Than ±3% Accuracy
Over Supply Voltage, Temperature and Unit-
Unit Variations and Allows Different Dialing
Rates, IDP and Tone Drive Timing by
Changing the Time Base

☐ Power Fail Detection

☐ BCD Output with Update for Number Display
Applications

General Description

The S2562 Repertory Dialer is a CMOS integrated
circuit that can perform storing or retrieving, normal
dialing, redialing or auto dialing and displaying of
one of several telephone numbers. It is intended to be
used with the AMI standard S5101—256x4 RAM that
functions as telephone number storage. With one
S5101 up to 32 8-digit or 16 16-digit numbers can
be stored. It can provide either dial pulses or DTMF
tones with the addition of the AMI S2559 tone
generator for either the dial or tone line applications.

Data subject to change at any time without notice. These sheets transferred for information only.

Block Diagram

Pin Configuration

Telecomunications

877283
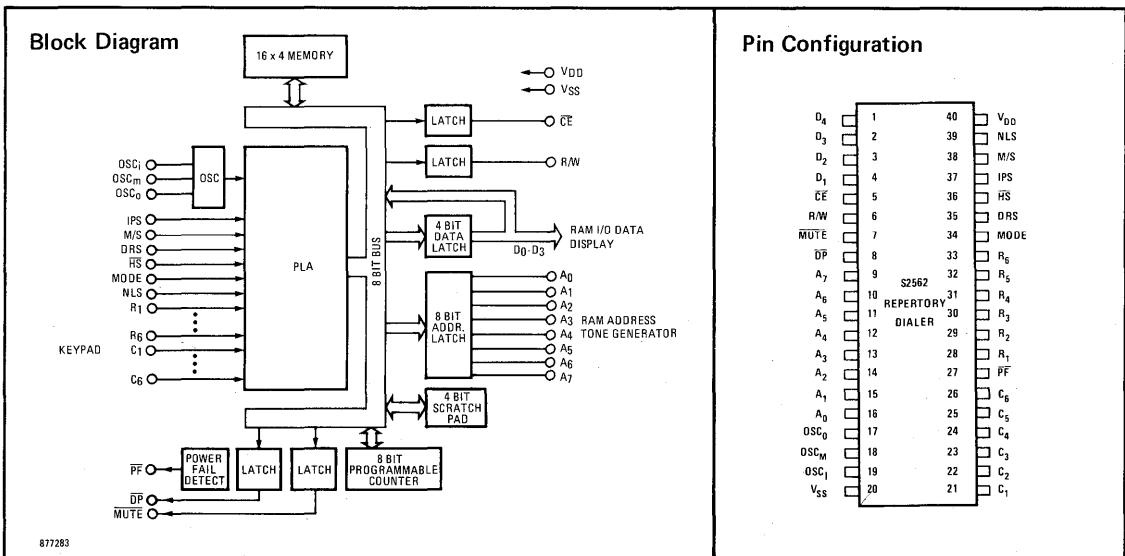
Absolute Maximum Ratings

Supply Voltage	13.5V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Voltage at Any Pin	V_{SS} - 0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10 sec.)	200°C

Electrical Characteristics Specifications apply over the operating temperature range and 4.5V ⩽ V_{DD} to V_{SS} ⩽ 5.5V unless otherwise specified. Absolute values of measured parameters are specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
	Output Drive				
I_{OLDP}	$\overline{DP}$ Output Sink Current	400		μA	V_{OUT} = 0.4V, V_{DD} = 5V
I_{OHDP}	$\overline{DP}$ Output Source Current	400		μA	V_{OUT} = 3.6V, V_{DD} = 5V
I_{OLM}	$\overline{MUTE}$ Output Sink Current	400		μA	V_{OUT} = 0.4V, V_{DD} = 5V
I_{OHM}	$\overline{MUTE}$ Output Source Current	400		μA	V_{OUT} = 3.6V, V_{DD} = 5V
I_{OLPF}	$\overline{PF}$ Output Sink Current	100		μA	V_{OUT} = 0.4V, V_{DD} = 3V
I_{OHPF}	$\overline{PF}$ Output Source Current	100		μA	V_{OUT} = 3.6V, V_{DD} = 5V
	CMOS to CMOS				
V_{IL}	Logic "0" Input Voltage		1.5	V	All inputs, V_{DD} = 5V
V_{IH}	Logic "1" Input Voltage	3.5		V	All inputs, V_{DD} = 5V
V_{OL}	Logic "0" Output Voltage		0.5	V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$, I_O = 10μA, V_{DD} = 5V
V_{OH}	Logic "1" Output Voltage	4.5		V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$, I_O = -10μA, V_{DD} = 5V
	Current Levels				
I_{DD}	Quiescent Current		25	μA	Standby, V_{DD} = 5V
I_{DD}	Operating Current		500	μA	All valid input combinations, $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$ outputs open V_{DD} = 5V
I_{IL}, I_{IH}	Input Current Any Pin (keyboard inputs)	10	100	μA	V_{IN} = V_{SS} or V_{DD}, V_{DD} = 5V
I_{IL}, I_{IH}	Input Current All Other Pins		100	nA	V_{IN} = V_{SS} or V_{DD}, V_{DD} = 5V
I_{OZ}	Output Current in High Impedance State		1	μA	V_{DD} = 5V, V_{OUT} = 0V data outputs (D1-D4)
			-1	μA	V_{DD} = 5V, V_{OUT} = 5V
fo	Oscillator Frequency	4	10	kHz	V_{DD} = 5V (min. duty cycle 30/70)
Δfo/fo	Frequency Deviation	-3	+3	%	V_{DD} - V_{SS} from 4.5V to 5.5V. Fixed R-C oscillator components 50kΩ ⩽ R_M ⩽ 750kΩ; 1MΩ ⩽ R_I ⩽ 5MΩ; 150pF ⩽ C_O ⩽ 3000pF; 330pF most desirable value for C_O, fo < 10kHz over the operating temperature and unit-unit variations
C_{IN}	Input Capacitance, Any Pin		7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off (V_{SS} ⩽ V_I ⩽ V_{DD} as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

Functional Description

The S2562 is a CMOS controller designed for storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101 256x4 RAM that functions as a telephone number storage. A single S5101 RAM will store up to 32 8-digit or 16 16-digit telephone numbers. The S2562 can be programmed to work with either 8-digit or 16-digit numbers by means of the Number Length Select (NLS) input.

The S2562 uses an inexpensive, but accurate R-C oscillator as a time base from which the dialing rate and inter-digit pause duration (IDP) are derived. Different dialing rates and IDP durations can be implemented by simply adjusting the oscillator frequency. The dialing rate and IDP can be further changed by a 2:1 factor by means of the dialing rate select (DRS) and inter-digit pause select (IPS) inputs. Thus, for the oscillator frequency of 8kHz, dialing rates of 10 and 20 pps and IDP's of 400 and 800ms can be achieved. The mark/space ratio is fixed independent of the time base and can be selected to be either 33-1/3 / 66-2/3 or 40/60 by means of M/S input. Over supply voltage (5V ±10%), operating temperature range and unit-unit variations, timing accuracy of ±3% can be achieved. A mute output is also available for muting of the receiver during dial pulsing. See Figure 5 for timing relationship.

The S2562 can be programmed by means of the MODE input for dual tone signaling applications as well. In this mode, it can interface directly with the AMI standard S2559 Tone Generator to produce the required DTMF signals. The tone on/off rate during an auto dial operation in this mode is derived from the time base. For the oscillator frequency of 8kHz, a tone drive rate of 50ms on, 50ms off is obtained. Different rates can be implemented by adjusting the time base as desired. See Tables 2 and 3 for the various combinations. In the tone mode, the mute output is used to gate the tone generator on and off. The 8 address lines that are normally used for addressing the RAM are also used to address the tone generator row, column inputs. Figure 6 shows a typical system application.

The S2562 can perform the following functions:

Normal Dialing

The user enters the desired number digits through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20 pps. Debouncing (min. 20ms) is provided on the keyboard entries to avoid false entries. The number entered is retained for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed the total number of digits (8 or 16).

An update pulse is generated to update the display digit as a new entry is made.

In the tone mode the tones will be transmitted at the rate the user enters the digits.

Redialing

The last number entered is retained in the internal memory and can be redialed by going "off hook" and depressing the "redial" (RDL) key. The RDL key is a unique 2 of 12 matrix location (R5, C3). The number being redialed out is displayed as it is dialed out.

In the tone mode, the redial tone drive rate depends upon the time base as discussed before.

Storing of a Normally Dialed or Redialed Number into the External Memory

After the normal dialing or redialing operation, the telephone number can be stored in the external memory for future repertory dialing use by going on hook and initiating the following key sequence.

1. Push "store" (ST) button.

2. Depress the single digit key corresponding to the desired address location.

Note that the "ST" key is a unique 2 of 12 matrix location (R5, C1).

Storing of a Telephone Number into the External Memory

This operation is performed "on hook'" and no out-dialing occurs. A telephone number can be stored in the desired address location by initiating the following key sequence.

1. Push the "*" key (This instructs the device to accept a new number for storage into the internal memory).

2. Enter the digits (including any access pauses) corresponding to the desired number.

3. Push the "ST" key.

4. Push the single digit key corresponding to the desired address location.

The entire sequence can be repeated to store as many numbers as desired.

Displaying of a Stored Telephone Number

This is an "on hook" operation. Either the last dialed number or the number stored in the external memory can be displayed one digit at a time. The key sequence for displaying the last dialed number is as follows:

1. Push the "read" (R) key.
2. Push the "RDL" key.

The number in the external memory can be displayed as follows:

1. Push the "R" key.
2. Push the single digit key corresponding to the desired address location.

Note that the "R" key is a unique 2 of 12 matrix location (R_5, C_2).

The number is displayed one digit at a time at a rate determined by the time base. With a time base of 8kHZ the display will be on 500ms, off 500ms. The display is updated by producing an update pulse. The update pulse must be decoded with external logic (one inverter and one 2-input gate) as shown in Figure 6.

The display is blanked by outputting an illegal (non BCD) code such as 1111. The 4511-type BCD to 7 segment decoder driver latch will blank the display when the illegal code is detected. When other driver circuits are employed, external logic must be used to detect the illegal code.

Repertory Dialing

This is the most common mode of usage and allows the user to dial automatically any number stored in the memory. This mode is initiated by the following key sequence after going off hook.

1. Push the "*" key.
2. Push the single digit key corresponding to the desired address location.

The number is displayed as it is dialed out. In the tone mode, the tone driver rate is dependent on the time base as described earlier.

Pause

Note that the out dialing in the repertory or redial operation continues unless an access pause is detected. The outpulsing will stop and resume only when the user terminates the access pause by pushing the "*" key again.

Power Fail Detection

This output is normally high. When the supply voltage falls below a predetermined value, it goes low. The output can then drive a suitable latching device that will switch the memory to either the tip and ring or an auxilliary battery supply.

Memory Expansion

The memory can be expanded by paralleling additional S5101 RAM's. External logic must be used to enable the desired RAM corresponding to a desired address location. The S2562 can drive up to 2 RAM's without the need of buffering address and data lines.

Keybounce Protection

When a key closure is detected by the S2562, an internal timeout (min. 4ms at fo = 8kHz) is started. Any transitions that occur during this timeout will reset the timer to zero so that a key will only be accepted as valid after a noise free timeout period. The key must remain closed for an additional 16ms before released. Thus, the total make time of the key must be at least 20ms. The key must be released for at least 1ms before a new key is activated. Any transitions occurring when the key is released are ignored as long as the make time does not exceed 4ms.

Table 1. Pin/Function Descriptions

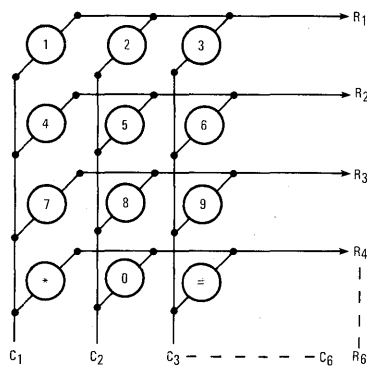| Pin	Number	Function
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 3.5V to 13.5V.
Keyboard (R_1-R_6, C_1-C_6)	12	These are 6 row and 6 column inputs from the keyboard contacts. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect to each other. Figures 1 and 2 depict the standard telephone DPCT and X-Y matrix keyboard arrangements that can be used. A logic, interface is also possible as shown in Figure 3. De-bouncing is provided to avoid false entry (typ. 20ms for oscillator frequency of 8kHz). Key pad entry options are shown in Figure 4.
Number Length Select (NLS)	1	This input permits programming of the device to accept either 8-digit numbers or 16-digit numbers.
Mode Select (MODE)	1	This input allows the use of the device in either dial pulsing applications or tone drive applications.
Dial Rate Select (DRS)	1	This input allows selection of two different dialing rates such as 10 or 20 pps, 7 or 14 pps, etc. See Tables 2 and 3.
Inter-Digit Pause Select (IPS)	1	This allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceeding the first dialed digit is an inter-digit time equal to the selected IDP. Two pause durations, either 400ms or 800ms are available at dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Mark/Space Ratio Select (M/S)	1	This input allows selection of the mark/space ratio as per Table 3.
Mute Output ($\overline{MUTE}$)	1	A pulse is available that can provide drive to turn on an external transistor to mute the receiver during dial pulsing. See Figure 5 for mute and dial pulse output relationship. It is also used as a keyboard disable in the tone drive applications. See Figure 6.
Dial Pulse Output ($\overline{DP}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. This output will be normally high and go low during "space" or "break."
Display Memory I/O Data (D_1-D_4)	4	These are 4 bidirectional pins for inputting and outputting data to the external memory and display driver.

Telecomunications

Table 1. (Continued)

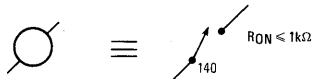| Pin	Number	Function
Memory Enable ($\overline{CE}$)	1	This line controls the external memory operation.
Memory Read/Write (R/W)	1	This line controls the read or the write operation of the external memory. This output along with the $\overline{CE}$ output can be used to produce a pulse to update the external display. See Figure 6.
Tone Generator/Memory Address (A_0-A_7)	8	These are 8 output lines that carry the external memory address and tone generator row/column information.
Hook Switch ($\overline{HS}$)	1	This input conveys the state of the subset. "Off hook" corresponds to V_{SS} condition.
Power Fail Detect ($\overline{PF}$)	1	This output is normally high and goes low when the power supply falls below a certain predetermined value.
Oscillator (OSC_i, OSC_m, OSC_o)	3	These pins are provided to connect external resistors R_I, R_M and capacitor C_O to form an R-C oscillator that generates the time base for the repertory dialer. The output dialing rate, tone drive rate and IDP are derived from this time base.
	40	

Figure 1. Standard Telephone Pushbutton Keyboard

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R_{ON} (CONTACT RESISTANCE) $\leqslant 1k\Omega$
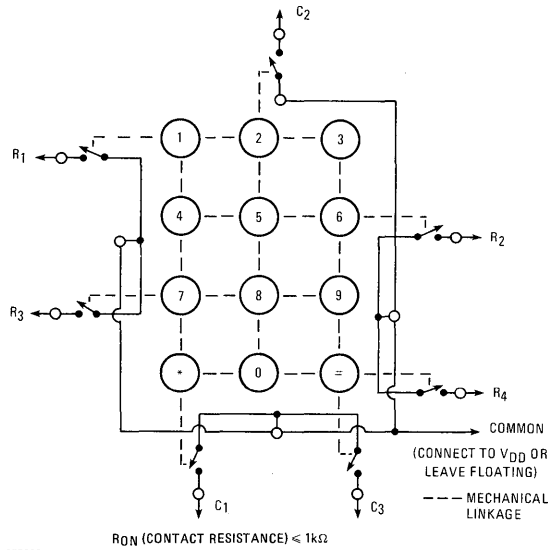
Figure 2. SPST Matrix Keyboard Arranged in the 2 of 12 Row, Column Format

SPST MATRIX KEYBOARD:

$$\bigcirc \equiv \text{140} \quad R_{ON} \leqslant 1k\Omega$$

877285

Figure 3. Logic Interface For the S2562

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G_1 through G_{12} any CMOS type logic gates.
D_1 through D_{12} DIODES type 1N 914. (Optional)
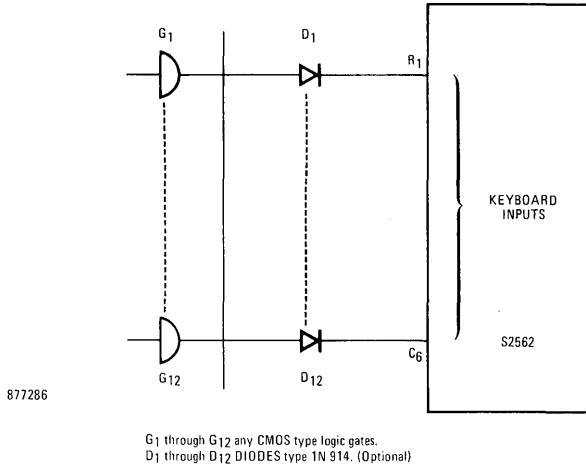
Figure 4. Example of Keypad Entry — Options

1-11 in parallel
with 1 = of
2 of 7 keypad

877287
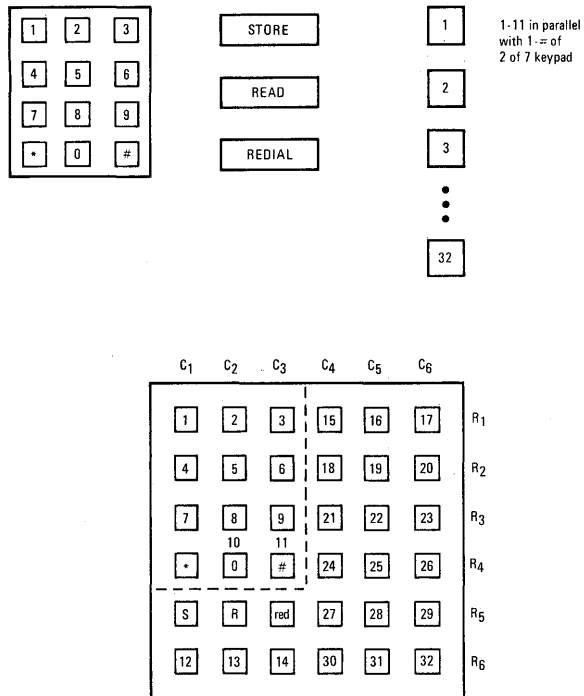
Table 2. Table for Selection of Oscillator Component Values for Desired Dialing Rate, I_{DP} or Tone Drive Rate.

Dial Rate Desired (PPS)	Osc. Freq. fo (Hz)	Oscillator Components			Dial Rate (PPS)		IDP (ms)		Tone Drive On/Off Time (ms)
		R_M (kΩ)	R_I (kΩ)	C_O (pF)	DRS = V_{SS}	DRS = V_{DD}	IPS = V_{SS}	IPS = V_{DD}	
5.5/11	4400				5.5	11	1454	727	90/90
6/12	4800				6	12	1334	667	83.3/83.3
6.5/13	5200				6.5	13	1230	615	77/77
7/14	5600				7	14	1142	571	71/71
7.5/15	6000	To Be			7.5	15	1066	533	66.7/66.7
8/16	6400	Determined			8	16	1000	500	62.5/62.5
8.5/17	6800				8.5	17	942	471	59/59
9/18	7200				9	18	888	444	55.5/55.5
9.5/19	7600				9.5	19	842	421	52.6/52.6
10/20	8000				10	20	800	400	50/50
(fo/800)/ (fo/400)	fo				fo/800	fo/400	$\dfrac{6400 \times 10^3}{fo}$	$\dfrac{3200 \times 10^3}{fo}$	$\dfrac{400 \times 10^3}{fo}/\dfrac{400 \times 10^3}{fo}$

Table 3.

Function	Pin Designation	Input Logic Level	Selection
Dial Rate Selection	DRS	V_{SS}	(fo/800) pps
		V_{DD}	(fo/400) pps
Inter-Digit Pause Selection	IPS	V_{DD}	(3200/fo) S
		V_{SS}	(6400/fo) S
Mark/Space Ratio	M/S	V_{SS}	33-1/3/66-2/3
		V_{DD}	40/60
Hook Switch	$\overline{HS}$	V_{DD}	On hook
		V_{SS}	Off hook
Mode Selection	MODE	V_{SS}	Dial pulse
		V_{DD}	Tone drive
Number Length Selection	NLS	V_{SS}	8 digits
		V_{DD}	16 digits

Note: fo is the oscillator frequency and is determined as shown in Table 2.

Telecomuni-cations

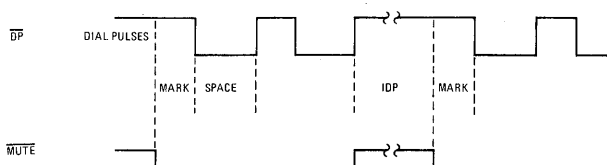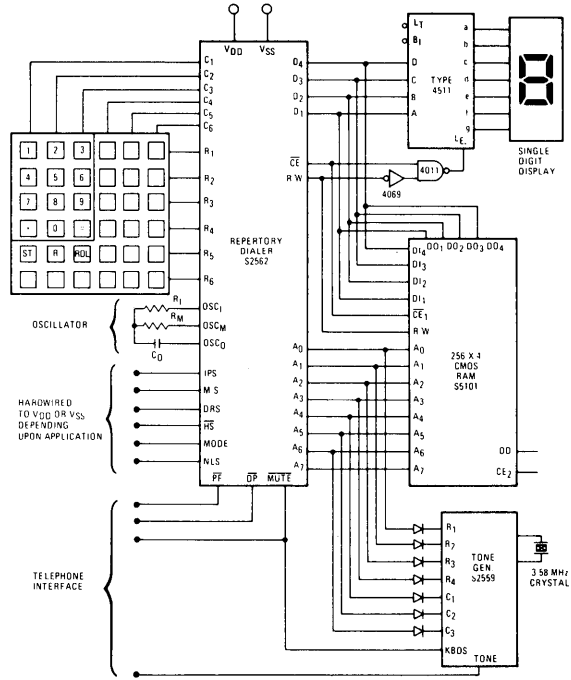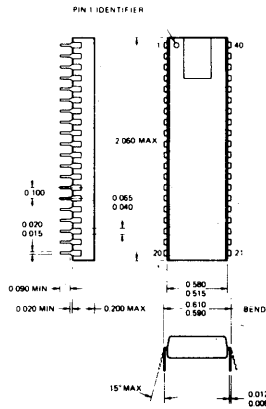Figure 5. Mute and Dial Pulse Output Timing Relationship

877288

Figure 6. Typical Application of the S2562

Physical Dimensions

AMI ®

# SIGNAL PROCESSING PERIPHERAL

Features

☐ High Speed VMOS Technology

☐ Programmable for Digital Processing of Signals in Voice-Grade Communications Systems and Other Applications with Signal Frequencies in the Range of DC to 10KHz

☐ Extremely Fast 12-Bit Parallel Multiplier On Chip (300ns Max. Multiplication Time)

☐ Built-In ROM (256 x 17), 3-Port RAM (256 x 16) and Add/Subtract Unit (ASU)

☐ Pipeline Structure for High Speed Instruction Execution (300ns Max. Cycle Time)

☐ Bus Oriented Parallel I/O for Easy Microprocessor Interface

☐ Additional Serial I/O for Easy A/D-D/A Interface

General Description

The S2811 Signal Processing Peripheral (SPP) is a high speed special purpose arithmetic processor with on-chip ROM, RAM, multiplier, adder/subtractor, accumulator and I/O organized in a pipeline structure to achieve an effective operation of one multiply, add and store of up to 12-bit numbers in 300 nanoseconds.

Block Diagram

Logic Diagram

Telecommunications

AMI®
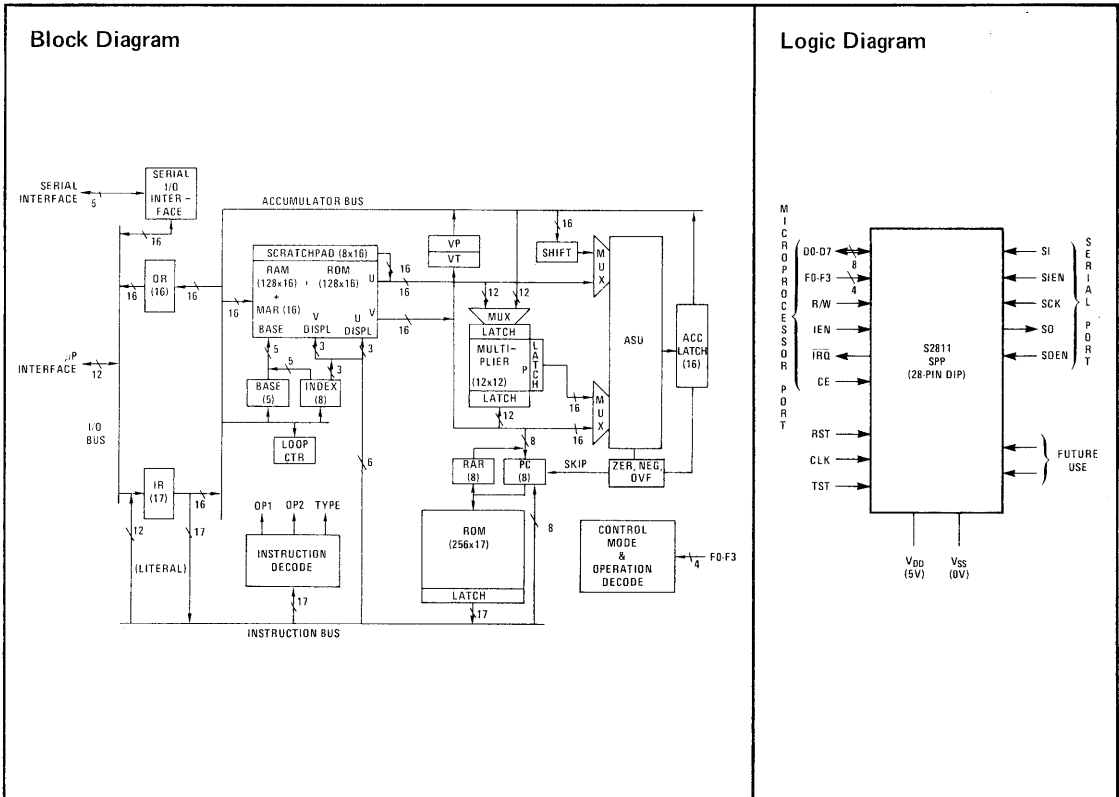
# CMOS SINGLE CHANNEL
μ-LAW PCM CODEC/FILTER SET

Features

☐ Full Independent Encoder with Filter and Decoder with Filter Chip Set
☐ Meets or Exceeds AT&T D3 and CCITTG. 712 Specifications
☐ On-Chip Phase-Lock Loop Derives All Timing
☐ Low Power Dissipation — Power Down Mode
☐ Wide Supply Voltage Range
☐ Low Absolute Group and Relative Delay Distortion
☐ Single Negative Polarity Voltage Reference Input
☐ Encoder with Filter Chip Has Built-In Auto Zero Circuit that Eliminates Long Term Drift Errors and Need for Trimming
☐ Serial Data Rates from 56KHz to 3.088MHz at 8KHz Nominal Sampling Rate
☐ Programmable Gain Input/Output Amplifier Stage
☐ CCIS* Compatible A/B Signaling Option

General Description

The S2900 and S2901 form a monolithic CMOS Companding Encoder/Decoder chip set designed to implement the per channel voice frequency. CODECS used in PCM Channel Bank and PBX systems requiring a μ-255 law transfer characteristic. Each chip contains two sections: (1) a band-limiting filter, and (2) an analog ↔ digital conversion circuit that conforms to the μ-255 law transfer characteristic. Transmission and reception of 8-bit data words containing the analog information is performed at 1.544Mb/s rate with analog sampling occurring at 8KHz rate. A strobe input is provided for synchronizing the transmission and reception of time multiplexed PCM information of several channels over a single transmission line.
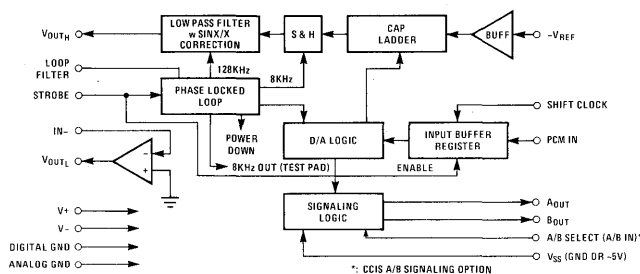
*Common Channel Interoffice Signaling
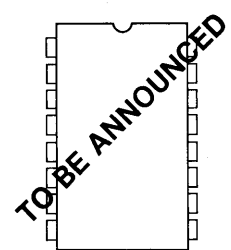
S2900 Block Diagram Encoder with Filter
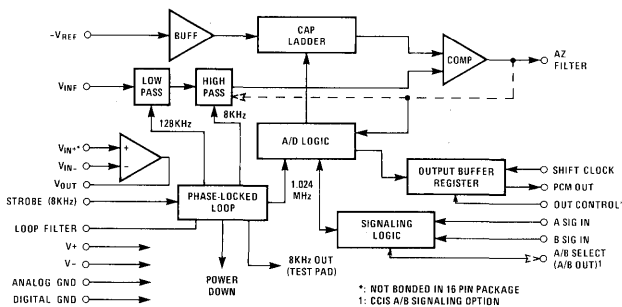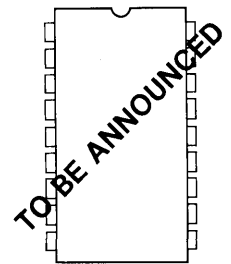
Pin Configuration

S2901 Block Diagram Decoder with Filter

Pin Configuration

S2900/S2901 Typical Group Delay Characteristic

Device	Abs. Gr. Delay μs		Relative Gr. Delay Distortion (Over Band of 1000Hz to 2600Hz wrt 1000Hz)μs
	f = 1000Hz	f = 2600Hz	
Encoder Low Pass	166.4	250	83.6
Encoder High Pass	104.0	22	−82.0
Encoder (Total)	270.4	272	1.6
Decoder Low Pass	153.0	250.0	97.0
Encoder + Decoder (Total)	423.4	522.0	98.6

AMI®

7

REMOTE CONTROL CIRCUITS

PART NO.	DESCRIPTION	PROCESS	POWER SUPPLIES	I/O BITS	PACKAGES
S2600	Remote Control Transmitter	CMOS	+7V to +10V	11	16 Pin
S2601	Remote Control Receiver	P-I²	+10V to +18V	5	22 Pin
S2742	Remote Control Decoder	P-MOS	+9V		18 Pin
S2743	Remote Control Encoder	P-MOS	+9V		16 Pin

TOUCHCONTROL™ INTERFACE CIRCUITS

PART NO.	DESCRIPTION	PROCESS	POWER SUPPLIES	INPUT/OUTPUT	PACKAGES
S9260/61	Seven-Switch Interface	P-I²	−13.5V to −18V	CMOS/TTL	22 Pin
S9263/64/65	Sixteen-Switch Interface	P-I²	−13.5V to −18V	CMOS/MOS/TTL	40 Pin
S9262	Fourteen-Switch Interface	P-I²	−13.5V to −18V	MOS/TTL	22 Pin
S9266	Thirty-Two-Switch Interface	P-I²	−13.5V to −18V	MOS/TTL	40 Pin

CONSUMER CIRCUITS

PART NO.	DESCRIPTION	PROCESS	POWER SUPPLIES	DIGITS	PACKAGES
S1424A	Five Function LCD Watch with alternating time/date mode and voltage tripler display options	CMOS	+1.5V	3½	Die
S1424C	Five Function LCD Watch Circuit	CMOS	+1.5V	3½	Die
S1425A	Five Function LCD Watch Circuit	CMOS	+1.5V	3½	Chip Carrier
S1427A	Five Function LCD Watch Circuit	CMOS	+1.5V	3½	40 Pin
S1865	Digital Clock Circuit — LED/Gas Discharge Auto Clock	P-I²	+6V to +16V	3½	40 Pin
S1998A	50/60Hz Line LED Clock Circuit	P-I²	+8V to +26V	4	40 Pin
S1998B	50/60Hz Line Clock — Gas Discharge	P-I²	+8V to +33V	4	40 Pin
S2709	Fluorescent Automotive Digital Clock	P-I²	+12V	4	22 Pin
S2733	Six Function LCD Watch Circuit	CMOS	+1.5V	4	40 Pin

ORGAN CIRCUITS

PART NO.	DESCRIPTION	PROCESS	POWER SUPPLIES	POWER DISSIPATION	PACKAGES
S10110	Analog Shift Register	P-I²	−24V		8 Pin
S10111	Analog Shift Register	P-I²	−24V		8 Pin
S10129	Six-Stage Frequency Divider	P-I²	−14V, −27V	350mW	14 Pin
S10130	Six-Stage Frequency Divider	P-I²	−14V, −27V	350mW	14 Pin
S10131	Six-Stage Frequency Divider	P-I²	−14V, −27V	350mW	14 Pin
S10377	Analog Shift Register	P-I² MOS			8 Pin
S10430	Divider-Keyer	P-I² MOS			40 Pin
S2193	Seven-Stage Frequency Divider	P-I²	−14V, −28V	300mW	14 Pin
S2567	Rhythm Counter	HI V$_T$	−15V, −27V	400mW	14 Pin
S8890	Rhythm Generator	P-I²	−12V	400mW	40 Pin
S9660	Rhythm Generator	P-I²	−12V	400mW	28 Pin
S50240	Top Octave Synthesizer	P-I²	−11V, −16V	360mW	16 Pin
S50241	Top Octave Synthesizer	P-I²	−11V, −16V	360mW	16 Pin
S50242	Top Octave Synthesizer	P-I²	−11V, −16V	360mW	16 Pin
S50243	Top Octave Synthesizer	P-I²	−11V, −16V	360mW	16 Pin
S50244	Top Octave Synthesizer	P-I²	−11V, −16V	360mW	16 Pin
S50145	Top Octave Synthesizer	P-I²	−11V, −16V	360mW	16 Pin

AMI®

ENCODER/DECODER
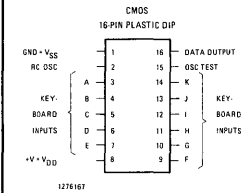# REMOTE-CONTROL 2-CHIP SET

Features

- Small Parts Count — No Crystals Required
- Easily Used in LED, Ultrasonic, RF, or Hard-wire Transmission Schemes
- Very Low Reception Error
- Low Power Drain CMOS Transmitter for Portable and Battery Operation
- 31 Commands — 5-bit Output Bus with Data Valid

- 3 Analog (LP Filterable PWM) Outputs
- Muting (Analog Output Kill/Restore)
- Indexing Output — 2½ Hz Pulse Train
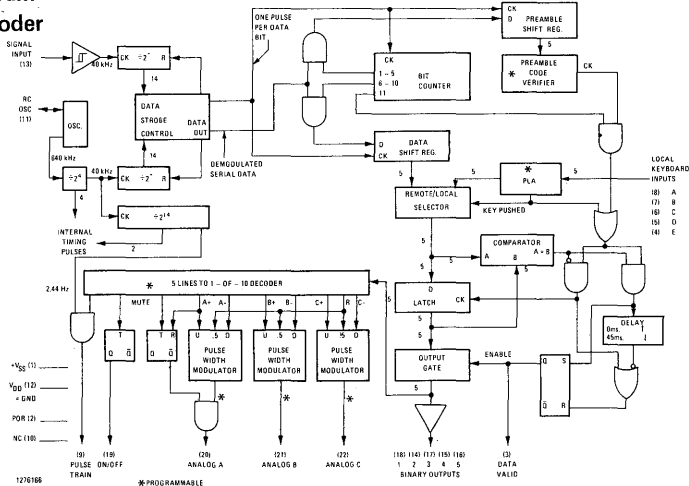- Toggle Output (On/Off)
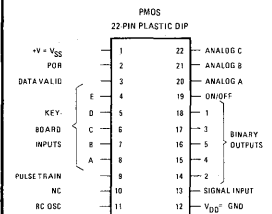- Mask-Programmable Codes

Block Diagram S2600 Encoder

Pin Configuration S2600

CMOS
16-PIN PLASTIC DIP

GND = V_{SS}	1	16	DATA OUTPUT
RC OSC	2	15	OSC TEST
A	3	14	K
KEY-BOARD	B	4	13	J	KEY-BOARD
INPUTS	C	5	12	I	INPUTS
	D	6	11	H	
	E	7	10	G	
+V = V_{DD}	8	9	F	

1276167
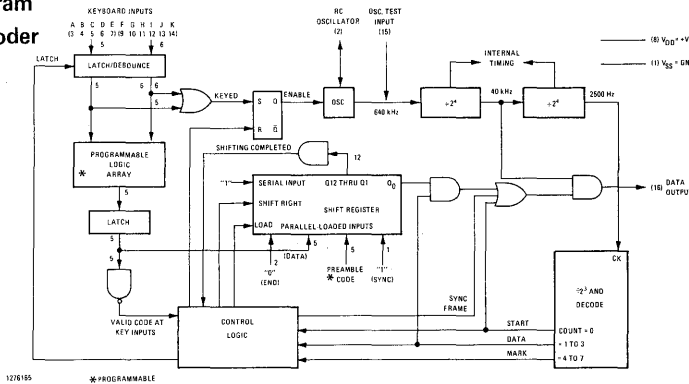
Block Diagram S2601 Decoder

Pin Configuration S2601

PMOS
22-PIN PLASTIC DIP

+V = V_{SS}	1	22	ANALOG C
POR	2	21	ANALOG B
DATA VALID	3	20	ANALOG A
KEY-BOARD INPUTS	E 4	19	ON/OFF
	D 5	18	1
	C 6	17	2	BINARY OUTPUTS
	B 7	16	3	
	A 8	15	4	
PULSE TRAIN	9	14	5	
NC	10	13	SIGNAL INPUT
RC OSC	11	12	V_{DD} = GND

1276168

Interface

7.3

Functional Description

The S2600/S2601 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a synchronizing marker technique has eliminated the need for highly accurate frequencies generated by crystals. The S2600 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 thru 6 constitute a fixed preamble which must be received correctly for the command bits to be received, and bits 7 thru 11 contain the command data. The S2601 Decoder produces an output only after two complete, consecutive, identical, 12-bit transmissions. Marker pulses, preamble bits, and redundant transmissions, have given the S2600/S2601 system a very high immunity to noise, without a large number of discrete components.

S2600 Encoder

The S2600 is a CMOS device with an on-chip oscillator, 11 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator requires only an external resistor and capacitor, and to conserve power, runs only during transmission. Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group A thru E is activated with one from the group F thru K, the keyboard encoder generates a 5-bit code, as given in the table entitled ((S2600/S2601 CODING," below. This code is loaded into a shift register in parallel with the sync, preamble, and end bits, to form the 12-bit message.

The transmitter output is a 40 kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in 38.4 milliseconds. The minimum number of tranmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The Test Input is used for functional testing of the device. A low level input will cause the oscillator frequency to be gated to the Data Output pin. This input has an internal pull-up resistor to V_{DD}.

S2601 Decoder

The S2601 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40 kHz signal input, and 11 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2601, overriding any 40 kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40 kHz signal from the local RC oscillator timing chain. A 40 kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ± 24% with respect to the receiver oscillator frequency.

Decoded data bits from the next five bit frames following the initial synchronizing frame are compared with the fixed preamble code. The next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, and if the preamble bits are correct, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next 12-bit transmission. In the case where 2 identical, proper, 12-bit transmissions are immediately followed either by transmissions with erroneous preamble codes or by

nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

The S2601 has five other outputs: Pulse Train, On/Off, Analog A, Analog B, and Analog C. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated. The Pulse Train output provides a 2.44 Hz square wave (50% duty factor) whenever 11011 appears at the Binary Outputs, but otherwise it remains at a logic "0". This pulse train can be used for indexing, e.g., for stepping a TV channel selector.

The On/Off ("mains") output changes state each time 01111 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

Analog Outputs A, B, and C are 10 kHz pulse trains whose duty factors are independently controllable. With a simple low-pass filter each of these outputs can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. Each Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code — 6 codes in all. The entire range of 0% to 100% duty factor can be traversed in 26 seconds or at a rate of the oscillator frequency divided by 262,144. All three Analog Outputs are set to 50% duty factor whenever 01011 appears at the Binary Outputs. Analog A is mutable; 01100 sets it to 0% duty factor. If 01100 then disappears and reappears, the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2601 has an on-chip power-on reset (POR) circuit which sets the Pulse Train and On/Off Outputs to "0," sets the Analog Outputs at 50% duty factor, and insures that Analog A is muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

Message Bit Format
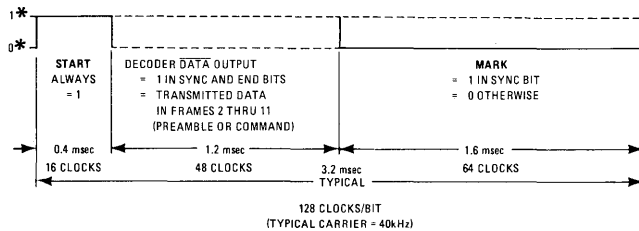
Message Format
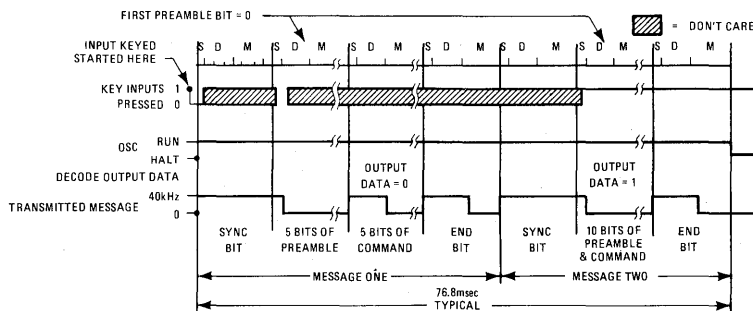
S2600/S2601 Coding

Transmitter Keyboard Input Pins Tied to V$_{SS}$	Receiver Keyboard Input Pins Tied to V$_{DD}$ (See Note 1)	1	2	3	4	5	Receiver Dedicated Functions (Mask programmable except for rest state)
AB	–	0	0	0	0	0	
AF	–	0	0	0	0	1	
AG	–	0	0	0	1	0	
AH	–	0	0	0	1	1	
AI	BC	0	0	1	0	0	Increase Analog C pulse width
AJ	–	0	0	1	0	1	
AK	–	0	0	1	1	0	
BF	AE	0	0	1	1	1	Decrease Analog B pulse width
BG	–	0	1	0	0	0	
BH	–	0	1	0	0	1	
BI	–	0	1	0	1	0	
BJ	DE	0	1	0	1	1	RESET Analog (See Note 2)
BK	CE	0	1	1	0	0	MUTE (See Note 3)
CF	–	0	1	1	0	1	
CG	–	0	1	1	1	0	
CH	CD	0	1	1	1	1	Toggle On/Off Output
CI	–	1	0	0	0	0	
CJ	–	1	0	0	0	1	
CK	–	1	0	0	1	0	
DF	AD	1	0	0	1	1	Increase Analog B pulse width
DG	BD	1	0	1	0	0	Decrease Analog C pulse width
DH	–	1	0	1	0	1	
DI	–	1	0	1	1	0	
DJ	AB	1	0	1	1	1	Increase Analog A pulse width
DK	–	1	1	0	0	0	
EF	–	1	1	0	0	1	
EG	–	1	1	0	1	0	
EH	BE	1	1	0	1	1	Activate Pulse Train Output
EI	–	1	1	1	0	0	
EJ	–	1	1	1	0	1	
EK	AC	1	1	1	1	0	Decrease Analog A pulse width
–	–	1	1	1	1	1	Rest State

NOTES:
1. Receiver keyboard inputs override any remote signal input.
2. Sets Analog A, B, and C waveforms to 50% Duty Factor.
3. First operation sets Analog A to 0% Duty Factor; second operation restores former Analog A Duty Factor.

Electrical Specifications — 2600 Encoder

All voltages measured with respect to V$_{SS}$.

Absolute Maximum Ratings

Operating ambient temperature T$_A$ .... 0 to +70°C
Storage temperature .... – 65°C to +150°C
Positive voltage on any pin .... +14V
Negative voltage on any pin .... – 0.3V

Electrical Characteristics

Unless otherwise noted, V$_{DD}$ = 8.5 ± 1.5V and T$_A$ = 0 to +70°C.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f0	Oscillator frequency	7	640	2000	kHz	R$_{OSC}$ = 12K, C$_{OSC}$ = 100pF
Δf0/f0	Frequency deviation	– 10		+10	%	Fixed R$_{OSC}$, C$_{OSC}$, V$_{DD}$ ± 10%
I$_{DD}$	Supply current			2	mA	During transmission, Data Output = 1mA
	Standby			10	μA	No transmission (25°C)
V$_{IH}$	Input "1" threshold	25	50		%V$_{DD}$	
V$_{IL}$	Input "0" threshold		50	75	%V$_{DD}$	
I$_{IL}$	Input source current	50		200	μA	V$_I$ = 0V
I$_{OH}$	Output source current	1	1.5		mA	V$_0$ = V$_{DD}$ – 3V
I$_{OL}$	Output sink current	– .2	– .5		mA	V$_0$ = +0.5V

Note: Circuit operates with V$_{DD}$ from 3.0V to 12.0V.

Electrical Specifications — S2601 Decoder

All voltages measured with respect to V_{DD}.

Absolute Maximum Ratings

Operating ambient temperature T_A .... $0°C$ to $70°C$
Storage temperature .... $-65°C$ to $+150°C$
V_{SS} power supply voltage .... $+31V$
Positive voltage on any pin .... $V_{SS} +0.3V$
Negative voltage on any pin .... $V_{SS} -31V$

Electrical Characteristics

Unless otherwise noted, $V_{SS} = 14 \pm 4V$ and $T_A = 0$ to $+70°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f0	Oscillator frequency	7	640	2000	kHz	$R_{OSC} = 71K, C_{OSC} = 25pF$
$\Delta f0/f0$	Frequency deviation	-10		$+10$	%	Fixed R_{OSC}, C_{OSC}, V_{SS}
I_{SS}	Supply current		34	50	mA	No loads, $V_{DD} = 18V$
			28		mA	$V_{DD} = 10V$
Signal Input:						
V_{IH}	"1" threshold		70	85	$\%V_{SS}$	
V_{IL}	"0" threshold	30	48		$\%V_{SS}$	
V_{IH}-V_{IL}	Voltage hysteresis	5		35	$\%V_{SS}$	
Keyboard and POR Inputs:						
V_{IH}	"1" voltage	$V_{SS} - .5$	$V_{SS}- 3.0$		V	
V_{IL}	"0" voltage			$V_{SS} - 5.5$	V	
I_{IL}	Source current	50	150	300	μA	$V_I = V_{SS} - 10V$
	Debounce delay (Keyboard inputs only)	1.45		2.2	msec	
Binary Outputs (open source):						
I_{OL}	Sink current	-1.28			mA	$V_0 = V_{SS} - 5.2V, V_{SS}=18V$
		-0.50	-0.60		mA	$V_0 = V_{SS} - 5.2V, V_{SS}=10V$
	Duration	34.9			msec	f0 = Max = 704 kHz
Analog Outputs (open drain):						
ΔV_{step}	Step Voltage change		$V_{SS}/64$		V	
I_{OH}	Source current		1.04		mA	$V_0 = V_{SS} - 0.5V, V_{SS}=10V$
			1.15		mA	$V_0 = V_{SS} - 0.5V, V_{SS}=18V$
		1.0	1.2		mA	$V_0 = V_{SS} - 1V$
f_{step}	Analog step rate		10		kHz	$(f0 \div 64)$
Data Valid, Pulse Train, and On/Off Outputs:						
I_{OH}	Source current	1	1.5		mA	$V_0 = V_{SS} - 2V$
I_{OL}	Sink current	-40	-50		μA	$V_0 = .7V$
t_r	Risetime (.1V_{SS} to .9 V_{SS})			10	μsec	$R_L = \infty, C_L$ 50pF
t_f	Falltime (.9V_{SS} to .1 V_{SS})			10	μsec	$R_L = \infty, C_L$ 50 pF

Note: Circuit operates with V_{SS} from 7.0V to 30.0V

Interface

Circuit Application
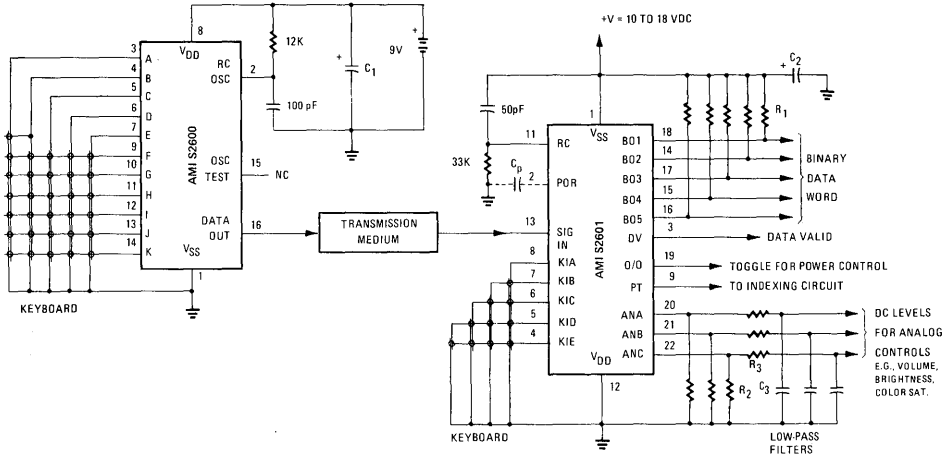
1276172
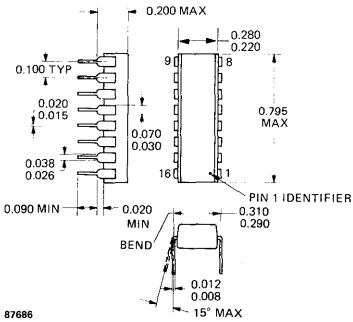
RIPPLE ON FILTER OUTPUT <10mV p-p USING R₂ = 10K, R₃ = 100K, C₃ = 0.47 μF, V$_{SS}$ = 14VDC
C1, C2, AND Cp OPTIONAL

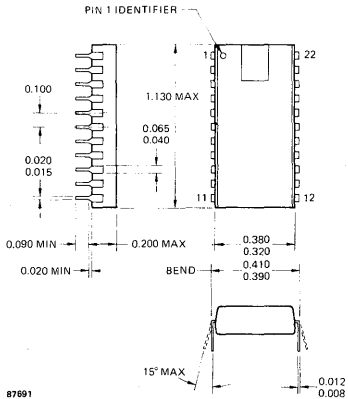## Package Outline
S2600 Encoder

16-Pin Plastic

87686

Package Outline
S2601 Decoder

22-Pin Plastic

87691

7.8

AMI ®

TOUCH
CONTROL

SWITCHING

The AMI® TouchControl Kit
TCK-100

Instructions for Assembly and Operation

INTRODUCTION

The AMI TouchControl kit demonstrates the ease with which this unique system of capacitive switching may be implemented. Included in the kit are a printed circuit board and AMI's newly developed S9263 TouchControl circuit. The printed wiring board, which has 16 touch switches etched onto its top surface, contains on its reverse side all the interconnection necessary to interface the S9263 inputs with the 16 touch switches and the S9263 outputs with 16 light emitting diodes. As the touch switches are activated, the corresponding diodes are lighted to indicate the output states of the S9263. If desired, external logic may be operated by connecting a cable directly to the S9263 outputs.

Additional components required for the kit are readily available, and assembly of the kit should take less than an hour's time. The circuit board may be mounted either on standoffs or on a standard aluminum chassis box.

Interface

PARTS LIST FOR AMI TOUCHCONTROL KIT:

QUANTITY REQUIRED	DESCRIPTION	QUANTITY REQUIRED	DESCRIPTION
1	S9263 TouchControl circuit (Included)	16	3.3KΩ Resistor ¼ Watt
1	Printed wiring board (Included)	1	Transistor 2N3569 or equivalent
1	Transformer, 12.6 volt 300mA	1	500μF capacitor/20 volts
	Radio Shack P/N 273-1385 or equivalent	1	0.33μF capacitor
1	Line cord	1	220 pF capacitor
1	Diode IN920 or equivalent	16	Light emitting diode — MV5023
2	100KΩ Resistor ¼ Watt		or equivalent
1	60KΩ Resistor ¼ Watt	1	Aluminum chassis box — 15″ x 9″
1	15KΩ Resistor ¼ Watt		Bud # AC1421 or equivalent
1	10KΩ Resistor ¼ Watt		(optional)

ASSEMBLY

The circuit board may be assembled easily by referring to Figure 2, a view of the reverse side of the board. For appearance, it is recommended that all components except the LED's and the S9263 be mounted on the reverse side of the board, with all leads cut off flush with the board's top surface.

For convenience, a 15 volt power supply is provided on the circuit board, so that the system may be plugged into a standard 110 volt outlet. If desired, an external DC supply of 15 volts may be used, connecting the positive and negative outputs to the corresponding holes designated for C1. If a DC supply is used, the transformer, diode, and C1 may be eliminated.

OPERATION

The AMI TouchControl kit provides sixteen touch switches that interface with the S9263 to activate sixteen light emitting diodes. Each of the switches numbered from one to fifteen has a light associated with it which is labeled with the same number. The switch labeled "T" is used to select the mode of operation of the S9263, either momentary or toggle. When the LED labeled "T" is off, touch pads one through fifteen operate as momentary switches, and any switch's corresponding LED will turn on when the switch is touched, remaining on only for the duration of touching the switch. If "T" is touched, the "T" LED will turn on and stay on even after "T" is untouched. The S9263 is now operating in a toggle mode, and the brief touch of any switch from one through fifteen will cause its corresponding LED to turn on and latch. Subsequent activations of the switch will turn the LED

off and on alternately. Touching "T" once again causes the "T" LED to turn off, and the S9263 once again operates in the momentary mode. By removing the 0.33μF capacitor, it is possible to use the "T" pad as a clear switch. In this mode, all numbered pads function as "push on, push off" switches. Touching the "T" pad turns off all LED's corresponding to the numbered switches.

To operate external logic systems with the TouchControl kit, a cable may be soldered, using a grounded soldering iron, directly to the outputs of the S9263. The voltage on an output that is turned off (corresponding LED is off) is – 15 volts (or V_{DD}). When turned on, the output will rise towards ground (V_{SS}). Appropriate loading conditions are specified in the advanced product description for this part.
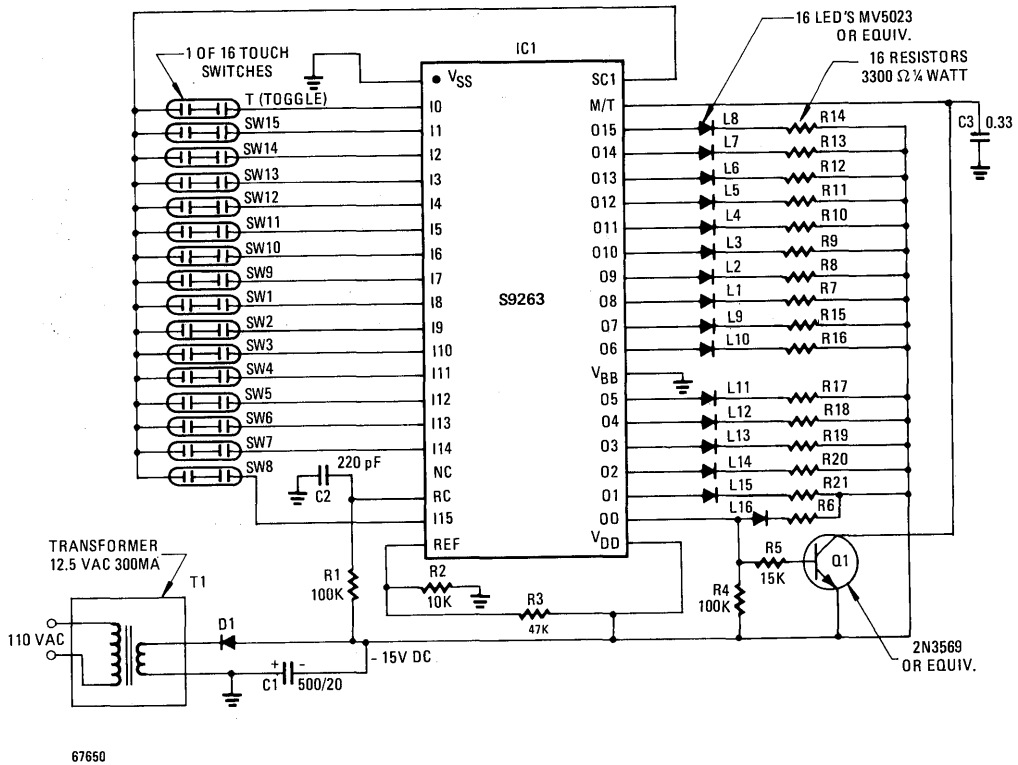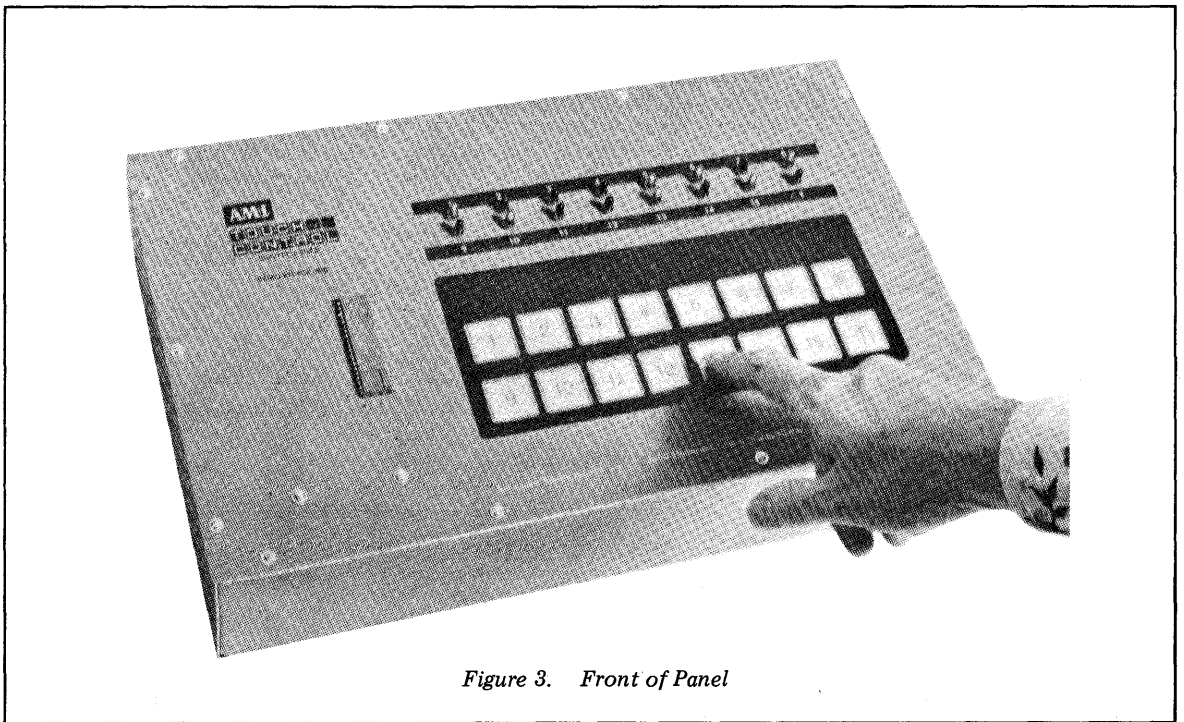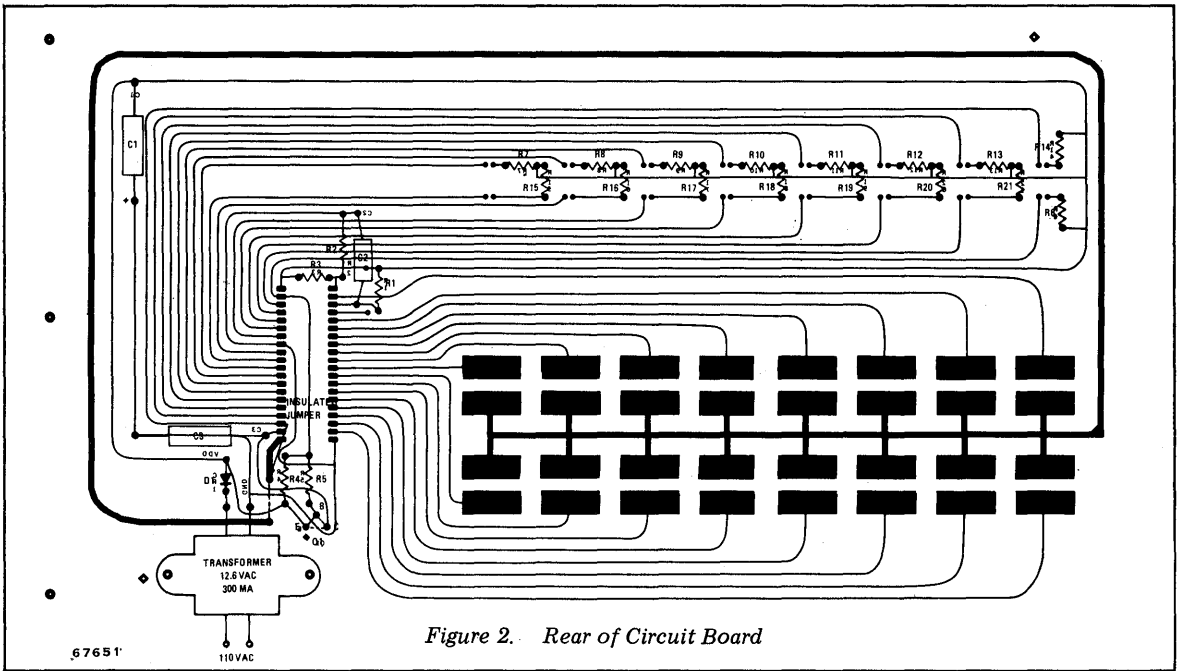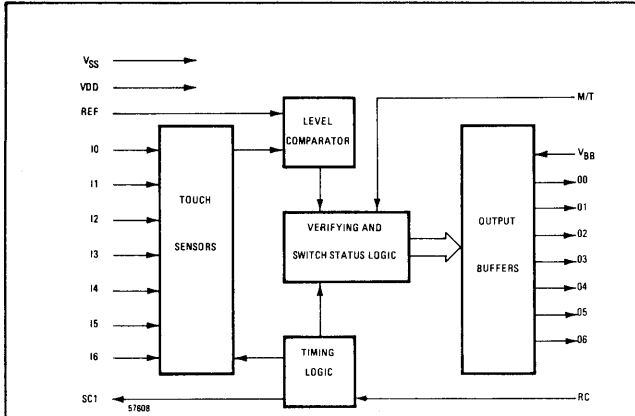
16 LED'S MV5023 OR EQUIV.

16 RESISTORS 3300 Ω ¼ WATT

1 OF 16 TOUCH SWITCHES

IC1

● V$_{SS}$ SC1

T (TOGGLE)

SW15 I0 M/T
SW14 I1 O15 L8 R14 C3 0.33
SW13 I2 O14 L7 R13
SW12 I3 O13 L6 R12
SW11 I4 O12 L5 R11
SW10 I5 O11 L4 R10
SW9   I6 O10 L3 R9
SW1   I7 O9   L2 R8
SW2   I8 O8   L1 R7
SW3   I9 O7   L9 R15
SW4   I10 O6   L10 R16
SW5   I11 V$_{BB}$
SW6   I12 O5   L11 R17
SW7   I13 O4   L12 R18
SW8   I14 O3   L13 R19
      220 pF O2 L14 R20
      C2 NC   O1 L15 R21
      RC O0   L16 R6
      I15 V$_{DD}$
      REF

S9263

R5 15K Q1

TRANSFORMER 12.5 VAC 300MA
T1

R1 100K R2 10K R3 47K

R4 100K

110 VAC

D1

- 15V DC

C1 500/20

2N3569 OR EQUIV.

67650

Figure 1.   Schematic Diagram of TCK-100
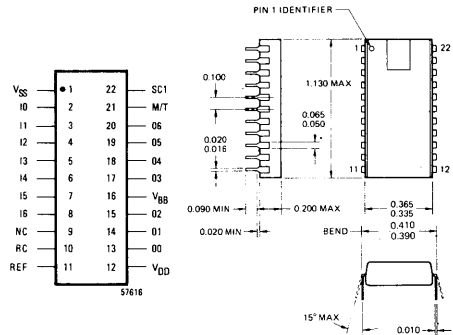
PARTS LIST FOR ASSEMBLING TCK − 100 KIT:

PART NUMBER	PART DESCRIPTION	PART NUMBER	PART DESCRIPTION
R1, R4	100 KΩ ¼ Watt resistor	Q1	NPN transistor 2N3569 or equivalent
R2	10 KΩ ¼ Watt resistor	D1	Diode IN920 or equivalent
R3	47KΩ ¼ Watt resistor	L1 thru L16	Light emitting diode — MV5023 or
R5	15 KΩ ¼ Watt resistor		equivalent
R6 thru R21	3.3 KΩ ¼ Watt resistor	IC1	AMI integrated circuit S9263
C1	500 μF capacitor 20 Volts	T1	Transformer 12, 6 VAC @ 300 mA.
C2	220 pF capacitor		Radio Shack P/N 273-1385
C3	0.33 μF capacitor		or equivalent

Interface

Figure 2. Rear of Circuit Board
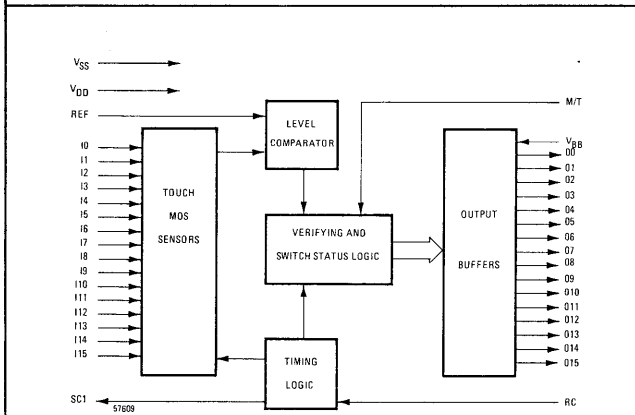

Figure 3. Front of Panel

TOUCHCONTROL INTERFACE

BLOCK DIAGRAM – S9260/S9261 (7 SWITCHES)

**PIN/PACKAGE CONFIGURATION
S9260/S9261**

BLOCK DIAGRAM – S9263/S9264/S9265 (16 SWITCHES)
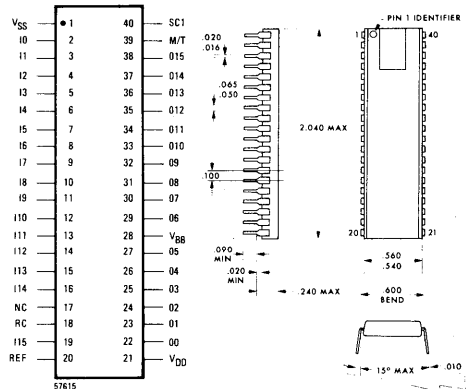
**PIN/PACKAGE CONFIGURATION
S9263/S9264/S9265**

Interface

FEATURES

- Interfaces with up to 16 touch switches
- Eliminates contact noise
- Comparator sensing permits use with wide variety of touch switch configurations
- Momentary or toggle operation electrically selectable
- Outputs are TTL/CMOS/MOS compatible
- Simplifies design of touch-sensitive switches

TOUCH CONTROL

GENERAL DESCRIPTION

The S9260 series of MOS TouchControl interface circuits permits almost any control panel containing mechanical switches to be easily replaced by a flat-surface capacitive control panel providing superior styling, reliability, ease of cleaning, and safety. Connecting directly to a screened or etched pattern on the panel's reverse side, these MOS circuits provide outputs to drive a variety of logic systems from household appliances to industrial controls. All system functions are then selected by merely touching the flat conductive Touch-Control "switch" areas that have been deposited on the panel's front surface in practically any configuration desired.

These circuits provide an individual output for each of up to 16 TouchControl switches. For applications requiring more switches or encoded outputs, refer to AMI's S9262 and S9266, which can interface with up to 32 switches.

FUNCTIONAL DESCRIPTION

Fabricated with P-channel ion implanted MOS/LSI technology, the S9260 family* of TouchControl integrated circuits has been designed to interface with a variety of touch panel switches and provide a high degree of flexibility in the selection of touch panel materials, layout of touch pad configurations, and design of switching functions. These circuits can interface directly with either seven TouchControl switches (22 lead versions) or sixteen TouchControl switches (40 lead versions). For each TouchControl switch input there is a corresponding output that may be used to interface with various logic families such as CMOS or TTL.

Both momentary and "push on – push off" (toggle) switching operations are available on all AMI TouchControl circuits and are electrically selected by the logic levels of one input pin. To ensure reliable switch action, a built-in delay is incorporated in all circuits requiring a minimum touch time for switch response.

TYPICAL APPLICATIONS

- Appliance Control Panels
- Home Entertainment Systems
- Power Tool Controls
- Televisions
- Automotive Controls

- Telephones
- Games
- Fast Food Waterproof Keyboards
- Moisture Proofing
- Industrial Controllers
- Computer Terminals

- Keyboards
- Instrumentation
- 16 to 1 Multiplexers
- Microprocessor Interface
- Vending Machines
- Cash Registers

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}:	+ 0.3V to – 20V	Storage temperature (Ambient)	– 65°C to + 150°C
Operating temperature range:	0°C to + 70°C		

FOR MULTIPLEXED TOUCHCONTROL CIRCUITS SEE AMI S9262 and S9266.

ELECTRICAL CHARACTERISTICS

($0°C < T_A < 70°C$; $V_{SS} = 0V$; $V_{DD} = -13.5V$ to $-18.0V$ unless otherwise specified.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input logic 0 level — all except "I" inputs.	+0.3	0	-1.5	Volts	Note: M/T input is internally pulled up to V_{SS}
V_{IH}	Input logic 1 level — all except "I" inputs	-10.0	-12.0	-18.0	Volts	
f_{RC}	Internal oscillator frequency measured at RC input.	50		100	kHz	
T_S T_{RST}	Switch delay time Time to reset all latches using M/T input.	65	100	135 135	msec msec	Frequency measured at RC Input = 50 kHz
V_{OL} V_{OH}	Output low voltage Output high voltage	V_{SS}		-1.0 V_{DD}	Volts	$V_{BB} = V_{SS}$; 10K resistive load to V_{DD}
V_{OL} V_{OH}	Output low voltage Output high voltage	V_{SS} $V_{BB} + 0.4$		$V_{SS} - 0.5$ V_{BB}	Volts	$V_{SS} = +5V$; $V_{BB} = 0V$ $V_{DD} = 12V$; $2800Ω$ resistive load to V_{SS}
SC1	Scan clock output: Output low voltage Output high voltage	V_{SS}		-1.5 V_{DD}		Max. capacitive loading < 150 pF
I_{DD}	Supply Current		7.0	15.0	ma	Outputs unconnected

OPERATION

Device operation can be understood by referring to Figure 1, depicting a typical application of the S9263. Each of the sixteen pairs of series capacitors labeled S1 — S16 is one touch switch located on a TouchControl panel. (For details on touch panel configuration and operation, see the TouchControl application note included in this APD.) In each capacitor pair, the two common plates represent the conductive area on the control panel surface that is to be touched. The other two plates are formed by two conductive surfaces parallel to the touched surface and located directly under it on the reverse side of the panel. Referring again to Figure 1, the S9263 generates a clock signal on output SC1 that is applied to one plate of each capacitor pair; this signal passes through the two series capacitors and is detected in the MOS circuit. When a panel switch surface is touched, the signal level into the chip dimishes, and the on-chip differential amplifier senses the change and performs the appropriate switching function. For example, if surface S1 is touched, the signal at input 13 decreases, and output 03, normally open, now becomes active and drives the S1 input to the TTL circuitry toward voltage level V_{BB}.

I INPUTS

Inputs from the touch switch pads to the TouchControl circuit are labeled I0 through I15 (S9263, S9264, and S9265) or I0 through I6 (S9260 and S9261). Each I input relates directly to an 0 output of identical numeral.
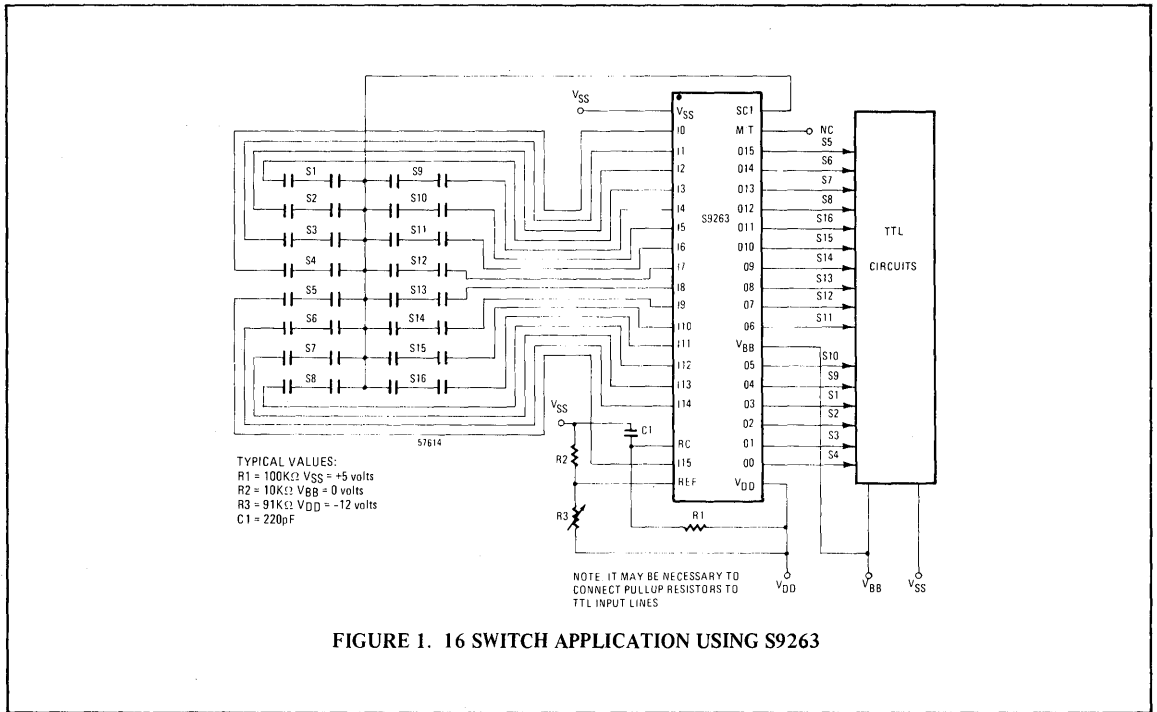
Interface

FIGURE 1. 16 SWITCH APPLICATION USING S9263

RC INPUT

A resistor connected to V_{DD} and a capacitor connected to V_{SS} are connected to the RC input pin to establish the on-chip clock frequency that controls the touch switch delay time. Nominal values for these components are suggested in Figure 1, but they may be varied to change clock frequency over a range of 50 kHz to 100 kHz.

REF INPUT

In order to allow flexibility in the choice of Touch-Control panel materials, switch layout, and switch size, AMI Touch Control inputs have been designed to detect a differential change rather than an absolute change in level. To obtain a reference level, two resistors are connected to input REF, one to V_{SS} and the other to V_{DD}.

O OUTPUTS

Each output pin labeled "O" corresponds to an input pin labeled "1." Whenever an input is selected, the output becomes active and will drive an external load toward supply voltage V_{BB}. When outputs are not active, they are high impedance open drain.

V_{BB} SUPPLY

The sources of all output devices are common and connected to pin V_{BB}. This allows TTL compatibility as shown in Figure 1, as well as the ability to drive higher level signals. For instance, if $V_{SS} = 0$ volts, $V_{DD} = -16$ volts, and $V_{BB} = V_{SS}$, then active outputs would drive a load connected to V_{DD} towards V_{SS}. The V_{BB} pin can be used also to switch analog signals; in this configuration the analog signals are applied to the "O" pins and V_{BB} is the output pin.
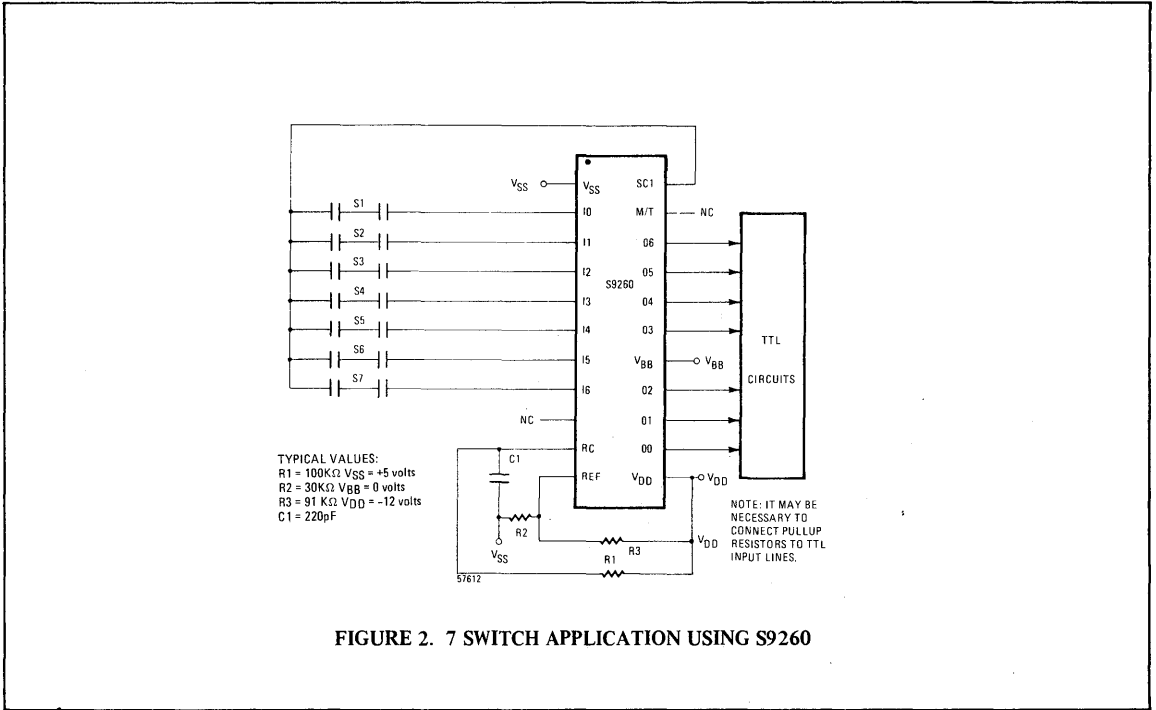
FIGURE 2. 7 SWITCH APPLICATION USING S9260

M/T INPUT

The M/T input pin selects the mode of switch operation, either momentary or toggle. With no connection to the M/T pin momentary operation is selected, and appropriate outputs are active only for the duration of touching a switch. In this mode, no output is active when no switch is touched. A V_{DD} level applied to M/T causes the circuit to operate in the toggle mode. In this condition, the brief touch of any switch will turn on the appropriate output, which will remain latched on until the switch is touched again. Subsequent activations of the switch will toggle the corresponding output on and off alternately. To reset all outputs when the toggle mode is selected, a pulse of V_{SS} level may be applied to the M/T input.

SCI OUTPUT

The SC1 output provides the clock signal for the Touch-Control panel. Its frequency is determined by the RC time constant, and it is connected in common with one of each of the two common conductive surfaces on the reverse side of the touch panel.

MOMENTARY AND TOGGLE COMBINATION

The S9261, S9264, and S9265 contain several outputs that are permanently in the momentary mode of operation.

With the M/T input at V_{SS} these parts function identically to the S9260 and S9263. With M/T at a logic 1 level, however, the S9261 has four momentary and three toggle inputs. Table 1 shows the combinations available on all three parts.

Interface

7.17

TABLE 1. COMPARISON OF FEATURES

Part Number	Pin Count	Touch Switch Capacity			Number of Outputs
		Total Touch Switch Interface Capability	Touch Inputs Selectable For Either Momentary Or Toggle Operation Through Use of M/T Input	Touch Switch Inputs Fixed In Momentary Operation (Not affected by state of M/T input)	
S9260	22	7	7	0	7
S9261	22	7	3 (I4 thru I6)	4 (I0 thru I3)	7
S9263	40	16	16	0	16
S9264	40	16	8 (I8 thru I15)	8 (I0 thru I7)	16
S9265	40	16	12 (I4 thru I15)	4 (I0 thru I3)	16

MULTIPLEXED
TOUCHCONTROL INTERFACE
SEPTEMBER 1976

BLOCK DIAGRAM – S9262 (14 SWITCHES)

PIN/PACKAGE CONFIGURATION – S9262

BLOCK DIAGRAM – S9266 (32 SWITCHES)

PIN/PACKAGE CONFIGURATION – S9266
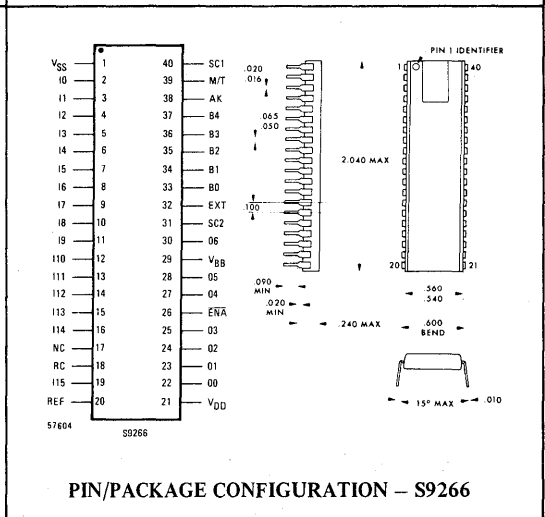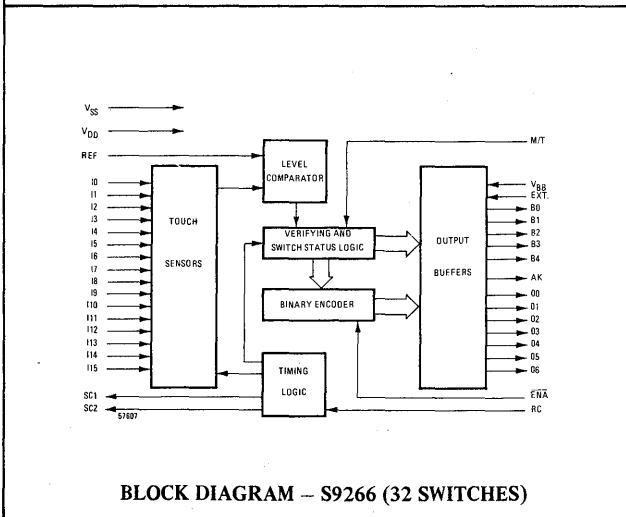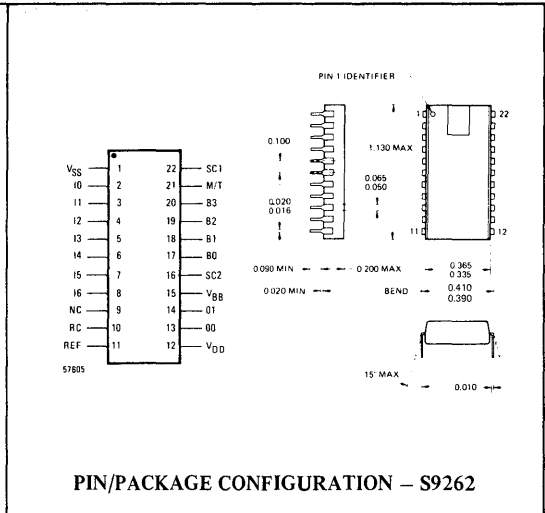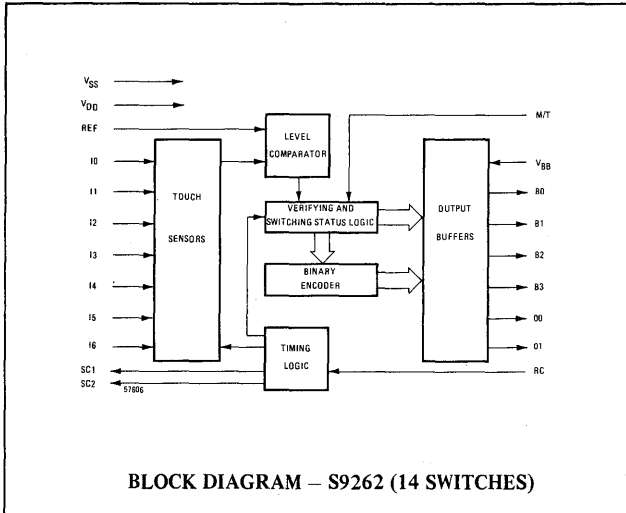
Interface

FEATURES

- Simplifies design of Touch-sensitive switches
- Interfaces with up to 32 touch switches
- Eliminates contact noise
- Comparator sensing permits use with wide variety of touch switch configurations

- Binary outputs provided
- Outputs are TTL compatible
- Permits design of totally isolated touch surfaces, facilitating UL approval

GENERAL DESCRIPTION

The S9262 and S9266 TouchControl interface circuits permit almost any control panel containing mechanical switches to be easily replaced by a flat-surface capacitive control panel providing superior styling, reliability, ease of cleaning, and safety. Connecting directly to a screened or etched pattern on the panel's reverse side, these MOS circuits provide outputs to drive a variety of logic systems from household appliances to industrial controls. All system functions are then selected by merely touching the flat conductive Touch-Control "switch" areas that have been deposited on the panel's front surface in practically any configuration desired.

These circuits can operate up to 32 TouchControl switches, and their outputs are encoded for easy interfacing with microprocessors. For applications requiring an individual output for each TouchControl switch, refer to AMI's S9260, S9261, S9263, S9264 and S9265.

FUNCTIONAL DESCRIPTION

Fabricated with P-channel ion implanted MOS/LSI technology, AMI TouchControl integrated circuits* are designed to interface with a variety of touch panel switches and provide a high degree of flexibility in the selection of touch panel materials, layout of touch pad configurations, and design of switching functions. These parts are designed to address an array of TouchControl switches in either a 2 x 7 matrix (S9262) or a 2 x 16 matrix (S9266) to interface with a total of either 14 or 32 switches. The outputs are binary encoded for easy interfacing with microprocessors or TTL, CMOS or MOS logic.

Both momentary and "push on — push off" (toggle) switching operations are available on AMI TouchControl circuits and are electrically selected by the logic level of the M/T input pin. To ensure reliable switch action, a built in delay is incorporated in all circuits requiring a minimum touch time for switch response.

TYPICAL APPLICATIONS

- Appliance Control Panels
- Home Entertainment Systems
- Power Tool Controls
- Televisions
- Automotive Controls

- Telephones
- Games
- Fast Food Waterproof Keyboards
- Moisture Proofing
- Industrial Controllers
- Computer Terminals

- Keyboards
- Instrumentation
- 16 to 1 Multiplexers
- Microprocessor Interface
- Vending Machines
- Cash Registers

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin except EXT relative to V_{SS}:	+ 0.3V to – 20V	Operating temperature range:	0°C to + 70°C
Voltage on EXT pin relative to V_{SS}:	+ 0.3V to – 27V	Storage temperature (Ambient)	– 65°C to + 150°C

*For non-multiplexed TouchControl circuits see AMI S9260, S9261, S9263, S9264, S9265

ELECTRICAL CHARACTERISTICS

($0°C \leqslant T_A \leqslant 70°C$; $V_{SS} = 0V$; $V_{DD} = -13.5V$ to $-18.0V$ unless otherwise specified.)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IL}	Input logic 0 level — all except "I" inputs.	+ 0.3	0	- 1.5	Volts	Note: M/T and $\overline{ENA}$ inputs are internally pulled up to V_{SS}.
V_{IH}	Input logic 1 level — all except "I" inputs.	- 10.0	- 12.0	- 18.0	Volts	
f_{RC}	Internal oscillator frequency measured at RC input.	50		100	kHz	
T_S	Switch delay time	65		135	msec	Frequency measured at RC Input = 50 kHz.
T_{RST}	Time to reset all latches using M/T input.		100	135	msec	
V_{OL}	Output low voltage.	V_{SS}		- 1.0	Volts	$V_{BB} = V_{SS}$; 10K resistive load to V_{DD}.
V_{OH}	Output high voltage			V_{DD}		
V_{OL}	Output low voltage.	V_{SS}		$V_{SS} - 0.5$	Volts	$V_{SS} = + 5V$; $V_{BB} = 0V$ $V_{DD} = -12V$; 2800Ω resistive load to V_{SS}.
V_{OH}	Output high voltage	$V_{BB} + 0.4$		V_{BB}		
SC1, SC2	Scan clock output. Output low voltage Output high voltage.	V_{SS}		- 1.5 V_{DD}		Max. capacitive loading $\leqslant$ 150 pF.
I_{DD}	Supply Current		7.0	15.0	ma	Outputs unconnected

OPERATION

Device operation can be understood by referring to Figure 1, depicting a typical application of the S9266. Each of the 32 pairs of series capacitors labeled S1 — S32 is one touch switch located on a TouchControl panel constructed of glass, printed circuit board, epoxy, or other dielectric material. (For details on touch panel configuration and operation, see the TouchControl application note included in this APD.) In each capacitor pair, the two common plates represent the conductive area on the control panel surface that is to be touched. The other two plates are formed by two conductive surfaces parallel to the touched surface and located directly under it on the reverse side of the panel. Referring again to Figure 1, the S9266 generates a clock signal on output SC1 and a similar signal on output SC2. The SC1 clock output is connected to the common conductors of 16 of the 32 touch switches; the SC2 clock connects to the remaining 16 switches. For each touch switch the clock signal passes through the two series capacitors and is detected in the MOS circuit. When a panel switch surface is touched, the signal level into the chip diminishes, and the on-chip differential amplifier senses the change and performs the appropriate switching function.

I INPUTS

Inputs from the touch switch pads to the TouchControl circuit are labeled I0 through I15 (S9266), or I0 through I6 (S9262). The I inputs in conjunction with SC1 and SC2 outputs form a touch switch matrix of 2 x 16 or 2 x 7, respectively. In both these parts the outputs are binary coded and will be described later.

Interface
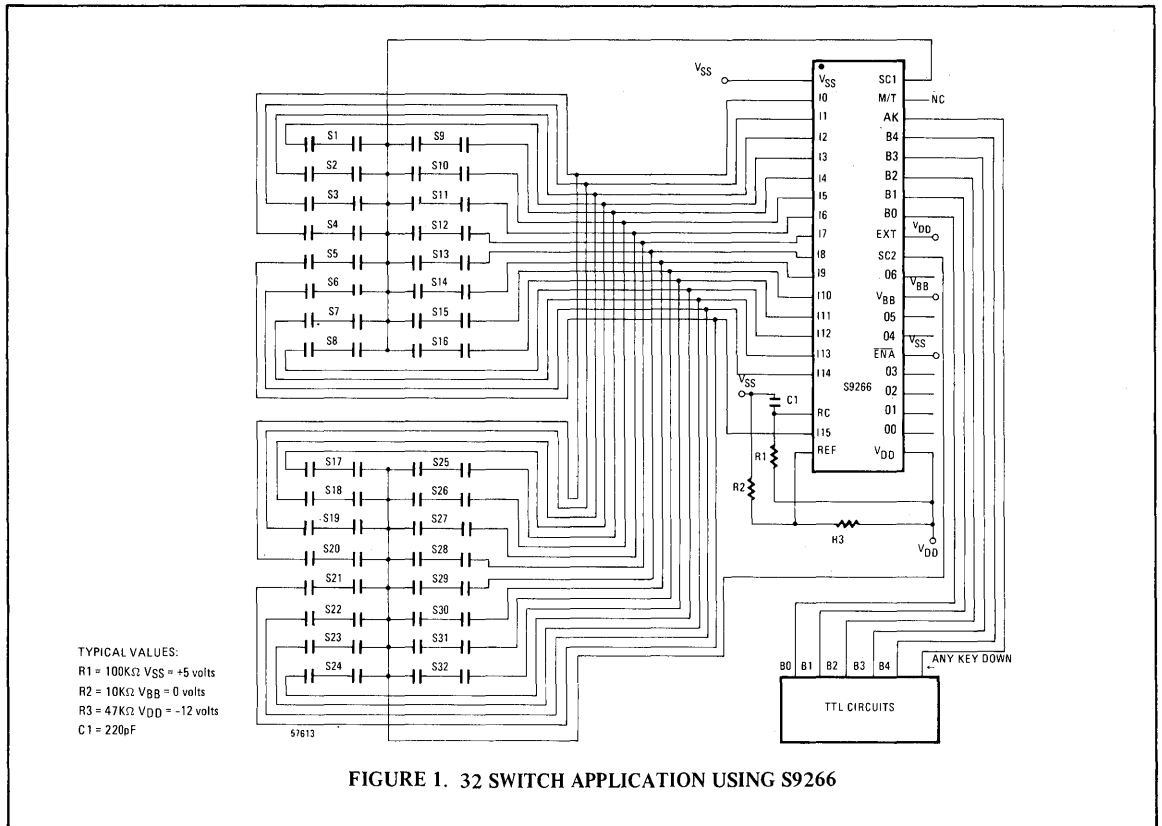
FIGURE 1. 32 SWITCH APPLICATION USING S9266

TYPICAL VALUES:
R1 = 100KΩ V_{SS} = +5 volts
R2 = 10KΩ V_{BB} = 0 volts
R3 = 47KΩ V_{DD} = -12 volts
C1 = 220pF

RC INPUT

A resistor connected to V_{DD} and a capacitor connected to V_{SS} are connected to the RC input pin to establish the on-chip clock frequency that controls the rate of multiplexing and the touch switch delay time. Nominal values for these components are suggested in Figure 1, but they may be varied to change clock frequency over a range of 50kHz to 100 kHz.

REF INPUT

In order to allow flexibility in the choice of TouchControl panel materials, switch layout, and switch size, AMI Touch-Control inputs have been designed to detect a differential change rather than an absolute change in level. To obtain a reference level, two resistors are connected to input REF, one connected to input REF, one connected to V_{SS} and the other to V_{DD}.

V_{BB} SUPPLY

The sources of all output devices (both "O" and "B" outputs) are common and connected to pin V_{BB}. This allows TTL compatibility as shown in Figure 1, as well as the ability to drive higher level signals. For instance, if V_{SS} = 0 volts, V_{DD} = – 16 volts, and $V_{BB} = V_{SS}$, then active outputs would drive a load connected to V_{DD} towards V_{SS}.

M/T INPUT

The M/T input pin selects the mode of switch operation, either momentary or toggle. Applying V_{SS} to the M/T pin selects momentary operation in which appropriate outputs are active only for the duration of touching a switch. In this mode, no output is active when no switch is touched. A V_{DD} level applied to M/T causes the circuit to operate in the toggle mode
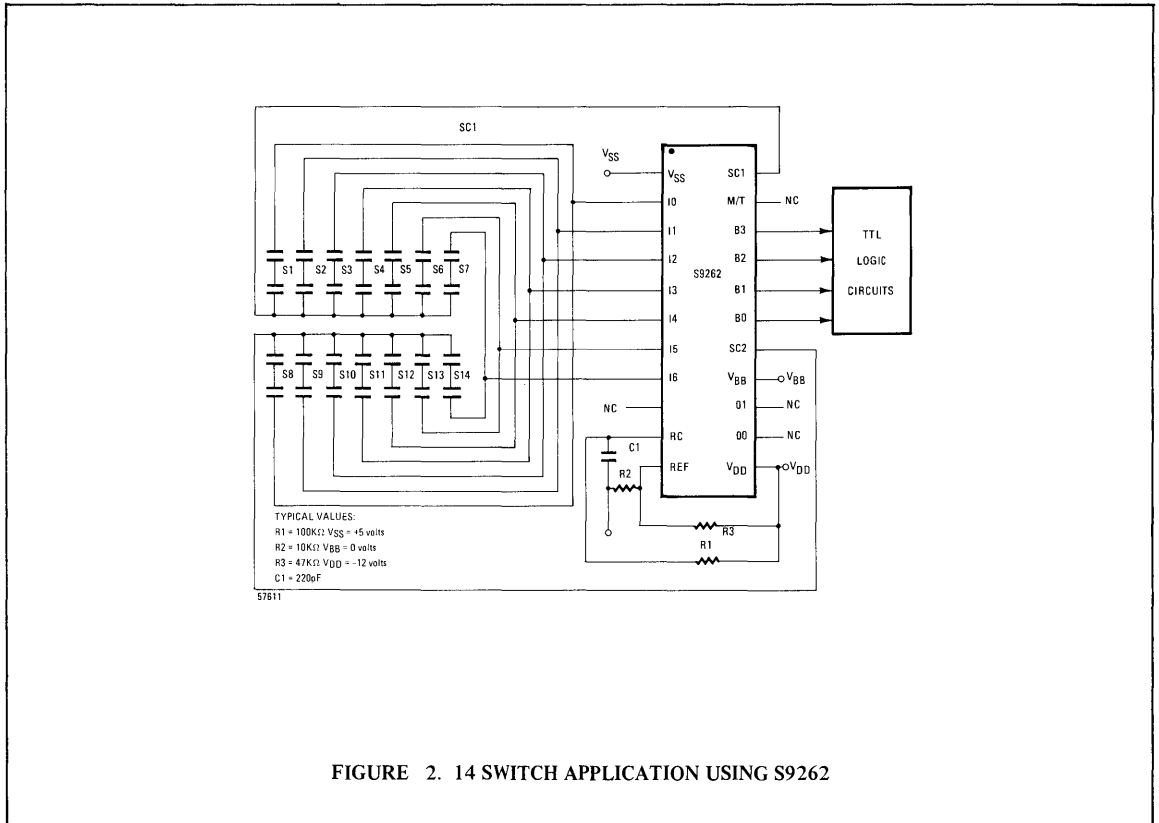
FIGURE 2. 14 SWITCH APPLICATION USING S9262

for "push-on, push-off" operation. Subsequent activation of the switch will toggle the corresponding output on and off alternately. It should be noted that each input should be cleared to the off state before selecting a new input to obtain meaningful data from the binary outputs. To reset all outputs when the toggle mode is selected, a pulse of V_{SS} level may be applied to the M/T input.

SC1 and SC2 OUTPUTS

The S9262 and S9266 have multiplexed inputs, using 2 x 7 and 2 x 16 matrices, respectively, to provide 14 and 32 input states. Clock signals SC1 and SC2 are used along with the "I" inputs to form these matrices as connected in the schematic of Figure 1.

O OUTPUTS

Each output pin labeled "O" corresponds to an input pin labeled "I". Whenever an input is selected, the output becomes active and will drive an external load toward supply voltage V_{BB}. This is true for momentary operation only; toggle operation is described in the section labeled "MT input." When "O" outputs are not active, they are high impedance open drain.

B AND AK OUTPUTS

The S9262 has four and the S9266 has five outputs labeled "B." These supply a binary code relating to the state of the inputs. Fourteen unique states are available on S9262 and thirty-two on S9266. The output configuration is identical to the "O" outputs. An extra output labeled AK is available on the S9266 and is active whenever any key is selected.

Interface

$\overline{ENA}$ INPUT

Available on the S9266, the $\overline{ENA}$ input allows the outputs to be bussed and may be gated off by application of a logic 1 level. V_{SS} applied to the input enables all five outputs and AK.

EXT

The EXT pin is used in the output circuitry and should be connected to V_{DD}.

SCAN OUTPUT	TOUCHED INPUT	B0	B1	B2	B3	O0	O1
		"B" OUTPUTS				"O" OUTPUTS	
SC1	I0	0	0	0	0	1	0
SC1	I1	1	0	0	0	0	1
SC1	I2	0	1	0	0	0	0
SC1	I3	1	1	0	0	0	0
SC1	I4	0	0	1	0	0	0
SC1	I5	1	0	1	0	0	0
SC1	I6	0	1	1	0	0	0
SC2	I0	1	1	1	0	0	0
SC2	I1	0	0	0	1	0	0
SC2	I2	1	0	0	1	0	0
SC2	I3	0	1	0	1	0	0
SC2	I4	1	1	0	1	0	0
SC2	I5	0	0	1	1	0	0
SC2	I6	1	0	1	1	0	0
—	None	1	1	1	1	0	0

TABLE 1. OUTPUT ENCODING (V_{BB} = 0 VOLTS)

SCAN OUTPUT	TOUCHED INPUT	B0	B1	B2	B3	B4	O0	O1	O2	O3	O4	O5	O6	AK OUTPUT
		"B" OUTPUTS					"O" OUTPUTS							
SC1	I0	0	0	0	0	0	1	0	0	0	0	0	0	1
SC1	I1	1	0	0	0	0	0	1	0	0	0	0	0	1
SC1	I2	0	1	0	0	0	0	0	1	0	0	0	0	1
SC1	I3	1	1	0	0	0	0	0	0	1	0	0	0	1
SC1	I4	0	0	1	0	0	0	0	0	0	1	0	0	1
SC1	I5	1	0	1	0	0	0	0	0	0	0	1	0	1
SC1	I6	0	1	1	0	0	0	0	0	0	0	0	1	1
SC1	I7	1	1	1	0	0	0	0	0	0	0	0	0	1
SC1	I8	0	0	0	1	0	0	0	0	0	0	0	0	1
SC1	I9	1	0	0	1	0	0	0	0	0	0	0	0	1
SC1	I10	0	1	0	1	0	0	0	0	0	0	0	0	1
SC1	I11	1	1	0	1	0	0	0	0	0	0	0	0	1
SC1	I12	0	0	1	1	0	0	0	0	0	0	0	0	1
SC1	I13	1	0	1	1	0	0	0	0	0	0	0	0	1
SC1	I14	0	1	1	1	0	0	0	0	0	0	0	0	1
SC1	I15	1	1	1	1	0	0	0	0	0	0	0	0	1
SC2	I0	0	0	0	0	1	0	0	0	0	0	0	0	1
SC2	I1	1	0	0	0	1	0	0	0	0	0	0	0	1
SC2	I2	0	1	0	0	1	0	0	0	0	0	0	0	1
SC2	I3	1	1	0	0	1	0	0	0	0	0	0	0	1
SC2	I4	0	0	1	0	1	0	0	0	0	0	0	0	1
SC2	I5	1	0	1	0	1	0	0	0	0	0	0	0	1
SC2	I6	0	1	1	0	1	0	0	0	0	0	0	0	1
SC2	I7	1	1	1	0	1	0	0	0	0	0	0	0	1
SC2	I8	0	0	0	1	1	0	0	0	0	0	0	0	1
SC2	I9	1	0	0	1	1	0	0	0	0	0	0	0	1
SC2	I10	0	1	0	1	1	0	0	0	0	0	0	0	1
SC2	I11	1	1	0	1	1	0	0	0	0	0	0	0	1
SC2	I12	0	0	1	1	1	0	0	0	0	0	0	0	1
SC2	I13	1	0	1	1	1	0	0	0	0	0	0	0	1
SC2	I14	0	1	1	1	1	0	0	0	0	0	0	0	1
SC2	I15	1	1	1	1	1	0	0	0	0	0	0	0	1
	None	1	1	1	1	1	0	0	0	0	0	0	0	0

TOUCHCONTROL APPLICATION NOTES

PANEL CONSTRUCTION

A TouchControl switch panel consists of a single sheet of a rigid material with conductive surfaces applied on both sides as shown in Figure 3.

A number of materials may be used for touch panels, the selection of the material most suited for a particular application being dependent on such things as durability, appearance, ease of assembly, cost, and dielectric constant of the material.

Regardless of the selected panel material, a touch switch is formed by applying a single conductive surface to its front surface with two other conductive surfaces applied directly in line on the reverse side of the panel. Figure 3 shows three views of a typical touch panel containing two TouchControl switches. On switch one, conductive surface A is applied to the front of the panel and is the surface to be touched to effect a switch closure. Surfaces B and C are applied directly in line with A on the opposite side of the panel. A should cover completely and may overlap surfaces B and C.
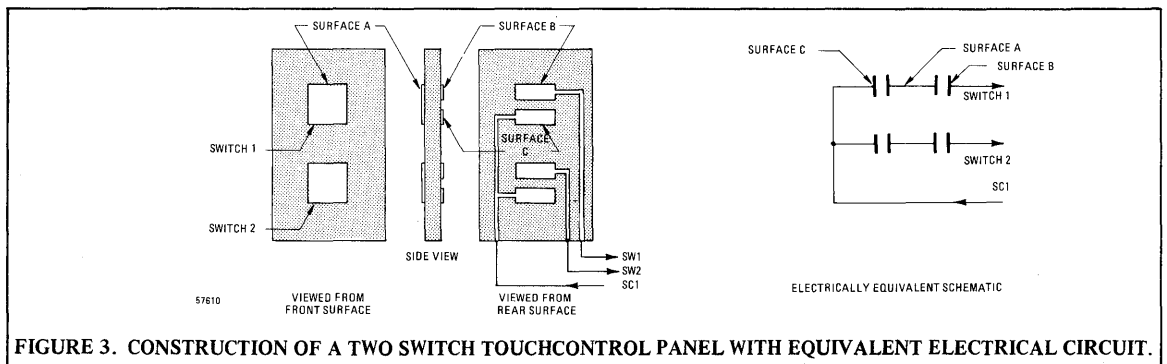

FIGURE 3. CONSTRUCTION OF A TWO SWITCH TOUCHCONTROL PANEL WITH EQUIVALENT ELECTRICAL CIRCUIT.

The application of the conductive surfaces depends on selection of the panel materials. If glass is used, for example, it is common to apply a coating of tin oxide, which is then fired on for durability; rear surface conductors may be screened on with a conductive ink. Touch panels may be made more simply from double-sided printed circuit boards in which the conductive TouchControl surfaces are created by standard etching. For breadboarding purposes, a number of conductive tapes and paints are available and may be applied to a variety of touch panel materials.

ELECTRICAL OPERATION

The three conductive surfaces in a TouchControl switch combine to form two capacitors connected in series, as shown in the schematic diagram of Figure 3. An AC signal generated in the MOS circuit is applied to the rear conductive surface labeled C. This signal is coupled through to surface A by the capacitor formed by C and A. The signal is then coupled to surface B by the capacitor formed by A and B and applied to one of the inputs of the MOS circuit, which detects the signal's presence. When surface A is touched, the amplitude of the signal is significantly decreased because of body capacitance. This is sensed by the MOS circuit, and the appropriate switching function is performed.

TOUCH SWITCH LAYOUT GUIDELINES

AMI TouchControl circuits have been designed to interface with a variety of touch switch configurations. However, there are several guidelines that must be observed to insure a satisfactory TouchControl system.

The size of a TouchControl switch is dependent on the amount of capacitance needed to couple the clock signal to the "I" inputs of the MOS circuits. Because the input capacitance associated with the circuit input is typically five picofarads, it is advisable that each of the two series capacitors formed by the three conductive TouchControl panel surfaces be no less than seven picofarads. Since the capacitance in picofarads can be calculated by $C = 0.22 \in A \div d$, where $\in$ is the dielectric constant, A is area, and d is the material's thickness, it is apparent that minimum switch size is dependent on the thickness and dielectric constant of the panel material. If, for example, the panel is made from 1/8" thick glass with a dielectric constant of 8, then the minimum area of each of the two rear surface conductors is 0.5 sq. inches. Since the touch surface must cover the entire area of the two rear conductors, it must, then, be at least 1.0 sq. inch. It is desirable to separate the two rear-surface conductors by at least 0.125 inches, so the touch surface would be somewhat larger than 1.0 sq. inch. Higher capacitance, and thus smaller touch switches, can be obtained by using epoxy printed circuit material; though the dielectric constant is lower (around 5.0) the thickness can be decreased substantially.

CIRCUIT TO PANEL CONNECTIONS

There are a number of ways to make the necessary connections between TouchControl circuits and panels. A simple approach is to use a printed circuit board for the touch panel. In this case, the connections to the circuit are made by the etched copper pattern. In laying out a printed circuit, it is important to keep the copper traces running to the individual touch pads separated from each other as much as possible. In most instances a minimum spacing of 0.125" between traces is acceptable, though wider spacing might be necessary in cases where traces will run parallel to each other for distances of over six inches. It is also important to keep the clock output (SC1) at least 0.75 inches away from any input trace. These spacing requirements are guidelines to be followed regardless of the touch panel material.

With glass touch panels, a simple method for breadboarding systems is to fasten individual wires onto the conductive surfaces with a conductive epoxy. For production situations, it is possible to locate the electronic circuitry on a separate printed circuit board. Contact to the glass touch panel can be made through spring contacts mounted in the appropriate locations on the circuit board. An alternate approach is to route the traces on the glass to an edge of the glass, making connection through an edge connector, keeping in mind the spacing requirements between traces.

Interface

$\mathbf{AMI}_{\circledR}$

ENCODER/DECODER
REMOTE-CONTROL 2-CHIP SET

Features

☐ **Lower System Costs**
  - **RC oscillator used on encoder (no crystal required)**
  - **Phase-locked-loop on decoder (no crystal required)**
  - **Single binary inputs allow inexpensive switches on pc board jumpers**

☐ **Flexibility of Application**
  - **512 user selectable address codes**
  - **Decoder signal valid output**
  - **Externally selectable one-shot tailors message reception**
  - **User has choice of transmission media: infrared, ultrasonic, RF, or hardware**
  - **Eight ROM programmable preamble codes**
  - **Encoder operates on a single 9V battery**

☐ **Reliable System Operation**
  - **Frequency shift keying scheme means low reception error**
  - **PLL allows frequency variation ± 15% between encoder and decoder**
  - **One-shot period allows adjustment for system noise**
  - **Triple message redundancy required**
  - **Preamble adds to message security**
  - **High noise immunity**

General Description

Encoder/Decoder

This two chip PMOS set includes a user programmable serial data encoder for use in a simple low power transmitter and a serial data decoder for use in a user addressable receiver. The user can select the transmission medium (RF, infrared ultrasonic, or hard wired). The externally selectable message allows up to 512 codes or addresses; this is done with the nine binary inputs on each device. An additional 3 bits of address can be programmed on chip as a fixed preamble.

The serial data encoder encodes by means of a frequency-shift-keyed trinary data pattern composed of 16 data bits. Each data bit will have a length equivalent to 32 cycles of high frequency clock (20kHz typical). Each trinary data pattern will be 512 cycles of 1/2 the oscillator frequency length. The encoder frequency oscillator reference is controlled with an external RC network. The encoder transmitter can be powered by a single 9 volt battery so that a single momentary push button will activate the encoder and transmitter. In the off position there is no current flow.

The serial data decoder in conjunction with a receiver amplifier decodes the transmitted 16 bit coded signal. The on-chip phase-locked-loop locks in on the 20kHz signal even if the transmitted frequency differs from the receiver by up to ± 15%. The coded signal input is

S2743 Serial Data Encoder Block Diagram and Pin Configuration

S2742 Serial Data Decoder Block Diagram and Pin Configuration

compared with the externally selected code. The serial decoder looks at the transmitted signal a minimum of three times before validating a good message. A 3 bit "good" code counter or a 3 bit "bad" code counter accumulates the number of successive good and bad codes being received.

The decoder has an on-chip one-shot which is user programmed by an external RC combination. Whenever three complete good codes are received in the "good" counter a signal enables the one-shot which controls the signal valid output. If a series of three sequential bad codes enter the "bad" code counter the "bad" counter resets the "good" code counter and one-shot period and will not allow an active output until the end of the one-shot period. Any "good" code resets the "bad" code counter. If the "good" counter has accumulated three good codes and activated the output one-shot, any occasional "good" code (occurring within the one-shot period) will maintain the output by retriggering the one-shot. The output appears like a single switch, on when "good" codes are received, off when not, with the minimum total period being determined by twice the one-shot period. The one-shot can be used to prevent the output from switching on and off too rapidly due to system noise. The typical RC components shown in the block diagram give a period of about one half second.

Applications

☐ **Paired Operation**

– **Entry access systems**
– **Identity verification**
– **Remote car starting and location**
– **Telephone dial-in coded access**
– **Remote control of equipment, toys, etc.**

☐ **Multiple Pairs**

– **Intercom systems**
– **Multiple station communication**
– **Traffic control**

☐ **Multiple Encoders**

– **Security systems**
– **Alarm/monitor/intrusion systems**
– **Travel/traffic monitors, rally car identification**
– **Safety beacons/portable alarms**

☐ **Multiple Decoders**

– **Paging systems**
– **Car/people/animal locator systems**
– **Remote control of house appliances**

Figure 1. Serial Data Encoder

Interface
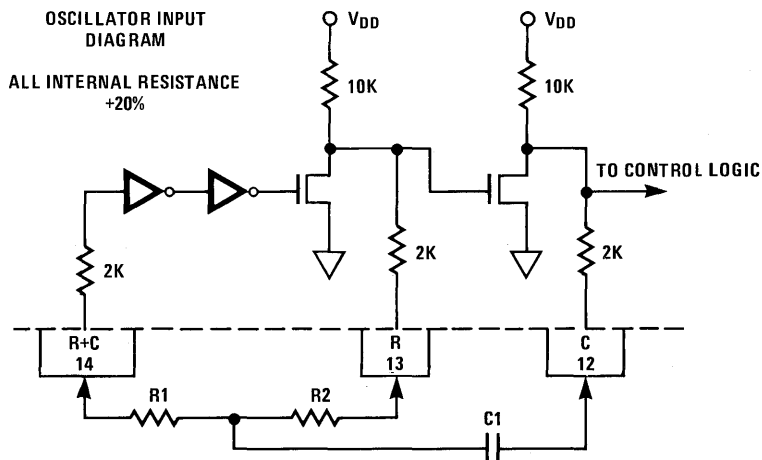
Functional Description

Serial Data Encoder

The AMI serial data encoder is comprised of three sections: Oscillator, Programming Logic, and Control Logic. Specifically it will provide logical ones "1," logical zeroes "0," and synchronization pulses "S" and arrange them into a trinary data pattern composed of 16 data bits. Each data bit will be 32 cycles of the high frequency (HF-1/2 Oscillator Frequency) in length. Each trinary data pattern will be 512 cycles of 1/2 the Oscillator Frequency length.

A logical "1" is represented by 32 cycles of the high frequency.

A logical "0" is represented by 16 cycles of the high frequency followed directly by 8 cycles of the low frequency (LF = 1/2 HF).

A synchronization pulse "S" is represented by 16 cycles of the low frequency.

A 16-bit data pattern will be encoded in the device in such a manner as to have (3) bits programmed internally and (9) bits programmed externally.

The Oscillator Frequency equals twice that of the High Frequency, and the High Frequency equals twice that of the Low Frequency.

The Oscillator circuit will require a maximum of (3) external components (Refer to page 2 Figure 1).

External programming inputs connected to the device $-V_{DD}$ supply will be considered as a logical "1." The bit programming current will not exceed $50\mu a$. The programming resistance should not exceed $1k\Omega$. Unconnected external bit programming inputs will be considered at a logical "0."

A "1" (-5 volts $\leq$ "1" $\leq -V_{DD}$) presented to the "Test" input sets the Internal counter and maintains the output of the device "On." The input impedance of the test input is greater than $5M\Omega$.

For portable operation a 9V transistor battery can be used for the DC voltage supply. Proper circuit polarity must be observed ($-V_{DD}, +V_{SS}$).

External Oscillator Components

The Astable Multivibrator Circuit employed here required three (3) external components.

R_1 aids in keeping the operating frequency independent of variators in supply voltage. R_2 and C_1 form the RC time constant which controls the oscillator frequency. In this case R_1 will be specified at $270k\Omega$ regardless of the oscillator operating frequency. Typically it will be found that $R_1 \geq 2T_2$. R_2 should not be greater than $80k\Omega$; C_1 should not be less than 100pF. A method for determining the approximate value of R_2 and C_1 is:

Start with the approximate formula for oscillator frequency

$$\text{osc. freq} \approx \frac{1}{2\pi RC}$$

It must be noted that the oscillator frequency must be set at twice the desired device high frequency value.

Using a set value of R or C and a known desires oscillator frequencies:

Solve for C   w/osc. freq. = 30kHz $R = 60k\Omega$

$$C\frac{1}{2\pi Rf} \approx \frac{1}{2(60X10^3)(30X10^3)} \approx 2.77 \times 10^{-10} \ 277pFd$$

Solve for R   2/osc. freq. = 30kHz $C = 500pF$

$$R\frac{}{2cf} \approx \frac{1}{2(500X10^{-12})(30X10^3)} \approx 3.33 \times 10^4 \ 33k\Omega$$

Absolute Maximum Ratings

DC Supply Voltage .... $-15V$
Input Voltage.. $V_{SS} + .3V$ to $V_{SS} - 15V$
Operating Temperature Range .... $0°C$ to $+70°C$
Storage Temperature Range .... $-65°C$ to $+150°C$
Lead Temperature (During Soldering) .... $300°C$ for maximum 10 sec

Electrical Characteristics (25°C Air Temperature Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Operating Supply Voltage	-6.65	-9.5	-15	V	V_{DD}
	Operating Power Dissipation		27	40	mW	$-8V$, $-5mA$
	Operating Frequency	2	20	60	kHz	Oscillator
	Frequency Stability					Refer to Page Graphs
	Programming Bits 1-9, Current			50	μA	Programming Input, $R \leq 1k\Omega$
	External Programming Resistance			1	$k\Omega$	Bits 1-9
	(DC) Bit 1-9 Program Logical "1"	-5	-6.05	$-V_{DD}$	V	
	Input Levels Logical "0"		-0.4		V	
	Bit 1-9 Current		55		μA	Input R 9V ≥ 1.5M @ 5V
	Test and $R+C$ Input Impedance	5		75	$M\Omega$	Input Resistance 5MΩ
	(DC) Test Input Levels Test On	-5		$-V_{DD}$	V	Maintains Output Device On
	(See Note 1) Test Off	V_{SS}		-1	V	Permits Normal Operation
	R, C Resistance Logical "1"		12		$k\Omega$	Resistance to V_{DD}, $\pm 20\%$
	Logical "0"		3		$k\Omega$	Resistance to V_{SS}, $\pm 20\%$-30%
	Output Current (See Note 2)	5			mA	Output Voltage $= -.8V$ w/$V_{DD} - 7V$

NOTES:
1) Effect Noted at Pin 15 to V_{SS}
2) Output Voltage Pin 15 to V_{SS}

All Voltages Measured with Respect to V_{SS}

General Description

Serial Data Decoder

The AMI serial data decoder is comprised of four sections: Phase locked loop (PLL), 16-bit digital decoder, Good/Bad code logic and the Retriggerable output one-shot.

The decoder is always on and the phase locked loop is running. A small external capacitor determines the center frequency while an external low pass filter smooths out and generates the VCO control voltage. The typical center frequency of the PLL is 20kHz allowing the received signal to be slightly off frequency and the PLL will still "lock in."

The 16-bit trinary data pattern includes:
 3 "1" bits (fixed) 32 cycles of 20kHz each
 1 Sync bit 16 cycles at 10kHz
 3 Mask programmable bits either "1" or "0"
 9 User selectable bits externally programmed

The PLL locks on the "1" bits present in the data pattern. Once locked the PLL generates a clock which controls the digital decoder section (DDS). The DDS waits for a sync bit and then compares the incoming data pattern bits, one by one, to make sure *all* the bits are correct; fixed ones are ones, mask programmable bits match and finally is the user selectable 9-bit pattern correct.

Bit position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Data Pattern	I	I	M	M	M	U	U	U	U	U	U	U	U	U	I	S

 I = FIXED "1" (32 Cycles at 20kHz)   U = USER SELECTABLE BITS
 M = MASK PROGRAMMABLE BITS   S = SYNC BIT (16 cycles at 10kHz)

$$\text{Time for one Pattern} = 16 \times 32 \times \frac{1}{20\text{kHz}} \approx 25\text{ms}$$

If the pattern was correct a good count (GC) is stored in a "Good Pattern Counter" (GPC). If the pattern match did not occur a bad count (BC) is stored in a "Bad Pattern Counter" (BPC).

1. Any GC resets the BPC.
2. 3 BC's in a row will reset the GPC.
3. When the GPC reaches 4 the one-shot is triggered and an output will occur, i.e., 3 good codes completed.
4. *Any one* GC after an output, occurring within the one-shot time will retrigger the one-shot and maintain the output on.

The retriggerable one-shot stabilizes the systems operations by introducing hysterisis.

1. It takes more good pattern counts to turn the output on than to maintain it on.
2. After the output goes off, it will stay off for the one-shot period regardless of any good patterns being received.

An external RC is used to control the one-shot period.

Absolute Maximum Ratings

DC Supply . . . . −20V
Input Voltage . . . .
Operating Temperature Range . . . . 0°C to +70°C
Storage Temperature Range . . . . −65°C to +150°C
Lead Temperature (During Soldering) . . . . 300°C for maximum 10 sec

Electrical Characteristics (25°C Air Temperature Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
	Operating Supply Voltage	−15V		−20V	V	V_{DD}
	Operating Power Dissipation			200	mW	
	Operating Frequency	2	20	75	kHz	Oscillator
	Operating Current Static			−10	μA	No signal, no bit
	Programming Bits 1-9 Current				μA	Program input, R ≤ 1kΩ
	(DC) Bit 1-9 Program Logical "1"			−20	V	
	Input Levels Logical "0"			0	V	
	Bit 1-9 Current				μA	
	VCO Input Voltage				V	
	VCO Input Current				μA	
	Output Voltage		−1		V	
	Output Current ($V_{OUT} = -1V$)		10		mA	
	Signal Input, AC Coupled	0.025	0.05	1.0	V_{apk-pk}	
	Input Impedance, AC Coupled Amplifier		20		kΩ	
	Phase Output Voltage				μA	
	Phase Output Current				μA	
	R.C. One-Shot Voltage				V	
	R.C. One-Shot Current				μA	

AMI®

Musical Application for an S2000 Microcomputer

Introduction

AMI's S2000 is a complete single-chip computer ideal for a wide range of applications. The S2000 contains an on-chip 1024 byte instruction ROM, a 256 bit scratch-pad RAM, an arithmetic logic unit, and a versatile input/output configuration capable of such tasks as driving displays and interfacing with TouchControl keyboards. Although the circuit is well-suited for use in such end-products as interval timers, appliance timers, and various process controllers, there are other seemingly unrelated applications in which the S2000 also excells. One of these is the generation of musical frequencies and the storage of tunes. This application note describes the capabilities of an S2000 programmed to generate any one of 60 musical frequencies and play on command any one of twelve pre-programmed tunes.

General Description

In typical usage, a mechanical selector switch would be used to tell the processor which song it is to play. Then, when the start switch is touched, the song will be played through to its end. It will then wait for the start switch to be touched again before replaying the song.

The S2000 has the ability to generate five octaves of musical frequencies and can play notes of 16 different lengths. Musical rests [times during which no note is heard] are also obtainable. At any time, four octaves of frequencies are available, making possible the generation of complex waveforms [i.e., sawtooth and pulse].

A typical application of this product would be a musical doorbell capable of playing any one of a number of owner-selected tunes whenever the doorbell switch was touched. Other applications might include electronic games, alarm clocks, and telephones.

TouchControl Start Switch

To begin the playing of any tune, the start switch is touched. Although this switch may be a mechanical button, as found on conventional doorbells, the TouchControl capability of the S2000 allows for this to be a non-moving capacitive touch switch. As soon as this switch is touched, the tune will start playing until it reaches its end, at which time the processor waits for the switch to be touched again.

Number and Length of Tunes Available

In the present configuration, twelve tunes can be played by this S2000. These tunes are programmed into the device during manufacture and can each be selected by switching either of two "A" outputs to one of six "K" and "I" inputs. Whichever of the twelve tunes has been pre-selected by a mechanical switch, that tune will play when the start switch is touched.

The length of the tunes is dependent on several factors. There are 625 words in memory in which to store the notes of the twelve tunes. Since each note requires only a single word of memory, the S2000 is capable of playing up to 625 notes, or an average of 52 notes per tune. Some tunes may be longer than others; for example if one tune is only ten notes long, this leaves 94 notes for another tune.

The exception to the 625 note storage capability comes from the fact that all notes are not of the same duration nor in the same musical octave. Each new note in a tune that is either in a different octave from or is a different length from its preceding note will require four words instead of one. Any note that changes both octave and length requires five words. In the unlikely event that all notes change octave and length, then all notes would require five words each, and a total of 125 notes [10 notes per tune] would be available. In a typical set of tunes, lengths and octaves of notes would most likely not change that often, so it should be possible to obtain 25 notes per song.

In other versions of this application, it would be possible to obtain more tunes by using additional "A" outputs with the "I" inputs. Either 24 or 48 tunes could be stored, however the tunes would have to be proportionately shorter.

Generation of Frequencies

The S2000 is capable of generating all twelve notes of the tempered scale over a five octave range, a total of 60 frequencies. The highest note is C at 1047Hz and the lowest is C sharp at 34.6Hz. The relative tuning accuracy of the frequencies is fixed so that if the RC components used for the S2000 oscillator shift, the notes will still sound in tune with each other. If the S2000 is operating at 1MHz, the frequencies are accurate to ± 0.26%, or about ± 4.3 cents absolute.

Each frequency in a tune is played for a given duration and this is programmable in 16 steps. That is, each note may be programmed to any one of 16 different lengths from length x to length 16x. The actual length of x is dependent on the tempo control, as mentioned below.

Outputs

The eight "D" lines are all used to supply musical outputs. Outputs D0 through D3 provide four octaves of tones, each a squarewave of 50 percent duty factor. The highest octave appears at D0, with the lowest at D3. Although in many applications, only a single output would be listened to, it is possible to add several outputs to create more complex waveforms having higher harmonic content, such as the sawtooth waveform of Figure 3.

The remaining four "D" lines, D4 through D7, are identical to D0 through D3 except that they are 180° out of phase. This allows the S2000 to drive a speaker without the use of an amplifier. The technique is illustrated in Figure 1, where D0 and D4 are used as push-pull outputs connected to an impedance matching transformer to drive an 8 ohm speaker.

Tempo Adjustment

The speed of the tune, or tempo, can be controlled by the frequency of the external oscillator that is fed to the I8 input. If the tempo oscillator frequency is 600Hz, for example, then the shortest notes would be 0.1 second and the longest would be 1.6 seconds. Depending on the programmed note lengths, as mentioned above, with a 600Hz tempo oscillator, the length of the notes can be from 0.1 second to 1.6 seconds in 0.1 second intervals.

If the tempo oscillator frequency is changed, the tempo of the tune changes accordingly, keeping the timing relationships among all notes intact.

General Description of Logic

An overview of the logical operations of this music processor is shown in the flow chart of Appendix A. Because the heart of the logic is the note subroutine, during which the musical frequencies are generated, this is presented as a separate flow diagram in Appendix B. Appendix C lists the entire source program minus all but one of the twelve tunes [only one tune listing is necessary to describe the tune logic].

Referring now to Appendix A, when power is first applied to the unit, the start switch continuously checks for a touched condition [if TouchControl is used] or for a switch depression [for a mechanical switch].

As soon as the switch is touched, the A_0 and A_5 outputs are used to scan the K1, K2, K4, I1, I2, and I4 inputs to determine which of the 12 tunes has been selected. This causes the program counter to jump to the location in ROM that stores the desired tune.

At the beginning of each tune, the octave and duration of the tune's first note are stored from ROM into specific RAM locations. Next, a "note code", relating to the period of the note to be played, is stored in RAM. The note subroutine is then entered, in which the D lines are switched on and off at a rate corresponding to the desired frequency, as determined by the octave and "note code" previously stored in RAM. During each half period of the musical frequency the note subroutine checks information from the I8 timer input and the desired note length [previously stored in RAM] to determine if the end of the note has been reached. If so, the note subroutine returns the program counter to that location in ROM where the next note of the tune is stored. If the tune is over, the program counter returns to "start" and the start switch is scanned continuously until it is touched, causing the tune to be played again.

TouchControl Logic

The S2000 has the capability of interfacing with one or a number of capacitive TouchControl switches. However, only a single start switch is required for this musical application, and this switch may be either TouchControl or mechanical. Although the TouchControl type is discussed here, a mechanical momentary switch with normally closed contacts could be substituted for the two series capacitors of the TouchControl version.

The TouchControl switch consists of two capacitors connected in series between the A4 output [pin 16] and the K8 input [pin 33]. Referring to Figure 1, when the switch is to be interrogated, a pulse is sent out the A4 output to one of the capacitors. Under normal conditions, the pulse is transmitted through the two capacitors to the K8 input. If the pulse appears at the K8 input, then the processor assumes the switch is not touched and does not go on to play a tune, but continues to send pulses from A4 to the switch. Touching the common connection between the two capacitors is the equivalent of loading this junction with a relatively large capacitance to ground. Under this condition, when a pulse is sent from the A4 output, it is attenuated at the K8 input, and the processor assumes the switch is touched and commences to play the tune.

The area to be touched to start the tune is the junction between the two capacitors. These capacitors may be either discrete components or they may be formed by conductive areas on a rigid dielectric material. Reference may be made to AMI's Application Note, "TouchControl Circuits for Capacitance Switching," for a discussion on the construction of these switches. For conditions where stray capacitance loading is minimal, 25pF capacitors should be sufficient to operate the TouchControl system. The resistors in series with K8 and A4 and the two diodes on A4 are included for added protection against damage caused by static discharge.

Ap Notes

Referring to Appendix C, the source coded for the TouchControl begins at the label "Start", location 5. Instructions in locations 5, 6, 7, and B force A4 to a logic 0 level. [Locations 8, 9, and A are used for an AK output and are not a part of TouchControl.] Location E removes the internal discharge device from the K8 input, and C, D, F, and 10 drive the A4 line high. Location 12 tests the K8 input, which, if high, will cause the program to jump back to "Start". If the K8 input is low, indicating a touched switch, the SZK instruction at location 12 causes a jump to location 14, where A4 is reset to a low level, and the scanning of the K1, K2, K4, I1, I2, and I4 inputs begins to determine which tune is to be played.

Selector Switch Scanning Logic

Tune selection is accomplished by the two mechanical switches of Figure 1. For each position of switch 1 there are six tunes that can be selected by switch 2. The source code controlling this selection process begins at label "Play", location 15, and ends at location 35. During the first scan of K1, K2, K4, I1, I2, and I4, the A0 output is high. If no K or I input is found to be at a logic 1, the A5 output is set high and a second scan of the K1 through I4 inputs begins. Flag 1 is set for the first scan and reset for the second scan; this flag is used later to cause the program counter to jump to either the first or second set of six tunes in the tune memory.

Tune Memory

The twelve tunes are stored in ROM from locations E4 through 3BF. In Appendix C, only the first tune [label TUN1] is shown, a typical example of how tunes would be coded.

Suppose the scanning logic has caused the program counter to jump to "TUN1". At location E4, flag 1 is tested to determine if the jump was taken during the first or second scan of K1 through I4. If the jump was taken in the second scan, this means the selector switch SW1 was in the A5 position, flag 1 is reset, and the program counter would jump to "TUN7". If SW1 was in the A0 position, flag 1 will be set, the jump to "TUN7" will not be taken, and tune 1 will play. Assuming tune 1 is selected, locations E7 through EB store the octave and length of the first note in designated RAM locations.

The octave code and length code information is shown at the start of the source listing in Appendix C. The first "note" in the tune is a reset, or a time during which no note is heard. This is done to synchronize the start of the tune with information from the I8 input and "sec FF", which determine the tempo [speed] of the tune. The "Rest" subroutine has the same effect as any of the C, D, etc. subroutines, except that during a rest "note", no D output states are changed. This causes no note, or frequency, to be heard during a rest.

The first actual note to be played in TUN1 is a C in octave 2 [octave code 1], the second highest octave of musical frequencies. Its length code is 13, resulting in a length of 0.18 seconds when a frequency of 1KHz is applied to the I8 input. Subroutine "C" is located on page 15 of the ROM, as are all twelve note letter subroutines, and the subroutines, "Rest" and "Note". This was done to allow for the smallest possible tune memory. [If the note subroutines were not located on page 15, a "PP" instruction would have to appear before each note in the tune memory, almost doubling the required memory length.]

The "C" subroutine begins with a jump statement to location "FC", because all note letter subroutines [FC, FCS, FD, etc.] would not fit on page 15. Likewise, all other note letter subroutines start with a jump statement to "F__". The "C" subroutine loads a unique note code, comprising 3 words into three RAM locations. This note code, when used in a timer in the note subroutine causes the output frequencies to be C frequencies. After loading these codes into RAM, a jump is made to the "Note" subroutine, during which a C note in octave 2 is generated for the duration of the first note. On return from the note subroutine, the program counter is returned to the tune memory to look for the next note in the tune.

Still following tune 1, after the first note, "C", has been played, the instructions in locations EE, EF, F0 cause the octave to change from octave 2 [octave code 1] to octave 1 [octave code 0], or the highest octave. The next note to be played is an F, followed by an A, C, Rest, and A. These four notes and Rest are all of the same length and octave. Then, for the note following A, the length is changed by location F6, F7, and F8 to a length code 7, or 0.54 seconds. The next note, which is the last note in the tune, is a C in the top octave and 0.54 seconds long. After the last note, the program counter returns to "Start" and scans the TouchControl switch to determine if the tune is to be played again.

Note Subroutine

The heart of this musical processor is the "Note" subroutine, whose job it is to generate the musical frequencies. Before entering the note subroutine, a three word note code must have been loaded into designated RAM locations along with the octave code and length code to determine the frequency and length of the note to be played. A detailed explanation of this subroutine would be lengthy and is omitted here in favor of a description of some of its key operations. The logic is presented in the flow-diagram in appendix B with source code in appendix C.

Each half-period of the musical frequency to be generated is divided into two parts, a fixed and a variable part. The fixed part is 100 machine cycles long and it is this part that performs such tasks as determining if the length of the note has been reached, up-

dating the output status, and handling the octave information stored in RAM. The variable part of the note subroutine is called the note period timer that is loaded with the three byte note code to time the length of the half period of the note.

The note period timer occupies ROM locations 3EE through 3FB, and its length, in machine cycles, is equal to $9 + 3 \times [15\text{-code 1}] + 4 \times [15\text{-code 2}] + 5 \times [15\text{-code 3}]$. The highest frequency, C, has a note code of 15, 15, 13, resulting in a total of 19 machine cycles for the note period timer for a C note. Adding this to the 100 cycle fixed timer, there are 119 machine cycles in one half period of a C note or 238 cycles per period. For an operating frequency of 1MHz, the resulting $4\mu s$ per machine cycle yields a C period of $952\mu s$, a frequency of 1050Hz. The same analysis for the A note with its note code of 12, 14, 11 gives an A period of 284 machine cycles or $1136\mu s$, a frequency of 800Hz. The note codes used here result in relative accuracies of $\pm 0.26\%$, which are easily acceptable for single note instruments.

Octave information is handled by the E register. At the label, "Load", the octave code is loaded from RAM into register E, which is examined after each run of the note period timer. If E were always equal to 0, the program counter would always jump from the end of the note period timer to the label "CHGO" to change status of the outputs. If the octave code stored in RAM is 0, E will always be 0. If the octave code were 1 instead of 0 then, after the first run of the note period timer, E would equal 1; E would then be decremented, the 89 cycle "filler timer" is run, and the note period timer would be run again. E would now be 0, so the program jumps to "CHGO" to effect the end of a half period. This latter example results in an output of half the frequency. Thus, the lower the octave code, the higher the resulting output frequency.

Mention was made above to an 89 cycle filler timer. These filler timers are used in various lengths throughout the "Note" subroutine to keep the fixed portion of the half period equal to 100 machine cycles for all possible paths in the flow diagram.

The output status of D0 and D4 must be changed every half period of the generated frequency, since they both provide the highest octave output. D1 through D5 states change every other half period, and so on through D3 and D7 which change once every eight half periods. This is easily accomplished by adding one to the output status register in RAM at every half period of the note generated. To obtain the four D0, D1, D2 and D3 outputs 180° out of phase with the four D4, D5, D6, and D7 outputs, the output status register is loaded into the accumulator, complimented and a DISB instruction then updates all eight D outputs as desired.

The length of a note is dependent on both the length code stored in RAM and the frequency applied to I8, which is internally divided by 60 to operate the

seconds flip flop. Each time after the output status of the D lines is changed, the SOS instruction tests the seconds flip flop. If it is a 1, the length counter is incremented and, if it is greater than 15, the note is over. A higher length code results in a shorter note length, as indicated in the table at the beginning of appendix C.

When the note is over, a fixed "space timer" is run to put a gap between adjacent notes. The "Note" subroutine then returns the program counter back to the note letter subroutine and, ultimately, back to the next location in the tune memory.

Options for Outputs

The musical frequencies generated by this S2000 are available at four different octaves on D0 through D3. In addition, the same frequencies are available on D4 through D7 but 180° out of phase. These eight outputs by themselves or in combination with one of the two AK outputs allow for a variety of sounds to be generated.

The out-phased outputs allow for driving a speaker through an impedance matching transformer without the use of any power amplifier. Although the circuit in Figure 1 shows D0 and D4 connected as a push-pull output driving a speaker, lower frequency tones could be derived by driving with D1 and D5, D2 and D6 or D3 and D7.

Figure 3 shows three of the D outputs mixed to form a stair-stepped [or sawtooth] waveform. This provides more harmonics to be used more effectively with filter circuits for obtaining the sounds of brass instruments, strings, and other complex voices.

The two AK signals, outputs A2 and A3, are provided for creating percussive sounds, such as plucked strings, pianos, and bells. These signals are turned on at the beginning of a note, and off at the note's end to be used in the generation of an envelope to key on and decay gradually the audio signal. Figure 2 shows a simple percussive circuit that uses a single transistor driven by the AK signal of A3 to charge a capacitor that creates a keying envelope causing the amplitude of the audio signal to decay. The A2 signal is identical to A3 but opposite in polarity.

Summary

This application note describes a fairly specific product. As a doorbell, music box, telephone "tune" ringer, or other musical memory, this product may fit the application as is, or with some modifications. However, the broader intent has been to describe how an S2000 could be used to create music and to suggest a variety of applications in which the S2000 can be used musically to create many types of imaginative end products.
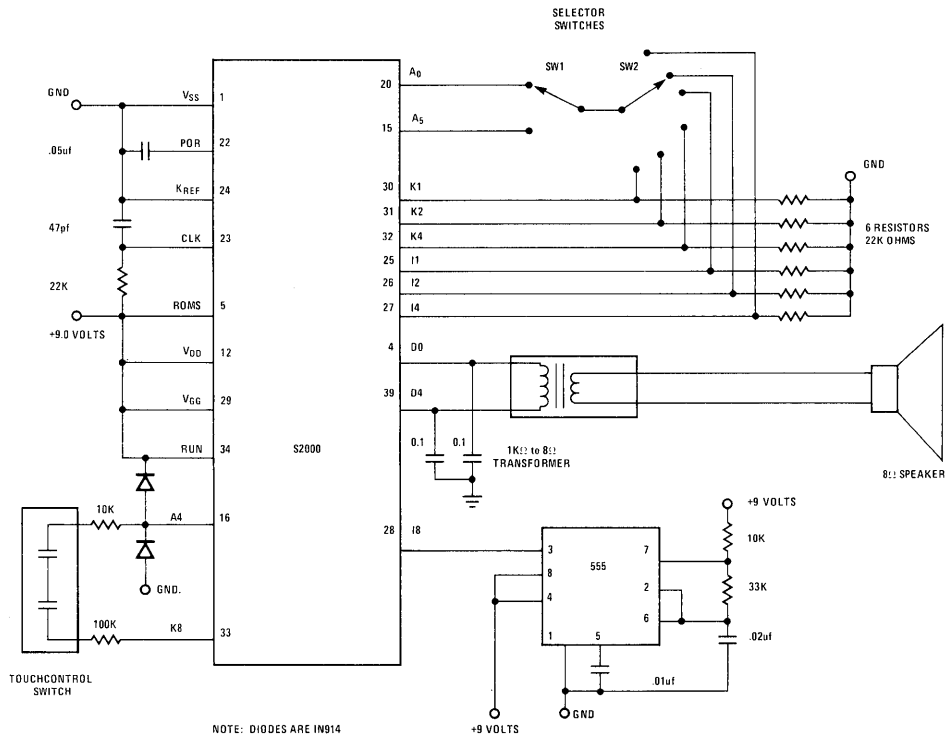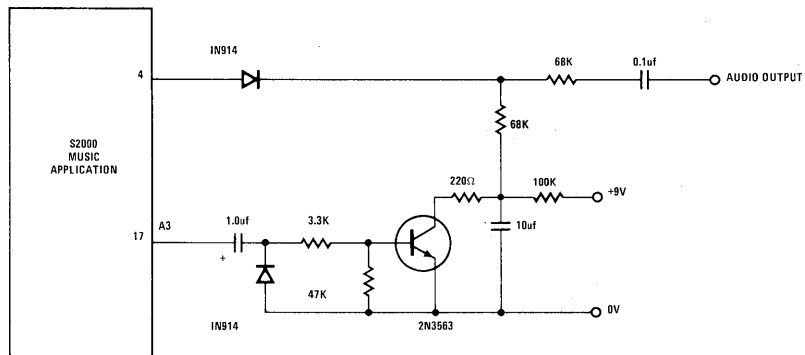
Ap Notes

Figure 1. Schematic of Typical Application

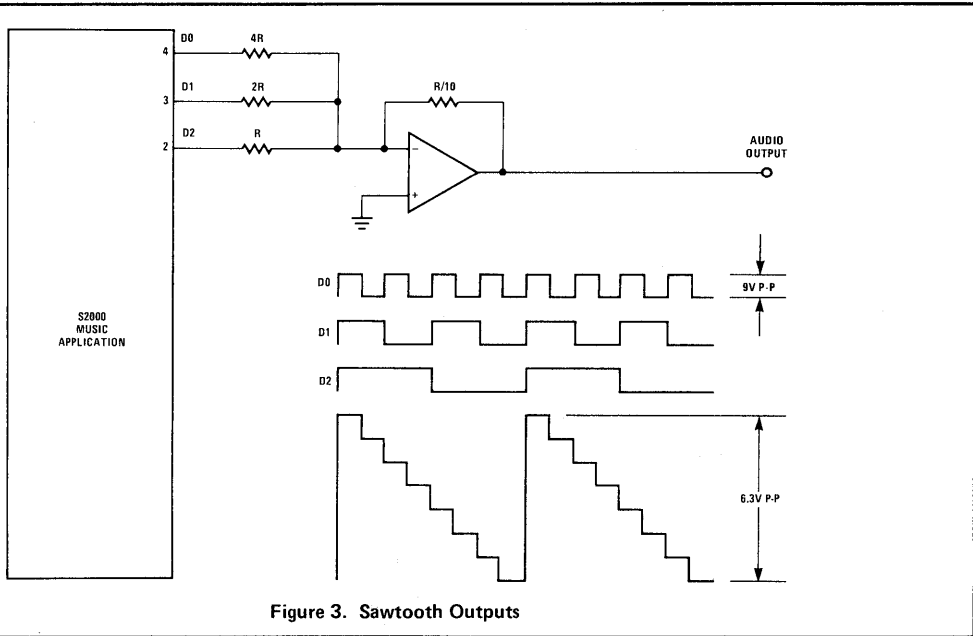Figure 2. Schematic Program of Percussive Output
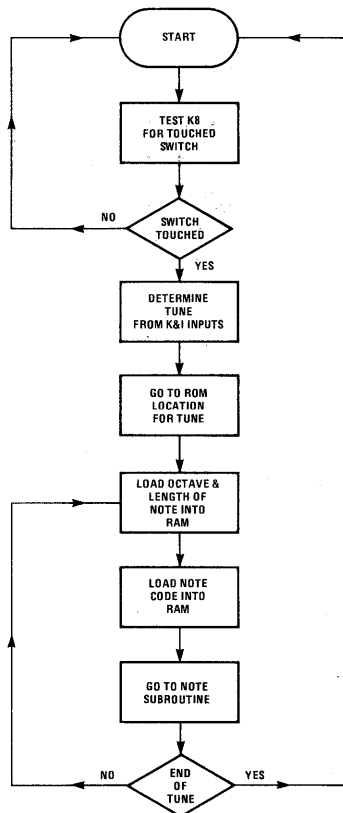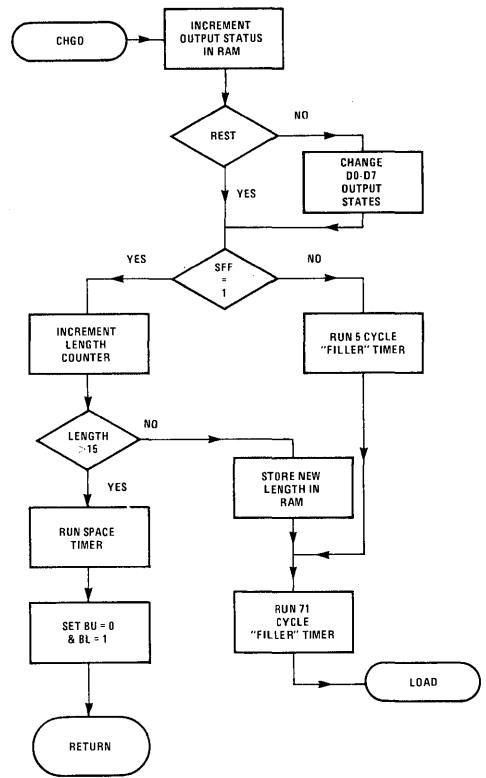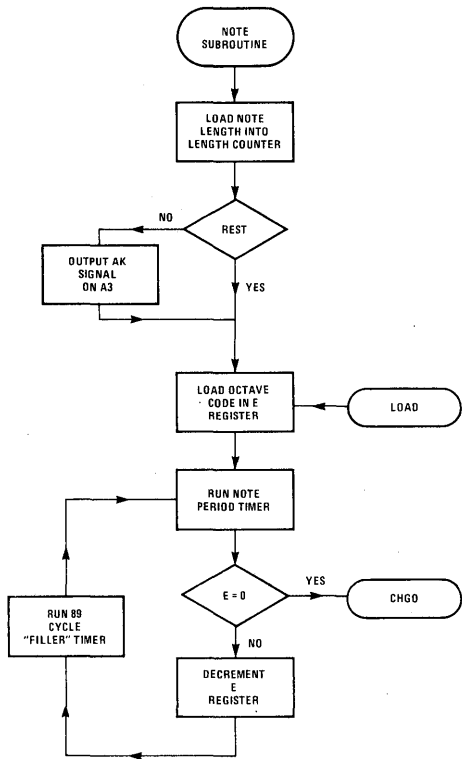
Figure 3. Sawtooth Outputs

Appendix A. System Flow Diagram

Appendix B. Note Subroutine Flow Diagram

STMT LOC OBJ SOURCE

```
0001                    TITLE   DOORBELL
0002     *THIS PROGRAM PLAYS TWELVE TUNES OF VARIOUS LENGTHS.TUNES MAY OCCUPY
0003     *MEMORY LOCATIONS FROM 00E7 THROUGH 0B3F.AT THE BEGINNING OF EACH
0004     *TUNE,THE LENGTH AND OCTAVE OF EACH NOTE SHOULD BE ENTERED,
0005     *FOLLOWED BY ONE "JMS REST" STATEMENT.NOTES MAY THEN FOLLOW
0006     *EACH OTHER IN SEQUENCE,ONE "JMS (NOTE LETTER)"AFTER ANOTHER,
0007     *UNLESS A NOTE CHANGES LENGTH OR OCTAVE FROM THE PREVIOUS NOTE.
0008     *THIS CHANGE MUST BE ENTERED BEFORE EACH NOTE THAT CHANGES
0009     *LENGTH OR OCTAVE.
0010     *TO CHANGE LENGTH:    TO CHANGE OCTAVE:   TO CHANGE LEN.&OCT.:
0011     *   LBZ 1                LBZ 0                LBZ 0
0012     *   LAI (LENGTH CODE)    LAI (OCTAVE CODE)    LAI (OCTAVE CODE)
0013     *   XCI 1                XCI 0                XC 0
0014     *                                            LAI (LENGTH CODE)
0015     *                                            XCI 1
0016     * OCTAVE:          OCTAVE CODE:
0017     *   1(554 TO 1046HZ) 0
0018     *   2                1
0019     *   3                3
0020     *   4                7
0021     *   5(35 TO 65 HZ)  15
0022     *
0023     * WITH A TEMPO OSCILLATOR FREQUENCY OF 1000 HZ.:
0024     * DURATION OF NOTE(SEC.):  #TIME CYCLES:    LENGTH CODE:
0025     *       0.96              16                0
0026     *       0.90              15                1
0027     *       0.84              14                2
0028     *       0.78              13                3
0029     *       0.72              12                4
0030     *       0.66              11                5
0031     *       0.60              10                6
0032     *       0.54               9                7
0033     *       0.48               8                8
0034     *       0.42               7                9
0035     *       0.36               6                10
0036     *       0.30               5                11
0037     *       0.24               4                12
0038     *       0.18               3                13
0039     *       0.12               2                14
0040     *       0.06               1                15
0041 0000              ORG     0
0042 0000 6F           PP      0
0043 0001 6F           PP      0
0044 0002 7D           LAI     13
0045 0003 13           XAB
0046 0004 05           PSL
0047 0005 7F  START    LAI     15              ;BEGIN TOUCH CYCLE
0048 0006 13           XAB
0049 0007 05           PSL
0050 0008 72           LAI     2
0051 0009 13           XAB
0052 000A 04           PSH
0053 000B 19           MVS
0054 000C 74           LAI     4
0055 000D 13           XAB
0056 000E 78           LAI     8
0057 000F 04           PSH
0058 0010 19           MVS
0059 0011 05           PSL
```

Ap Notes

STMT LOC OBJ SOURCE

```
0060 0012 2B          SZK
0061 0013 C5          JMP     START
0062 0014 19          MVS
0063 0015 40 PLAY     LBZ     0
0064 0016 2B          SF1                     ;SET TUNE FLAG
0065 0017 04 SCAN     PSH
0066 0018 19          MVS                     ;TURN ON A0 OR A5
0067 0019 71          LAI     1
0068 001A 28          SZK                     ;TEST TUN1
0069 001B 6C          PP      TUN1/64
0070 001C E4          JMP     TUN1            ;PLAY TUN1
0071 001D 29          SZI                     ;TEST   TUN4
0072 001E 69          PP      TUN4/64
0073 001F D4          JMP     TUN4
0074 0020 72          LAI     2
0075 0021 28          SZK                     ;TEST TUN2
0076 0022 6C          PP      TUN2/64
0077 0023 FC          JMP     TUN2
0078 0024 29          SZI                     ;TEST TUN5
0079 0025 68          PP      TUN5/64
0080 0026 D2          JMP     TUN5
0081 0027 74          LAI     4
0082 0028 28          SZK                     ;TEST TUN3
0083 0029 6B          PP      TUN3/64
0084 002A DD          JMP     TUN3
0085 002B 29          SZI                     ;TEST TUN6
0086 002C 67          PP      TUN6/64
0087 002D E9          JMP     TUN6
0088 002E 2E          TF1                     ;TEST TUNE FLAG
0089 002F C5          JMP     START
0090 0030 05          PSL                     ;TURN OFF A0
0091 0031 19          MVS
0092 0032 75          LAI     5               ;TURN ON A5
0093 0033 13          XAB
0094 0034 2A          RF1
0095 0035 D7          JMP     SCAN
0096 0036 7F FC       LAI     15              ;LOAD 15 INTO BU=0;BL=1
0097 0037 3A          XC      1
0098 0038 7F          LAI     15              ;LOAD 15 INTO BU=1;BL=1
0099 0039 38          XC      3
0100 003A 7D          LAI     13              ;LOAD 13 INTO BU=2,BL=1
0101 003B 39          XC      2               ;BU=0;BL=1
0102 003C 9C          JMS     NOTE            ;PLAY NOTE
0103 003D 02          RT
0104 003E 7E FB       LAI     14
0105 003F 3A          XC      1
0106 0040 7E          LAI     14
0107 0041 38          XC      3
0108 0042 7D          LAI     13
0109 0043 39          XC      2
0110 0044 9C          JMS     NOTE
0111 0045 02          RT
0112 0046 7D FA5      LAI     13
0113 0047 3A          XC      1
0114 0048 7E          LAI     14
0115 0049 38          XC      3
0116 004A 7C          LAI     12
0117 004B 39          XC      2
0118 004C 9C          JMS     NOTE
```

STMT LOC OBJ SOURCE

```
0119 004D 02          RT
0120 004E 7C FA        LAI     12
0121 004F 3A          XC      1
0122 0050 7E          LAI     14
0123 0051 38          XC      3
0124 0052 7B          LAI     11
0125 0053 39          XC      2
0126 0054 9C          JMS     NOTE
0127 0055 02          RT
0128 0056 7B FGS       LAI     11
0129 0057 3A          XC      1
0130 0058 7E          LAI     14
0131 0059 38          XC      3
0132 005A 7A          LAI     10
0133 005B 39          XC      2
0134 005C 9C          JMS     NOTE
0135 005D 02          RT
0136 005E 78 FG        LAI     8
0137 005F 3A          XC      1
0138 0060 7E          LAI     14
0139 0061 38          XC      3
0140 0062 7A          LAI     10
0141 0063 39          XC      2
0142 0064 9C          JMS     NOTE
0143 0065 02          RT
0144 0066 75 FFS       LAI     5
0145 0067 3A          XC      1
0146 0068 7E          LAI     14
0147 0069 38          XC      3
0148 006A 7A          LAI     10
0149 006B 39          XC      2
0150 006C 9C          JMS     NOTE
0151 006D 02          RT
0152 006E 75 FF        LAI     5
0153 006F 3A          XC      1
0154 0070 7E          LAI     14
0155 0071 38          XC      3
0156 0072 78          LAI     8
0157 0073 39          XC      2
0158 0074 9C          JMS     NOTE
0159 0075 02          RT
0160 0076 74 FE        LAI     4
0161 0077 3A          XC      1
0162 0078 7C          LAI     12
0163 0079 38          XC      3
0164 007A 78          LAI     8
0165 007B 39          XC      2
0166 007C 9C          JMS     NOTE
0167 007D 02          RT
0168 007E 73 FDS       LAI     3
0169 007F 3A          XC      1
0170 0080 7A          LAI     10
0171 0081 38          XC      3
0172 0082 78          LAI     8
0173 0083 39          XC      2
0174 0084 9C          JMS     NOTE
0175 0085 02          RT
0176 0086 73 FD        LAI     3
0177 0087 3A          XC      1
```

STMT LOC OBJ SOURCE

```
0178 0088 77         LAI    7
0179 0089 38         XC     3
0180 008A 78         LAI    8
0181 008B 39         XC     2
0182 008C 9C         JMS    NOTE
0183 008D 02         RT
0184 008E 70 FCS     LAI    0
0185 008F 3A         XC     1
0186 0090 76         LAI    6
0187 0091 38         XC     3
0188 0092 78         LAI    8
0189 0093 39         XC     2
0190 0094 9C         JMS    NOTE
0191 0095 02         RT
0192 03C0            ORG    $3C0
0193 03C0 2D REST    SF2
0194 03C1 9C         JMS    NOTE
0195 03C2 2C         RF2
0196 03C3 02         RT
0197 03C4 6F C       PP     FC/64
0198 03C5 F6         JMP    FC
0199 03C6 6D CS      PP     FCS/64
0200 03C7 CE         JMP    FCS
0201 03C8 6D D       PP     FD/64
0202 03C9 C6         JMP    FD
0203 03CA 6E DS      PP     FDS/64
0204 03CB FE         JMP    FDS
0205 03CC 6E E       PP     FE/64
0206 03CD F6         JMP    FE
0207 03CE 6E F       PP     FF/64
0208 03CF EE         JMP    FF
0209 03D0 6E FS      PP     FFS/64
0210 03D1 E6         JMP    FFS
0211 03D2 6E G       PP     FG/64
0212 03D3 DE         JMP    FG
0213 03D4 6E GS      PP     FGS/64
0214 03D5 D6         JMP    FGS
0215 03D6 6E A       PP     FA/64
0216 03D7 CE         JMP    FA
0217 03D8 6E AS      PP     FAS/64
0218 03D9 C6         JMP    FAS
0219 03DA 6F B       PP     FB/64
0220 03DB FE         JMP    FB
0221 03DC 72 NOTE    LAI    2                    ;
0222 03DD 13         XAB
0223 03DE 05         PSL
0224 03DF 41         LBZ    1
0225 03E0 3D         LAM    2          ;LOAD LENGTH OF NOTE IN ACC
0226 03E1 3B         XC     0          ;STORE LENGTH IN INC LENGTH
0227 03E2 73         LAI    3
0228 03E3 13         XAB
0229 03E4 04         PSH               ;PRESET A3 HIGH
0230 03E5 2F         TF2               ;DONT OUTPUT "ANY KEY"IF NOTE IS A REST
0231 03E6 19         MVS               ;OUTPUT AK SIGNALS ON A2 AND A3
0232 03E7 40 LOAD    LBZ    0
0233 03E8 3F         LAM    0
0234 03E9 0D         XAE               ;STORE OCTAVE INFO IN E
0235 03EA 40 TIME    LBZ    0
0236 03EB 71         LAI    1
```

STMT LOC OBJ SOURCE

```
0237 03EC 13           XAB
0238 03ED 3E           LAM      1              ;BEGIN TIMER LOOP STARTING AT LOOP1
0239 03EE 51 LOOP1     ADIS     1              ;TIME=9+3(15-CODE1)+4(15-CODE2)+5(15-CODE3)
0240 03EF F1           JMP      OUT1
0241 03F0 EE           JMP      LOOP1
0242 03F1 3C OUT1      LAM      3
0243 03F2 51 LOOP2     ADIS     1
0244 03F3 F6           JMP      OUT2
0245 03F4 60           PP       LOOP2/64
0246 03F5 F2           JMP      LOOP2
0247 03F6 3D OUT2      LAM      2
0248 03F7 51 LOOP3     ADIS     1
0249 03F8 6D           PP       OCTAV/64
0250 03F9 D6           JMP      OCTAV
0251 03FA 00           NOP
0252 03FB F7           JMP      LOOP3
0253 0096              ORG      $96
0254 0096 40 OCTAV     LBZ      0
0255 0097 08           SBE                     ;SKIP IF E=0
0256 0098 DA           JMP      DECE
0257 0099 E6           JMP      CHGO
0258 009A 0D DECE      XAE                     ;LOAD OCTAVE INFO IN ACC
0259 009B 5F           ADIS     15             ;DECREMENT ACC
0260 009C 00           NOP
0261 009D 0D           XAE                     ;LOAD OCTAVE INFO BACK IN E
0262 009E 71 FILL1     LAI      1              ;BEGIN 89 CYCLE TIMER
0263 009F 00           NOP
0264 00A0 51 FILL2     ADIS     1
0265 00A1 60           PP       TIME/64
0266 00A2 EA           JMP      TIME           ;TIMER OVER
0267 00A3 00           NOP
0268 00A4 00           NOP
0269 00A5 E0           JMP      FILL2
0270 00A6 42 CHGO      LBZ      2              ;SET RAM ADDRESS TO OUTPUT STATUS
0271 00A7 3B           XC       0
0272 00A8 51           ADIS     1              ;INCREMENT OUTPUT INFORMATION
0273 00A9 00           NOP
0274 00AA 3B           XC       0
0275 00AB 3F           LAM      0
0276 00AC 10           CMA
0277 00AD 2F           TF2                     ;DONT CHANGE OUTPUTS IF REST ON
0278 00AE 18           DISB
0279 00AF 07           SOS
0280 00B0 F9           JMP      FILL3          ;DONT INCREMENT INC LENGTH IF SEC NOT 1
0281 00B1 43           LBZ      3
0282 00B2 3B           XC       0
0283 00B3 51           ADIS     1
0284 00B4 6C           PP       ENNOT/64
0285 00B5 C8           JMP      ENNOT          ;END NOTE IF OVER
0286 00B6 3B           XC       0
0287 00B7 6D           PP       FILL4/64
0288 00B8 FE           JMP      FILL4
0289 00B9 00 FILL3     NOP
0290 00BA 00           NOP
0291 00BB 00           NOP
0292 00BC 00           NOP
0293 00BD 00           NOP
0294 00BE 74 FILL4     LAI      4              ;BEGIN 71 CYCLE TIMER
0295 00BF 00           NOP
```

STMT LOC OBJ SOURCE

```
0296 00C0 51 FILL5    ADIS   1
0297 00C1 6C          PP     ENFL/64
0298 00C2 C6          JMP    ENFL
0299 00C3 00          NOP
0300 00C4 6C          PP     FILL5/64
0301 00C5 C0          JMP    FILL5
0302 00C6 60 ENFL     PP     LOAD/64
0303 00C7 E7          JMP    LOAD
0304 00C8 73 ENNOT    LAI    3              $SET A3 LOW
0305 00C9 13          XAB
0306 00CA 05          PSL
0307 00CB 72          LAI    2
0308 00CC 13          XAB
0309 00CD 04          PSH                   $SET A2 HIGH
0310 00CE 19          MVS
0311 00CF 70          LAI    0              $BEGIN SPACE TIMER
0312 00D0 0D          XAE
0313 00D1 40          LBZ    0
0314 00D2 70 SPACE    LAI    0
0315 00D3 51 SP1      ADIS   1
0316 00D4 D6          JMP    SP2
0317 00D5 D3          JMP    SP1
0318 00D6 0D SP2      XAE
0319 00D7 51          ADIS   1
0320 00D8 DB          JMP    SP3
0321 00D9 0D          XAE
0322 00DA D2          JMP    SPACE
0323 00DB 13 SP3      XAB
0324 00DC 51          ADIS   1
0325 00DD E0          JMP    SPOUT
0326 00DE 13          XAB
0327 00DF D2          JMP    SPACE
0328 00E0 40 SPOUT    LBZ    0
0329 00E1 3B          XC     0
0330 00E2 33          XCI    0
0331 00E3 02          RT
0332 00E4 2E TUN1     TF1                   $TEST FOR SCAN NUMBER
0333 00E5 66          PP     TUN7/64
0334 00E6 CD          JMP    TUN7
0335 00E7 40          LBZ    0              $CHARGE
0336 00E8 71          LAI    1
0337 00E9 3A          XC     1              $LOAD OCTAVE INFO IN RAM
0338 00EA 7D          LAI    13
0339 00EB 32          XCI    1              $LOAD LENGTH INFO IN RAM
0340 00EC 80          JMS    REST
0341 00ED 84          JMS    C              $PLAY NOTE C
0342 00EE 40          LBZ    0
0343 00EF 70          LAI    0              $CHANGE OCTAVE
0344 00F0 33          XCI    0
0345 00F1 8E          JMS    F
0346 00F2 96          JMS    A
0347 00F3 84          JMS    C
0348 00F4 80          JMS    REST
0349 00F5 96          JMS    A
0350 00F6 41          LBZ    1
0351 00F7 77          LAI    7
0352 00F8 32          XCI    1              $CHANGE NOTE LENGTH
0353 00F9 84          JMS    C
0354 00FA 6F          PP     START/64
```

STMT LOC OBJ SOURCE

```
0355 00FB C5           JMP    START
0356 00FC 2E TUN2      TF1                        ;JINGLE BELLS
0357 00FD 66           PP     TUN8/64
0358 00FE E9           JMP    TUN8
0359 00FF 40           LBZ    0
0360 0100 70           LAI    0
0361 0101 3A           XC     1
0362 0102 7C           LAI    12
0363 0103 32           XCI    1
0364 0104 80           JMS    REST
0365 0105 8E           JMS    F
0366 0106 8E           JMS    F
0367 0107 8E           JMS    F
0368 0108 80           JMS    REST
0369 0109 8E           JMS    F
0370 010A 8E           JMS    F
0371 010B 8E           JMS    F
```

S2559 Digital
Tone Generator

Applications of the S2559 Digital Tone Generator

The S2559 Series Digital Tone Generators were designed specifically for use in the implementation of the DTMF tone dialing push-button telephones. Other applications of the device include radio and mobile telephones, Remote Control, Point of Sale and Credit Card Verification Terminals, Alarm Reporting Devices, Automatic Dialers, etc. This application note describes design considerations, test methods and results obtained using the S2559 Tone Generator in these applications. For detailed specifications of the device refer to the S2559 Data Sheet.

Push-Button Dual Tone Telephone

The primary application of the Digital Tone Generator is in the design of a push-button dual tone telephone. To help explain how it can be used in a modified standard telephone, a description of the standard telephone is presented first.

Figure 1 shows the circuit diagram of a 500 type telephone set, an industry standard. Although there are various manufacturers of the 500 type telephone set, the internal circuitry is similar. Some manufacturers encapsulate all the active circuits with access provided at terminals only. The nomenclature of these terminals and their number may vary, depending upon the telephone model and its manufacturer.

The telephone set is composed of a transmitter, a receiver, an electrical network for equalization and associated circuitry to control sidetone and to connect power and signaling. The transmission circuitry of the telephone set is designed to separate the transmitter and receiver circuits to limit the amount of the talker's signal appearing in his own receiver (sidetone) and to block the direct current in the transmitter from the receiver. A controlled amount of sidetone is necessary for maintaining a natural conversation.

In the diagram of Figure 1, L1, L2 and L3 form a 3 winding transformer and V2, C3, R3, C4 form the sidetone balancing network. With the phone on-hook, hookswitch contacts S1, S2 are open and S3 is closed to protect the transmitter and receiver from ringing current from the central office to pass through the transmitter. When the phone is off the hook, contacts

Figure 1. 500 Type Telephone Set

S1, S2 close, S3 opens and direct current flows in the transmitter. Capacitors in the sidetone balance network prevent the direct current flowing in the transmitter from appearing in the receiver. During dialing, contact S6 across the receiver is closed to eliminate undesirable clicks and contact S5 interrupts the direct current at the dial pulse rate. Capacitor C2 forms a dial pulse filter to suppress high frequency interference into radio sets. Varistor V_3 suppresses clicks in the receiver. Varistors V_1 and V_2 are part of the equalizing network to reduce transmitting and receiving efficiency on short loops.

The varistors have a property of decreasing in resistance with increasing currents. On long loops the direct current from the central office battery is low; the varistor impedances are therefore high and the maximum telephone set efficiency is obtained. On short loops the high direct current results in low varistor impedances which shunt the speech currents and reduce the set efficiency. The overall effect is to make speech volumes at the central office and at the subscriber receivers less dependent on loop length.

The voltage developed in the local transmitter is divided in the windings L1 and L2 so that the voltages induced in the winding L3 are opposing. The voltage across the sidetone network resistance R3 arising from current flowing in winding L2 is arranged to oppose the resultant of voltages induced in L3. The overall effect of this balance is that the current in the receiver as a result of voltages developed in the transmitter is small and thus produces a low sidetone level. On the other hand, speech currents received from the loop pass through windings L1 and L2 and produce additive voltages in winding L3 which is connected to the receiver. These additive voltages are opposed by an approximately equal voltage 180° out of phase which results from the receiving current in winding L2. As a result there is little voltage drop across R3 and maximum receiving levels are obtained without appreciable power loss in resistor R3.

Implementation Using Mechanical Switching

Figure 2 shows how the circuit of Figure 1 can be modified to incorporate the Digital Tone Generator eliminating the dial, adding a push-button keyboard to achieve a push-button dual tone telephone. It is seen that the device interfaces directly with the encapsulated circuitry without modification of it. Diodes D1 through D4 are inserted to insure that the polarity of the direct voltage across the device is the same even if connections to the phone terminals are reversed.

Figure 2. 500 Type Telephone Set Modified for Dual Tone Signaling

MECHANICALLY SWITCHED TRANSMIT AND RECEIVE
FUNCTIONS, DEVICE POWERED DURING KEY CLOSURE.

When the phone goes off-hook and a digit key is pushed, the device is powered up by the closure of common switch contact K2B. Zener V_z insures that the voltage across the device will not exceed the maximum operating voltage. The recommended value for Vz is 12 volts. Common switch K2A opens, removing the drive to the transmitter. The common switch K1 opens, which leaves the receiver connected through resistor Rs. Resistor Rs determines the amount of digit sidetone heard in the receiver. Typical value of Rs is 5.1KΩ.

The tone output of the device can be connected directly to the phone line through resistor R_T. To obtain tone amplitudes in the acceptable range, typically a resistor in the range of 100 ohms to 200 ohms is required. Lower resistor values produce higher amplitudes at the phone terminals but at increased distortion. An alternate way to produce higher amplitudes at the same time keeping distortion low is to use an emitter follower transistor, as shown in Figure 2. R_T is now increased to 10KΩ while R_L is chosen in the range of 100 to 200 ohms to produce the desired amplitude. Lower values of R_L tend to increase amplitude seen at the phone terminals as before.

Implementation Using Electronic Switching

Electronic switching using transistors can be employed to control the transmit and receive functions of the telephone as shown in Figure 3, which depicts an interface circuit for the 2500 type network. PNP transistors Q_T and Q_R are used as series contacts with the microphone and the receiver. In the tone dialing mode, transistors Q_T and Q_R are turned off, while in the voice mode they are turned "on." There is a slight loss in the transmission efficiency due to the finite "on" impedances of the transistors and due to base drive currents required by the two transistors for "hard switching."

Figure 3. Tone Generator Interface Circuit

TYPICAL VALUES

Z1: 1N4742 ZENER 12 VOLT R_0: 10MΩ
R_L: 150Ω Q_2: 2N4401 R_T: 10KΩ
Q_1: 2N4401 R_1: 10KΩ, R_2: 30KΩ, R_3: 2.7KΩ
R_4: 2.4KΩ, R_5: 30KΩ, R_S: 5.1KΩ
Q_R, Q_T: 2N4143
D1-D4: 1N4004
XTAL: 3.579545MHz
C_1: .001μF

2500 NETWORK
X = HOOK SWITCH CONTACTS
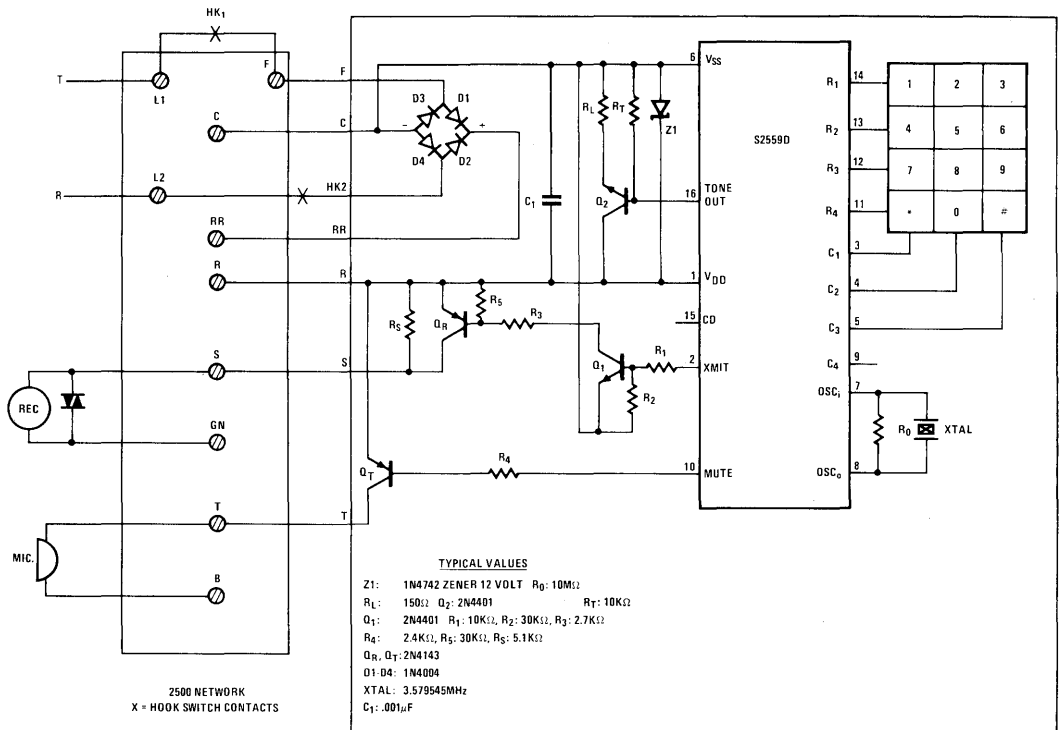
Performance Evaluation

The two major criteria in the evaluation of the Digital Tone Generator in the telephone application are 1) the Amplitude/Loop Current characteristic, and 2) Distortion.

Figure 4 shows a test circuit suitable for these measurements. Note that the circuit allows simulation of DC Loop Conditions only. With this circuit, loop current can be varied over the range of 20mA to 80mA.

Figure 4. Bench Method for Measurement of Amplitude and Distortion Performance
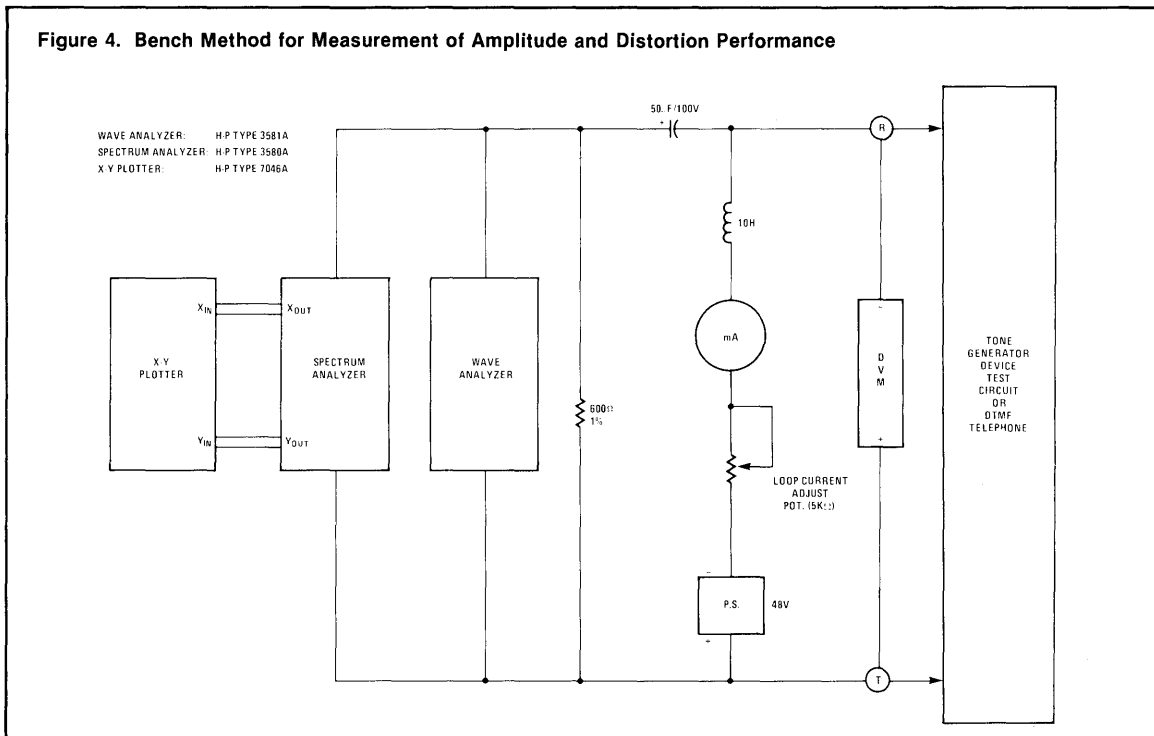
Amplitude Loop Current

Figure 5 shows a typical plot of amplitude vs loop current superimposed on the recommended AT&T specification (ref. 1) obtained using the circuit of Figure 2 with $R_T = 150\Omega$ (external emitter follower stage disconnected) in the test configuration of Figure 4. The absolute amplitude can be increased or decreased in a variety of ways. One way is to vary R_L. R_L typically will be in the range of 100 to 200Ω. Increasing R_L tends to decrease amplitude but improve distortion. Another alternative for increased amplitude is to use a bypass capacitor across R_L. This, however, tends to increase distortion. An emitter-follower transistor can be connected on the tone output. This allows increased amplitude and reduced distortion at the same time. These alternatives are shown in Figure 6. Use of the extra emitter-follower stage, however, decreases the amplitude slope characteristic. In general, a trade-off between amplitude, amplitude slope and distortion is necessary.

Figure 5. Typical Amplitude/Loop Current Plot for Circuit of Figure 2
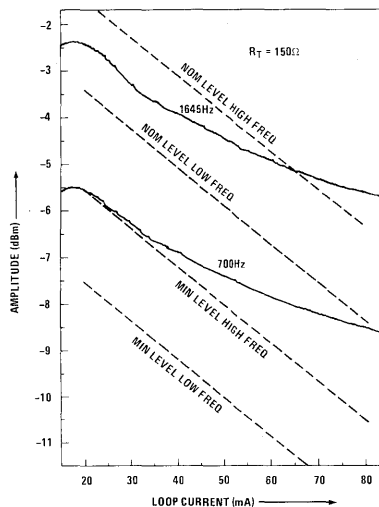
Figure 6. Alternatives for Increasing Amplitude

a) INCREASES AMPLITUDE BUT
INCREASES DISTORTION AND
DECREASES AMPLITUDE SLOPE

b) INCREASES AMPLITUDE,
REDUCES DISTORTION BUT
DECREASES AMPLITUDE SLOPE

Distortion

The AT&T specification (ref. 1) reads "The total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal should be at least 20dB below the level of the frequency pair." The key words here are the total power, voiceband and level of frequency pair. The voiceband is normally defined to be 300Hz to 3400Hz. Therefore, the total power of all extraneous components in the 500Hz to 3400Hz is of interest. The measurement of total power is not easy. To measure it precisely, first the total power of the DTMF signal with extraneous components in the 500Hz to 3400Hz band should be measured. The DTMF signal then should be removed by use of two notch filters centered around the appropriate low group and high group frequencies and the total power measured again. The ratio of the two readings gives a measure of distortion. An alternative is to plot a spectrum of the dual tone waveform and compute distortion using the following formula.

$$\text{Dist. (dB)} = 20 \log \frac{\sqrt{\sum_{i=1}^{n} (V_i)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

$$= 10 \left\{ \log \left[\sum_{i=1}^{n} (V_i)^2 \right] - \log \left[(V_L)^2 + (V_H)^2 \right] \right\} \quad (1)$$

where V_L and V_H correspond to the rms voltage levels of the low group and high group signal components in the dual tone signal and V_i is the ith extraneous (either intermodulation or harmonic) component in the voiceband (500Hz to 3400Hz). Individual component amplitudes in dB can be readily read off from the spectrum plot, converted to (rmsv)^2 by the use of the conversion chart shown in Table 1. Distortion is then calculated by use of equation (1), above.

Figures 7 and 8 show typical spectrum plots obtained in the test circuit of Figure 4 on a S2559D device in the circuit of Figure 3. Detailed distortion calculations on these spectrum plots are shown in Tables 2 and 3. The results show the distortion at 20mA loop current to be -24.9dB and at 30mA loop current -36.3dB. It is evident that distortion decreases rapidly as the supply voltage increases and as the modulation of the supply voltage decreases.

A rule of thumb for quick estimate of distortion is: As a first approximation, distortion in dB equals the difference between the levels in dB of the extraneous component with the highest amplitude and the low group signal component; or

$$\text{Dist. (dB)} = V_{ih \, (dB)} - V_{L \, (dB)} \quad (2)$$

Using this rule of thumb gives estimates of -25dB and -37dB respectively for the loop currents of 20 and 30mA which are close to the computed values of -24.9dB and -36.3dB.

Table 1. dB to (rmsV) and (rmsV)² Conversion Chart

dB	(rsmV)	(rsmV)²	dB	(rsmV)	(rsmV)²	dB	(rsmV)	(rsmV)²	dB	(rsmV)	(rsmV)²
−1.0	0.8913	0.79433	−20	0.1	0.0100000	−33	0.02238	0.0005012	−46	0.005011	0.0000251
−1.5	0.8414	0.70795	−21	0.089	0.0079433	−34	0.01995	0.0003981	−47	0.00446	0.0000199
−2.0	0.7943	0.63096	−22	0.07943	0.0063096	−35	0.01778	0.0003162	−48	0.00398	0.0000158
−2.5	0.7498	0.56234	−23	0.0707	0.0050119	−36	0.01584	0.0002512	−49	0.00354	0.0000126
−3.0	0.7079	0.50119	−24	0.063	0.0039811	−37	0.014125	0.0001995	−50	0.00316	0.0000100
−3.5	0.6683	0.44668	−25	0.0562	0.0031623	−38	0.01259	0.0001585	−51	0.002818	0.0000079
−4.0	0.6309	0.39811	−26	0.050118	0.0025119	−39	0.01122	0.0001259	−52	0.00251	0.0000063
−4.5	0.5957	0.35481	−27	0.0446	0.0019953				−53	0.00223	0.0000050
−5.0	0.5623	0.31623	−28	0.0398	0.0015849	−40	0.01	0.0001000	−54	0.00199	0.0000040
−5.5	0.53088	0.28184	−29	0.03548	0.0012589	−41	0.0089	0.0000794	−55	0.00177	0.0000032
−6.0	0.5012	0.25119				−42	0.00794	0.0000631	−56	0.00158	0.0000025
−6.5	0.4732	0.22387	−30	0.03162	0.0010000	−43	0.00707	0.0000501	−57	0.0014125	0.0000020
−7.0	0.4467	0.19953	−31	0.02818	0.0007943	−44	0.0063	0.0000398	−58	0.001259	0.0000016
−7.5	0.4217	0.17783	−32	0.0251	0.0006310	−45	0.00562	0.0000316	−59	0.001122	0.0000013

Figure 7. Typical Spectrum Plot of a S2559D Device in Circuit of Figure 3 with Test CKT of Figure 4
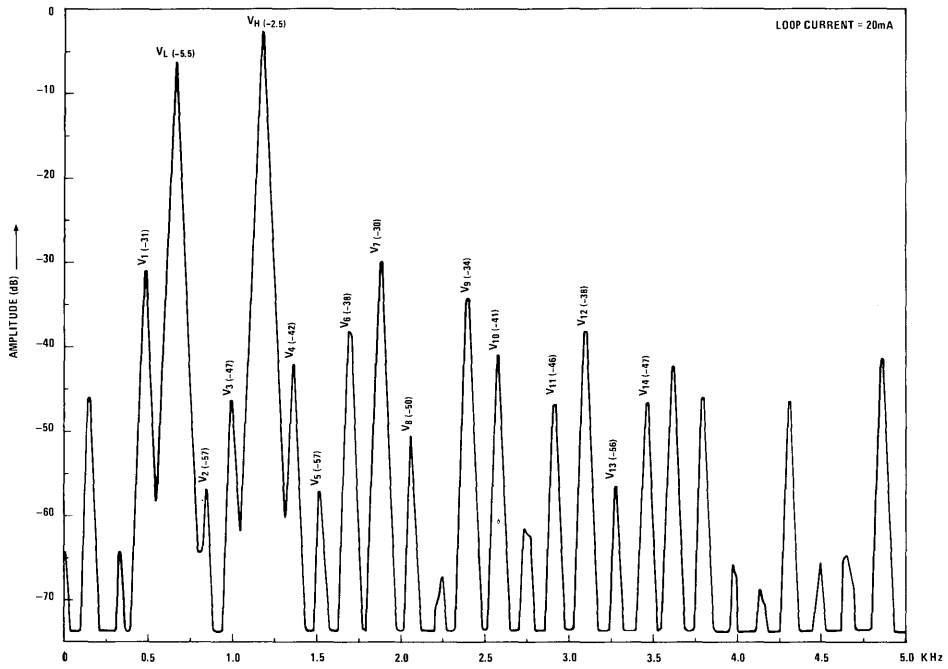

Figure 8. Typical Spectrum Plot of a S2559D in Circuit of Figure 3 with Test CKT of Figure 4
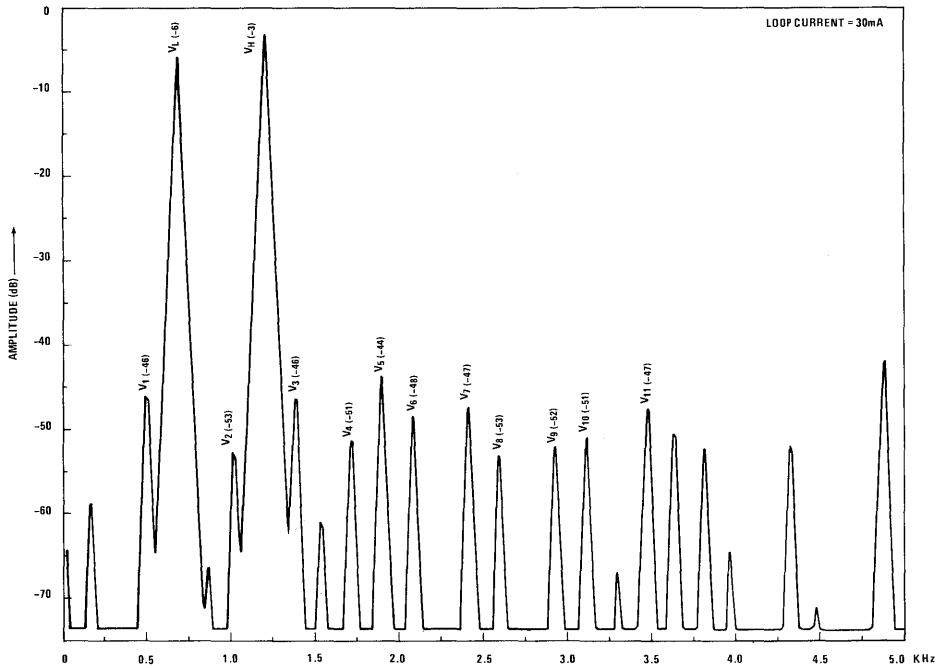
8.21

Table 2. Distortion Calculations for Spectrum of Figure 7

Device: S2559D in Circuit of Figure 3, Test Circuit Figure 4, 20mA Loop Current

Component	Measured (dB)	rmsV INV log $\frac{dB}{20}$	$(rmsV)^2$
V_L	−5.5		.28184
V_H	−2.5		.56234
V_1	−31		.0007943
V_2	−57		.0000020
V_3	−47		.0000199
V_4	−42		.0000631
V_5	−57		.0000020
V_6	−38		.0001585
V_7	−30		.0010000
V_8	−50		.0000100
V_9	−34		.0003981
V_{10}	−41		.0000794
V_{11}	−46		.0000251
V_{12}	−38		.0001585
V_{13}	−56		.0000025
V_{14}	−47		.0000199
V_{15}			.
$\sum_{i=1}^{n}(V_i)^2$			.0027333
$(V_L)^2+(V_H)^2$			.84418

Table 3. Distortion Calculations for Spectrum of Figure 8

Device: S2559D in Circuit of Figure 3, Test Circuit Figure 4, 30mA Loop Current

Component	Measured (dB)	rmsV INV log $\frac{dB}{20}$	$(rmsV)^2$
V_L	−6.0		.25118
V_H	−3.0		.50118
V_1	−46		.0000251
V_2	−53		.0000050
V_3	−46		.0000251
V_4	−51		.0000079
V_5	−44		.0003981
V_6	−48		.0001585
V_7	−47		.0001199
V_8	−53		.0000050
V_9	−52		.0000063
V_{10}	−51		.0000079
V_{11}	−47		.0001199
V_{12}			.
V_{13}			.
V_{14}			.
V_{15}			.
$\sum_{i=1}^{n}(V_i)^2$			.001777
$(V_L)^2+(V_H)^2$			.75236

$$DIST = 20 \log \frac{\sqrt{\sum_{i=1}^{n}(V_i)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\left\{\log\left[\sum_{i=1}^{n}(V_i)^2\right] - \log\left[(V_L)^2+(V_H)^2\right]\right\}$$

$$= 10\left\{-2.56 - (-0.074)\right\}$$

$$= -24.9dB \ (5.7\%)$$

$$DIST = 20 \log \frac{\sqrt{\sum_{i=1}^{n}(V_i)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\left\{\log\left[\sum_{i=1}^{n}(V_i)^2\right] - \log\left[(V_L)^2+(V_H)^2\right]\right\}$$

$$= 10\left\{-3.75 - (-0.124)\right\}$$

$$= -36.3dB \ (1.5\%)$$

Other Considerations

The supply voltage available to the Tone Generator is a function of the DC loop current flowing through the telephone network and the DC impedance presented by the network. The insertion of the diode bridge and voltage drop in the transformer winding further reduce the available voltage. Typically, the DC voltage available to the device is 1.7 volts less than that measured at the TIP and RING terminals. The instantaneous minimum voltage as seen by the device is even smaller because of the DTMF signal riding on the DC component. The instantaneous minimum voltage can be expressed as $V_{min} = V_{dc} - V_{ac}$ (peak). Because the signal amplitude is larger at lower loop currents, i.e., at lower DC voltages, the instantaneous minimum voltage is significantly less than the average voltage measured across the device. This causes higher distortion at lower loop currents.

The DC voltage across the device is under the designer's control during DTMF dialing. The AT&T specification (ref. 1) recommends a minimum DC voltage of 6 volts (4 volts preferred) across the TIP and RING during voice and initial off-hook condition at a loop current of 20mA. However, during DTMF dialing, the DC voltage is permitted to increase to 8 volts (6 volts preferred). The designer can take advantage of this specification to insure adequate voltage across the device at low loop currents. Even with a preferred 6 volt specification, allowing for 1.7 volts drop in the bridge and transformer winding, the average voltage across the device will be at least 4.3 volts. The instantaneous minimum voltage will not drop significantly below 3.6 volts, assuring good distortion performance down to lower loop currents. The voltage across the device can be increased by allowing the telephone DC impedance to increase during DTMF signalling. Since the microphone is switched out during signalling, this is directly a function of the DC current drawn by the device. Since the DC current required by the device is low, it is primarily a function of the load R_L. Increasing R_L will increase the DC impedance and thereby increase the average supply voltage, thus reducing distortion. Increasing R_L, however, reduces signal amplitude so a trade off has to be made between amplitude and distortion.

Consideration should also be given to insure adequate base drive to the external transmit and mute transistors when operating at low loop currents if electronic switching is used.

Transient Voltage Protection

An important consideration in the design of electronic equipment to be connected to the telephone network is that adequate transient voltage protection circuitry must be incorporated such that the equipment can withstand lightning surges without causing harm to the telephone network. In particular, all equipment must meet the metallic and longitudinal surge voltage specifications outlined in the FCC part 68 (ref. 2).

When aplied to tone generator interface circuits, such as those in Figures 2 and 3, transient voltage protection requires proper selection of components for the diode bridge and the zener diode. It is necessary that the diode bridge utilize high voltage breakdown and high current capacity diodes. 1N4004 type diodes may be adequate but higher rated diodes might be required.

Selection of the zener diode depends upon its transient response characteristic. A slow zener diode will not clamp voltage to its rated value. However, it should be noted that the S2559 Tone Generator can withstand pulse voltages that exceed the absolute maximum continuous DC voltage ratings (10.0V for S2559C, D; 13.5V for S2559A, B). Typically, the S2559 devices can withstand up to 20 volts of pulse voltages for durations of

less than 1mS. It should also be noted that the zener diode and the device are behind the network transformer winding and not directly across the telephone terminals. These considerations allow selection of a wide range of zener diodes as protection elements. A zener diode of the type 1N4742 may be adequate in most cases.

Ancillary Interface to Phone Lines

The Digital Tone Generator can be used in ancillary station apparatus (such as alarm reporting devices, automatic dialers, data terminals, etc.) for tone dialing or low speed data transmission applications. A transformer interface, such as that shown in Figure 9, can be used. Consideration must be given to the device latch up possibility due to induced voltage spikes in the transformer winding connected to the tone output. Latch up can be prevented by diode clamping the tone output to V_{DD} and V_{SS}.

Figure 9. Transformer Coupled Phone Interface

T: 600/900 OHMS TRANSFORMER
D1, D2: 1N914 TYPE DIODES
R_L: 1KΩ TYP.
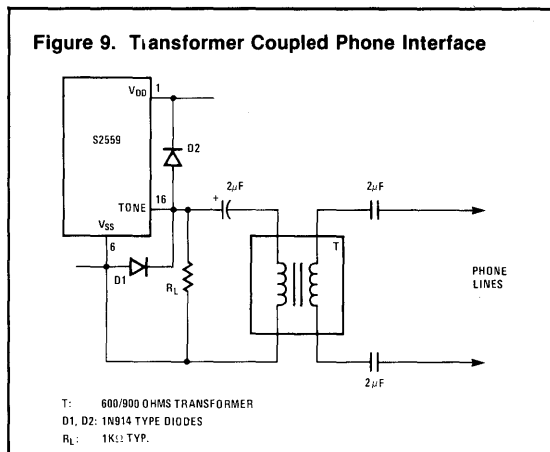
Precise Dial Tone Generator

The Digital Tone Generator can be used in other single or multitone applications by selecting a crystal of appropriate frequency. The precise dial tone is defined to be a multifrequency tone consisting of 350Hz and 440Hz. By selecting a crystal of 1.3071124MHz, a dial tone of 346Hz and 444Hz can be obtained by activating the R4, C1 inputs of the device.

References

Ref. 1:   Bell System Communications Technical Reference (PUB 47001). *Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment.* August 1976.

Ref. 2:   Rules and Regulations, FCC part 68. *Connection of Terminal Equipment to the Telephone Network.* July 1977.

TouchControl™ Circuits
For Capacitance Switching

INTRODUCTION

As more manufacturers turn to solid state electronics to enhance the reliability and performance of their products, the need arises for more reliable, noise-free, nonmechanical switches to control these products. To satisfy this need, AMI offers a series of seven MOS TouchControl circuits that will interface directly with a stationary panel to create a capacitive, nonmechanical switching system. The individual capacitors, or touch switches, are formed simply by conductive areas screened or etched onto the panel's front and rear surfaces; connections between the panel's rear surface and the TouchControl interface circuit create the capacitance switches. As many as 32 touch switches can be implemented with a single TouchControl interface circuit.

Outputs from the S926X series are offered in two configurations: S9260, S9261, S9263, S9264, and S9265 have an individual output associated with each input; the S9262 and S9266 outputs are encoded in binary for use with more complex logic such as microprocessors. All outputs may be used to drive a variety of logic levels such as MOS, CMOS, and TTL.

TouchControl panels may be constructed from many different materials, offering the engineer flexibility in his design. Commonly used panel materials are glass, printed circuit board, plexiglass, and polycarbonate. Selection of a particular material depends on the intended application, as discussed later in this note.

Technical specifications for all seven TouchControl circuits may be found in two data sheets. One describes the S9260, S9261, S9263, S9264, and S9265; the S9262 and S9266 are included in a separate data sheet.

KEYBOARD SCANNING DESCRIPTION

A TouchControl switch panel consists of a single sheet of a rigid material with conductive surfaces applied on both sides as shown in Figure 1.

FIGURE 1 CONSTRUCTION OF A TWO SWITCH TOUCHCONTROL PANEL
WITH EQUIVALENT ELECTRICAL CIRCUIT
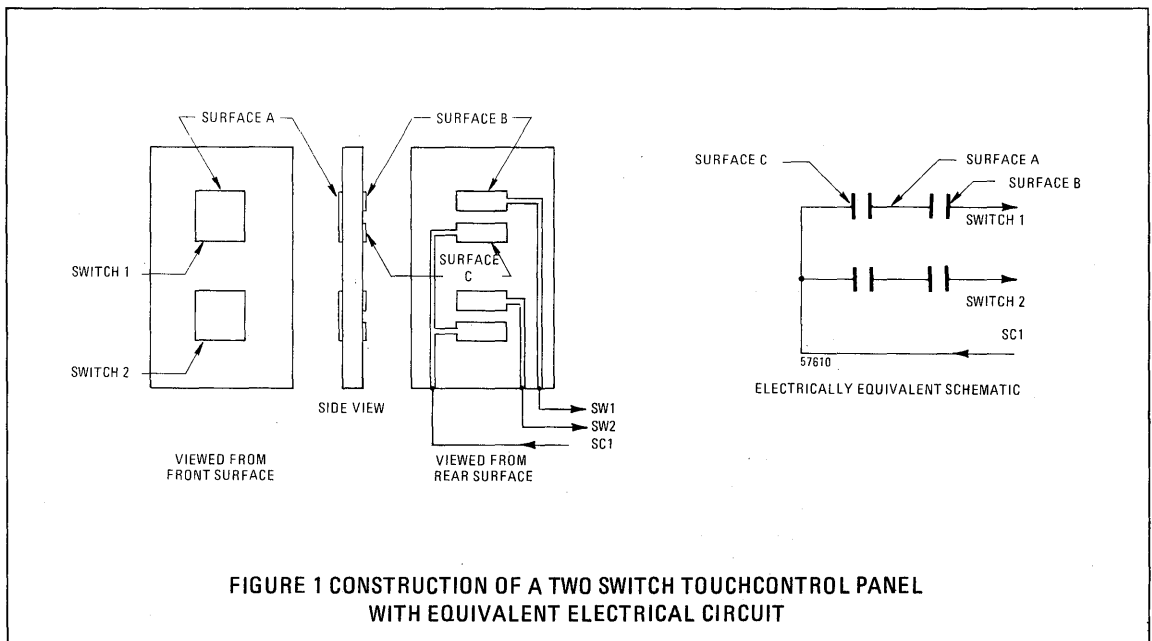
Regardless of the selected panel material, a touch switch is formed by applying a single conductive area to its front surface with two other conductive areas applied directly in line on the reverse side of the panel. Figure 1 shows three views of a typical touch panel containing two TouchControl switches. On switch one, conductive surface A is applied to the front of the panel and is the surface to be touched to effect a switch "closure." Surfaces B and C are applied directly in line with A on the opposite side of the panel. Surface A should cover completely and may overlap surfaces B and C so that a capacitor is formed between "plates" B and A and another between A and C. This forms two capacitors connected in series, their common connection point being the surface to be touched to effect switch operation. For all non-multiplexed parts, all "C" surfaces are connected to the SC1 output. Multiplexed parts (S9262, and S9266) will be discussed later.

Shown in Figure 2, the SC1 output appears as alternating sets of 16 pulses. The peak-to-peak voltage of the SC1 output is approximately equal to the V_{DD} supply level, and the logic 1 (negative) level duration is twice the period of the oscillator frequency at pin 18. Since the SC1 logic 0 level between two adjacent pulses lasts one oscillator period, then the duration of all 16 pulses is $(2 + 1) \times 16 = 48$ oscillator periods. Following the 16 pulses, a logic 0 level appears for a duration of 96 oscillator periods before the next series of 16 pulses commences.

V_C=CLOCK VOLTAGE
V_{INU}=PK. TO PK. INPUT SIGNAL
(SWITCH UNTOUCHED)
V_{INT}=PK. TO PK. INPUT SIGNAL
(SWITCH TOUCHED)
C_P=CAPACITANCE OF TOUCH PAD
C_B=HUMAN BODY CAPACITANCE
(WORST CASE ~ 50 PF.)
C_S=STRAY CAPACITANCE AT CHIP INPUT, INCLUDING CHIP INPUT CAPACITANCE WHICH IS APPROXIMATELY 6 PF.
777231

FIGURE 2. KEYBOARD SCANNING WAVEFORMS

FIGURE 3. CURVES FOR TYPICAL RC VALUES FOR SCANNING FREQUENCY

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The oscillator period is determined by the external RC time constant with values for R and C shown in Figure 3. Note that, if several TouchControl interface parts are used in a given system, all RC pins may be connected together to a single RC time constant.

Each of the 16 pulses in the SC1 signal corresponds to an individual "I" input to the interface circuit. Figure 2 shows the input I5 for both the untouched (VINU) and touched (VINT) conditions. The SC1 signal is coupled through to input I5 through the two touch panel capacitors, C_p. Note that instead of observing 16 pulses at the I5 input as might be expected, only one pulse appears for every 16 SC1 pulses; this is because of an active device on the MOS circuit that grounds the I5 input at all times except for the duration of the sixth of the 16 pulses. (This technique allows the input conductors to be run close to each other, as described in the section on "Proximity of Clock and Input Lines.") It is during this sixth pulse that the touch switch connected to the I5 input is interrogated. (The first SC1 pulse related to I0, the second to

I1, etc.) With the switch untouched, the voltage of the single pulse at I5 will be dependent on the ratio of C_p (touch switch capacitance) to C_S (input stray capacitance, usually equal to MOS input capacitance). For example, if $V_{DD} = -15$ volts and $C_p = C_S$, then $V_C = 15$ volts, and VINU = 5 volts. When the capacitive switch is touched, capacitor C_B (human body capacitance) loads the signal to ground; in this condition, the higher V_{INU} level decreases to a lower V_{INT} level, and the MOS comparator circuitry detects the change, causing the appropriate output to occur. For every set of 16 pulses on the SC1 output, the circuit scans all 16 switches. Although the values of V_{INU} and V_{INT} depend on all capacitances involved, typical values might be V_{INU} = 5 volts; V_{INT} = 1 volt. Calculation of these values, required to insure a reliable system design, is described in the section on "Capacitance Calculations."

Keyboard scanning behaves identically in the S9264 and S9265. The S9260 and S9261 scanning is similar, although only seven inputs are available instead of 16.

The S9266 employs a 2 x 16 matrix to scan 32 touch switches. One set of 16 switches is clocked by SC1 and the other by SC2, as indicated in Figure 4. The first switch and the seventeenth switch share input I0, the second and eighteenth share input I1, etc. Every group of 16 pulses appearing on the SC1 output is followed immediately by a group of 16 identical pulses on the SC2 output. Following the 16 SC2 pulses, both outputs remain at a logic 0 level for a time equal to one set of 16 pulses, after which time the pulses on SC1 again commence. The S9262 device is similar to the S9266, except that its matrix of 2 x 7 (i.e. SC1 and SC2 by seven inputs) scans 14 instead of 32 touch switches.

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FIGURE 4. 2 X 16 MULTIPLEXED MATRIX WITH S9266 INTERFACE CIRCUIT

NOISE IMMUNITY

Just as mechanical switches have a certain amount of contact bounce associated with them, capacitance switches have the same inherent problem. This contact bounce, or noise, occurs as a finger makes contact with or removes contact from the touched switch surface. All seven TouchControl interface parts contain circuitry to prevent this "contact bounce" from appearing on any output.

As discussed in the section on "Keyboard Scanning," the S9263 scans all 16 keys in the time required for 48 periods of the oscillator, and a total of 96 additional periods are required before the scan begins again. During the first 48 of these 96 additional periods, the SC2 output scans its 16 key inputs. Thus, for any of the seven parts, a complete scan of the keyboard occurs in 48 + 96 = 144 periods of the RC oscillator. After every 23 of these complete keyboard scans, a signal is generated on the circuit that clocks the most recent scan information into 32 two-bit shift registers (one for each of 32 switches). Thus, this load pulse occurs every 144 x 23 (=3312) oscillator periods. If a logic one level is loaded into the first bit of one of the registers, indicating a touched switch, no change in output condition occurs, because the second bit of the register is at a zero level. When the next load pulse is generated 3312 periods later, however, if the switch is still touched, another logic one level is clocked into the register, and a one level is transferred from register bit one to register bit two; since both register bits are now "ones," the output is allowed to change state. This means that a minimum of 3312 and a maximum of 6624 oscillator periods are required between the touching of any switch and the changing of any output condition. For an oscillator frequency of 90 kHz, for example, an average of 55 ms of debounce time is obtained. The same debouncing method is applied to the release of any touch switch.
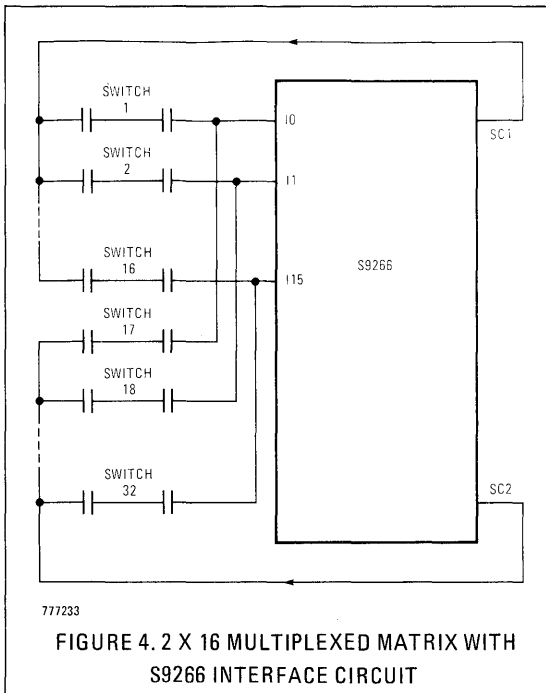
DETERMINATION OF TOUCH SWITCH SIZES

Because one of TouchControl's major advantages is the versatility it offers the design engineer, the actual size of the TouchControl switch becomes an important consideration. As shown in Figure 1, a TouchControl switch consists of three conductive areas, one of which is applied to the front surface of a panel. The other two areas are each slightly less than half the area of the first and are located directly behind on the rear side of the panel so that each forms a capacitor, C_p, with the larger conductive area on the front surface of the panel.

To insure a reliable TouchControl system, it is important that each of these capacitors, C_p, has the required capacitance value. This value depends on a number of factors such as power supply, reference voltage, scan clock voltage, and input stray capacitance; it is discussed in detail in the section on "Determining Required Capacitance Values."

After determining the required value for C_p, it is then easy to calculate the area of the touch switch from the relationship,

$$C_p = \frac{0.225\ KA}{t}$$

in which K is the relative dielectric constant of the panel material, A is the area in square inches of one of the two rear surface conductive areas, and t the panel thickness in inches. This equation calculates C_p in picofarads. Figure 5 provides some nomographs for quick determination of pad area. Since two of the three variables in the equation, K and t, depend entirely on the touch panel, it is clear that the selection of the panel material entails some electrical as well as aesthetic consideration. Touch switches of small area can be formed by choosing a panel material of high dielectric constant and minimum thickness.

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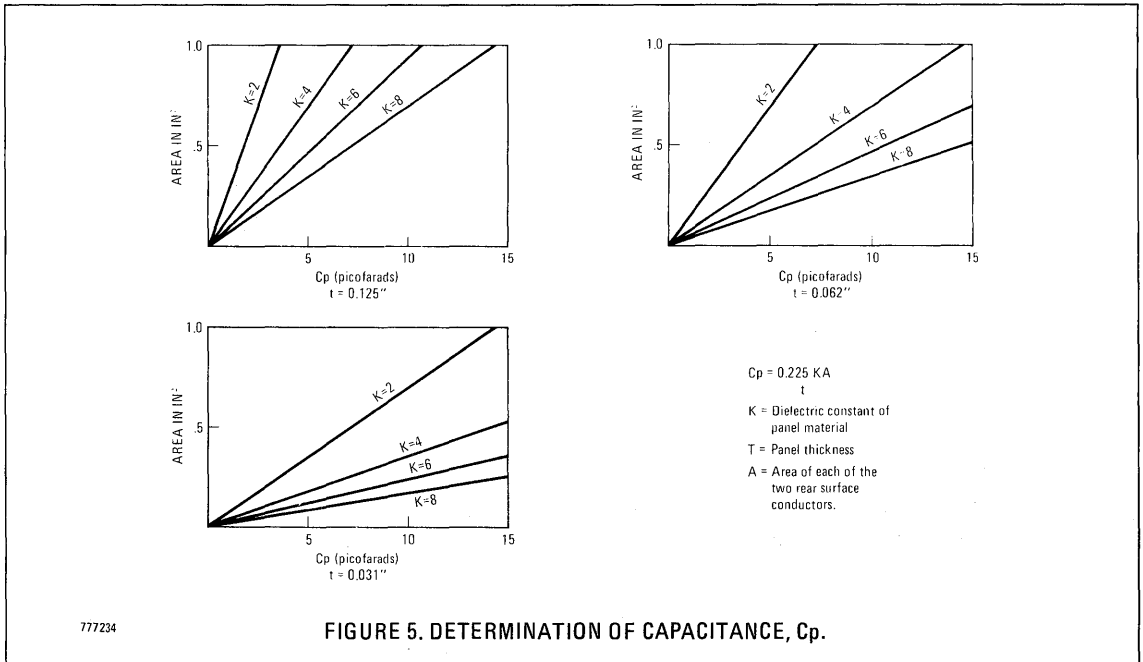
FIGURE 5. DETERMINATION OF CAPACITANCE, Cp.

A typical touch switch area calculation might take these steps: From the information determined in the section on "Determining Required Capacitance Values" it is discovered that a particular system requires 7 picofarad C_p capacitors. The panel material is to be a .062 inch thick printed circuit board with a dielectric constant of 5.0. From the relationship

$$C_p = \frac{0.225 \, KA}{t}$$

it is seen that an area, A, of 0.386 square inches is required for each of the two rear surface conductors. If the touch switch area is to be approximately square, then each of the two rear surfaces must have a length about twice its width. Each rear surface conductor can be 0.44 x 0.877 inches, giving an area of 0.386. Separating the two conductors by 0.125 inches, the area required for the front surface touch switch then, is $(2 \times .44 + 0.125)$ by .88 or 1.0 x 0.88 inches.

Of course the touch switch can be designed in many different shapes by altering the dimensions of the three conductors, keeping the rear surface areas constant and insuring that each rear surface conductor is "covered" completely by the front surface conductor (touch pad). If, in this example, the 1.0 x 0.88 inch touch switches are too large, there are several options available. The most obvious would be to use a thinner panel material to increase the C_p capacitance, allowing the switch areas to be smaller. Another alternative is to increase the scan clock voltage, as described in the section on "Determining Required Capacitance Values," to allow the use of smaller C_p capacitors.

DETERMINING REQUIRED CAPACITANCE VALUES

What is required for a reliable TouchControl system is that the peak-to-peak signal level appearing at any "I" input of the interface IC be equal to or greater than a certain value when the switch is untouched and equal to or less than another fixed value when the switch is touched. It is this variation in amplitude that causes the circuit to recognize whether or not a switch is being touched. Referring to Figure 2, the higher voltage level appearing on an input and caused by an untouched switch has been designated V_{INU}. The lower level, V_{INT}, occurs whenever the switch is touched. It can be seen that the V_{INU} level is determined by the peak-to-peak scan clock output level, V_C, the value of the series touch capacitors, C_p, and the value of stray capacitance, C_S, at the input to the circuit. The V_{INT} level is affected by all these parameters plus the value of human body capacitance, C_B, which ranges typically from 100 to 200 picofarads with a typical minimum value of 50 pF. Because most of the capacitances involved are on the order of 10 pFs or less, it is not meaningful to measure V_{INU} to V_{INT} with conventional equipment. However, it is possible to calculate their values accurately, given V_C, C_p, C_S, and C_B, and these calculations are the first steps in determining the required touch capacitors for a given system. The simplest approach is to assume a C_p value and then determine V_{INU} and V_{INT}.

To calculate V_{INU} and V_{INT} for all conditions:

$$V_{INU} = \frac{C_p \, V_C}{C_p + 2C_S}$$

$$V_{INT} = \frac{C_p^2 V_C}{C_p^2 + C_p C_B + C_S C_B + 2C_p C_S}$$

As already stated, V_{INU} must be equal to or greater than a specified value, and V_{INT} must be equal to or less than another specified value. What these values are is determined by the use of the input pin labeled V_{REF}. This pin is used to establish a reference voltage which the internal comparator compares against the "I" input voltage levels to determine if a switch is touched. In some cases it is possible to connect the V_{REF} pin to ground (V_{SS}). In others, it may be beneficial to set V_{REF}, using two resistors, to a value that is 20 percent of the V_{DD} supply level. If V_{REF} is connected to ground (V_{SS}), then V_{INU} must be $\geqslant 4.0$ volts and V_{INT} must be $\leqslant 1.3$ volts. If these two conditions are met, the resulting TouchControl system will operate satisfactorily.

In many proposed TouchControl systems, calculations of V_{INU} and V_{INT} will indicate that the range of 4 to 1.3 volts is difficult to achieve due to high C_S capacitance or the need for small switches. In such cases it may be beneficial to use the V_{REF} input to provide a reference voltage for the internal comparator. This comparator typically operates over a V_{REF} range of from – 2.5 volts to – 3.8 volts. Whenever V_{REF} is within this range, the TouchControl system will function properly under the conditions: $V_{INU} \geqslant V_{REF} + 1.0$ volt and $V_{INT} \leqslant V_{REF} - 0.5$ volt.

If the V_{REF} voltage is derived from the V_{DD} supply voltage using two resistors as a voltage divider, an additional advantage is obtained. As V_{DD} varies, the V_C level (SC1 output level) changes, and so does the V_{REF} level. This causes the V_{REF} level to track the scan clock voltage, making the circuit less vulnerable to supply fluctuations. If, for example, V_{REF} is set to a value 20% of the V_{DD} supply voltage, then as the supply, and hence V_C, varies from – 13.5 to – 18.0 volts, V_{REF} will vary from – 2.7 to – 3.6 volts, remaining within the

comparator's operating range. Setting V_{REF} equal to 20% of the V_{DD} (or V_C) level, the following expressions will insure a functioning TouchControl system:

| UNTOUCHED SWITCH CONDITION	TOUCHED SWITCH CONDITION
$V_{INU} > V_{REF} + 1.0$	$V_{INT} < V_{REF} - 0.5$
$V_{REF} = .2\ V_C$	$V_{REF} = .2V_C$

Substituting the expressions for V_{INU} and V_{INT}:

$$\frac{C_p V_C}{C_p + 2C_S} > .2V_C + 1.0 \qquad \frac{C_p^2 V_C}{C_p^2 + C_p C_B + C_S C_B + 2C_p C_S} < .2\ V_C - 0.5$$

or

$$\frac{C_p}{C_p + 2C_S} > .2 + \frac{1}{V_C} \qquad \frac{C_p^2}{C_p^2 + C_p C_B + C_S C_B + 2C_p C_S} < .2 - \frac{0.5}{V_C}$$

From these expressions, it can be seen that the required C_p value is highly dependent on the stray capacitance at the TouchControl input, and only slightly on the fluctuation of the V_C level. It is also of interest to note that, in both cases, the "worst case" condition is the lowest expected V_C value, and the highest expected V_C value is irrelevant. For calculation of the required touch switch capacitance, C_p, for a given input stray capacitance, C_S, reference can be made to Figure 6. These curves may be used for any TouchControl system in which the reference voltage is set to between 18 and 22 percent of V_{DD}, V_{DD} is within the specified limits of - 13.5 volts to - 18.0 volts, and V_C, the peak-to-peak scan clock voltage, is determined by the SC1 output (i.e., $V_C = V_{DD}$ and no external amplification of V_C is used). The upper curve represents the case where the switch is touched, and the lower corresponds to the untouched condition. Operating TouchControl between the two curves results in a properly functioning system.

FIGURE 6. C_P VS. C_S FOR $V_C = V_{DD}$
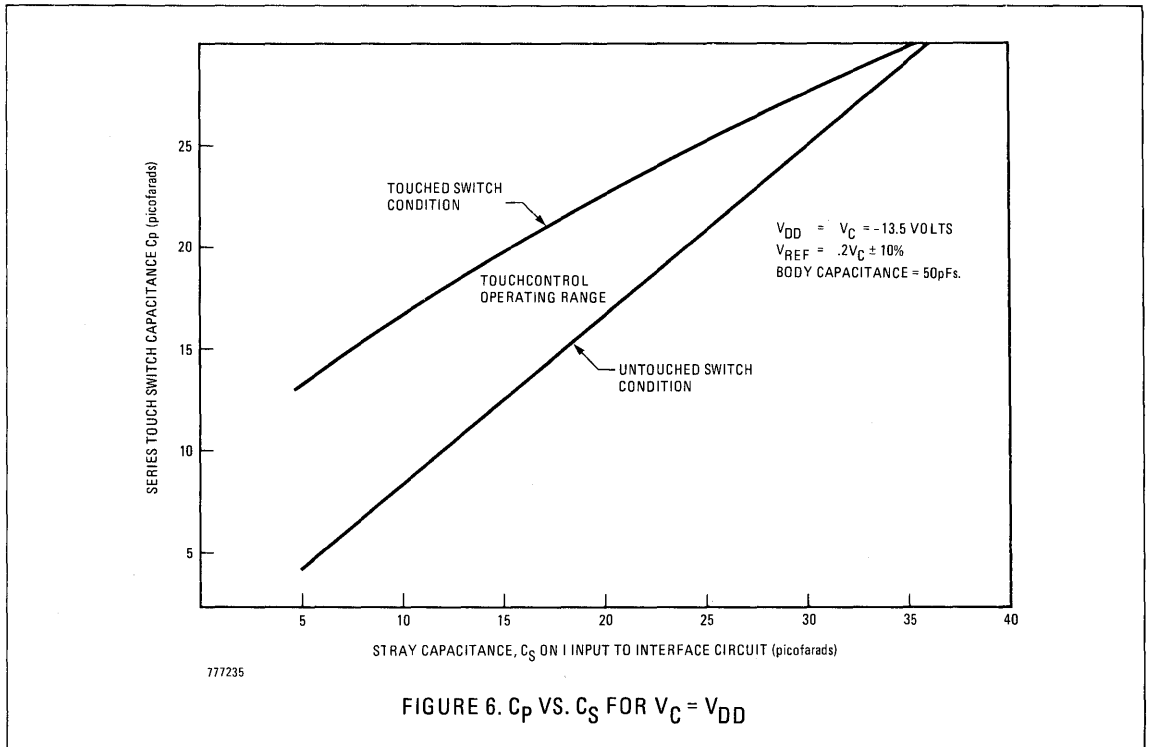
As a specific example, assume that a proposed Touch-Control system is to be implemented on a printed circuit board. The traces that connect the individual switch areas to the I inputs are to be arranged on the board such that the longer traces contribute 4 pF to the stray input capacitance, while the shorter traces contribute only 1 pF. Since the MOS input capacitance is typically 6 pFs, then the total stray capacitance on any input, C_S, will vary from (1 + 6 pFs) to (4 + 6 pFs), or 7 to 10 pFs. Referring to the curves in Figure 6 again, it can be seen that the system will function over the 7 to 10 pF C_S range if a touch capacitor, C_p, is chosen between 8.2 pFs and 14.5 pFs. Now that the required C_p capacitance is known, the switch area can be determined from the relationship

$$C_p = \frac{.225 \, K \, A}{t}$$

as previously discussed. If the resulting switch area is too large for the intended application, it is possible to decrease the required C_p value by increasing the V_C scan clock level. This is discussed in the following section.

INCREASING SCAN CLOCK VOLTAGE

As has been described, the capacitance required for TouchControl switches, and hence the area required for the switches, is dependent on input stray capacitance, C_S, human body capacitance, C_B, and the scan clock output level, V_C. If it is necessary in a given system to use small switches, or if the C_S loading is high, it is possible to reduce the required touch pad capacitance, C_p, by increasing V_C. Although it is not advisable to increase V_{DD} higher than – 18.0 volts, it is possible

to insert external circuitry between the SC1 output and the keyboard clock bus to increase V_C.

One method of increasing V_C is to use a voltage doubler circuit, such as shown in Figure 7. This circuit is driven by the SC1 (or SC2) output, doubles the voltage, and provides a scan clock with a V_C of twice the V_{DD} level (minus 3 to 4 volts). At V_{DD} = – 13.5 volts, the doubler consumes typically 20 mA, and at V_{DD} = – 18 volts, it uses about 28 mA. The curves in Figure 8 can be used to calculate the required C_p, given C_S. The solid lines apply to a system in which a voltage doubler is used to provide a V_C of 23 to 32 volts from a V_{DD} supply of – 13.5 to – 18.0 volts. The dotted lines represent the best performance obtainable with the doubler circuit, describing a a system with a 30 volt V_C and – 2.7 volt reference. It can be seen that both these sets of curves allow the use of smaller touch capacitors, C_p, than if the doubler were not used, as in the curves of Figure 6.

If a still smaller C_p is required, V_C may be increased further by use of a separate power supply and a non-inverting buffer, as shown in Figure 9. For these higher V_C values, the expressions already given for V_{INU} and V_{INT} can be used to determine the required C_p values, keeping in mind the conditions that $V_{INU} > V_{REF} + 1.0$ volts, $V_{INT} < V_{REF} - 0.5$ volts, and V_{REF} is set between – 2.5 and – 3.8 volts. For high values of V_C, it is possible to use very low touch capacitors, as indicated by Figure 10. These curves plot V_C vs. C_p for two values of C_S, 9 pFs and 14 pFs. A fixed V_{REF} of – 3 volts is assumed. If C_S = 9 pFs, for example, it can be seen that an 8 pF C_p is required for a V_C of 16.0 volts, whereas raising V_C to 40 volts permits the system to function with a 2 pF C_p value.
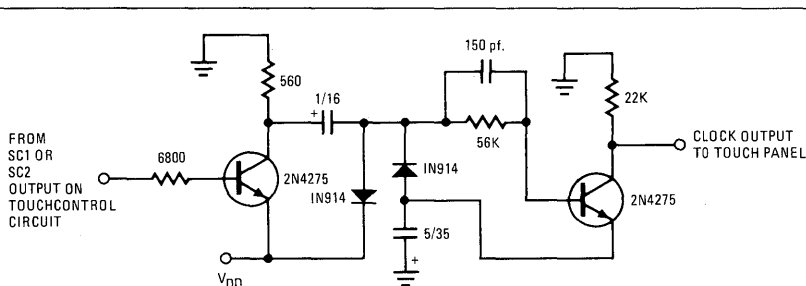

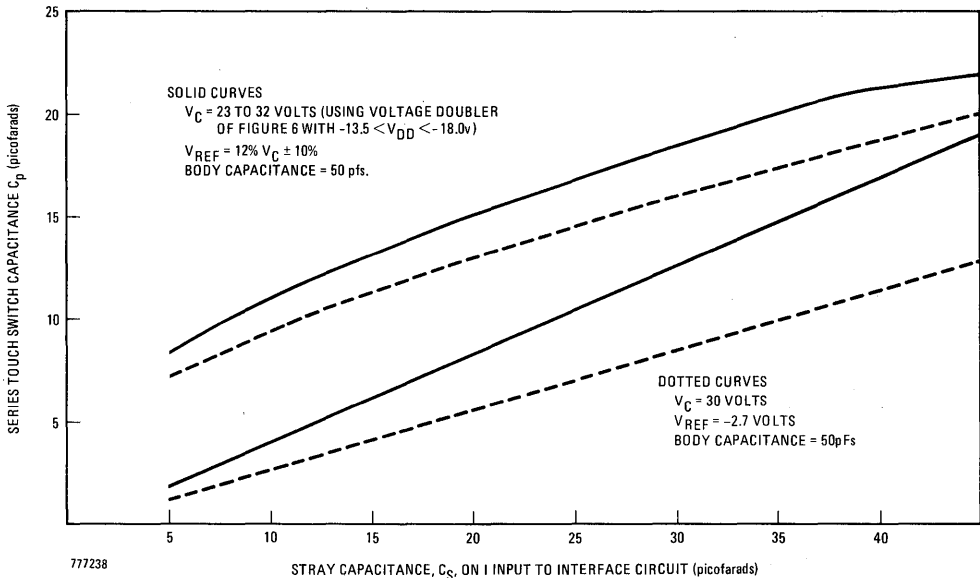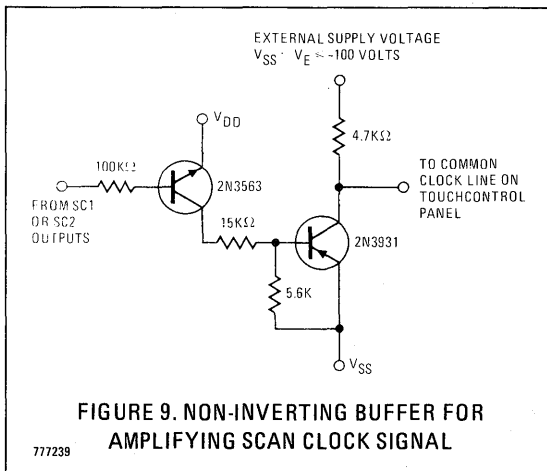FIGURE 7. TOUCHCONTROL SCAN CLOCK VOLTAGE DOUBLER

777237

FIGURE 8. C_P VS. C_S FOR $V_C > V_{DD}$

SOLID CURVES
V_C = 23 TO 32 VOLTS (USING VOLTAGE DOUBLER OF FIGURE 6 WITH -13.5 < V_{DD} < -18.0v)
V_{REF} = 12% V_C ± 10%
BODY CAPACITANCE = 50 pfs.

DOTTED CURVES
V_C = 30 VOLTS
V_{REF} = -2.7 VOLTS
BODY CAPACITANCE = 50pFs

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STRAY CAPACITANCE, C_S, ON I INPUT TO INTERFACE CIRCUIT (picofarads)

SERIES TOUCH SWITCH CAPACITANCE C_P (picofarads)

FIGURE 9. NON-INVERTING BUFFER FOR AMPLIFYING SCAN CLOCK SIGNAL

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EXTERNAL SUPPLY VOLTAGE
V_{SS} · V_E ≃ -100 VOLTS

V_{DD}

100KΩ

FROM SC1 OR SC2 OUTPUTS

2N3563

4.7KΩ

TO COMMON CLOCK LINE ON TOUCHCONTROL PANEL

15KΩ

2N3931

5.6K

V_{SS}

MULTIPLEXED OPERATION

To permit a larger number of switches to be interfaced by a single TouchControl circuit, two parts employ a keyboard matrix approach. The S9262 uses a 2 x 7 matrix to control 14 switches, and the S9266 uses a 2 x 16 matrix to control 32 switches. As described in the section on "Keyboard Scanning," these parts provide two scan clock outputs, SC1 and SC2. Each of the "I" inputs shares two touch switches, one clocked by SC1 and the other by SC2, as shown in Figure 4.

The multiplexed parts operate similarly to the non-multiplexed circuits, and the expressions and curves already presented for V_{INU} and V_{INT} calculations are valid for all TouchControl parts. It is important to note, however, that there are two touch capacitors connected to each input of the multiplexed devices. When one of a pair is being scanned, the other acts like two capacitors connected in series loading the input, and that load must be added to C_S. For example, if
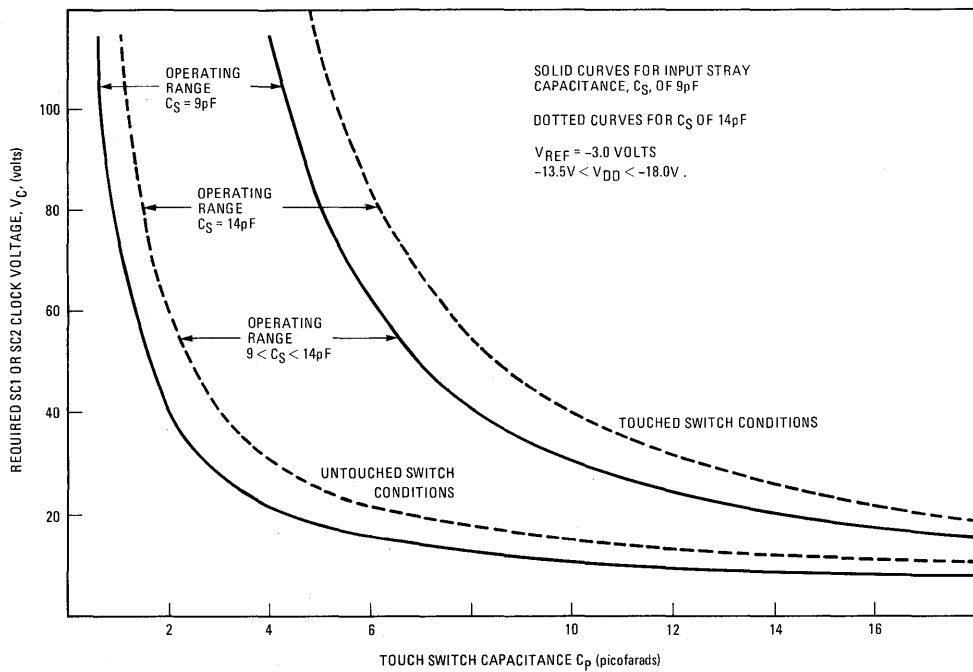
OPERATING RANGE C_S = 9pF

OPERATING RANGE C_S = 14pF

OPERATING RANGE $9 < C_S < 14pF$

SOLID CURVES FOR INPUT STRAY CAPACITANCE, C_S, OF 9pF

DOTTED CURVES FOR C_S OF 14pF

V_{REF} = –3.0 VOLTS
$-13.5V < V_{DD} < -18.0V$.

TOUCHED SWITCH CONDITIONS

UNTOUCHED SWITCH CONDITIONS

REQUIRED SC1 OR SC2 CLOCK VOLTAGE, V_C, (volts)

TOUCH SWITCH CAPACITANCE C_p (picofarads)

FIGURE 10. REQUIRED V_C VS. C_p

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8 pF C_p capacitors are being used with a multiplexed part, and the stray capacitance developed on an input node due to the printed circuit traces is 2 pFs, then the total C_S capacitance will be 6 pF (circuit's input capacitance) plus 2 pF (from P.C. traces) plus 4 pF (two 8 pF capacitors in series), or a total of C_S = 12 pF.

When using the S9262 or S9266 multiplexed parts, attention must be paid to any unused inputs. Whereas unused inputs may be left unconnected in all nonmultiplexed devices, this is not possible with the S9262 and S9266. Two solutions exist for unused inputs on these parts. The first is to connect a capacitor between the input and the appropriate scan clock output, causing the capacitor to look like a "dummy" touch capacitor. Its value should be 0.5 C_p. The other solution is to connect all unused inputs to a – 5 volt supply level, which may be derived from two external resistors, each of which should be less than 2KΩ. If an odd number of switches is to be unused, then at least one "dummy" capacitor is required.

Available only with the S9266, a two key rollover feature is provided. This feature is selected by hard-wiring pin 17 to V_{DD}. When selected, this feature causes the circuit to ignore two simultaneously touched switches. If switch A is selected first, and then switch B is selected, only the output associated with switch A will be observed. If A is then released while still touching B, the B output condition will occur.

TOUCHCONTROL PANEL MATERIAL

Selection of the best material for a given TouchControl panel depends on the intended application. Many materials are suitable for the panels, the main requirements being that they must have controllable thickness and dielectric constant. Some of the more common materials in use today are glass, printed circuit material, plexiglass, and polycarbonates.

The use of glass as a panel material has several advantages. The first is the ability to apply conductive tin oxide coatings to a glass panel's front surface to form the touch switches. The tin oxide is then fired at a high temperature, and the result is an extremely durable TouchControl panel. The transparent property of the tin oxide coatings would permit the design of virtually invisible touch switches. Another favorable property of glass is its high dielectric constant. Though it varies depending on specific compositions, a relative dielectric constant of 8 can be achieved with glass.

Plastic materials, such as plexiglass, can also be used to make TouchControl panels. These panels are lightweight and, in some cases, may be less expensive than the comparable glass panel. In place of the tin oxide coatings, various conductive inks or paints can be applied to form the switch areas on a plastic panel. These materials are not quite as durable as the tin oxide coating but appear to be durable enough for most switch panel applications. Where small switches are required, plexiglass has the disadvantage of a low dielectric constant (about half that of glass), although this often can be compensated for by use of the clock doubling methods discussed earlier.

The use of polycarbonate material may be applicable for panels requiring a high impact resistance. Aside from its durability and somewhat higher cost, it behaves similarly to plexiglass.

Whenever possible, the most convenient material to use for a TouchControl panel is printed circuit material. The TouchControl switches are formed by conventional etching of a standard double-sided circuit board. To avoid the problem of discoloration of the copper, it is advisable to plate the board with a nickel alloy. The advantage obtained by using a circuit board is the ability to locate all connections between the switches and the interface circuit on the rear surface of the board as a part of the etched pattern. The TouchControl circuit plugs directly into the TouchControl panel, along with other associated components. Connections from the panel to external circuitry can then be made with an edge connector.

The dielectric constant of printed circuit materials is somewhat lower than glass, but this is compensated by the ability to produce much thinner circuit boards. Whereas 0.125 inches is the practical minimum glass thickness, circuit boards can be produced easily as thin as 0.031 inches. The biggest objection to the use of printed circuit touch panels is appearance. Although standard printed circuit material is often not aesthetically pleasing, it is possible through the use of decorative inks to design an attractive TouchControl panel for use in a variety of applications.

Connecting TouchControl switches to the interface circuit inputs is as important a consideration as the selection of the panel material. As already stated, this task is easiest if a printed circuit touch panel is used. If glass or plastic panels are used, one method of connecting the circuitry to the panel is inserting individual contactors in a printed circuit board which is then forced up against the rear surface of the panel. It is also possible to use an edge connector into which the glass or plastic panel can be inserted.

SEPARATION BETWEEN INPUT AND
SCAN CLOCK CONDUCTORS

A typical concern in the design of a TouchControl panel is the allowable spacing between the conductors that run from the switches to the interface circuit's inputs. Because of a unique feature offered by all AMI TouchControl parts, this poses less of a problem than might be anticipated. Every "I" input has an active output transistor connected to it that actually pulls that input to V_{SS} for all times except when that input is interrogated by the scanning logic. Stated differently, whenever any input is being interrogated, all other inputs are pulled to V_{SS}. This means that no matter how much capacitance is developed between adjacent "I" inputs, there can be no crosstalk between them to supply invalid information. It should be noted, however, that running adjacent traces or wires close together for long distances develops capacitance to ground; this capacitance must be measured and added to the stray capacitance, C_S, when calculating V_{INU} and V_{INT} values. Since some switches will usually be farther from the circuit than others, C_S may vary for different inputs. To compensate for this, it is possible to use larger rear-surface conductive areas for switches whose inputs develop higher C_S capacitance, usually the switches farthest from the circuit. Note that the front surface touch switch areas can remain identical in size.

A related concern involves the location of the SC1 or SC2 clock outputs. These outputs contain a clock signal at all times and thus would adversely affect operation if substantial coupling developed between either output line and any "I" input. It is a good practice to keep the clock output(s) isolated from any inputs. To insure proper operation, it is necessary to keep the ratio of touch capacitor, C_p, to the capacitance developed between SC1 (or SC1) and any input greater than 20 to 1.

Another related item is the allowable proximity of the two rear surface conductors of a touch switch to each other. It is necessary that a minimum amount of capacitive coupling exists between these conductors so that the clock signal is coupled through the two C_p capacitors and not directly between the two rear surface conductors. The spacing between these two areas should insure that the ratio of C_p to the capacitance developed between the two conductors be at least 20 to 1. For example, if the series touch capacitance, C_p, is 8 pFs, there should be no more than 0.4 pFs developed between the two rear surface conductors. Two typical rear surface conductors of dimensions 0.375 inches by 0.75 inches spaces 0.188 inches apart would develop about 0.3 pFs capacitance between them.

OUTPUT CONFIGURATION

Each output stage of all seven TouchControl circuits consists of a single MOS transistor, as shown in Figure 11. This is true regardless of whether the outputs are direct, as in the S9260, S9261, S9263, S9264, and S9265, or encoded, as in the S9262 and S9266. The drain of each output transistor is connected to the appropriate output pin; the sources of all output transistors are connected in common and tied to the V_{BB} supply pin. When an output transistor is turned on, either by the touching of a Touch pad or by the latching on of an output in the toggle mode, its output pin becomes a low impedance to the V_{BB} supply voltage. The data sheets for these parts should be referenced to determine actual impedance values. This allows the user to define the magnitude and polarity of the output voltage swing by setting the V_{BB} supply voltage to any desired level over the range of V_{SS} to V_{DD}. It should be noted that, since the outputs are open-ended (i.e., not push-pull), an external load or pullup resistor must be connected to each output and tied to whatever output level is expected when the output transistor turns off.

For example, Figure 15 shows an S9266 whose V_{BB} supply pin has been tied to V_{SS}, or + 15 volts. When an output device (B0 through B4) turns on, it supplies + 15 volts to the logic gate it drives. When an output is off, the pulldown resistor R5, causes the B output to return to V_{DD}, or 0 volts.

Because of the output configuration, it is possible to use TouchControl devices to multiplex analog or digital information. Although the V_{BB} pin would often be connected to a supply voltage, it does not need to be. It can actually be used as an output, using the O0 through O15 "output" pins as inputs. For example, if the Touch pad connected to I5 input is touched, then whatever signal is present on the O5 "output" pin is switched to the V_{BB} pin. A specific application of this is shown in Figure 16, the TouchControl Organ. All musical frequencies are continuously generated by the S50240 top octave synthesizer and the S10131 divider circuits. These frequencies are fed to the "O" pins on the S9263 TouchControl devices. As the TouchControl I inputs are activated by touching the capacitive keys, the desired musical freqencies appear at the V_{BB} "output" and are amplified. Multiple keys may be played simultaneously, making the TouchControlled organ completely polyphonic.
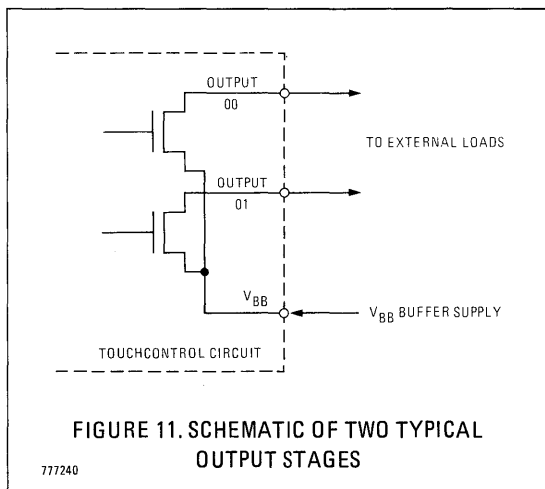

FIGURE 11. SCHEMATIC OF TWO TYPICAL OUTPUT STAGES

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TOUCHCONTROL INPUT PROTECTION

All seven TouchControl interface parts have devices on all inputs to protect them from the effects of static charge that could be introduced by a charged body touching a switch.

TouchControl systems in some environments, however, may be subjected to an excessive amount of static discharge that might damage the circuits. An extremely dry room with heavy carpeting would be an example of such an environment. To protect TouchControl circuits from excessive static discharge, we recommend the addition of the following external components:

1)   150KΩ resistor in series between each touch switch and "I" input.
2)   10KΩ resistor in series between SC1 and/or SC2 outputs and the TouchControl panel.
3)   Clamp diodes (such as 1N914) on SC1 and/or SC2 outputs. Connect anode of one diode to SC1, with its cathode connected to V_{SS}. Connect cathode of a second diode to SC1, with its anode connected to V_{DD}. (The S9262 and S9266 have two clock outputs, SC1 and SC2, and hence will require four diodes.)

MECHANICAL KEYBOARD ENCODER

The S9262 and S9266 can both be used as conventional mechanical keyboard encoders if capacitance switches are not required. Figure 12 shows an S9266 connected to a set of 32 mechanical switches. The capacitors in series with each normally-closed mechanical switch take the place of the C_p touch capacitors that would be used in a capacitance keyboard. When switch one is opened, for example, the SC1 signal can no longer pass through the capacitor to input I_0, and output code 0 0 0 0 0 will appear on B outputs (AK output will equal

"1"). This configuration will encode a set of 32 switches onto five binary outputs. These outputs can be wire-ored to allow the encoding of additional keys. That is, two S9266 devices could be used to encode 64 switches; their "B" outputs are connected in common, and the most significant bit is obtained from the AK output of the second S9266 circuit.

A corollary to this application is a touch panel that uses some mechanical switches along with some capacitance switches. The only concern here is that the capacitor, C, should be half the value of touch capacitor, C_p.
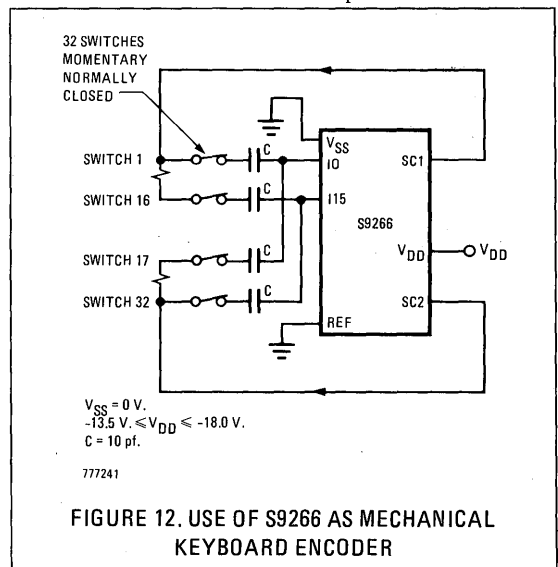


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32 SWITCHES
MOMENTARY
NORMALLY
CLOSED
```

$V_{SS} = 0 V.$
$-13.5 V. \leqslant V_{DD} \leqslant -18.0 V.$
$C = 10 pf.$

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FIGURE 12. USE OF S9266 AS MECHANICAL KEYBOARD ENCODER

NOTE: ALL OUTPUTS LOADED TO V_{DD} WITH 10K RESISTORS

V_{SS} = 0V
V_{DD} = –15V ± 10%
D1, D2, D3 = 1N914
C1 = 0.33μF
Q1 = 2N4403
R1 = 680
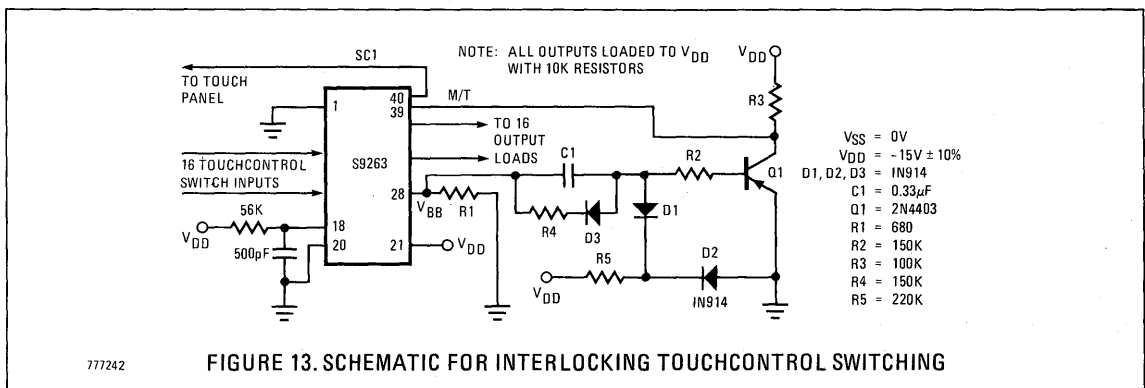R2 = 150K
R3 = 100K
R4 = 150K
R5 = 220K

777242   FIGURE 13. SCHEMATIC FOR INTERLOCKING TOUCHCONTROL SWITCHING

If, instead of mechanical switches, logic levels are to be used to operate the TouchControl I inputs, the mechanical switch can be directly replaced by a transmission gate. The logic level output would then be connected to the control pin of the transmission gate.

INTERLOCKING FEATURE

A feature that is desirable for a number of TouchControl applications is interlocking. As defined here, interlocking is a mode of keyboard operation in which any previously latched output is cancelled whenever a new output is selected. A typical example of this would be a TV channel selector; only a single channel would be selected at a time, and when a new channel is selected, the previously selected channel would be cancelled.

The schematic in Figure 13 shows an easy method for obtaining this interlock feature. This circuit takes advantage of the fact that each time a new output is selected, more current is drawn on the V_{BB} supply input. The current is sensed, and a pulse is sent to the M/T input, placing the device temporarily in the momentary mode. This cancels all previously latched outputs, while retaining the newly selected output. When the M/T input returns to its normal logic 1 level (V_{DD}), the device

returns to the Toggle mode, latching only the newly selected output.

Referring to the schematic, resistor R1 is selected so as to cause a voltage drop of 1 volt whenever an output turns on. This voltage drop causes transistor Q1 to turn on, placing the device in the momentary mode and cancelling any previously latched outputs.

Referring again to the schematic diagram, D1 and R5 are used to obtain a -0.6 volt bias voltage that allows D1 to hold Q1's base bias slightly negative. This enables R1 to be small enough so that V_{BB} drops only 1 volt when an output is selected. Components D3 and R4 prevent more than one output from being latched simultaneously.

This method for interlocking TouchControl switches is effective and inexpensive. It should be noted that it is applicable only on the non-multiplexed devices and that the output voltage levels will be decreased by 1 volt, but for most cases this approach represents an easy way to implement a desirable feature.

Figure 15 shows a scheme for obtaining the interlocking feature with the S9266. Output information is latched in five CMOS latches. Whenever a new key is touched, the AK output provides a pulse to unlatch the previously latched condition. The "B" outputs latch on the newly selected output condition.
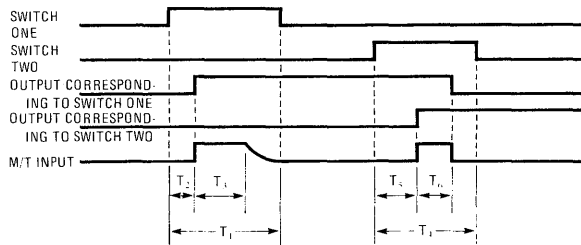
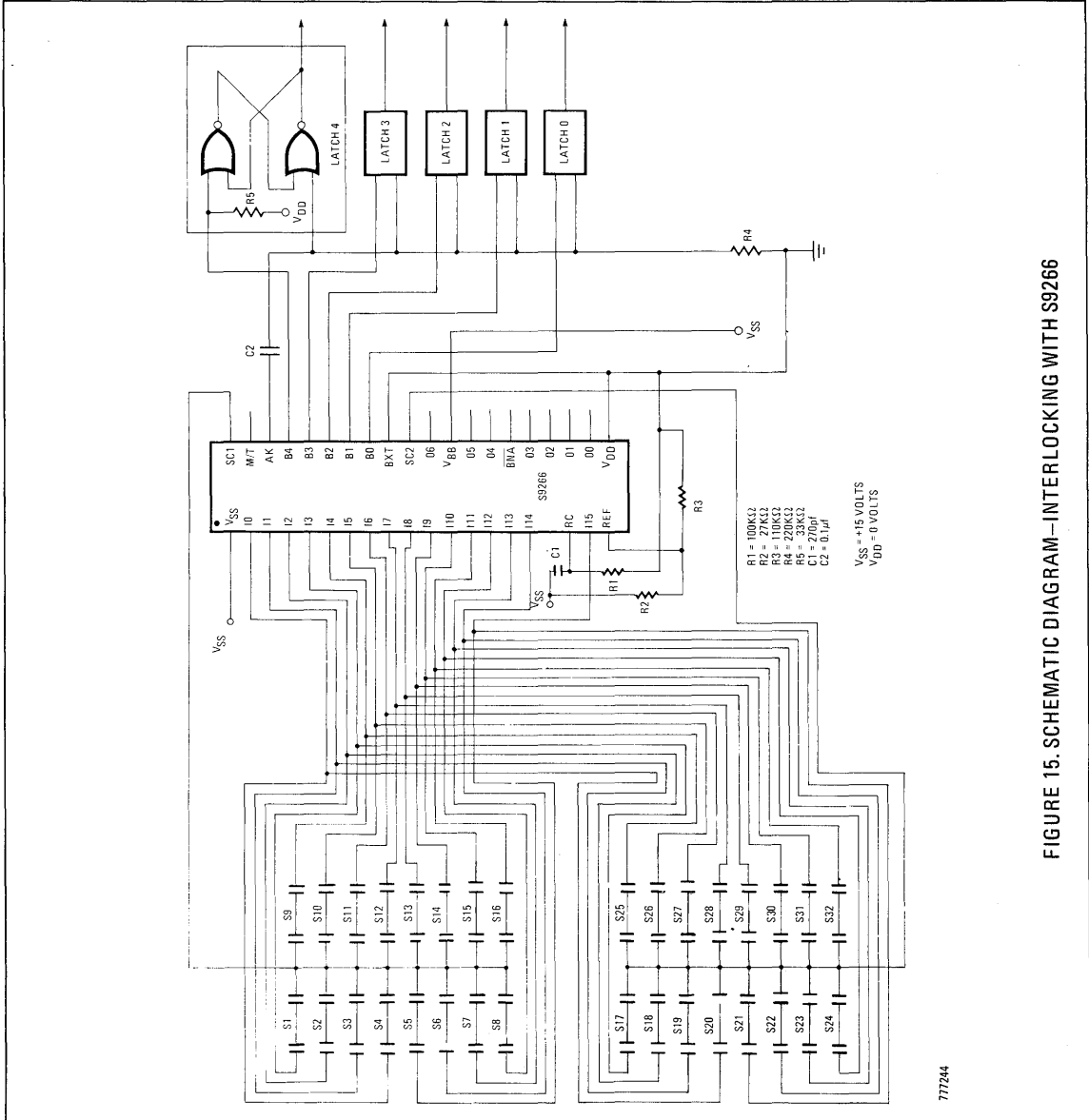

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FIGURE 14. INTERLOCK TIMING DIAGRAM

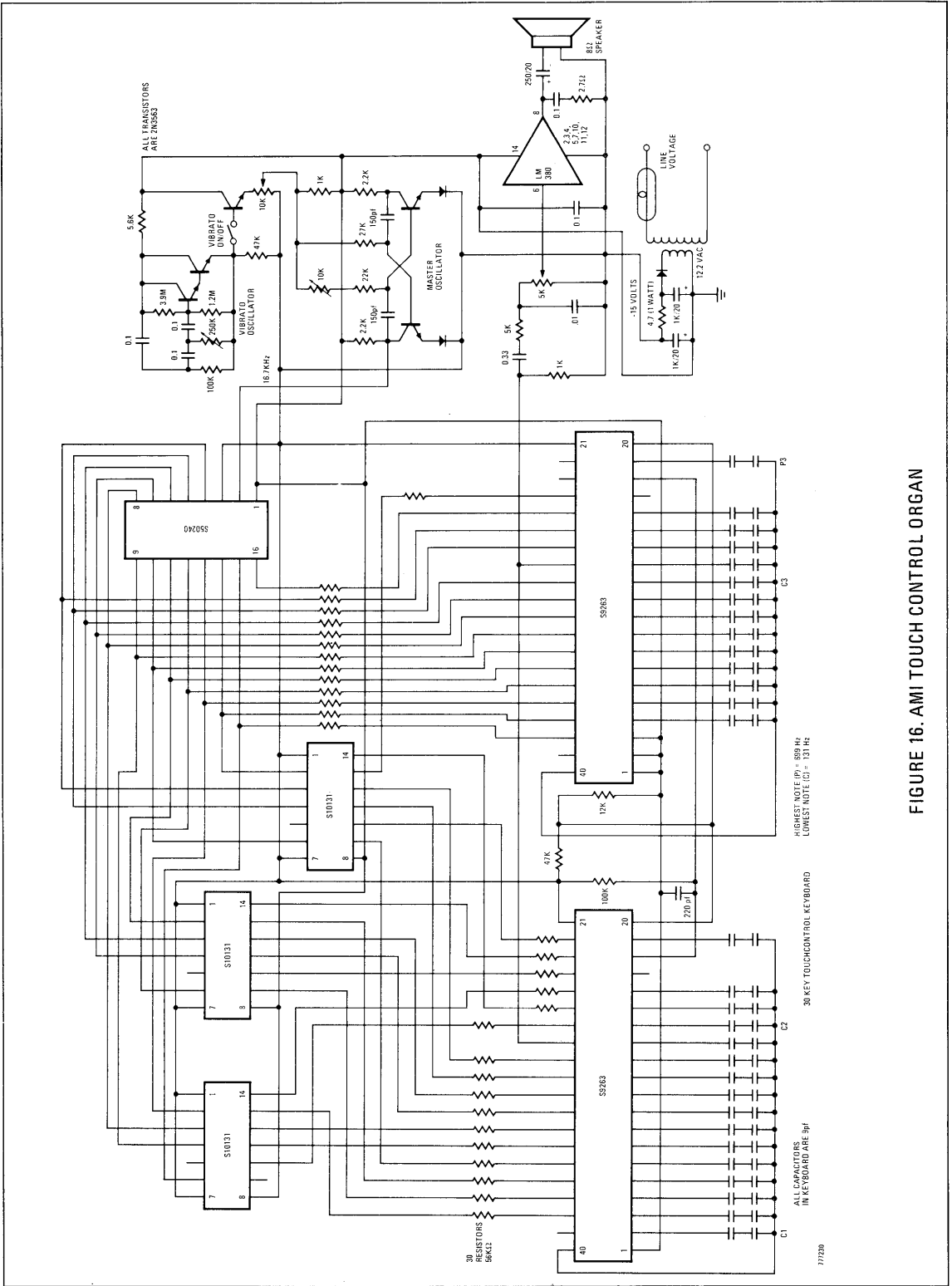FIGURE 15. SCHEMATIC DIAGRAM—INTERLOCKING WITH S9266

R1 = 100KΩ
R2 = 27KΩ
R3 = 110KΩ
R4 = 220KΩ
R5 = 33KΩ
C1 = 270pf
C2 = 0.1μf

V_{SS} = +15 VOLTS
V_{DD} = 0 VOLTS

777244

FIGURE 16. AMI TOUCH CONTROL ORGAN