AMI
A Subsidiary of Gould Inc.

1984 MOS Products Catalog

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Introduction

American Microsystems, Inc. (AMI) headquartered in Santa Clara, California is the semiconductor industry leader in the design and manufacture of custom MOS/VLSI (metal-oxide-silicon very-large-scale-integrated) circuits. It manufactures special circuits for the leading computer manufacturers, telecommunications companies, automobile manufacturers and consumer product companies worldwide. AMI is a wholly owned subsidiary of Gould, Inc.

Along with being the leading designer of custom VLSI, AMI is a major alternate source for the S6800 8-bit microprocessor family and the only alternate source for the S9900 16-bit family of microprocessors. AMI is also an alternate source for the 4-bit 7500 and the 8-bit 7800 series of single chip microcomputers. The company provides the market with selected low power CMOS Static RAMs, and 8K, 16K, 32K, 64K and 128K ROMs for all JEDEC pinouts or as EPROM replacements.

The most experienced designer of systems-oriented MOS/VLSI communication circuits, AMI provides components for station equipment, PABX and Central Office Switching systems, data communications and advanced signal processing applications.

AMI is a leading innovator in combining digital and analog circuitry on a single silicon chip, and is a recognized leader in switched capacitor filter technology.

Processing technologies range from the mature PMOS metal gate, to silicon gate N-Channel to the advanced, small geometry, high performance silicon gate CMOS. Over 25 variations are available.

Headquartered in Santa Clara, California, AMI has design centers in Santa Clara; Pocatello, Idaho; and Swindon, England. Wafer fabricating plants are in Santa Clara and Pocatello, and assembly facilities are in Seoul, Korea and the Philippines. A joint venture company in Graz, Austria will include complete design and manufacturing facilities.

Field sales offices are located throughout the United States, in Europe and in the Far East. Their listing, plus those of domestic and international representatives and distributors appear on pages B.31 through B.34 of this publication.

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Cross Reference Guide

Communication Products

Cross Reference by Manufacturer

Manufacturer	Part Number	AMI Functional Equivalent Part
G.I.	SPR 128	3630
G.I.	ACF 7310,12,7410	3526
G.I.	ACF 7323C	3525
G.I.	ACF 7363C	3525
G.I.	ACF 7383C	3525
G.I.	AY5-9100	2560A
G.I.	AY5-9151	2560A
G.I.	AY5-9152	2560A
G.I.	AY5-9153	2560A
G.I.	AY5-9154	2560A
G.I.	AY5-9158	2560A
G.I.	AY5-9200	2562/2563
G.I.	AY3-9400	2559
G.I.	AY3-9401	2559
G.I.	AY3-9410	2559
G.I.	AY5-9800	3525
G.I.	AY3-9900	3501/3502
Hitachi	HD 44211	3507
Hitachi	HD 44231	3506
Intel	2364	3630
Intel	2910/2912	3501/2
Intel	2913	3507
Intel	2914	3507
Intersil	ICM 7206	2559
Mitel	MT 4320	3525
Mitel	ML 8204	2561A
Mitel	ML 8205	2561A
Mitel	MT 8865	3525
Mostek	MK 5087	2559E
Mostek	MK 5089	25089
Mostek	MK 50981	2560A

Manufacturer	Part Number	AMI Functional Equivalent Part
Mostek	MK 50982	2560A
Mostek	MK 50991	2560A
Mostek	MK 50992	2560A
Mostek	MK 5116	3501/3502, 3507
Mostek	MK 5151	3501/3502, 3507
Mostek	MK 5156	3503/3504, 3506
Mostek	MK 5170	2562/2563
Mostek	MK 5175	25610
Mostek	MK 5387	2559
Mostek	MK 5389	25089
Motorola	MC 14400	3507
Motorola	MC 14401	3507
Motorola	MC 14402	3507
Motorola	MC 14406	3501/3502
Motorola	MC 14408	2560A
Motorola	MC 14409	2560A
National	MM 5393	2560A
National	MM 5395	2559
NEC	μPD 7720	2811
Nitron	NC 320	2560A
OKI	MSM 38128	3630
Phillips	TDA 1077	2559
RCA	CD 22859	2559
SSI	SSI 201	3525
Siliconix	DF 320	2560A
Siliconix	DF 321	2560A
Siliconix	DF 322	2560A
Siliconix	DF 341	3501/3502
Siliconix	DF 342	3501/3502
Supertex	CM 1310	3630

Communication Products

Cross Reference by Part Number

Manufacturer	Part Number	AMI Functional Equivalent Part
TDA 1077	Phillips	2559
SPR 128	G.I.	3630
CM 1310	Supertex	3630
MC 14400	Motorola	3507
MC 14401	Motorola	3507
MC 14402	Motorola	3507
MC 14406	Motorola	3501/3502
MC 14408	Motorola	2560A
MC 14409	Motorola	2560A
SSI 201	SSI	3525
CD 22859	RCA	2559
2364	Intel	3630
2910/2912	Intel	3501/2
2913	Intel	3507
2914	Intel	3507
DF 320	Siliconix	2560A
NC 320	Nitron	2560A
DF 321	Siliconix	2560A
DF 322	Siliconix	2560A
DF 328	Siliconix	2560A
DF 341	Siliconix	3501/3502
DF 342	Siliconix	3501/3502
MSM 38128	OKI	3630
MT 4320	Mitel	3525
HD 44211	Hitachi	3507
HD 44231	Hitachi	3506
MK 5087	Mostek	2559E
MK 5089	Mostek	25089
MK 50981	Mostek	2560A
MK 50982	Mostek	2560A
MK 50991	Mostek	2560A

Manufacturer	Part Number	AMI Functional Equivalent Part
MK 50992	Mostek	2560A
MK 5116	Mostek	3501/3502, 3507
MK 5151	Mostek	3501/3502, 3507
MK 5156	Mostek	3503/3504, 3506
MK 5170	Mostek	2562/2563
MK 5175	Mostek	25610
MK 5387	Mostek	2559
MK 5389	Mostek	25089
MM 5393	National	2560A
MM 5395	National	2559
ICM 7206	Intersil	2559
ACF 7310,12,7410	G.I.	3526
ACF 7323C	G.I.	3525
ACF 7363C	G.I.	3525
ACF 7383C	G.I.	3525
μPD 7720	NEC	2811
ML 8204	Mitel	2561A
ML 8205	Mitel	2561A
MT 8865	Mitel	3525
AY5 9100	G.I.	2560A
AY5 9151	G.I.	2560A
AY5 9152	G.I.	2560A
AY5 9153	G.I.	2560A
AY5 9154	G.I.	2560A
AY5 9158	G.I.	2560A
AY5 9200	G.I.	2562/2563
AY3 9400	G.I.	2559
AY3 9401	G.I.	2559
AY3 9410	G.I.	2559
AY5 9800	G.I.	3525
AY3 9900	G.I.	3501/3502

Cross Reference Guide

Memory Products

CMOS RAMs

Vendor	256 × 4	1K × 1	1K × 4	4K × 1
AMI	S5101		S6514	
FUJITSU	—	—	6514/8414	8404
HARRIS	6561	6508	6514	6504
HITACHI	435101	—	4334	4315
INTERSIL	6551	6508	6514	6504
MOTOROLA	145101	146508	—	146504
NATIONAL	74C920	74C929	6514	6504
NEC	5101	6508	444/6514	—
OKI	573	574	5115	—
RCA	5101	1821	1825	5104
SSS	5101	5102	—	—
TOSHIBA	5101	5508	5514	5504

BYTE WIDE NMOS ROMs

Vendor	2K × 8	4K × 8	4K × 8*	8K × 8-24 Pin	8K × 8-28 Pin	16K × 8	32K × 8
AMI	S68A316	S68A332	S2333	S68A364	S2364A	S23128A	S23256B
AMD	AM9218	9232	9233	AM9264	AM9265	AM92128	
NEC/EA	μPD2316	μPD2332A	μPD2332B	μPD8364	μPD2364	μPD23128	μPD23256
FAIRCHILD	F68316	F3532	F3533	F3564			
FUJITSU							
GI	RO3-9316		RO3-9333	RO3-9364	RO3-9365	SPR-128	
GTE	2316	2332		2364			
MOS				MPS2364			
MOSTEK	MK34000			MK36000	MK37000		MK38000
MOTOROLA	MCM68A316	MCM68A332		MCM68365			MCM65256
SIGNETICS	2616	2632		2664A	2664AM	23128	23256
SYNERTEK	SY2316	SY2332	SY2333	SY2364	SY2365	SY23128	SY23256
OKI	MSM2916						
ROCKWELL	R2316	R2332		R2364A	R2364B		
SGS	M2316						
TOSHIBA	TSU2316		TSU333-2				
NATIONAL		MM52132		MM52164			
VTI		VT2332	VT2333		VT2365A	VT23129	VT23256

*Pin compatible with 2732 EPROM

DEVICE	DESCRIPTION	"A" 1.5MHz VERSION	"B" 2.0MHz VERSION	0 – 70°C	–40/+85°C 1MHz	ROM PROGRAMMABLE	REPLACES
S1602	UART (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER)			P C D	P C D		S1883, MB8868A, AY-5-1013, AY-3-1015, TR1863, TR1602, TMS6011, NATIONAL 5303, SMC2502
S2350	USRT (UNIVERSAL SYNCHRONOUS RECEIVER/TRANSMITTER)			P C D	P C D		
S6800	MPU (MICROPROCESSOR)	X	X	P C D	P C D		MC6800, HD46800D, F6800
S6801	8-BIT MICROCOMPUTER 2K ROM, 128 BYTES RAM, UART, TIMER, I/O			P C D	C D	X	MC6801, HD6801X
S6802	8-BIT MICROPROCESSOR WITH CLOCK AND 128 BYTES RAM	X	X	P C	P C		MC6802, HD46802, F6802
S6803	S6801 WITHOUT ROM			P C D	C		MC6803
S6803NR	S6803 WITHOUT RAM			P C D	C		MC6803NR
S6805	8-BIT MICROCOMPUTER WITH 1.1K BYTES ROM, 64 BYTES RAM, TIMER, I/O			P C D	P C D	X	MC6805P2, HD6805S
S6808	MICROPROCESSOR AND CLOCK	X	X	P C	P C		MC6808, HD46808, F6808
S6809	ENHANCED 8-BIT MPU	X	X	P C D	P C D		MC6809, HD6809, F6809E
S6809E	ENHANCED 8-BIT MPU EXTERNAL CLOCK INPUT			P C D	P C D		MC6809E, HD6809E, F6809E
S6810	RAM (128x8)	X	X	P C D	P C D		MC6810, HD46810, F6810
S6810-1	RAM LOW COST (575ns)			P C D	P C D		
S6821	PIA	X	X	P C D	P C D		MC6821, HD46821, F6821, SY6520
S6840	TIMER	X	X	P C D	P C D		MC6840, HD46840, F6840
S6846	ROM, I/O, TIMER	X	X	P C D	P C D	X	MC6846, HD46846, F6846
S6850	ACIA	X	X	P C D	P C D		MC6850, HD46850, F6850
S6852	SSDA	X	X	P C D	P C D		MC6852, HD46852, F6852
S6854	ADLC	X	X	P C D	P C D		MC6854, HD46854, F6854
S68045	CRT CONTROLLER	X	X	P C D	P C D	X	MC6845, HD46505, SY6545
S6551/6551A	ACIA/BAUD RATE GENERATOR		X	P C D	P C D		SY6551, ROCKWELL 6551
S9900	16-BIT MICROPROCESSOR			P C			TMS9900
S9980A	16-BIT μPROCESSOR—8-BIT DATA BUS			P C D			TMS9980A
S9901	PCI			P C D			TMS9901
S9902	ACC			P C D			TMS9902

PART NUMBER CONVENTIONS

S = AMI PRODUCT PREFIX
68 = FAMILY DESIGNATION
A = BUS SPEED (OPTIONAL)
NONE — 1MHz
A = 1.5MHz
B = 2.0MHz

00 = PART DESIGNATION
I = QUALIFIER (OPTIONAL)
NONE 0—70°C
I —40/+85°C

P = PACKAGE TYPE
P = PLASTIC
C = CERAMIC
D = CERDIP

☒ = AVAILABLE ☐ = NOT AVAILABLE OR NOT APPLICABLE

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SEMI-CUSTOM

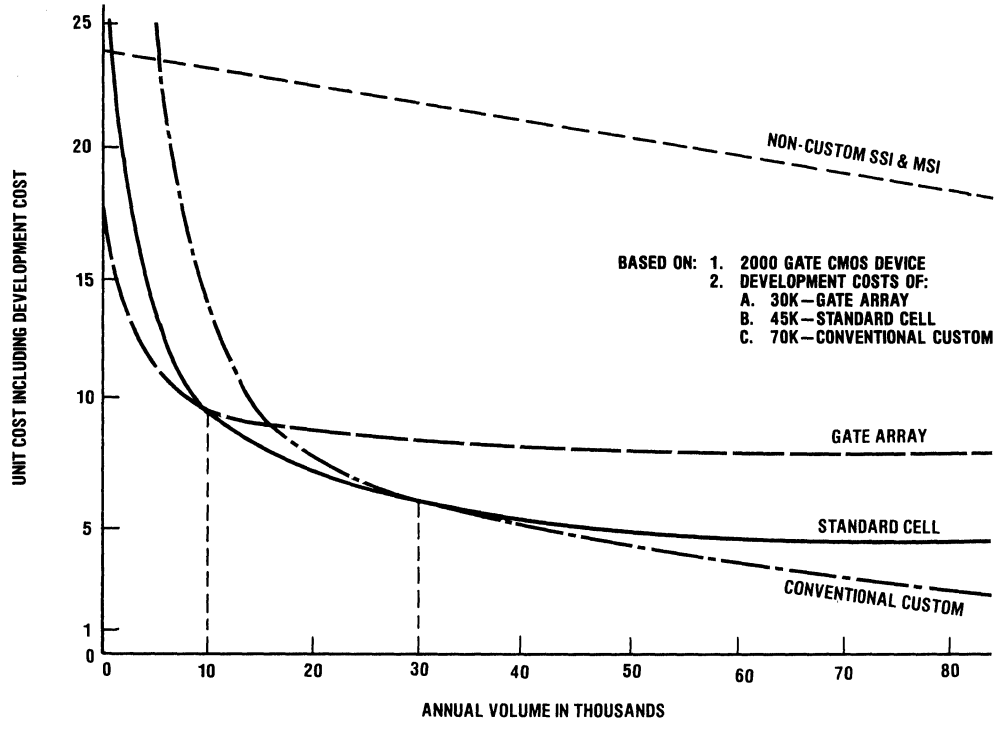
Semi-Custom Capabilities

Semi-Custom Capabilities

I. Introduction

As the semiconductor industry has marched into the new era of VLSI, a new market has appeared—fast turn custom or, as it is now called, semi-custom. AMI, a leader in custom MOS since 1966, is also a leader in this new semi-custom market. AMI has introduced CAE software and hardware tools to allow customers to design, simulate, and layout circuits using AMI gate array and standard cell families. Figure 1 shows the economic tradeoffs between gate array, standard cell, and full custom, all of which are offered by AMI.

Figure 1. Cost vs. Volume Alternatives



The simplest semi-custom ICs are gate arrays. As the name implies, a gate array consists of uncommitted component matrices of transistors (usually P- and N-type for CMOS) that allow user-defined interconnections through a single or double layer of metal. Since arrays employ fixed component locations and geometries, AMI can process the wafers up to the metallization stage and inventory the wafers for future customization. Thus gate arrays look like late mask programmable ROMs and benefit from this large-volume production because they appear to be a standard product. Thus AMI can offer them at an economical price and with fast prototyping and production turn on spans.

The second semi-custom product group is standard cells. Standard cells employ fully customized process/mask sets and must pass through all process steps before a user-specified circuit is completed. To design such chips, AMI customers use precharacterized functional cells from AMI cell libraries. Placing and routing the cells is done on AMI computers using specially developed software. Standard cell designs usually result in smaller chips since only the component structures required for the user specified circuit are included, thus chips designed with cells are less expensive than gate array designed chips.

Semi-Custom Capabilities

The key to success in this new market is flexibility. Flexibility to the user entails: low risk circuit implementation, short development span, lower development cost, lower piece part cost (over TTL implementations), easy to change or modify, enhanced product features, etc. For the manufacturer, flexibility means: ease of manufacture, economies of scale, and easy interface with customers. One last point: AMI offers the user the opportunity to migrate at a low cost, from a gate array to a standard cell (or possibly full custom) to further enhance his/her product. By using analog cells, significant advances in chip function integration are at the user's disposal.

In addition, AMI offers a wide selection of packages to meet specific user needs. AMI offers the CAE tools needed to work in the new market. AMI also offers the training required to move customers quickly and easily into this new technology. See the appropriate sections in this catalog for more details.

2 Micron Products

AMI is developing 2 micron CMOS technology to support the next generation of semi-custom products, in both gate arrays and standard cells. These products will offer size and performance improvements of up to 50% from their 3 micron counterparts.

Introduction of the first 2 micron gate array family is planned for second quarter 1984 and is expected to offer capabilities of greater than 8000 gates.

II. Gate Arrays

Features

- Arrays of Uncommitted CMOS Transistors Programmed by Metal Layer Interconnect to Implement Arbitrary Digital Logic Functions
- Multiple Developmental Interfaces: AMI or Customer Designed
- Three Array Families—5-Micron Single Metal CMOS, 3-Micron Single Metal CMOS, and 3-Micron Double Metal Versions
- Multiple Array Configurations—From 300 to 1260 Gates for 5-Micron Devices, and 500 to 5000 Gates for 3-Micron Devices
- Quick Turn Prototypes and Short Production Turn-On Time
- Economical Semi-Custom Approach for Low-to-Medium Production Volume Requirements
- Advanced Oxide-Isolated Silicon Gate CMOS Technology
- High Performance—2 to 3ns Typical Gate Delay for 3-Micron Devices
- Broad Power Supply Range—3V to 12V (± 10%)
- TTL or CMOS Compatible I/O
- Up to 134 I/O Connections
- Numerous Package Options
- Full Military Temperature Range (−55°C to 125°C) and MIL-STD-883 Class B Screening Available

General Description

AMI's gate array products consist of arrays of CMOS devices whose interconnections are initially unspecified. By "programming" interconnect at the metal layer mask level, virtually arbitrary configurations of digital logic can be realized in an LSI implementation.

AMI gate array designs are based on topological cells—i.e., groups of uncommitted silicon-gate N-Channel and P-Channel transistors—that are placed at regular intervals along the X and Y axes of the chip with intervening polysilicon underpasses. Pads, input protection circuitry, and uncommitted output drivers are placed around the periphery.

Compared to SSI/MSI logic implementations, AMI's gate array approach offers lower system cost and, in addition, all the benefits of CMOS LSI. The lower system cost is due to significant reductions in component count, board area and power consumption. Product reliability, a strong function of component count, is thereby greatly enhanced. And compared to fully custom LSI circuits, the gate array offers several advantages: low development cost; shorter development time; shorter production turn-on time; and low unit costs for small to moderate production volumes.

AMI's CMOS gate arrays are offered in three families: the 5-micron UA series, the 3-micron single metal GA series, and the 3-micron double metal GA-D series. The 5-micron UA series has been in production since 1980 and well over one hundred circuits have been produced in that technology. The 3-micron GA and GA-D series are the high-speed high-density devices fabricated in AMI's state-of-the-art 3-micron CMOS processes.

Table 1. Five-Micron Gate Array Family

Circuit	Equivalent Two-Input Gates	Pads	LS Output Drivers	TTL Output Drivers
UA-1	300	40	17	20
UA-2	400	46	23	20
UA-3	540	52	25	24
UA-4	770	62	31	28
UA-5	1000	70	35	32
UA-6	1260	78	39	36

Five-Micron Gate Array Family

The family of 5-micron CMOS products is offered in six configurations, summarized in Table I, with circuit complexities equivalent to 300, 400, 540, 770, 1000, and 1260 two-input gates, respectively. All pads can be individually configured as inputs, outputs, or I/O's. Input switching characteristics can be programmed for either CMOS or TTL compatibility. LS buffer output drivers will support CMOS levels of two low power schottky TTL loads. TTL buffer outputs will also provide CMOS levels and are capable of driving up to six LS TTL loads. All output drivers can be programmed for tri-state or open drain (open collector) operation as required.

The CMOS technology used for these products is AMI's state-of-the-art 5-micron, oxide-isolated, silicon gate CMOS process. This process offers all the conventional advantages of CMOS—i.e., very low power consumption, broad power supply voltage range (3V to 12V ± 10%), and high noise immunity—as well as dense circuits with high performance. Gate propagation delays are in the five to ten ns range for 5 volt operation at room temperature. AMI gate array products can be supplied in versions intended for operation over the standard commercial temperature range (0°C to +70°C), the industrial range (−40°C to +85°C), or the full military range (−55°C to +125°C). MIL-STD-883 Class B screening, including internal visual inspection and

high temperature burn-in, is offered. Similarly, customer-specified high reliability screening is available for commercial and industrial applications.

D.C. characteristics for the 5 micron gate array family are summarized in Table 2.

Table 2

Logic Element	2-Input Gate Equivalent
2-Input NOR	1
2-Input NAND	1
3-Input NOR	1.5
3-Input NAND	1.5
INVERTER	.5
D FLIP-FLOP W/RESET	5
D FLIP-FLOP W/SET-RESET	6
J-K FLIP-FLOP	8
CLOCKED LATCH	2.5
EXCLUSIVE OR	2.5
SCHMITT TRIGGER	2
4-BIT BCD CNTR W/RESET	27
TRANSMISSION GATE	.5

The current AMI array family, 300 gates to 1260 gates, is run in a 3-12V CMOS process (internally coded as CVA process). AMI is currently optimizing this array family for 3V to 5V operation (internally coded as CVH process). This new family, called UA-300 through UA-1260, is be functionally identical to the existing UA-1 through UA-6. All design tools are interchangeable.

Customers who require 3V to 5V operation will be able to use the CVH family now. This optimized process will result in a 25-50% performance enhancement for 5V gate array designs. Customers who require operating voltages greater than 5V will continue to use the UA-1 to UA-6 CVA family.

In conjunction with these arrays, AMI has developed a set of "functional overlays." These are basic logic element building blocks—e.g. two input and larger gates of various types, flip-flops, and so forth—from which complete logic designs can be developed. Each functional overlay corresponds to a metal interconnect pattern that is superimposed on a set of uncommitted transistors (and polysilicon underpasses) in the array to implement the the logic element. Typical functional overlay logic elements and the number of two-input gate equivalents they utilize are shown in Table 3.

Currently over 75 functional cells exist for this family.

Three-Micron Gate Array Family

As part of AMI's long range semi-custom strategy in MOS/VLSI, AMI will continue to introduce new gate array products. These new products will offer performance and cost advantages not currently realizable. In conjunction with these new array products, AMI has introduced computer-aided design tools to automate the entire gate array design process.

The newest gate array family is the high-performance GA and GA-D series which is based on AMI's 3-micron CMOS silicon gate process technology. With a 3-micron drawn geometry, it is equivalent to a 2-micron effective channel length which is the state-of-the-art.

The AMI GA and GA-D series are designed for 5V operation over military temperature range (−55 to 125°C). Besides high speed (2 to 3ns typical delay) and high density (up to 5K gates), it features total I/O flexibility in that each I/O pad can be one of any 13 options.

The single metal version provides up to 2500 gates and the double metal GA-D version 5000 gates. See Table 3 for configurations.

Table 3. Three-Micron Gate Array Family

Process	Product No.	Gates	Pads
Single Metal	GA-2500	2500	84
	GA-2000	2025	74
	GA-1500	1500	64
	GA-1000	1020	52
	GA-500	540	40
Double Metal	GA-5000D	4995	134
	GA-4000D	4012	120
	GA-3000D	3080	102
	GA-2000D	2016	84
	GA-1000D	1024	64

In conjunction with these new array products, AMI will have a complete powerful set of design automation software to allow users complete design flexibility. Using a terminal tied to a central AMI owned or customer owned minicomputer or mainframe, the user will have access to a complete set of design automation software tools including:

- Schematic digitization and capture
- Logic simulation
- Circuit simulation
- Test vector generation
- Interactive or autoplace and route
- Auto continuity checking

These tools will allow the user to partially or fully automate the design task for maximum flexibility.

Customer Interface

AMI can interface with a user at one of three input levels: logic, layout or PG tape. At the logic level, AMI will customize and develop the metal interconnect pattern from the user's logic diagram. This is known as the AMI-Designed interface.

Semi-Custom Capabilities

For programs involving multiple gate array patterns from customers with suitable MOS design and layout experience, AMI will also support arrangements in which the customer designs the metal interconnect patterns and furnishes AMI with corresponding composite layout or metal mask PG tapes to AMI specification. This is known as the Customer-Designed Interface. To support this interface, AMI will provide the users with the CAD package plus training.

Packages

Pinout or lead count varies with die size and array complexity. The arrays are offered in standard plastic and ceramic dual-in-line packages with pin counts ranging from 16 to 64, JEDEC-Standard leadless and leaded chip carriers, miniflat packs to 84 pins, and pin grid arrays to 120 pins. AMI gate array products are also available in wafer or unpackaged die form.

5-Micron Gate Array Series

DC Characteristics—TTL Interface

Specified @ $V_{DD} = +5V \pm 10\%$; $V_{SS} = 0$; Temperature = $-55°C$ to $+125°C$

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	V
V_{IL}	Input Low Voltage	0.0		0.8	V
V_{OH}	Output High Voltage (LS Buffer $I_{OH} = -700\mu A$) (T Buffer $I_{OH} = -1.5mA$)	2.7 2.4			V V
V_{OL}	Output Low Voltage (T Buffer $V_{OL} = 2.4mA$) (LS Buffer $I_{OL} = 0.8mA$)			0.4 0.4	V V
I_{OZ}	3-State Output Leakage $V_O = 0$ or V_{DD}	−10	1	10	μA

DC Characteristics—CMOS Interface

Sym.	Parameter	V_{DD}	Limits *T Low Min	*T Low Max	25°C Min	25°C Typ	25°C Max	*T High Min	*T High Max	Units	Condition
I_{DD}	Quiescent Device Current	5V 10V		0.1 0.2		.001 .002	0.1 0.2		1 2	μA/gate μA/gate	$V_{IN} = 0$ or V_{DD}
V_{OL}	Low Level Output Voltage			0.05			0.05		0.05	V	$I_O = 1\mu A$
V_{OH}	High Level Output Voltage	5V 10V	4.95 9.95		4.95 9.95			4.95 9.95		V V	$I_O = -1\mu A$
V_{IL}	Input Low Voltage	5V 10V	0.0 0.0	1.5 3.0	0.0 0.0		1.5 3.0	0.0 0.0	1.5 3.0	V V	
V_{IH}	Input High Voltage	5V 10V	3.5 7.0	5.0 10.0	3.5 7.0		5.0 10.0	3.5 7.0	5.0 10.0	V V	
I_{OL}	Output Low (Sink) Current T Buffer LS Buffer	5V 10V 5V 10V	3.2 6.0 1.0 1.8		3.2 6.0 1.0 1.8	4.8 9.0 1.6 3.1		2.4 4.0 0.8 1.0		mA mA mA mA	$V_O = 0.4V$ $V_O = 0.5V$ $V_O = 0.4V$ $V_O = 0.5V$
I_{OH}	Output High (Source) Current T Buffer LS Buffer	5V 10V 5V 10V		−600 −1120 −300 −560			−600 −1120 −300 −560		−500 −940 −250 −470	μA μA μA μA	$V_O = 4.6V$ $V_O = 9.5V$ $V_O = 4.6V$ $V_O = 9.5V$
I_{IN}	Input Leakage Current			1			1		1	μA	$V_{IN} = 0$ or V_{DD}
I_{OZ}	3 State Output Leakage Current			±1			±1		±10	μA	$V_O = 0$ or V_{DD}
C_I	Input Capacitance					5				pF	Any Input

*Military temperature range is $-55°C$ to $+125°C$
Industrial temperature range is $-40°C$ to $+85°C$
Commercial temperature range is $0°C$ to $+70°C$

Absolute Maximum Ratings

Supply Voltage, V_{DD} ..... −.5V to +7V
Input Voltage, V_{IN} ..... −.5V to V_{DD} +.5V
D.C. Input Current, I_I ..... ±10mA
Storage Temperature, T_{STG} ..... −65° to +150°C

3-Micron Gate Array Series

D.C. Electrical Characteristics: $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -55°$ to $+125°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{DD}	Quiescent Supply Current		10	50	μA	$V_I = V_{DD}$ or V_{SS}
V_{OL}	Low Level Output Voltage			.05	V	$I_{OL} = 1\mu A$
				.4	V	$I_{OL} = 3.2mA$
V_{OH}	High Level Output Voltage	4.95			V	$I_{OH} = -1\mu A$
		2.40			V	$I_{OH} = -5mA$
V_{IL}	Low Level Input Voltage	−.5		.8	V	TTL Interface
		−.5		1.5	V	CMOS Interface
V_{IM}	High Level Input Voltage	2.0		V_{DD} +.5	V	TTL Interface
		3.5		V_{DD} +.5	V	CMOS Interface
I_{IN}	Input Leakage Current			1	μA	$V_{IN} = V_{DD}$
I_{OZ}	High Impedance Output Leakage Current	−10	.001	10	μA	$V_{OH} = V_{DD}$ or V_{SS}
C_{IN}	Input Capacitance		5		pF	Any Input

Table 4. Propagation Delay Characteristics for AMI Gate Arrays
A.C. Characteristics: $T_A = 25°C$, $V_{DD} = 4.5V$, F.O. = 2

Function		Gate Delays 5μ	Gate Delays 3μ S.M.	Gate Delays 3μ D.M.	Units
INVERTER	L-H	6.0	4.5	3.4	ns
	H-L	5.3	1.3	1.0	ns
2INPUT NAND	L-H	9.0	5.8	4.4	ns
	H-L	9.0	1.8	1.4	ns
2INPUT NOR	L-H	12.0	8.4	6.3	ns
	H-L	8.2	1.5	1.1	ns
D-TYPE F/F					
MAX FREQUENCY		15	36	45	MHz
TTL INPUT BUFFER		18	7	5	ns
OUTPUT BUFFER					
DELAY ($C_L = 30pF$)		20	9	6.7	ns

NOTE: BASED ON WORST CASE PROCESS PARAMETERS. FOR TYPICAL DATA, DIVIDE GATE DELAYS BY 1.8.

AMI®

A Subsidiary of Gould Inc.

HIGH PERFORMANCE GATE ARRAYS

3μ SILICON GATE CMOS TECHNOLOGY

Features

- ☐ Typical Delay: 2ns/gate
- ☐ Up to 5000 Equivalent 2-Input Gates
- ☐ Total I/O Flexibility
- ☐ 36 to 134 Pins Available
- ☐ Power Supply Range: 2.5V to 5V ± 10%
- ☐ Temperature Range: −55°C to 125°C
- ☐ TTL or CMOS Compatible I/O
- ☐ Input Protection Networks on All Pads
- ☐ High External/Internal Noise Immunity
- ☐ Virtually Latch-Up Free
- ☐ Fully Integrated Software Support

General Description

The GA-series of gate arrays are fabricated using state-of-the-art 3 micron, oxide-isolated, isoplanar, silicon-gate CMOS technology. This process, called CMOS-II, features effective channel lengths for P-and N-channel transistors of approximately 2 micro-meters, allowing circuit complexities of up to 5000 equivalent 2-input gates with typical propagation delays of 2ns.

Gate arrays are pre-designed and pre-fabricated silicon chips that contain matrices of uncommitted CMOS transistor pairs used to implement combinatorial and sequential logic functions by connecting the available components with a unique metal pattern tailored to satisfy user requirements. The number of customized masks is dependent on the number of metal layers used to interconnect the uncommitted devices on the array, and it affects the development and manufacturing costs since more engineering effort and lower yields are associated with multi-level metal personalization. As shown below, the GA-series of gate arrays comprises a single metal interconnect option with gate densities ranging from 500 to 2500 gates, and a double metal family with up to 5000 gates.

Table 1. 3μ Single Metal Family

Part No.	Eq. 2-Input Gates	Bonding Pads	Die Size (Mils)	*Typical Development Span (weeks)
GA-2500	2500	84	265 × 244	14
GA-2000	2025	74	245 × 219	12
GA-1500	1500	64	224 × 195	10
GA-1000	1020	52	199 × 166	8
GA-500	540	40	162 × 127	7

Table 2. 3μ Double Metal Family

Part No.	Eq. 2-Input Gates	Bonding Pads	Die Size (Mils)	*Typical Development Span (weeks)
GA-5000 D	4995	134	350^2	14
GA-4000 D	4012	120	320^2	12
GA-3000 D	3080	102	290^2	10
GA-2000 D	2070	84	260^2	8
GA-1000 D	1024	64	230^2	7

*Assumes customer supplies breadboard schematic, and device specifications

Peripheral Cells

They occupy the outermost area of the chip, and are used to interface with circuitry external to the array.

Figure 1 shows the topological layout of the peripheral cell for the GA-series of gate arrays. The criteria behind its design were to offer total flexibility in determining pin-out configurations, and to maximize the number of options associated with each bonding pad. The result is that each pin in the 3μ gate arrays can serve any of the following functions:

- ☐ TTL Output Driver
- ☐ LSTTL Output Driver
- ☐ CMOS Output Driver
- ☐ Open Drain Output
- ☐ Tri-State Output
- ☐ Bipolar, Emitter Follower Output
- ☐ Analog Switch
- ☐ TTL Input Buffer
- ☐ CMOS Input
- ☐ V_{DD} Supply
- ☐ V_{SS} Supply

Furthermore, the peripheral cell also contains high-impedance transistors that can be used as pull-ups or pull-downs if required.

Array Cells

In addition to the active components used in building the basic logic blocks, the core cells also contain the routing area for the customized metal pattern. Connecting the uncommitted P- and N-channel transistors to perform a specific logic function is facilitated by using predefined metal interconnect patterns called macros. An added advantage of using these macros is that their D.C. and A.C. characteristics are well known, thus allowing a more accurate prediction of the static and dynamic behavior of the finished part.

The GA-series of arrays is supported by a macro library, which in addition to the options associated with the peripheral cell allows the implementation of all the functions listed on Table 3.

Figure 1. Peripheral Cell Architecture

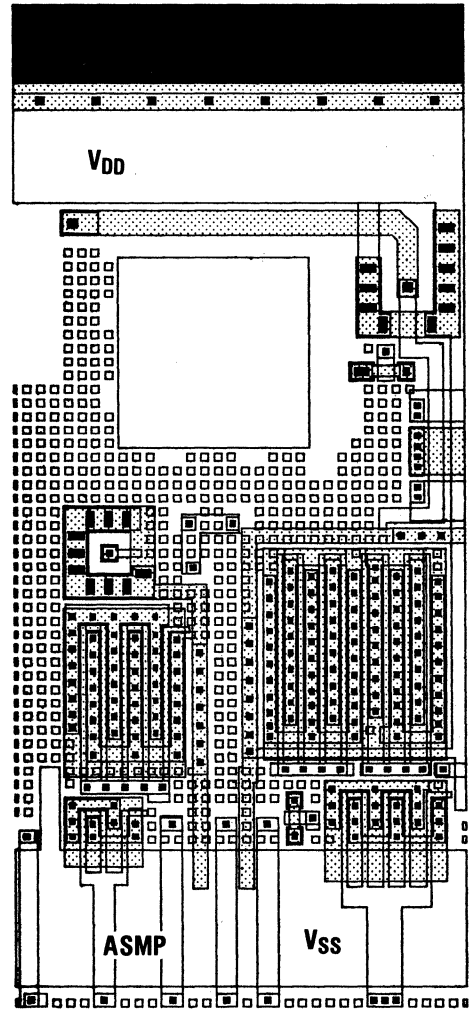
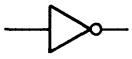
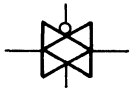
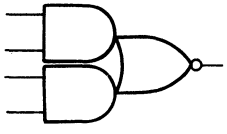
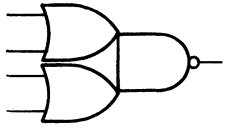
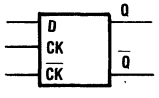
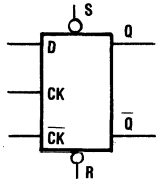


Table 3. 3μ Gate Arrays Macro Library

Logic Symbol	Logic Function	Eq. 2-Input Gates
	INVERTER	1/2
	TRANSFER GATE	1/2
	NAND	1/2 per input
	NOR	1/2 per Input
	EX-NOR	2-1/2
	EX-OR	2-1/2
	AND-OR-INVERT	2
	OR-AND-INVERT	2
	CLOCKED LATCH	2-1/2
	D-FLIP FLOP	5/6

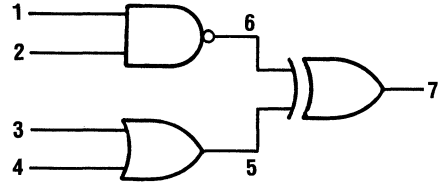
Software Support

AMI CAD Technology (ACT) is the most advanced integrated software package for CMOS/VLSI design available in the industry. It uses a common database for logic simulation, mask layout and test program generation. By operating from a common database, a gate array design can be converted into a standard cell or a fully crafted custom circuit with minimal risks.

The heart of the system is BOLT (Block Oriented Logic Translator) which is at the same time a hardware description language and a compiler. It allows the system designer to describe the logic network in a hierarchical fashion due to an unlimited macro nesting capability.

The common data base is created in a very simple fashion, consistent with the way that logic files are created in most timeshared logic simulators. Figure 2 shows a simple logic network and the corresponding BOLT file which allows programmability of rise and fall times for all gates.

Figure 2.




```
6 ° NAND   1  2 (TDR = XX, TDF = XX);
5 ° OR     3  4 (TDR = XX, TDF = XX);
7 ° EXOR   5  6 (TDR = XX, TDF = XX);
```

GLIDE is the graphics editor on Prime used for interactive design of the single metal families of arrays. TRACE is a module that checks the layout database for continuity, and COMPARE verifies that the layout matches the BOLT logic file.

GAPAR is the software module that allows automatic placement and routing of the double metal family of arrays. It is designed to complete at least 98% of the wiring connections on a 100% utilized array, based on a 90% confidence level using Donath-Heller-Milkhail two-dimensional model. The GAPAR system also offers interactive routing tools which can be used to complement the auto router when overflow conditions exist or to manually route critical delay paths.

CAPACITANCE calculates the actual capacitive load of the active gates from the layout database. The capacitance parameters are different for poly and metal interconnections, and for aluminum over diffusions or field oxide. In conjunction with DELAY, it allows to accurately predict the dynamic behavior of the actual integrated circuit before it is fabricated.

TESTGEN is used to generate efficiently compressed functional test patterns based on the results of logic simulations from SIMAD. This pattern compression minimizes the use of local memory on Sentry testers.

TESTPRO operates on Prime, allowing off-line generation of D.C. parametric tests in Factor language used in Fairchild test systems. Its output is merged with the compressed functional patterns from TESTGEN, and the result is a full dynamic test program that can be tailored for use in any Sentry tester.

Customer Interfaces

Unlike other gate-array vendors, AMI offers all the services required to develop and fabricate a semi-custom circuit. In-house capabilities include circuit and logic simulation, mask making, full wafer fabrication, assembly, and test.

Gate array developments are supported in two basic ways:

1) The **AMI-Tooled Interface** is available to customers with little or no experience in semi-custom circuit development, or to experienced users with limited in-house capabilities. In these cases AMI requires a logic diagram or breadboard schematic of the circuit to be integrated, along with D.C. and A.C. specifications, and functional patterns in I/O format.

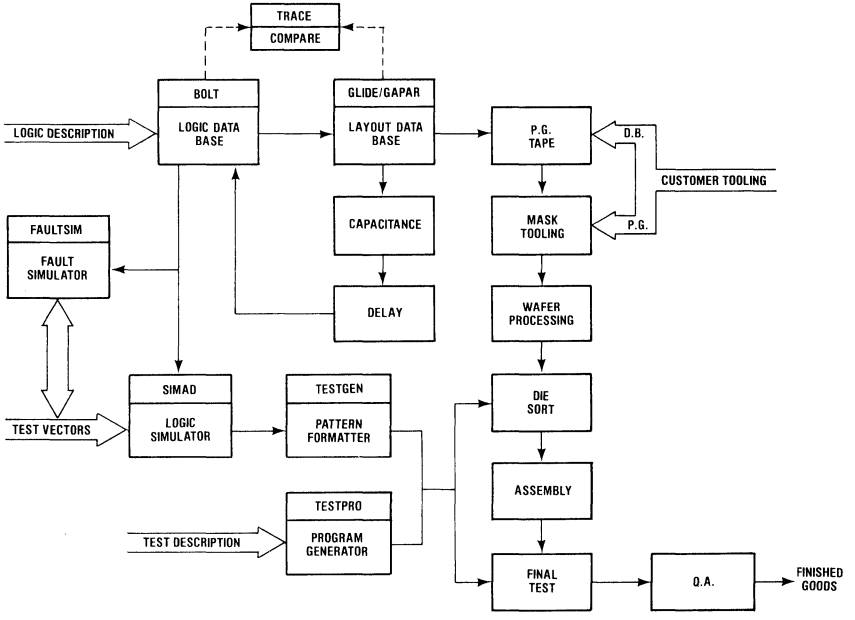
At the end of the development phase, the customer receives 25 fully tested prototypes, assembled in ceramic packages, which have been subjected to our stringent Q.A. screening requirements.

2) The **Customer-Tooled Interface** is more applicable to customers with multiple circuit development requirements and suitable in-house design capabilities. For these customers AMI will supply the necessary software tools which have been written in FORTRAN and PASCAL languages so they will be compatible not only with PRIME computers, as is presently the case, but also with VAX and IBM minis. The user in turn provides AMI with either a database tape in CALMA format, or an ELECTROMASK or DAVID MANN compatible pattern generator tape, along with test requirements. A debugged SENTRY program is preferred. AMI will then fabricate and test 25 prototypes which should be representative of the production units.

Development Phase

Figure 3 below shows the typical development flow for the GA-series of arrays. The only difference between the single and double metal families is the fact that the design for single metal patterns is interactive, rather than automated, and TRACE and COMPARE are used to match logic and layout data bases.

Figure 3. Typical Development Flow for GA-Series of Arrays



Packaging

The 3μ gate arrays are assembled in the broadest selection of packages available in the semiconductor industry. These include plastic and ceramic DIPs, leadless chip carriers, pin grid array or plug-in packages. AMI has also developed a family of plastic quad flat-packages which resemble a leaded chip carrier with 40-mil centers, and is ideal for consumer applications where high pin counts and low costs are required.

Table 4 shows a list of the package options for the GA-series of arrays with the range of presently available pins.

Table 4.

Package Type	Lead Counts
Plastic DIP	8 to 64
CERDIP	14 to 40
Ceramic DIP	14 to 64
Leadless Chip Carrier	20 to 84
Leaded Chip Carrier	18 to 68
Pin Grid Array	64 to 120

Under special conditions AMI gate arrays can be also purchased in wafer or die form if required.

Testing

Unless otherwise specified, all input and output D.C. parameters are tested to AMI standard specifications outlined in the table of Electrical Characteristics. Exceptions to this rule might be applicable in cases where output buffers are paralleled to provide more sourcing and sinking currents, or where the inputs or outputs interface with logic families other than TTL or CMOS.

In any case, prior to the start of any circuit development, the device specifications have to be approved and signed off by both the customer and AMI representatives. For circuits that do not require high-rel screening, each device is tested at the temperature extremes for commercial, industrial, and military applications. AMI testing capabilities are unparalleled in the industry, and Table 5 shows the different type of digital testers currently in production. As shown there, the dynamic behavior of any circuit can be verified up to a maximum frequency of 30MHz.

Table 5.

Test System	Function	Local Memory	Freq.	Pins
S-600	Digital	1K/Pin	5 MHz	60 I/O
S-II	Digital	2K/Pin	10 MHz	60 I/O
S-VII	Digital	4K/Pin	10 MHz	60 I/O
Sentinel	Digital	4K/Pin	10 MHz	60 I/O
GR-16	Digital	4K/Pin	30 MHz	96/144
		Future Systems		
Series 20	Digital	4K/Pin	20 MHz	120 I/O
GR-16	Digital	4K/Pin	30 MHz	144 I/O

Absolute Maximum Ratings

Supply Voltage, V_{DD} ..... $-.5V$ to $+7V$
Input Voltage, V_{IN} ..... $-.5V$ to $V_{DD} + .5V$
D.C. Input Current, I_I ..... $\pm 10mA$
Storage Temperature, T_{STG} ..... $-65°$ to $+150°C$

D.C. Electrical Characteristics: $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -55°$ to $+125°C$

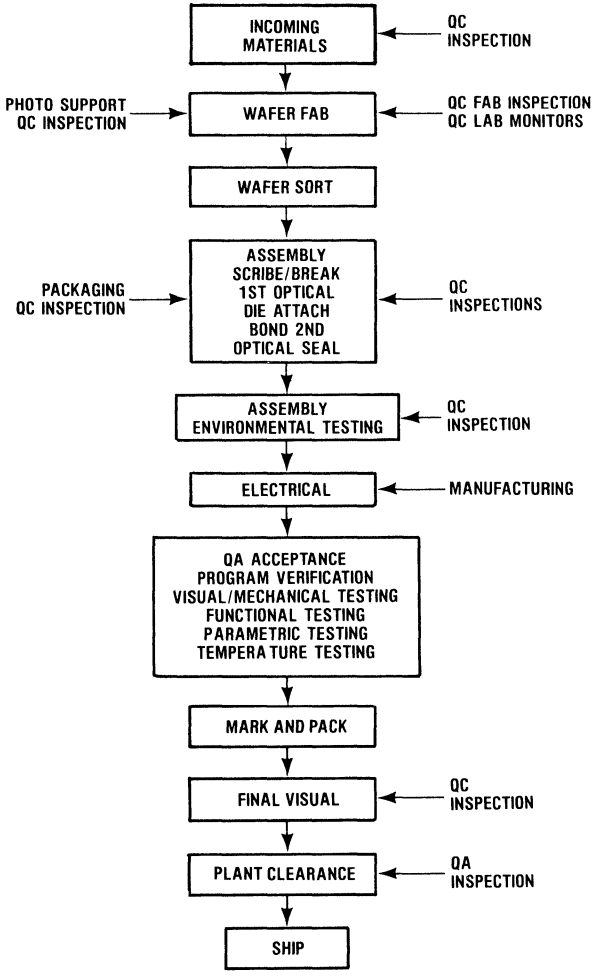
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{DD}	Quiescent Supply Current		10	50	μA	$V_I = V_{DD}$ or V_{SS}
V_{OL}	Low Level Output Voltage			.05	V	$I_{OL} = 1\mu A$
				.4	V	$I_{OL} = 3.2mA$
V_{OH}	High Level Output Voltage	4.95			V	$I_{OH} = -1\mu A$
		2.40			V	$I_{OH} = -5mA$
V_{IL}	Low Level Input Voltage	$-.5$		.8	V	TTL Interface
		$-.5$		1.5	V	CMOS Interface
V_{IM}	High Level Input Voltage	2.0		$V_{DD} + .5$	V	TTL Interface
		3.5		$V_{DD} + .5$	V	CMOS Interface
I_{IN}	Input Leakage Current			1	μA	$V_{IN} = V_{DD}$
I_{OZ}	High Impedance Output Leakage Current	-10	.001	10	μA	$V_{OH} = V_{DD}$ or V_{SS}
C_{IN}	Input Capacitance		5		pF	Any Input

Switching Characteristics: $V_{DD} = 4.5V$, $C_L = .2pF$

Logic Macro	Parameter	$T_A = 25°C$	$T_A = 70°C$	Units
Inverter	tpd	1.7	2.5	Ns
2-In NAND	tpd	2.5	4	Ns
D-Flip Flop	Max Frequency	40	25	MHz

$$tpd = \frac{t_{LH} + t_{HL}}{2}$$

AMI Product Assurance Flowchart



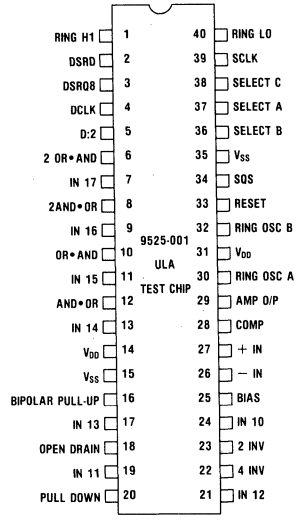
3μ CMOS Evaluation Kit

The 9525-001 and 9525-002 test chips are two different bonding options of the GA-2500 single metal array, patterned with test circuitry specifically designed to evaluate the 3μ gate array's A.C. and D.C. characteristics.

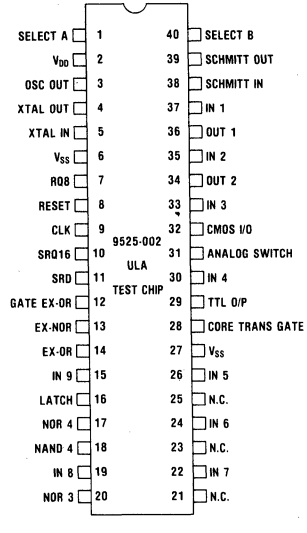
These test chips are available in small sample quantities and contain:

- ☐ Ring Oscillators
- ☐ 5-Bit Synchronous Counter
- ☐ 8-Bit Ripple Counter
- ☐ 16-Bit Static Shift Register
- ☐ 8-Bit Dynamic Register
- ☐ Schmitt Trigger Inputs
- ☐ Simple Operational Amplifier
- ☐ Interface Buffers

GA-2500 Test Chips



9525-001



9525-002

For more information on availability and functionality of these test devices, please contact your nearest AMI representative.

III. AMI's Standard Cell Program

Program Description

The cells in the Standard Cell Program are basic logic elements such as gates, flip-flops, register counter bits and I/O devices. Each cell has been previously designed and analyzed for performance. Complex digital functions can be rapidly implemented by interconnecting the various cells. Most cells have a series 4000 CMOS equivalent and a 74LS TTL equivalent for ease of breadboarding.

The cells are initially designed on an interactive color graphics terminal — AMI's SIDS (symbolic interactive design) system. The cell library is maintained within the SIDS data base. If other CAD (Computer-Aided Design) systems are used internally by a customer, the cell library can be digitized onto these systems.

Using the SIDS system, new cells or modifications of existing cells can be generated and added to the cell library rapidly, without any hand layout. Similarly, non-cell functions such as analog elements or memory arrays, RAM or ROM, can be designed using SIDS and merged with standard cells.

This ability to add special features efficiently makes AMI's standard cell program far more flexible than other manufacturer's cell development systems.

Table 5. Standard Cell Offerings

Part No.	Process Technology		Availability
XXXX-001	5μ CMOS	Single Metal	NOW
XXXX-001	4μ NMOS	Single Metal	NOW
XXXX-001	3μ CMOS	Single Metal	NOW
XXXX-001	3μ CMOS	Double Metal	NOW
XXXX-001	2μ CMOS	Double Metal	2Q'84

Performance

AMI's standard cell circuits can be successfully used in digital circuits with operating speeds up to 10MHz for NMOS (or CMOS at 10V V_{CC}) up to 40MHz for CMOS (5V V_{CC}). It should be emphasized that if only a small portion of the circuit requires faster performance, this portion can be "customized" either by creating special cells or by designing circuitry outside of the cell structure. AMI will review customer logic without obligation to determine if a cell design is feasible.

Features

The high speed, high performance 3-micron cell families are also available. These cells are designed in AMI's 3 micron single and double layer metal process. They have been characterized for 3-5V operation and over the full military temperature range. As in 4000 series CMOS, power for static operation is near zero.

3-Micron Single Metal Standard Cells

- State-of-the Art CMOS Technology
- 3-Micron Single Metal Cell as Basic Building Block
- Same Macros and Performance for Cells and Arrays

3-Micron Double Metal Standard Cells

- Automatic Placement and Routing
- Cells are Designed to Exceed the Performance of 3-Micron DLM Gate Arrays
- Fixed Cell Height/Variable Width
- Characterized at 25°C, 70°C, and 125°C with V_{DD} = 4.5V

Table 6. 3μ CMOS Single Metal Standard Cells

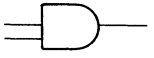
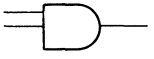
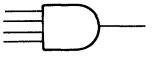
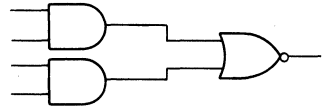
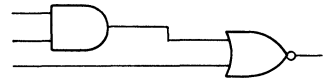
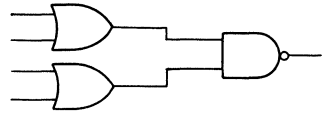
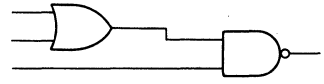
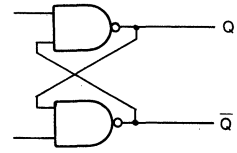
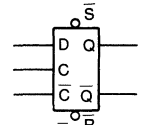
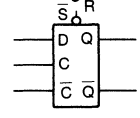
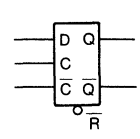
Name	Description	
AND GATES		
A215	2 INPUT AND	
A315	3 INPUT AND	
A415	4 INPUT AND	

Table 6. Continued

Name	Description	
COMPLEX GATES		
AN15	4 INPUT, AND-NOR	
AN25	3 INPUT, AND-NOR	
ON15	4 INPUT, OR-NAND	
ON25	3 INPUT, OR-NAND	
RS15	CROSS COUPLED NANDS AS A S- R- LATCH	
D FLIP FLOPS		
DHLLN25	D FLOP WITH SET D-, RESET D-, AND Q-	
DHLLN25	D FLOP WITH SET D- AND Q-	
DHNLN35	D FLOP WITH RESET D- AND Q-	

Semi-Custom Capabilities

Table 6. Continued

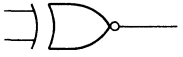
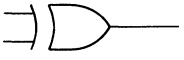
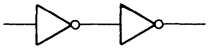
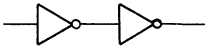
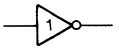
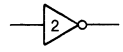
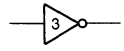
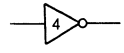
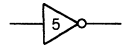
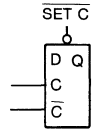
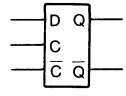
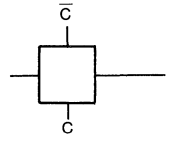
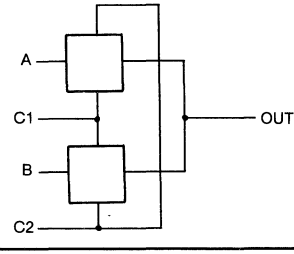
Name	Description	
EXCLUSIVE GATES		
EN215	2 INPUT EXCLUSIVE NOR	
EO215	2 INPUT EXCLUSIVE OR	
INPUT BUFFERS		
IB17	INPUT BUFFER, CMOS, INVERTING	
IB27	INPUT BUFFER, CMOS, NON-INVERTING	
IB37	INPUT BUFFER, TTL, INVERTING	
IB47	INPUT BUFFER, TTL, NON-INVERTING	
INVERTERS		
IN11	INVERTER (ONE WIDE)	

Table 6. Continued

Name	Description	
INVERTERS		
IN12	INVERTER (TWO WIDE)	
IN13	INVERTER (THREE WIDE)	
IN14	INVERTER (FOUR WIDE)	
IN15	INVERTER (FIVE WIDE)	
LATCHES		
LHCNN15	D LATCH WITH SET C-	
LHNNN25	D LATCH WITH Q-	
MULTIPLEXERS		
MU1115	SINGLE TRANSMISSION GATE	
MU2115	2:1 WITH SELECT AND SELECT-	

C1	C2	A	B	OUT
1	0	1,0	X	A
0	1	X	1,0	B

ONLY VALID STATES FOR C1 AND C2

Semi-Custom Capabilities

Table 6. Continued

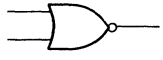
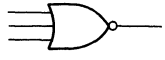
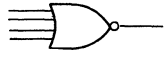
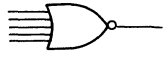
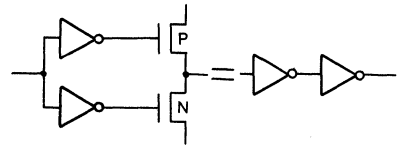
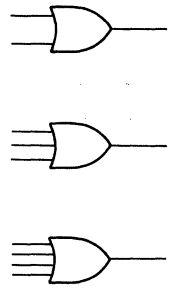
Name	Description	
NAND GATES		
NA215	2 INPUT NAND	
NA315	3 INPUT NAND	
NA415	4 INPUT NAND	
NA515	5 INPUT NAND	
NOR GATES		
NO215	2 INPUT NOR	
NO315	3 INPUT NOR	
NO415	4 INPUT NOR	
NO515	5 INPUT NOR	

Table 6. Continued

Name	Description
OUTPUT BUFFERS	
0817	OUTPUT BUFFER, CMOS NON-INVERTING
0827	OUTPUT BUFFER, TTL, NON-INVERTING



OR GATES	
OR215	2 INPUT OR
OR315	3 INPUT OR
OR415	4 INPUT OR



3-Micron Single Metal Standard Cell Performance — Selected Cells

Function	Prop Delay—nsec			Conditions
	25°C	70°C	125°C	
Inverter	1.2	1.5	1.7	1. One load of 0.25pF including 510 microns of metal (0.08pF)
2 In NAND	1.7	2.1	2.5	2. $V_{DD} = 4.5V$
4 In NAND	4.5	5.7	6.9	3. Typical Process
Ex NOR	4.4	6.5	6.6	4. Average of Low-High and High-Low
D LATCH (Clock-Q)	2.8	3.4	4.1	
DFF (Clock-Q)	3.6	4.4	5.3	

Semi-Custom Capabilities

3-Micron CMOS Double Metal

This is the list of all the 3-micron CMOS double metal standard cells presently available through AMI's Semi-Custom Design Group.

Name	Description
AND GATES	
A214	2 INPUT AND
A217	2 INPUT AND
A314	3 INPUT AND
A317	3 INPUT AND
A414	4 INPUT AND
A417	4 INPUT AND
COMPLEX GATES	
AN14	4 INPUT, AND-NOR
AN17	4 INPUT, AND-NOR
AN24	3 INPUT, AND-NOR
AN27	3 INPUT, AND-NOR
ON14	4 INPUT, OR-NAND
ON17	4 INPUT, OR-NAND
ON24	3 INPUT, OR-NAND
ON27	3 INPUT, OR-NAND
RS14	CROSS COUPLED NANDS AS AN SN RN LATCH
RS17	CROSS COUPLED NANDS AS AN SN RN LATCH
RS24	CROSS COUPLED NORS AS AN S R LATCH
RS27	CROSS COUPLED NORS AS AN S R LATCH
D FLIP FLOPS	
DHLLN14	D FLOP WITH RESETDN AND SETDN
DHLLN17	D FLOP WITH RESETDN AND SETDN
DHLLN24	D FLOP WITH RESETDN, SETDN, AND QN
DHLLN27	D FLOP WITH RESETDN, SETDN, AND QN
DHLNN14	D FLOP WITH SETDN
DHLNN17	D FLOP WITH SETDN
DHLNN24	D FLOP WITH SETDN AND QN
DHLNN27	D FLOP WITH SETDN AND QN
DHNLN14	D FLOP WITH RESETDN
DHNLN17	D FLOP WITH RESETDN
DHNLN24	D FLOP WITH RESETDN AND QN
DHNLN27	D FLOP WITH RESETDN AND QN
DHNNN14	D FLOP
DHNNN17	D FLOP
DHNNN24	D FLOP WITH QN
DHNNN27	FLOP WITH QN
EXCLUSIVE GATES	
EN214	EXCLUSIVE NOR, 2 INPUT
EN217	EXCLUSIVE NOR, 2 INPUT
EO214	EXCLUSIVE OR, 2 INPUT
EO217	EXCLUSIVE OR, 2 INPUT

Name	Description
INPUT BUFFERS	
IB17	INPUT BUFFER, CMOS, INVERTING, PAD LIMITED
IB27	INPUT BUFFER, CMOS, NON-INVERTING, PAD LIMITED
IB37	INPUT BUFFER, TTL, INVERTING, PAD LIMITED
IB47	INPUT BUFFER, TTL, NON-INVERTING, PAD LIMITED
IB57	INPUT BUFFER, CMOS, INVERTING, CORE LIMITED
IB67	INPUT BUFFER, CMOS, NON-INVERTING, CORE LIMITED
IB77	INPUT BUFFER, TTL, INVERTING, CORE LIMITED
IB87	INPUT BUFFER, TTL, NON-INVERTING, CORE LIMITED
IBD17	INPUT BUFFER, CMOS, NON-INVERTING, INTERNAL PULL DOWN, PAD LIMITED
IBD27	INPUT BUFFER, TTL, NON-INVERTING, INTERNAL PULL DOWN, PAD LIMITED
IBD37	INPUT BUFFER, CMOS, NON-INVERTING, INTERNAL PULL DOWN, CORE LIMITED
IBD47	INPUT BUFFER, TTL, NON-INVERTING, INTERNAL PULL DOWN, CORE LIMITED
IBT17	INPUT BUFFER, CMOS, INVERTING, TRI-STATE, PAD LIMITED
IBT27	INPUT BUFFER, CMOS, NON-INVERTING, TRI-STATE, PAD LIMITED
IBT37	INPUT BUFFER, TLL, INVERTING, TRI-STATE, PAD LIMITED
IBT47	INPUT BUFFER, TTL, ON-INVERTING, TRI-STATE, PAD LIMITED
IBT57	INPUT BUFFER, CMOS, INVERTING, TRI-STATE, CORE LIMITED
IBT67	INPUT BUFFER, CMOS, NON-INVERTING, TRI-STATE, CORE LIMITED
IBT77	INPUT BUFFER, TTL, INVERTING, TRI-STATE, CORE LIMITED
IBT87	INPUT BUFFER, TTL, NON-INVERTING, TRI-STATE, CORE LIMITED
IBT37	INPUT BUFFER, TTL, INVERTING, TRI-STATE, PAD LIMITED
IBT47	INPUT BUFFER, TTL, ON-INVERTING, TRI-STATE, PAD LIMITED
IBT57	INPUT BUFFER, CMOS, INVERTING, TRI-STATE, CORE LIMITED
IBT67	INPUT BUFFER, CMOS, NON-INVERTING, TRI-STATE, CORE LIMITED
IBT77	INPUT BUFFER, TTL, INVERTING, TRI-STATE, CORE LIMITED
IBT87	INPUT BUFFER, TTL, NON-INVERTING, TRI-STATE, CORE LIMITED
INVERTERS	
IN14	INVERTER
IN17	INVERTER
JK FLIP FLOPS	
JHLLN14	JK FLOP WITH KN, SETDN, AND RESETDN
JHLLN17	JK FLOP WITH KN, SETDN, AND RESETDN
JHLNN14	JK FLOP WITH KN AND SETDN
JHLNN17	JK FLOP WITH KN AND SETDN
JHNLN14	JK FLOP WITH KN AND RESETDN
JHNLN17	JK FLOP WITH KN AND RESETDN
JHNNN14	JK FLOP WITH KN
JHNNN17	JK FLOP WITH KN
LATCHES	
LHCLN14	D LATCH WITH SETCN AND RESETN
LHCLN17	D LATCH WITH SETCN AND RESETN
LHCNN14	D LATCH WITH SETCN
LHCNN17	D LATCH WITH SETCN
LHNLN14	D LATCH WITH RESETDN
LHNLN17	D LATCH WITH RESETDN
LHNNN14	D LATCH
LHNNN17	D LATCH
NAND GATES	
NA214	2 INPUT NAND

Semi-Custom Capabilities

Name	Description
NAND GATES (Continued)	
NA217	2 INPUT NAND
NA314	3 INPUT NAND
NA317	3 INPUT NAND
NA414	4 INPUT NAND
NA417	4 INPUT NAND
NA514	5 INPUT NAND
NA517	5 INPUT NAND
NOR GATES	
NO214	2 INPUT NOR
NO217	2 INPUT NOR
NO314	3 INPUT NOR
NO317	3 INPUT NOR
NO414	4 INPUT NOR
NO417	4 INPUT NOR
NO514	5 INPUT NOR
NO517	5 INPUT NOR
OUTPUT BUFFERS	
OB17	OUTPUT BUFFER, NON-INVERTING, PAD LIMITED
OB27	OUTPUT BUFFER, NON-INVERTING, CORE LIMITED
OBT17	OUTPUT BUFFER, NON-INVERTING, TRI-STATE, PAD LIMITED
OBT27	OUTPUT BUFFER, NON-INVERTING, TRI-STATE, CORE LIMITED
OBD17	OUTPUT BUFFER, NON-INVERTING, EXTERNAL PULL DOWN RESISTOR REQUIRED, PAD LIMITED
OBD27	OUTPUT BUFFER, NON-INVERTING, EXTERNAL PULL DOWN RESISTOR REQUIRED, CORE LIMITED
OBU17	OUTPUT BUFFER, NON-INVERTING, EXTERNAL PULL UP RESISTOR REQUIRED, PAD LIMITED
OBU27	OUTPUT BUFFER, NON-INVERTING, EXTERNAL PULL UP RESISTOR REQUIRED, CORE LIMITED
OR GATES	
OR214	2 INPUT OR
OR217	2 INPUT OR
OR314	3 INPUT OR
OR317	3 INPUT OR
OR414	4 INPUT OR
OR417	4 INPUT OR
T FLIP FLOPS	
THLNN14	T FLOP WITH SETDN
THLNN17	T FLOP WITH SETDN
THNLN14	T FLOP WITH RESETDN
THNLN17	T FLOP WITH RESETDN

NMOS Cells

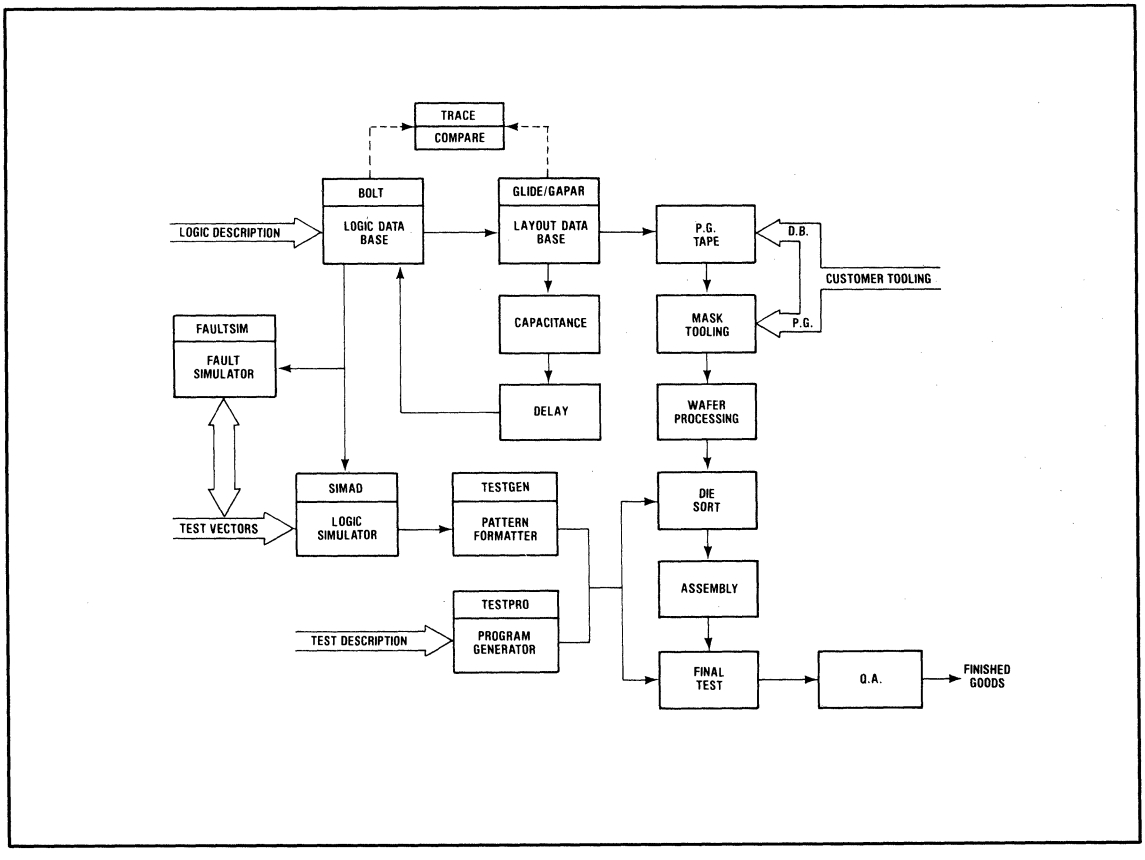
This family is AMI's most complete cell family with over 135 cells in 4 speed/power combinations. V_{DD} and V_{SS} connections are metal lines running horizontally across the cell. Two other metal lines, usually used for clock signals, also run across the cell. Typical and worst case inverter delays are 5.5ns and 10.0ns, respectively.

The NMOS cells are implemented using a 4 micron silicon gate process and can be used over the full military temperature range (−55°C to 125°C). Operating voltage is 5V ± 10%. The NMOS cells have been designed with three power/speed options. The fastest cells also have the highest power consumption and use the most area. Therefore, the fast cells should be used only where circuit performance requires high speed. Most circuits are optimized by using a combination of low power, standard and high speed cells.

CMOS Cells

The CMOS cells are designed using a 5 micron silicon gate oxide-isolated process and using 3 micron single and double layer metal process. These processes are well suited for analog circuitry and some analog cells will be added to the digital cells. The 5 micron CMOS cells are characterized for 3V to 12V operation over the full military temperature range (−55°C to 125°C). CMOS cells are generally used where low power battery operation or backup are required.

Table 7. Gate Array/Standard Cell Development Flow



Semi-Custom Capabilities

Developing Your Standard Cell Design

AMI offers three basic options for developing a standard cell custom circuit. All of these apply to the Development Flow Diagram of Table 7.

AMI Standard Development

The circuit user provides a completed logic diagram and a circuit specification. AMI performs all other design activity including MOS logic design, circuit design, layout, mask generation and fabrication of wafers. This development option is recommended for most users desiring to build a single LSI device and for multiple circuit users who do not wish to become directly involved in the MOS circuit development.

Shared Development

For those users who want to participate in the design of a standard cell circuit, a Design Manual is provided for either the NMOS or CMOS cell family. The Design Manual has complete performance data over temperature and voltage for all the cells. The manual contains information for calculating speed, power and die size. In addition, guidelines for logic design, breadboarding and developing test programs are provided. In a typical "shared" development, the user designs the logic using the available cells and performs preliminary power and speed calculations. The user may then identify or even lay out areas of the circuit requiring special attention to guarantee performance. The Design Manual is provided without obligation, but AMI does require the user to sign a "Non-Disclosure" agreement. A shared development is recommended for users who are considering multiple circuit developments, but who do not have an internal MOS design capability.

Customer Designed Input by Terminal

Users who wish to design their standard cell circuits, but do not want to invest in a CAD (Computer-Aided Design) system, can design their circuit on a low cost terminal. AMI's logic simulator SIMAD (SIMulator with Assignable Delays) is available for the users to simulate their desired logic on a time share terminal. The standard cells have been stored as logic MACROS. When the users are satisfied with the logic simulation they notify AMI, and AMI uses this data base to run the customer's software programs. A plot of the circuit is returned to the user for approval. After approval, AMI will deliver samples of the device in a short time period.

Customer Designed Circuits

For those users who wish to design custom circuits entirely within their own facility, AMI licenses the use of both (NMOS & CMOS) cell families. Standard cell tooling is provided in the form of a data base tape containing the topological information of the cells. AMI also licenses the use of several powerful CAD tools used in developing cell circuits. The user does the complete circuit design and develops a pattern generator tape which is used to make the wafer processing masks. Customer designed standard cell circuits require the user to have or be willing to develop a MOS design capability. However, a mask making or wafer fabrication facility is not required.

Development Schedule

One of the primary objectives of a cell program is to design a VLSI circuit in the shortest possible time span. Circuit design is almost eliminated since both function and performance of the cells have been previously determined. Some effort is still required to verify that timing and power requirements are met. When cells are used, layout is completely automatic using the appropriate place and route program. In a conventional custom circuit layout, seven or eight mask layers must be carefully layed out and checked for possible layout errors. This layout simplicity greatly reduces the possibility of a layout error causing a time consuming second iteration of the design cycle.

Development Cost

Most AMI cell developments cost between $15,000 and $50,000. The factors that determine the cost of a standard cell circuit are: size of circuit in equivalent 2 input NAND gates, critical performance requirements and point of entry into the design cycle.

Test Plan Development

Regardless of the design or layout method, production shipments of a custom device are dependent on a test program to test devices at wafer sort and after final assembly. A substantial portion (up to 20%) of the development cost is required for generating and "debugging" the test program. For users who are able to provide detailed test information, the development cost is reduced. A summary of standard cell costs and development spans is shown in Table 8.

Table 8. AMI Standard Cell
3 Micron Single Metal Interface

	Logic Diagram Input		Net List Input	
No. of Gates	Cost	Max. Span	Cost	Max. Span
500	$19.7K	9 Weeks	$15.7K	7 Weeks
1000	$22.8K	11 Weeks	$16.8K	9 Weeks
2000	$31.3K	13 Weeks	$21.3K	11 Weeks

AMI®

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Custom Capabilities

Spectrum of Custom Solutions

No other company can match AMI's track record in developing state-of-the-art custom MOS products. With more than 2000 custom devices designed and manufactured since 1966, AMI has more experience than any other integrated circuit company in building a wide variety of custom microcircuits.

AMI not only has the experience, but the design engineering organization and the advanced production and testing facilities to produce the highest quality MOS/VLSI circuits. And because AMI also offers standard memory, microprocessor, telecommunication and consumer products and the widest variety of custom VLSI processes in the industry, we're able to be objective in helping customers determine their most cost effective approach.

The Advantages of Custom Circuits

Since a single custom MOS/VLSI chip can replace expensive electromechanical devices, discrete logic components, or less efficient general purpose LSI circuits, it offers a number of benefits not available with standard logic.

Custom circuits save money. Grouping functions onto a single chip lowers production and inventory costs dramatically. That reduces your product manufacturing costs as well.

Custom circuits are more reliable. Putting a complete system on a chip trims component count, improving both product reliability and production yields. Rework, repair and replacements are minimized.

Custom circuits reduce space and power requirements. Fewer components means both space and power requirements are reduced.

Custom circuits offer superior performance. Since the circuit is designed to your requirements, features and functions can be incorporated which are not available in general purpose chips. Special tailoring reduces test requirements as well.

Custom circuits offer proprietary protection. Being tailored exactly to your requirements, a custom circuit cannot be easily duplicated. This can help put you ahead — and keep you ahead — of your competition.

The Spectrum of Solutions

The decision to use a custom circuit depends on your system design requirements — such things as complexity, features, size and power limitations. But no longer is your custom decision limited by low volume or short development time — not when you come to AMI.

AMI has a full spectrum of custom solutions to assure you get that solution which meets your system performance and time-to-market requirements at the lowest possible cost.

AMI's spectrum of solutions bridges the total span of volume, timing and interface needs of our customers. From semi-custom designs, to full custom design — somewhere on the spectrum, your development time and volume requirements can be met. For customers who already have their designs, AMI can provide custom fabrication for the customer's tooling. We will even teach custom design if that's what our customers need. And we can even go a step further and license the technology for a customer to set up his own fabrication capability. No other company offers such a spectrum of solutions. And no other company has more experience at helping you pick the best solution for your needs.

Semi-Custom Gate Arrays

AMI offers both gate arrays and standard cell design methods for semi-custom circuit development.

Gate arrays are the best solution for circuits of moderate complexity in low-to-medium volume applications or where the shortest possible development time is required. AMI offers both gate arrays and standard cell design methods for semi-custom circuit development.

AMI CMOS semi-custom gate arrays are standard logic layouts of everything except the final metal interconnect pattern. Since only the final pattern needs to be developed to customize your circuits, both development time spans and development costs are dramatically reduced. Because wafers containing arrays are preprocessed and inventoried, production lead times are short. Gate arrays are especially attractive for applications requiring circuit volumes from 1,000 to 50,000 units per year.

For more details on AMI's gate arrays, refer to the "Semi-Custom" section of this catalog.

Standard Cell Custom

Standard cells are custom circuits which are designed from computer stored modular cells. The computer assembles the cells into a collection of functional blocks to form a custom circuit. Since standard cells utilize predesigned cells, development time is reduced dramatically and development costs are cut 30 to 50 percent over conventional custom design. Circuit size is likely to be slightly larger than a conventional custom circuit, so they are most appropriate where rapid development is more important than minimal size. Standard cells are cost effective in volume levels beginning around 10,000 circuits.

For more details on AMI standard cells refer to the "Semi-Custom" section of this catalog.

Optimized Custom Design

Where end product volume is high — beyond 50,000 units per year — or where special requirements for lowest power, minimal space or highest performance exist, the solution is likely to be conventional custom design. By optimizing circuit elements and layout for a specific part, die size is substantially smaller than using semi-custom design methods. In high volume applications, a smaller die size results in lower unit cost to the customer.

In addition, custom designs allow you to combine logic elements, memory, and analog circuits in a single device. This design flexibility is not available in gate arrays and only available to a limited extent in standard cells.

Instrumental in the design of custom circuits is our Symbolic Interactive Design System (SIDS). The design is done primarily with SIDS where a layout designer works with symbols directly at a large screen alphanumeric color CRT. After the SIDS circuit design has been completed and verified, the symbols are converted to polygons and a 10X reticle tape is prepared.

SIDS uses on-line, real-time design rule checking capability to isolate design rule errors in the layout. This allows immediate correction which greatly reduces the development span time.

Also a nodal trace function permits a designer to trace and highlight a given electrical node. In this way, the designer can manually insure that the node is connected as specified in the master logic description.

Full background real-time design rule checking on windows, cells, and chips is supported, as is full background continuity checking against the master logic description. This eliminates the delay from digitizing and batch processed computer checking of circuits for accuracy.

With SIDS, error correction, circuit modification and area relocations take only minutes. That significantly reduces design cycle time and development costs.

Computer-aided hand-drawn layouts are used to reduce extremely complex circuits to the absolute smallest size. Development time and costs are higher, but in certain cases, size or complexity requirements may require the hand-drawn approach.

Customer Owned Tooling

In many cases AMI customers design their own circuits, either through an internal design center, a design house, or another vendor. In these cases, AMI can provide custom circuit fabrication from customer owned tooling. In conjunction with a silicon foundry service, AMI's Customer Owned Tooling (COT) group can offer the customer design support in the form of design rules, standard cells, a three phase development program, test program generation and general technical support. In the event of design problems, AMI's COT group utilizes the design expertise of the custom or semi-custom group for technical assistance.

Once the circuit is designed, the customer has the option of transferring the circuit tooling to AMI in PG tape, data base tape or working plate form. Close cooperation between the customer and AMI's COT Group during an established three phase prototype development program simplifies circuit debug and reduces risk of design error.

Drawing on AMI's extensive manufacturing ability, COT offers a wide range of process variations, package types, and test capabilities. Unlike most of AMI's competition in the silicon foundry market, AMI has internal photolithography (mask making) and assembly capability. This internal capability avoids the high costs and quality risks of subcontracting two very important steps in custom IC manufacturing.

Once the prototype development program is completed, AMI can ship as few as five to as many as thousands of wafers per week to the customer. AMI can ship tested die, fully tested packaged devices and devices meeting military 883-B standards.

AMI's Customer Owned Tooling group is the only vendor in the silicon foundry market that offers design support, full service manufacturing capability, flexibility and experience.

Joint Development Ventures

Through a Joint Development Team (JDT) we can teach a customer to design his own MOS/VLSI circuits. The JDT is a combination of technically skilled people from the partner company and AMI who function as a design group concentrating on the customer's products alone. The JDT partner brings his system design staff and AMI brings the MOS/VLSI staff and its design technology. The partner becomes part of an in-house AMI design group. The end result is a design capability for the partner company for circuits that AMI will fabricate.

If the customer wants to go beyond designing his own circuits to operating his own manufacturing/pilot line, AMI will license the necessary technology in those situations where a long-term business relationship can be established between the partner company and AMI.

AMI Provides Leading CAD Technology

At almost all levels of the spectrum, computer-aided design (CAD) software and hardware aids are employed to assure correctness of design each step of the way and to shorten design spans reducing customer risk and lowering design cost. Highly efficient programs have been implemented to assist in logic design and simulation, layout planning, switched capacitor analysis routines and symbolic interactive design layout, to name just a few.

Hardware design aids include:

- On-site Burroughs 7760 computer with multiprocessing capability.
- Computer terminals built around a Prime computer and engineering design facilities which tie into the on-site 7760 and time-sharing services.
- Computervision interactive graphics system which provide on-line generation and editing of composite drawings; includes drafting surfaces and CRT displays.
- Calma graphics system for both production digitizing and on-line changes.
- Calma GDS-11 high speed electrostatic plotter.

• High speed, high resolution Electromask 9-track pattern generator.

Software design aids include:

Logic Design

• **Register Transfer Language (RTL) Simulation** — Provides a system behavior description to define instruction sets, optimize data paths, control hardware algorithm design and establish register designs.

• **Glide** — Permits user to design layout, simulate, generate patterns and develop test programs for logic arrays.

• **Path Analysis Program (PATH)** — Permits gross logic checks to be made before design, and final logic checks from the ultimate design.

• **Logic Simulator (SIMAD)** — (SIMulator with Assignable Delays) simulates logic network behavior for design verification and propagation delays.

• **Programmable Logic Array Designs Aids (PLAID)** — Uses state tables and Boolean equations to generate the optimum physical structure for random logic designs.

• **Block Oriented Logic Translator (BOLT))** — A logic description compiler that generates a common data base used by SIDS, SIMAD, LPA, continuity check, PATH and CIPAR.

• **Design Rule Checking (DRC)**

• **Trace and Continuity Checking**

Circuit Design

• **Circuit Simulator (ASPEC)** — Analyzes DC operation, DC transfer functions, time domain or transients and frequency domain or small signal AC characteristics.

• **Pole Zero Analysis (PZSLIC)** — Program analyzes the frequency domain of linear integrated circuits.

• **Switched Capacitor Analysis Routine (SCAR)** — Analyzes switched capacitor filter designs for telecommunications and other analog circuits.

• **Data Analysis Program (DAP)** — Analyzes data from circuit fabrication to maintain the parameters of circuit designs.

Mask Design

• **Layout Planning Aid (LPA)** — Lays out the chip plan and interconnection between functional blocks of an integrated circuit.

• **Symbolic Interactive Design System (SIDS)** — Permits a layout designer to work directly with a computer to lay out and check a circuit on a CRT screen, dramatically shortening layout time requirements.

• **Circuit Interactive Place and Route (CIPAR)** — Automatically creates error-free mask designs in extremely short time spans.

Test Generation

AMI utilizes numerous software programs to generate test programs for integrated circuits. All serve to reduce the time needed to develop test programs to meet customer specifications.

Digital and Analog Combinations

AMI is a leading innovator in combining digital and analog functions on a single chip. We can combine any of the functions below into an optimum circuit configuration to meet your needs. Unique combinations of these functions are already used in many applications in the communications, consumer, and industrial marketplace.

DIGITAL	ANALOG
PLA	OP AMP
ALU	Oscillator
Inverter	Comparator
RAM and ROM	Voltage Reference
Shift Register	A/D and D/A Converters
Interface Driver	Switched Capacitor Filters
Automatic Power Down	Programmable Power Down
	Phase Locked Loops

State of the Art Packaging

AMI's packaging capability spans a broad spectrum, beginning with plastic, ceramic and CERDIP and going on to chip carriers, die bonding to PC boards and, most recently, mini-flat packs. As well as being a leader in plastic packaging for the high volume, low cost consumer industry, AMI's high reliability plastic packages and chip carriers are accepted under the stringent requirements in the Telecom and Automotive industries. As many industry segments move toward space-saving packages, AMI remains in the forefront in packaging using chip carriers. AMI now is developing a family of mini-flat packs which are a plastic alternative to a chip carrier.

AMI Delivers Quality

AMI quality controls for in-process wafer inspection and final assembly and test are the best in the industry. Our care in fabrication, assembly and test mean that you get products that meet your specifications for reliability. Because over 70 percent of our total production is custom, we perform many checks routinely that would only be done on special orders and at additional cost by other manufacturers. In fact, our own in-house standards are tougher than most of our customers require. Most importantly, AMI is committed to making sure that everything we do is done right, every time we do it.

The Industry's Highest Standard

AMI has consistently pursued product excellence and has reached for higher quality levels in finished products shipped. Circuits are inspected to 0.04% AQL or your specifications, whichever is more stringent.

This 0.04% AQL can put you in a superior competitive position. Your incoming test and assembly costs come down since there is less reworking on the line. And your customers receive a more reliable product.

Quality Checks

Among the routine quality controls exercised over every product at AMI are:

- Full logic design checks against system specifications
- Circuit simulation to verify performance against objectives
- Working plates check on automatic checkers
- Automated mask fabrication checks
- In-process wafer fabrication checks
- Wafer sort tests
- 100% optical inspection at dicing
- 100% die attach checking
- 100% lead bonding inspection prior to package sealing
- Seal checks, fine and gross leak tests
- Final digital and analog tests
- Customer specified environmental tests

Meticulous in-process checks are performed on design and workmanship at every step, to ensure a full manufacturable device. In manufacture, lot process and yield data are captured and examined as a matter of routine.

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Communication Products

For more information on those data sheets which are not included in their entirety refer to AMI's Telecom Design Manual or contact Telecom Marketing at (408) 554-2070

Communication Products Selection Guide

STATION PRODUCTS

Part No.	Description	Process	Power Supplies	Packages
S2550A	Speech Network with Tone Ringer	CMOS	Line Powered	18 Pin
S2559A/B	DTMF Generator	CMOS	3.5V to 13V	16 Pin
S2559C/D	DTMF Tone Generator	CMOS	2.75V to 10V	16 Pin
S2559E/F/G/H	DTMF Generator	CMOS	2.5V to 10V	16 Pin
S2859	DTMF Generator	CMOS	3.0V to 10.0V	16 Pin
S2860	DTMF Generator	CMOS	3.5V	16 Pin
S2560A	Pulse Dialer	CMOS	1.5V to 3.5V	18 Pin
S2560G	Pulse Dialer	CMOS	2.0V to 3.5V	18 Pin
S2561, S2561C	Tone Ringer	CMOS	4.0V to 12.0V	18 Pin
S2561A	Tone Ringer	CMOS	4.0V to 12.0V	8 Pin
S2563	Pulse Repertory Dialer, Line Powered	CMOS	2V to 5.5V	40 Pin
S2569/A	DTMF Generator with Redial	CMOS	2.0V to 3.5V	16 Pin
S2569B	DTMF Generator with Redial	CMOS	2.0V to 3.5V	18 Pin
S25089	DTMF Generator	CMOS	2.5V to 10V	16 Pin
S25610	Repertory Dialer	CMOS	1.5V to 3.5V	18 Pin
S25610E	DTMF Repertory Dialer	CMOS	2.0V to 3.5V	18 Pin
S25910	DTMF Repertory Dialer	CMOS	Line Powered	14 Pin

PCM PRODUCTS

S3501	μ-Law Encoder with Filter	CMOS	$\pm$5V	18 Pin
S3502	μ-Law Decoder with Filter	CMOS	$\pm$5V	16 Pin
S3506	A-Law Combo Codec with Filters	CMOS	$\pm$5V	22 Pin
S3507/A	μ-Law Combo Codec with Filters	CMOS	$\pm$5V	22/28 Pin

SIGNAL PROCESSORS

RTDS28212	Real-Time Development System			
SSPP28211	Software Simulator Assembly Program Package			
S28211	Signal Processing Peripheral (ROM Programmed)	NMOS	5V	28 Pin
S28212	Signal Processing Peripheral (Externally Programmed)	NMOS	5V	64 Pin
S28214	Fast Fourier Transformer	NMOS	5V	28 Pin
S28215	Digital Filter/Utility Peripheral	NMOS	5V	28 Pin
S28216	Echo Cancellor Processor	NMOS	5V	28 Pin

MODEM AND FILTER PRODUCTS

S3522	Bell 212/V.22 Modem Filter	CMOS	9V to 11V	16 Pin
S35212	Bell 212/V.22 Modem Filter with I/O Filtering	CMOS	8V to 12V	24 Pin
S3525A/B	DTMF Bandsplit Filter	CMOS	10.0V to 13.5V	18 Pin
S3526	2600Hz Band-Pass/Notch Filter	CMOS	9V to 13.5V	14 Pin
S3528	Programmable Low Pass Filter	CMOS	9V to 13.5V	18 Pin
S3530	Single Chip Bell 103/V.21 Modem	CMOS	9.5V to 10.5V	28 Pin

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Advanced Product Description **S2550A**

TWO TO FOUR WIRE TELEPHONE HYBRID WITH TONE RINGER

COMMUNI-CATIONS

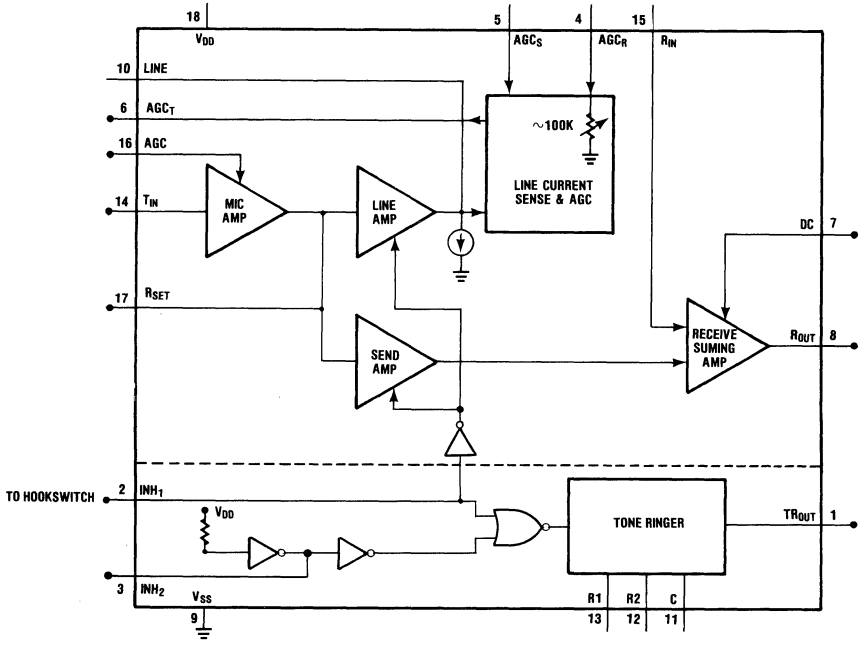
Features

- ☐ Monolithic IC Consisting of the Speech Network and Tone Ringer
- ☐ Interfaces With Inexpensive Condenser Electret Microphone, Electromagnetic Receiver and a Piezoelectric Ringer Transducer
- ☐ Automatic Gain Adjustment for Loop Loss Compensation
- ☐ Low Voltage CMOS Process for Operation Over Varying Loop Lengths and Currents
- ☐ Uses Inexpensive and Non-Critical External Components

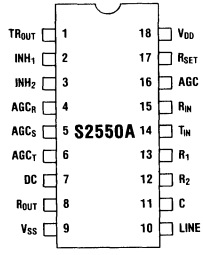
General Description

The S2550A is a monolithic integrated circuit specifically designed for implementing a low cost telephone set circuit. It consists of the hybrid circuit for speech transmission and reception and a tone ringer circuit that generates an audible tone coincident with the incoming ringing signal through a suitable piezoelectric transducer or high impedance speaker.

Functional Block Diagram



Pin Configuration



Circuit Description

The S2550A consists of the following functional blocks.

1. Transmitting transconductance amplifier with AGC. The transconductance is programmed by an external resistor to R-set.
2. Receiving transconductance amplifier with AGC. The output current level is adjusted on pin "DC".
3. Hybrid circuit. An external RC circuit must be added to compensate the phase shift for different line length and line impedance.
4. Line current sensing circuit for automatic gain control.
5. Tone ringer with output stage capable of driving a piezoelectric transducer or a high impedance speaker.

Voltage gain of the first stage of transmitting amplifier can be adjusted by the ratio of the negative feedback resistors R11, R12. Current gain and current level is programmed by R13.

The Inhibit Input 1 turns off the speech part of the circuit and activates the tone ringer if it is set to logical "1". Setting it to logical "0" activates the speech circuit and puts the tone ringer output to a high impedance state. AGC input is active when connected to pin AGC_T via capacitor. The side tone cancelling current is connected to the receiver input pin R_{IN}.

The automatic gain control of the receiver amplifier is provided by connection of input R_{IN} to AGC_R via a capacitor.

Tone ringer frequency is set by RC time constant on pins R1, R2 and C. The Inhibit Input 2 is provided to inhibit the oscillator by setting the necessary delay to avoid false ringing.

Absolute Maximum Ratings

Line Voltage V_L	15V
Line Current I_L	120mA
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +140°C

S2550A Electrical Characteristics (@ 25°C. Measured Using Circuits of Figures 1 and 2.)

Parameter	Min.	Typ.	Max.	Test Conditions
Sending Gain $G_S = 20 \log \frac{V_L}{V_T}$	37dB 30dB	40dB 33dB	43dB 36dB	f = 1000Hz V_T = 10mV RMS I_L = 20mA I_L = 60mA
Sending Gain Flatness		±0.5dB		I_L = 20 to 80mA f = 300 to 3400Hz
Sending Distortion @ 20mA I_L		2.5%	5%	f = 1000Hz V_T = 10mV RMS
Receiving Gain $G_R = 20 \log \frac{V_R}{V_L}$	−4dB −9dB	−1dB −6dB	+2dB −3dB	f = 1000Hz V_L = 100mV RMS I_L = 20mA I_L = 60mA
Receiving Gain Flatness		±0.5dB		I_L = 20 to 80mA f = 300 to 3400Hz
Receiving Distortion @ 20mA I_L		2%	5%	f = 1000Hz V_R = 100mV RMS
Side Tone $G_L = 20 \log \frac{V_R}{V_T}$	23dB 15dB	29dB 21dB	35dB 27dB	f = 1000Hz V_T = 10mV RMS I_L = 20mA I_L = 60mA

S2550A Electrical Characteristics (continued)

Parameter	Min.	Typ.	Max.	Test Conditions
Sending Noise		20dBrnC0		I_L = 60mA V_T = 0V
V_{IL} Logic "0" Input Voltage			.3V Max.	
V_{IH} Logic "1" Input Voltage		V_{DD}		
I_L (Operating Current)	20mA	10mA Min.		Note 1
V_{DD} (Operating Voltage)	2.0V		12V	Note 2

Note 1. Although the S2550 is tested to a 20mA minimum loop current, it will normally work down to a 10mA loop current.
Note 2. This is a voltage guideline, not a tested specification. The S2550A is tested at specific loop currents, not voltages.

Table 1. S2550A Pin/Function Descriptions

Pin #	Name	Function
1	TR_{OUT}	Tone ringer output.
2	INH_1	This input selects the tone ringer or the speech network depending on the input level. A high level inhibits speech network but enables the tone ringer. A low level enables the speech network but inhibits the tone ringer.
3	INH_2	For normal operation this pin can be left open. It has an internal pull-up resistor. To avoid false ringing, a capacitor can be connected to V_{SS} from this pin to create a delay in response time to ringing signal.
4	AGC_R	A capacitor (C4) connected between this pin and R_{IN} allows loop loss compensation for receiving gain. This input looks like a variable resistor varying with loop current.
5	AGC_S	This input also looks like a variable resistor varying with loop current; can be used to modify the artificial line consisting of R7, R8, and C5.
6	AGC_T	This input is used to adjust sending gain.
7	DC	This input controls DC current through receiver by ratio of two resistors, R_9 and R_{10}.
8	R_{OUT}	Receiver output, capable of driving low impedance receivers (300Ω value suggested).
9	V_{SS}	Negative power terminal.
10	LINE	Line Input. AC input impedance seen by the phone line is primarily a function of resistor R3 and Cap C2 connected between LINE, V_{DD} and V_{SS}. This pin modulates the line current.
11	C	This pin is to connect external capacitor to form R-C oscillator for tone ringer.
12	R_2	External resistor to form R-C oscillator for tone ringer.
13	R_1	Tone ringer input to modulate ringing frequency.
14	T_{IN}	Microphone input to sending amplifier.
15	R_{IN}	Input of receiving amplifier.
16	AGC	AGC input for sending amplifier.
17	R_{SET}	Input to second stage sending amplifier. (22K for R13 gives approximately 50mA line current at 4.5V. R_{SET} is inversely proportional to line current.)
18	V_{DD}	Positive power terminal.

Figure 1. Test Set-Up Using Loop Simulator Shown in Figure 2 to Test Hybrid Functions

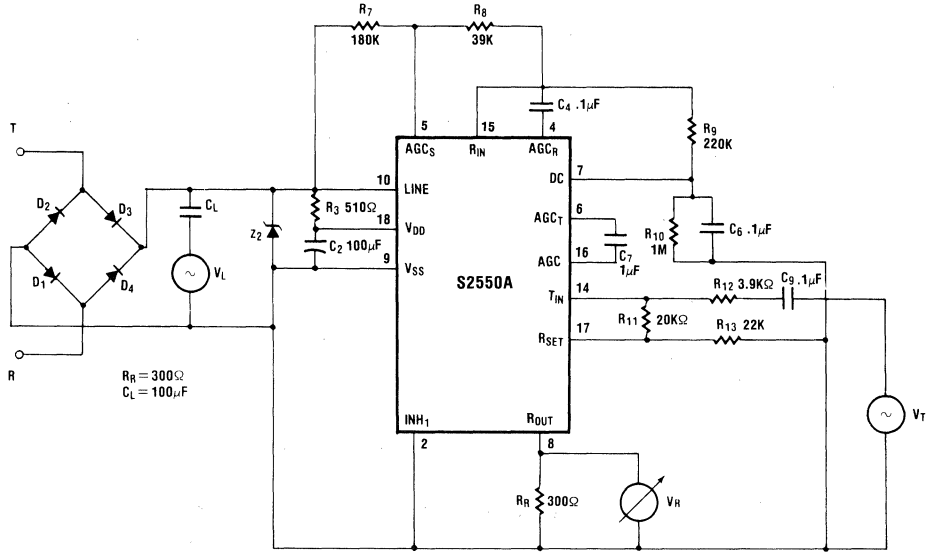


Figure 2. Loop Simulator

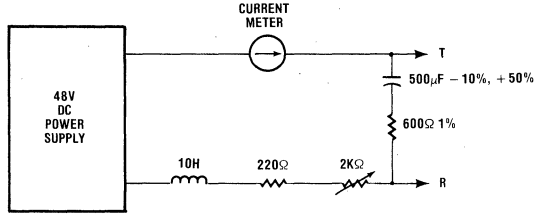
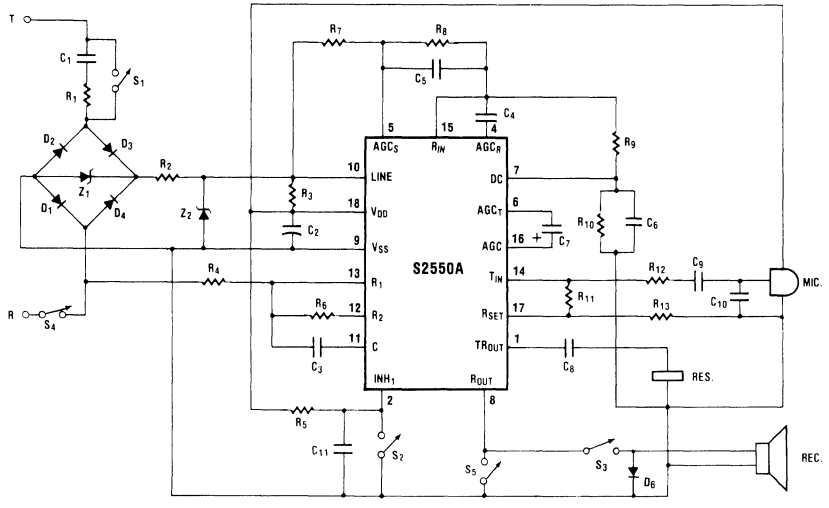


Figure 3. Typical Application Circuit for a Rotary Dial Telephone



NOTES: CIRCUIT SHOWN WITH CONTACT POSITIONS IN THE ON-HOOK STATE. S1, S2 and S3 ARE HOOKSWITCH CONTACTS. S4 AND S5 ARE ROTARY DIAL CONTACTS.

Parts List for Application Circuit of Figures 1, 3, 4, 5

R1	= 2KΩ	R23	= 5KΩ	C15	= 100μF
R2	= 20Ω	R24	= 5KΩ	C16	= 1μF
R3	= 510Ω	R25	= 1KΩ		
R4	= 5.6MΩ	R26	= 100KΩ	Q1	= 2N5401
R5	= 1MΩ	R27	= 20KΩ	Q2	= 2N5550
R6	= 500KΩ	R28	= 10KΩ	Q3	= 2N5550
R7	= 180KΩ	R29	= 7.5KΩ	Q4	= 2N5550
R8	= 39KΩ				
R9	= 220KΩ	C1	= 1μF	Z1	= 110V ZENER
R10	= 1MΩ	C2	= 100μF	Z2	= 12V ZENER
R11	= 20KΩ	C3	= .001μF	Z3	= 3.9V ZENER
R12	= 3.9KΩ	C4	= .1μF		
R13	= 22KΩ	C5	= 220pF	D1-D4	= 1N4004
R14	= 20MΩ	C6	= .1μF		
R15	= 1KΩ	C7	= 1μF	D5-D6	= 1N914
R16	= 5KΩ	C8	= 1μF	MIC	= EM-60 (PRIMO ELECTRO DYNAMIC)
R17	= 150KΩ	C9	= .1μF		
R18	= 10KΩ	C10	= .01μF	RES	= PIEZOELECTRIC TRANSDUCER OR SPEAKER
R19	= 750KΩ	C11	= .1μF		
R20	= 750KΩ	C12	= 15μF	REC	= ELECTROMAGNETIC RECEIVER (300Ω IMPEDANCE)
R21	= 750KΩ	C13	= 270pF		
R22	= 900Ω	C14	= 1μF	X	= 3.58 MHz Crystal

Figure 4. A Typical Application Circuit for an Electronic Telephone (Circuit Shown With Hookswitch Contact Position S1-S5 in the On-Hook State.)

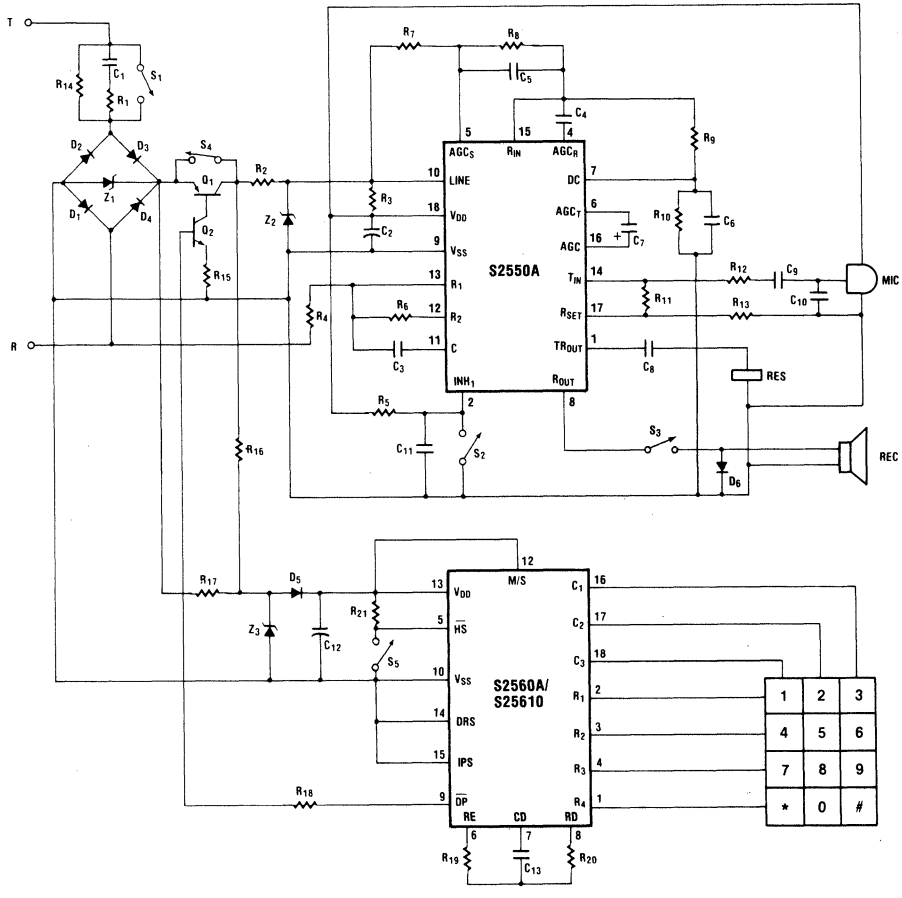
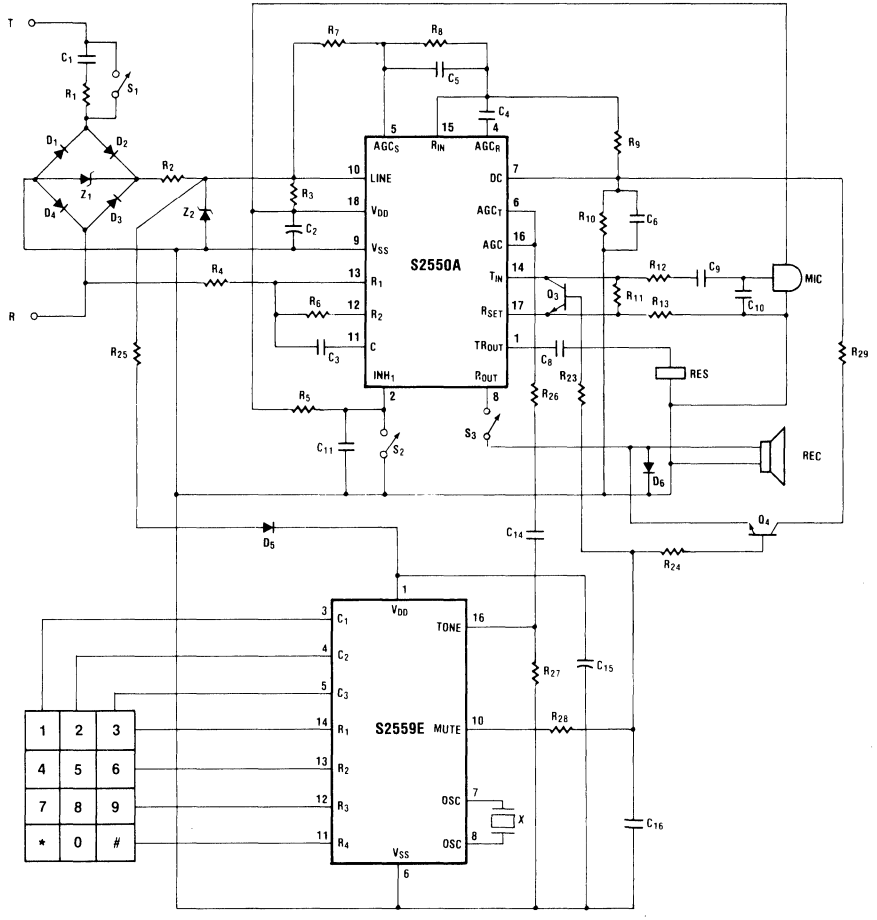


Figure 5. A Typical Application Circuit for an Electronic Telephone With DTMF (Circuit Shown With Hookswitch Contact Position S1-S3 in the On-Hook State.)



S2559A/B/C/D

DTMF TONE GENERATOR

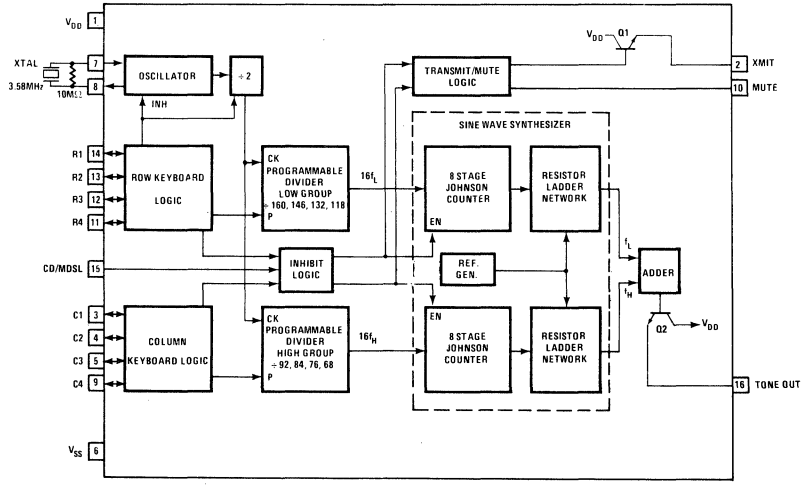
Features

- ☐ Wide Operating Supply Voltage Range: 3.5 to 13.0 Volts (A,B) 2.75 to 10 Volts (C,D)
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V
- ☐ Uses TV Crystal Standard (3.58MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability
- ☐ Mute Drivers On-Chip
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator-Type X-Y Keyboard
- ☐ The Total Harmonic Distortion is Below Industry Specification
- ☐ On-Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range
- ☐ Single Tone as Well as Dual Tone Capability
- ☐ Four Options Available:
  - A:3.5 to 13.0V Mode Select
  - B:3.5 to 13.0V Chip Disable
  - C:2.75 to 10V Mode Select
  - D:2.75 to 10V Chip Disable

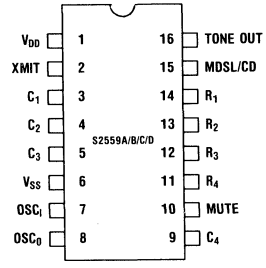
General Description

The S2559 DTMF Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton

Block Diagram



Pin Configuration



General Description (Continued)

telephone keyboard or calculator type X-Y keyboard and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinudsoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2559 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, Point-of-Sale, and Credit Card Verification Terminals and process control.

Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$) S2559 A, B	+ 13.5V
DC Supply Voltage ($V_{DD} - V_{SS}$) S2559 C, D	+ 10.5V
Operating Temperature	− 0°C to + 70°C
Storage Temperature	− 55°C to + 155°C
Power Dissipation at 25°C	500mW
Input Voltage	$-0.6 \leq V_{IN} \leq V_{DD} + 0.6$

S2559A & B Electrical Characteristics:

(Specifications apply over the operating temperature range of 0°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions	($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage					
V_{DD}	Tone Out Mode (Valid Key Depressed)		3.5		13.0	V
	Non Tone Out Mode (No Key Depressed)		3.0		13.0	V
	Supply Current					
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)	3.5		0.4	40	μA
		13.0		1.5	130	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)	3.5		0.95	2.9	mA
		13.0		11	33	mA

S2559A & B Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Tone Output						
V_{OR}	Single Tone Mode Output Voltage	Row Tone, $R_L = 390\Omega$	5.0	417	596	789	mVrms
		Row Tone, $R_L = 240\Omega$	12.0	378	551	725	mVrms
V_{OC}		Column Tone, $R_L = 390\Omega$	5.0	534	781	1022	mVrms
		Column Tone, $R_L = 240_\varrho$	12.0	492	722	955	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.5 – 13.5	1.75	2.54	3.75	dB
%DIS	Distortion*		3.5 – 13.5			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage (No Key Depressed)(Pin 2)	$I_{OH} = 15mA$	3.5	2.0	2.3		V
		$I_{OH} = 50mA$	13.0	12.0	12.3		V
I_{OF}	XMIT, Output Source Leakage Current $V_{OF} = 0V$		13.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed) No Load		3.5		0	0.4	V
			13.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed) No Load		3.5	3.0	3.5		V
			13.0	13.0	13.5		V
I_{OL}	MUTE, Output Sink Current	$V_{OL} = 0.5V$	3.5	0.66	1.7		mA
			13.0	3.0	8.0		mA
I_{OH}	MUTE, Output Source Current	$V_{OH} = 2.5V$	3.5	0.18	0.46		mA
		$V_{OH} = 9.5V$	13.0	0.78	1.9		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current	$V_{OL} = 0.5V$	3.5	0.26	0.65		mA
	One Key Selected	$V_{OL} = 0.5V$	13.0	1.2	3.1		mA
I_{OH}	Output Source Current	$V_{OH} = 2.5V$	3.5	0.14	0.34		mA
	One Key Selected	$V_{OH} = 9.5V$	13.0	0.55	1.4		mA
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	$V_{IL} = 13.0V$	13.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	$V_{IH} = 0.0V$	13.0			1.0	μA
I_{IL}	Sink Current	$V_{IL} = 0.5V$	3.5	24	93		μA
	No Key Selected	$V_{IL} = 0.5V$	13.0	27	130		μA
t_{START}	Oscillator Startup Time		3.5		3	6	ms
			13.0		0.8	1.6	ms
$C_{I/O}$	Input/Output Capacitance				12	16	pF
					10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, $V_{IL} = 3.5V$ (Pull-down)	3.5	7	17		μA
		Sink Current $V_{IL} = 13.0V$ (Pull-down)	13.0	150	400		μA
I_{IH}		Source Current, $V_{IH} = 3.0V$ (Pull-up)	3.5	90	230		μA
		Source Current, $V_{IH} = 12.5V$ (Pull-up)	13.0	370	960		μA

*Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

S2559A & B Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
I_{IH}	Mode Select Input (S2559A)	Source Current, $V_{IH} = 0.0V$ (Pull-up)	3.5	1.5	3.6		μA
		Source Current, $V_{IH} = 0.0V$ (Pull-up)	13.0	23	74		μA
I_{IL}	Chip Disable Input (S2559B)	Source Current, $V_{IL} = 3.5V$ (Pull-down)	3.5	4	10		μA
		Sink Current, $V_{IL} = 13.0V$ (Pull-down)	13.0	90	240		μA

S2559C & D Electrical Characteristics:

(Specifications apply over the operating temperature range of – 25°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			2.75		10.0	V
	Non Tone Out Mode (No Key Depressed)			2.5		10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		0.3	30	μA
			10.0		1.0	100	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		1.0	2.0	mA
			10.0		8	16.0	mA
	Tone Output						
V_{OR}	Single Tone Mode Output Voltage	Row Tone, $R_L = 390\Omega$	3.5	250	362	474	mVrms
			5.0	367	546	739	mVrms
		Row Tone, $R_L = 240\Omega$	10.0	350	580	730	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.0 – 10.0	1.75	2.54	3.75	dB
%DIS	Distortion*		3.0 – 10.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High (No Key Depressed)(Pin 2)	($I_{OH} = 15mA$)	3.0	1.5	1.8		V
		($I_{OH} = 50mA$)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, $V_{OF} = 0V$		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load		2.75		0	0.5	V
			10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed) No Load		2.75	2.5	2.75		V
			10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink Current	$V_{OL} = 0.5V$	3.0	0.53	1.3		mA
			10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source Current	$V_{OH} = 2.5V$	3.0	0.17	0.41		mA
		$V_{OH} = 9.5V$	10.0	0.57	1.5		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current One Key Selected	$V_{OL} = 0.5V$	3.0	0.21	0.52		mA
		$V_{OL} = 0.5V$	10.0	0.80	2.1		mA
I_{OH}	Output Source Current One Key Selected	$V_{OH} = 2.5V$	3.0	0.13	0.31		mA
		$V_{OH} = 9.5V$	10.0	0.42	1.1		mA

S2559C&D Electrical Characterics: (Continued)

Symbol	Parameter/Conditions		($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	$V_{IL} = 10.0V$	10.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	$V_{IH} = 0.0V$	10.0			1.0	μA
I_{IL}	Sink Current	$V_{IL} = 0.5V$	3.0	24	93		μA
	No Key Selected	$V_{IL} = 0.5V$	10.0	27	130		μA
t_{START}	Oscillator Startup Time		3.5		2	5	ms
			10.0		0.25	4	ms
$C_{I/O}$	Input/Output Capacitance		3.0		12	16	pF
			10.0		10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, $V_{IL} = 3.0V$ (Pull-down)	3.0		16		μA
		Sink Current $V_{IL} = 10.0V$ (Pull-down)	10.0		24		μA
I_{IH}		Source Current, $V_{IH} = 2.5V$ (Pull-up)	3.0		210		μA
		Source Current, $V_{IH} = 9.5V$ (Pull-up)	10.0		740		μA
I_{IH}	Mode Select Input (S2559C)	Source Current, $V_{IH} = 0.0V$ (Pull-up)	3.0	1.4	3.3		μA
		Source Current, $V_{IH} = 3.0V$ (Pull-up)	10.0	18	46		μA
I_{IL}	Chip Disable Input (S2559D)	Source Current, $V_{IL} = 3.0V$ (Pull-down)	3.0	3.9	9.5		μA
		Sink Current, $V_{IL} = 10.0V$ (Pull-down)	10.0	55	143		μA

*Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

Table 1. Comparisons of Specified vs Actual Tone Frequencies Generated by S2559

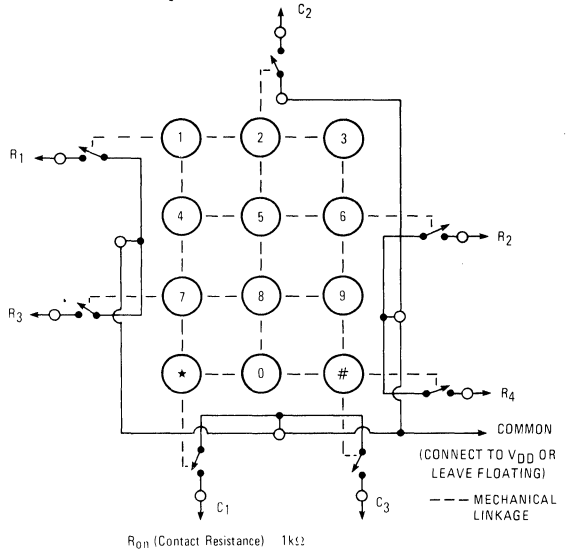
ACTIVE INPUT	OUTPUT FREQUENCY Hz		% ERROR SEE NOTE
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	−0.32
C3	1,477	1,417.9	−0.35
C4	1,633	1,645.0	+0.73

NOTE: % Error does not include oscillator drift.

Table 2. XMIT and MUTE Output Functional Relationship

OUTPUT RELEASED	'DIGIT' KEY DEPRESSED	'DIGIT' KEY	COMMENT
XMIT	V_{DD}	High Impedance	Can source at least 50mA at 10V with 1.5V max. drop
MUTE	V_{SS}	V_{DD}	Can source or sink current

Figure 1. Standard Telephone Push Button Keyboard



Circuit Description

The S2559 is designed so that it can be interfaced easily to the dual tone signaling telephone system and that it will more than adequately meet the recommended telephone industry specifications regarding the dual tone signaling scheme.

Design Objectives

The specifications that are important to the design of the DTMF Generator are summarized below: the dual tone signal consists of linear addition of two voice frequency signals. One of the two signals is selected from a group of frequencies called the "Low Group" and the other is selected from a group of frequencies called the "High Group". The low group consists of four frequencies 697, 770, 852 and 941 Hz. The high group consists of four frequencies 1209, 1336, 1477 and 1633 Hz. A keyboard arranged in a row, column format (4 rows x 3 or 4 columns) is used for number entry. When a push button corresponding to a digit (0 thru 9) is pushed, one appropriate row (R1 thru R4) and one appropriate column (C1 thru C4) is selected. The active row input selects one of the low group frequencies and the active column input selects one of the high group frequencies. In standard dual tone telephone systems, the highest high group frequency of 1633Hz (Col. 4) is not used. The frequency tolerance must be ±1.0%. However, the S2559 provides a better than .75% accuracy. The total harmonic and intermodulation distortion of the dual tone must be less than 10% as seen at the telephone terminals. (Ref. 1.) The high group to low group signal amplitude ratio should be 2.0 ±2dB and the absolute amplitude of the low group and high group tones must be within the allowed range. (Ref. 1.) These requirements apply when the telephone is used over a short loop or long loop and over the operating temperature range. The design of the S2559 takes into account these considerations.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSC_I and OSC_O terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

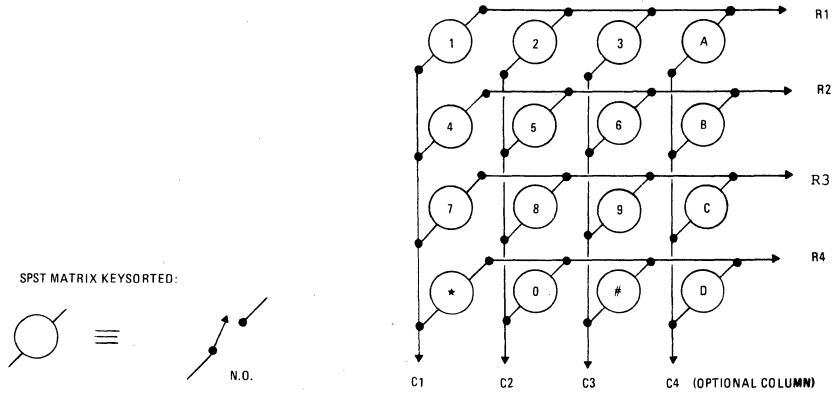
Keyboard Interface

The S2559 employs a calculator type scanning circuitry to determine key closures. When no key is depressed, active pull-down resistors are "on" on the row inputs and active pull-up resistors are "on" on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull-up or pull-down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The advantage of the scanning technique is that a keyboard arrangement of SPST switches are shown in Figure 2 without the need for a common line, can be used. Conventional telephone push button keyboards as shown in Figure 1 or X-Y keyboards with common can also be used. The common line of these keyboards can be left unconnected or wired "high".

Logic Interface

The S2559 can also interface with CMOS logic outputs directly. The S2559 requires active "High" logic levels. Since the active pull-up resistors present in the S2559 are fairly low value (500Ω typ), diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their "Low" state.

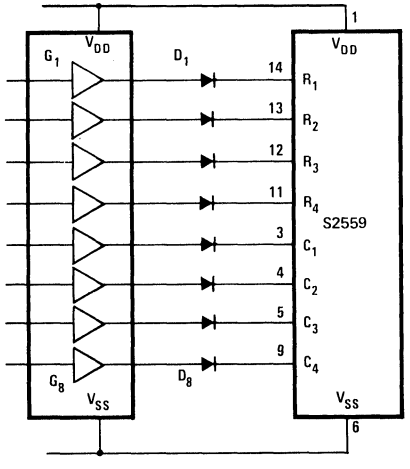
Figure 2. SPST Matrix Keyboard Arranged in the 2 of 8 Row, Column Format



Tone Generation

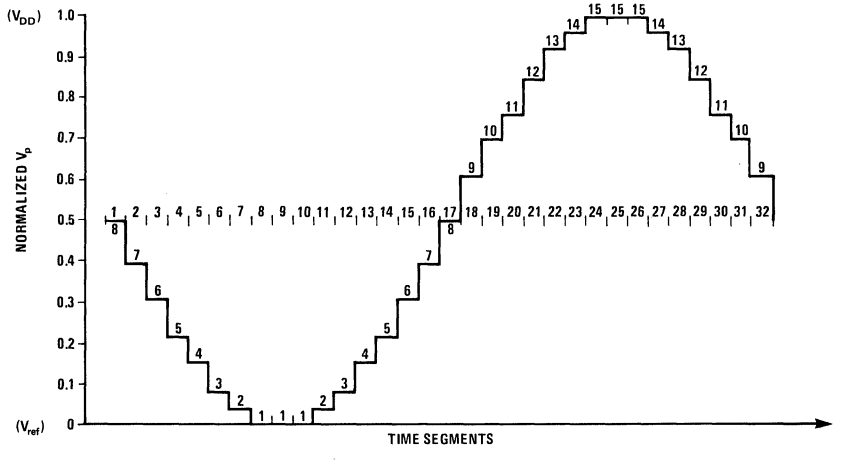
When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD} - V_{REF}$) of the stairstep function is fairly constant. V_{REF} is so chosen that V_P falls within the allowed range of the high group and low group tones.

Figure 3. Logic Interface for Keyboard Inputs of the S2559



G1 THRU G8 ANY TYPE CMOS GATE
D1 THRU D8 DIODES TYPE IN914 (OPTIONAL)

Figure 4. Stairstep Waveform of the Digitally Synthesized Sinewave



The individual tones generated by the sinewave synthesizer are then linearly added and drive a bipolar NPN transistor connected as emitter follower to allow proper impedance transformation, at the same time preserving signal level.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by activating the appropriate row input or by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Mode Select

S2559A and S2559C have a Mode Select (MDSL) input (Pin 15). When MDSL is left floating (unconnected) or connected to V_{DD}, both the dual tone and single tone modes are available. If MDSL is connected to V_{SS}, the single tone mode is disabled and no output tone is produced if an attempt for single tone is made. The S2559B and S2559D do not have the Mode Select option.

Chip Disable

The S2559B and S2559D have a Chip Disable input at Pin 15 instead of the Mode Select input. The chip disable for the S2559B and S2559D is active "high." When the chip disable is active, the tone output goes to V_{SS}, the row, column inputs go into a high impedance state, the oscillator is inhibited and the MUTE and XMIT outputs go into active states. The effect is the device essentially disconnects from the keyboard. This allows one keyboard to be shared among several devices.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ± 0.02%
$R_S \leq 100\Omega$, $L_M = 96MHY$
$C_M = 0.02pF$, $C_h = 5pF$

MUTE, XMIT Outputs

The S2559A, B, C, D have a CMOS buffer for the MUTE output and a bipolar NPN transistor for the XMIT output. With no keys depressed, the MUTE output is "low" and the XMIT output is in the active state so that substantial current can be sourced to a load. When a key is depressed, the MUTE output goes high, while the XMIT output goes into a high impedance state. When Chip Disable is "high" the MUTE output is forced "low" and the XMIT output is in active state regardless of the state of the keyboard inputs.

Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the Digital Tone Generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the Tone Output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 5 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 5 volts. The load resistor value also controls the amplitude. If R_L is low the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than 5kΩ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3581A) and amplitudes at the selected frequencies can be noted. This measurement also permits verification of the preemphasis between the individual frequency tones.

Distortion is defined as "the ratio of the **total** power of all extraneous frequencies in the **voiceband** above 500Hz accompanying the signal to the power of the frequency **pair**." This ratio must be less than 10% or when expressed in dB must be lower than – 20dB.

(Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

$$\text{Dist.} = \frac{\sqrt{(V_1)^2 + (V_2)^2 + \ldots + (V_N)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

where $(V_1) \ldots (V_N)$ are extraneous frequency (i.e., intermodulation and harmonic) components in the 500Hz to

3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$DIST_{dB} = 20 \log \frac{\sqrt{(V_1)^2 + (V_2)^2 + \ldots (V_N)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

$$= 10\{\log[(V_1)^2 + \ldots (V_N)^2] - \log[(V_L)^2 + (V_L)^2 + (V_H)^2]\} \ldots (1)$$

An accurate way of measuring distortion is to plot a spectrum of the signal by using a spectrum analyzer (H-P type 3580A) and an X-Y plotter (H-P type 7046A). Individual extraneous and signal frequency components are then noted and distortion is calculated by using the expression (1) above. Figure 6 shows a spectrum plot of a typical signal obtained from a S2559D device operating from a fixed supply of 4Vdc and $R_L = 10k\Omega$ in the test circuit of Figure 5. Mathematical analysis of the spectrum shows distortion to be – 30dB (3.2%). For quick estimate of distortion, a rule of thumb as outlined below can be used.

"As a first approximation distortion in dB equals the difference between the amplitude (dB) of the extraneous component that has the highest amplitude and the amplitude (dB) of the low frequency signal." This rule of thumb would give an estimate of – 28dB as distortion for the spectrum plot of Figure 6 which is close to the computed result of – 30dB.

In a telephone application amplitude and distortion are affected by several factors that are interdependent. For detailed discussion of the telephone application and other applications of the 2559 Tone Generator, refer to the applications note "Applications of Digital Tone Generator."

Ref. 1: Bell System Communications Technical Reference, PUB 47001, "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment," August 1976.

Figure 5. Test Circuit for Distortion Measurement

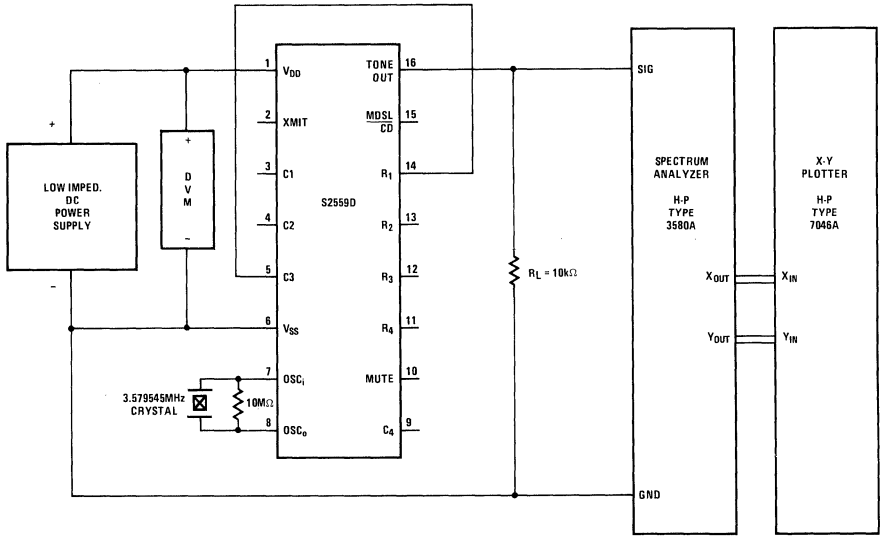
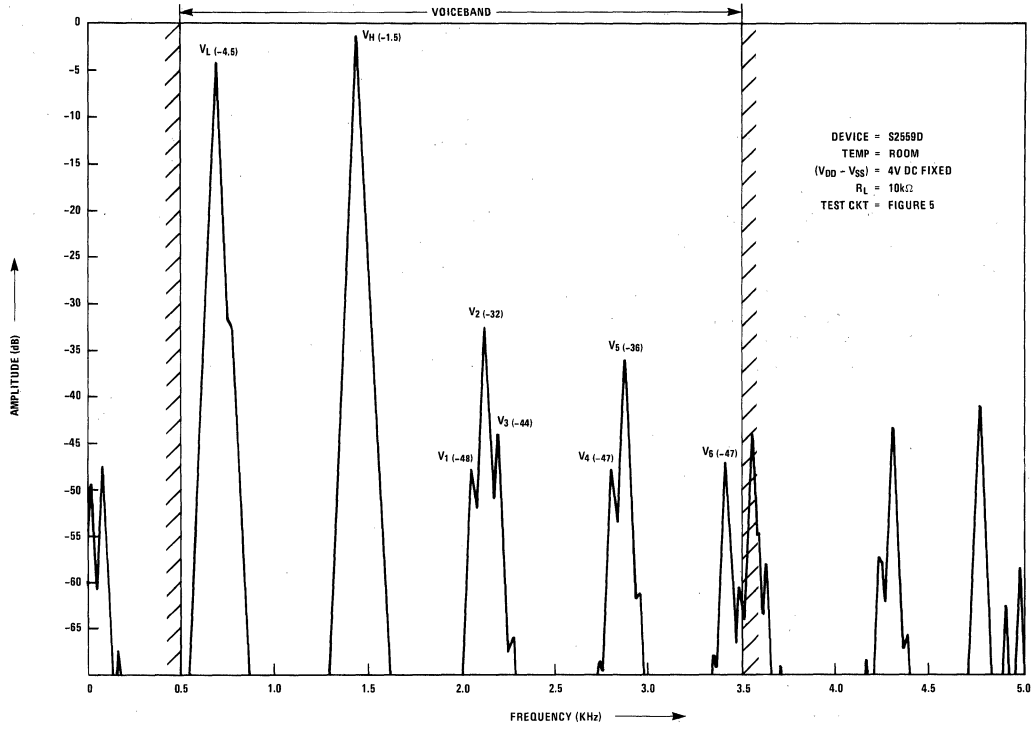


Figure 6. A Typical Spectrum Plot



Advanced Product Description **S2559E/F/G/H**

DTMF TONE GENERATOR

Features

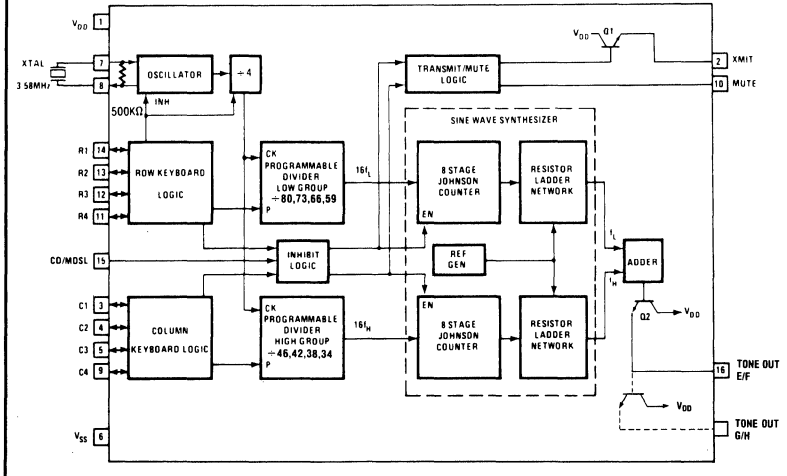
- ☐ Low Output Tone Distortion: 7%
- ☐ Wide Operating Supply Voltage Range: 2.5 to 10 Volts
- ☐ Oscillator Bias Resistor On-Chip
- ☐ Can be Powered Directly from Telephone Line or from Small Batteries
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- ☐ Four Options Available on Pin 15 and Pin 16:
  - Bipolar Output
    - E: Mode Select
    - F: Chip Disable
  - Darlington Output
    - G: Mode Select
    - H: Chip Disable

General Description

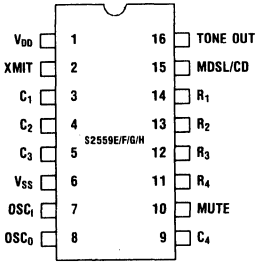
The S2559E, F, G and H are improved members of the S2559 Tone Generator Family. The new devices feature extended operating voltage range, lower tone distortion, and an on-chip oscillator bias resistor. The S2559E and F are pin and functionally compatible with the S2559C and D, respectively.

The S2559 G and H are identical to the E and F, except that there is a Darlington amplifier configuration on the tone out pin, rather than a single bipolar transistor as shown in the block diagram. In many applications this eliminates the need for a transistor in the telephone circuit. Tone distortion in the telephone is also likely to be lower.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... +10.5V
Operating Temperature ..... −0°C to +70°C
Storage Temperature ..... −30°C to +125°C
Power Dissipation at 25°C 1000mW
Digital Input ..... $V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$
Analog Input ..... $V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$

S2559E, F, G and H Electrical Characteristics:

(Specifications apply over the operating temperature range of 0°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				2.5		10.0	V
	Non Tone Out Mode (No Key Depressed)				1.6		10.0	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)			3.0		0.3	30	μA
				10.0		1.0	100	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)			3.0		1.0	2.0	mA
				10.0		8	16.0	mA
	Tone Output							
S2559E/F V_{OR}	Single Tone Mode Output Voltage	Row Tone,	$R_L = 390\Omega$	3.5	335	465	565	mVrms
				5.0	380	540	710	mVrms
		Row Tone,	$R_L = 240\Omega$	10.0	380	550	735	mVrms
S2559G/H V_{OR}	Single Tone Mode Output Voltage	Row Tone,	$R_L = 390\Omega$	4.0	110	315	495	mVrms
				5.0	340	540	675	mVrms
		Row Tone,	$R_L = 240\Omega$	10.0	415	590	770	mVrms
dB_{CR}	Ratio of Column to Row Tone (Dual Tone Mode)		2559E/F	3.5 – 10.0	1.0	2.0	3.0	dB
			2559G/H	4.0 – 10.0				
%DIS	Distortion*		2559E/F	3.5 – 10.0			7	%
			2559G/H	4.0 – 10.0			7	%
	XMIT, MUTE Outputs							
V_{OH}	XMIT, Output Voltage, High (No Key Depressed)(Pin 2)		($I_{OH} = 15mA$)	3.0	1.5	1.8		V
			($I_{OH} = 50mA$)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, $V_{OF} = 0V$			10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load			2.75		0	0.5	V
				10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed) No Load			2.75	2.5	2.75		V
				10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink Current		$V_{OL} = 0.5V$	3.0	0.53	1.3		mA
				10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source Current		$V_{OH} = 2.5V$	3.0	0.17	0.41		mA
			$V_{OH} = 9.5V$	10.0	0.57	1.5		mA

*Distortion is defined as "the ratio of the total power of all extraneous frequencies, in the VOICE and above 500Hz, to the total power of the DTMF frequency pair".

AMI

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S2859

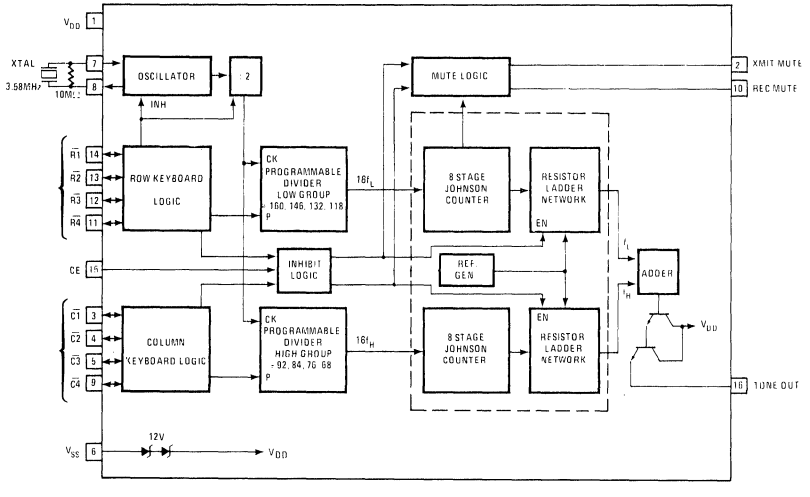
DTMF TONE GENERATOR

COMMUNICATIONS

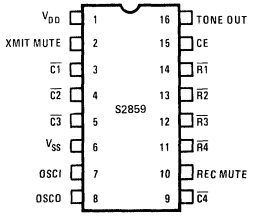
Features

- ☐ Wide Operating Supply Voltage Range: 3.0 to 10 Volts
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V
- ☐ Uses TV Crystal Standard (3.58 MHz) to Derive All Frequencies thus Providing Very High Accuracy and Stability
- ☐ Timing Sequence for XMIT, REC MUTE Outputs
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard with Common Terminal
- ☐ The Total Harmonic Distortion is Below Industry Specification
- ☐ On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range
- ☐ Single Tone as Well as Dual Tone Capability
- ☐ Darlington Configuration Tone Output

Block Diagram



Pin Configuration



General Description

The S2859 DTMF Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton telephone keyboard or X-Y keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2859 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, point-of-sale, and credit card verification terminals and process control.

Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD} - V_{SS}$)	+ 10.5V
Operating Temperature	0°C to + 70°C
Storage Temperature	− 55°C to + 125°C
Power Dissipation at 25°C	500mW
Input Voltage	$V_{SS} - 0.6 \leqslant V_{IN} \leqslant V_{DD} + 0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of − 0°C to + 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				3.0	—	10.0	V
	Non Tone Out Mode (Mute Outputs Toggle With Key Depressed)				2.2	—	10.0	V
V_Z	Internal Zener Diode Voltage, I_Z = 5mA			—	—	12.0	—	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone and Mute Outputs Unloaded)			3.0	—	0.001	0.3	mA
				10.0	—	0.003	1.0	mA
	Operating (One Key Selected, Tone and Mute Outputs Unloaded)			3.0	—	1.3	2.0	mA
				10.0	—	11	18	mA
	Tone Output							
V_{OR}	Single Tone Mode Output Voltage	Row	$R_L = 100\Omega$	5.0	366	462	581	mVrms
		Tone	$R_L = 100\Omega$	10.0	370	482	661	mVrms
dB_{CR}	Ratio of Column to Row Tone			3.0 − 10.0	1.0	2.0	3.0	dB
%DIS	Distortion*			3.0 − 10.0	—	—	10	%
	REC, XMIT MUTE Outputs							
I_{OH}	Output Source Current		$V_{OH} = 1.2V$	2.2	0.43	1.1	—	mA
			$V_{OH} = 2.5V$	3.0	1.3	3.1	—	mA
			$V_{OH} = 9.5V$	10.0	4.3	11	—	mA

*Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

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S2860

DTMF TONE GENERATOR

COMMUNI-CATIONS

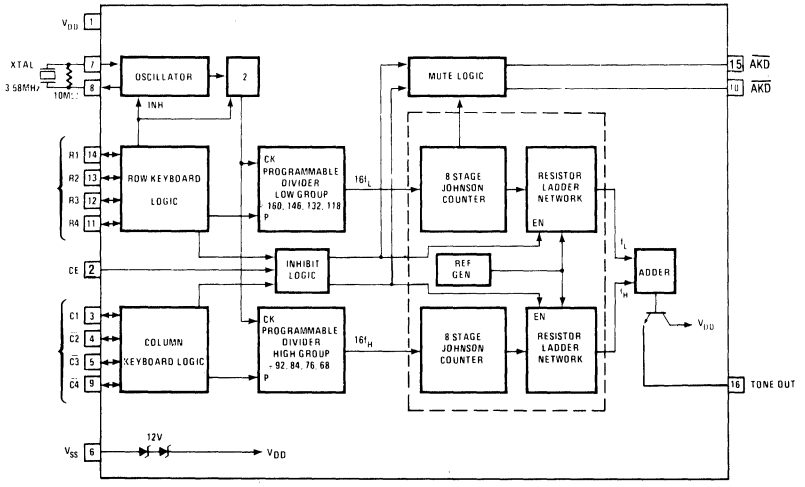
Features

- ☐ Optimized for Constant Operating Supply Voltages, Typically 3.5V
- ☐ Tone Amplitude Stability is Within ± 1.3dB of Nominal Over Operating Temperature Range
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries
- ☐ Uses TV Crystal Standard (3.58MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability
- ☐ Specifically Designed for Electronic Telephone Applications
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- ☐ The Total Harmonic Distortion is Below Industry Specification
- ☐ Single Tone as Well as Double Tone Capability

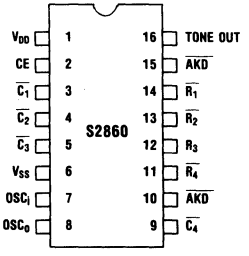
General Description

The S2860 DTMF Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard or X-Y keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very

Block Diagram



Pin Configuration



General Description (Continued)

low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$)	+ 10.5V
Operating Temperature	0°C to + 70°C
Storage Temperature	− 55°C to + 125°C
Power Dissipation at 25°C	500mW
Input Voltage	$V_{SS} - 0.6 \leq V_{IN} \leq V_{DD} + 0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of 0°C to + 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			3.0		10.0	V
	Non Tone Out Mode (AKD Outputs toggle with key depressed)			1.8			V
V_Z	Internal Zener Diode Voltage, $I_Z = 5mA$				12.0		V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone and AKD Outputs Unloaded)		3.5 10.0		1 5	20 100	μA μA
	Operating (One Key Selected, Tone and AKD Outputs Unloaded)		3.5 10.0		0.9 3.6	1.25 5	mA mA
	Tone Output						
V_{OR}	Single Tone Mode Output Row Tone,	$R_L = 10k\Omega$	3.5	305	350	412	mVrms
		$R_L = 1k\Omega$	3.5	272	350	412	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.0 – 10.0	1.0	2.0	3.0	dB
%DIS	Distortion*		3.0 – 10.0			10	%
	AKD Outputs						
I_{OL}	Output Sink Current	$V_{OL} = .7V$	3.5	0.1	1.0		mA
	Oscillator Input/Output						
I_{OL}	One Key Selected Output Sink Current	$V_{OL} = 0.5V$	3.0	0.21	0.52		mA
		$V_{OL} = 0.5V$	10.0	0.80	2.1		mA
I_{OH}	Output Source Current One Key Selected	$V_{OH} = 2.5V$	3.0	0.13	0.31		mA
		$V_{OH} = 9.5V$	10.0	0.42	1.1		mA
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	$V_{IL} = 10.0V$	10.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	$V_{IH} = 0.0V$	10.0			1.0	μA
I_{IL}	Sink Current	$V_{IL} = 0.5V$	3.0	24	58		μA
	No Key Selected	$V_{IL} = 0.5V$	10.0	27	66		μA

*Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		$(V_{DD} - V_{SS})$ Volts	Min.	Typ.	Max.	Units
t_{START}	Oscillator Startup Time		3.0		2	5	ms
$C_{I/O}$	Input/Output Capacitance		3.0		12	16	pF
			10.0		10	14	pF
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low			$V_{SS} - 0.6$		$.2(V_{DD} - V_{SS})$	V
V_{IH}	Input Voltage, High			$8.(V_{DD} - V_{SS})$		$V_{SS} + 0.6$	V
I_{IH}	Input Current,	$V_{IH} = 0.0V$	3.0	20	60	100	μA
	(Pull up)	$V_{IH} = 0.0V$	10.0	66	200	336	μA

Oscillator

The S2860 contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSC_I and OSC_O terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Crystal Specification

A Standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ± 0.02%

$R_S \leqslant 100\Omega$, $L_M = 96MHY$

$C_M = 0.02pF$, $C_h = 5pF$

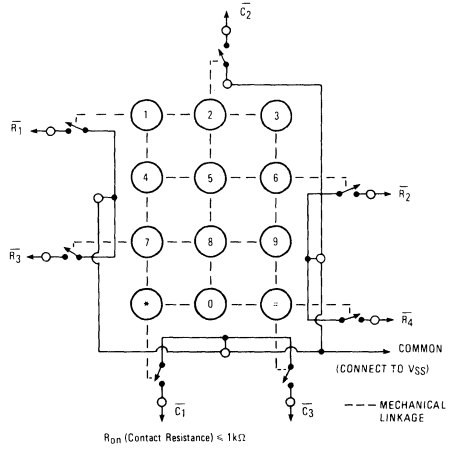
Keyboard Interface

The S2860 can interface with either the standard telephone pushbutton keyboard (see Figure 1) or an X-Y keyboard with common. The common of the keyboard must be connected to V_{SS}.

Logic Interface

The S2860 can also interface with CMOS logic outputs directly. (See Figure 2.) The S2860 requires active "LOW" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 33kΩ–150kΩ.

Figure 1. Standard Telephone Push Button Keyboard



Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step wave form to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder

S2560A

PULSE DIALER

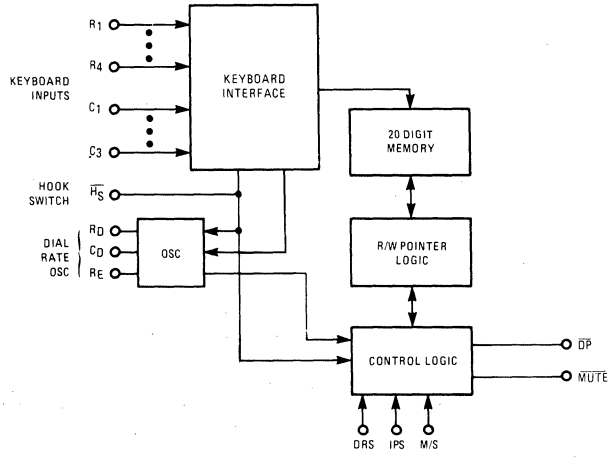
Features

- ☐ Low Voltage CMOS Process for Direct Operation from Telephone Lines
- ☐ Inexpensive R-C Oscillator Design Provides Better than ± 5% Accuracy Over Temperature and Unit to Unit Variations
- ☐ Dialing Rate Can be Varied by Changing the Dial Rate Oscillator Frequency
- ☐ Dial Rate Select Input Allows Changing of the Dialing Rate by a 2:1 Factor Without Changing Oscillator Components
- ☐ Two Selections of Mark/Space Ratios (33⅓/66⅔ or 40/60)
- ☐ Twenty Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Mute and Dial Pulse Drivers on Chip
- ☐ Accepts DPCT Keypad with Common Arranged in a 2 of 7 Format; Also Capable of Interface to SPST Switch Matrix

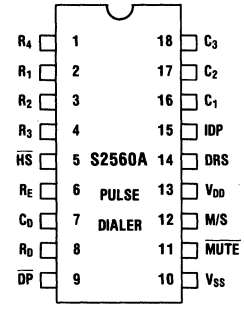
General Description

The S2560A Pulse Dialer is a CMOS integrated circuit that converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone lines with minimum interface. Storage is provided for 20 digits, therefore, the last dialed number is available for redial until a new number is entered. IDP is scaled to the dialing rate such as to produce smaller IDP at higher dialing rates. Additionally, the IDP can be changed by a 2:1 factor at a given dialing rate by means of the IDP select input.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leqslant V_{DD} - V_{SS} \leqslant 3.5V$ unless otherwise specified.

Symbol	Parameter	V_{DD}-V_{SS} (Volts)	Min.	Max.	Units	Conditions
	Output Current Levels					
I_{OLDP}	DP Output Low Current (Sink)	3.5	125		µA	V_{OUT} = 0.4V
I_{OHDP}	DP Output High Current (Source)	1.5 3.5	20 125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	MUTE Output Low Current (Sink)	3.5	125		µA	V_{OUT} = 0.4V
I_{OHM}	MUTE Output High Current (Source)	1.5 3.5	20 125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLT}	Tone Output Low Current (Sink)	1.5	20		µA	V_{OUT} = 0.4V
I_{OHT}	Tone Output High Current (Source)	1.5	20		µA	V_{OUT} = 1V
V_{DR}	Data Retention Voltage		1.0		V	"On Hook" $\overline{HS}$ = V_{DD}. Keyboard open, all other input pins to V_{DD} or V_{SS}
I_{DD}	Quiescent Current	1.0		750	nA	
I_{DD}	Operating Current	1.5 3.5		100 500	µA µA	$\overline{DP}$, $\overline{MUTE}$ open, $\overline{HS}$ = V_{SS} ("Off Hook") Keyboard processing and dial pulsing at 10 pps at conditions as above
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	1.5 to 2.5 2.5 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50K\Omega \leqslant R_D \leqslant 750K\Omega$; $100pF \leqslant C_D{}^* \leqslant 1000pF$; $750k\Omega \leqslant R_E \leqslant 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD}-V_{SS}$)	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of ($V_{DD}-V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leqslant V_I \leqslant V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded. When power is first applied to the device, the device should be in "On Hook" condition ($\overline{HS}$ = 1). This is necessary because there is no internal power or reset on chip and for proper operation all internal latches must come up in a known state. In applications where the device is hard wired in "Off Hook" ($\overline{HS}$ = 0) condition, a momentary "On Hook" condition can be presented to the device during power up by use of a capacitor resistor network as shown in Figure 6.

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

The device contains an oscillator circuit that requires three external components: two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including the "on hook" condition. For a dialing rate of 10pps the oscillator should be adjusted to 2400Hz. Typical values of external components for this are R_D and $R_E = 750k\Omega$ and $C_D = 270pF$. It is recommended that the tolerance of resistors to be 5% and capacitor to be 1% to insure a 10% tolerance of the dialing rate in the system.

Keyboard Interface (S2560A)

The S2560A employs a scanning technique to determine a key closure. This permits interface to a DPCT keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2) and interface to a SPST switch matrix (Figure 7). A high level on the appropriate row and column inputs constitutes a key closure for logic interface. When using a SPST switch matrix, it is necessary to add small capacitors (30pF) from the column inputs to V_{SS} to insure that the oscillator is shut off after a key is released or after the dialing is complete.

OFF Hook Operation: The device is continuously powered through a 150kΩ resistor during Off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The $\overline{DP}$ output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during the pulse break. The $\overline{MUTE}$ output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

ON Hook Operation: The device is continuously powered through a 10-20MΩ resistor during the ON hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20pps can be achieved. Dialing rates of 7 and 14pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14pps, IDP's of 1143ms and 572ms can be similarly obtained. If the IDP select is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10pps an IDP of 800ms is obtained and at 20pps an IDP of 400ms is obtained.

The user can enter a number up to 20 digits long from a standard 3x4 double contact keypad with common (Figure 1). It is also possible to use a logic interface as shown in Figure 2 for number entry. Antibounce protection circuitry is provided on chip (min. 20ms) to prevent false entry.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed twenty.

Auto Dialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

Table 1. S2560A/S2560B Pin/Function Descriptions

Pin	Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	2, 3, 4, 1, 16, 17, 18	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 2. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 20ms).
Inter-Digit Pause Select (IDP)	15	One programmable line is available that allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceding the first dialed pulse is an inter-digit time equal to the selected IDP. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Dial Rate Select (DRS)	14	A programmable line allows selection of two different output rates such as 7 or 14 pps, 10 or 20 pps, etc. See Tables 2 and 3.
Mark/Space (M/S)	12	This input allows selection of the mark/space ratio, as per Table 3.
Mute Out ($\overline{MUTE}$)	11	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.
Dial Pulse Out ($\overline{DP}$)	9	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator (R_E, C_D, R_D)	6, 7, 8	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	5	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	13, 10	These are the power supply inputs. The device is designed to operate from 1.5V–3.5V.

Figure 1. Standard Telephone Pushbutton Keyboard

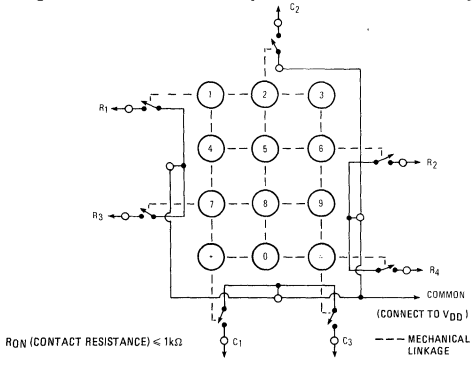


Figure 2. Logic Interface for the S2560

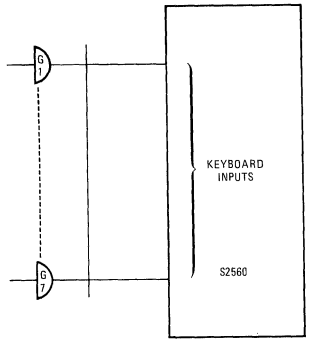


Figure 3. Timing

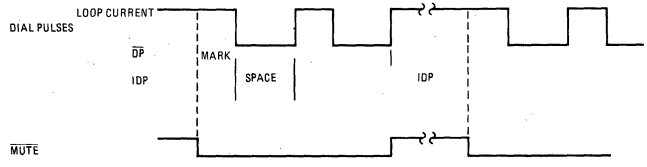


Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)	
					DRS = V_{SS}	DRS = V_{DD}	IPS = V_{SS}	IPS = V_{DD}
5.5/11	1320				5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680	Select components in the ranges indicated in table of electrical specifications			7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920				8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
$(f_d/240)/(f_d/120)$	f_d				$(f_d/240)$	$(f_d/120)$	$\frac{1920}{f_i}\times10^3$	$\frac{960}{f_i}\times10^3$

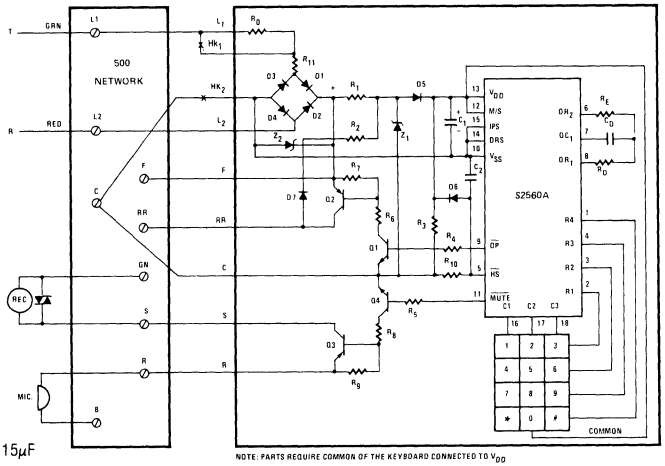
NOTE: IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14pps, and IDP of either 1142ms or 571ms can be selected.

Table 3.

Function	Pin Designation	Input Logic Level	Selection
Dial Pulse Rate Selection	DRS (14)	V_{SS} V_{DD}	(f/240)pps (f/120)pps
Inter-Digit Pause Selection	IDP (15)	V_{DD} V_{SS}	$\frac{960}{f}$ s $\frac{1920}{f}$ s
Mark/Space Ratio	M/S (12)	V_{SS} V_{DD}	33⅓/66⅔ 40/60
On Hook/Off Hook	$\overline{HS}$ (5)	V_{DD} V_{SS}	On Hook Off Hook

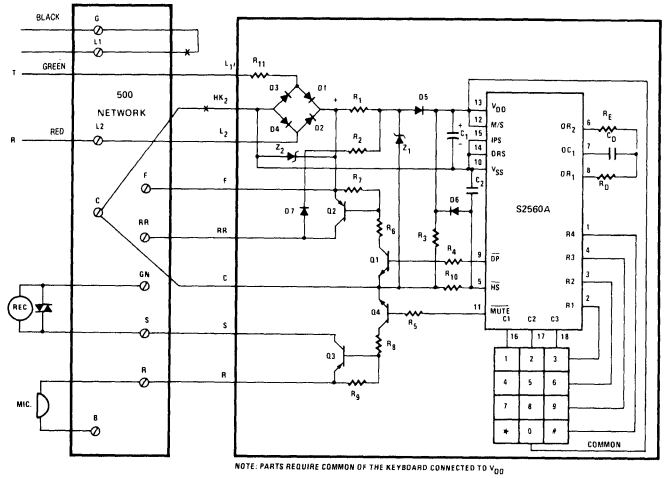
NOTE: f is the oscillator frequency and is detemined as shown in Figure 5.

Figure 4. Pulse Dialer Circuit with Redial



R_0 = 10-20MΩ, R_1 = 150kΩ, R_2 = 2kΩ
R_3 = 470kΩ, R_4, R_5 = 10kΩ, R_{10} = 47kΩ
R_6, R_8 = 2kΩ, R_7, R_9 = 30kΩ, R_{11} = 20Ω, 2W
Z_1 = 3.9V, D_1—D_4 = IN4004, D_5, D_6, D_7 = IN914, C_1 = 15μF
R_E = R_D = 750kΩ, C_D = 270pF, C_2 = 0.01μF
Q_1, Q_4 = 2N5550 TYPE Q_2, Q_3 = 2N5401 TYPE
Z_2 = IN5379 110V ZENER OR 2XIN4758

Figure 5. Pulse Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



R_1 = 10-20MΩ, R_2 = 2kΩ
R_3 = 470kΩ, R_4, R_5 = 10kΩ
R_6, R_8 = 2kΩ, R_7, R_9 = 30kΩ
R_{10} = 47kΩ, R_{11} = 20Ω, 2W
Z_1 = 3.9V, D_1—D_4 = IN4004
D_5, D_6, D_7 = IN914, C_1 = 15μF
R_E, R_D = 750kΩ, C_D = 270pF
C_2 = 0.01μF, Q_1, Q_4 = 2N5550
Q_2, Q_3 = 2N5401
Z_2 = 150V ZENER OR VARISTOR TYPE GE MOV150

Figure 6. Circuit for Applying Momentary "ON Hook" Condition During Power Up

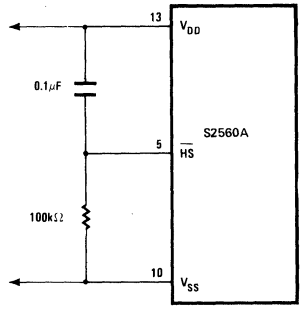
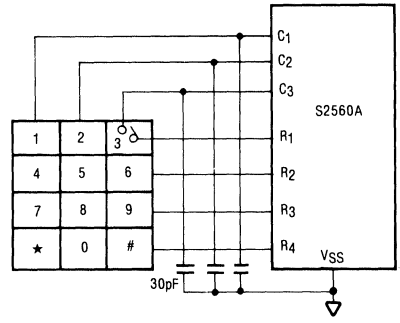


Figure 7. SPST Switch Matrix Interface



Advanced Product Description

S2560G

PULSE DIALER

General Description

The S2560G is a modified version of the S2560A Pulse Dialer with complete pin/function compatibility. It is recommended to be used in all new and existing designs. Most electrical specifications for both devices are identical. Please refer to S2560A data sheet for details.

Differences between the two devices are summarized below:

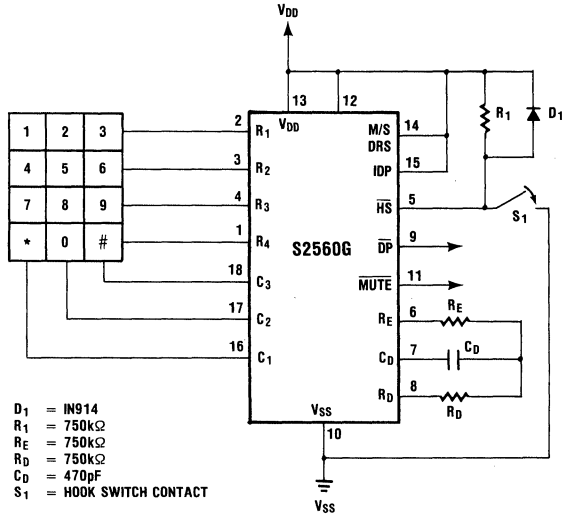
	2560G	**2560A**
Operating Voltage, Dialing:	2.0V to 3.5V	1.5V to 3.5V
Operating Voltage, Voice Mode:	1.5V to 3.5V	1.5V to 3.5V
Data Retention Voltage (Minimum):	1.0V	1.0V
I_{DD} Operating Current:	200μA@2.0V 1000μA@3.5V	100μA@1.5V 500μA@3.5V
I_{DD} Standby Current:	2μA@1V	750nA@1V
Keyboard Debounce Time:	10msec	16msec
X-Y Keyboard Interface:	Does not need capacitors	Capacitors required between column inputs and V_{SS}
Redial Buffer:	22 digits	20 digits
Dialing Characteristics:	Can dial more than 22 digits. Redial disabled if more than 22 digits are entered.	Accepts a maximum of 20 digits. Will not dial additional digits.

Application Suggestions

1) In most existing designs, the S2560G will work in place of S2560A without any modifications. Problems may arise however, if the keyboard bounce time exceeds 10ms. In such a case, the device may interpret a single key entry as a double key. To avoid this false detection, the keyboard debounce time can be easily increased from 10ms to 20ms by changing the Oscillator Frequency from 2400Hz down to 1200Hz. This is done by changing the value of the capacitor connected to pin 7 from 270pF to 470pF. To preserve the dialing rate at 10pps and IDP at 800ms the DRS and IDP pins now must be connected to V_{DD} instead of V_{SS}. Figure 1 shows the implementation details. Note, that interfacing with X-Y keyboard no longer requires capacitors to V_{SS} from column pins.

2) The hookswitch input pin (pin 5) must be protected from spikes that can occur when the phone goes from off-hook condition to on-hook. Voltage exceeding V_{DD} on this pin can cause the device to draw excessive current. This will discharge the capacitor across V_{DD} and V_{SS} causing the supply voltage to drop. If the voltage drops below 1 volt (data retention voltage) the device could lose redial memory. To prevent the voltage on the hookswitch pin from exceeding V_{DD}, an external diode must be added on the hookswitch pin as shown in Figure 1.

Figure 1.


VDD
13
12
R1
D1
1 2 3
4 5 6
7 8 9
* 0 #
2
3
4
1
18
17
16
R1
R2
R3
R4
C3
C2
C1
VDD
S2560G
VSS
10
M/S
DRS
IDP
HS
DP
MUTE
RE
CD
RD
14
15
5
9
11
6
7
8
S1
D1 = IN914
R1 = 750kΩ
RE = 750kΩ
RD = 750kΩ
CD = 470pF
S1 = HOOK SWITCH CONTACT

A Subsidiary of Gould Inc.

Advanced Product Description | **S2561/S2561A/S2561C**

TONE RINGER

COMMUNICATIONS

Features

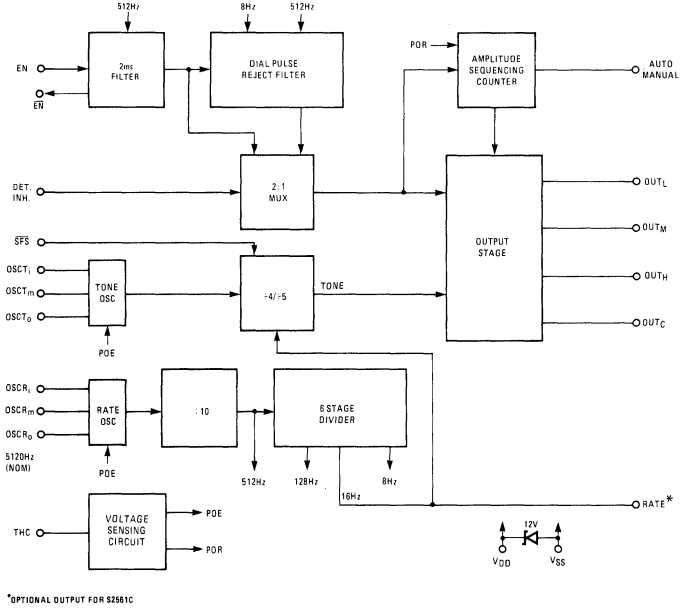
- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- ☐ Also Capable of Logic Interface for Non-Telephone Applications
- ☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
- ☐ 50mW Output Drive Capability at 10V Operating Voltage
- ☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- ☐ Single Frequency Tone Capability

General Description

The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

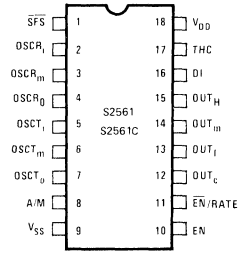
Data Subject to change at any time without notice. These sheets transmitted for information only.

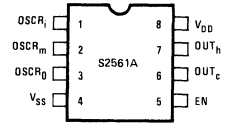
Block Diagram



*OPTIONAL OUTPUT FOR S2561C

Pin Configuration





Absolute Maximum Ratings:

Supply Voltage	+12.0V*
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

*This device incorporates a 12V internal zener diode across the VDD to VSS pins. Do NOT connect a low impedance power supply directly across the device unless the supply voltage can be maintained below 12V or current limited to <25mA.

Electrical Characteristics:

Specifications apply over the operating temperature and $3.5V \leqslant V_{DD}$ to $V_{SS} < 12.0V$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{DS}	Operating Voltage (V_{DD} to V_{SS})	8.0	12.0	V	Ringing, THC pin open
V_{DS}	Operating Voltage	4.0		V	"Auto" mode, non-ringing
I_{DS}	Operating Current		500	μA	Non-ringing, V_{DD} = 10V, THC pin open, DI pin open or V_{SS}
I_{OHC}	Output Drive Output Source Current (OUT_H, OUT_C outputs)	5		mA	V_{DD} = 10V, V_{OUT} = 8.75V
I_{OLC}	Output Sink Current (OUT_H, OUT_C outputs)	5		mA	V_{DD} = 10V, V_{OUT} = 0.75V
I_{OHM}	Output Source Current (Out_M output)	2		mA	V_{DD} = 10V, V_{OUT} = 8.75V
I_{OLM}	Output Sink Current (OUT_M output)	2		mA	V_{DD} = 10V, V_{OUT} = 0.75V
I_{OHL}	Output Source Current (OUT_L output)	1		mA	V_{DD} = 10V, V_{OUT} = 8.75V
I_{OLL}	Output Sink Current (OUT_L output)	1		mA	V_{DD} = 10V, V_{OUT} = 0.75V
	CMOS to CMOS				
V_{IH}	Input Logic "1" Level	0.7 V_{DD}	V_{DD} + 0.3	V	All inputs
V_{IL}	Input Logic "0" Level	V_{SS} − 0.3	0.3 V_{DD}	V	All inputs
V_{OHR}	Output Logic "1" Level (Rate output)	0.9 V_{DD}		V	I_O = 10μA (Source)
V_{OLR}	Output Logic "0" Level (Rate output)		0.5	V	I_O = 10μA (Sink)
V_{OZ}	Output Leakage Current (OUT_H, OUT_M outputs in high impedance state)		1 1	μA μA	V_{DD} = 10V, V_{OUT} = 0V V_{DD} = 10V, V_{OUT} = 10V
C_{IN}	Input Capacitance		7.5	pF	Any pin
Δfo/fo	Oscillator Frequency Deviation	−5	+5	%	Fixed RC component values $1M\Omega \leqslant R_{ri}$, $R_{ti} \leqslant 5M\Omega$; $100k\Omega \leqslant R_{rm}$, $R_{tm} \leqslant 750k\Omega$; $150pF \leqslant C_{ro}$, $C_{to} \leqslant 3000pF$; 330pF recommended value of C_{ro} and C_{to}, supply voltage varied from 9V ± 2V (over temperature and unit-unit variations)
R_{LOAD}	Output Load Impedance Connected Across OUT_H and OUT_C	600		Ω	Tone Frequency Range = 300Hz to 3400Hz
I_{IH}, I_L	Leakage Current, $V_{IN} = V_{DD}$ or V_{SS}		100	nA	Any input, except DI pin V_{DD} = 10V
V_{TH}	POE Threshold Voltage	6.5	8	V	
V_Z	Internal Zener Voltage	11	13	V	I_Z = 5mA

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leqslant V_I \leqslant V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

Functional Description

The S2561 is a CMOS device capable of simulating the effects of the telephone bell. This is achieved by producing a tone that shifts between two predetermined frequencies (512 and 640Hz) with a frequency ratio of 5:4 at a 16Hz rate.

Tone Generation: The output tone is derived from a tone oscillator that uses a 3 pin R-C oscillator design consisting of one capacitor and two resistors. The oscillator frequency is divided alternately by 4 or 5 at the shift rate. Thus, with the oscillator adjusted for 5120Hz, a tone signal is produced that alternates between 512Hz and 640Hz at the shift rate. The shift rate is derived from another 3 pin R-C oscillator which is adjusted for a nominal frequency of 5120Hz. It is divided down to 16Hz which is used to produce the shift in the tone frequency. It should be noted that in the special case where both oscillators are adjusted for 5120Hz, it is only necessary to have one external R-C network for one oscillator with the other oscillator driven from it. The oscillators are designed such that for fixed R-C component values an accuracy of ± 5% can be obtained over the operating supply voltage, temperature and unit-unit variations. See Table 1 for component and frequency selections. In the single frequency mode, activated by connecting the $\overline{SFS}$ input to V_{SS} only the higher frequency continuous tone is produced by using a fixed divider ratio of 4 and by disabling the shift operation.

Ring Signal Detection: In the following description it is assumed that both the tone and rate oscillators are adjusted for a frequency of 5120Hz. Ringing signal (nominally 42 to 105 VAC, 20Hz, 2 sec on/4 sec off duty cycle) applied by the central office between the telephone line pair is capacitively coupled to the tone ringer circuitry as shown in Figure 2. Power for the device is derived from the ringing signal itself by rectification (diodes D1 thru D4) and zener diode clamping (Z_2). The signal is also applied to the EN input after limiting and clamping by a resistor (R_2) and internal diodes to V_{DD} and V_{SS} supplies. Internally the signal is first squared up and then processed thru a 2ms filter followed by a dial pulse reject filter. The 2ns filter is a two-stage register clocked by a 512Hz signal derived from the rate oscillator by a divide by 10 circuit. The squared ring signal (typically a square wave) is applied to the D input of the first stage and also to reset inputs of both stages. This provides for rejection of spurious noise spikes. Signals exceeding a duration of 2ms only can pass through the filter. The dial pulse reject filter is clocked at 8Hz derived from the rate oscillator by divide by 640 circuit. This circuit is designed to pass any signal that has at least two transitions in a given 125ms time period. This insures that signals below 8Hz will be rejected with certainty. Signals over 16Hz will be passed with certainty and between 8Hz and 16Hz there is a region of uncertainty. By adjusting the rate oscillator to a different frequency the break points of 10Hz and 20Hz the rate oscillator can be adjusted to 6400Hz. Of course this also increases the tone shift rate to 20Hz. The action of the dial pulse reject filter minimizes the dial pulse interference during dialing although it does not completely eliminate it due to the rather large region of uncertainty associated with this type of discrimination circuitry. The dial pulse filter also has the characteristic that an input signal is not detected unless its duration exceeds 125ms. This insures that the tone ringer will not respond to momentary bursts of ringing less than 125 milliseconds in duration (Ref. 1).

In logic interface applications, the 2ms filter and the dial pulse reject filter can be inhibited by wiring the Det. INHIBIT pin to V_{DD}. This allows the tone ringer to be enabled by a logic '1' level applied at the "ENABLE" input without the necessity of a 20Hz ring signal.

Voltage Sensing: The S2561 contains a voltage sensing circuit that enables the output stage and the rate and tone oscillators, only when the supply voltage exceeds a predetermined value. Typical value of this threshold is 7.3 volts. This prduces two benefits. First, it insures that the audible intensity of the output tone is fairly constant throughout the ringing period; and secondly, it insures proper circuit operation during the "auto" mode operation by reducing the power consumption to a minimum when the supply voltage drops below 7.3 volts. This extends the supply voltage decay time beyond 4 seconds (off period of the ring signal) with an adequate filter capacitor and insures the proper functioning of the "amplitude sequencing" counter. It is important to note that the operating supply voltage should be well above the threshold value during the ringing period and that the filter capacitor should be large enough so that the ripple on the supply voltage does not fall below the threshold value. A supply voltage of 10 to 12 volts is recommended.

In applications where the tone ringer is continuously powered and below the threshold level, the internal threshold can be bypassed by connecting the THC pin to V_{DD}. The internal threshold can also be reduced by

connecting an external zener diode between the THC and V_{DD} pins.

Auto Mode: In the "auto" mode, activated by wiring the "auto/manual" input to V_{SS}, an amplitude sequencing of the output tone can be achieved. Resistors R_L and R_M are inserted in series with the Out_L and Out_M outputs, respectively, and paralleled with the Out_H output (Figure 1). Load is connected across Out_H and Out_C pins. R_L is chosen to be higher than R_M. In this manner the first ring is of the lowest amplitude, second ring is of medium amplitude and the third and consecutive rings thereafter are at maximum amplitude. For the proper functioning of the "amplitude sequencing" counter the device must have at least 4.0 volts across it throughout the ring sequence. The filter capacitor is so chosen that the supply voltage will not drop below 4.0 volts during the off period. At the end of a ring sequence when the off period substantially exceeds the 4 second duration, the counter will be reset. This will insure that the amplitude sequencing will start correctly beginning a new ring sequence. The counter is held in reset during the "manual" mode operation. This produces a maximum ring amplitude at all times.

Figure 1-A. Output Stage Connected for Auto Mode Operation

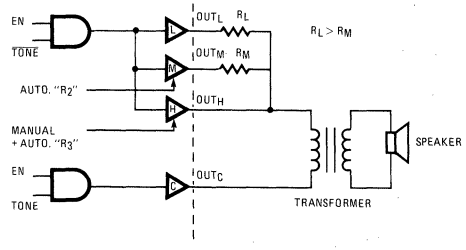


Figure 1-B. Output Stage Connected for Manual Mode Operation

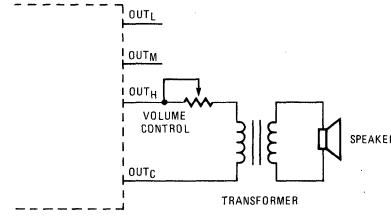
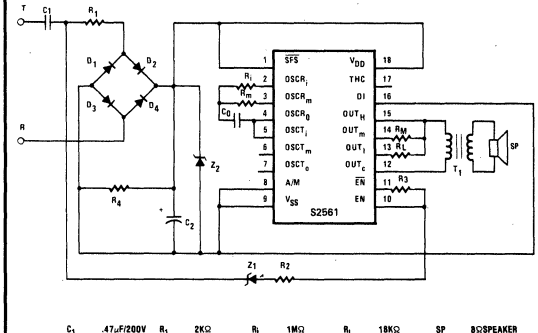
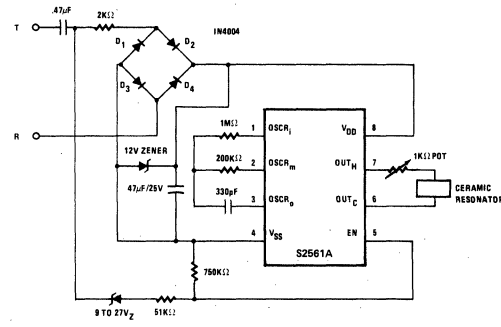


Figure 2-A. Typical Telephone Application of the S2561



C_1	.47μF/200V	R_1	2KΩ	R_i	1MΩ	R_L	18KΩ	SP	8ΩSPEAKER
C_2	47μF/25V	R_2	51KΩ	R_m	200KΩ	R_M	3.3KΩ	T_1	2000Ω/8ΩXFMR
D_1–D_4	IN4004	R_3	10MΩ	C_0	300pF	R_4	100KΩ	Z_1	9 TO 27V ZENER
Z_2	IN4742 12V ZENER								

Figure 2-B. Typical Telephone Application of the S2561A



Output Stage: The output stage is of push-pull type consisting of buffers L, M, H and C. The load is connected across pins Out_H and Out_C (Figure 2). During ringing, the Out_H and Out_C outputs are out of phase with each other and pulse at the tone rate. During a non-ringing state, all outputs are forced to a known level such as ground which insures that there is no DC component in the load. Thus, direct coupling can be used for driving the load. The major benefit of the push-pull arrangement is increased power output. Four times as much power can be delivered to the load for the same operating voltage. Buffers M and H are three-state. In the "auto" mode buffer M is active only during the second ring and in the "high impedance" state at all other times. Buffer H is active beginning the third ring. In the "manual" mode buffers H, L and C are active at all times while buffer M is in a high impedance state. The output buffers are so designed that they can source or sink 5mA at a V_{DD} of 10 volts without appreciable voltage drop. Care has been taken to make them symmetrical in both source and sink configurations. Diode clamping is provided on all outputs to limit the voltage spikes associated with transformer drive in both directions V_{DD} and V_{SS}.

Normal protection circuits are present on all inputs.

Table 1. S2561/S2561C Pin/Function Descriptions

Pin	Number	Function
Power (V_{DD}*, V_{SS}*)	2	These are the power supply pins. The device is designed to operate over the range of 3.5 to 12.0 volts. A range of 10 to 12 volts is recommended for the telephone application.
Ring Enable (EN*, $\overline{EN}$)	2	These pins are for the 20Hz ring enable input. They can also be used for DC level enabling by wiring the DI pin to V_{DD}. $\overline{EN}$ is available for the S2561 only.
Auto/Manual (A/M)	1	"Auto" mode for amplitude sequencing is implemented by wiring this pin to V_{SS}. "Manual" mode results when connected to V_{DD}. The amplitude sequencing counter is held in reset during the "manual" mode.
Outputs (Out_L, Out_M, Out_H^*, Out_C^*	4	These are the push-pull outputs. Load is directly connected across Out_H and Out_C outputs. In the "auto" mode, resistors R_L and R_M can be inserted in series with the Out_L and Out_M outputs for amplitude sequencing (see Figure 1).
Oscillators Rate Oscillator ($OSCR_i^*$, $OSCR_m^*$ $OSCR_o^*$)	3	These pins are provided to connect external resistors RR_i, RR_m and capacitor CR_o to form an R-C oscillator with a nominal frequency of 5120Hz. See Table 2 for components selection.
Tone Oscillator ($OSCT_i$, $OSCT_m$, $OSCT_o$)	3	These pins are provided to connect external resistors RT_i, RT_m and capacitor CT_o to form an R-C oscillator from which the tone signal is derived. With the oscillator adjusted to 512Hz and 640Hz results. See Table 2 for components selection.
Threshold Control (THC)	1	The internal threshold voltage is brought out to this pin for modification in non-telephone applications. It should be left open for telephone applications. For power supplies less than 9V connect to V_{DD}.
Rate	1	This is an optional output for the S2561C version which replaces the EN output. This is a 16Hz output that can be used by external logic as shown in Figure 3-A to produce a 2sec on/4sec off waveform.

Table 1. (Continued)

Pin	Number	Function
Rate	1	This is an optional output for the S2561C version which replaces the $\overline{EN}$ output. This is a 16Hz output that can be used by external logic as shown in Figure 3-A to produce a 2sec on/4sec off waveform.
Detector Inhibit (DI)	1	When this pin is connected to V_{DD}, the dial pulse reject filter is disabled to allow DC level enabling of the tone ringer. This pin should be hardwired to V_{SS} in normal telephone-type applications.
Single Frequency Select (SFS)	1	When this pin is connected to V_{SS}, only a single frequency continuous tone is produced as long as the tone ringer is enabled. In normal applications this pin should be hardwired to V_{DD}.
	$\overline{18}$	

*Pinouts of 8 pin S2561A package.

Table 2. Selection Chart for Oscillator Components and Output Frequencies

Tone/Rate Oscillator Frequency (Hz)	Oscillator Components R_I (kΩ)	R_M (kΩ)	C_O (pF)	Rate (Hz)	Tone (Hz)
5120	1000	200	330	16	512/640
6400	Select components in the ranges indicated in the table of electrical characteristics			20	640/800
3200				10	320/400
8000				25	800/1000
fo				$\frac{fo}{320}$	$\frac{fo}{10}/\frac{fo}{8}$

Applications

Typical Telephone Application: Figure 2 shows the schematic diagram of a typical telephone application for the S2561 tone ringer. Circuit power is derived from the telephone lines by the network formed by capacitor C_1, resistor R_1, diode bridge D_1 through D_4, and filter capacitor C_2. C_2 is chosen to be large enough so as to insure that the power supply ripple during ringing does not fall below the internal threshold level (typ. 7.3 volts) and to provide large enough decay time during the off period. A typical value of C_2 may be 47μF. C_1 and R_1 are chosen to satisfy the Ringer Equivalence Number (REN) specification (Ref. 1). For REN = 1 the resistor should be a minimum of 8.2kΩ. It must be noted that the amount of power that can be delivered to the load depends upon the selection of C_1 and R_1.

The device is enabled by limiting the incoming ring signal through resistors R_2, R_3 and diodes d_5 and d_6. Zener diode Z_1 (typ. 9-27 volts) may be required in certain applications where large voltage transients may occur on the line during dial pulsing. The internal 2ms filter and the dial pulse reject filter will suppress any undesirable components of the signal and will only respond to the normal 20Hz ring signal. Ring signals with frequencies above 16Hz will be detected.

The configuration shown will produce a tone with frequency components of 512Hz and 540 Hz with a shift rate of approximately 16 Hz and deliver at least 25mW to an 8Ω speaker through a 2000Ω:8Ω transformer. If "manual" mode is used, a potentiometer may be inserted in series with the transformer primary to provide volume control. If "automatic" mode is used, resistors R_L and R_M can be chosen to provide desired amplitude sequencing. Typically, signal power

will be down $20 \log \left(\frac{R_{LOAD}}{R_L + R_{LOAD}} \right)$ dB during the

first ring, and down $20 \log \left(\frac{R_{LOAD}}{R_M + R_{LOAD}} \right)$ dB during the

Figure 3-A. Simulation of the Telephone Bell in Non-Telephone Applications

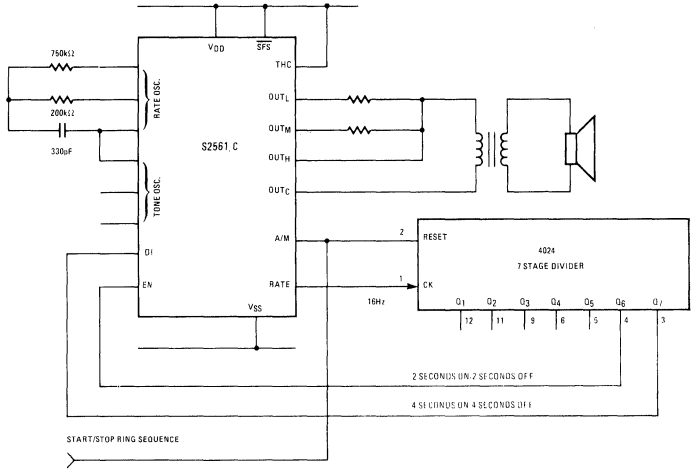
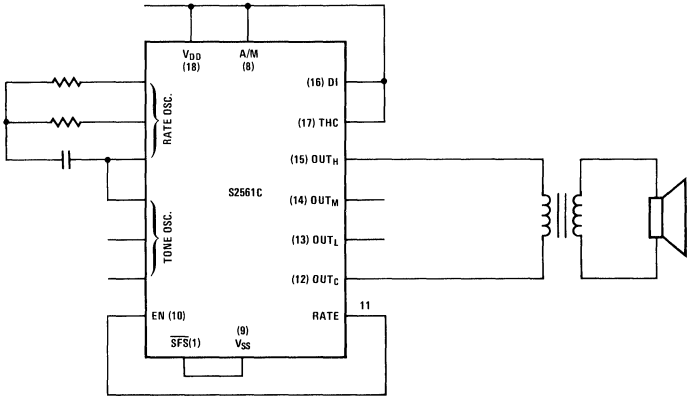


Figure 3-B. Single Frequency Tone Application in Alarms, Buzzers, Etc.



second ring with maximum power delivered to the load beginning the third and consecutive rings.

In applications where dial pulse rejection is not necessary, such as in DTMF telephone systems, the ENABLE pin may be connected directly to V_{DD}. Det. Inh pin must be connected to V_{DD} to allow DC level enabling of the ringer.

Non-Telephone Applications: The configuration shown in Figure 3-A may be used in non-telephone applications where it is desired to simulate the telephone bell.

The internal threshold is bypassed by wiring THC to V_{DD}. The rate output (16Hz) is divided down by a 7-stage divider type 4024 to produce two signals: a 2 second on/2 second off signal and a 4 second on/4 second off signal. The first signal is connected to the EN pin and the second to the DI pin to produce a 2 second on/4 second off telephone-type ring signal. The ring sequence is initiated by removing the reset on the divider. If "auto" mode is used, a reset signal must be applied to the "amplitude sequencing" counter at the end of a ring sequence so that the circuit will respond correctly to a new ring sequence. This is done by temporarily connecting the "auto/manual" input to V_{SS}.

Figure 3-B shows a typical application for alarms, buzzers, etc. Single frequency mode is used by connecting the $\overline{SFS}$ input to V_{SS}. A suitable on/off rate can be determined by using the 7-stage divider circuit. If tinuous tone is not desired, the 16Hz output can be used to gate the tone on and off by wiring it into the ENABLE input.

Many other configurations are possible depending upon the user's specific application.

Reference 1. Bell system communications technical reference:

PUB 47001 of August 1976.
"Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment"—2.6.1 and 2.6.3

AMI®

A Subsidiary of Gould Inc.

S2563

REPERTORY DIALER

Features

- ☐ Specifically Designed for Telephone Line Powered Applications
- ☐ CMOS Process Achieves Low Power Operation
- ☐ 8 or 16 Digit Number Capability (Pin Programmable)
- ☐ Dial Pulse and Mute Output
- ☐ Tone Outputs Obtained by Interfacing With Standard AMI S2559 Tone Generator
- ☐ Two Selections of Dial Pulse Rate
- ☐ Two Selections of Inter-Digit Pause
- ☐ Two Selections of Mark/Space Ratio
- ☐ Memory Storage of 29 8-Digit Numbers or 16-Digit Numbers with Standard AMI S5101 RAM
- ☐ 16-Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Accepts the Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboards; Also Capable of Logic Interface
- ☐ Can Use Standard 3×4 or 4×4 Keyboards
- ☐ Inexpensive, but Accurate R-C Oscillator Design
- ☐ BCD Output with Update for Single Digit Display

General Description

The S2563 is an improved version of the S2562 repertory dialer and can replace the S2562 in existing applications using local power. It is however specifically designed for applications that will only use telephone line power. To achieve this following changes were made to the S2562 design.

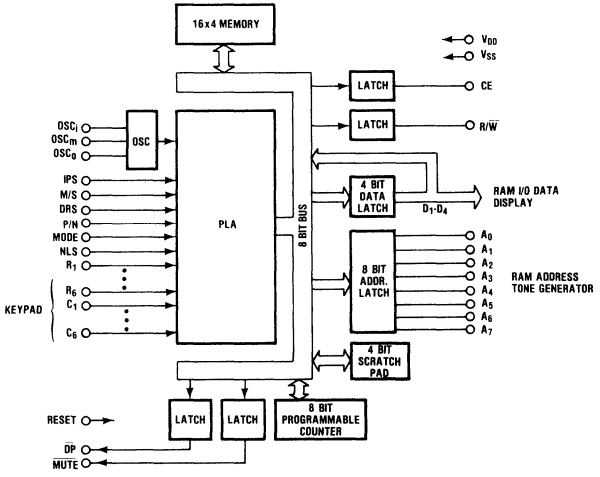
a. $\overline{PF}$ output was replaced by a level reset input which allows the device to be totally powered down in the on-hook state of the telephone.

b. To reduce power consumption in the associated S5101 memory in the standby mode, the interface was changed so that its CE_2 input rather than the the $\overline{CE_1}$ input is controlled by the device.

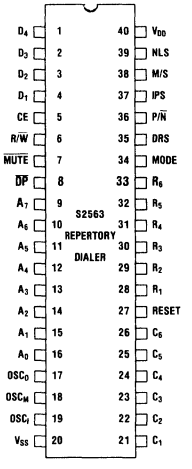
c. Process was changed to a lower voltage CMOS process. Additionally a mark/space selection input (M/S) was added to allow selection of either 40/60 or 33/67 ratio. Provision was also made to allow the device to work with a standard 3×4 or 4×4 keyboard.

Data subject to change at any time without notice. These sheets transferred for information only.

Block Diagram



Pin Configuration



DTMF TONE GENERATOR WITH REDIAL

Features

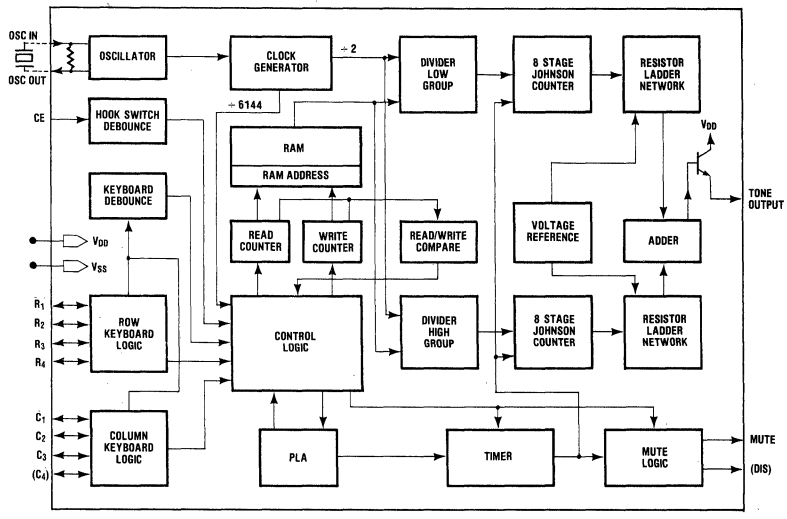
- ☐ Wide Operating Supply Voltage Range (2.50–10V)
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines
- ☐ 21 Digit Memory for Redial
- ☐ Uses Standard 3x4 (S2569A) or 4x4 (S2569) SPST or X-Y Matrix Keyboard
- ☐ The Total Harmonic Distortion is Below Industry Specification (Max. 7% Over Typical Loop Current Range)
- ☐ Separate Control Keys (S2569) for Disconnect, Pause, Redial and Flash in Column Four
- ☐ Allows Dialing of * and # Keys on S2569. For S2569A Redial Initiated by * or # Key as First Key Offhook, * or # can be Dialed After First Key Offhook.

General Description

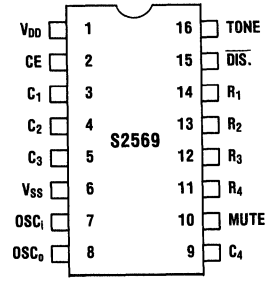
The S2569/A is a member of the S2559 Tone Generator family with the added features of Redial, Disconnect and Flash. The device produces 12 out of 16 dual tones corresponding to the 12-digit keys located on the conventional Touch-Tone® telephone keypad. Function keys for Disconnect(D), Pause(P), Redial(R), and Flash(F) are located in column four. (Note that column 4 will not generate any tone.) S2569A utilizes only Redial initiated by * or # key as first key offhook.

A voltage reference generated on the chip regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

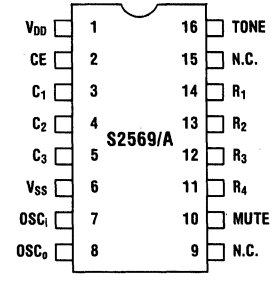
Block Diagram



S2569 Pin Configuration



S2569/A Pin Configuration



Absolute Maximum Rating:

DC Supply Voltage (V_{DD}-V_{SS})	+13.5V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +140°C
Power Dissipation at 25°C	500mW
Input Voltage	$V_{SS} - 0.6 < V_{IN} < V_{DD} + 0.6V$

S2569A Electrical Characteristics: (Specifications apply over the operating temperature range of 0°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions	($V_{DD} - V_{SS}$) Volts	Min.	Max.	Unit
	Supply Voltage				
V_{DD}	Tone Out Mode (Valid Key Depressed)		2.50	10.0	V
	Non Tone Out Mode (No Key Depressed)		1.50	10.0	V
	Supply Current				
I_{DD}	STANDBY (NO Key Depressed, Tone, Mute and Flash Outputs Unloaded, CE = low	2.00 5.00		1 20	μA μA
	Operating (One Key Selected, Tone, Mute and Flash Outputs Unloaded).	3.00		2.5	mA
	Operating During Flash	3.0		300	μA
	Tone Output				
V_{OR}	Low Group Frequency Voltage (R_L = 1kΩ)	3.0	246	310	mVrms
dBcr	Ratio Of Column To Row Tone	2.5-5.0	1.0	3.0	dB
% DIS	Distortion*	2.5-10.0		7	%
	Mute and Flash Outputs				
I_{OH}	Output Source Current V_{OH} = 2.7V	3.0	1.0		mA
I_{OL}	Output Sink Current V_{OL} = 0.3V	3.0	1.0		mA

* Distortion measured in accordance with the specifications described as "ratio of total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

NOTE: R_L = load resistor connected from output to V_{SS}.

Basic Chip Operation

The dual tone signal consists of linear addition of two voice frequency signals. One of two signals is selected from a group of frequencies called "low group" and the other is selected from a group of frequencies called "high group". The low group consists of four frequencies; 697, 770, 852 and 941 Hz. The high group consists of three frequencies; 1209, 1336 and 1477 Hz.

When a push button corresponding to a digit (0 thru 9, *, #) is pushed, one appropriate row (R_1 thru R_4) and one appropriate column (C_1 thru C_3) is selected. The active row input selects one of the low group frequencies and active column input selects one of the high group frequencies.

Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide-by-16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function. This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD}-V_{REF}$) of the stairstep function is fairly constant. V_{REF} is chosen so that V_P falls within the allowed range of the high group and low group tones.

Normal Dialing

Tone dialing starts as soon as the first digit is entered and debounced. The entered digits are stored sequentially in the internal memory. Pauses may be entered when required in the dial sequence by pressing the "P" key, which provides access pause for future redial. Any number of access pauses may be entered as long as the total entries do not exceed the total number of digits. Numbers up to 21 digits can be redialed. Numbers exceeding 21 digits will clear redial buffer. Note that only the S2569 has "Pause" capability and the access pause is included in the 21 digit maximum number.

Redial

The last number dialed is retained in the memory and therefore can be redialed by going off hook and pressing the "R" key on the S2569 (located at column 4 and row 3). The S2569A does not use column four and Redial is initiated by "#" or "*" key as the first key off-hook. Tone dialing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the tone dialing output will stop and will resume only after the user pushes any key except Flash and Disconnect keys. During redial all keys are ignored until 70ms after the last digit is dialed (except Disconnect). (Note that the "Pause" function is not available on the S2569A.)

Disconnect/Flash Functions

The S2569 has a push-pull buffer for Disconnect output. With no keys depressed the Disconnect output is high. When the Disconnect key is depressed the Disconnect output goes low until the key is released. Disconnect output can also be used to implement a "Flash" function. When the Flash key is depressed the Disconnect output goes low for 90ms.

Figure 1

1	2	3	D
4	5	6	P
7	8	9	R
#	0	*	F

S2569 Keypad

1	2	3
4	5	6
7	8	9
#	0	*

S2569A Keypad

Keyboard Interface

The S2569/A employs a scanning circuitry to determine key closures. When no key is depressed active pull down resistors are on on the row inputs and active pull up resistors are on on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull up or pull down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The value of pull down and pull up resistors will vary with supply voltage. Typical values of pull up and pull down resistors are shown in Table 1.

Table 1. Typical Resistance Values

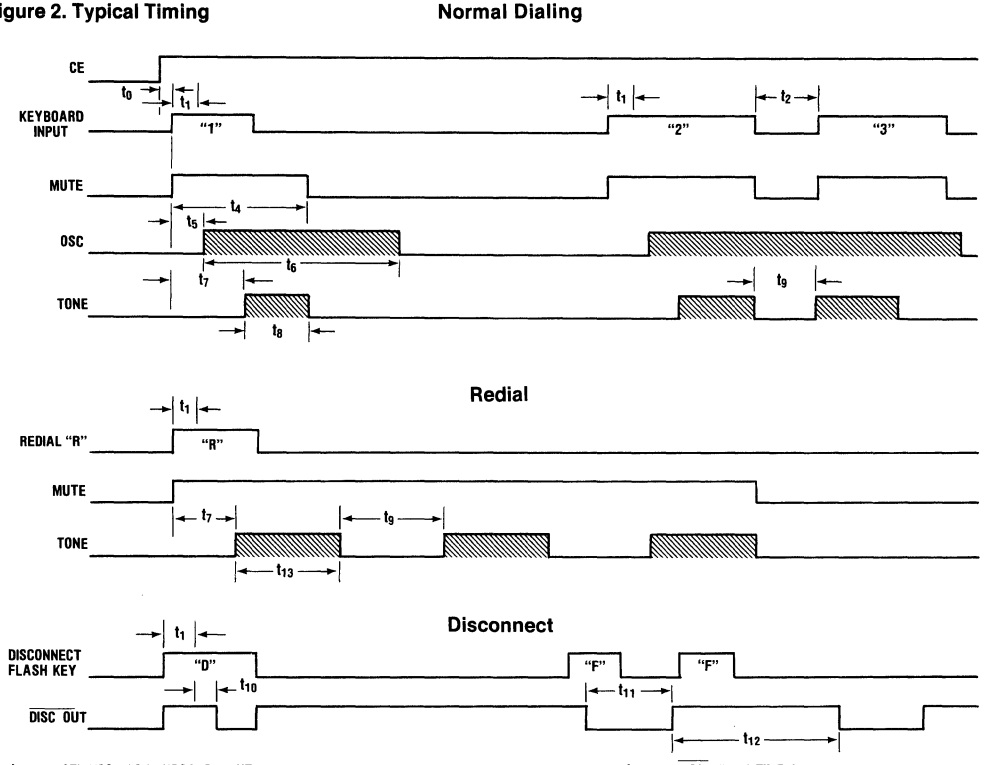
V_{DD}	PULL UP RESISTANCE (TYP.)
2.0V	3.3 K ohm
5.0V	1.5 K ohm
10.0V	1.3 K ohm
V_{DD}	**PULL DOWN RESISTANCE (TYP.)**
2.0V	340 K ohm
5.0V	36.6 K ohm
10.0V	16.6 K ohm

Table 2. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2569/A

ACTIVE INPUT	OUTPUT FREQUENCY HZ SPECIFIED	ACTUAL	% ERROR
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1339	1331.7	−0.32
C3	1477	1471.9	−0.35

NOTE: % error does not include oscillator drift.

Figure 2. Typical Timing



t_0 : OFF HOOK TO KEYBOARD INPUT DELAY TIME:0ms
t_1 : DEBOUNCE TIME:18ms
t_2 : KEY RELEASE TIME:6ms
t_4 : MIN. MUTE PULSE WIDTH:73ms
t_5 : OSC START UP:3ms
t_6 : OSC MIN. ON TIME:142ms
t_7 : TONE OUTPUT DELAY TIME:21ms
t_8 : MIN. TONE OUT TIME:70ms
t_9 : MIN. OFF TIME:70ms
t_{10} : $\overline{\text{DISC}}$ DELAY TIME:4ms
t_{11} : MAX. OUTPUT PULSE:90ms
t_{12} : MIN. DISC OFF TIME:50ms
t_{13} : TONE ON TIME:70ms

Logic Interface

The S2569/A can also interface with CMOS logic outputs directly. The S2569/A requires active high logic levels. Since the pull up resistors present in the S2569/A are fairly low values, diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their low logic state.

Figure 3a. Typical Application Circuit for Line Powered DTMF Dialer With Redial S2569

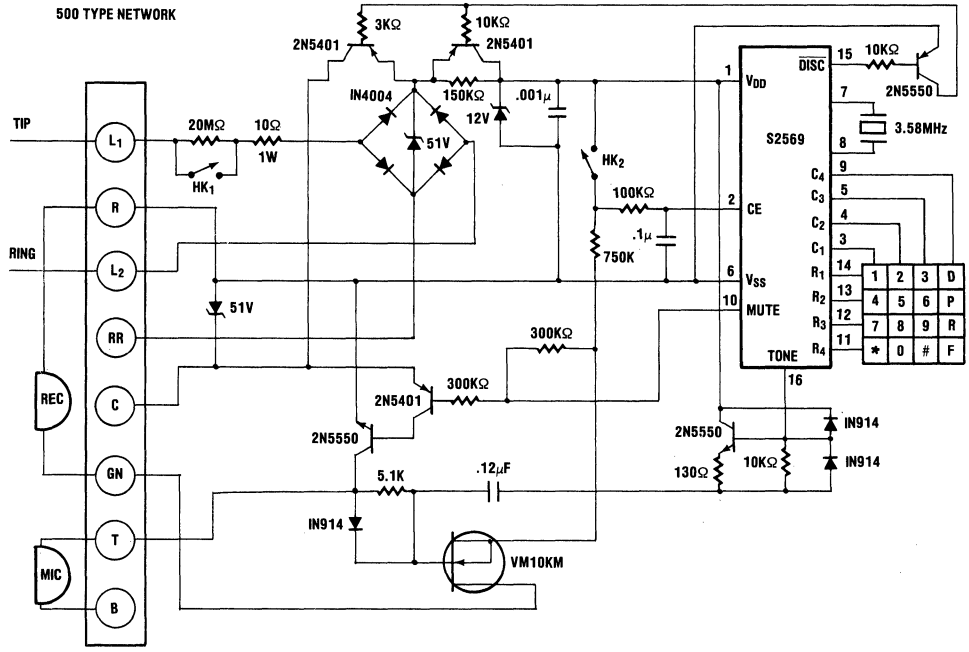
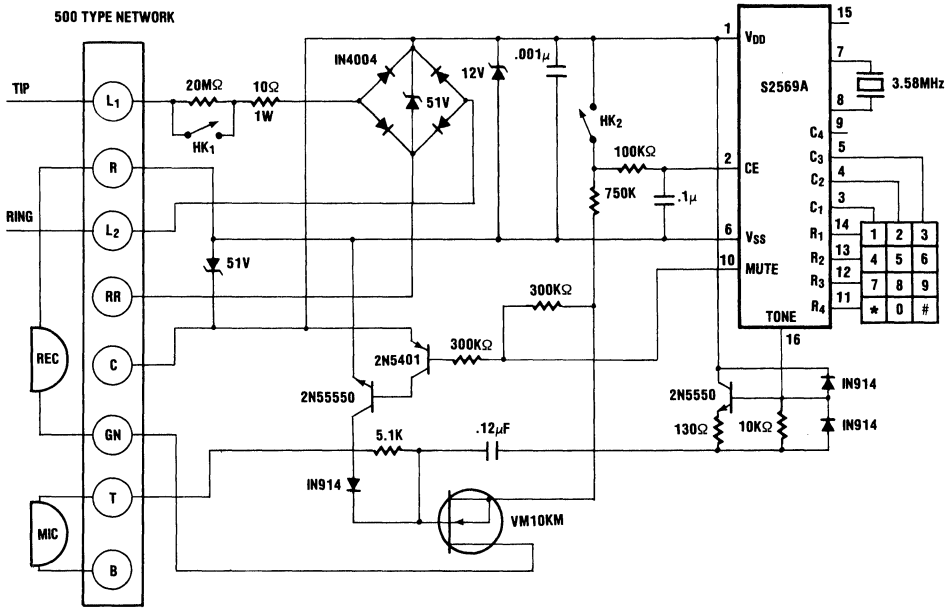


Figure 3b. Typical Application Circuit for Line Powered DTMF Dialer With Redial S2569A



Chip Enable

The S2569/A has a Chip Enable input at pin 2. The Chip Enable for the S2569/A is an active "high". When the Chip Enable is "low", the Tone output goes to V_{SS}, the oscillator is inhibited and the Mute and Disconnect outputs will go into a low state.

Mute Output

The S2569/A has a push-pull buffer for Mute output. With no keys depressed the Mute output is low, when a key is depressed the Mute output goes high until the key is released. Note that minimum mute pulse width is 70ms.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor (1MΩ) on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_i and OSC_o terminals to implement the oscillator function.

Oscillator Crystal Specifications

Frequency 3.579545MHz ±.02%, Rs<100Ω,
Lm = 96Mhy, Cm = .02pF Ch = 5pF

Test Mode

The S2569/A will enter the test mode if all rows are pulled high momentarily. 16 times the low group frequency will appear at mute output depending on which row is selected. Also, 16 times the high group frequency will appear at disconnect output depending upon which column is selected.

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Advanced Product Description **S2569B**

DTMF TONE GENERATOR WITH REDIAL

COMMUNI-CATIONS

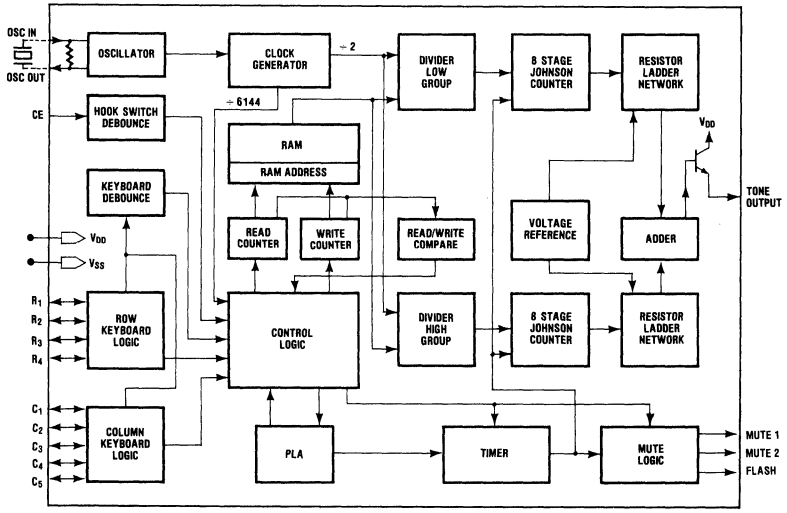
Features

- ☐ Wide Operating Supply Voltage Range (2.50–10V)
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines
- ☐ 21 Digit Memory for Redial
- ☐ Uses 4x5 SPST or X-Y Matrix Keyboard
- ☐ The Total Harmonic Distortion is Below Industry Specification (Max. 7% Over Typical Loop Current Range)
- ☐ Separate Control Keys for Flash and Redial
- ☐ Allows Dialing of *, # and A Through D Keys

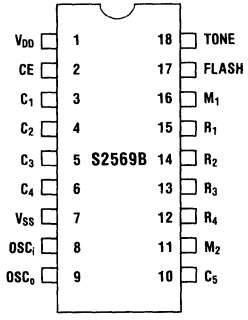
General Description

The S2569B is a member of the S2559 Tone Generator family with the added features of Redial and Flash. The device produces 16 dual tones corresponding to the 16-digit keys located on the conventional Touch-Tone® telephone keypad. Function keys for Redial(R) and Flash(F) are located in column five. A voltage reference generated on the chip regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration



Absolute Maximum Rating:

DC Supply Voltage (V_{DD}-V_{SS})	+13.5V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +140°C
Power Dissipation at 25°C	500mW
Input Voltage	$-0.6<V_{IN}<V_{DD}+0.6V$

S2569B Electrical Characteristics: (Specifications apply over the operating temperature range of 0°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions	($V_{DD}-V_{SS}$) Volts	Min.	Max.	Unit
	Supply Voltage				
V_{DD}	Tone Out Mode (Valid Key Depressed)		2.50	10.0	V
	Non Tone Out Mode (No Key Depressed)		1.50	10.0	V
	Supply Current				
I_{DD}	STANDBY (NO Key Depressed, Tone, Mute and Flash Outputs Unloaded, CE = low	2.00 5.00		1 20	μA μA
	Operating (One Key Selected, Tone, Mute and Flash Outputs Unloaded). Operating During Flash	3.00 3.0		2.5 300	mA μA
	Tone Output				
V_{OR}	Low Group Frequency Voltage (R_L = 1kΩ)	3.0	246	310	mVrms
dBcr	Ratio Of Column To Row Tone	2.5-5.0	2.4	3.0	dB
% DIS	Distortion*	2.5-10.0		7	%
	Mute and Flash Outputs				
I_{OH}	Output Source Current V_{OH} = 2.7V	3.0	1.0		mA
I_{OL}	Output Sink Current V_{OL} = 0.3V	3.0	1.0		mA

* Distortion measured in accordance with the specifications described as "ratio of total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

NOTE: R_L = load resistor connected from output to V_{SS}.

Basic Chip Operation

The dual tone signal consists of linear addition of two voice frequency signals. One of two signals is selected from a group of frequencies called "low group" and the other is selected from a group of frequencies called "high group". The low group consists of four frequencies; 697, 770, 852 and 941 Hz. The high group consists of four frequencies; 1209, 1336, 1477 and 1633 Hz.

When a push button corresponding to a digit (0 thru D, *, #) is pushed, one appropriate row (R_1 thru R_4) and one appropriate column (C_1 thru C_4) is selected. The active row input selects one of the low group frequencies and active column input selects one of the high group frequencies.

Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the program-

Tone Generation (Continued)

mable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide-by-16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function. This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD}-V_{REF}$) of the stair-step function is fairly constant. V_{REF} is chosen so that V_P falls within the allowed range of the high group and low group tones.

Normal Dialing

Tone dialing starts as soon as the first digit is entered and debounced. The entered digits are stored sequentially in the internal memory. Numbers up to 21 digits can be redialed. Numbers exceeding 21 digits will clear redial buffer. Note that the S2569B will not accept roll over entries.

Redial

The last number dialed is retained in the memory and therefore can be redialed by going offhook and pressing the "R" key (located at column 5 and row 3). Tone dialing will start when the key is depressed and finish after the entire number is dialed out.

If the redial key is held down, tone dialing will stop after the first digit is dialed, and will resume again when the key is released. This provides for single digit access codes. During Redial the S2569B will ignore any keyboard entry. Keys will be accepted 70ms after last number is dialed.

Redial Inhibit

Redial can be inhibited by dialing (*), (#), and Flash, in normal dialing sequence. Numbers exceeding 21 digits and single tones will also inhibit redial.

Flash Output

The S2569B has a push-pull buffer for Flash output. With no keys depressed the Flash output is low. When the Flash key is depressed, the Flash output goes high for 90ms.

Keyboard Interface

The S2569B employs a scanning circuitry to determine key closures. When no key is depressed, active pull down resistors are on on the row inputs and active pull up resistors are on on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull up or pull down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The values of pull down and pull up resistors will vary with supply voltage. Typical values of pull up and pull down resistors are shown in Table 1.

Table 1. Typical Resistance Values

V_{DD}	PULL UP RESISTANCE (TYP.)
2.0V	3.3 K ohm
5.0V	1.5 K ohm
10.0V	1.3 K ohm
V_{DD}	**PULL DOWN RESISTANCE (TYP.)**
2.0V	340 K ohm
5.0V	36.6 K ohm
10.0V	16.6 K ohm

Table 2. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2569B

ACTIVE INPUT	OUTPUT FREQUENCY HZ SPECIFIED	ACTUAL	% ERROR
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1339	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

NOTE: % error does not include oscillator drift.

Figure 1. Standard Telephone Push Button Keyboard

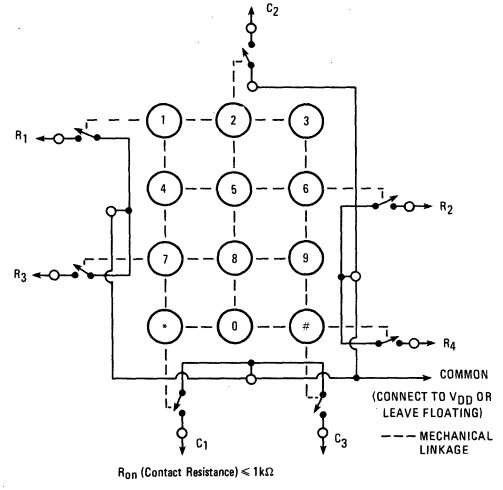
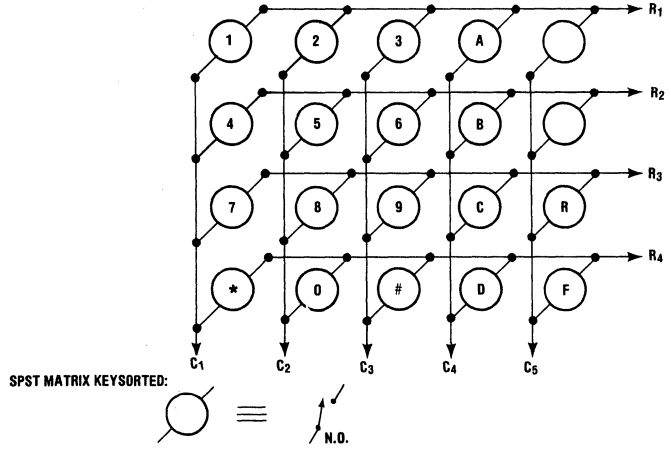


Figure 2. SPST Matrix Keyboard Arranged in the 2 of 8 Row, Column Format

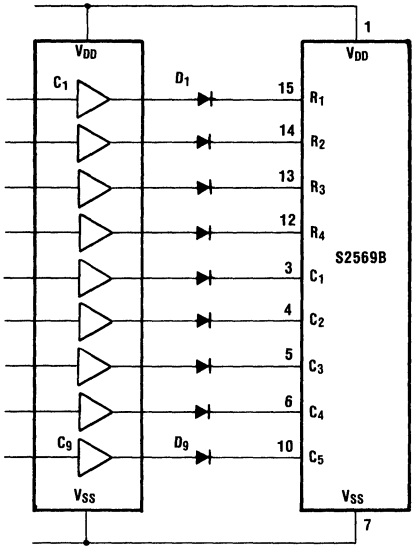


Logic Interface

The S2569B can also interface with CMOS logic outputs directly. The S2569B requires active high logic levels.

Since the pull up resistors present in the S2569B are fairly low values, diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their low logic state.

Figure 3. Logic Interface for Keyboard Inputs of the S2569B



G1 THRU G9 ANY TYPE CMOS GATE
D1 THRU D9 DIODES TYPE IN914 (OPTIONAL)

Chip Enable

The S2569B has a Chip Enable input at pin 2. The Chip Enable for the S2569B is an active "high". When the Chip Enable is "low", the tone output goes to V_{SS}, the oscillator is inhibited and the Mute and Disconnect outputs will go into a low state.

Mute Outputs (M1, M2)

The S2569B has push-pull buffers for Mute outputs. With no keys depressed the Mute outputs are low. When a key is depressed the outputs go high until the key is released. M1 will stay high for additional 250ms. Note that minimum mute pulse width is 70ms for M2 and 320ms for M1.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor (1MΩ) on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_I and OSC_O terminals to implement the oscillator function.

Oscillator Crystal Specifications

Frequency 3.579545MHz + .02% Rs<100 ohm, LM = 96 Mhy, Cm = .02pF Ch = 5pF.

Single Tone Mode

The S2569B is capable of dialing single as well as dual tones. Single tones in either the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column.

Note that two keys have to be depressed simultaneously or the output will be the normal dual tones. If the keys are depressed within 10msec of each other, the single tone will be generated. If not, the standard dual tone representing the first key depressed will be sent and the second button will be ignored.

Test Mode

The S2569B will enter the test mode if all rows are pulled high momentarily. 16 times the low group frequency will appear at the M2 output depending on which row is selected. Also 16 times high group freuqnecy will appear at the Flash output depending on which column is selected.

Figure 4. Stairstep Waveform of the Digitally Synthesized Sinewave

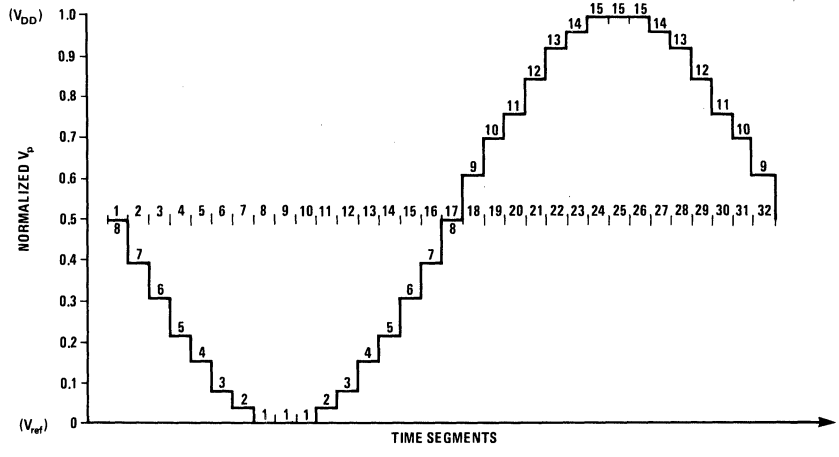
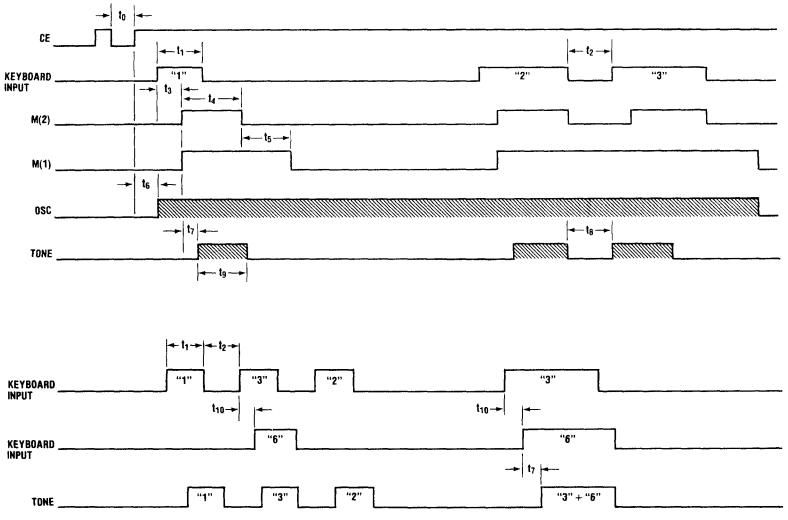


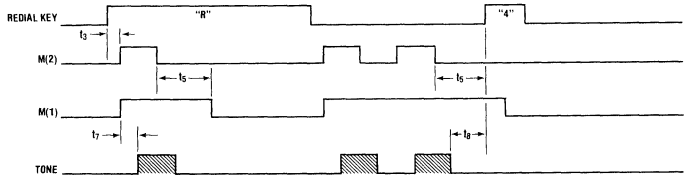
Figure 5. Typical Timing

Normal Dialing

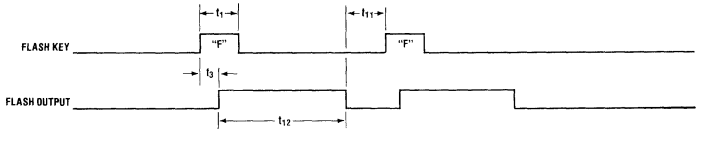


t_0 : MIN RESET TIME:12ms
t_1 : DEBOUNCE TIME:15ms
t_2 : KEY RELEASE TIME:6ms
t_3 : MUTE DELAY TIME:18ms
t_4 : MIN. MUTE PULSE WIDTH:70ms
t_6 : OSC START UP TIME:10ms
t_5 : M(1) TURN OFF TIME:250ms
t_7 : TONE DELAY TIME:3ms
t_9 : MIN. TONE OUT:70ms
t_8 : TONE OFF TIME:70ms
t_{10} : MAX. DELAY TIME:10ms

Redial

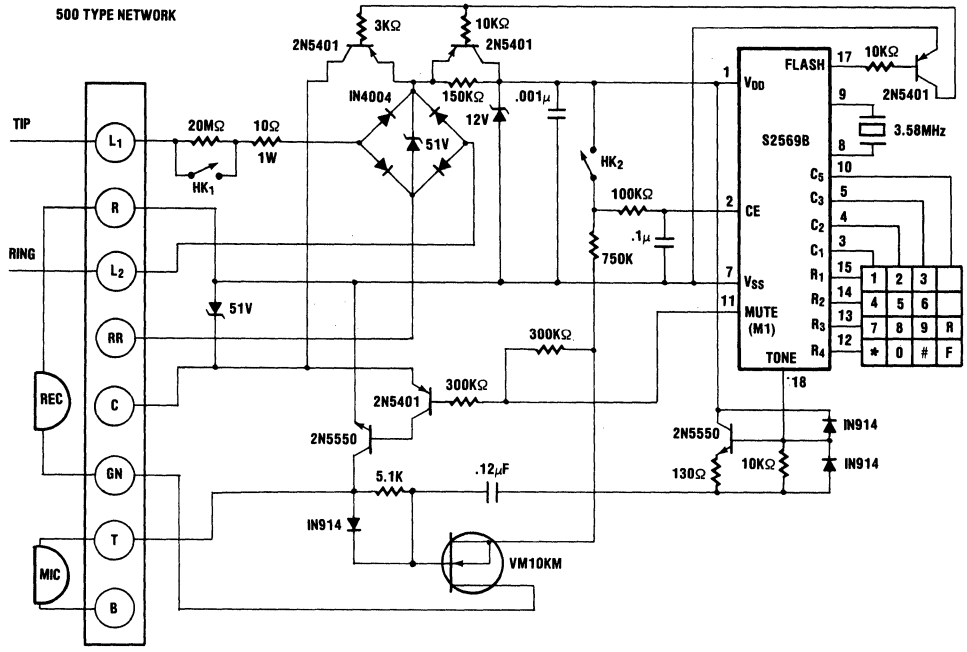


Flash



t_{11} : MIN TIME TO ENTER KEY:50ms
t_{12} : FLASH PULSE WIDTH:90ms

Figure 7. Typical Applications Circuit for Line Powered DTMF Dialer With Redial



AMI®

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S25089

DTMF TONE GENERATOR

COMMUNI-CATIONS

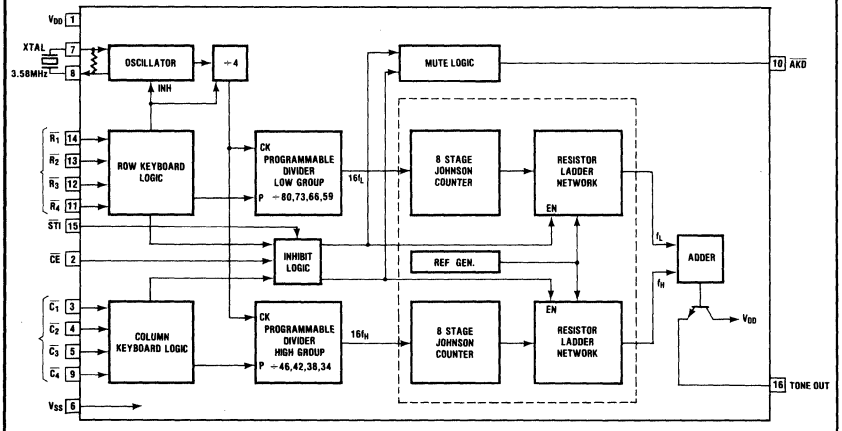
Features

- ☐ Wide Operating Voltage Range: 2.5 to 10 Volts
- ☐ Optimized for Constant Operating Supply Voltages, Typically 3.5V
- ☐ Tone Amplitude Stability is Within ± 1.5dB of Nominal Over Operating Temperature Range
- ☐ Low Power CMOS Circuitry Allows Device Power to to be Derived Directly From the Telephone Lines or From Small Batteries
- ☐ Uses TV Crystal Standard (3.58MHz) to Derive All Frequencies Thus Providing Very High Accuracy and Stability
- ☐ Specifically Designed for Electronic Telephone Applications
- ☐ Interfaces Directly to a Standard Telephone Push-Button Keyboard With Common Terminal
- ☐ Low Total Harmonic Distortion
- ☐ Single Tone as Well as Dual Tone Capability
- ☐ Direct Replacement for Mostek MK5089 Tone Generator

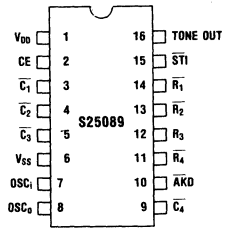
General Description

The S25089 DTMF Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is very stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage (V_{DD}-V_{SS})	+10.5V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	500mW
Input Voltage	$V_{SS} - 0.6 \leq V_{IN} \leq V_{DD} + 0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics: (Specifications apply over the operating temperature range of 0°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				2.5	—	10.0	V
	Non Tone Out Mode ($\overline{AKD}$ Outputs toggle with key depressed)				1.6	—	10.0	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone and $\overline{AKD}$ Outputs Unloaded)			3.0 10.0	— —	1 5	20 100	μA μA
	Operating (One Key Selected, Tone and $\overline{AKD}$ Outputs Unloaded)			3.0 10.0	— —	.9 4.5	1.25 10.0	mA mA
	Tone Output							
V_{OR}	Dual Tone	Row Tone	$R_L = 10k\Omega$	3.0	−11.0		−8.0	dBm
	Mode Output	Amplitude	$R_L = 100k\Omega$	3.5	−10.0		−7.0	dB
dB_{CR}	Ratio of Column to Row Tone			2.5-10.0	2.4	2.7	3.0	dB
%DIS	Distortion*			2.5-10.0	—	—	10	%
NKD	Tone Output—No Key Down						−80	dBm
	$\overline{AKD}$ Output							
I_{OL}	Output On Sink Current		$V_{OL} = 0.5V$	3.0	0.5	1.0	—	mA
I_{OH}	Output Off Leakage Current			10.00		1	10	μA
	Oscillator Input/Output							
I_{OL}	One Key Selected		$V_{OL} = 0.5V$	3.0	0.21	0.52	—	mA
	Output Sink Current		$V_{OL} = 0.5V$	10.0	0.80	2.1	—	mA
I_{OH}	Output Source Current		$V_{OH} = 2.5V$	3.0	0.13	0.31	—	mA
	One Key Selected		$V_{OH} = 9.5V$	10.0	0.42	1.1	—	mA
t_{START}	Oscillator Startup Time with Crystal as Specified			3.0-10.0	—	2	5	ms
$C_{I/O}$	Input/Output Capacitance			3.0	—	12	16	pF
				10.00	—	10	14	pF

*Distortion measured in accordance with the specifications described in REF. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		—	V_{SS}		.2(V_{DD} − V_{SS})	V
V_{IH}	Input Voltage, High		—	.8(V_{DD} − V_{SS}	—	V_{DD}	V
I_{IH}	Input Current	V_{IH} = 0.0V	3.0	30	90	150	μA
	(Pull up)	V_{IH} = 0.0V	10.0	100	300	500	μA

Oscillator

The S25089 contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_i and OSC_0 terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 4 and then drives two sets of programmable dividers, the high group and the low group.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ±0.02%

R_S 100Ω, L_M = 96mH

C_M = 0.02pF C_H = 5pF C_L = 12pF

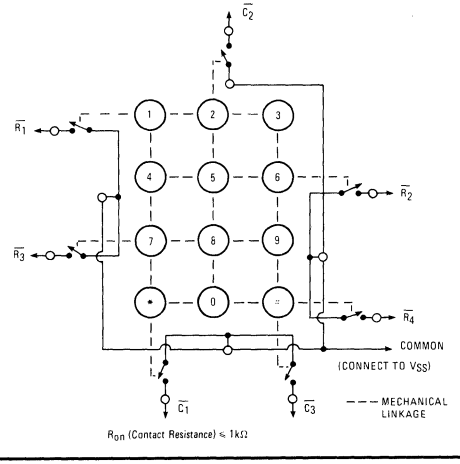
Keyboard Interface

The S25089 can interface with the standard telephone pushbutton keyboard (see Figure 1) with common. The common of the keyboard must be connected to V_{SS}.

Logic Interface

The S25089 can also interface with CMOS logic outputs directly (see Figure 2). The S25089 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 20kΩ-100kΩ.

Figure 1. Standard Telephone Push Button Keyboard



Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divided by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson

counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP (V_{DD}-V_{REF}) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

The individual tones generated by the sinewave synthesizer are then linearly added and drive an NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level. This allows the device to drive varying resistive loads without significant variation in tone amplitude. For example, a load resistor change from 10kΩ to 1kΩ causes a decrease in tone amplitude of less than 1dB.

Dual Tone Mode

When one row and one column is selected, dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys that are not either in the same row or in the same column are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column. This is slightly different from the MK5089 which requires a low to a single column pin to get a column tone.

Inhibiting Single Tones

The $\overline{STI}$ input (pin 15) is used to inhibit the generation of other than dual tones. It has an internal pull down to V_{SS} supply. When this input is left unconnected or connected to V_{SS}, single tone generation as described in the preceding paragraph (Single Tone Mode) is suppressed with all other functions operating normally. When this input is connected to V_{DD} supply, single or dual tones may be generated as previously described (Single Tone Mode, Dual Tone Mode).

Chip Enable Input (CE, Pin 2)

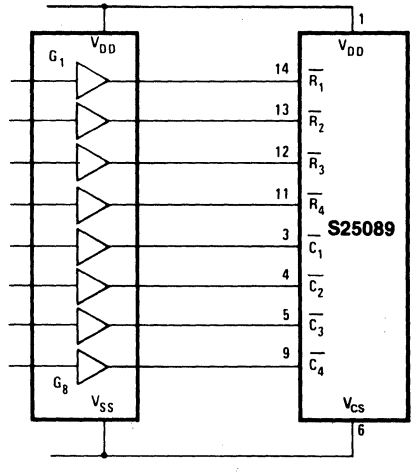
The chip enable input has an internal pull-up to V_{DD} supply. When this pin is left unconnected or connected to V_{DD} supply the chip operates normally. When connected to V_{SS} supply, tone generation is inhibited. All other chip functions operate normally.

Table 1. Comparison of Specified Vs. Actual Tone Frequencies Generated by S25089

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR
	SPECIFIED	ACTUAL	SEE NOTE
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

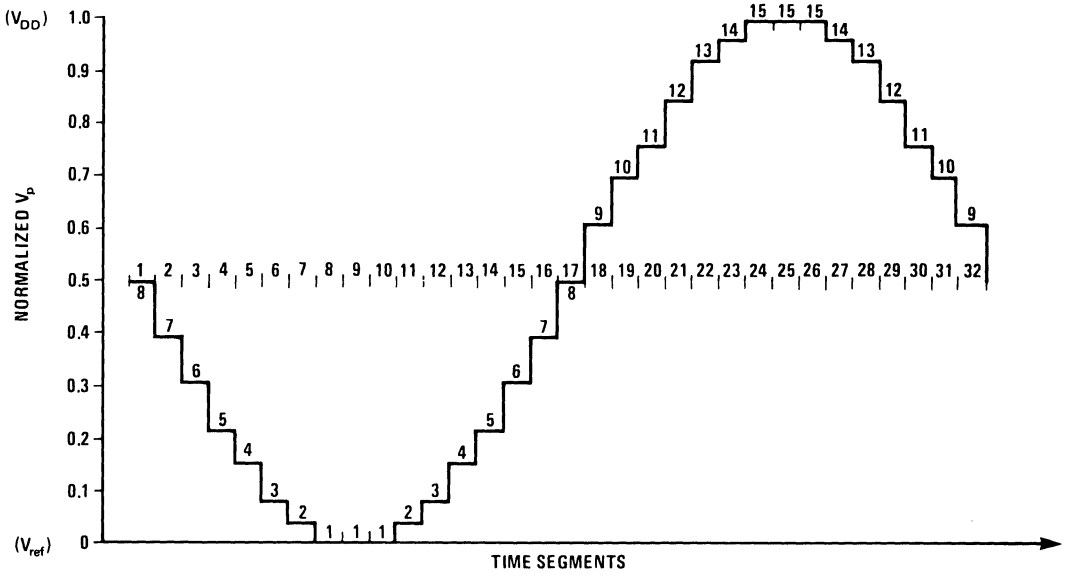
NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

Figure 2. Logic Interface for Keyboard Inputs of the S25089



G1 THRU G8 ANY TYPE CMOS GATE

Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



Reference Voltage

The structure of the reference voltage employed in the S25089 is shown in Figure 4. It has the following characteristics:

a) V_{REF} is proportional to the supply voltage. Output tone amplitude, which is a function of (V_{DD} - V_{REF}), increases with supply voltage (Figure 5).
b) The temperature coefficient of V_{REF} is low due to a single V_{BE} drop. Use of a resistive divider also provides an accuracy of better than 1%. As a result, tone amplitude variations over temperature and unit to unit are held to less than ± 1.0dB over nominal.
c) Resistor values in the divider network are so chosen that V_{REF} is above the V_{BE} drop of the tone output transistor even at the low end of the supply voltage range. The tone output clipping at low supply voltages is thus eliminated, which improves distortion performance.

$\overline{AKD}$ (Any Key Down or Mute) Output

The $\overline{AKD}$ output (pin 10) consists of an open drain N channel device (see Figure 6.) When no key is depressed the $\overline{AKD}$ output is open. When a key is depressed the $\overline{AKD}$ output goes to V_{SS}. The device is large enough to sink a minimum of 500μA with voltage drop of 0.2V at a supply voltage of 3.5V.

Figure 4. Structure of the Reference Voltage

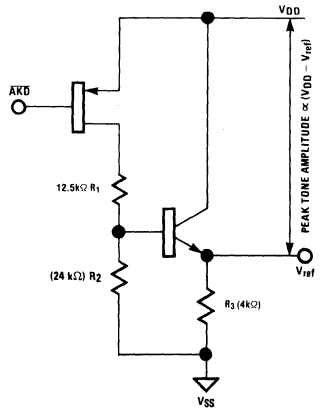


Figure 5. Typical Single Tone Output Amplitude Vs Supply Voltage (R_L = 10k)

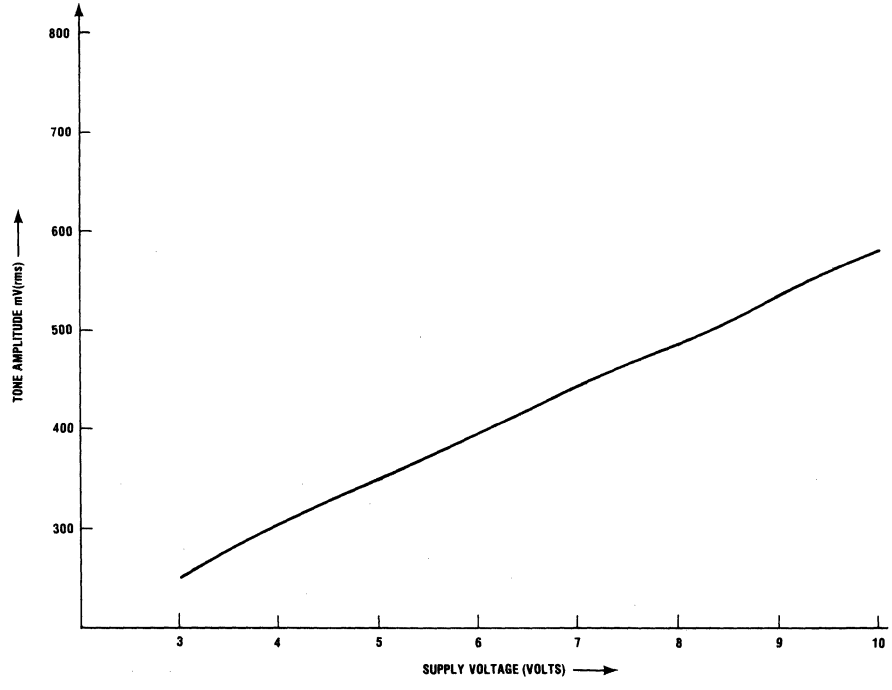
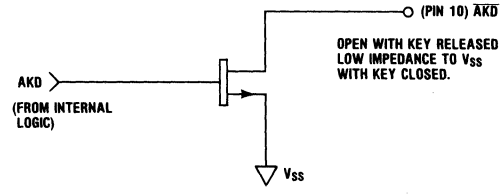


Figure 6. AKD output Structure



A Subsidiary of Gould Inc.

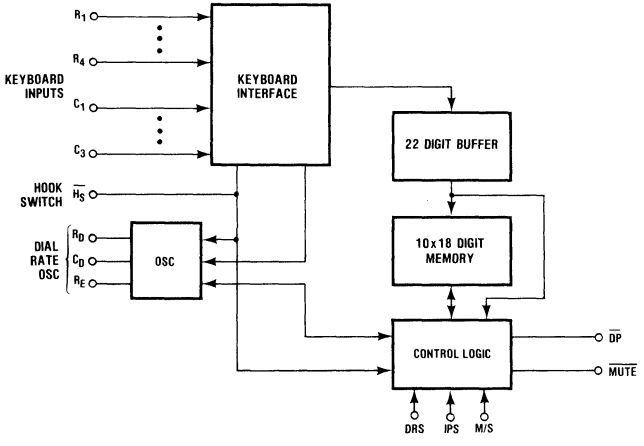
S25610

SINGLE CHIP REPERTORY DIALER

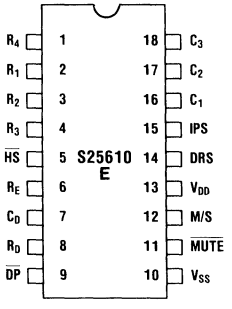
Features

- ☐ Complete Pin Compatibility With S2560A and S2560G Pulse Dialer Allowing Easy Upgrading of Existing Designs.
- ☐ Ten 18-Digit Number Memories Plus Last Number Redial (22 Digit) Memory On Chip.
- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines.
- ☐ Inexpensive R-C Oscillator Design With Accuracy Better Than ±5% Over Temperature and Unit-Unit Variations.
- ☐ Independent Select Inputs for Variation of Dialing Rates (10pps/20pps), Mark/Space Ratio (33⅓-66⅔/40-60), Interdigit Pause (400ms/800ms).
- ☐ Can Interface With Inexpensive XY Matrix or Standard 2 of 7 Keyboard With Common. Also Capable of Logic Interface (Active High).
- ☐ Mute and Pulse Drivers On Chip.
- ☐ Call Disconnect by Pushing * and # Keys Simultaneously.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leq V_{DD} - V_{SS} \leq 3.5V$ unless otherwise specified.

Symbol	Parameter	V_{DD}-V_{SS} (Volts)	Min.	Max.	Units	Conditions
	Operating Voltage					
V_{DD}	Data Retention		1.0		V	On Hook, ($\overline{HS} = V_{DD}$)
V_{DD}	Non Dialing State		1.5	3.5	V	Off Hook, Oscillator Not Running
V_{DD}	Dialing State		2.0	3.5	V	Off Hook, Oscillator Running
	Operating Current					
I_{DD}	Data Retention	1.0		2.0	μA	On Hook, ($\overline{HS} = V_{DD}$)
I_{DD}	Non Dialing	1.5		10	μA	Off Hook ($\overline{HS} = V_{SS}$), Oscillator Not Running, Outputs Not Loaded
I_{DD}	Dialing	2.0 3.5		100 500	μA μA	Off Hook, Oscillator Running, Outputs Not Loaded
	Output Current Levels					
I_{OLDP}	DP Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHDP}	DP Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	MUTE Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHM}	MUTE Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
fo	Oscillator Frequency	2.0		10	kHz	
Δfo/fo	Frequency Deviation	2.0 to 2.75 2.75 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50k\Omega \leq R_D \leq 750k\Omega$; $100pF \leq C_D{}^* \leq 1000pF$; $750k\Omega \leq R_E \leq 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD} - V_{SS}$)	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of ($V_{DD} - V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

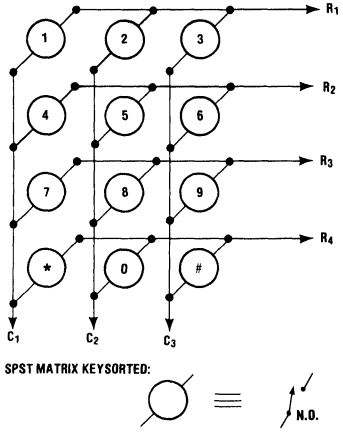
The device contains an oscillator circuit that requires three external components; two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including

the "on hook" condition. For a dialing rate of 10pps the oscillator should be adjusted to 2400Hz. Typical values of external components for this are R_D, R_E = 750kΩ and C_D = 270pF. It is recommended that the tolerance of resistors to be 1% and capacitor to be 5% to insure a ± 10% tolerance of the dialing rate in the system.

Keyboard Interface

The S25610 employs a scanning technique to determine a key closure. This permits interface to a DPCT (Double Pole Common Terminal) keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2),or a XY matrix. A high level on the appropriate row and column inputs constitutes a key closure for logic interface.

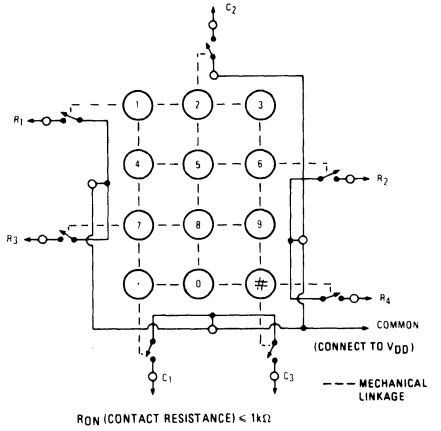
Figure 1. SPST Matrix Keyboard Arranged in a Row, Column Format



On Hook Operation: The device is continuously powered through a 10-20MΩ resistor during the on hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed. DP and mute outputs are low in the on hook state.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

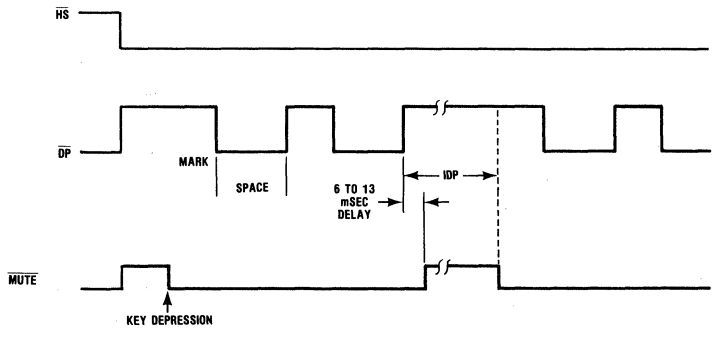
Figure 2. Standard Telephone Pushbutton Keyboard



Off Hook Operations: The device is continuously powered through a 150kΩ resistor during off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The DP output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during this pulse break. The MUTE output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20pps can be achieved. Dialing rates of 7 and 14pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

Figure 3. Timing (Off Hook)



The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14pps, IDP's of 1143ms and 572ms can be similarly obtained. If the IDP select pin is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10pps an IDP of 800ms is obtained and at 20pps an IDP of 400ms is obtained.

The user can enter a number up to 22 digits long from a standard 3 x 4 XY matrix keypad (Figure 1). It is also possible to use a logic interface or a keyboard with common (Figure 2) for number entry. Antibounce protection circuitry is provided on chip (min. 9ms) to prevent false entry.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed 22.

Redialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key twice. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

Repertory Dialing

Dialing of a number stored in memory is initiated by going OFF hook and pushing the "#" key followed by the single digit address. Numbers can be cascaded after dialing of the first number is completed.

Table 1. S25610 Pin/Function Descriptions

Pin Functions	Pin Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	7 2, 3, 4, 1, 16, 17, 18	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 2. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 10ms).
Inter-Digit Pause Select (IPS)	15	One programmable line is available that allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 4. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 4.
Dial Rate Select (DRS)	14	A programmable line allows selection of two different output rates such as 7 or 14pps, 10 or 20pps, etc. See Tables 2 and 4.
Mark/Space (M/S)	12	This input allows selection of the mark/space ratio, as per Table 4.
Mute Out ($\overline{MUTE}$)	11	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.
Dial Pulse Out ($\overline{DP}$)	9	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator (R_E, C_D, R_D)	6, 7, 8	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	5	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	13, 10	These are the power supply inputs. The device is designed to operate from 1.5V to 3.5V.

Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)	
					$DRS = V_{SS}$	$DRS = V_{DD}$	$IPS = V_{SS}$	$IPS = V_{DD}$
5.5/11	1320	Select components in the ranges indicated in table of electrical specifications			5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680				7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920				8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
$(f_d/240)/(f_d/120)$	f_d				$(f_d/240)$	$(f_d/120)$	$\frac{1920}{f_i} \times 10^3$	$\frac{960}{f_i} \times 10^3$

Notes:
1. IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14pps, an IDP of either 1142ms or 571ms can be selected.

Operating Characteristics

Normal Dialing

Off Hook, [D1] , - - - - - - - [Dn]

Dial pulsing to start as soon as first digit is entered (debounced and detected on chip). Pause may be entered in the dialing sequence by pressing the "#" key. Total number of digits entered not to exceed 22. Numbers exceeding 22 digits can be dialed but only after the first 22 digits have been completely dialed out. In this case redialing function is inhibited.

Storing of a Telephone Number(s)

Numbers can be stored as follows:

Off Hook, [*] , [D1] , - - - - [Dn] , [*] , [LOC]

[*] , [D1] , - - - [Dn] , [*] , [LOC]

etc.

Earpiece is muted in this operation to alert the user that a store operation is underway.

Repertory Dialing

Off Hook, [#] , [LOC]

Numbers can be cascaded repeating [#] , [LOC] sequence after completion of dialing of present sequence. If an access pause has been stored in "LOC", dialing will halt until the "#" key is pushed again.

Redialing

Last number dialed can be redialed as follows:

Off Hook, [#] , [#]

Last number for this purpose is defined as the last number remaining in the buffer. Access pause is terminated by pushing the "#" key as usual.

Special Sequences

There are some special sequences that provide for mixed dialing or other features such as call disconnect, redial inhibit or memory clear as follows:

a. Normal dialing followed by repertory dialing

Off Hook, [D1] , - - - [Dn] - - - - - [*] , [#] , [LOC]

(wait for dialing to complete before pressing star key)

b. Normal dialing after repertory dialing or redialing

Off hook, [#] , [#] - - - - - [D1] - - - [Dn]

or

[LOC]

(wait for dialing to complete before pressing D1 key)

c. Disconnecting call

Off hook, - - - - - , [*] [#]

Pushing * and # keys simultaneously causes DP and mute outputs to go low and remain low until the keys are released. This causes a break in the line. If the keys are held down for a sufficiently long time (approx. 400ms), the call will be disconnected and new dial tone will be heard upon release of the keys. This feature is convenient when disconnecting calls by the normal method, i.e., hanging up the phone or depressing hookswitch is cumbersome.

d. Inhibiting future redialing of a normally dialed number

Off hook, [D1] - - - [Dn] - - - - - [*] , [*]

(wait for dialing to complete before pressing star key)

Pushing * key twice after normal dialing is completed instructs the device to clear the redial buffer.

e. To clear a memory location(s)

Off hook, [*] , [#] , [*] [LOC1] ,- - - [*] , [#] , [*] [LOCn]

Essentially this operation is equivalent to storing a pause in the memory location.

The various operating characteristics are summarized in Table 3.

Table 3. Summary of Operating Characteristics

1) Normal Dialing: off hook , D1 - - - - - Dn

2) Inhibit Redialing: off hook , D1 - - - Dn - - - - - - - - - - - - * , *
(wait for dialing to complete before pressing star key)

3) Redialing: off hook , # , #

4) Storing of Number(s): off hook , * , D1 , - - - Dn , * , LOC1 - - - - - -
- - * , D1 , - - - Dn , * , LOCn

5) Repertory Dialing: off hook , # , LOC1 - - - - - - - - - - - - # , LOCn
(wait for dialing to complete before pressing # key)

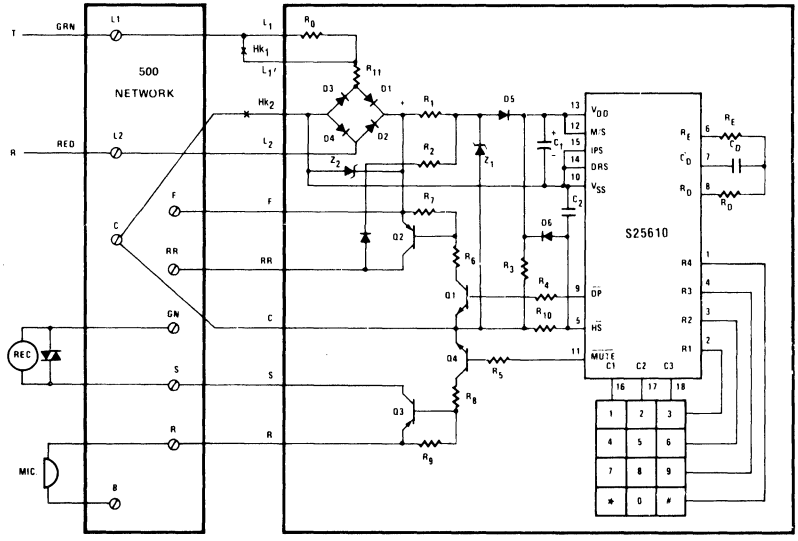
6) Normal Dialing + Repertory Dialing: off hook , D1 - - - Dn - - - - - - - - - - - - * , # , LOCn
(wait for dialing to complete before pressing star key)

7) Recall + Normal Dialing: off hook , # , # or LOCn , - - - - - - - - - - - - - D1 - - Dn
(wait for dialing to complete before pressing D1 key)

8) Call Disconnect: off hook , - - - - , * , #

9) Clear Memory Location(s): off hook , * , # , * , LOCn - - - * , # , * , LOCn

Figure 4. Repertory Dialer Circuit with Redial



R_0 = 10-20MΩ, R_1 = 150kΩ, R_2 = 2kΩ
R_3 = 470kΩ, R_4, R_5 = 10kΩ, R_{10} = 47kΩ
R_6, R_8 = 2kΩ, R_7, R_9 = 30kΩ, R_{11} = 20Ω, 2W
Z_1 = 3.9V, D_1—D_4 = IN4004, D_5, D_6, D_7 = IN914, C_1 = 15μF

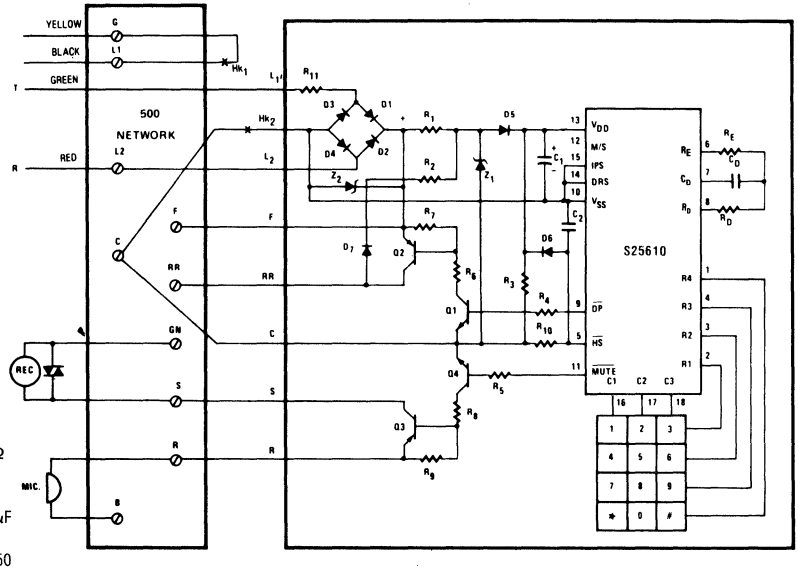
R_E = R_D = 750kΩ, C_D = 270pF, C_2 = 0.01μF
Q_1, Q_4 = 2N5550 TYPE Q_2, Q_3 = 2N5401 TYPE
Z_2 = IN5379 110V ZENER OR 2XIN4758

Table 4.

Function	Pin Designation	Input Logic Level	Selection
Dial Pulse Rate Selection	DRS	V_{SS} V_{DD}	(f/240)pps (f/120)pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	$\frac{960}{f}$ s $\frac{1920}{f}$ s
Mark/Space Ratio	M/S	V_{SS} V_{DD}	33⅓/66⅔ 40/60
On Hook/Off Hook	HS	V_{DD} V_{SS}	On Hook Off Hook

NOTE: f is the oscillator frequency and is detemined as shown in Figure 5.

Figure 5. Repertory Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



$R_1 = 10\text{-}20M\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$
$R_{10} = 47k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, D_1—D_4 = IN4004
D_5, D_6, D_7 = IN914, $C_1 = 15\mu F$
R_E, $R_D = 750k\Omega$, $C_D = 270pF$
$C_2 = 0.01\mu F$, Q_1, Q_4 = 2N5550
Q_2, Q_3 = 2N5401
Z_2 = 150V ZENER OR VARISTOR TYPE GE MOV150

AMI®

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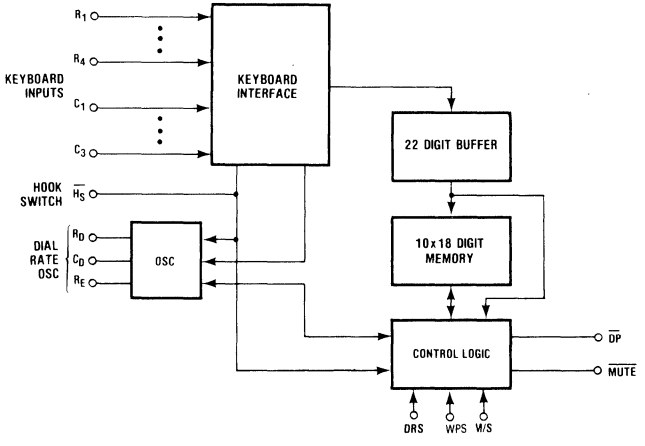
S25610E

SINGLE CHIP REPERTORY DIALER

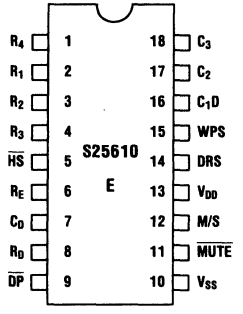
Features

- ☐ Modified Version of the S25610 Repertory Dialer. Optimized for European Applications
- ☐ Ten 18-Digit Number Memories Plus Last Number Redial (22 Digit) Memory On Chip.
- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines.
- ☐ Inexpensive R-C Oscillator Design With Accuracy Better Than ±5% Over Temperature and Unit-Unit Variations.
- ☐ Independent Select Inputs for Variation of Dialing Rates (10pps/20pps), Mark/Space Ratio (33⅓-66⅔/40-60)
- ☐ Can Interface With Inexpensive XY Matrix or Standard 2 of 7 Keyboard With Common. Also Capable of Logic Interface (Active High).
- ☐ Mute and Pulse Drivers On Chip.
- ☐ Call Disconnect by Pushing * and # Keys Simultaneously.
- ☐ Pin Selectable Access Pause/Wait Functions
- ☐ Auto Pause Insertion

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leqslant V_{DD} - V_{SS} \leqslant 3.5V$ unless otherwise specified.

Symbol	Parameter	V_{DD}-V_{SS} (Volts)	Min.	Max.	Units	Conditions
	Operating Voltage					
V_{DD}	Data Retention		1.0		V	On Hook, ($\overline{HS} = V_{DD}$)
V_{DD}	Non Dialing State		1.5	3.5	V	Off Hook, Oscillator Not Running
V_{DD}	Dialing State		2.0	3.5	V	Off Hook, Oscillator Running
	Operating Current					
I_{DD}	Data Retention	1.0		2.0	μA	On Hook, ($\overline{HS} = V_{DD}$)
I_{DD}	Non Dialing	1.5		10	μA	Off Hook ($\overline{HS} = V_{SS}$), Oscillator Not Running, Outputs Not Loaded
I_{DD}	Dialing	2.0 3.5		100 500	μA μA	Off Hook, Oscillator Running, Outputs Not Loaded
	Output Current Levels					
I_{OLDP}	DP Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHDP}	DP Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	MUTE Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHM}	MUTE Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
fo	Oscillator Frequency	2.0		10	kHz	
Δfo/fo	Frequency Deviation	2.0 to 2.75 2.75 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50k\Omega \leqslant R_D \leqslant 750k\Omega$; $100pF \leqslant C_D{}^* \leqslant 1000pF$; $750k\Omega \leqslant R_E \leqslant 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD} - V_{SS}$)	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of ($V_{DD} - V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

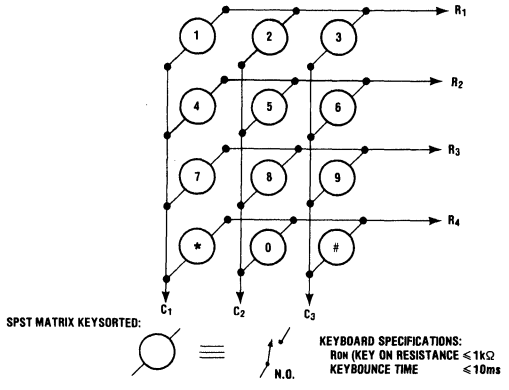
The device contains an oscillator circuit that requires three external components; two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including

the "on hook" condition. For a dialing rate of 10pps the oscillator should be adjusted to 2400Hz. Typical values of external components for this are R_D, R_E = 750kΩ and C_D = 270pF. It is recommended that the tolerance of resistors to be 1% and capacitor to be 5% to insure a ±10% tolerance of the dialing rate in the system.

Keyboard Interface

The S25610 employs a scanning technique to determine a key closure. This permits interface to a DPCT (Double Pole Common Terminal) keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2),or a XY matrix. A high level on the appropriate row and column inputs constitutes a key closure for logic interface.

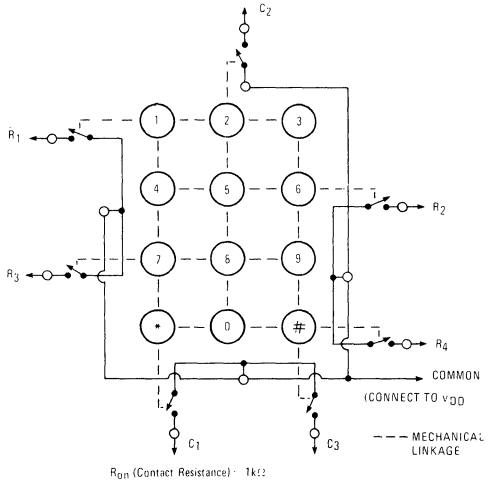
Figure 1. SPST Matrix Keyboard Arranged in a Row, Column Format



On Hook Operation: The device is continuously powered through a 10-20MΩ resistor during the on hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed. DP and mute outputs are low in the on hook state.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

Figure 2. Standard Telephone Pushbutton Keyboard



Off Hook Operations: The device is continuously powered through a 150kΩ resistor during off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The DP output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during this pulse break. The MUTE output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20pps can be achieved. Dialing rates of 7 and 14pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

Operating Characteristics

Normal Dialing

Off Hook, [D1] , - - - - - - - [Dn]

Dial pulsing to start as soon as first digit is entered and debounced on the chip. Total number of digits entered not to exceed 22. Numbers exceeding 22 digits can be dialed but only after the first 22 digits have been completely dialed out. Access wait or pause can be inserted by pressing the "#" key. Any number of waits or pauses can be entered as long as the total number of digits does not exceed 22. Additionally in the "pause" mode, pause is inserted automatically (two maximum) if no further digits are entered by the time mute turns off. (Figure 3.)

Storing of a Telephone Number(s)

Numbers can be stored as follows:

Off Hook, [*] , [D1] , - - - - [Dn] , [*] , [LOC]

[*] , [D1] , - - - [Dn] , [*] , [LOC]

Access wait/pause can be inserted in the stored sequence by pushing the "#" key. Any number of waits/pauses may be stored as long as the total number of digits does not exceed 22.

Repertory Dialing

Off Hook, [#] , [LOC]

Numbers can be cascaded repeating [#] , [LOC] sequence after completion of dialing of present sequence. If an access pause has been stored in "LOC", dialing will halt until the "#" key is pushed again. If an access pulse is detected dialing will stop for the selected duration.

Redialing

Last number dialed can be redialed as follows:

Off Hook, [#] , [#]

Last number for this purpose is defined as the last number remaining in the buffer. Access pause is terminated by pushing the "#" key as usual. If the device is operated in the "pause" mode and if an access pause was automatically inserted during normal dialing, during redialing the dialing will be stopped for the pause duration selected.

Special Sequences

There are some special sequences that provide for mixed dialing or other features such as call disconnect, redial inhibit or memory clear as follows:

a. Normal dialing followed by repertory dialing

Off Hook, [D1] , - - - [Dn] - - - - - [*] , [#] , [LOC]

(wait for dialing to complete before pressing star key)

b. Normal dialing after repertory dialing or redialing

Off hook, [#] , [#] - - - - - [D1] - - - [Dn]

or

[LOC]

(wait for dialing to complete before pressing D1 key)

c. Disconnecting call

Off hook, - - - - - , [*] [#]

Pushing * and # keys simultaneously causes DP and mute outputs to go low and remain low until the keys are released. This causes a break in the line. If the keys are held down for a sufficiently long time (approx. 400ms), the call will be disconnected and new dial tone will be heard upon release of the keys. This feature is convenient when disconnecting calls by the normal method, i.e., hanging up the phone or depressing hookswitch is cumbersome.

d. Inhibiting future redialing of a normally dialed number

Off hook, [D1] - - - [Dn] - - - - - [*] , [*]

(wait for dialing to complete before pressing star key)

Pushing * key twice after normal dialing is completed instructs the device to clear the redial buffer.

e. To clear a memory location(s)

Off hook, [*] , [#] , [*] [LOC1] ,- - - [*] , [#] , [*] [LOCn]

Essentially this operation is equivalent to storing a pause in the memory location.

The various operating characteristics are summarized in Table 3.

Table 3. Summary of Operating Characteristics

1) Normal Dialing: off hook , D1 - - - - - Dn

2) Inhibit Redialing: off hook , D1 - - - Dn - - - - - - - - - - - - * , *
(wait for dialing to complete before pressing star key)

3) Redialing: off hook , # , #

4) Storing of Number(s): off hook , * , D1 , - - - Dn , * LOC1 - - - - - -
- - * , D1 , - - - Dn , * LOCn

5) Repertory Dialing: off hook , # LOC1 - - - - - - - - - - - - # , LOCn
(wait for dialing to complete before pressing # key)

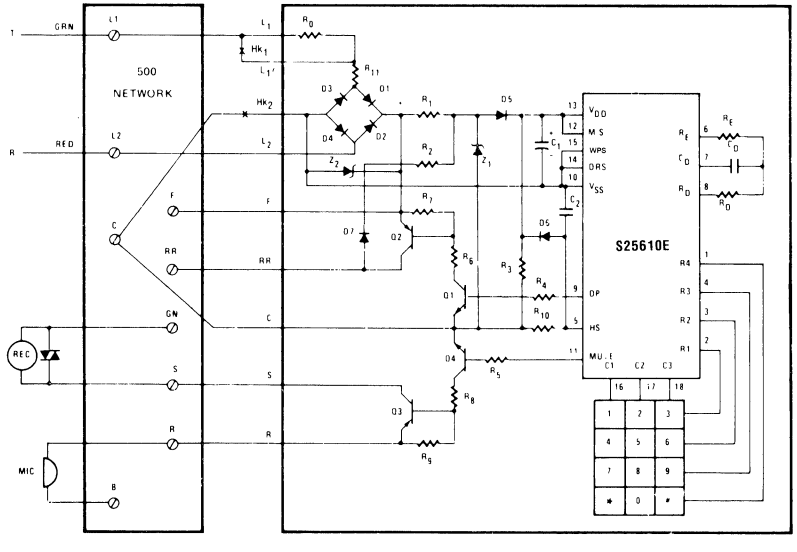
6) Normal Dialing + Repertory Dialing: off hook , D1 - - - Dn - - - - - - - - - - - - * , # , LOCn
(wait for dialing to complete before pressing star key)

7) Recall + Normal Dialing: off hook , # , # or LOCn , - - - - - - - - - - - - - D1 - - Dn
(wait for dialing to complete before pressing D1 key)

8) Call Disconnect: off hook , - - - - , * #

9) Clear Memory Location(s): off hook , * , # , * , LOCn - - - * , # , * LOCn

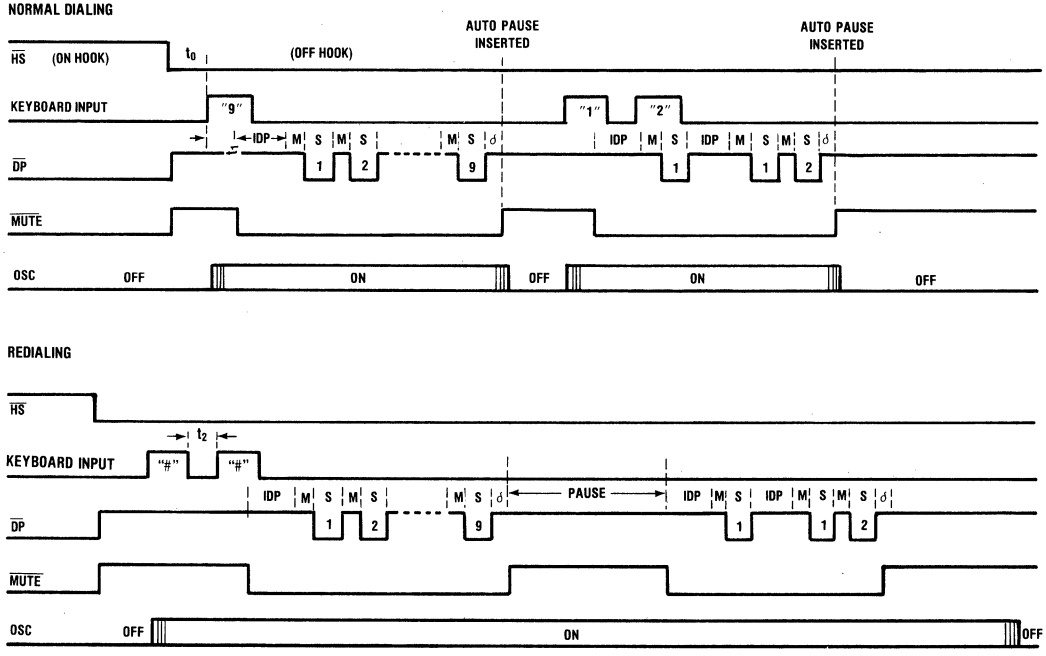
Figure 4. Repertory Dialer Circuit with Redial



$R_0 = 10\text{-}20M\Omega$. $R_1 = 150k\Omega$. $R_2 = 2k\Omega$
$R_3 = 470k\Omega$. R_4. $R_5 = 10k\Omega$. $R_{10} = 47k\Omega$
R_6. $R_8 = 2k\Omega$. R_7. $R_9 = 30k\Omega$. $R_{11} = 20\Omega$. 2W
$Z_1 = 3.9V$. $D_1 - D_4 = IN4004$. D_5. D_6. $D_7 = IN914$. $C_1 = 15\mu F$

$R_E = R_D = 750k\Omega$. $C_D = 270pF$. $C_2 = 0.01\mu F$
Q_1. $Q_4 = 2N5550$ TYPE Q_2. $Q_3 = 2N5401$ TYPE
$Z_2 = IN5379$ 110V ZENER OR 2XIN4758

Figure 3. Timing (Dial, Redial)



t_1 : KEY DEBOUNCE TIME : 10ms
t_2 : KEY RELEASE TIME : 2ms
ó : PULSE TURNOFF TO MUTE TURNOFF DELAY TIME: 8ms (10pps)/40ms (20pps)
t_0 : OFF HOOK TO KEYBOARD INPUT DELAY TIME: 2ms

NOTE: TYPICAL WAVEFORMS DURING NORMAL DIALING AND REDIALING
(ASSUMES PAUSE OPTION IS SELECTED)
(TIME BASED ON OSCILLATOR FREQUENCY OF 2400Hz)

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and it is a function of the dialing rate selected by the dial rate select input. If the oscillator is set to 2400Hz so that a dialing rate of 10pps is obtained with DRS = V_{SS}. Then an IDP of 800ms is automatically selected. Switching the dialing rate to 20pps (DRS = V_{DD}) will lower the IDP to 400ms.

The user can enter a number up to 22 digits long from a standard 3 x 4 XY matrix keypad (Figure 1). It is also possible to use a logic interface or a keyboard with common (Figure 2) for number entry. Antibounce protection circuitry is provided on chip (min. 9ms) to prevent false entry.

Table 1. S25610E Pin/Function Descriptions

Pin Functions	Pin Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	2, 3, 4, 1, 16, 17, 18	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 2. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 10ms).
Wait-Pause Select (WPS)	15	This is a Tri-Function input pin. Leaving it open selects the access wait function. Connect to V_{DD} selects access pause duration of 3.2sec. and connection to V_{SS} selects the access pause duration of 6.4sec. For detailed description of wait/pause functions see Operating Characteristics.
Dial Rate Select (DRS)	14	A programmable line allows selection of two different output rates such as 7 or 14pps, 10 or 20pps, etc. See Tables 2 and 4. Interdigit Pause (IDP) is a function of the selected dialing rate.
Mark/Space (M/S)	12	This input allows selection of the mark/space ratio, as per Table 4.
Mute Out ($\overline{MUTE}$)	11	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing. Normally it is "high" and "low" during dialing. It is "low" on hook.
Dial Pulse Out ($\overline{DP}$)	9	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise. On hook it is "low".
Dial Rate Oscillator	6, 7, 8	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	5	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.It is debounced during dialing. An interruption of 150ms or less will be ignored while that excess of 300ms will cause the device to go into standby condition.
Power (V_{DD}, V_{SS})	13, 10	These are the power supply inputs. The device is designed to operate from 1.5V to 3.5V.

Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

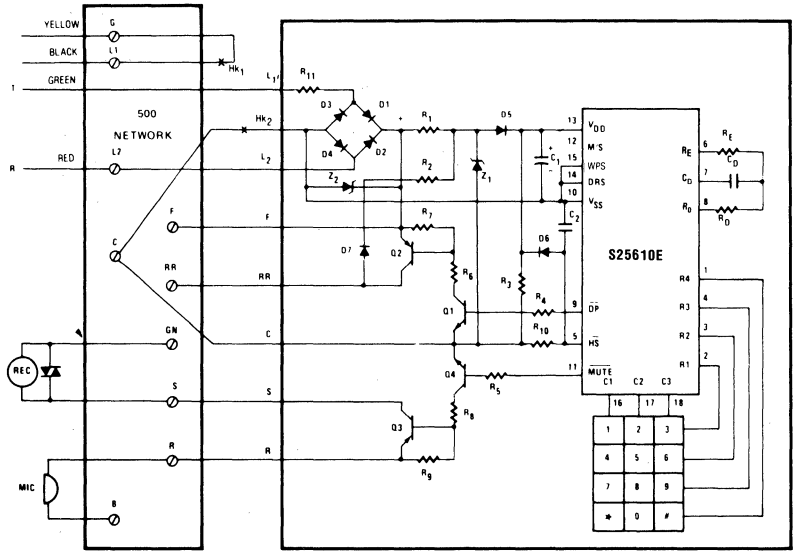
Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)
					DRS = V_{SS}	DRS = V_{DD}	
5.5/11	1320	Select components in the ranges indicated in table of electrical specifications			5.5	11	1454 / 727
6/12	1440				6	12	1334 / 667
6.5/13	1560				6.5	13	1230 / 615
7/14	1680				7	14	1142 / 571
7.5/15	1800				7.5	15	1066 / 533
8/16	1920				8	16	1000 / 500
8.5/17	2040				8.5	17	942 / 471
9/18	2160				9	18	888 / 444
9.5/19	2280				9.5	19	842 / 421
10/20	2400	750	750	270	10	20	800 / 400
$(f_d/240)/(f_d/120)$	f_d				$(f_d/240)$	$(f_d/120)$	$\frac{1920}{f_i} \times 10^3 \Big/ \frac{960}{f_i} \times 10^3$

Notes:
1. IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14pps, an IDP of either 1142ms or 571ms can be selected.

Table 4.

Function	Pin Designation	Input Logic Level	Selection
Dial Rate Selection and	DRS	V_{DD}	$\frac{960}{f}$ s IDP (f/120)pps
Inter-Digit Pause Selection			(f/240)pps
		V_{SS}	$\frac{1920}{f}$ s IDP
Mark/Space Ratio	M/S	V_{SS}	33⅓/66⅔
		V_{DD}	40/60
On Hook/Off Hook	$\overline{HS}$	V_{DD}	On Hook
		V_{SS}	Off Hook

Figure 5. Repertory Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



R_1 = 10-20MΩ, R_2 = 2kΩ
R_3 = 470kΩ, R_4, R_5 = 10kΩ
R_6, R_8 = 2kΩ, R_7, R_9 = 30kΩ
R_{10} = 47kΩ, R_{11} = 20Ω, 2W
Z_1 = 3.9V, D_1—D_4 = IN4004
D_5, D_6, D_7 = IN914, C_1 = 15μF
R_E, R_D = 750kΩ, C_D = 270pF
C_2 = 0.01μF, Q_1, Q_4 = 2N5550
Q_2, Q_3 = 2N5401
Z_2 = 150V ZENER OR VARISTOR TYPE GE MOV150

Advanced Product Description **S25910**

DTMF REPERTORY DIALER

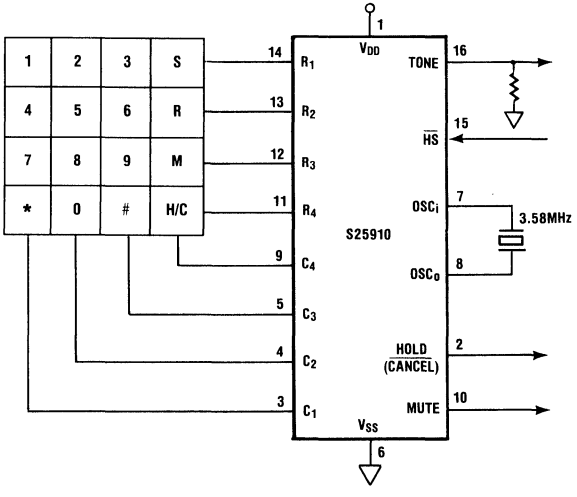
Features

- ☐ Ten 16-Digit Number Memories Plus Last Number Redial Buffer
- ☐ Store, Redial, Memory Dial and Hold/Cancel Functions in a Separate Column (Column 4) of the 16 Button X-Y Keypad
- ☐ Permits Dialing of "*" and "#" Keys as Other Digit Keys
- ☐ Extremely Low Data Retention Current (1μA Max) Eliminates Battery Backup Requirement and Provides Full Telephone Line Power Operation
- ☐ Similar to the S2559 Family Tone Generators, With Only 2 Changed Pins.
- ☐ Permits Cascading and Mixing of Operations

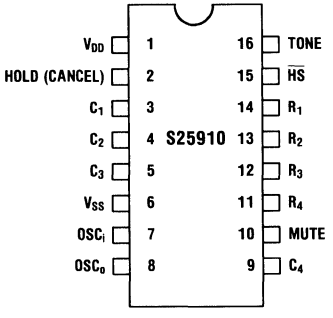
General Description

The S25910 DTMF Repertory Dialer is a CMOS integrated circuit that can provide storage and recall of previously entered numbers as well as perform the normal DTMF dialing functions. It can store ten 16-digit numbers as well as the last number dialed. Using a 4 x 4 keyboard for ease of control, this circuit will dial the * and # keys as well as the 10 digits and is completely telephone line powered.

Functional Diagram



Pin Configuration



Summary of Operations

Normal Dialing

↑, [D1] - - - - [Dn]

Number length can exceed 16 digits. In such a case redial will be inhibited.

Redial

↑, [R]

Store

↑, [S] [L1] [D1] - - - [Dn] [S] [L2] [D1] - - [Dn]

a. Cascading is permitted during store sequence.

Memory Dial

↑, [M] [L1] - - - - - - - - - - [M] [L2] - - - - -

(wait for dialing to complete)

a. Cascading of numbers is permitted as above

Mixed dialing

↑, Normal dialing, memory dialing

↑, redial, memory dial

Hold

↑, Voice mode - - - [H] - - - - - - - - - - [H]

Initiate Terminate

a. On the first depression of hold key both hold and mute outputs should go high and stay high until the hold mode is cleared by a second depression of hold key.

b. An alternating alerting single tone should appear on the tone out pin during hold mode with a rep. rate of approximately 800ms on/off.

Cancel

↑, Voice Mode [C] - - -

Cancel button depression should output a low level on the cancel output as long as the key is held down. Tone output must be at V_{SS} and oscillator should be stopped so as to minimize current drain below 200μA.

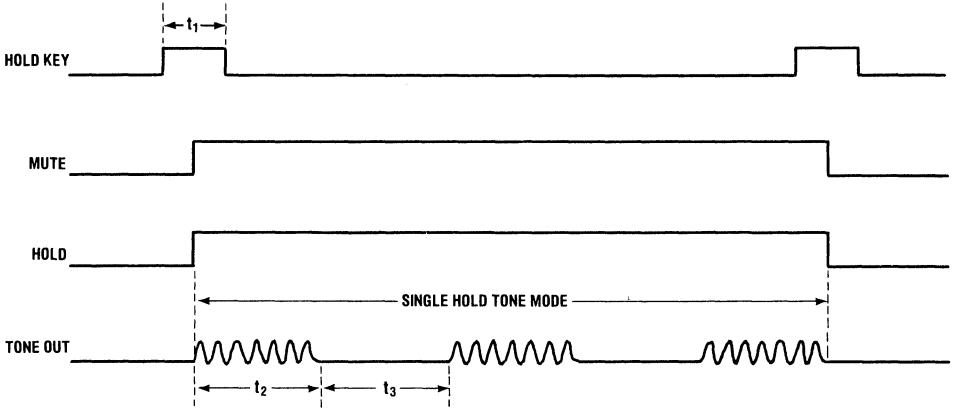
Electrical Specifications

Similar to S2559F with the addition of data retention current specification.

NOTE: ↑, indicates going off hook or picking up the handset.

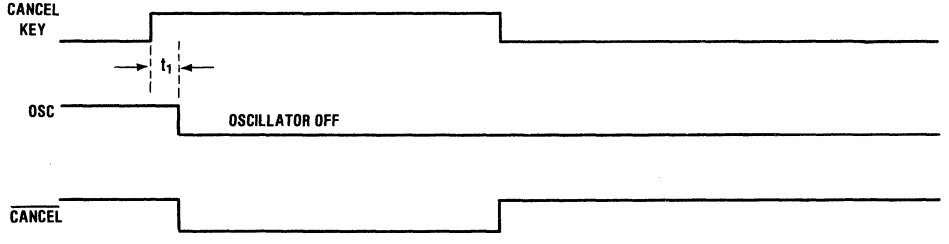
Waveforms

Hold Waveform Details



t_1: 10ms MIN
t_2, t_3: APPROXIMATELY 800ms

Cancel Waveform Details



t_1: DEBOUNCE TIME 10ms MIN

AMI

A Subsidiary of Gould Inc.

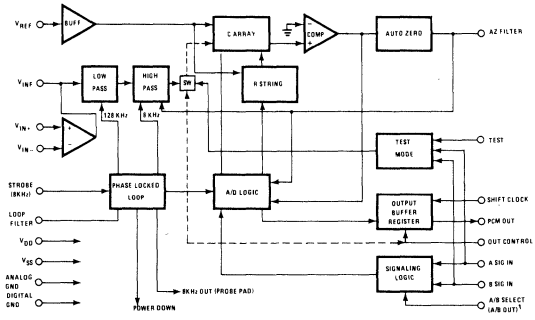
S3501/S3501A, S3502/S3502A

SINGLE CHANNEL μ-LAW PCM CODEC/FILTER

Features

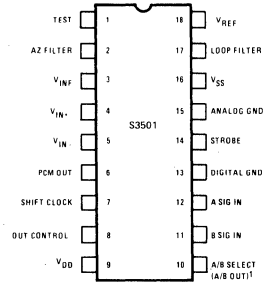
- ☐ CMOS Process for Low Power Dissipation
- ☐ Full Independent Encoder with Filter and Decoder with Filter Chip Set
- ☐ Meets or Exceeds AT&T D3 and CCITT G. 711 and G. 733 Specifications
- ☐ On-Chip Dual Bandwidth Phase-Lock Loop Derives All Timing and Provides Automatic Power Down
- ☐ Low Absolute Group and Relative Delay Distortion
- ☐ Single Negative Polarity Voltage Reference Input
- ☐ Encoder with Filter Chip Has Built-In Dual Speed Auto Zero Circuit with Rapid Acquisition During Power Up that Eliminates Long Term Drift Errors and Need for Trimming
- ☐ Serial Data Rates from 56kb/s to 3.152Mb/s at 8kHz Nominal Sampling Rate
- ☐ Programmable Gain Input/Output Amplifier Stages
- ☐ CCIS* Compatible A/B Signaling Option—S3501A/S3502A

S3501 Block Diagram Encoder with Filter



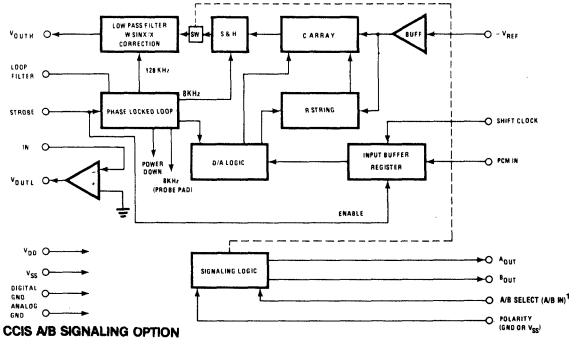
1 CCIS A/B SIGNALING OPTION

Pin Configuration



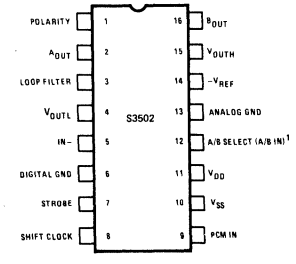
1 CCIS A/B SIGNALING OPTION-S3501A

S3502 Block Diagram Decoder with Filter



CCIS A/B SIGNALING OPTION

Pin Configuration



1 CCIS A/B SIGNALING OPTION-S3502A

General Description

The S3501 and S3502 form a monolithic CMOS Companding Encoder/Decoder chip set designed to implement the per channel voice frequency CODECS used in PCM Channel Bank and PBX systems requiring a μ-255 law transfer characteristic. Each chip contains two sections: (1) a band-limiting filter, and (2) an analog ↔ digital conversion circuit that conforms to the μ-255 law transfer characteristic. Transmission and reception of 8-bit data words containing the analog information is typically performed at 1.544Mb/s rate with analog sampling occurring at 8kHz rate. A strobe input is provided for synchronizing the transmission and reception of time multiplexed PCM information of several channels over a single transmission line.

*Common Channel Interoffice Signaling

S3501 Encoder with Filter Functional Description

S3501 Encoder with Filter chip consists of (1) a band-pass filter with D3 filter characteristic, (2) an analog to digital converter that uses a capacitor array, (3) a phase-lock loop that generates all internal timing signals from the externally supplied strobe signal and (4) control logic that performs miscellaneous logic functions.

The band-limiting filter is a 5th order low pass elliptic filter followed by a third order Chebyshev high pass filter. The combined response characteristic (Figure 3) exceeds the D3 filter specifications. Note that the loss below 65Hz is at least 25dB which helps minimize the effect of power frequency induced noise.

The analog to digital converter utilizes a capacitor array based on charge redistribution technique (Ref. 1) to perform the analog to digital conversion with a μ-255 law transfer characteristic (see Figure 4).

The timing signals required for the band-pass filter (128kHz and 8kHz) and analog to digital converter (1.024MHz) are generated by a phase-lock loop comprising a VCO, a frequency divider, a loop filter and a lock detector. The loop locks to the externally supplied 8kHz strobe pulses. In the absence of the strobe pulses, the lock detector detects the unlocked condition and forces the device into a power-down mode thereby reducing power dissipation to a minimum. Thus power-down mode is easily implemented by simply gating the strobe pulses "off" when the channel is idle. The lock-up time, when strobe pulses are gated "on", is approximately 20ms. During this time the device outputs an idle code (all 1's) until lock-up is achieved. Note that signaling information is not transmitted during this time.

The control logic implements the loading of the output shift register, gating and shifting of the data word, signaling logic and other miscellaneous functions. A new analog sample is acquired on the rising edge of the strobe pulse. The data word representing the previous analog sample is loaded into the output shift register at this time and shifted out on the positive transitions of the shift clock during the strobe "on" time. (See Figure 1.) The signaling information is latched immediately after the A/B select input makes a transition. The "A" signaling input is selected after a positive transition and the "B"signaling input is selected after a negative transition. Signaling information is transmitted in the eighth bit position (LSB) of the next frame. (See Figures 1 and 2.) In the CCIS compatible A/B signaling option, the A bit is transmitted during the first data bit time. B bit is transmitted during the remaining 7-bit times. (See Figures 1 and 2.)

"All zero" code suppression is provided so that negative input signal values between the decision value numbers 127 and 128 are encoded as "00000010" after signalling insertion has been done.

S3501 Encoder with Filter Pin Function Descriptions

Strobe: (Refer to Figure 1 for timing diagram.) This TTL compatible input is typically driven by a pulse stream of 8kHz rate. Its active state is defined as a logic 1 level and should be active for a duration of 8 clock cycles of the shift clock. A logic "1" initiates the following functions: (1) instructs the device to acquire a new analog sample on the rising edge of the signal (logic 0 to logic 1 transition); (2) instructs the device to output the data word representing the previous analog sample onto the PCM-out pin serially at the shift clock rate during its active state; (3) forces the PCM-out buffer into an active state. A logic "0" forces the PCM-out buffer into a high impedance state if the Out Control pin is wired to V_{DD}. This input provides the sync information to the phase-lock loop from which all internal timing is developed. The absence of the strobe conveys power-down status to the device. (See functional description of the phase-lock loop for details.)

Shift Clock: This TTL compatible input is typically a square wave signal at 1.544MHz. The device can operate with clock rates from 56kHz (as in the single channel 7-bit PCM system) to 3.152MHz (as in the T1-C carrier system). Data is shifted out of the PCM-out buffer on the rising edges of the clock after a valid logic 0 to logic 1 transition of the strobe signal.

AMI

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S3506/S3507/S3507A

CMOS SINGLE CHIP μ-LAW/A-LAW SYNCHRONOUS COMBO CODECS WITH FILTERS

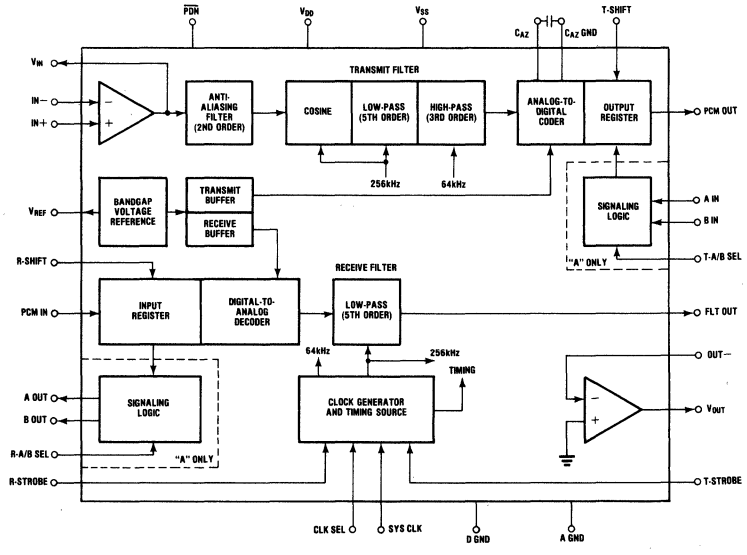
Features

- ☐ Independent Transmit and Receive Sections With 75dB Isolation
- ☐ Low Power CMOS 80mW (Operating) 8mW (Standby)
- ☐ Stable Voltage Reference On-Chip
- ☐ Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- ☐ Input Analog Filter Eliminates Need for External Anti-Aliasing Prefilter
- ☐ Input/Output Op Amps for Programming Gain
- ☐ Output Op Amp Provides ±3.1V into a 600Ω Load or Can Be Switched Off for Reduced Power (70mW)
- ☐ Special Idle Channel Noise Reduction Circuitry for Crosstalk Suppression
- ☐ Encoder has Dual-Speed Auto-Zero Loop for Fast Acquisition on Power-Up
- ☐ Low Absolute Group Delay = 450μsec. @ 1kHz

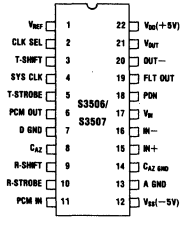
General Description

The S3506 and S3507 are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analog↔digital conversion circuits that conform to the desired transfer characteristic. The S3506 provides the European A-Law companding and the S3507 provides the North American μ-Law companding characteristic.

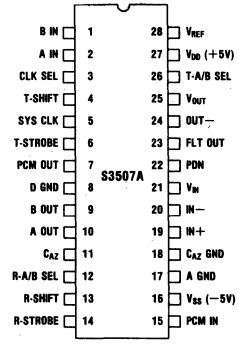
Block Diagram



Pin Configuration (22 Pin)



Pin Configuration (28 Pin)



General Description (Continued)

These circuits provide the interface between the analog signals of the subscriber loop and the digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ±5V.

For a sampling rate of 8kHz, PCM input/output data rate can vary from 64kb/s to 2.1Mb/s. Separate transmit/receive timing allows synchronous or time-slot asynchronous operation.

In 22-pin cerdip or ceramic packages (.400" centers) the S3506/S3507 are ideally suited for PCM applications: Exchange, PABX, Channel bank or Digital Telephone as well as fiber optic and other non-telephone uses. A 28-pin version, the S3507A, provides standard μ-Law A/B signaling capability. These devices are also available in a 28-pin chip carrier. Extended temperature range versions can be supplied.

Functional Description

The simplified block diagram of the S3506/S3507 appears on page one. The device contains independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. A bandgap voltage generator supplies the reference level for the conversion process.

Transmit Section

Input analog signals first enter the chip at the uncommitted op amp terminals. This op amp allows gain trim to be used to set 0TLP in the system. From the V_{IN} pin the signal enters the 2nd order analog antialiasing filter. This filter eliminates the need for any offchip filtering as it provides attenuation of 34dB (typ.) at 256kHz and 46dB (typ.) at 512Hz. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 256kHz, followed by a 3rd Order High-Pass Filter clocked at 64kHz. The resulting band-pass characteristics meet the CCITT G.711, G.712 and G.733 specifications. Some representative attenuations are >26dB (typ) from 0 to 60Hz and >35dB (typ) from 4.6kHz to 100kHz. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The polarity of the incoming signal selects the appropriate polarity of the reference voltage. The successive approximation analog-to-digital conversion process requires 9½ clock cycles, or about 72μs. A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

The PCM data word is formatted according to the μ-law companding curve for the S3507 with the sign bit and the ones complement of the 7 magnitude bits according to the AT&T D3 specification. In the S3506 the PCM data word is formatted according to the A-Law companding curve with alternate mark inversion (AMI), meaning that the even bits are inverted per CCITT specifications.

Included in the circuitry of the S3507/S3507A is "All Zero" code suppression so that negative input signal values between decision value numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronization by T1 line clock recovery circuitry as there are never more than 15 consecutive zeros. The 8-bit PCM data is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz to 2.048MHz, clocks the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 256kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic hybrids directly as long as the impedance is greater than 47kΩ. When used in this fashion the low impedance output amp can be switched off for a savings in power consumption. When it is required to drive a 600Ω load the output is provided by the output buffer op amp.

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Advanced Product Description **RTDS28212**

REAL-TIME DEVELOPMENT SYSTEM

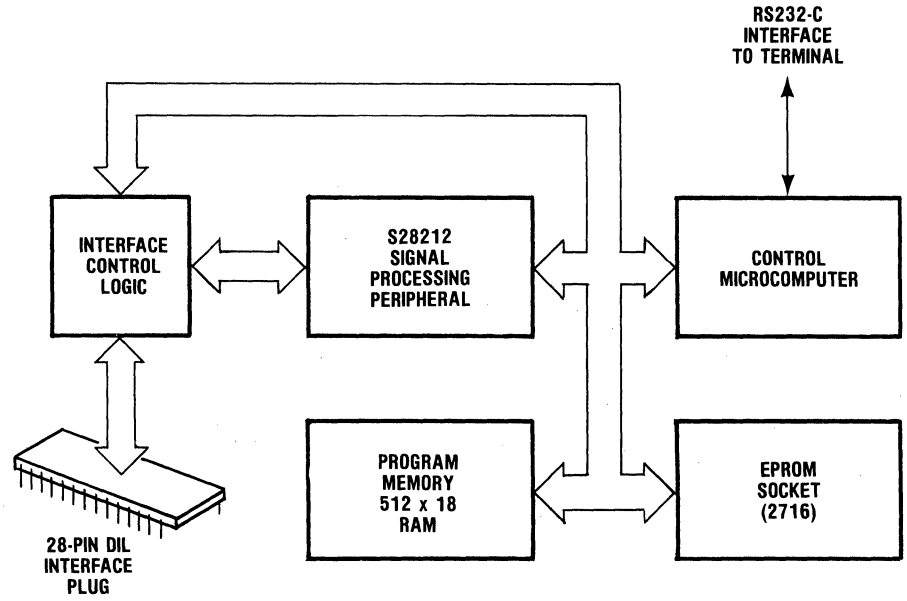
Features

- ☐ Real-Time In-Circuit Emulation of S28211 SPP
- ☐ Full Status Readout Capability for Easy Program Debug
- ☐ Allows Program to be Stopped at I/O Flag or Breakpoint
- ☐ Interfaces to Control Terminal Via RS232C Interface
- ☐ Program may be Stored in On-Board EPROM for Stand-Alone Operation

General Description

The RTDS28212 is a single board real-time in-circuit-emulator for the S28211 Signal Processing Peripheral (SPP). It is based on the S28212 version of the chip which allows programs stored in an external memory to be executed at full speed. In the RTDS28212 the memory is a high speed RAM, which may be loaded from the control terminal. After the program is assembled it can be loaded via the RS232C link. A cross-assembler is provided to generate the machine-code program from the mnemonic assembly language.

System Block Diagram



Data ROM Contents

The 128 word data ROM built into the S28212 contains a number of useful tables and constants. The ROM contents are listed in Table 1 below.

Table 1. Data ROM Contents.

BASE (B) ↓	→ DISPLACEMENT (D) 4	5	6	7
0	$0084	$0001	$FF00	$0000
1	$0000	$1001	$FE00	$0605
2	$0800	$2001	$FC00	$0C0A
3	$2000	$3001	$F800	$1210
4	$4000	$4001	$F000	$1815
5	$1000	$5001	$E000	$1E1A
6	$7FFF	$6001	$C000	$241F
7	$3000	$7001	$8000	$2A25
8	$00F0	$0000	$4200	$302A
9	$0070	$0000	$FF7C	$362F
10	$0030	$0000	$7F00	$3C34
11	$0010	$0000	$0100	$423A
12	$8070	$0000	$8284	$483F
13	$F830	$0000	$5A82	$4E44
14	$0000	$0000	$6EDA	$544A
15	$0000	$0000	$6487	$5A4F
16	$0000	$0000	$7FFF	$8000
17	$0000	$0C8C	$7F62	$4000
18	$0000	$18F9	$7D8A	$2AAA
19	$0000	$2528	$7A7D	$2000
20	$0000	$30FC	$7642	$1999
21	$0000	$3C57	$70E3	$1555
22	$0000	$471D	$6A6E	$1249
23	$0000	$5134	$62F2	$1000
24	$0000	$5A82	$5A80	$0E38
25	$0000	$62F2	$5134	$0CCC
26	$0000	$6A6E	$4717	$06A2
27	$0000	$70E3	$3C57	$0000
28	$0000	$7642	$30FC	$4580
29	$E800	$7A7D	$2528	$0000
30	$4000	$7D8A	$18F9	$0000
31	$6487	$7F62	$0C8C	$0000

Marked Blocks.

Block marked in area (B 0, D 4-6) to (B 6, D 4), (B 7, D 5), and (B 12, D 6): This is a lookup table used in PCM μ-law to linear and linear to μ-law conversions. Block marked in area (B 0, D 7) to (B 26, D 7): This is a lookup table used in linear to decibel conversion. Block marked in area (B 16, D 5-6) to (B 31, D 5-6): This is a sine/cosine lookup table. Hex 6487 = PI/4.
(Note: The S28212 data ROM is the same as that used in the S28215 Digital Filter/ Utility Peripheral.)

AMI®

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Advanced Product Description **SSPP28211**

SOFTWARE SIMULATOR/ASSEMBLER PROGRAM PACKAGE

Features

- ☐ Provides Exact Simulation of Operation of AMI S28211 Signal Processing Peripheral
- ☐ Written in ANSI Fortran IV for Maximum Portability
- ☐ Runs on Any 16-Bit or Larger Computer With > 28K Memory and Fortran IV Compiler
- ☐ Software Compatible with Real Time Development System (RTDS28212)
- ☐ Allows Continuous or Step-by-Step Operation
- ☐ Allows Setting of Breakpoints on All Major Flags
- ☐ Trace Buffer Allows Storage and Display of Status of Previous 50 Instructions During Continuous Operation

General Description

The SSPP28211 is a software simulator for the AMI S28211 Signal Processing Peripheral (SPP). For information on the SPP chip please refer to the S28211 Advanced Product Description. The program is written in ANSI Standard Fortran for maximum portability. The machine specific software is reduced to a minimum and is available for several popular ranges of computers including Burroughs 7700, PRIME 400, and Amdahl 470 (IBM compatible). Experienced Fortran programmers will have no difficulty in writing these small routines for other machines.

The SSPP28211 package allows the user to simulate the operation of the S28211 chip either in a step mode or free running, with or without breakpoints. Data I/O for the simulation may be provided by means of files or directly from the terminal. An assembler allows the user to input the SPP program (in SPP Assembly Language) and the memory data either from a file or from the keyboard. The assembly listing may be dumped to file which can then be used to generate the ROM mask for the S28211 by AMI. During simulation a trace buffer may be used to store the last 50 (maximum) instructions executed. This greatly facilitates continuous simulation in conjunction with the breakpoints which may be set on (1) any individual instruction (2) the input flag (3) the output flag (4) overflow in the accumulator. The trace feature, either using the trace buffer or in the step-by-step mode, gives the user the complete status of the simulation, including the last instruction executed and the conditions of all internal registers, counters, latches, and busses.

Software generated by the SSPP28211 is totally compatible with the RTDS28211 Real-Time Development System, allowing files to be transferred from one system to the other without modification.

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Advanced Product Description **S28211**

SIGNAL PROCESSING PERIPHERAL

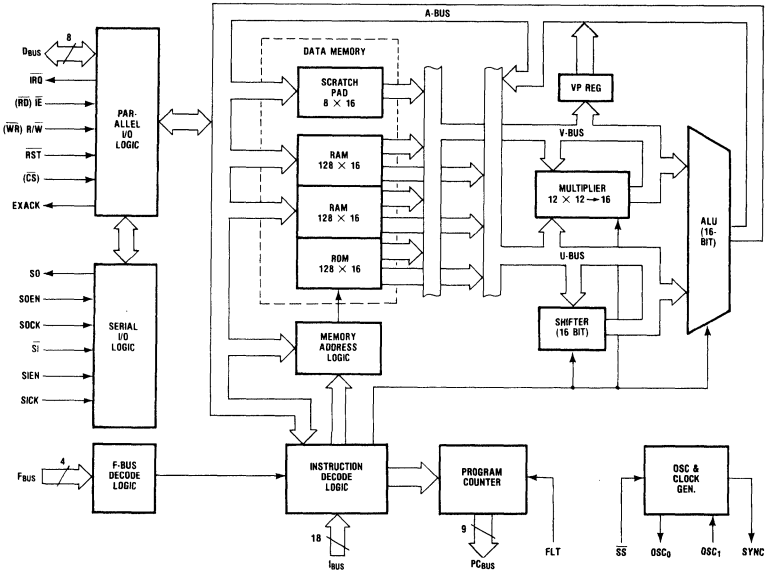
Features

- ☐ Single-Chip Programmable Digital Signal Processor
- ☐ May Be Customized (ROM Programmed) With Customer Generated Routines
- ☐ Self-Emulation Capability
- ☐ Standard Preprogrammed Processors Available
- ☐ Fetch/Multiply/Add/Store Cycle
- ☐ 512 Word × 18 Bit Instruction Memory
- ☐ Unique Three Port Data Memory
  256 × 16 RAM/128 × 16 ROM
- ☐ 12 × 12 Pipelined Multiplier With 16 Bit Product
- ☐ 16 Bit Accumulator With Overflow Detect/Protect
- ☐ Double Buffered Asynchronous Serial I/O Port
- ☐ μP-Compatible I/O Port i.e. 6800 (A Version), 8080 (B Version), etc.

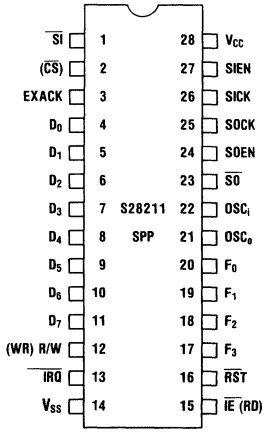
General Description

The S28211 is a single-chip microcomputer which has been optimized to execute digital signal processing algorithms commonly used in applications such as telecommunications speech processing, industrial process control instrumentation, etc. It may be used as a stand alone unit, or may be operated as a peripheral in a microprocessor based system. The latter configuration allows arrays of S28211s to be used together for increased processing throughput. The S28211's multibus, pipelined architecture and powerful multi-operation instructions make it possible to write very compact algorithms. This allows the available memory to be used efficiently and increases the execution speed of a given algorithm. The S28211 may be

Simplified Block Diagram



Pin Configuration



NOTE:
PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION

customized with user generated algorithms (Factory ROM Programmed). A selection of support tools (Assembler, Simulator, Real-time Emulator) are available for this task. In addition, a family of pre-programmed S28211s are available for standard applications.

Functional Description

The main functional elements of the S28211 (see Block Diagram) are:

1. a 512 × 18 ROM which contains the user program.
2. a 3-port 384 × 16 data memory (one input and two output ports) which allows simultaneous readout of two words.
3. a 12-bit × 12-bit high-speed parallel multiplier with 16-bit rounded product.
4. an Arithmetic/Logic Unit (ALU).
5. I/O and control circuits.

The S28211 is implemented in a combination of clocked and static logic which allows complete overlap of the multiply operation with the read, accumulate, and write operations. The basic instruction cycle is Read, Modify, Write, where the "Read" brings the operands from the data memory to the multiplier and/or the ALU, the "modify" operates on those operands and/or the product of the previous operands, and the "Write" stores the result of the "Modify." The cycle time for the instruction is 300 nanoseconds. This results in an arithmetic throughput of about 3.3 multiply and accumulate operations per microsecond.

The S28211 is intended to be used as a microprocessor peripheral. The S28211 control interface is directly compatible with the 6800 microprocessor bus (A version) or 8080/8085/Z80 microprocessor bus (B version), but can be adapted to other 8-bit microprocessors with the addition of a few MSI packages.

Operating in a microprocessor system, the S28211 can be viewed as a "hardware subroutine" module. The microprocessor can call up a "subroutine" by giving a command to the S28211. A powerful instruction set (including conditional branching and one level of subroutine) permits the S28211 to function independently of the microprocessor once the initial command is given. The S28211 will interrupt the microprocessor upon completion of its task. The microprocessor is free to perform other operations in the interim.

The S28211 contains a high-speed serial port for direct interface to an analog-to-digital (A/D) converter. In many applications, real-time processing of sampled analog data can be performed within the S28211 without tying up the main microprocessor. Data transfer to the microprocessor occurs upon completion of the S28211 processing.

Separate input and output registers exchange data with the S28211 data ports. Serial interface logic optionally converts the parallel 2's complement data to serial 2's complement or sign + magnitude format. Data format and source (serial or parallel port) is software selectable.

The S28211 is a memory-mapped peripheral, occupying 16 locations of the microprocessor memory space. Selecting the correct S28211 address will activate the corresponding control mode.

The control modes and the LIBL instruction enable real-time modification of the S28211 programs. This permits a single S28211 program to be used in several different applications. For example, an S28211 might be programmed as a "universal" digital filter, with cutoff frequency, filter order, and data source (serial or parallel port) selected at execution time by the control microprocessor.

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Advanced Product Description **S28212**

SIGNAL PROCESSING PERIPHERAL

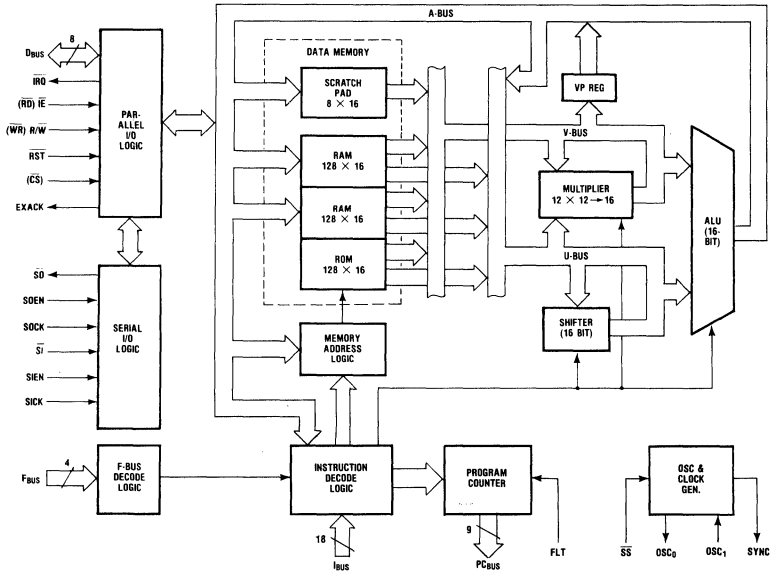
Features

- ☐ Programmable Digital Signal Processor
- ☐ Executes S28211 Functions From External Memory At Full Speed
- ☐ Fetch/Multiply/Add/Store In Single 300 nanosec. Cycle
- ☐ Addressing Capability Of 512 Instructions
- ☐ Unique Three Port Data Memory With 256 Words Of RAM And 128 Words Of ROM
- ☐ 12x12 Multiplier With 16 Bit Product
- ☐ 16 Bit Accumulator With Overflow Detect/Protect
- ☐ Double Buffered Asynchronous Serial I/O Port
- ☐ Microprocessor Compatible I/O Port For 6800 Family (A Version) or 8080/85/Z80 etc. (B Version)

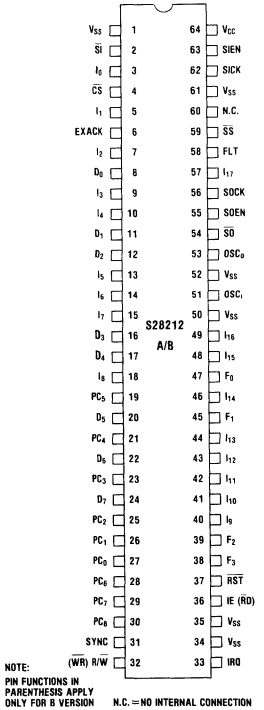
General Description

The S28212 is an external instruction memory version of the S28211 Signal Processing Peripheral. The internal program counter and instruction bus are made accessible via dedicated pins on the 64-pin package to allow the device to operate from an external instruction memory at full speed. This device may be used in place of the mask-programmed S28211 in development or small medium production run applications. In addition to the externally accessible program counter and instruction bus, the device also features a sync output to synchronize the external circuitry to the internal

Simplified Block Diagram



Pin Configuration



NOTE: PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION

N.C. = NO INTERNAL CONNECTION

General Description (continued)

instruction cycle, and a single-step capability. This allows the device to execute programs one step at a time, to simplify the debugging process. To aid the designer in writing software for this device a mnemonic assembler and simulation program (SSPP28211) is available. For information regarding the main architecture and programming of the device, please refer to the S28211 Advanced Product Description.

Functional Description

The main functional elements of the S28212 (see Block Diagram) are:

1. A dedicated interface to an external program memory with a 9 bit address drive capability.
2. A 3-port 384x16 data memory (one input and two output ports) which allows simultaneous readout of two words.
3. A 12 bit x 12 bit high-speed parallel multiplier with 16-bit rounded product.
4. An Arithmetic/Logic Unit (ALU).
5. I/O and control circuits.

The S28212 is implemented in a combination of clocked and static logic which allows complete overlap of the multiply operation with the read, accumulate, and write operations. The basic instruction cycle is Read, Modify, Write, where the "Read" brings the operands from the data memory to the multiplier and/or the ALU, the "Modify" operations on those operands and/or the product of the previous operands, and the "Write" stores the result of the "Modify". The cycle time for the instruction is 300 nanoseconds. This results in an arithmetic throughput of about 3.3 multiply and accumulate operations per microsecond.

The S28212 is intended to be used as a microprocessor peripheral. The S28212 control interface is directly compatible with the 6800 microprocessor bus (A Version) or 8080/8085/Z80 microprocessor bus (B Version) but can be adapted to other microprocessors with the addition of a few SSI packages.

Operating in a microprocessor system, the S28212 can be viewed as a "hardware subroutine" module. The microprocessor can call up a "subroutine" by giving a command to the S28212. A powerful instruction set (including conditional branching and one level of subroutine) permits the S28212 to function independently of the microprocessor once the initial command is given. The S28212 will interrupt the microprocessor upon completion of its task. The microprocessor is free to perform other operations in the interim.

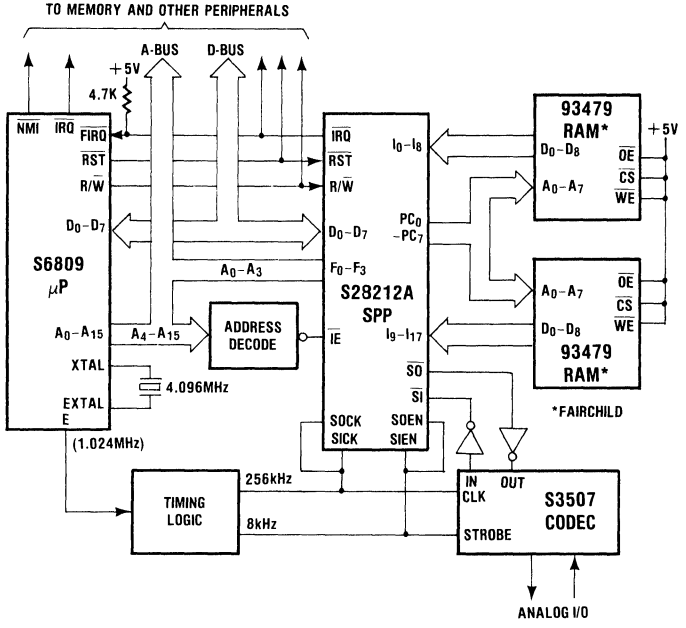
The S28212 contains a high speed serial port for direct interface to an analog-to-digital (A/D) converter or Codec. In many applications real time processing of sampled analog data can be performed with the S28212 without tying up the main microprocessor. Data transfer to the microprocessor occurs upon completion of the S28212 processing.

Separate input and output registers exchange data with the S28212 data ports. The serial interface logic optionally converts the parallel 2's complement data to serial 2's complement or sign + magnitude format. Data format and source (serial or parallel port) is software selectable.

The S28212 is a memory mapped peripheral, occupying 16 locations of the microprocessor memory space. Selecting the correct S28212 address will activate the corresponding control mode. The control modes and the LIBL instruction enable real-time modification of the S28212 programs. This permits a single S28212 program to be used in several different applications. For example, an S28212 might be programmed as a "universal" digital filter, with cut-off frequency, filter order, and data source (serial or parallel port) selected at execution time by the control microprocessor.

A typical application circuit is shown in Figure 1. The S28212 is here being controlled by the S6809 microprocessor and executes programs stored in the RAMs. The circuitry required to load the program into the RAMs is not shown here. The microprocessor memory and other peripherals are also omitted for simplicity. The Codec is integrated with anti-aliasing and smoothing filters, so that no other filtering of the analog signals will usually be necessary.

Figure 1. Typical Application



Data ROM Contents

The 128 word data ROM built into the S28212 contains a number of useful tables and constants. The ROM contents are listed in Table 1 below.

Table 1. Data ROM Contents.

BASE (B) →	DISPLACEMENT (D)			
↓	4	5	6	7
0	$0084	$0001	$FF00	$0000
1	$0000	$1001	$FE00	$0605
2	$0800	$2001	$FC00	$0C0A
3	$2000	$3001	$F800	$1210
4	$4000	$4001	$F000	$1815
5	$1000	$5001	$E000	$1E1A
6	$7FFF	$6001	$C000	$241F
7	$3000	$7001	$8000	$2A25
8	$00F0	$0000	$4200	$302A
9	$0070	$0000	$FF7C	$362F
10	$0030	$0000	$7F00	$3C34
11	$0010	$0000	$0100	$423A
12	$8070	$0000	$8284	$483F
13	$F830	$0000	$5A82	$4E44
14	$0000	$0000	$6EDA	$544A
15	$0000	$0000	$6487	$5A4F
16	$0000	$0000	$7FFF	$8000
17	$0000	$0C8C	$7F62	$4000
18	$0000	$18F9	$7D8A	$2AAA
19	$0000	$2528	$7A7D	$2000
20	$0000	$30FC	$7642	$1999
21	$0000	$3C57	$70E3	$1555
22	$0000	$471D	$6A6E	$1249
23	$0000	$5134	$62F2	$1000
24	$0000	$5A82	$5A80	$0E38
25	$0000	$62F2	$5134	$0CCC
26	$0000	$6A6E	$4717	$06A2
27	$0000	$70E3	$3C57	$0000
28	$0000	$7642	$30FC	$4580
29	$E800	$7A7D	$2528	$0000
30	$4000	$7D8A	$18F9	$0000
31	$6487	$7F62	$0C8C	$0000

Marked Blocks.

Block marked in area (B 0, D 4-6) to (B 6, D 4), (B 7, D 5), and (B 12, D 6): This is a lookup table used in PCM μ-law to linear and linear to μ-law conversions. Block marked in area (B 0, D 7) to (B 26, D 7): This is a lookup table used in linear to decibel conversion. Block marked in area (B 16, D 5-6) to (B 31, D 5-6): This is a sine/cosine lookup table. Hex 6487 = PI/4. (Note: The S28212 data ROM is the same as that used in the S28215 Digital Filter/ Utility Peripheral.)

AMI

A Subsidiary of Gould Inc.

Advanced Product Description **S28214**

FAST FOURIER TRANSFORMER

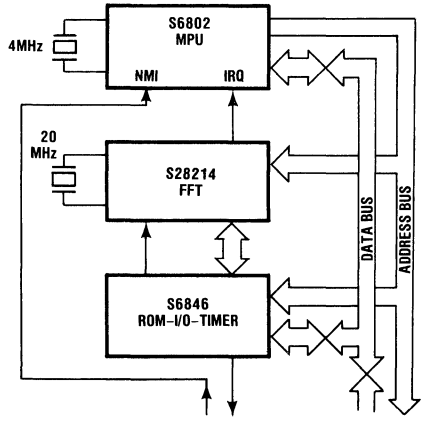
Features

- ☐ Performs 32 Complex Point Forward or Inverse FFT in 1.3msec, Using Decimation in Frequency (DIF)
- ☐ Transform Expandable either by Using Multiple S28214s (for Minimum Processing Time) or by a Single S28214 (for Minimum Hardware)
- ☐ Operates with any 8- or 16-Bit Microprocessor
- ☐ μP-Compatible I/O Port i.e., 6800 (A version), 8080 (B version)
- ☐ Basic Resolution of 57dB. Optional Conditional Array Scaling (CAS) Routine Increases Dynamic Range to 70dB
- ☐ Optional Windowing Routine Incorporated to Permit Use of Arbitrary Weighting Function
- ☐ Coefficient Generation On Chip, with Rotation Algorithm for Transform Expansion up to 512 Points
- ☐ Optional Power Spectrum Computation

General Description

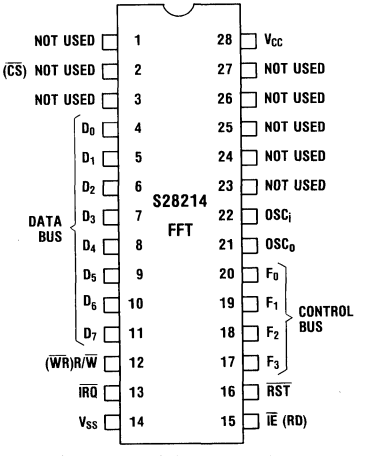
The AMI S28214 Fast Fourier Transformer is a preprogrammed version of the S28211 Signal Processing Peripheral. For further information on the internal operation of the S28211, please refer to the S28211 Advanced Product Description. It calculates FFTs and IFFTs using a decimation in frequency (DIF) technique for minimum distortion. The S28214 calculates a 32 complex point FFT using internally generated coefficients in a single pass. A coefficient rotation algorithm allows larger FFTs to be implemented (in blocks of 32 points). This implementation may be carried out by successive passes of the data through the two main routines in the S28214, allowing larger transforms to be carried out with a single S28214. Alternatively, an array of S28214s may be used to increase the transformation speed by parallel processing.

Block Diagram: Minimum System Configuration



TO I/O CIRCUITRY, e.g. ADC & DAC

Pin Configuration



NOTE: PIN FUNCTIONS IN PARENTHESIS APPLY ONLY TO B VERSION

The word length used in the S28214 gives the transformed data a resolution of up to 57dB, but the total dynamic range can be increased up to 70dB by using the Conditional Array Scaling (CAS) routine incorporated.

The S28214 is intended to be used in a microprocessor system (see Block Diagram), using an 8 or 16 bit microprocessor, ROM, RAM and an optional DMA Controller or Address Generator. The S28214 is used as a memory mapped peripheral, and should be assigned a block of 16 addresses. It is used as a "hardware subroutine" function. The microprocessor controls the flow of data, including I/O, and calls the routines in the S28214 to cause the FFT to be executed. The S28214 responds to the microprocessor with the $\overline{IRQ}$ line when the processing of each routine is completed. In the case of a 32 point transform this signifies the completion of the transform, and in larger transforms it signifies that the microprocessor should unload the output data, load the next input data and call the next routine to be executed. The data is stored externally in RAM. Input data to be transformed is loaded into displacements 0 and 1 of the S28214 data memory. At the end of the FFT routine output data overwrites the input data. If power spectrum flag (PSF) is set, the S28214 computes the sum of the squares of the real and imaginary components of the output data and places the result in displacement 3 of the data memory. Both complex FFT data and power spectrum data are thus available. Windowing weights may be loaded into the S28214 prior to processing if the windowing routine is to be used. A 6800 compatible source listing of a suitable control program is available to the S28214 user at no charge.

Absolute Maximum Ratings

Supply Voltage	7.0VDC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Voltage at any Pin	V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10sec.)	200°C

Electrical Specifications (V_{CC} = 5.0V ± 5%; V_{SS} = 0V, T_A = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.0		V_{CC} + 0.3	V	V_{CC} = 5.0V
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	V_{CC} = 5.0V
I_{IN}	Input Logic Leakage Current		1.0	2.5	μA	V_{IN} = 0V to 5.25V
C_I	Input Capacitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	I_{LOAD} = −100μA, V_{CC} = min, C_L = 30pF
V_{OL}	Output LOW Voltage			0.4	V	I_{LOAD} = 1.6mA, V_{CC} = min, C_L = 30pF
f_{CLK}	Maximum Clock Frequency		20.0		MHz	V_{CC} = 5.0V
P_D	Power Dissipation			700	mW	V_{CC} = 5.0V

S28214 Pin Functions/Descriptions

Pin	Number	Function
D_0-D_7	4-11	(Input/Output) Bi-directional 8-bit data bus. Data is Two's Complement coded.
F_0-F_3	20-17	(Input) Control Function bus. Four Microprocessor address lines (typically A_0-A_3) are used to control the S28214.
IE	15	(Input) Interface Enable. A low level on this line enables data transfer on the data bus and control functions on the F-bus. Usually generated by microprocessor address decode logic.
$\overline{(CS)}$		Chip Selection, B version only, LOW active.
R/$\overline{W}$ ($\overline{W/R}$)	12	(Input) Read/write select. When HIGH, output data from the S28214 may be read, and when LOW data may be written into the S28214. $\overline{WR}$ used on B version.
(RD)		Read Data, B version only, HIGH active.
$\overline{IRQ}$	13	(Output) Interrupt Request. This open drain output goes low when the S28214 has completed the execution of a routine and output data is available.
$\overline{RST}$	16	(Input) When LOW all registers and counters will be cleared, including the program counter, and all control functions cleared.
OSC_i, OSC_0	22, 21	Oscillator input and output. For normal operation a crystal is connected between these pins to generate the internal clock signals. Alternatively, an external square wave signal may be connected to OSC_i pin with OSC_0 pin left open.
V_{CC}	28	Positive power supply connection.
V_{SS}	14	Negative power supply connection. Normally connected to ground.

In addition to the above, pins 23-27 and 1 are connected internally. They should all be tied to V_{SS} during normal operation. Pin 2 is no connection on A version, but is used as Chip Select (CS) on B version. Pin 3 is no connection.

Functional Description

The S28214 is a pre-programmed version of AMI's S28211 Signal Processing Peripheral. This is a high speed microcomputer organized for efficient signal processing and contains a data memory, instruction memory, an arithmetic unit incorporating a 12-bit parallel multiplier, as well as control registers and counters.

For more detailed information about the chip, please refer to the S28211 Advanced Product Description.

The S28214 Instruction ROM contains the various routines together with their starting addresses in the Instruction ROM, are shown in Table 1A.

The Data ROM contains the coefficients required to execute the functions. 128 words of Data RAM are provided to hold the 32 point complex signal data during processing as well as the power spectrum of the output and various other parameters, including the total number of points in the desired transform. The memory is organized as a 32x4 matrix, with the data arranged in columns, as shown in Table 1B.

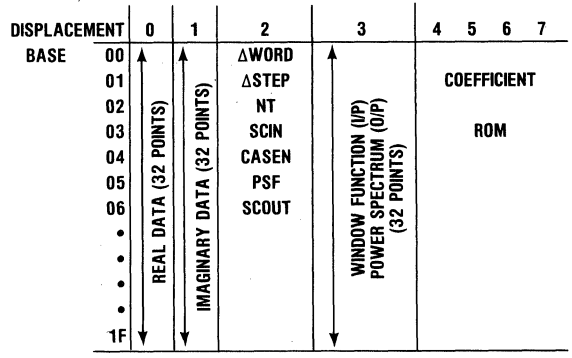
Table 1. Software Model of S28214

A. Routine Locations in Instruction Memory

LOC (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY PT. "INIT" ROUTINE
04	ENTRY PT. "FFT32" ROUTINE
D3	ENTRY PT. "COMPAS" ROUTINE
EA	ENTRY PT. "SCALE" ROUTINE
DC	ENTRY PT. "WINDOW" ROUTINE
E4	ENTRY PT. "CONJUG" ROUTINE

B. Data Memory Map

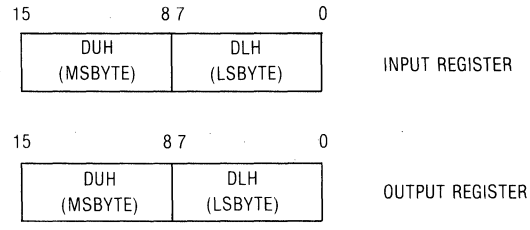
(Note: Address [Base AB, Displacement C] is written as AB·C)



C. Control Functions

F-BUS (HEX)	MNEMONIC	FUNCTION
1	RST	RESETS CHIP
2	DUH	SELECTS MSBYTE
3	DLH	SELECTS LSBYTE
4	XEQ	STARTS EXECUTION
9	BLK	SELECTS BLOCK MODE

D. Input and Output Registers



CODE IS TWO'S COMPLEMENT.

NOTE: A DUH BYTE MAY BE LOADED WITHOUT A DLH, BUT THE REVERSE CANNOT BE DONE.

Initial Set-Up Procedure

After power up, the RST line should be held low for a minimum of 300nsec. If this line is connected to the reset line of the microprocessor this condition will be met easily. This will clear the Base and Index Registers, which are used for memory addressing, the Loop Counter and the Program Counter. Address zero in the Instruction ROM contains a Jump to Zero instruction, and thus the S28214 will remain in an idle state after being reset. Every routine in the memory is also terminated with a Jump to Zero instruction, and thus the S28214 will also remain in this same idle state after the execution of each routine. The IRQ line will signal this condition each time (except after the initial reset).

The Control Functions

The S28214 is controlled by the host microprocessor by means of the F-bus, Interface Enable (IE) and the Read-Write (R/W) lines. It should be connected to the host processor as a memory mapped peripheral as shown in Figure 1.

The 12 most significant address lines decode a group of 16 addresses to activate the IE line each time an address in the group is called, and the S28214 is controlled by reading to or writing from those addresses. Only 5 of these addresses are used as described in Table 2. Throughout this Product Description these addresses will be referred to as NNNX (X = 0-F).

Figure 1. Connection of S28214 as a Mapped Peripheral (A Version)

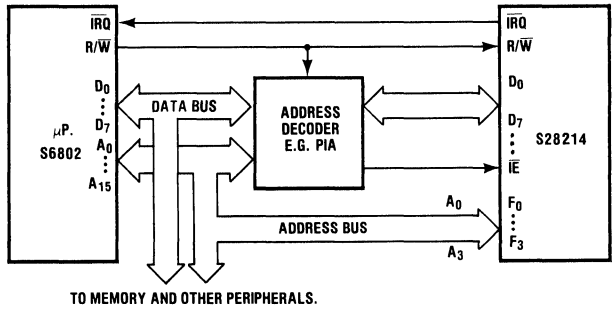


Table 2: S28214 Control Functions

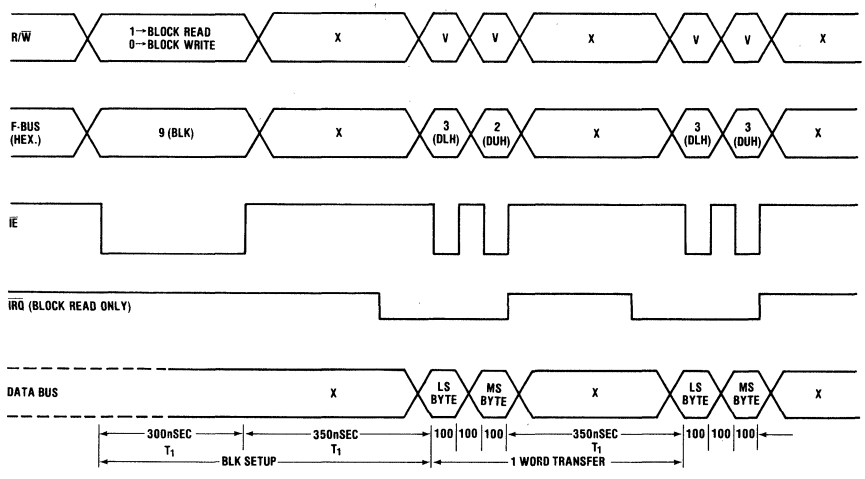
MNEMONIC	F-BUS HEX	DATA	TYPE OF OPERATION	FUNCTION
RST	1	XX	READ/WRITE	CLEARS ALL REGISTERS. STARTS PROGRAM EXECUTION AT LOCATION 00. THIS IS THE IDLE STATE. THIS INSTRUCTION SHOULD PRECEDE BLOCK READ, BLOCK WRITE AND EXECUTE COMMANDS.
DUH	2	HH	READ/WRITE	READS FROM OR WRITES INTO S28214 THE UPPER HALF OF THE DATA WORD. (SEE TABLE 1.D.)
DLH	3	HH	READ/WRITE	READS FROM OR WRITES INTO S28214 THE LOWER HALF OF THE DATA WORD. (SEE TABLE 1.D)
XEQ	4	HH	WRITE	STARTS EXECUTION AT LOCATION HH
BLK	9	XX	READ/WRITE	INITIATES A BLOCK READ OR BLOCK WRITE OPERATION. THE ENTIRE DATA RAM CAN BE ACCESSED SEQUENTIALLY BEGINNING WITH VALUES OF BASE AND DISPLACEMENT INITIALIZED USING "BLOCK TRANSFER SET UP" ROUTINE. IF A RESET OPERATION IS PERFORMED PRIOR TO BLOCK COMMAND THE DATA MEMORY ADDRESS IS INITIALIZED TO BASE 0, DISPLACEMENT 0. BLOCK READ OR WRITE OPERATION CAN BE TERMINATED ANY TIME BY PERFORMING A RESET OPERATION. THE INDEX REGISTER IS USED TO ADDRESS THE MEMORY DURING BLOCK TRANSFER AND INTERNAL ADDRESSING IS SEQUENCED AUTOMATICALLY.

NOTE: XX = Don't care
HH = 2 Hex characters (8-bit data)

The Block Transfer Operation

Block transfer is the mode used to load and unload the main data blocks into the S28214 at up to 4Mbytes/sec. In this mode the data memory is addressed by the Index Register, and after initialization the internal addressing is sequential and automatic. The sequence generated is that after each word transfer (16-bit words as 2 bytes, or 8-bit words as MSbyte (DUH) only) the base is incremented. After base 1F (31) has been reached, the base resets to 00 and the displacement increments. After base 1F displacement 3 has been reached (i.e., the highest address in the RAM, 1F.3), both base and displacement reset to zero. Note that when the BLK command is given the Read/Write line is latched internally, and remains latched until the RST command is given. The block transfer sequence and timing are shown in Figure 2.

Figure 2. Block Transfer Sequence and Timing



NOTE 1: DON'T CARE, OR NOT VALID.
NOTE 2: TIMES SHOWN ARE MINIMUM.
NOTE 3: THE R/W LINE MUST BE IN THE VALID STATE DURING ACTUAL READ OR WRITE PERIODS

In 6800 Assembly Language a Block Write would be executed with the following code:

```
LDX     OFFST   ;LOAD MEMORY START ADDRESS INTO INDEX REG.
STA   A BLK     ;WRITE DUMMY DATA TO ADDRESS $NNN9,BLOCK MODE.
LDA   A 0,X     ;READ FIRST BYTE FROM MEMORY.
STA   A DLH     ;WRITE INTO S28214 AS LSBYTE. ADDRESS $NNN3
LDA   A 1,X     ;READ SECOND BYTE FROM MEMORY.
STA   A DUH     ;WRITE INTO S28214 AS MSBYTE.ADDRESS $NNN2
LDA   A 2,X     ;SECOND WORD.
  .       .       .
  .       .       .
  .       .       .
LDA   A 62,X    ;32ND. WORD,LSBYTE.
STA   A DLH     ;
LDA   A 63,X    ;32ND. WORD,MSBYTE.
STA   A DUH     ;END OF TRANSFER.
STA   A RST     ;WRITE DUMMY DATA TO ADDRESS $NNN1.RESET.
```

Block Read would be executed by substituting LDA A for STA A, and vice versa.

where:

```
RST   EQU $NNN1
DLH   EQU $NNN3
DUH   EQU $NNN2
BLK   EQU $NNN9
```

The above code assumes that the block transfer is controlled by the host processor, not using DMA. Note that DLH must always precede DUH. 8-bit data may be transferred using DUH only, assuming that the significance of the data is correct.

The FFT Routines

Six individual routines are stored in the S28214 Instruction memory. Two or more of these are used in the computation of an FFT, depending on the transform size and the options selected. The starting addresses of the routines are shown in Table 3.

Table 3. FFT Routines and Their Starting Addresses

LOCATION (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY POINT FOR "INIT" ROUTINE
	(IR) = BASE, DISPLACEMENT
	$(BASE)_{4\text{-}0} \leftarrow (IR)_{15\text{-}11}, (DISP)_{1,0} \leftarrow (IR)_{9,8}$
	Returns to Idle state (IRQ not set after execution of INIT Routine) Exec. Time = 0.9μs
04	ENTRY POINT FOR "FFT32" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP2) = SCIN, CASEN, PSF
	Perform 32 point FFT. Sets IRQ, Returns to Idle state. Exec. Time = 1.2 ms to 1.8ms.
	(OR) = SCOUT (DISP0) = Transformed Data (Real), (DISP1) = Transformed Data (Imag.) (DISP2) = SCOUT, (DISP3) = Power Spectrum Data if PSF = 1
D3	ENTRY POINT FOR "COMPAS" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP2) = WORD, STEP, NT, SCIN, CASEN
	Perform COMPAS, Sets IRQ, Returns to Idle State Exec. Time = 233 to 374μsec.
	(DISP0) = Output Data (Real), (DISP1) = Output Data (Imag.) (DISP2) = SCOUT, (OR) = SCOUT
EA	ENTRY POINT FOR "SCALE" ROUTINE
	(IR) = SCIN, (DISP0) = Data (Real), (DISP1) = Data(Imag.)
	Performs scaling, Sets IRQ. Returns to Idle State Exec. Time = 51 to 250μsec.
	(DISP0) = Scaled Data (Real), (DISP1) = Scaled Data (Imag.)
DC	ENTRY POINT FOR "WINDOW" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP3) = Multiplying Factors
	Performs multiplication, Sets IRQ, Returns to Idle State Exec. Time = 49μsec.
	(DISP0) = Output Data (Real), (DISP1) = Output Data (Imag.)
E4	ENTRY POINT FOR "CONJUG" ROUTINE
	No set-up required. Conjugates input data (negates imaginary components). Sets IRQ. Returns to Idle State. Exec. time = 30μsec.

1. Block Transfer Set-Up (INIT). Entry Address 01.

This routine presets the Index Register to allow block transfer to commence at any location other than 00.0 in the S28214 data RAM. An eight-bit word is loaded into the upper half of the input register and the routine executed as shown:

```
DUH     EQU $HHH2
XEQ     EQU $HHH4
LDA     A #$XX
STA     A DUH
LDA     A #1
STA     A XEQ
```

where XX represents the start address for block transfer. The routine will be executed in 3 instruction cycles (0.9μsec.) and the S28214 will return to the idle state. Block transfer may then commence immediately.

Figure 3A. Flowchart for Subroutine FT32IN

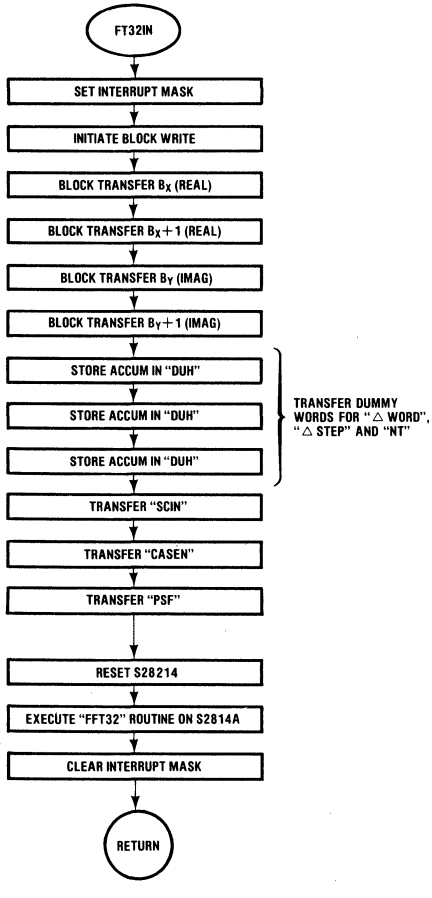
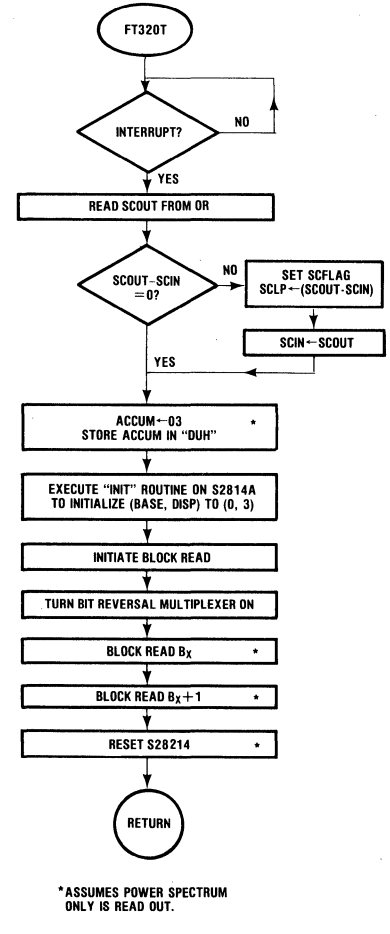


Figure 3B. Flowchart for Subroutine FT32OT



2. FFT32. Entry Address = 04.

This is the basic 32 complex point FFT routine. For a 32 point FFT this routine is called once only and the output of the routine is the FFT. Larger FFTs are computed by decimating them into 32 point arrays before final processing of these arrays using FFT32 to obtain the final outputs. The following data is loaded into the S28214, using block write starting at address 00.0, i.e., INIT is not used.

32 words of real input data (addresses 00.0-1F.0)
32 words of imaginary input data
(addresses 00.1-1F.1)
3 dummy words (to skip addresses)
(addresses 00.2-02.2)

2. FFT32. Entry Address = 04. (Continued)

SCIN (input scaling parameter) (address 03.2)
CASEN (CAS Enable) (address 04.2)
PSF (Power spectrum flag) (address 05.2)

Note that CASEN (Conditional array scaling enable) and PSF are not modified during processing, and need only be loaded once. CASEN should be positive to inhibit CAS (e.g. 0000) and negative to enable CAS (e.g. 8000). Note that SCIN is not needed if CAS is not enabled. PSF should be zero if the power spectrum output is not needed, any non-zero value (e.g. 0100) will cause the power spectrum to be computed. The block transfer should be terminated with the RST command, and the FFT32 routine called. Flow charts for loading and dumping the data are shown in Figure 3. The following sequence will cause the execution of the entire function:

```
CLR   B          ;CLEAR B ACC.
STA   A  RST     ;RESET S28214 REGISTERS.
SEI              ;SET INT. MASK.
STA   A  BLK     ;SET UP BLOCK WRITE.
JSR      BLKWT   ;WRITE 64 WORDS OF DATA.
STA   A  DUH     ;WRITE DUMMY DATA TO 00.0
STA   A  DUH     ;.....TO 00.1
STA   A  DUH     ;.....TO 00.2
LDA   A  SCIN    ;FETCH SCIN.
STA   A  DLH     ;WRITE TO ADDRESS 00.3
STA   B  DUH     ;COMPLETE WORD XFER.
LDA   A  CASEN   ;FETCH CAS ENABLE.
STA   A  DUH     ;WRITE TO ADDRESS 00.4
LDA   A  PSF     ;FETCH PS FLAG.
STA   A  DUH     ;WRITE TO ADDRESS 00.5
STA   A  RST     ;RESET S28214.
LDA   A  #4      ;FFT32 START ADDRESS.
STA   A  XEQ     ;START EXECUTING.
CLI              ;CLEAR INT. MASK.
WAI              ;WAIT FOR ROUTINE END.
LDA   A  DLH     ;START OF INT. ROUTINE.
LDA   B  DUH     ;(DUMMY).READ SCOUT.
LDA   B  SCIN    ;FETCH SCIN.
STA   A  SCIN    ;SCOUT→SCIN
SBA              ;COMP.SCOUT WITH SCIN.
BEQ      READ    ;JUMP IF NO CHANGE.
STA   A  SCLP    ;(SCOUT-SCIN) → SCLP
LDA   A  PASSN   ;FETCH PASS #
CMP   A  #1      ;IS THIS 1ST.PASS?
BEQ      READ    ;IF SO, JUMP
JSR      SKOUT   ;SCALE PREVIOUS ARRAYS
LDA   A  #3      ;(ASSUME PSF SET.)
STA   A  DUH     ;PRESET TO ADDRESS 00.3
LDA   A  #1      ;
STA   A  XEQ     ;EXECUTE INIT.
STA   A  BRV     ;TURN ON BIT REV.MUX.
LDA   A  BLK     ;SET UP BLOCK READ.
JSR      BLKRD   ;READ DATA.
STA   A  RST     ;END
```

The routine execution time is variable, depending on whether CASEN and PSF are set. The times are:

1. CAS-OFF. PSF-OFF 3730 instruction cycles (1.119msec.)
2. CAS-OFF. PSF-ON 3862 instruction cycles (1.159msec.)
3. CAS-ON . PSF-OFF 5867max. instruction cycles (1.760msec.)
4. CAS-ON . PSF-ON 5999max. instruction cycles

When CAS is enabled, the time depends on the number of times overflow is corrected. At the end of the routine the complex output data will have overwritten the input data in the memory (addresses 00.0 to 1F.1) and the power spectrum data will be in displacement 3 (addresses 00.3 - 1F.3). The output scaling factor (SCOUT) will be loaded in the output register, generating the $\overline{IRQ}$ to signify to the host processor that the routine has completed processing.

3. Combination Pass Routine, COMPAS. Entry Address = D3.

This is the decomposition routine that breaks up larger transforms into a number of 32 point transforms to be executed by FFT32. The N data points are split into N/16 blocks of 16 points, and pairs of blocks are passed through COMPAS. The procedure is repeated one or more times if N is greater than 64, but for a 64 point FFT the resulting data is ready for processing using FFT32. The procedure is explained in greater detail in the section "Executing Larger Transforms". The following data is loaded into the S28214 before execution:

32 words of real input data (addresses 00.0 - 1F.0)
32 words of imaginary input data (addresses 00.1-1F.1)
Δ WORD (address 00.2)
Δ STEP Set up parameters (address 01.2)
NT (address 02.2)
SCIN (address 03.2)
CASEN (address 04.2)
PSF (address 05.2)

The new parameters required, Δ WORD, Δ STEP and NT are dependent on the size of the transform and Δ WORD changes with each pass through the COMPAS routine. The values required are shown in the tables in sections "Executing 64 Point Transforms" and "Executing Larger Transforms". Flow charts for loading and dumping the data are shown in Figure 4. The routine execution time varies with transform size and depends on whether CAS is enabled or not, as shown:

TRANSFORM SIZE	64 POINT	128 POINT	256 POINT	512 POINT
Without CAS, Inst. cycles, (μsec.)	776 (233)	828 (248)	842 (253)	949 (255)
With CAS. (Max.) Inst. cycles (μsec.)	1172(352)	1224(367)	1238(371)	1245(374)

Figure 4A. Flowchart for Subroutine CSIN

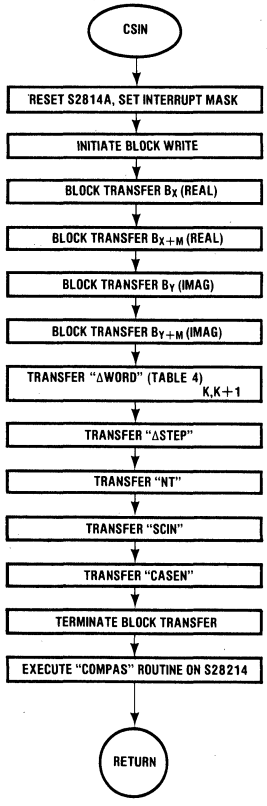
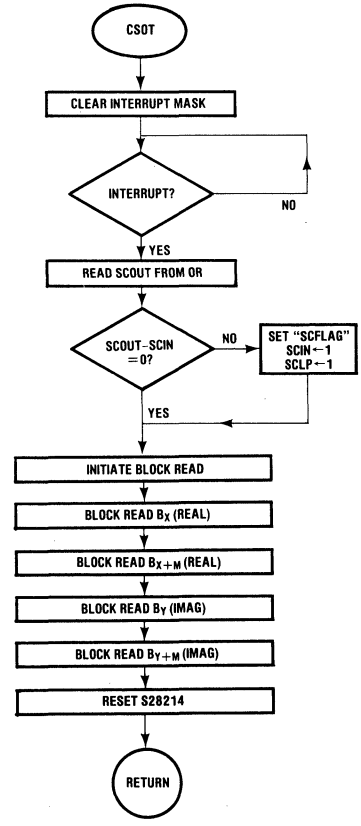


Figure 4B. Flowchart for Subroutine CSOT



4. Data Point Scaling Routine, SCALE. Entry location = EA.

If CAS is enabled, then routines COMPAS, and FFT32 will scale all 32 data points being processed if an overflow occurs during that pass. The value of SCOUT allows the data during subsequent passes to be scaled automatically during the pass. However, data points which have already been processed must also be scaled, so that all the data is scaled by the same factor during each processing step. SCALE is a routine that allows this to be done at high speed. Each block to be scaled is block loaded into the S2814A, the routine SCALE executed, and the block dumped back into the original locations in memory.

Care must be taken to keep track of which blocks have already been processed during each step, so that blocks

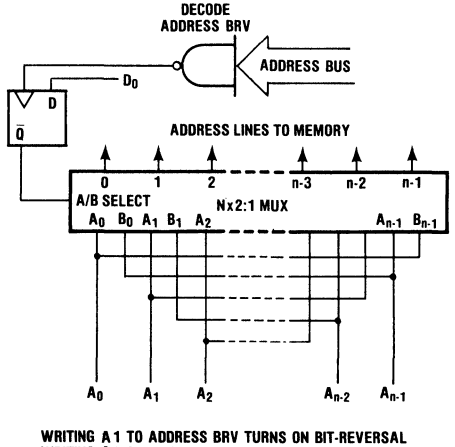
do not get missed or scaled twice. The execution time depends on the scaling factor (SCOUT), as shown below:

Scaling Factor (SCOUT)	1	2	3	4	5
Execution time. Inst. Cycles, (μsec.)	170(51)	336(101)	502(151)	668(200)	834(250)

5. Windowing Routine, WINDOW. Entry Address = DC

In order to allow the input data points to be windowed, a routine is provided to multiply the 32 real or complex points loaded in the S28214 by 32 window points. This is done on each block of 32 points prior to commencing the actual FFT processing. The input data required, in addition to the normal input data, are the 32 points of the window. They should be loaded into displacement 3 of the S28214 RAM and the routine WINDOW executed. The windowed data points will be returned to their original positions in the memory, so that COMPAS or FFT32 may then be executed immediately without further processing. The entire data can be loaded in a single block transfer operation by using INIT to preset the start address to 00.3. The 32 point window data is then loaded, followed by the signal data. This is possible because after loading the window the memory address will automatically reset to 00.0, the start address for the real data. The parameters are then loaded into displacement 2 addresses in the usual way. They will not be affected by the windowing operation. The total execution time is 163 instruction cycles, 49μsec.

Figure 5. Bit Reversal Hardware



WRITING A1 TO ADDRESS BRV TURNS ON BIT-REVERSAL
WRITING A0 CLEARS BIT REVERSAL

Executing FFTs

Executing the FFTs consists of loading data blocks, executing routines in the S28214 and dumping the data. However, the sequence of the FFT output data is scrambled, and in order to use the results meaningfully, it must be unscrambled. This is done by reversing the order of the bits of the address lines for the final output data. Thus, for a 2^N point FFT the N address lines A_0, A_1, A_2 ..... A_{N-1} must be reversed to the sequence A_{N-1}, A_{N-2} ..... A_1, A_0 to address the output buffer memory. This is most conveniently done as the data points are being dumped out of the S28214 after the processing of the FFT32 routine(s). The bit reversal can be done either by software or hardware. The hardware realization is shown in Figure 5, and an example of software bit reversal is given in the section "Executing 32 Point FFTs."

Executing 32 Point Transforms

The basic 32 point transform is easily implemented with the S28214 since it simply requires the loading of the 32 real or complex data points and the 3 parameters SCIN, CASEN and PSF, executing FFT32 once only and dumping the data using bit reversal. The flowchart for this sequence is shown in Figure 6. It is assumed that the loading of data from the source into the input buffer and dumping of data from the output buffer to destination is carried out by the NMI (non-maskable interrupt) routine. The parameter SCIN should be set to zero, and the output data should be scaled (multiplied) by $2^{(SCOUT)}$ if absolute levels are wanted.

Executing 64 Point Transforms

This is the simplest expansion of the FFT. The first step is to use COMPAS (twice) to decimate the data into two 32 point transforms, and then use FFT32 (twice) to produce the transforms. This is shown in the signal flow graph in Figure 7. The flow graph is independent of whether one or two S28214s are used, since the two passes through each of the 2 routines (COMPAS and FFT32) can be carried out sequentially or in parallel. The set up parameters for the 64 point FFT are:

For COMPAS 0: ΔWORD = 8070
ΔSTEP = 4000 NT = 0001

For COMPAS 1: ΔWORD = C070

The treatment of SCIN and SCOUT is dealt with in the next section.

Note: All values in Hex.

Figure 6. Flowchart for 32 Point FFT

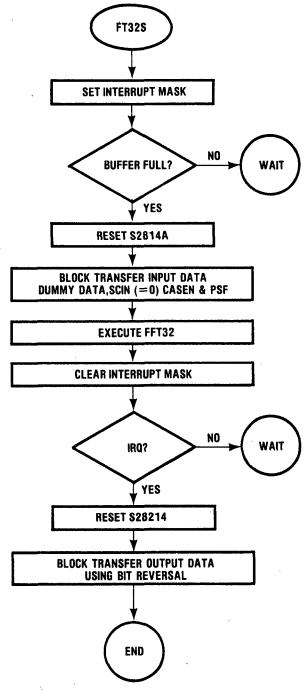


Figure 7. 64 Point FFT Flowgraph

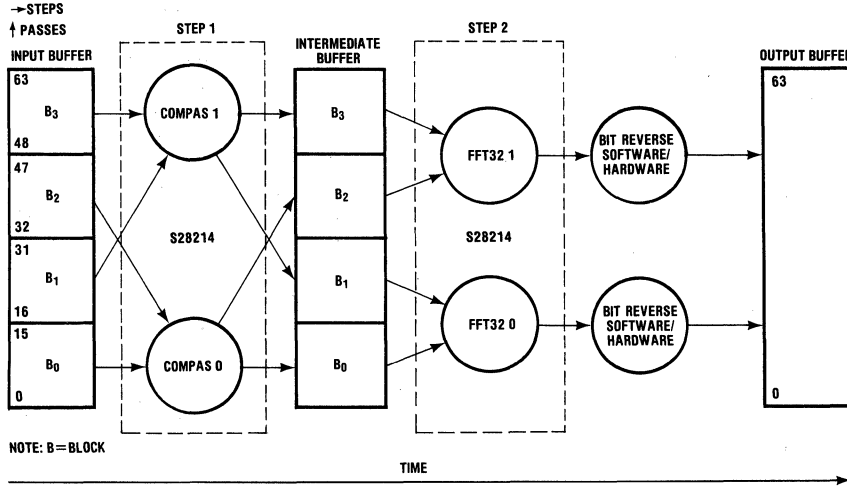
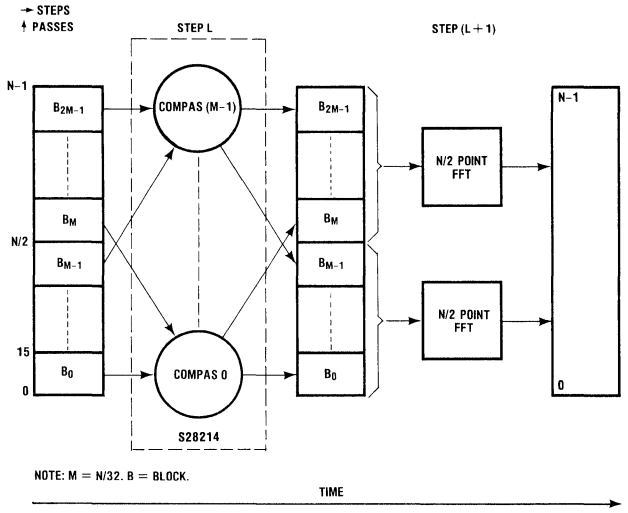


Figure 8. N Point FFT Flowgraph



Executing Larger Transforms

The execution of larger transforms follows the same sequence as the 64 point transforms: namely the decimation of the data into a series of 32 point blocks that can be processed using FFT32. For a 2^N point FFT this involves N-5 steps of processing using COMPAS, and each step requires $2^{(N-5)}$ passes through the COMPAS routine. This is followed by $2^{(N-5)}$ passes through the FFT32 routine. Within each step, each pass may be carried out sequentially using a single S28214, or in parallel using $2^{(N-5)}$ chips. There are also intermediate sequential + parallel combinations possible, of course, using fewer chips. A signal flow graph for 1 step is shown in Figure 8.

At the start of each step, SCIN should be set to zero. For the remaining passes in that step the value of SCOUT for the current pass should be used for SCIN for the next pass. The outputs of previously computed passes must be scaled using routine SCALE each time SCOUT increases during a pass. The maximum value of SCOUT after executing COMPAS is 1, and after executing FFT32 it is 5.

A flow chart for an N point transform control program is shown in Figure 9. The routine is called NFFT and uses the following subroutines:

- CSIN — procedure for loading S28214 with COMPAS input data (Figure 4A)
- CSOT — procedure for dumping COMPAS output data (Figure 4B)
- SCLPRV — procedure for scaling previously computed blocks of data in each step. See Figure 10.
- FT32IN — procedure for loading S28214 with FFT32 input data (Figure 3A)
- FT32OT — procedure for dumping FFT32 output data (Figure 3B)

The values of ΔWORD, ΔSTEP and NT are shown in Tables 4 and 5.

Figure 9. Flow Chart for N Point FFT, Routine "NFFT"

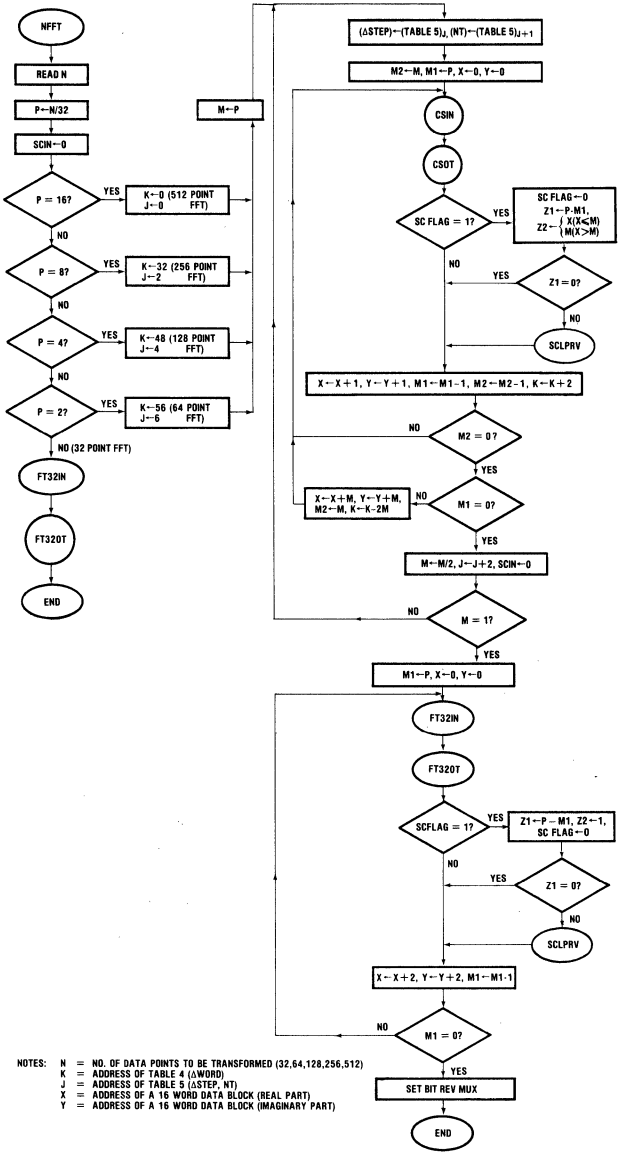


Figure 10. Flow Chart for Subroutine "SCLPRV"

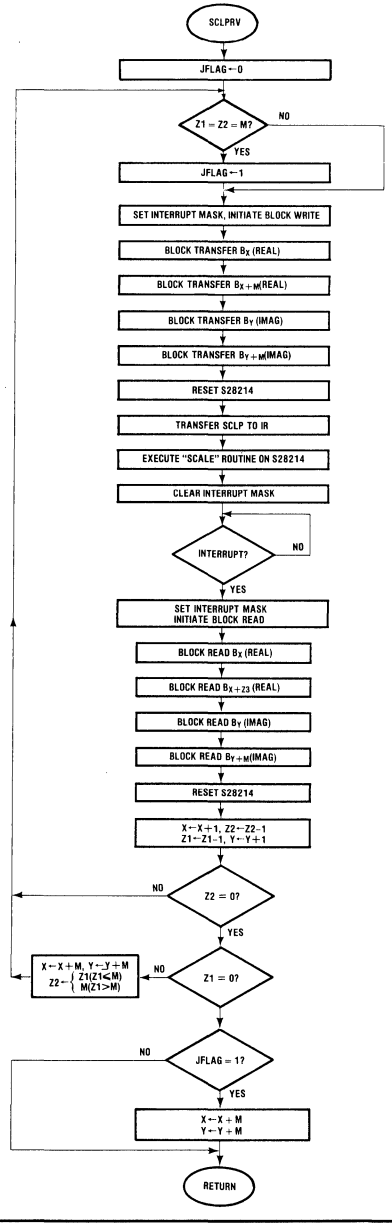


Table 4. (ΔWORD)

ENTRY PT for	K	VALUE	COMMENTS
512→	0	00	(ΔWORD L)
point	1	80	(ΔWORD H)
x'form	2	00	
	3	88	
	4	00	
	5	90	
	6	00	
	7	98	
	8	00	
	9	A0	
	10	00	
	11	A8	
	12	00	
	13	B0	
	14	00	
	15	B8	
	16	00	
	17	C0	
	18	00	
	19	C8	
	20	00	
	21	D0	
	22	00	
	23	D8	
	24	00	
	25	E0	
	26	00	
	27	E8	
	28	00	
	29	F0	
	30	00	
	31	F8	
256→	32	10	
point	33	80	
x'form	34	10	
	35	90	
	36	10	

Table 4. (Continued)

ENTRY PT for	K	VALUE
	37	A0
	38	10
	39	B0
	40	10
	41	C0
	42	10
	43	D0
	44	10
	45	E0
	46	10
	47	F0
128 →	48	30
point	49	80
x'form	50	30
	51	A0
	52	30
	53	C0
	54	30
	55	E0
64 →	56	70
point	57	80
x form	58	70
	59	C0

Table 5. (ΔSTEP, NT)

ENTRY PT for	J	VALUE	COMMENTS
512 point	0	08	ΔSTEP(DUH)
x'form	1	0F	NT(DLH)
256	2	10	''
	3	07	''
128	4	20	''
	5	03	''
64	6	40	''
	7	01	''

NOTE: FOLLOWING LOADING OF THE N.T. BYTE, A DUMMY DUH MUST BE LOADED TO COMPLETE WORD LOADING, OTHERWISE THE S28214 DOES NOT RECOGNIZE THE COMPLETION OF THE TRANFER.

Hardware

The minimum hardware for a 32 point FFT is shown in Figure 11. All data transfer and control is handled by the S6802. The availability of the next input sample is signalled with the NMI line. A suitable analog interface is shown in Figure 12. The sampling clock is derived from the microprocessor clock, and the NMI signal is generated by the EOC (end of conversion) output of the A/D converter. This system may be expanded simply by adding more memory. The memory requirements are shown in Table 6. A word may be up to 16 bits long. In order to speed up the complete procedure it is necessary to use DMA for block transfer of data. The S28214 will transfer data at up to 4Mbytes/sec. A suitable DMA Address Generator is the Advanced Micro Devices' AM2940, but a 68B44 will accomplish the function more conveniently at a slightly lower speed (1.5Mbyte/sec).

Data Bus Interface

Figure 13 shows how to interface the S28214 with a typical 6800 family microprocessor data bus. Note that the data bus must be isolated from the microprocessor system data bus by use of a PIA as in Figure 11 or a 74LS245 or 74LS645 type data transceiver as shown in Figure 13, since the S28214 drive capability is only one TTL load. The bus isolation may be omitted in some small systems.

Figure 11. 32/64 Joint FFT Hardware

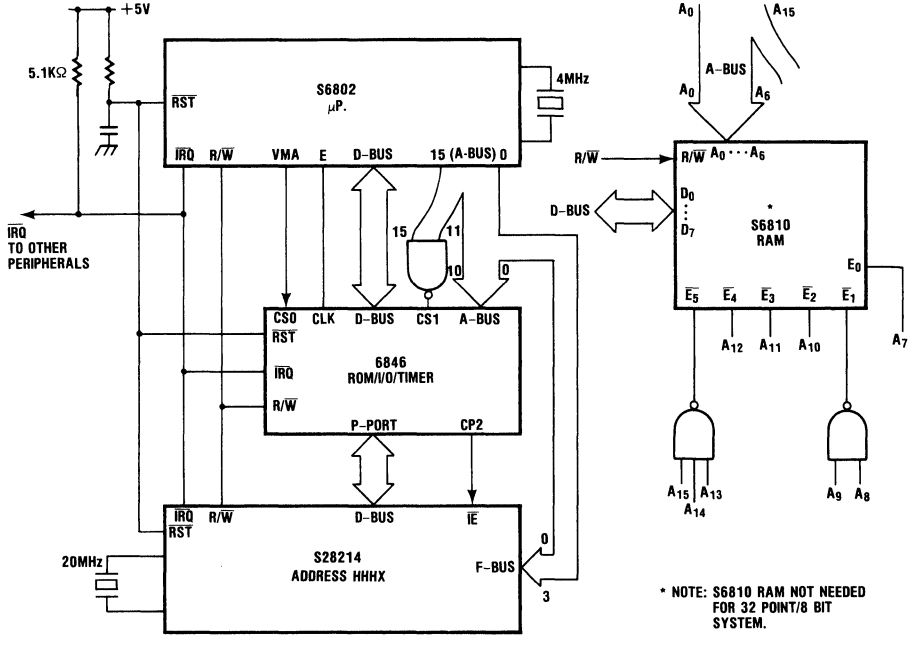


Figure 12. Analog Interface

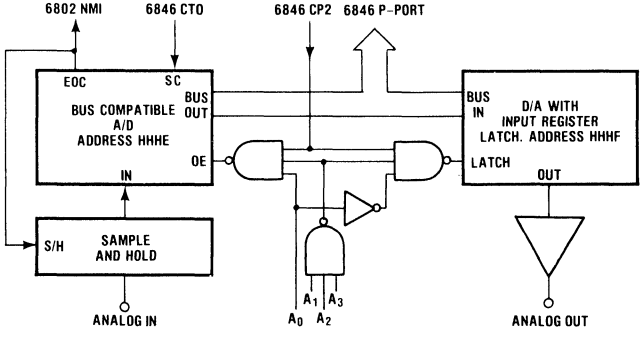


Figure 13. Interfacing the S28214 with a Microprocessor

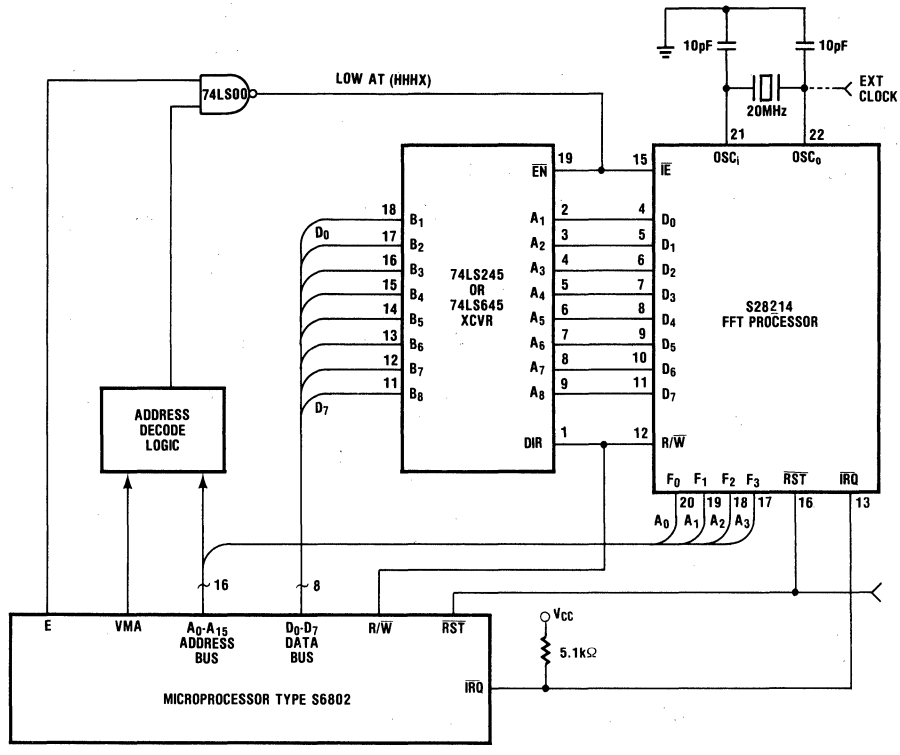


Table 6. Memory Requirements for Data Point Storage

TRANSFORM SIZE (POINTS)	WORD LENGTH (BITS)	MEMORY REQUIREMENTS
32	8	64 bytes
	10/12	See Note 1
	16	128 bytes
64	8	128 bytes
	10/12	See Note 1
	16	256 bytes
128	8	256 bytes
	10/12	768 nibbles
	16	1024 bytes
256	8	512 bytes
	10/12	1536 nibbles
	16	1024 bytes
512	8	1024 bytes
	10/12	3072 nibbles
	16	2048 bytes

Note 1: In practice the memory realization for these cases will be the **same as for 16-bit systems.**

FFT Resolution and Dynamic Range

The use of the Decimation in Frequency (DIF) algorithm in the S28214 ensures optimum signal to noise ratio, (SNR) for the architecture used. The use of the Conditional Array Scaling (CAS) gives a total dynamic range of approximately 70dB on all sizes of Transforms. The maximum resolution obtainable is approximately 57dB. CAS operates by detecting overflow in the butterfly computation routine. As soon as an overflow is detected the two points being combined in that butterfly are halved in magnitude (both the real and imaginary portions) and the butterfly recomputed. A flag is set, all previously computed butterfly outputs are then scaled, and all the inputs to subsequent butterflies are scaled before computation begins, so that at the end of the pass all points have been scaled equally. A scale factor is made available (SCOUT) so that the remaining data points in larger transforms, i.e., those other than the 32 in the S28214 when the overflow occurred, may also be scaled to keep them all in line. Thus, CAS operates as a discrete AGC, halving the signal levels each time an overflow is detected. By using SCOUT after executing the FFT the output may be expanded, so that the levels displayed in the spectrum will increase monotonically as the input increases.

Transform Execution Times.

The maximum execution times of transforms are shown in Table 7. The actual execution time when CAS is enabled will be between the times shown for CAS off and the maximum with CAS on. It will depend on the number of times that scaling has to be done.

Table 7. Total FFT Execution Times Including Block Transfers (msec.)

TRANSFORM SIZE (PT.)	USING SINGLE S28214 BLOCK TRANSFER USING: S6802 (22μsec/word)		USING SINGLE S28214 BLOCK TRANSFER USING: DMA 2MW/sec		USING MULTIPLE S28214 ARRAY # OF S28214As	USING MULTIPLE S28214 ARRAY (USING DMA AT 2MW/sec)	
	MIN	MAX	MIN	MAX		MIN	MAX
32	4.0	4.6	1.3	1.9	1	1.3	1.9
64	14.2	15.7	3.2	4.6	2	1.6	2.3
128	40.7	44.0	7.6	11.0	4	1.9	2.8
256	106	114	17.8	25.4	8	2.3	3.2
512	262	280	40.7	57.9	16	2.6	3.7

Note: Minimum times assume that CAS and PSF are off. Maximum times assume that CAS and PSF are on, and that maximum overflow occurs during 1st pass. All times assume 20MHz clock frequency and must be increased proportionally for lower clock frequencies (except Column A).

AMI®

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Advanced Product Description

S28215

DIGITAL FILTER/UTILITY PERIPHERAL

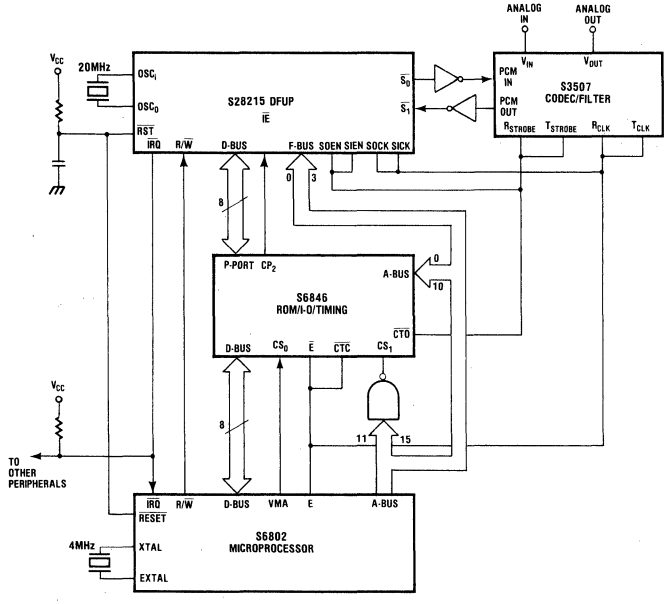
Features

- ☐ S28211 Signal Processing Peripheral Programmed With Filter and Utility Routines
- ☐ Microprocessor Compatible Interface Plus Asynchronous Serial Interface
- ☐ Two Independent 32 Tap Transversal Filter Routines, Cascadable into a Single 60 Tap Filter
- ☐ Two Recursive (biquadratic) Filters Providing a Total of 16 Filter Sections
- ☐ Computation Functions: Two Integrating, Two Rectifying, Squaring, and Block Multiply Routines
- ☐ Conversion Functions: μ255 Law-to-Linear, Linear-to-μ255 Law, and Linear-to-dB Transformations
- ☐ Generator Functions: Sine and Pseudo-Random Noise Patterns
- ☐ μP-Compatible I/O Port; i.e. 6800 (A Version), 8080 (B Version)

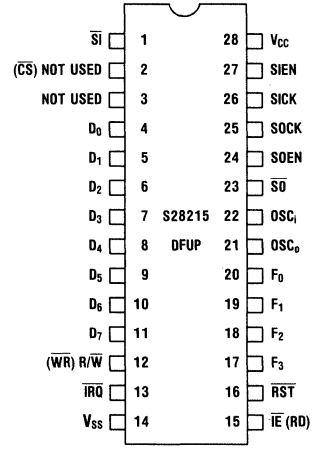
General Description

The AMI S28215 Digital Filter/Utility (DFUP) is a pre-programmed version of the S28211. Architectural and internal operating details of the S28211 may be found in the S28211 Advanced Product Description. The S28215 has been programmed with a collection of filter, computational, conversion, and generator routines which may be selected individually, or cascaded under control of

Block Diagram



Pin Configuration



NOTE: PIN FUNCTIONS IN PARENTHESIS APPLY ONLY TO B VERSION

General Description (Continued)

of the host processor. This arrangement allows a wide range of signal processing functions frequently required in application areas such as telecommunications, test and instrumentation, industrial automation, process control, etc., to be satisfied by a single S28215 DFUP.

The I/O structure of the S28215 provides flexibility and easy interfacing in microprocessor based systems. Input and output data transfers may be accomplished serially, as shown in the block diagram, using a μ255-law Codec such as the S3507, or using linear A/D and D/A converters. Data may also be transferred in parallel under control of a host processor, such as the S6802. Routines may be executed individually, completely under control of the host processor, or internal transfer addresses may be set up by the host, allowing routines to be cascaded internally. The ability to cascade routines allows complicated functions to be completed without intervention by the host processor.

Absolute Maximum Ratings

Supply Voltage	7.0VDC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Voltage at any Pin	V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C

Electrical Specifications: $V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_A = 0°C$ to $+70°C$, unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input HIGH Logic "1" Voltage	2.0		$V_{CC}+0.3$	V	$V_{CC} = 5.0V$
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	$V_{CC} = 5.0V$
I_{IN}	Input Logic Leakage Current		1.0	2.5	μAdc	$V_{IN} = 0V$ to 5.25V
C_I	Input Capacitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{LOAD} = -100\mu A$, $V_{CC} = \min$, $C_L = 30pF$
V_{OL}	Output LOW Voltage			0.4	V	$I_{LOAD} = 1.6mA$, $V_{CC} = \min$, $C_L = 30pF$
f_{CLK}	Clock Frequency	5.0	20		MHz	$V_{CC} = 5.0V$
P_D	Power Dissipation		700		mW	$V_{CC} = 5.0V$
$f_{CLK}(max)$	Maximum Clock Frequency		20.0		MHz	$V_{CC} = 5.0V$

S28215 Pin Functions/Descriptions

Microprocessor Interface (16 Pins)

D_0-D_7	(Input/Output) Bi-directional 8-bit data bus.
F_0-F_3	(Input) Control Mode/Operation Decode. Four Microprocessor address leads are used for this purpose. See "CONTROL MODES AND OPERATIONS." (Table 2)
$\overline{IE}$	(Input) Interface Enable. A low level on this pin enables the SPP microprocessor interface. Generated by microprocessor address decode logic.
(RD)	Read Data Pin. HIGH active. Used when interfacing to 8080/Z80μP.
R/$\overline{W}$ ($\overline{W/R}$)	(Input) Read/Write Select. When HIGH, output data from the SPP is available on the data bus. When LOW, data can be written into SPP. WR used when interfacing with 8080/Z80 μP.
$\overline{IRQ}$	(Output) Interrupt Request. This open drain output goes LOW when the SPP needs service from the microprocessor.
$\overline{RST}$	(Input) When LOW, clears all internal registers and counters, clears all modes and initiates program execution at location 00.
$\overline{CS}$	Chip Select pin. LOW active. Used when interfacing with a 8080/Z80 μP.

Serial Interface (6 pins)

SICK, SOCK	(Input) Serial Input/Output clocks. Used to shift data into/out of the serial port.
$\overline{SI}$	(Input) Serial Input. Serial data input port. Data is entered MSB first and is inverted.
SIEN	(Input) Serial Input Enable. A HIGH on this input enables the serial input port. The length of the serial input word (16 bits maximum) is determined by the width of this strobe.
$\overline{SO}$	(Output) Serial Output. Three-state serial output port. Data is output MSB first and is inverted.
SOEN	(Input) Serial Output Enable. A HIGH on this input enables the serial output port. The length of the serial output (16 bits maximum) is determined by the width of this strobe.

Miscellaneous

OSC_i, OSC_o	An external crystal with suitable capacitors to ground can be connected across these pins to form the time base for the SPP. An external clock can also be applied to OSC_i input if the crystal is not used.
V_{CC}, V_{SS}	Power supply pins $V_{CC} = +5V$, $V_{SS} = 0$ volt (Ground)

Functional Description

The S28215 is a pre-programmed version of AMI's Signal Processing Peripheral. This is a high speed microcomputer organized for efficient signal processing and contains a data memory, instruction memory, an arithmetic unit incorporating a 12-bit parallel multiplier, as well as control registers and counters. For more detailed information about the chip, please refer to the S28211 Advanced Product Description.

The S28215 Instruction ROM contains the various routines which make up the DFUP package. The routines together with their starting addresses in the Instruction ROM, are shown in Table 1A.

The Data ROM contains the parameters required to execute the functions. 128 words of Data RAM and an 8 word scratchpad are provided to hold the signal data and the jump addresses for cascading routines. The Data memory is arranged as a matrix of 32x8 words, as shown in Table 1B. The RAM utilization is routine dependent and is illustrated in the routine descriptions.

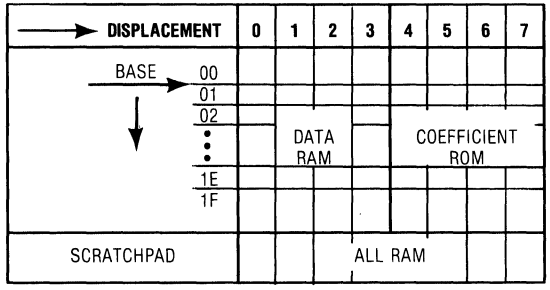
Table 1. Software Model of S28215

A. Routine Locations in Instruction Memory

(LOC (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY POINT "INIT" ROUTINE
04	ENTRY POINT "SETUP" ROUTINE
18 or 19*	ENTRY POINT "LINIP" ROUTINE
1B or 1C*	ENTRY POINT "MULIP" ROUTINE
34	ENTRY POINT "LIN01" ROUTINE
36	ENTRY POINT "LIN02" ROUTINE
38	ENTRY POINT "MULOP" ROUTINE
65	ENTRY POINT "DBOP" ROUTINE
80	ENTRY POINT "BMPY" ROUTINE
87	ENTRY POINT "IIR1" ROUTINE
96,97 or 98*	ENTRY POINT "IIR2" ROUTINE
A7	ENTRY POINT "FIR1" ROUTINE
AF, B0 or B1*	ENTRY POINT "FIR2" ROUTINE
BC	ENTRY POINT "RECT" ROUTINE
BF	ENTRY POINT "SQUAR" ROUTINE
C4	ENTRY POINT "FINT" ROUTINE
CA	ENTRY POINT "RINT" ROUTINE
CE	ENTRY POINT "SQUINT" ROUTINE
D6	ENTRY POINT "SINE" ROUTINE
E5	ENTRY POINT "NSET" ROUTINE
E9	ENTRY POINT "NOISE" ROUTINE

*See Routine descriptions for explanation of alternative entry points

B. Data Memory Map



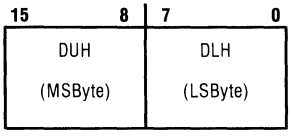
NOTE: Address [Base AB, Displacement C] is written as AB.C

C. Control Functions

F-Bus (HEX)	MNEMONIC
0	CLR
1	RST
2	DUH
3	DLH
4	XEQ
5	SRI
6	SRO
7	SMI
8	SMO
9	BLK
B	SOP
C	COP

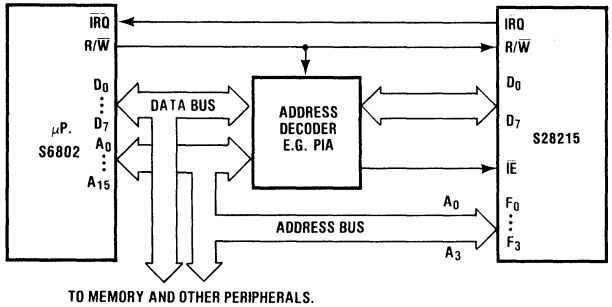
See Table 2 for descriptions

D. Input and Output Registers



Code is Two's Complement

Figure 1. Connection of S28215 as a Memory Mapped Peripheral



AMI®

A Subsidiary of Gould Inc.

S28216

ECHO CANCELLER PROCESSOR (ECP)

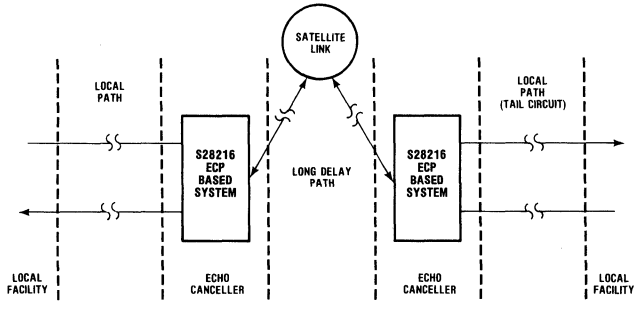
Features

- ☐ S28211 Based System With Echo Canceller Routines
- ☐ Especially Suited to Single-Hop or Double-Hop Satellite and Long Haul Terrestrial Circuits
- ☐ Eliminates Echo Without Signal Degradation
- ☐ Allows Full-Duplex Speech
- ☐ Accommodates Unlimited Long Haul Delays
- ☐ Expandable Delay Handling Capacity
- ☐ Cancel Echoes With up to 6mSec Dispersion
- ☐ Convergence Time < 250mSec

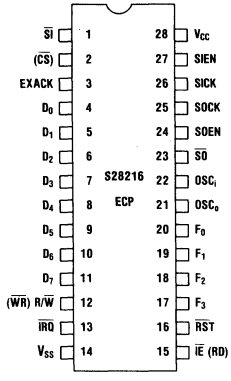
General Description

The AMI S28216 Echo Canceller Processor (ECP) is a pre-programmed version of the S28211 Signal Processing Peripheral. Architectural and internal operating details of the S28211 may be found in the S28211 Advanced Product Description. The S28216 is designed to provide the main echo canceller processing functions in a microprocessor based split-type echo canceller system. Programmed functions provided by the S28216 include μ255 law-to-linear and linear-to-μ255 law I/O conversion, local loop delay estimation, 48-tap auto-equalizing transversal filter, silence detection, and echo canceller performance estimation. This collection of routines allows the S28216 to dynamically eliminate echoes from long distance satellite undersea cable and terrestrial communication systems, employing either analog or digital links.

Typical System Application



Pin Configuration



NOTE:
PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION

Echo Canceller Routines

I/O Conversion

The input and output conversion routines are optional routines used when the echo canceller is placed in a PCM data stream, or when the echo canceller is placed in an analog data stream and a codec is used at the interface. The input conversion routine converts μ255 law PCM data to linear data. The output conversion routine converts linear data to μ255 law PCM data.

Local Loop Delay Estimator

The local loop delay estimator is used to determine the delay around the local loop. This information is supplied to the control processor which transfers the received data delayed by this estimate. The maximum local loop delay handling capability of the S28216 may be expanded by adding additional memory storage.

Auto-Equalizing Transversal Filter

The auto-equalizing transversal filter is used to model the echo so that it may be subtracted from the signal presented on the long haul side. A 48-tap filter is used to accomplish this task. Echoes with up to 6mSec dispersion may be eliminated by this arrangement.

Silence Detector

The silence detector is used to control the learning rate of the auto-equalizing transversal filter; the silence detector routine calculates the running power average and makes a decision whether the incoming signal is speech or noise. If there is no signal to learn on, or there is a high level interfering signal, learning is suspended.

Echo Canceller Performance Estimator

The Echo Canceller performance estimate, like the silence detector, is used to set the learning rate of the echo canceller. The learning rate of the canceller is set at a level which is proportional to the estimated performance. Performance is based on the ratio of the running averages of the signal before and after cancellation. This ratio is used to control the learning rate of the auto-equalizing transversal filter. Convergence time, for 18dB echo cancellation with a 6dB Echo Return Loss (ERL), is less than 500mSec plus the local loop delay time.

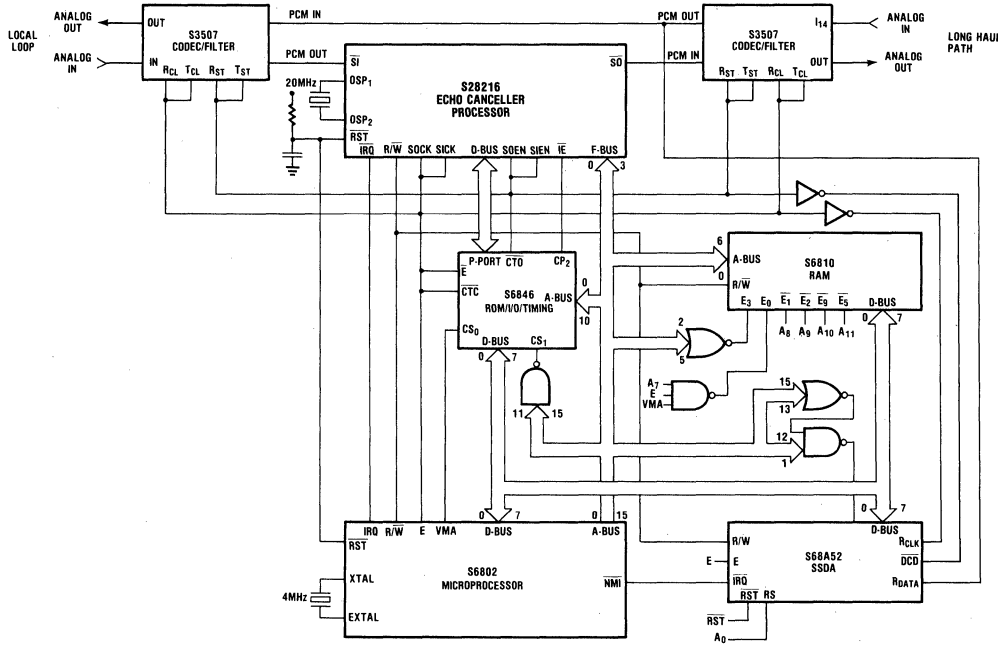
System Application

A proposed echo canceller system based on the S28216 is shown in Figure 2 together with the expected performance specifications. The S3507 codecs provide the required interfacing to the analog data stream. The S68A52 synchronous serial data adapter is used to convert the serial data stream into 8-bit words which can then be loaded into the S6810 RAM. The S6810 is used to store the receive data for a period of time equal to the local loop delay and then loaded into the S28216 for processing. The S6846 ROM-I/O-Timing is used to store the S6802 program, control the I/O between the S6802 and S28216, and provide timing signals required by the codecs. The S28216 performs the echo cancelling routines outlined above. Finally, the S6802 controls and monitors the entire operation.

Typical Echo System Specifications Using the S28216

Echo Return Loss (ERL)	>6dB
Residual Echo (Center Clipping Operating/Echo Suppression High S/N Ratios)	<-60dBmo
Convergence Time: ERL of 6dB and R_{in} of -10dBmo)	12dB < 250mSec 18dB < 500mSec
Maximum Tail Circuit Delay	25.6mSec (1200 mi. nom.)
Nominal Transmission Levels	+7dBm receive path -16dBm send path
Insertion Loss	0 ± 0.5dB, @1004Hz
Frequency Response	± 0.5dB, 300-3200Hz Ref. to 1kHz
Harmonic Distortion	<1% for 0dBmo test tone @1004Hz
Idle Noise	≤16dBrnco
Envelope Delay Distortion	≤100μSec, 500-3000Hz
Dynamic Range	+3.5 to -60dBmo

System Application



BELL 212A/CCITT V.22 COMPATIBLE MODEM FILTER WITH EQUALIZER

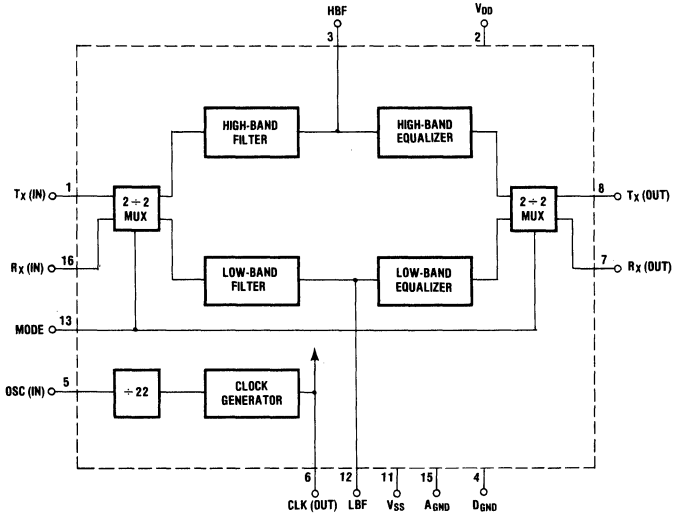
Features

- ☐ Bell 212A/V.22 Compatible
- ☐ Usable for Bell 103/113 Applications
- ☐ High and Low Band Filters with Compromise Group Delay Equalizers
- ☐ Originate/Answer Operating Modes
- ☐ Buffered Clock Output
- ☐ Excellent Rejection of CCITT Guard Tones
- ☐ Low Power CMOS 50mW Typ.
- ☐ ±5 Volt Operation
- ☐ Low Cost 16-Pin Package

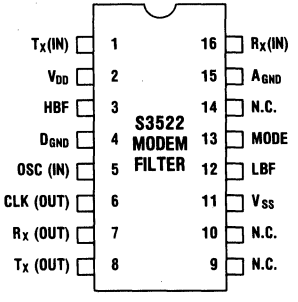
General Description

The AMI S3522 Modem Filter is a 16-pin monolithic CMOS integrated circuit designed to implement both the filtering and equalizing functions required in Bell 212A and CCITT V.22 Modems. The S3522 includes both the transmit signal shaping filter and the receive signal separation filter and features on-chip originate/answer mode selection logic. In addition, half-channel compromise amplitude and group delay equalization is included, giving full compromise equalization through the transmit and receive filter pair. The S3522 features excellent rejection of the CCITT Guard Tones at 550Hz: Low-Band (56dB), High-Band (61dB) and 1800Hz: Low-Band (48dB), High-Band (28dB).

Block Diagram



Pin Configuration



Functional Description

The S3522 is shown in simplified form in the block diagram. It consists of a low-band filter (800-1600Hz), a high-band filter (2000-2800Hz), and half-channel compromise group delay equalizers for both bands (see Figure 1). A changeover switch selects the routing of the input signals into the 2 filters, and another changeover switch routes the filter outputs to the appropriate output pins. The switches are controlled by the MODE selector, allowing the chip to be used in both the ORIGINATE and ANSWER modes without external switching. The outputs of both filters are brought out on separate pins, LBF and HBF. This allows the user to bypass the group delay equalizers if desired. Note that in this mode the filter outputs are not routed through the changeover switch, and external switching must be provided if mode changing is required. The filters are implemented using CMOS Switched Capacitor Filter technology, using a clocking frequency of 104.7kHz. The internal clocks are derived from the externally supplied 2.304MHz clock signal.

NOTE: External buffering is required for the LBF and HBF outputs.

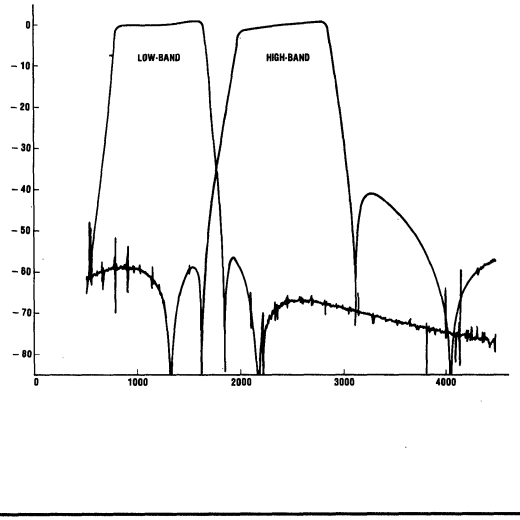
Low-Band Filter

The characteristics of the low-band filter are shown in Figure 2. The in-band response rises slightly near the top end of the pass-band, to compensate for typical line characteristics. The out-of-band attenuation ensures adequate rejection of the high-band signal and pilot tones at either 550Hz or 1800Hz. The weighted adjacent channel rejection exceeds 60dB. The group delay response of the filter is compensated by the compromise equalizer, which also compensates for the group delay distortion of typical lines. Only half the line characteristic is compensated in the filter, since 2 filters will always be connected in tandem in an end-to-end application. The group delay characteristic of the low-band filter is shown in Figure 3.

High-Band Filter

The characteristics of the high-band filter are shown in Figure 4. The in-band response has a slope of approximately 1.5dB from edge-to-edge, to compensate for typical line characteristics in this region. The out-of-band attenuation ensures adequate rejection of the low-band signal and pilot tones at either 550Hz or 1800Hz. The weighted adjacent channel rejection exceeds 60dB. Group delay compensation for the filter and half-channel characteristics is provided, as with the low-band filter. The group delay characteristic of the high-band filter is shown in Figure 5.

Figure 1. Typical Amplitude Response



Input and Output Considerations

The input signals to the S3522 should ideally be symmetrical about ground (0 volts). However, and D.C. offset existing at the input pins will not be transmitted to the outputs, since both filters have transmission zeroes at D.C. Since switched capacitor filters are sampled data circuits, care must be taken to avoid aliasing problems caused by signals around the sampling frequency. In the S3522 this means that an anti-aliasing filter should be used at the Receive Input if there is any possibility of input signal components lying in the region of 205.4 ± 3kHz and multiples of this frequency. A smoothing filter may be required at the Transmit Output where the signal is to be transmitted over a telephone line. Care must be taken to avoid distorting the group delay characteristics of the system if a smoothing filter is used. See Figure 6 for Typical Anti-Aliasing Circuit.

Clock Considerations

The S3522 is designed to operate with an externally

Figure 2. Typical Low-Band Amplitude

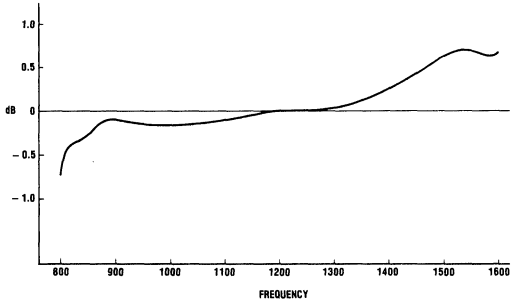


Figure 3. Typical Low-Band Group Delay

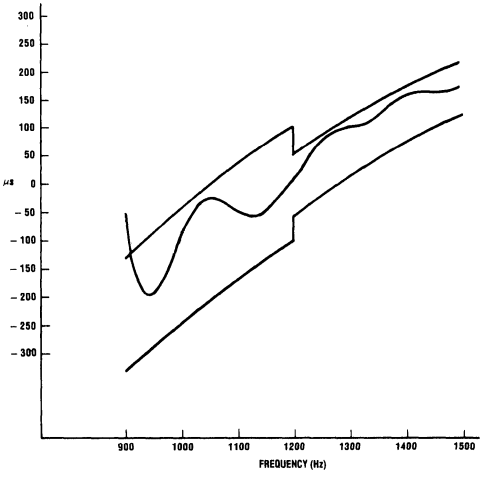


Figure 4. Typical High-Band Amplitude

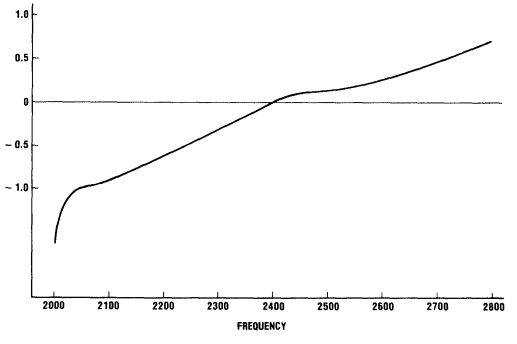


Figure 5. Typical High-Band Group Delay

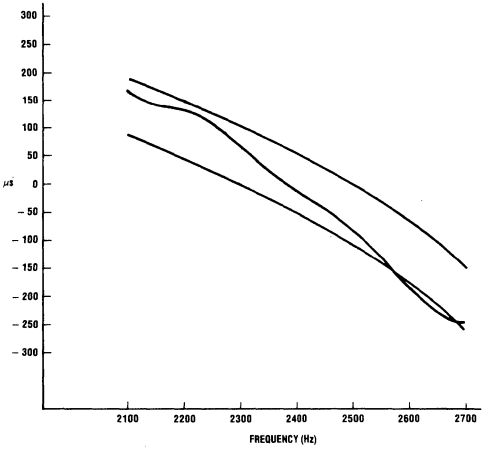
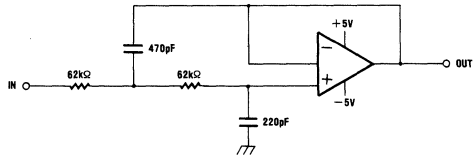


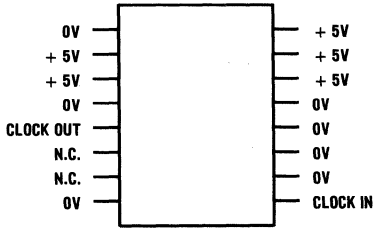
Figure 6. Anti-Aliasing L.P. Filter for S3522 at T_X (OUT) and R_X (IN)



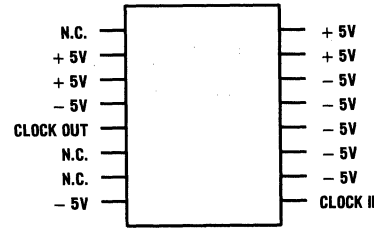
supplied 2.304MHz clock. The accuracy and stability of this frequency will directly affect the accuracy and stability of the filter characteristics. The center frequency and bandwidth may be scaled directly in proportion to the clock frequency if desired to modify them for other applications. The 2.305MHz frequency may be derived from the more commonly available 2.4576MHz by dividing this frequency by 15/16, using a binary rate multiplier (BRM). The BRM will generate an uneven pulse train, since it does the frequency division by eliminating one pulse out of each group of sixteen. This does modify the performance of the S3522, since it effectively modulates the sampling frequency. However, the only consequence is the generation of low level out-of-band signals, the largest of which is more than 50dB below the signal level. The in-band performance is not measureably affected. The BRM can be either TTL (7497), using the 0 and +5 volt supplies, or CMOS (4089) using the −5 and +5 volt supplies. The 4089 requires a 10 volt supply for guaranteed operation at this frequency. The S3522 will operate with a clock "0" level anywhere between +1.4 and −5 volts. Both 7497 and 4089 circuits are shown in Figure 7.

Figure 7. Connections for Clock Divider Circuits

7497 Circuit



4089 Circuit



Pin/Function Descriptions

Pin	Name	Function
1	$TX_{(IN)}$	Transmit Signal Input.
2	V_{DD}	Positive Voltage Supply (4.5 to 5.5 Volts).
3	$HBF_{(OUT)}$	Output from high-band filter without delay equalizer circuit. NOTE that the signal appearing at this pin depends on the state of the MODE input. See text for further information.
4	D_{GND}	Digital Ground. Connect to the ground line common to other digital circuits in system.
5	$OSC_{(IN)}$	2.304MHz Clock Input. This input is TTL and CMOS compatible.
6	$CLK_{(OUT)}$	104.7kHz Buffered Clock Output. This reference output is available to drive other circuitry. The frequency is the Input Clock Frequency divided by 22. The output will drive one CMOS load.
7	$RX_{(OUT)}$	Receive Signal Output. This output will drive a 20kΩ load.
8	$TX_{(OUT)}$	Transmit Signal Output. This output will drive a 20kΩ load.

Pin/Function Descriptions (Continued)

Pin	Name	Function
9, 10	N.C	No Connection.
11	V_{SS}	Negative Voltage Supply (-4.5 to -5.5 Volts).
12	$LBF_{(OUT)}$	Output from low-band filter without delay equalizer circuit. NOTE that the signal appearing at this pin depends on the state of the MODE input. See text for further information.
13	MODE	Originate Answer Mode Control Input. A logic '0' on this pin sets the device to the ORIGINATE mode, with the transmit signal in the low-band and the receive signal in the high-band. A logic '1' sets the device to the ANSWER mode, with the transmit signal in the high-band and the receive signal in the low-band. This input is CMOS and open collector TTL compatible.
14	N.C.	No Connection.
14	A_{GND}	Analog Ground. Connect to the ground line common to other analog circuitry in the system.
16	$RX_{(IN)}$	Receive Signal Input.

Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... $+15.0V$
Operating Temperature ..... $0°C$ to $+70°C$
Storage Temperature ..... $-55°C$ to $+115°C$
Analog Input ..... $V_{SS} - 0.3V \leqslant V_{IN} \leqslant V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°$ to $+70°C$, $V_{DD} = +5V$, $V_{SS} = -5V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply Voltage	4.5	5	5.5	V
V_{SS}	Negative Supply Voltage	-4.5	-5	-5.5	V
V_{IH} (MODE)	High Level Logic Input	4			V
V_{IH} (OSC-IN)	High Level Logic Input		2.8		V
V_{IL} (MODE, OSC-IN)	Low Level Logic Input	V_{SS}		$+0.8$	V
V_{OL} (CLK OUT)	Low Level Logic Output (1 CMOS Load)	V_{SS}		$V_{SS}+0.5$	V
V_{OH} (CLK OUT)	High Level Logic Output (1 CMOS Load)	$V_{DD}-0.5$		V_{DD}	V
R_{IN} (TX IN, RX IN)	Input Resistance		5		$M\Omega$
C_{IN} (TX IN, RX IN)	Input Capacitance		10		pF
R_{OUT} (TX OUT, RX OUT)	Output Resistance		2		$k\Omega$
I_{DD}, I_{SS}	Supply Currents		5	10	mA

A.C. System Specifications: $T_A = 0°$ to $-70°C$, $V_{DD} = +5V$, $V_{SS} = -5V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
f_{0L}	Low-Band Center Frequency		1200		Hz
f_{0H}	High-Band Center Frequency		2400		Hz
BW	Bandwidth (both bands) (−1dB)		800		Hz
A_{F0}	Gain at Center Frequencies	−0.5	0	+0.5	dB
A_{FREL}	Gain Relative to Center Frequency: See Figures 2 and 3				
	@ 800Hz (Low-Band Filter)	−1.0	−0.25	+0.5	dB
	900Hz (Low-Band Filter)	−0.5	0	+0.5	dB
	1500Hz (Low-Band Filter)	0	+0.50	+1.0	dB
	1600Hz (Low-Band Filter)	+0.25	+0.75	+1.25	dB
	2000Hz (High-Band Filter)	−2.0	−1.5	0	dB
	2100Hz (High-Band Filter)	−2.0	−0.8	0	dB
	2700Hz (High-Band Filter)	0	+0.50	+1.0	dB
	2800Hz (High-Band Filter)	+0.25	+0.75	+1.25	dB
GD_{REL}	Group Delay Relative to Center Frequency: See Figures 4 and 5				
	@ 900Hz (Low-Band Filter)		−70		μsec
	1100Hz (Low-Band Filter)		−80		μsec
	1300Hz (Low-Band Filter)		+90		μsec
	1500Hz (Low-Band Filter)		+70		μsec
	2100Hz (High-Band Filter)		+190		μsec
	2300Hz (High-Band Filter)		+50		μsec
	2500Hz (High-Band Filter)		−80		μsec
	2700Hz (High-Band Filter)		−210		μsec
R_{AC}	Adjacent Channel Rejection	50			dB
V_0 (Peak-to-Peak)	Output Voltage Swing		6		V
V_{NL} C-Message Weighted	Noise Level, Low-Band		240		μV RMS
V_{NH} C-Message Weighted	Noise Level, High-Band		240		μV RMS

AMI®

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Preliminary Advanced Product Description **S35212**

212A/V.22 MODEM FILTER WITH EQUALIZERS

COMMUNI-CATIONS

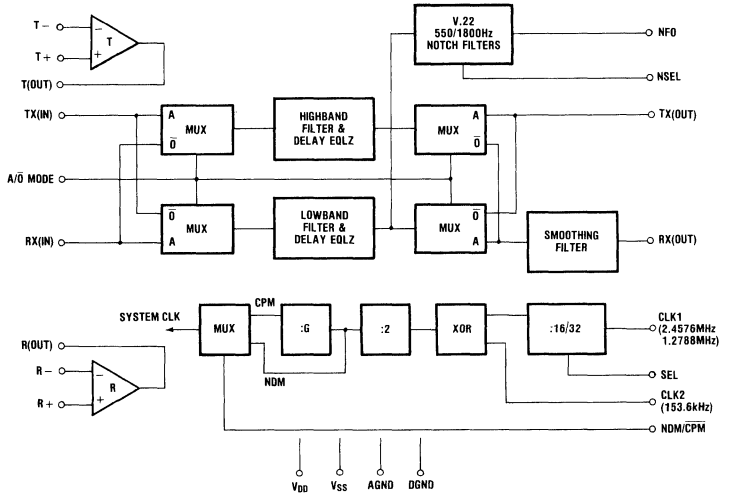
Features

- ☐ Bell 212A/V.22 Compatible
- ☐ Usable for Bell 103/113 Applications
- ☐ High and Low Band Filters With Compromise Group Delay Equalizers and Output Filters
- ☐ CCITT V.22 Compatible Guard Tone Notch Filters
- ☐ Originate/Answer Operating Modes
- ☐ Low Power CMOS: 75 mW Typ.
- ☐ Wide Supply Operation (±4V to ±6V)
- ☐ Two Uncommitted Operational Amps.
- ☐ Choice of Clocking Frequencies: 2.4576MHz, 1.2788MHz, or 153.6kHz
- ☐ Detection of Call Process Tones

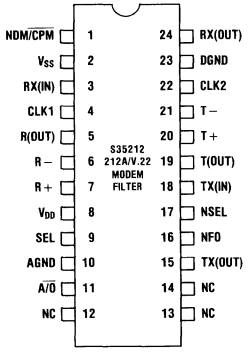
General Description

The AMI S35212 Model Filter is a monolithic CMOS integrated circuit designed to implement both the filtering and equalizing functions required in Bell 212A and CCITT V.22 modems. The S35212 includes both the transmit signal shaping filter and the receive signal separation filter and features on-chip originate/answer mode selection capability. In addition, half-channel compromise amplitude and group delay equalizers are included giving full compromise equalization through the transmit and receive filter pair. For CCITT V.22 applications a notch filter is included. It can be programmed to provide rejection at 1800Hz or 550Hz. Two

Block Diagram



Pin Configuration



General Description (continued)

uncommitted operational amplifiers are provided which can be used as amplifiers or anti-aliasing filters for each filter. A continuous low pass filter is also included on the RX(OUT) which acts as a smoothing filter. Provision is made to select between detection of call process tone detection mode and the normal data transmission mode. For maximum flexibility the S35212 may be operated from a 2.4576MHz, 1.2788MHz, or 153.6kHz clock.

Pin/Function Description

Pin Name	Pin Number	Function
T−, T+, T(OUT)	19, 20, 21	Inverting and non-inverting inputs and output respectively for the T-amplifier. T-amplifier may be used in an anti-aliasing filter.
TX(IN)	18	Transmit Data Input.
A/$\overline{O}$	11	Mode Selection: (Answer/Originate Modes).
RX(IN)	3	Receive Data Input.
R−, R+, R(OUT)	6, 7, 5	Inverting and non-inverting inputs and output respectively for the R-amplifier. R-amplifier may be used in an anti-aliasing filter.
NFO	16	Notch Filter Output.
NSEL	17	Notch Filter Selection: (550Hz or 1800Hz).
TX(OUT)	19	Transmit Data Output.
RX(OUT)	24	Receive Data Output.
CLK1	4	Clock Input: (2.4576MHz or 1.2788MHz).
SEL	9	Divider Selection Input (÷16 when CLK1 is 1.2788MHz and ÷32 when CLK1 is 2.4576MHz).
CLK2	22	Clock Input: 153.6kHz.
NDM/$\overline{CPM}$	1	Mode Selection: Normal Data Mode/$\overline{\text{Call Progress Mode}}$. Mode Selection: Normal
V_{DD}, V_{SS}	8, 2	+5 Volts, −5 Volts.
AGND, DGND	10, 23	Analog Ground, Digital Ground.
	12, 13, 14	No Connection to these pins.

AMI®

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S3525A/S3525B

DTMF BANDSPLIT FILTER

COMMUNICATIONS

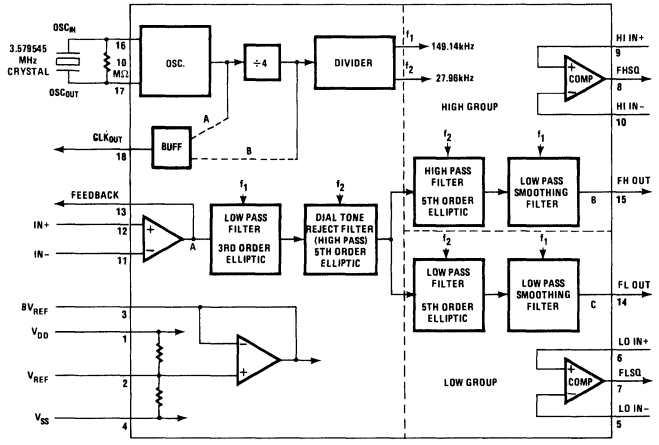
Features

- ☐ CMOS Technology for Wide Operating Single Supply Voltage Range (7.0V to 13.5V). Dual Supplies (±3.5V to ±6.75V) Can Also Be Used.
- ☐ Uses Standard 3.58MHz Crystal as Time Base. Provides Buffered Clock to External Decoder Circuit.
- ☐ Ground Reference Internally Derived and Brought Out.
- ☐ Uncommitted Differential Input Amplifier Stage for Gain Adjustment
- ☐ Filter and Limiter Outputs Separately Available Providing Analog or Digital Outputs of Adjustable Sensitivity.
- ☐ Can be Used with Variety of Available Decoders to Build 2-Chip DTMF Receivers.

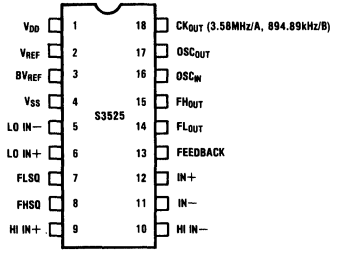
General Description

The S3525 DTMF Bandsplit Filter is an 18-pin monolithic CMOS integrated circuit designed to implement a high quality DTMF tone receiver system when used with a suitable decoder circuit. The device includes a dial tone filter, high group and low group separation filters and limiters for squaring of the filtered signals. An uncommitted input amplifier allows a programmable gain stage or anti-aliasing filter. An overall signal gain of 6dB is provided for the low group and high group signals in the circuit. The dial tone filter is designed to provide a rejection of at least 52dB in the frequency band of 300Hz to 500Hz. The difference between the S3525A and the S3525B is the frequency of output clock signal at the CKOUT pin. In the S3525B, it is a 894.89kHz square wave while in the S3525A, it is a

Block Diagram



Pin Configuration



Functional Description (Continued)

3.58MHz buffered oscillator signal. The S3525A can be used with digital DTMF decoder chips that need the TV crystal time base allowing use of only one crystal between the filter and decoder chips.

Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... +15.0V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +125°C
Analog Input ..... $V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

DC Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref to V_{SS})		9.6	12.0	13.5	V
$V_{OL(CKOUT)}$	Logic Output "Low" Voltage $I_{OL} = 160\mu A$			$V_{SS} + 0.4$		V
$V_{OH(CKOUT)}$	Logic Output "High" Voltage $I_{OH} = 4\mu A$			$V_{DD} - 1.0$		V
$V_{OL(FH, FL)}$	Comparator Output Voltage Low	500pF Load			$V_{SS} + 0.5$	V
		10kΩ Load			$V_{SS} + 2.0$	V
$V_{OH(FH, FL)}$	Comparator Output Voltage High	500pF Load	$V_{DD} - 0.5$			V
		10kΩ Load	$V_{DD} - 2.0$			V
$R_{INA\ (IN-, IN+)}$	Analog Input Resistance		8			MΩ
$C_{INA\ (INA-, IN+)}$	Analog Input Capacitance				15	pF
V_{REF}	Reference Voltage Out		0.49 ($V_{DD} - V_{SS}$)	0.50 ($V_{DD} - V_{SS}$)	0.51 ($V_{DD} - V_{SS}$)	V
$V_{OR} = [BV_{REF} - V_{REF}]$	Offset Reference Voltage				50	mV
P_D	Power Dissipation	$V_{DD} = 10V$		170		mW
		$V_{DD} = 12.5V$		400		mW
		$V_{DD} = 13.5V$ and 0°C			650	mW

AC System Specifications:

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
A_F	Pass Band Gain		5.5	6	6.5	dB
	Dial Tone Rejection Dial Tone Rejection is measured at the output of each filter with respect to the passband					
DTR_L	Low Group Rejection	350Hz	55	59		dB wrt 700Hz
		440Hz	50	53		dB wrt 700Hz
DTR_H	High Group Rejection	Either Tone	55	68		dB wrt 1200Hz

AC System Specifications (Continued)

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
	Attenuation Between Groups				
	Attenuation of the nearest frequency of the opposite group is measured at the output of each filter with respect to the passband				
GA_L	Attenuation of 1209Hz	50	>60		dB wrt 700Hz
GA_H	Attenuation of 941Hz	40	42		dB wrt 1200Hz
	Total Harmonic Distortion				
THD	Total Harmonic Distortion (dB). Dual tone of 770Hz and 1336Hz sine-wave applied at the input of the filter at a level of 3dBm each. Distortion measured at the output of each filter over the band of 300 Hz to 10kHz ($V_{DD} = 12V$)			−40	dB
	Idle Channel Noise				
ICN	Idle Channel Noise measured at the output of each filter with C-message weighting. Input of the filter terminated to BV_{REF}			1	mV_{rms}
	Group Delay (Absolute)				
GD_L	Low Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms
GD_H	High Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms

Pin/Function Descriptions

OSC_{IN}, OSC_{OUT} — These pins are for connection of a standard 3.579545MHz TV crystal and a 10MΩ ±10% resistor for the oscillator from which all clocking is derived. Necessary capacitances are on-chip, eliminating the need for external capacitors.

CKOUT (S3525A) — Oscillator output of 3.58MHz is buffered and brought out at this pin. This output drives the oscillator input of a decoder chip that uses the TV crystal as time base. (Only one crystal between the filter and decoder chips is required.)

CKOUT (S3525B) — This is a divide by 4 output from the oscillator and is provided to supply a clock to decoder chips that use 895kHz as time base.

IN −, IN +, Feedback — These three pins provide access to the differential input operational amplifier on chip. The feedback pin in conjunction with the IN − and IN + pins allows a programmable gain stage and implementation of an anti-aliasing filter if required.

FH OUT, FL OUT — These are outputs from the high group and low group filters. These can be used as inputs to analog receiver circuits or to the on-chip limiters.

HI IN −, HI IN +
LO IN −, LO IN + — These are inputs of the high group and low group limiters. These are used for squaring of the respective filter outputs. (See Figure 2.)

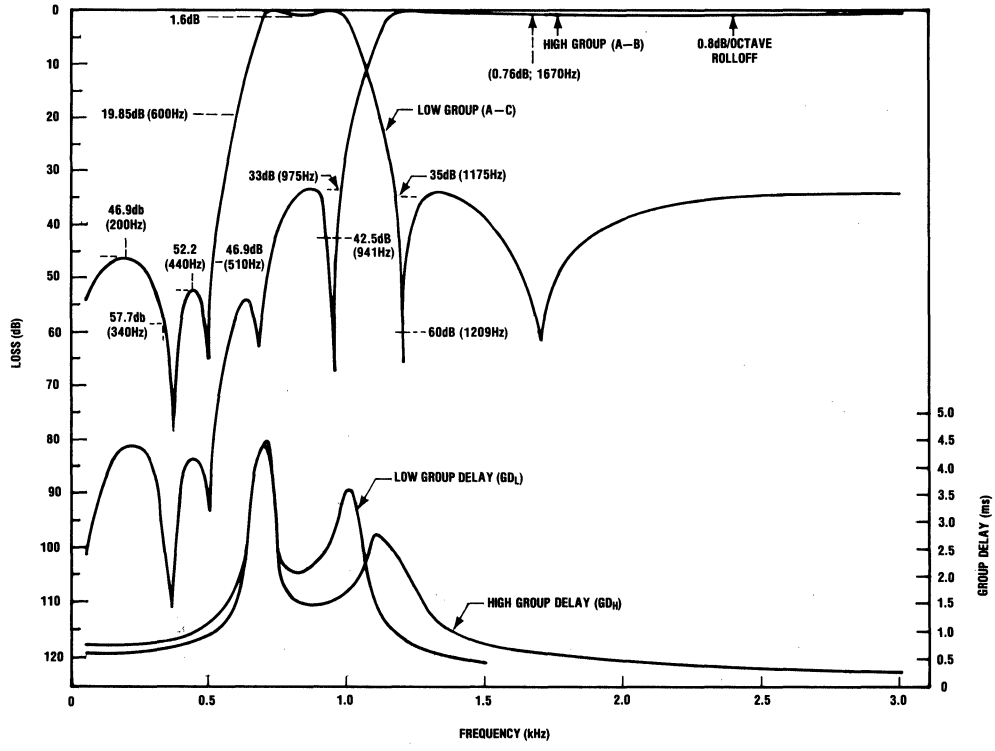
FHSQ, FLSQ — These are respectively the high group and low group square wave outputs from the limiters. These are connected to the respective inputs of digital decoder circuits.

V_{DD}, V_{SS} — These are the power supply voltage pins. The device can operate over a range of $7V \leqslant (V_{DD} - V_{SS}) \leqslant 13.5V$.

V_{REF} — An internal ground reference is derived from the V_{DD} and V_{SS} supply pins and brought out to this pin. V_{REF} is $1/2(V_{DD} - V_{SS})$ above V_{SS}.

BV_{REF} — Buffered V_{REF} is brought out to this pin for use with the input and limiter stages.

Figure 1. Typical S3525 DTMF Bandsplit Filter Loss/Delay Characteristics



Input Configurations

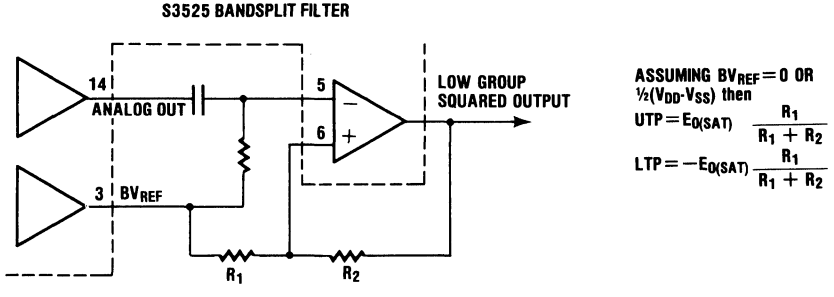
The applications circuits show some of the possible input configurations, including balanced differential and single ended inputs. Transformer coupling can be used if desired. The basic input circuit is a CMOS op amp which can be used for impedance matching, gain adjustment, and even filtering if desired. In the differential mode, the common mode rejection is used to reject power line-induced noise, but layout care must be taken to minimize capacitive feedback from pin 13 to pin 12 to maintain stability.

Since the filters have approximately 6dB gain, the inputs should be kept low to minimize clipping at the analog outputs (FL_{OUT} and FH_{OUT}).

Output Considerations

The S3525 has both analog and digital outputs available. Most integrated decoder circuits require digital inputs so the on-chip comparators are used with hysteresis to square the analog outputs. The sensitivity of the receiver system can be set by the ratio of R1 and R2, shown in Figure 2. The amount of hysteresis will set the basic sensitivity and eliminate noise response below that level.

Figure 2. Typical Squaring Circuit



ASSUMING $BV_{REF} = 0$ OR $\frac{1}{2}(V_{DD}-V_{SS})$ then

$$UTP = E_{O(SAT)} \frac{R_1}{R_1 + R_2}$$

$$LTP = -E_{O(SAT)} \frac{R_1}{R_1 + R_2}$$

Clock Considerations

The clock is provided by a standard 3.58MHz TV crystal in parallel with a 10MΩ resistor across pins 16 and 17. A buffered output at pin 18 is provided to drive the companion decoder at 3.58MHz (S3525A) or 895kHz (S3525B). It can be directly coupled or capacitively coupled depending on the decoder.

The circuits shown are not necessarily optimal but are intended to be good starting points from which an optimal design can be developed for each individual application.

Applications

Companion decoders to be used with the S3525 vary in performance and features. Teltone Corporation's TT6174, MOSTEK's MK5102/03 and Nitron's NC2030 are available units that can be used with the S3525.

Figure 3. AMI/Teltone 2 Chip DTMF Receiver

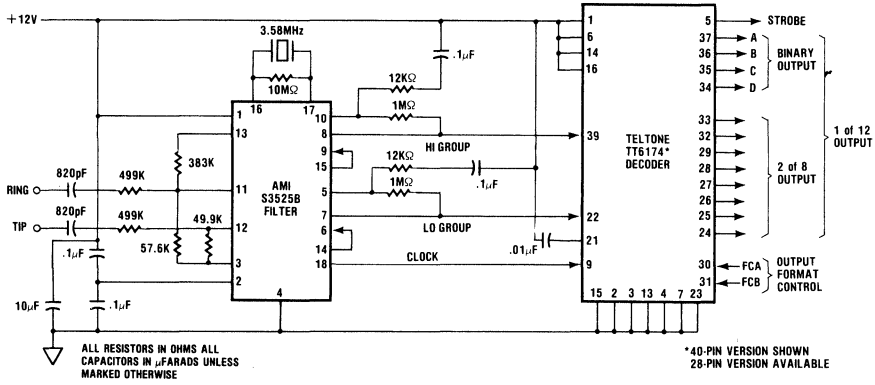


Figure 2. AMI/Mostek 2 Chip DTMF Receiver

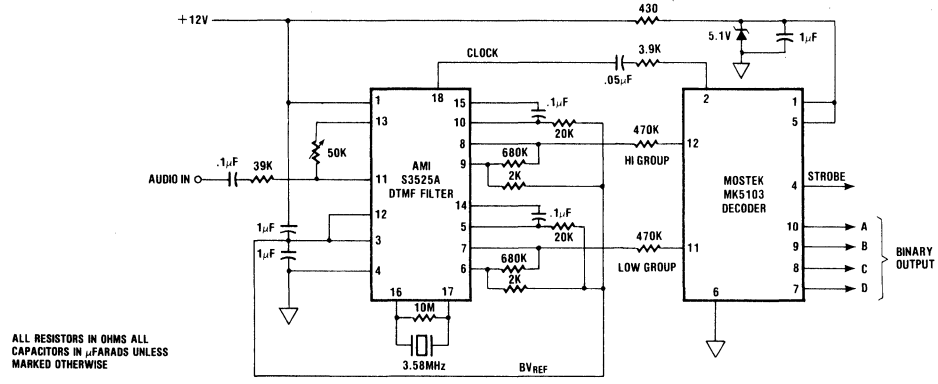
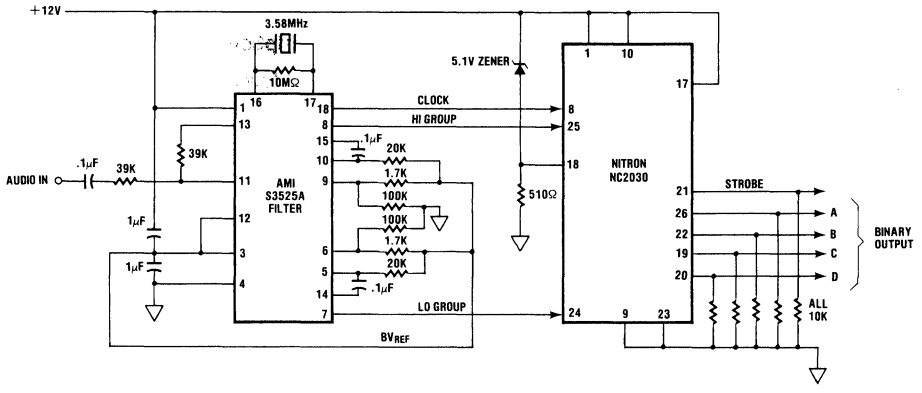


Figure 5. AMI/Nitron 2 Chip DTMF Receiver



ALL RESISTORS IN OHMS ALL CAPACITORS IN μFARADS UNLESS MARKED OTHERWISE

AMI

A Subsidiary of Gould Inc.

Advanced Product Description **S3526**

SINGLE FREQUENCY TUNEABLE BANDPASS/NOTCH FILTER/TONE GENERATOR

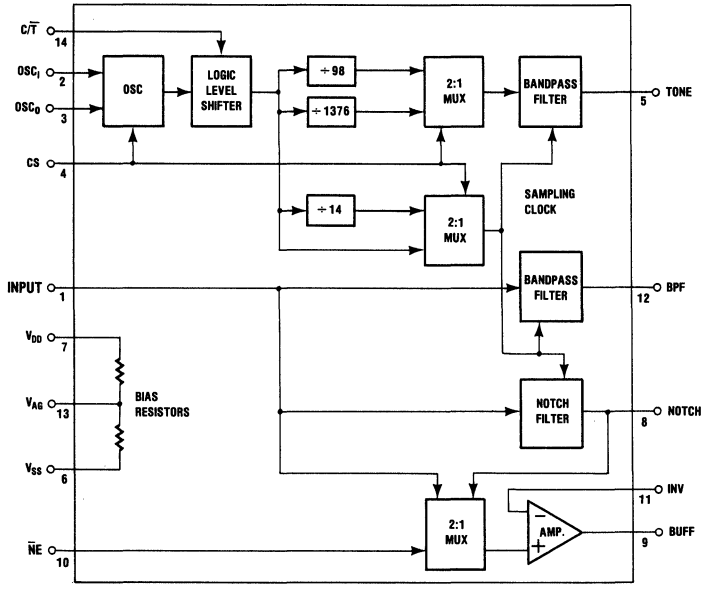
Features

- ☐ Center Frequency of Filters Match and Track Frequency of Generated Tone
- ☐ Tone Frequency Adjustable Over a 100Hz to 5kHz Range
- ☐ Unfiltered Input, Input with Notched Tone, Input Tone and Tone Generator Outputs
- ☐ Operation from a Crystal or External CMOS/TTL Clock
- ☐ Operation at 2600Hz from a Low Cost 3.58MHz TV Color Burst Crystal or 256kHz Ext. Clock
- ☐ Buffered Output Drives 600Ω Loads
- ☐ Single or Split Supply Operation
- ☐ Low Power CMOS Technology

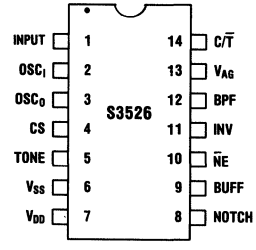
General Description

The S3526 is a low power CMOS Circuit which may be used in a variety of single frequency (SF) communication applications such as SF-Tone Receivers, Tone Remote Control in Mobile systems, Loopback Diagnostics in Modems, control of Echo Cancellers, dialing and privacy functions in Common Carrier Radio Telephone, etc. The main functional blocks of the S3526 include a low distortion tone (sinewave) generator whose frequency may be programmed using a crystal (i.e. 2600Hz using a low cost TV color burst crystal) or external clock time base; a bandpass filter used to extract tone information from the input signal; a band reject filter which is used to "Notch" out tone information from the input signal; and a buffer amplifier with selectable input (unfiltered input signal, or input signal with tone notched) capable of driving a 600Ω load.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$) ..... + 15.0V
Operating Temperature ..... 0°C to + 70°C
Storage Temperature ..... − 65°C to + 150°C
Input Voltage, All Pins ..... $V_{SS} - 0.3V < V_{IN} < V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to + 70°C, $(V_{DD} - V_{SS}) = 10V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation (Maximum @13.5V)		100	275	mW
R_{IN}	Input Resistances (Except Input)	8			MΩ
C_{IN}	Input Capacitances			15.0	pF

General Analog Signal Parameters: $T_A = 0°C$ to + 70°C, $(V_{DD} - V_{SS}) = 10V$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Straight Through Gain (Measured at − 10dBm0)	− 0.5	0	0.5	dB
Z_{IN}	Input Impedance (Input, Pin 1)		2.5		MΩ
TLP	Transmission Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level (+ 3dBm0)		2.1		VRMS
R_L	Load Resistance (BPF, NOTCH)	10			kΩ
R_L	Load Resistance (BUFF)	600			ohms
V_{OSB}	Buffer Output Offset Voltage		± 50	± 150	mV
ICN_P	Idle Channel Noise in Pass Condition		2		dBrnC0
V_{OUT}	Output Signal Level into R_L for NOTCH, BPF, BUFF	2.0	2.1		VRMS
V_{OT}	Sine Wave (Tone) Output (Load = 10KΩ)		$0.6(V_{DD} - V_{SS})$ ± 0.5dB		Vpk-pk
V_{TD}	Sine Wave Distortion (f_{OSC} = 3.58MHz) (See Figure 4)		− 35		dB

Filter Performance Specifications

Band Pass Filter Characteristics $T_A = 0°C$ to + 70°C, $(V_{DD} - V_{SS}) = 10V$, $f_{OSC} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{FS}	Maximum Input Voltage (+ 3dBm0)		2.1		VRMS
A_{BP}	Passband Gain @ − 10dBm0	− 0.8	0	+ 0.8	dB
I_{CN}	Idle Channel Noise		24		dBrnC0
V_{OS}	Output Offset		± 50	± 150	mV
	2600Hz Bandpass Filter Response (referenced from 2600Hz, + 3dBm0) (See Figures 1 and 2)				
	DC to 1600Hz		− 80		dB
	2100Hz		− 63	− 50	dB
	2400Hz		− 37	− 30	dB
	2540Hz		− 7.0	− 3	dB
	2560Hz	− 3	− 1.8		dB
	2640Hz	− 3	− 1.0		dB
	2660Hz		− 5.4	− 3	dB
	2800Hz		− 35	− 30	dB
	3100Hz		− 58	− 50	dB
	3600Hz		− 74		dB
DR	Dynamic Range (V_{FS} to ICN)		70		dB

Notch Filter Characteristics $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$ (Symmetrical Supplies), $f_{OSC} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{FS}	Maximum Input Voltage (+3dBm0)		2.1		VRMS
A_{BR}	Passband Gain @ −10dBm0)	−0.5	0	+0.5	dB
ICN	Idle Channel Noise		18		dBrnC0
V_{OS}	Output Offset		±100	±225	mV
DR	Dynamic Range (V_{FS} to ICN)		75		dB
	2600Hz Notch Filter Response (referenced from 1000Hz, (+3dBm0) (See Figures 1 and 3)				
	250Hz to 2200Hz	−0.5	±0.1	0.5	dB
	2200Hz to 2400Hz	−5.0		0.5	dB
	2585Hz to 2615Hz		−70	−53	dB
	2800Hz to 3000Hz	−5.0		0.5	dB
	3000Hz to 3400Hz	−0.5	±0.1	0.5	dB

Digital Electrical Parameters $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$

Symbol	Mode Control Logic Levels	Min.	Typ.	Max.	Units
V_{IH}	C/T CMOS Operation (Pin 14)	$V_{DD} - 0.5$		V_{DD}	V
V_{IL}	C/T TTL Operation (Pin 14)	V_{SS}		$V_{DD} - 4$	V
V_{IH}	CS for Low Speed Clock Input	$V_{DD} - 0.5$		V_{DD}	V
V_{IL}	CS for Crystal or High Speed Clock	V_{SS}		V_{AG}	V
	CMOS Logic Levels				
V_{IH}	Input Voltage "1" Level	$V_{AG} + 2$		V_{DD}	V
V_{IL}	Input Voltage "0" Level	V_{SS}		$V_{AG} - 2$	V

Control Pin Definitions

Pin#	Name	Connection	Operation	Note
14	C/T	V_{DD} to $(V_{DD} - 0.5V)$	CMOS Logic Levels	1
		$(V_{DD} - 4V)$ to V_{SS}	TTL Logic Levels	
4	CS	V_{DD}	Ext. Low Speed Sq. Wave Clock @ Pin 3	2
		V_{SS} or V_{AG}	Crystal Connected Between Pins 2 and 3 or High Speed Clock to Pin 2	
10	$\overline{NE}$	V_{DD} to .7 $(V_{DD} - V_{SS})$	Buffer Out = Input Signal	
		V_{SS} to .3 $(V_{DD} - V_{SS})$	Buffer Out = Notch Filter Out	

NOTES: 1) CMOS logic levels are same as V_{DD} and V_{SS} supply voltage levels. For TTL interface ground of TTL logic must be connected to V_{SS} supply pin.
2) For ext. low speed clock operation pin 2 must be connected to V_{DD}. For ext. high speed clock, drive pin 2, leave pin 3 open.
3) The performance specifications are guaranteed with ±5% power supplies for normal operation.

Pin Function Description

Pin	No.	Function
Input	1	This pin is the analog input to the filters and the buffer. It is a high impedance input ($Z \cong 2.5M\Omega$).
OSC_I OSC_O	2 3	These pins are the timing control for the entire chip. A crystal may be connected across these two pins in parallel with a 10MΩ resistor. Another option is to provide an ext clock at pin 3 and connect pin 2 to V_{DD}. TTL or CMOS may be used. As a third choice, a CMOS level external clock may be applied to pin 2 directly leaving pin 3 open.
CS	4	Clock Select-This pin when tied to V_{DD} configures the chip to operate from a low speed clock. When tied to V_{AG} or V_{SS} the chip operates from external crystal or high speed clock.
TONE	5	This is an output pin providing a sine wave with a frequency of fosc ÷ 1376 if CS is low or fosc ÷ 98 if CS is high.
V_{SS}	6	Negative supply voltage pin. Typically $-5V \pm 5\%$
V_{DD}	7	Positive supply voltage pin. Typically $+5V \pm 5\%$.
NOTCH	8	Band Reject (Notch) Filter-This is the output of the filter that notches the tone information from the input signal. It is capable of driving a load $\geq 10k\Omega$.
BUFF	9	Buffer Output-The buffer is capable of driving a 600Ω load and provides from its output either the signal input without filtering, or the signal input with the tone frequency notched out.
$\overline{NE}$	10	Notch Enable-This pin controls which signal is presented to the buffer input. A logic high (V_{DD}) connects the input signal. A logic low (V_{SS}) connects the output of the band reject (notch)filter.
INV	11	Inverting-This is the inverting input of the buffer.
BPF	12	Band Pass Filter-This is the output of the band pass filter which will pass any energy at the tone frequency present in the input signal. It is capable of driving a load $\geq 10k\Omega$.
V_{AG}	13	Analog Ground-This is the analog ground pin. When used with a single supply, this pin is ½ ($V_{DD} - V_{SS}$) ±100mV. When used with ±5V supplies, this point is at ground. The S3526 has internal voltage divider resistors to V_{DD} and V_{SS} of $\cong 20k\Omega$.
$C/\overline{T}$	14	CMOS/TTL-This pin determines whether CMOS or TTL levels will be accepted at pin 3 for a clock input. When tied to V_{DD}, the chip accepts CMOS logic levels. When tied to a point $\leq (V_{DD} - 4V)$, the chip accepts TTL levels. For crystal operation pin 14 should be at V_{DD}.

Application Information

The S3526 device is a very versatile filter chip. Although it was designed for the telephone market SF signaling application when used with the commonly available TV colorburst crystal, it will work over a wide range of frequencies. Typically, it will cover from 100Hz to 5kHz providing coverage of the entire voice band for in-band signaling.

Because it is a very high Q filter the transient response time must be considered when determining the maximum data rate for a particular frequency. This response is illustrated in Figure 5 and shows that it is quite adequate for 10 pulse-per-second (50% duty cycle) data rate at 2600Hz. But the same data rate could not be used at 500Hz, for example, as a detector could not differentiate between tone on and tone off conditions.

Figure 1. Typical Filter Performance Curves at 2600Hz

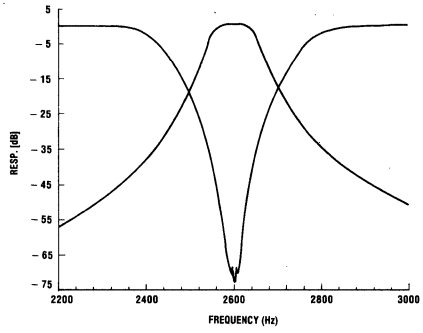


Figure 2. Typical Bandpass Response

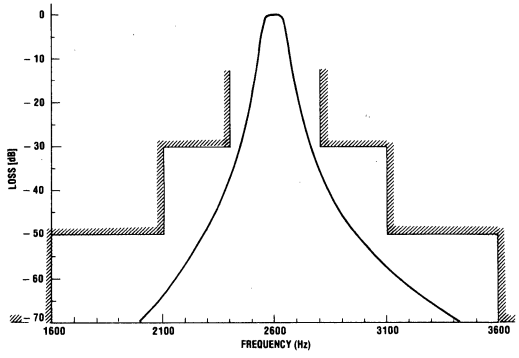


Figure 3. Typical Notch Response

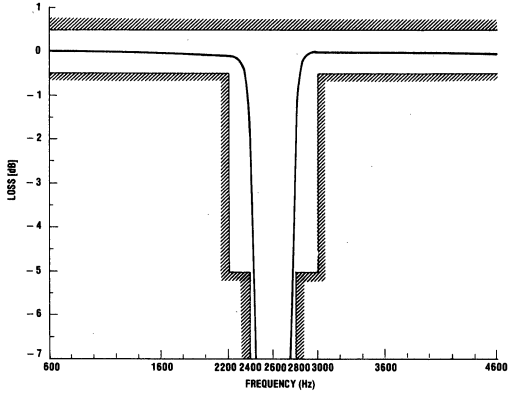


Figure 4. Typical Sine Wave Output Spectrum from Pin 5

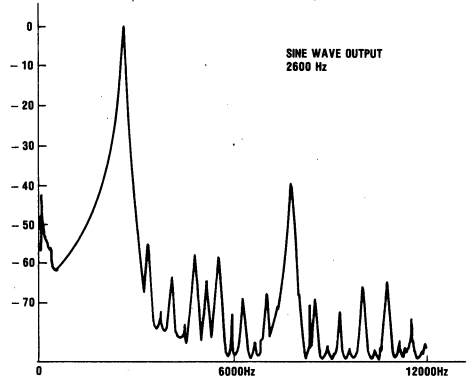


Figure 5. Typical Delay Characteristics at + 3dBmO with 2600Hz Pulsed at 10pps with 50% Duty Cycle

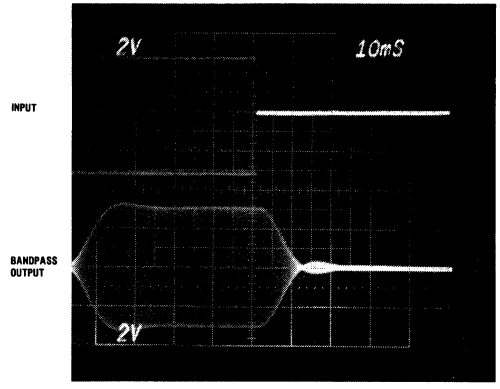
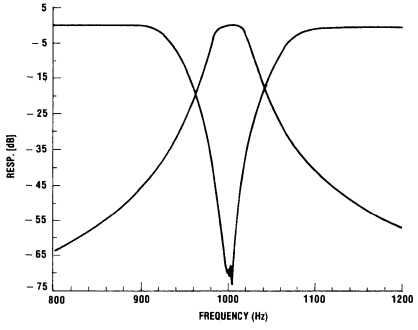


Figure 6. Typical Filter Performance Curves at 1000Hz



The combination of tone generator, notch filter, and bandpass filter allows one to generate a signaling tone at the sending end and notch it out at the receiving end, as well as detect it through the bandpass filter. For reliable detection the output of the bandpass filter can be compared with the output of the bandreject filter. If the output of the BR filter is within a fixed ratio of the BP filter (such as 10dB) then the signal present may be considered voice rather than signaling and ignored.

In situations where the entire voice band is desired except during signaling the buffer output can be switched straight through to the input. When the output of the filters indicates that a signaling tone is present, the $\overline{NE}$ pin can be switched low, switching the notch filter into the signal path to prevent the tone from reaching the listener or from being passed further down the system to another signaling receiver.

By using the notch filter with telephone accessories it can be guaranteed that the accessory will not violate the telephone company specifications about transmitting 2600Hz into the lines, causing disconnected calls.

Power Supplies

The S3526 will work with either single or dual power supplies. When used with dual power supplies ($\pm$ 5V) the analog inputs and outputs will be referenced to ground. If an external clock signal is provided, rather than using a crystal, it must be swinging from V_{SS} to V_{AG} for TTL swings or from V_{SS} to V_{DD} for CMOS swings. If this is not convenient the signal can be capacitively coupled into pin 3 as illustrated in Figure 7. In the dual supply mode, the power supplies should track or maintain close tolerances for maximum accuracy. If the supplies should skew, the filter characteristics will change very slightly and in most applications, will have no effect at all but can be seen if the curves are plotted on high accuracy equipment.

When using the S3526 on a single power supply the analog inputs and outputs will be referenced to V_{AG} which is ½ ($V_{DD} - V_{SS}$). This means that the analog signals may need to be capacitively coupled in and out if they are normally ground referenced. For example, the input may appear as in Figure 8. But when an external clock is used in the single supply situation it can be direct coupled TTL levels referenced to ground.

Selecting Clocking Sources

The switched capacitor filter design allows the S3526 to be easily tuned by varying the clock frequency. This makes it useful for many applications in telephone signaling, data communications, medical telemetry, test equipment, automatic slide projectors, etc. The necessary clock frequency can be determined by multiplying the desired center frequency by 1376. This frequency

can then be provided from a crystal, an external clock, or a rate multiplier chip. With Clock Select (CS), pin 4 tied low the TONE, pin 5, will provide the desired frequency and the filters will be centered around that frequency. There are many common, low cost microprocessor frequency crystals available that might be very close to a desired frequency. Table 1 illustrates some possible application frequencies. For example, by using a standard 3.00MHz crystal the 2175Hz tone would be 2180Hz or .23% high.

If it is desired to use a lower frequency clock and precision tone generation is not required the external clock can be determined by multiplying the center frequency by 98.4, and tying Clock Select (CS) pin 4 high. Note that the TONE, pin, 5, is not accurate in this situation, being .41% higher than the filter center frequency, although it will fall well within the passband of both filters and be perfectly usable.

Figure 7. External Clock Drive

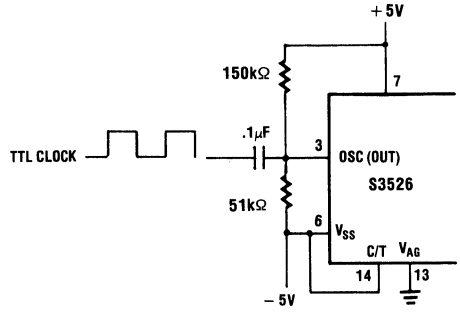


Figure 8.

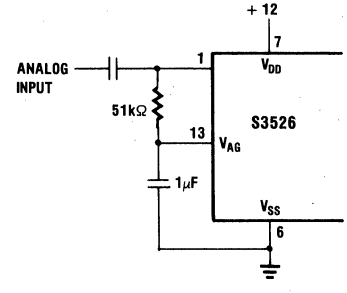


Table 1. Tone and Clock Frequencies for Various Applications

Tone In Hertz	Application	XTAL or HIGH Freq. Clock (MHz)	Ext. Clock Input (Hz)
550	Pilot Tone—Data Comm	.756800	54,120
1000	Test Tone	1.376000	98,400
1020	Test Tone	1.403520	100,368
1400	Medical Telemetry	1.926400	137,760
1600	SF Signaling—Military	2.201600	157,440
1800	Pilot Tone-Data Comm	2.476800	177,120
1850	Pilot Tone-Radio	2.545600	182,040
1950	Pilot Tone-Radio	2.683200	191,880
2125	Echo Suppressor Disable	2.924000	209,100
2150	Echo Suppressor Disable	2.958400	211,560
2175	Guard Tone-Radio	2.992800	214,020
2280	SF Signaling-Telephone	3.137280	224,352
2400	SF Signaling-Telephone	3.302400	236,160
2600	SF Signaling-Telephone	3.579545	256,000
2713	Loopback Tone-Datacom	3.733088	266,959
2800	SF Signaling-Telephone	3.852800	275,520
2805	Signaling Tone-Radio	3.859680	276,012
3825	SF Signaling-European	5.263200	376,380

S3528

PROGRAMMABLE LOW PASS FILTER

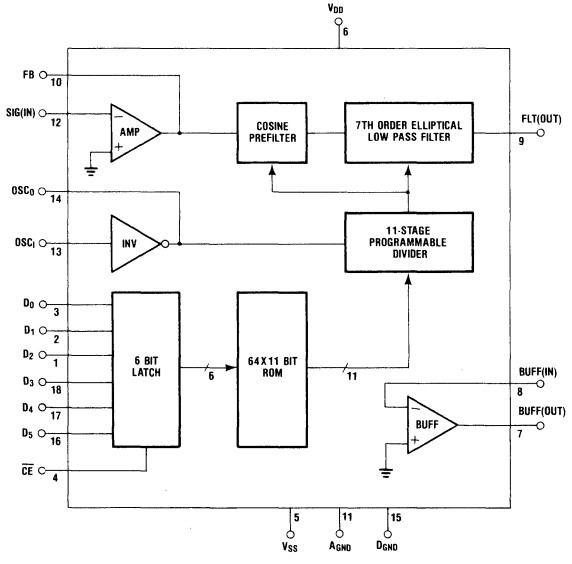
Features

- ☐ Seventh Order Ellipitical Ladder Filter with Cosine Prefiltering Stage
- ☐ Cutoff Frequency (f_C) Range of 10Hz to 20kHz, 40Hz to 20kHz Via 3.58MHz TV Crystal
- ☐ Passband Ripple: <0.1dB
- ☐ Stopband Attenuation: >51dB for $f>1.3f_C$
- ☐ Cutoff Frequency Selectable in 64 Steps Via Six Bit Control Word
- ☐ Steps May Be Custom Programmed from a Set of 2,048 Discrete Points Via Internal ROM
- ☐ Cutoff Frequency Continuously Variable Via External Clock (Crystal, Resonator, or TTL/CMOS Clock)
- ☐ Uncommitted Input and Output Op Amps for Anti-Aliasing and Smoothing Functions
- ☐ Low Power CMOS Technology

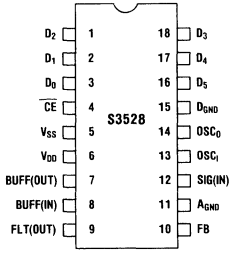
General Description

The S3528 is a programmable low pass filter which may be used in a wide variety of filtering applications commonly found in speech analysis, telecommunications, test equipment and instrumentation, etc. The 3528's CMOS design using switched capacitor design techniques allows easy programming of the filter's cutoff frequency (f_C), discretely, in 64 steps via a six bit control word or continuously by varying the external time base. The useful range of operation of the filter passband extends from 10Hz to 20kHz. When operating from a low cost TV crystal (3.58MHz) a range of 40Hz to 20kHz may be realized. For special applications the S3528 may be customized via the internal ROM to accomodate a specific set of cutoff frequencies from a choice of 2,048 possiblities.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$)	+ 15.0V
Operating Temperature	0°C to + 70°C
Storage Temperature	− 65°C to + 150°C
Input Voltage, All Pins	$V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation @10V @13.5V		70 135	110 225	mW mW
R_{IN}	Input Resistance Pins—1-4, 8, 12, 13, 16-18	8			MΩ
C_{IN}	Input Capacitance Pins—1-4, 8, 12, 13, 16-18			15.0	pF

General Analog Signal Parameters: $(V_{DD} - V_{SS}) = 10V$, $T_A = 0°C$ to $+70°C$, $f_{OCC} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Pass Band Gain at 0.6 f_C	−0.5	0	0.5	dB
V_0	Reference Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level (+ 3dBm0)		2.1		VRMS
R_L	Load Resistance FLT (OUT), Pin 9	10			kΩ
R_L	Load Resistance BUFF (OUT), Pin 7	600			ohms
V_{OUT}	Output Signal Level into R_L for FLT (OUT), BUFF (OUT), $V_{IN} = 2.1V$	2.0	2.1		VRMS
THD	Total Harmonic Distortion at .3f_C		.3		%
WBN	Wideband Noise (to 30kHz) $f_C = 3.2kHz$		.15		mVRMS
WBN	Wideband Noise (to 80kHz) $f_C = 15kHz$		.13		mvRMS
ICN	Idle Channel Noise $f_C = 3200Hz$		8	23	dBrnC0
V_{OS}	Buffer Output (Pin 7) Offset Voltage		±10	±30	mV
V_{OFS}	Filter Output (Pin 9) Offset Voltage		±80	±200	mV

Filter Performance Specifications
Low Pass Filter Characteristics: $f_{osc} = 3.58MHz$, $(V_{DD} - V_{SS}) = 10V$, $T_A = 0°C$ to $+70°C$

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
	Pass Band Ripple (Ref. 0.6 f_C)		−0.5	±0.05	0.5	dB
Filter Response(1): F_C = 3200Hz (Pin 9)						
	(See Figure 5)	(fc) 3200Hz	−0.5	±0.1	0.5	dB
		(1.06fc) 3372Hz	−5.5	−3.0	−0.5	dB
		(1.27fc) 4060		−42		dB
		(1.3fc) 4155		−51	−48	dB
		(1.32fc) 4235		−65	−48	dB
		(1.62fc) 5175		−75	−48	dB
	(1.3fc Upward)	4155 to 100,000Hz		< −51		dB
DR	Dynamic Range (V_{FS} to ICN)			82		dB

Digital Electrical Parameters: $V_{DD} = +5V$, $V_{SS} = -5V$, $T_A = 0°C$ to $+70°C$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	Volts
V_{IL}	Input Low Voltage	V_{SS}		0.8	Volts
I_N	Input Leakage Current ($V_{IN} = 0$ to 4VDC)			10	μADC
C_{IN}	Input Capacitance			15	pF

Digital Timing Characteristics

t_{CE}	$\overline{\text{Chip Enable}}$ Pulse Width	200	300		nsec
t_{AS}	Address Setup Time		300		nsec
t_{AH}	Address Hold Time		20		nsec
f_{osc}	Crystal Oscillator Frequency(2)		3.58		MHz
t_{SET}	Settling Time from $\overline{CE}$ to Stable f_C ($f_C = 3200$)(3)		6		msec

1.) Filter Response Referenced to $f = 1{,}920$Hz

2.) The tables are based on common TV crystal. See paragraph on "Clock Frequencies" for more detail.

3.) $t_{SET} = \frac{10{,}000}{f_c} + 3\text{msec}$

Pin Function Description

Pin Name	Number	Function
V_{DD}	6	Positive supply voltage pin. Normally $+5V \pm 10\%$.
V_{SS}	5	Negative supply voltage pin. Normally $-5V \pm 10\%$.
A_{GND}	11	Analog ground reference point for analog input and output signals. Normally connected to ground.
D_{GND}	15	Digital ground reference point for digital input signals. Normally connected to ground.
D_0	3	Control word Inputs: The set of six bits allows selection of one of sixty-four cutoff frequencies. The 6 bit control word is latched on the rising edge of $\overline{CE}$. The high-impedance inputs may be bridged directly across a microprocessor data bus.
D_1	2	
D_2	1	
D_3	18	
D_4	17	
D_5	16	
$\overline{CE}$	4	$\overline{\text{Chip Enable}}$: This pin has 3 states. When $\overline{CE}$ is at V_{DD} the data in the latch is presented to the ROM and the inputs have no effect. When $\overline{CE}$ is at ground the data presented on the inputs is read into the latch but the previous data is still in the ROM. Returning $\overline{CE}$ to V_{DD} presents the new data to the ROM and f_C changes. When $\overline{CE}$ is at V_{SS} the inputs go directly to the ROM, changing f_C immediately. This is the configuration for a fixed filter; $\overline{CE}$ is at V_{SS} and the D_0 through D_5 are tied to V_{DD} or V_{SS} depending on the desired f_C.
OSC_I, OSC_O	13, 14	Oscillator In and Oscillator Out: Placing a crystal and a 10MΩ resistor across these pins creates the time base oscillator. An inexpensive choice is to use the 3.58MHz TV colorburst crystal.
SIG(IN)	12	Signal Input: This is the inverting input of the input op amp. The non-inverting input is internally connected to Analog Ground.
FB	10	Feedback: This is the feedback point for the input op amp. The feedback resistor should be ⩾10kΩ for proper operation.
FLT(OUT)	9	Filter Out: This is the high impedance output of the programmable low pass filter. Loads must be ⩾10kΩ.
BUFF(IN)	8	Buffer Input: The inverting input of the buffer amplifier.
BUFF(OUT)	7	Buffer Out: The buffer amplifier output to drive low impedance loads. This pin may drive as low as 600Ω loads.

Example of Circuit Connection for S3528

Figure 1. Stand Alone Operation

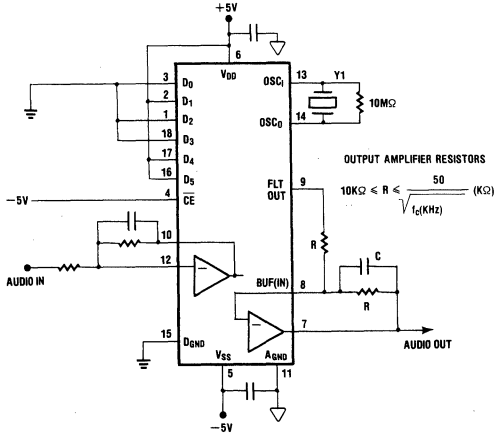
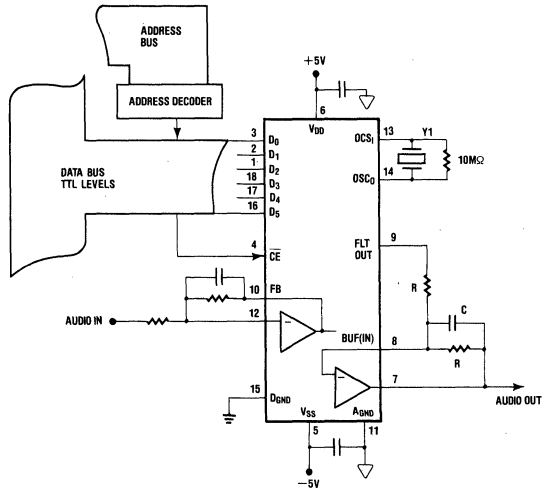


Figure 2. Microprocessor Interface



Operation

S3528 Filter is a CMOS Switched Capacitor Filter device designed to provide a very accurate, very flat, programmable filter that can be used in fixed applications where only one cutoff frequency is used, or in dynamic applications where logic or a microprocessor can select any one of 64 different cutoff frequencies. It is normally clocked by an inexpensive TV color burst crystal and provides the cutoff frequencies seen in Table 1 when the Data Bus pins are programmed.

All that is required for fixed operation is a 10MΩ resistor, the 3.58MHz TV crystal, and some resistors and capacitors around the input and output amplifiers to set the gain, anti-aliasing, and smoothing. The Data Bus pins are programmed from the table to either +5V (1) or ground (0) for the desired cutoff frequency. The $\overline{CE}$ pin is tied low, to V_{SS}.

The ROM is addressed by the contents of the latch and presents an 11-bit word to the programmable divider which divides f_{osc}, the oscillator frequency, down to the filter clock frequency.

The filter is designed to provide a cutoff frequency of one-fortieth of the clock frequency. Using the 3200Hz cutoff frequency as an example, the input pins would be set to 110010_2 (32_{16}). The ROM would output a code causing the divider to divide by 28, so 3.579545MHz ÷ 28 = 127.840kHz. Dividing the filter clock by 40 gives an fc or cutoff frequency of 3196Hz.

The FILTER OUT pin is capable of driving a 10kΩ load directly or, for smoothing and driving a 600Ω load, the output buffer amplifier can be used for impedance matching.

As illustrated in the curves of Figures 3, and 5 through 7, the passband ripple (for fc<18kHz) is less than ±0.1dB and the stop band rejection is better than 50dB as measured on a Hewlett-Packard Network Analyzer.

For microprocessor controlled operation, the Data Bus can be bridged across a regular TTL bus and when $\overline{CE}$ is strobed, the data present will be latched in and the filter will settle down to its new cutoff frequency. In CMOS systems, the Data Bus and $\overline{CE}$ can be swung rail-to-rail. A_{GND} and D_{GND} must be at ½ the supply voltage.

The following tables illustrate the available cutoff frequencies based on using a 3.58MHz TV crystal for a time base. Table 1.0 lists the frequencies by approx-

Figure 3. Family of Loss Curves

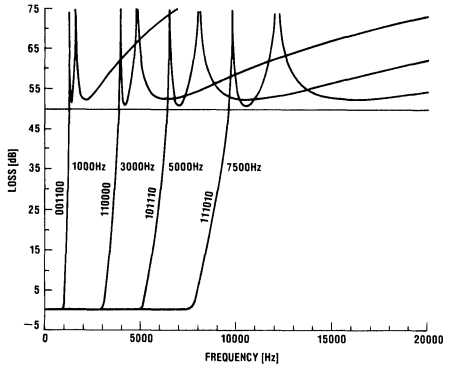


Figure 4. Address and Chip Enable Timing

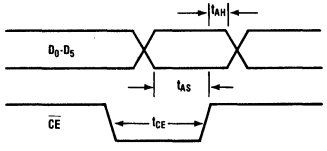


Figure 5. Loss Curve, Control = 110010, f_c = 3200Hz

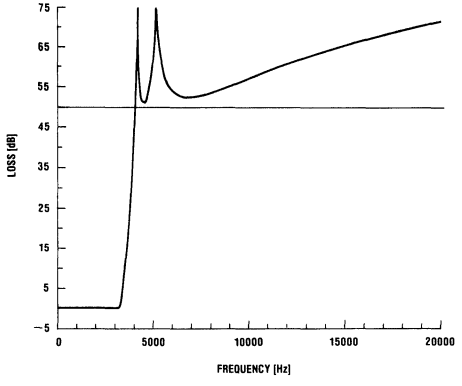


Figure 6. Passband Control Detail, Control = 110010, f_c = 3200Hz

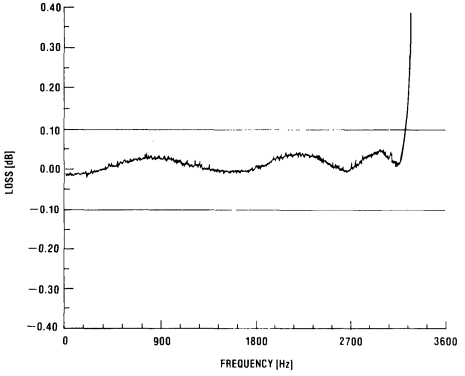
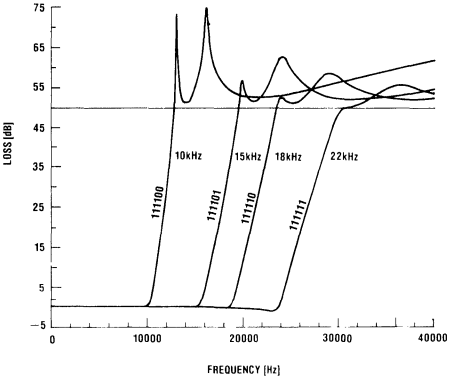


Figure 7. Family of Loss Curves



imately 100Hz steps through the voice band from 100Hz to 3900Hz. Note that the hex input code for each frequency in the voice band is one-hundredth of the cutoff frequency. For 3200Hz, the hex code is 32, for 900Hz it is 09. Additional frequencies are listed with their codes on the right side of the Table 1.0. Table 1.1 lists the cutoff frequencies in ascending order with the corresponding hex coded inputs. Note that the 18kHz and 22kHz cutoffs do not meet the ripple specs but still provide excellent filtering. See Figure 7.

Table 1.0—Standard Frequency Table: Programmable Filter S3528. f_{osc} = 3.58MHz

Voice Bandx100Hz Steps

fc (Hz)	Input Code (HEX) D_5-D_0	Divider Ratio	fc Actual (Hz)
40	00	2048	44
100	01	895	100
200	02	447	200
300	03	298	300
400	04	224	399
500	05	179	500
600	06	149	601
700	07	128	699
800	08	112	799
900	09	99	904
1000	10	89	1005
1100	11	81	1105
1200	12	74	1209
1300	13	69	1297
1400	14	64	1398
1500	15	60	1491
1600	16	56	1598
1700	17	53	1688
1800	18	50	1790
1900	19	47	1904
2000	20	45	1989
2100	21	43	2081
2200	22	41	2183
2300	23	39	2295
2400	24	37	2418
2500	25	36	2686
2600	26	34	2632
2700	27	33	2711
2800	28	32	2797
2900	29	31	2887
3000	30	30	2983
3100	31	29	3086
3200	32	28	3196
3300	33	27	3314
3400	34	26	3442
3600	36	25	3579
3700	37	24	3728
3900	39	23	3891

Additional Points Available

fc (Hz)	Input Code (HEX) D_5-D_0	Divider Ratio	fc Actual (Hz)
475	0A	188	476
250	0B	358	250
1000	0C	90	994
1030	0D	87	1028
1050	0E	85	1053
1150	0F	78	1147
1470	1A	61	1467
1540	1B	58	1542
1720	1C	52	1721
1950	1D	46	1945
2030	1E	44	2034
2240	1F	40	2237
2350	2A	38	2350
2560	2B	35	2557
4000	2C	22	4067
4470	2D	20	4474
5000	2E	18	4971
5600	2F	16	5593
6000	35	15	5965
6400	38	14	6392
7500	3A	12	7457
9000	3B	10	8949
10000	3C	9	9943
15000	3D	6	14915
18000	3E	5	17897
22000	3F	4	22372

Table 1.1—Standard Frequency Table: Programmable Filter S3528

Frequencies Listed in Ascending Order

fc (Hz)	Input Code (HEX) D_5-D_0	Divider Ratio	fc Actual (Hz)
40	00	2048	44
100	01	895	100
200	02	447	200
250	0B	358	250
300	03	298	300
400	04	224	399
475	0A	188	476
500	05	179	500
600	06	149	601
700	07	128	699
800	08	112	799
900	09	99	904
1000	0C	90	994
1000	10	89	1005
1030	0D	87	1028
1050	0E	85	1053
1100	11	81	1105
1150	0F	78	1147
1200	12	74	1209
1300	13	69	1297
1400	14	64	1398
1470	1A	61	1467
1500	15	60	1491
1540	1B	58	1542
1600	16	56	1598
1700	17	53	1688
1720	1C	52	1721
1800	18	50	1790
1900	19	47	1904
1950	1D	46	1945
2000	20	45	1989
2030	1E	44	2034
2100	21	43	2081
2200	22	41	2183
2240	1F	40	2237
2300	23	39	2295
2350	2A	38	2350
2400	24	37	2418
2500	25	36	2686
2560	2B	35	2557
2600	26	34	2632
2700	27	33	2711
2800	28	32	2797
2900	29	31	2887
3000	30	30	2983
3100	31	29	3086
3200	32	28	3196
3300	33	27	3314
3400	34	26	3442
3600	36	25	3579
3700	37	24	3728
3900	39	23	3891
4000	2C	22	4067
4470	2D	20	4474
5000	2E	18	4971
5600	2F	16	5593
6000	35	15	5965
6400	38	14	6392
7500	3A	12	7457
9000	3B	10	8949
10000	3C	9	9943
15000	3D	6	14915
18000	3E	5	17897
22000	3F	4	22372

NOTE: The S3528 cutoff frequency steps may be custom selected.

Table 2.0—Standard Frequency Table: Programmable Filter S3528A. f_{osc} = 3.58MHz

Input Code D_5–D_0	f_c Actual (Hz)	Divider Ratio
000000	389.1	230
000001	403.1	222
000010	420.1	213
000011	434.4	206
000100	452.0	198
000101	468.5	191
000110	486.4	184
000111	505.6	177
001000	523.3	171
001001	545.7	164
001010	566.4	158
001011	584.9	153
001100	608.8	147
001101	630.2	142
001110	653.2	137
001111	677.9	132
010000	704.6	127
010001	733.5	122
010010	758.4	118
010011	791.9	113
010100	821.0	109
010101	852.3	105
010110	886.0	101
010111	913.1	98
011000	952.0	94
011001	983.4	91
011010	1028.6	87
011011	1065.3	84
011100	1104.8	81
011101	1147.3	78
011110	1193.2	75
011111	1242.9	72

Input Code D_5–D_0	f_c Actual (Hz)	Divider Ratio
100000	1278.4	70
100001	1335.7	67
100010	1376.7	65
100011	1443.4	62
100100	1491.5	60
100101	1542.9	58
100110	1598.0	56
100111	1657.2	54
101000	1720.9	52
101001	1789.8	50
101010	1864.3	48
101011	1945.4	46
101100	1988.6	45
101101	2081.1	43
101110	2182.6	41
101111	2237.2	40
110000	2355.0	38
110001	2418.6	37
110010	2485.8	36
110011	2632.0	34
110100	2711.8	33
110101	2796.5	32
110110	2886.7	31
110111	2983.0	30
111000	3085.8	29
111001	3196.0	28
111010	3314.4	27
111011	3441.9	26
111100	3579.5	25
111101	3728.7	24
111110	3890.8	23
111111	4067.7	22

NOTE: Frequency steps for S3528A are different than for S3528. Either option is available as a standard product.

Applications Information

Many filter applications can benefit from the S3528, particularly if extremely flat passband response with precise, repeatable cutoff frequencies are required. Or, if the same performance is required at different frequencies it can be switch or microprocessor controlled. The circuits (Figures 1 and 2) illustrate how the S3528 might be connected for two different uses. The "stand alone" drawing (Figure 1) shows how it would be programmed as a fixed, 3200Hz low pass filter. The other drawing (Figure 2) shows a microprocessor driven application that lets the cutoff frequency be varied on command.

Some fields that can use such a filter are speech analysis and scrambling, geo-physical instrumentation, under water accoustical instrumentation, two-way radio, telecommunications, electronic music, remotely programmable test equipment, tracking filter, etc.

Anti-Aliasing

In planning an application the basic fundamentals of sampling devices must be considered. For example, aliasing must be taken into consideration. If a frequency close to the sampling frequency is presented to the input it can be aliased or folded back into the passband. Because the S3528 has an input cosine filter the effective sample frequency is twice the filter clock frequency of 40 times the cutoff frequency. If f_c = 1000Hz and a signal of 79,200Hz is put into the filter, it will alias the 80kHz effective sampling frequency of the input cosine filter and appear as an 800Hz signal at the output. This means that for some applications the input op amp must be used to construct a simple one or two pole RC anti-aliasing filter to insure performance. In many situations, however, this will not be necessary since the input signal will already be band-limited.

Smoothing

In addition, all sampling devices will have aliased components near the clock frequency in the output. For example, there will be small components at $f_{clk} \pm f_{in}$ in the output waveform. This can be reduced by constructing a simple smoothing filter around the output buffer amplifier. Because of the sinx/x characteristics of a sample and hold stage the aliasing components are already better than 30dB down. The clock feed through is approximately −50dBV. This means that a simple one pole filter can provide another 20dB of rejection to keep the aliasing below 50dB down. In the case of a 3kHz fc and the smoothing filter designed for a 3dB point at 4fc the smoothing filter will affect the 3kHz point by .25dB. If this is not desirable then the smoothing filter might be constructed as a second order filter.

For a fixed application, anti-aliasing and smoothing are straight forward. For a dynamic operation, the desired operating range of frequencies must be considered carefully. It may be necessary to switch in or out additional components in the RC filters to move cutoff frequencies. The S3528 has a ratio of cutoff frequencies of 550:1 and to use the full range would require some switching. The S3528A has a narrower range of 10:1.

Notch Rejection

The filter is designed to have 51dB of rejection at 1.3fc and greater. If greater rejection of a specific tone or signal frequency is desired, the cutoff frequency can be selected to position the undesired tone at 1.325fc or 1.62fc. This will place it in a notch as illustrated in Figure 5.

Clock Frequencies

Although the tables are constructed around the TV colorburst crystal, other clock frequencies can be used from crystals or external clocks to achieve any cutoff frequency in the operating range. For example, by using a rate multiplier and duty-cycle restorer circuit between the system clock and the S3528, and switching the inputs to the S3528, almost any cutoff frequency between 40Hz and 22kHz can be selected. The clock input frequency can be anywhere between 500kHz and 5MHz.

In addition to crystals or external clocks the S3528 can be used with ceramic resonators such as the Murata CSA series "Ceralock" devices. All that is required is the resonator and 2 capacitors to V_{SS}. Although the resonators are not quite as accurate as crystals they can be less expensive.

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Advanced Product Description **S3530**

BELL 103/V.21 SINGLE CHIP MODEM

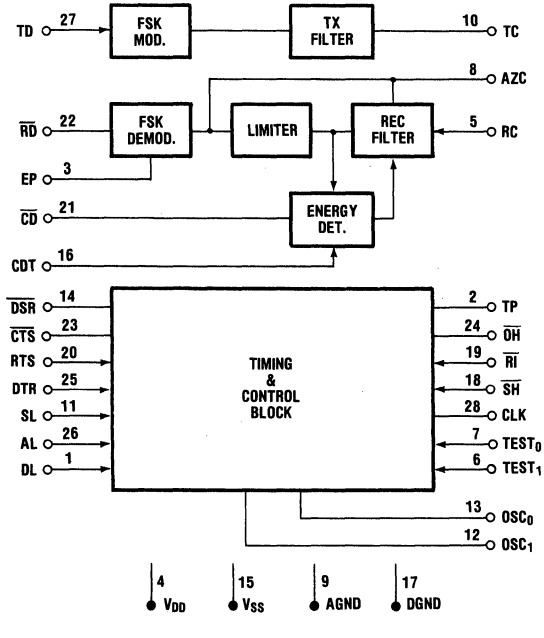
Features

- ☐ Single-Chip 300 bps, Full Duplex, Asynchronous FSK Modem
- ☐ Bell 103/113 & CCITT V.21 Operation (Selectable)
- ☐ Auto Answer/Originate Operating Modes
- ☐ No External Filtering Required
- ☐ Phase Continuous Transmit Carrier Frequency Switching
- ☐ RS-232 Control Interface
- ☐ Low Cost 3.58MHz (TV Crystal) Time Base
- ☐ Digital & Analog Loopback Modes
- ☐ UART Clock Output (4.8KHz)
- ☐ V25 Tone Generation
- ☐ Low Power CMOS Technology

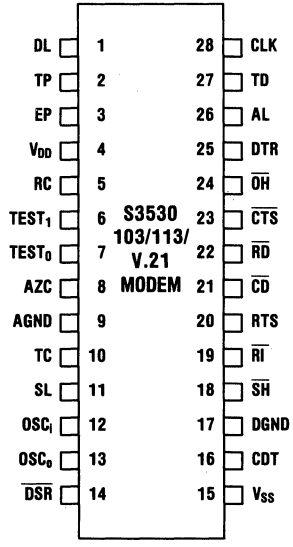
General Description

The S3530 is a Single-Chip 300 bps Full Duplex FSK Modem which may be operated in Bell 103/113 or CCITT V.21 applications. The S3530 features on-chip transmit and receive filtering; answer/originate mode selection; RS-232 control interface; digital and analog loopback test modes; and generation of both the 4.8KHz UART clock and V.25 Answer Tone. The S3530 is designed for use in stand-alone modem applications and in applications in which the modem function is designed directly into the DTE.

Block Diagram



Pin Configuration



Pin/Function Descriptions

Pin #	Name	Function
25	DTR (Data Terminal Ready)	A high level on this input enables all the other inputs and outputs and must be present before the device will enter the data mode either manually or automatically. The device will enter an irreversible disconnect sequence if the input is turned off (low level) for more than 13.33 mSec during a data call. A pulse duration of less than 6.67 mSec will not be detected.
20	RTS (Request to Send)	A high level on this input with the DTR input in the on condition causes the device to enter the originate mode. OH output goes to low level to seize the phone line. Auto dialing can be performed by turning the RTS input on and off to effect dial pulsing. This input must remain high for the duration of data transmission.
23	$\overline{\text{CTS}}$ (Clear to Send)	This output goes to a low level at the completion of the handshaking sequence and turns off when the modem disconnects. It is always turned off if the device is in the digital loop mode. Data to be transmitted should not be applied at the TD input until this output turns on.
21	$\overline{\text{CD}}$ ($\overline{\text{Carrier Detect}}$)	This output goes to a low level to indicate that the receive data carrier has been received at a level of at least −43dBm. It turns off if the received data carrier falls below the carrier detection threshold (−48dBm). During the off state, the receive data is clamped to the marking state (high level). Refer to Table 2 for timing requirements.
27	TD (Transmit Data)	Data bits to be transmitted are presented to this input serially by the data terminal. A high level is considered a binary '1' or MARK and a low level is considered a binary '0' or SPACE. The data terminal should hold this input in the marking state when data is not being transmitted. During handshaking phase external control is not required.
22	$\overline{\text{RD}}$ ($\overline{\text{Received Data}}$)	The device presents data bits demodulated from the received data carrier at this output. This output is forced to the marking state (high level) if the DTR input or the carrier detect output is off.
14	$\overline{\text{DSR}}$	This output, when high, indicates to the data terminal that the modem is not ready to transmit data.
19	$\overline{\text{RI}}$ ($\overline{\text{Ring Indicator}}$)	This input when high permits auto answer capability. The data access arrangement should apply a low level when a ringing signal is detected. The level should be low for at least 107msec. The input can remain low until reset by DTR or loss of carrier. In manual mode the answer mode can be entered by applying a low level to this input.
26	AL (Analog Loopback)	This input allows the data terminal to electronically make the telephone line appear busy (off hook) and implement the analog loopback mode. A high level on this input while DTR is high causes the device to make the $\overline{\text{OH}}$ output low and to enter the analog loopback mode. In the loopback mode, the receive filter center frequency is switched to correspond to the transmit filter center frequency and the transmit data carrier output is internally connected to the receive data carrier input.
11	SL (Select)	A high level on this input selects the CCITT V.21 data transmission format. Applying a low level selects the Bell 103 data transmission format.
16	CDT (Carrier Detect Threshold)	Applying a variable voltage level at this pin allows control of the receiver carrier detection threshold. This will override the internally determined threshold.
28	CLK (Clock)	A 4.8kHz TTL compatible square wave output is present at this output and is provided for supplying the 16X clock signal required by a UART for 300 bits/sec. data rate. This output facilitates the integration of the modem function within the data terminal.

Pin/Function Descriptions (Continued)

Pin #	Name	Function
24	$\overline{OH}$ (Off-Hook)	This output goes to a low level when either the $\overline{SH}$ or the RTS input is on in the originate mode and when a valid ring signal is detected on the $\overline{RI}$ input in the answer mode. This output is off if DTR is off or if the disconnect sequence has been completed.
10	TC (Transmit Carrier)	This analog output is the modulated transmit data carrier. Its frequency depends upon whether the modem is in the answer or originate mode and if a mark or space condition is being sent (Table 1). Typically, the output level is at −9dBm. This output is turned on only during data transmission and handshaking intervals.
7 6	Test 0 Test 1	These are test inputs. In normal operation these should be connected to V_{SS}. These inputs are used to reconfigure internal blocks so that they may be tested.
5	RC (Receive Carrier)	This analog input is the data carrier received by the data access arrangement. The modem demodulates this signal to generate the receive data bits.
17	DGND (Digital Ground)	Digital signal ground pin.
9	AGND (Analog Ground)	Analog signal ground pin (for transmitted and received carrier).
8	AZC	Connection terminal for external 0.1μF auto-zero capacitor.
4,15	V_{DD}, V_{SS}	Positive and negative power supply pins (±5V).
18	$\overline{SH}$ (Switch Hook)	This input is used to manually place the device in the originate mode. The device will make the $\overline{OH}$ output low and start the originate sequence if $\overline{SH}$ input is low and DTR is on. This can be a level or a momentary low going pulse input (min. 53.67 mS). A pulse duration of less than 26.67 mS will not be detected.
13,12	OSC_0, OSC_I	These are connection terminals for connecting an external 3.579545MHz TV crystal. All internal clock signals are derived from this time base. An external clock signal may also be applied at the OSC_I input. Feedback resistor and capacitors required to make the circuit oscillate are all integrated on the chip.
1	DL (Digital Loopback)	A high level on this input causes the device to enter the digital loopback mode. In this mode, the received data from the remote end is internally looped-back to transmit data.
2	TP (Test Point)	I/O pin which is used in conjunction with $Test_0$ and $Test_I$ control pins for testing the S3530 in manufacture.
3	EP (Eye Pattern)	Output (analog) of the demodulator prior to slicing.

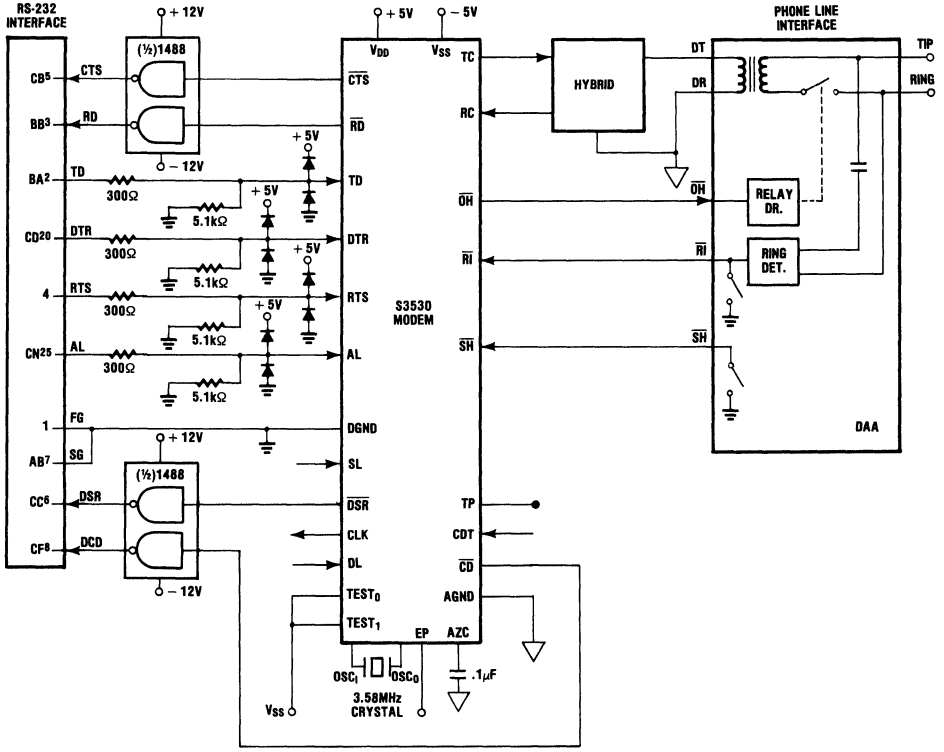
Table 1. 103/V.21 Mark and Space Frequencies

Mode	Transmit Frequency (Hz)		Receive Frequency (Hz)	
	Mark	Space	Mark	Space
103 Originate	1270	1070	2225	2025
103 Answer	2225	2025	1270	1070
V.21 Originate	980	1180	1650	1850
V.21 Answer	1650	1850	980	1180

Table 2. Nominal Timing for Carrier Detection

Standard	Transition (mS)	
	Off-To-On	On-To-Off
103	106.67	6.67
V.21	426.67	20

Figure 1. Answer/Originate Full Duplex 300 Baud Modem



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Consumer Products

Contact factory for complete data sheets

Consumer Products Selection Guide

SPEECH PRODUCTS

Part No.	Description	Process	Power Supplies	Packages
S3610	Speech Synthesizer	CMOS	+ 5V	24 Pin
S3620	Speech Synthesizer	CMOS	+ 5V	22 Pin

DRIVERS

Part No.	Description	Process	Power Supply	Outputs	Packages
S2809	Universal Driver	PMOS	+ 8V to + 22V	32	40 Pin
S4535	32 Bit, High Voltage, Driver	CMOS	+ 5V	32	40 Pin
S4534	10 Bit, High Voltage, High Current Driver	CMOS	+ 5V	10	18 Pin
S4521	32 Bit Driver	CMOS	+ 5V	32	40 Pin

REMOTE CONTROL CIRCUITS

Part No.	Description	Process	Power Supply	Commands	Packages
S2600	Remote Control Encoder	CMOS	+ 7V to 10V	31	16 Pin
S2601	Remote Control Decoder	PMOS	+ 10V to 18V	31	22 Pin
S2602	Remote Control Encoder	CMOS	+ 9V	18	16 Pin
S2603	Remote Control Decoder	PMOS	+ 9V	18	22 Pin
S2604	Remote Control Encoder	CMOS	+ 9V	18	16 Pin
S2605	Remote Control Decoder	CMOS	+ 9V	18	22 Pin
S2742	Remote Control Decoder	PMOS	+ 15V	512	18 Pin
S2743	Remote Control Encoder	PMOS	+ 9V	512	16 Pin
S2747	Remote Control Encoder	CMOS	+ 9V	512	16 Pin
S2748	Remote Control Decoder	CMOS	+ 12V	512	16 Pin

ORGAN CIRCUITS

Part No.	Description	Process	Packages
S10110	Analog Shift Register	PMOS	8 Pin
S10131	Six-Stage Frequency Divider	PMOS	14 Pin
S10430	Divider-Keyer	PMOS	40 Pin
S2567	Rhythm Counter	PMOS	16 Pin
S2688	Noise Generator	PMOS	8 Pin
S50240	Top Octave Synthesizer	PMOS	16 Pin
S50241	Top Octave Synthesizer	PMOS	16 Pin
S50242	Top Octave Synthesizer	PMOS	16 Pin

CLOCK CIRCUITS

Part No.	Description	Process	Power Supply	Digits	Packages
S4003	Fluorescent Automotive Digital Clock (12 Hour + Date + Rally Timer)	PMOS	+ 12V	4	40 Pin
S2709A	Vacuum Fluorescent Digital Clock	PMOS	+ 12V	4	22 Pin

A/D CONVERTER AND DIGITAL SCALE CIRCUIT

Part No.	Description	Process	Power Supply	Digits	Packages
S4036	General Purpose A/D Converter and Digital Scale Circuit	CMOS	+ 9V	4	24 Pin

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S3610

LPC-10 SPEECH SYNTHESIZER WITH ON-CHIP 20K SPEECH DATA ROM

CONSUMER PRODUCTS

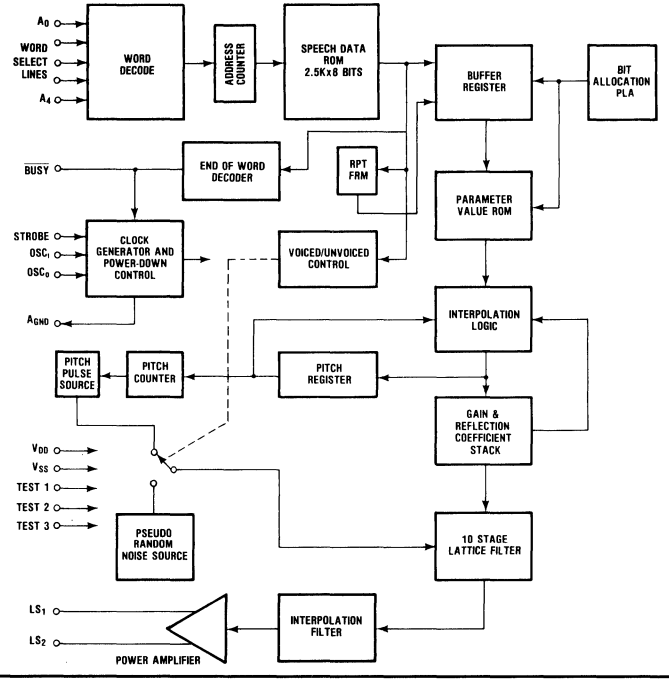
Features

- ☐ Simple Digital Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ 5-8 Volts Single Power Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 20mW Audio Output
- ☐ 20K Bits Speech ROM
- ☐ Low Data Rate
- ☐ Up to 32 Word Vocabulary

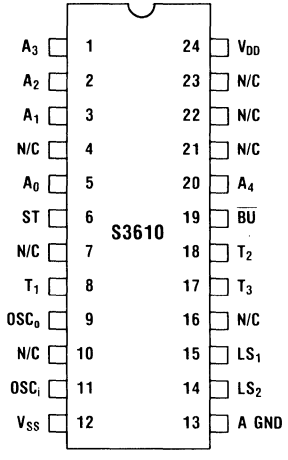
General Description

The S3610 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an internal 20K bit ROM. The simple digital interface consists of 5 word-select lines, a strobe input to load the address data and initiate operation, and a busy output signal. At the end of enunciation the chip automatically goes into the powerdown mode until a new word select address is strobed in. The data rate from the speech ROM into the synthesizer is 2.0K bits/sec max. Typically the average data rate will be reduced to about 1.2K bits/sec. by means of the data rate reduction techniques used internally, giving about 17 seconds of

Block Diagram



Pin Configuration



N/C = NO CONNECTION

speech from the ROM data. The 5 word-select lines allow a maximum vocabulary of 32 words.

The synthesizer is realized using analog switched-capacitor filter technology and operates at 8K samples/sec. An output interpolating filter and bridge power amplifier give 20mW output power at 5 volts supply and allow the device to be connected directly to a 100Ω loudspeaker.

The S3610 also features an on-chip oscillator, requiring only a 640kHz ceramic resonator and a capacitor for normal operation.

AMI is able to provide a speech analysis service to generate the LPC parameters from customers' word lists.

Absolute Maximum Ratings*

Supply Voltage	11 Volts DC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Voltage at any Pin	V_{SS} −0.3 to V_{DD} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications: (V_{DD} = 5.0V ± 10%, V_{SS} = 0V, C_{AG} = 0.047μF, T_A = 0° to 70°C, unless otherwise specified)

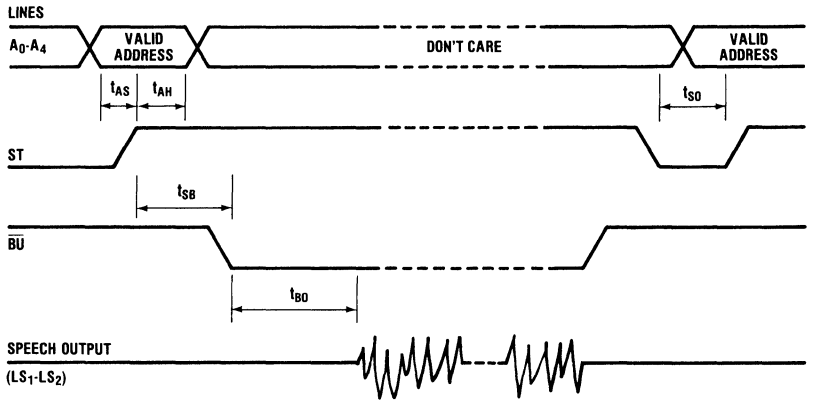
D.C. Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.4		V_{DD}	V	
V_{IL}	Input Low Logic "0" Voltage	0		0.8	V	
I_{IN}	Input Leakage Current			10	μA	V_{IN} = 0 to V_{DD}
V_{OL}	Output Low Voltage ($\overline{BU}$)			0.4	V	I_{OL} = 1.6mA
V_{OS}	DC Offset Voltage, Audio Output		$0.5V_{DD}$		V	R_{LOAD} = 100Ω
I_{DD}	Supply Current, Operating			35	mA	
I_{DDL}	Supply Current, Powerdown			4	mA	

AC Characteristics

P_O	Audio Output Power		20		mW	R_{LOAD} = 100Ω
t_{AS}	Address Set-up Time	200			nsec	See Figure 1
t_{AH}	Address Hold Time	10			nsec	See Figure 1
t_{SO}	Strobe Off Width	3.2			μsec	See Figure 1
t_{SB}	Strobe to Busy Delay		100	500	nsec	See Figure 1
t_{BO}	Busy to Speech Output Delay		19		msec	See Figure 1
F_{OSC}	Oscillator Resonator Frequency	−1%	640	+1%	KHz	
R_{LOAD}	Audio Output Load Impedance		100		Ω	
C_{INOSC}	Input Capacitance, Oscillator		100		pF	
C_{IN}	Input Capacitance, Digital Interface		7		pF	

Figure 1. Timing Requirements



Pin Function/Description

A_0 through A_4	**Word Select Inputs.** The 5-bit address data on these lines selects the word to be enunciated from the internal vocabulary.
ST	**Strobe Input.** A rising edge on this line strobes in the word select data and causes enunciation to commence. If this line is taken low prior to the end of enunciation (as indicated by the busy signal), enunciation stops immediately and the chip goes into power down mode.
$\overline{BU}$	**Busy Output.** This open drain output signals that enunciation is in progress by going low.
LS1 and 2	**Loudspeaker Outputs.** These pins are used to connect the chip to the loudspeaker. They are D.C. coupled and have an offset of half the supply voltage. The audio output is balanced on the two outputs.
OSC_i, OSC_0	**Oscillator Input and Output.** A 640KHz ceramic resonator (MuRata CSB640A or equivalent) should be connected between these pins for normal operation, or an external 640KHz signal may be fed into OSC_i. When a resonator is used, a 120pF capacitor should be connected between OSC_i input and ground.
T_1, T_2, T_3	**Test Inputs and Outputs.** These inputs should be left unconnected for normal operation.
V_{SS}	Most negative supply input. Normally connected to 0V.
V_{DD}	Most positive supply input.
A_{GND}	**Analog Ground.** An internally generated level approximately half way between V_{SS} and V_{DD}. A 0.047μF decoupling capacitor C_{AG} should be connected from this pin to V_{SS}. Do not connect this pin to a voltage supply.

Circuit Description

The main components of the S3610 LPC-10 Speech Synthesizer are shown in the block diagram.

Word Decode ROM—This ROM decodes the data presented on the word select lines into the start addresses of the speech words as stored in the Speech Data ROM. Up to 32 twelve bit start addresses may be programmed into this ROM. When the strobe line is taken high the start address selected is used to preset the Address Counter.

Address Counter—This binary counter is used to address the Speech Data ROM. After being preset to the desired start address it is incremented each time a new byte of data is required for the synthesizer.

Speech Data ROM—This ROM contains the 2.5K (2560) bytes of LPC-10 parameters encoded into a non-linearly quantized packed format. This format allows each frame of LPC parameters to be stored in only 5 bytes or less and is shown in Figure 2.

End of Word Decoder—This circuit detects the special code indicating that the last byte read from the Speech Data ROM denotes the end of the speech word data and initiates the power down routine after the previous frame has been enunciated.

Buffer Registers—The data from the Speech Data ROM is assembled into frames and then decimated into the 12 parameters required for LPC-10 synthesis: pitch, gain and the 10 lattice filter coefficients. The parameters are stored in an encoded format and the decoding is done in the Parameter Value ROM. The coefficient address registers are used to store the assembled frame data and address this ROM.

Bit Allocation PLA—A programmable logic array is used to control the allocation of bits in the Buffer Register to the 12 parameters. The allocation and permissible variations are shown in Figure 2.

Parameter Value ROM—This ROM is used as a look-up table to decode the stored parameters into the LPC coefficients.

Interpolation Logic—The coefficients for each frame of speech, normally 20msec. are interpolated four times per frame to generate smoother and more natural sounding speech. Hence, the interpolation period is one quarter of a frame period, normally 5msec. After interpolation, the coefficients are used to drive the pitch-pulse source, the lattice filter and the gain control. Interpolation is inhibited when a change from voiced to unvoiced speech, or vice versa, is made.

Pitch Register and Counter—This register stores the pitch parameter used to control the pitch counter.

Pitch-pulse Source—This is the signal source for voiced speech (vowel sounds). It is realized in switched-capacitor technology and generates symmetrical bipolar pulses at the rate specified by the pitch parameter and controlled by the pitch counter.

Pseudo-random Noise Source—This is the signal source for unvoiced speech (fricatives and sibilants) and consists of a 15-bit linear code generator giving a periodicity of 32767 sampling periods (4.096sec.). The output of this generator is scaled to a lower value and used as a random sign, constant amplitude signal.

Voiced/Unvoiced Speech Selector Switch—This switch determines whether the voiced or unvoiced signal source is used to drive the filter during a given frame.

LPC-10 Parameter Stack—This stack of 10 filter coefficients is used to control the lattice filter. The coefficients have an accuracy of 8-bits plus sign.

10 Stage Lattice Filter—The filter which simulates the effect of the vocal tract on the sound source (glottis) in the human speaker is realized here as a switched-capacitor (analog sampled data) 10 stage lattice filter. The filter parameters are determined dynamically by the time varying coefficients in the Parameter Stack and the filter operates at a sampling frequency of 8KHz (clock frequency/80).

Gain Controller—This controls the input signal level to the lattice filter to vary the sound level, and is an integral part of the lattice filter.

Interpolation Filter—The output signal from the lattice filter is sampled at 8KHz, and consequently its spectrum is rich in aliasing (foldover) distortion components above 4KHz (See Figure 3). The signal is cleaned up by passing it through a 4KHz low pass filter sampled at 160KHz. The spectrum of the output signal contains no aliasing distortion components below 156KHz, making the output suitable for feeding directly into a loudspeaker after amplification. This filter is also realized using switched-capacitor filter technology.

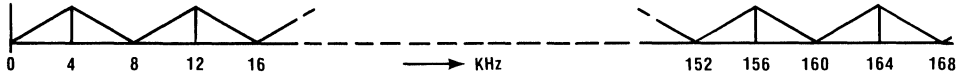
Power Amplifier—The amplifier brings up the level of the signal to give an output level of 20mW RMS into 100Ω load. The output is a balanced bridge configuration with anti-phase signals on the 2 output pins.

Figure 2. Packed Quantized Data Formats

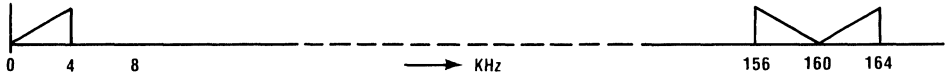
	BYTE 5								BYTE 4								BYTE 3								BYTE 2								BYTE 1							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
VOICED	← PITCH →								← K10,K9,K8,K7,K6,K5 →								← K4,K3, K2, K1 →										V/UV	REPT	← GAIN →									
UNVOICED	← NOT USED →																← K4,K3, K2, K1 →										V/UV	REPT	← GAIN →									
REPEAT	← NOT USED →																												← PITCH →				GAIN							REPT*
END OF WORD	← NOT USED →																								0	0	0	0	0	0	0	0								

*NOTE: 0 = SINGLE (OR LAST) REPEAT. 1 = MULTIPLE REPEAT.

Figure 3.



(a) SPECTRUM OF SIGNAL OUTPUT OF LATTICE FILTER



(b) SPECTRUM OF SIGNAL AT OUTPUT OF INTERPOLATION FILTER.
NOTE: IN BOTH CASES A SIN x/x CHARACTERISTIC MODULATES THE SPECTRA. THIS IS OMITTED FOR SIMPLICITY.

Clock Generators and Power-down Control—This block contains the oscillator and timing circuits and also generates the analog ground reference voltage.

Speech Data Compression

The speech data rate of the synthesizer is reduced to less than 2000 bits/sec for storage by means of a non-linear quantization technique. Each of the 12 coefficients is constrained to have a fixed set of values in an optimized manner. The actual values are dependent on the speech data and generated automatically

in the analysis process. The parameters used to specify the coefficients are stored in the speech data ROM and used to address the coefficient look-up table ROM. The packing formats for the speech data are shown in Figure 2.

The speech data rate is further reduced by two other techniques shown in Figure 2. A substantial reduction is achieved by reducing the order of the lattice filter (the LPC order) to 4 during periods of unvoiced speech. This allows a 40% data reduction during these periods, which themselves typically account for 30-40% of speech (in the English language). A second reduction is obtained by detecting periods during which the filter parameters may be the same as those in the previous frame. Only the gain and pitch parameters are updated in such a frame, allowing an 80% data reduction. Note that in repeat frame only 3 bits are allocated to the gain parameter. The LSB is forced internally to zero.

Programming the S3610

The word decode ROM, the speech data ROM and the coefficient ROM are mask programmed with the customer's speech data. Interfacing with AMI to produce the ROM mask is possible at several levels, to suit the customer's requirements. AMI is able to provide a complete speech analysis service for this purpose. Customers who have LPC speech analysis facilities and wish to interface with AMI at a different level should contact the factory for further details about the quantization technique and formats acceptable.

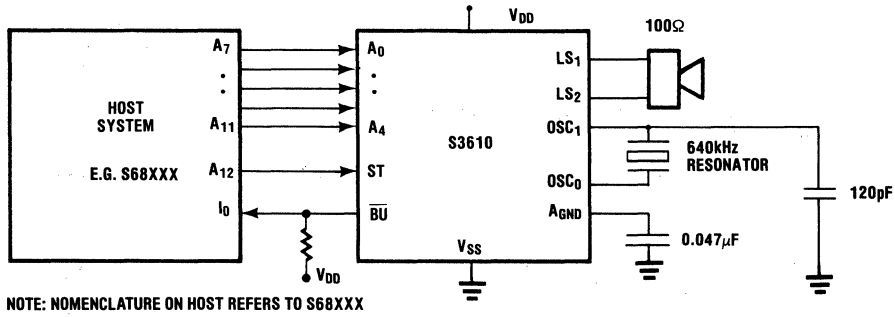
Interfacing

The S3610 is designed to be easily interfaced to a host controller. The interface timing requirements are shown in Figure 1. A valid 5-bit address (i.e., word number) should be presented on the word select lines and the strobe line taken to a logic 1 and held there until the end of enunciation, as indicated by the Busy output. A typical system configuration is shown in Figure 4. If it is not possible or inconvenient to monitor the Busy output or to maintain the strobe for the duration of the enunciation, these 2 lines may be combined as shown in Figure 5. The Busy output will automatically maintain the Strobe input once it is initiated. Note that an inverted strobe input is now required, and its duration should ensure that the Busy output goes low before it is removed. A minimum duration of 3.2μsec is recommended. A method of operating the synthesizer directly from a keyboard is shown in Figure 6. Using the 74C922 encoder limits the vocabulary to 16 words. This can be expanded to the maximum of 32 words by using 2 encoders. The R-C delay provides the address set-up time required before ST goes high.

Applications

Toys and Games
EDP
Instrumentation
Communications
Industrial Controls
Automotive
Appliances

Figure 4. Typical System Configuration



NOTE: NOMENCLATURE ON HOST REFERS TO S68XXX

Figure 5. Using Busy Output to Maintain Strobe

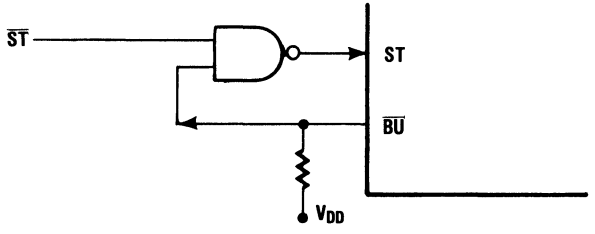
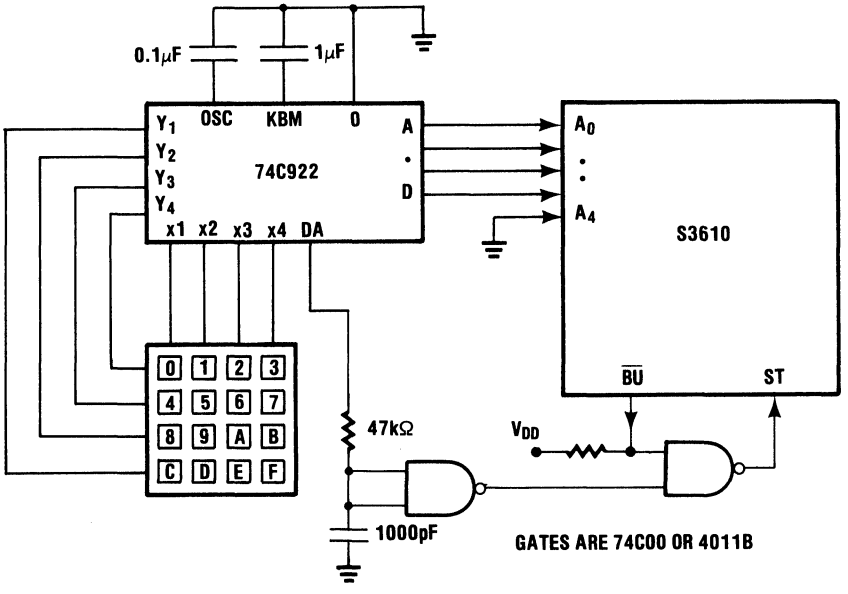


Figure 6. Direct Keyboard Operation



LPC-10
SPEECH SYNTHESIZER

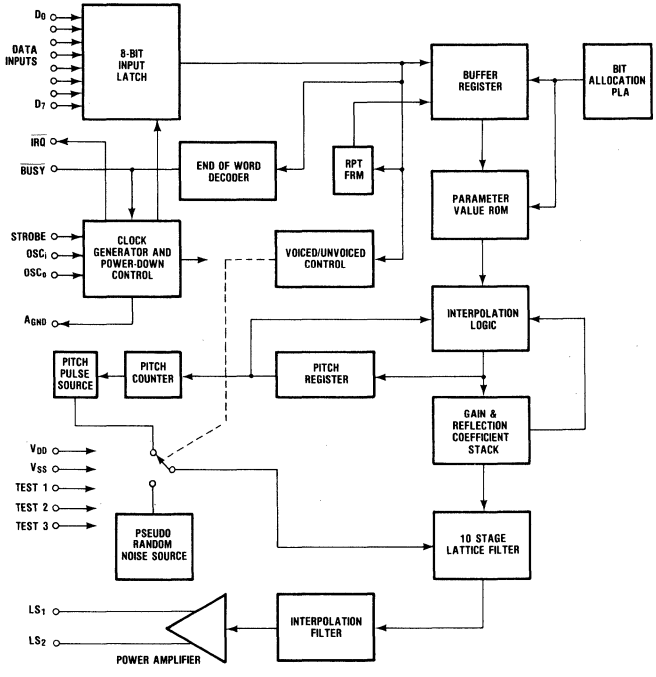
Features

- ☐ Simple Microprocessor Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ 5-8 Volts Single Power Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 20mW Audio Output
- ☐ Low Data Rate

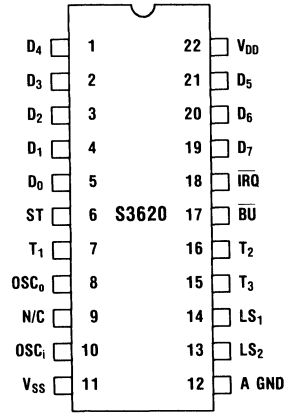
General Description

The S3620 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an external memory. The digital interface circuitry is fully microprocessor compatible and allows the processor to load the data with or without a DMA controller. The loading takes place on a handshake basis, and in the absence of a response from the processor the synthesizer automatically shuts down and goes into the powerdown mode. A busy signal allows the processor to sense the status of the synthesizer. The input data

Block Diagram



Pin Configuration



N/C = NO CONNECTION

rate is 2.0K bits/sec. max., but typically the average data rate will be reduced to about 1.4K bits/sec. by means of the data rate reduction techniques used internally.

The synthesizer is realized using analog switched-capacitor filter technology and operates at 8K samples/sec. An output interpolating filter and bridge power amplifier give 20mW output power at 5 volts supply and allow the device to be connected directly to a 100Ω loudspeaker.

The S3620 also features an on-chip oscillator, requiring only a 640kHz ceramic resonator and a 120pF capacitor for normal operation.

AMI is able to provide a speech analysis service to generate the LPC parameters from customers' word lists.

Absolute Maximum Ratings*

Supply Voltage	11 Volts DC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Voltage at any Pin	V_{SS} −0.3 to V_{DD} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications: (V_{DD} = 5.0V ± 10%, V_{SS} = 0V, C_{AG} = 0.047μF, T_A = 0° to 70°C, unless otherwise specified)

D.C. Characteristics

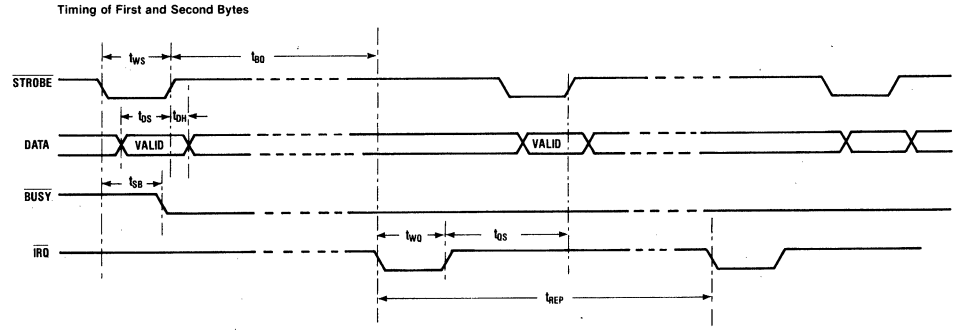
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.4		V_{DD}	V	
V_{IL}	Input Low Logic "0" Voltage	0		0.8	V	
I_{IN}	Input Leakage Current			10	μA	V_{IN} = 0 to V_{DD}
V_{OL}	Output Low Voltage ($\overline{BU}$, $\overline{IRQ}$)			0.4	V	I_{OL} = 1.6mA
V_{OS}	DC Offset Voltage, Audio Output		0.5 V_{DD}		V	R_{LOAD} = 100Ω
I_{DD}	Supply Current, Operating			35	mA	
I_{DDL}	Supply Current, Powerdown			4	mA	

AC Characteristics

P_O	Audio Output Power		20		mW	R_{LOAD} = 100Ω
t_{DS}	Data Set-up Time	100			nsec	See Figure 1
t_{DH}	Data Hold Time	10			nsec	See Figure 1
t_{WS}	Strobe Pulse Width	3.2		100	μsec	See Figure 1
t_{SB}	1st Strobe to Busy Delay		100	500	nsec	See Figure 1
t_{BQ}	1st Strobe to 1st IRQ Delay		19		msec	See Figure 1
t_{REP}	IRQ Repetition Rate		250		μsec	See Figure 1
t_{WQ}	IRQ Pulse Width	3		3.5	μsec	See Figure 1
t_{QS}	IRQ to Strobe Delay[See Note 1]			200	μsec	See Figure 1
F_{OSC}	Oscillator Resonator Frequency	−1%	640	+1%	KHz	See Figure 1
R_{LOAD}	Audio Output Load Impedance		100		Ω	
C_{INOSC}	Input Capacitance, Oscillator		100		pF	
C_{IN}	Input Capacitance, Digital Interface		7		pF	

NOTE 1: Failure to respond to an IRQ with a new strobe within the specified period results in the chip going into the power down mode.

Figure 1. Timing Requirements



Pin Function/Description

D_0 through D_7	**Data Inputs.** The speech data (in quantized form is loaded on these line in 8-bit bytes.)
ST	**Strobe Input.** A rising edge on this input strobes in the data bytes. Enunciation will commence after the first frame of data has been loaded. If no strobe is received by the chip in response to an IRQ output then enunciation stops immediately and the chip goes into power down mode.
$\overline{BU}$	**Busy Output.** This open drain output signals that enunciation is in progress by going low.
$\overline{IRQ}$	**Interrupt Request Output.** This open drain output signals that the chip is ready to receive the next byte of data. Failure to respond within the prescribed time results in the chip going into the power-down mode.
LS1 and 2	**Loudspeaker Outputs.** These pins are used to connect the chip to the loudspeaker. They are D.C. coupled and have an offset of half the supply voltage. The audio output is balanced on the two outputs.
OSC_i, OSC_o	**Oscillator Input and Output.** A 640KHz ceramic resonator (MuRata CSB640A or equivalent) should be connected between these pins for normal operation, or an external 640KHz signal may be fed into OSC_i. When a resonator is used, a 120pF capacitor should be connected between OSC_i input and ground.
T_1, T_2, T_3	**Test Inputs and Outputs.** These inputs should be left unconnected for normal operation.
V_{SS}	Most negative supply input. Normally connected to 0V.
V_{DD}	Most positive supply input.
A_{GND}	**Analog Ground.** An internally generated level approximately half way between V_{SS} and V_{DD}. A 0.047μF decoupling capacitor C_{AG} should be connected from this pin to V_{SS}. Do not connect this pin to a voltage supply.

Circuit Description

The main components of the S3620 LPC-10 Speech Synthesizer are shown in the block diagram.

Input Latch—This 8-bit latch stores the input data after the strobe pulse and loads it into the Coefficient Address Registers.

End of Word Decoder—This circuit detects the special code indicating that the last byte loaded in the Input Latch denotes the end of the speech word data and initiates the power down routine after the previous frame has been enunciated.

Buffer Registers—The data from the Speech Data ROM is assembled into frames and then decimated into the 12 parameters required for LPC-10 synthesis: pitch, gain and the 10 lattice filter coefficients. The parameters are stored in an encoded format and the decoding is done in the parameter value ROM. The coefficient address registers are used to store the assembled frame data and address this ROM.

Bit Allocation PLA—A programmable logic array is used to control the allocation of bits in the Buffer Register to the 12 parameters. The allocation and permissible variations are shown in Figure 2.

Parameter Value ROM—This ROM is used as a look-up table to decode the stored parameters into the LPC coefficients.

Interpolation Logic—The coefficients for each frame of speech, normally 20msec. are interpolated four times per frame to generate smoother and more natural sounding speech. Hence, the interpolation period is one quarter of a frame period, normally 5msec. After interpolation, the coefficients are used to drive the pitch-pulse source, the voiced/unvoiced switch, the lattice filter and the gain control. Interpolation is inhibited when a change from voiced to unvoiced speech, or vice versa, is made.

Pitch Register and Counter—This register stores the pitch parameter used to control the pitch counter.

Pitch-pulse Source—This is the signal source for voiced speech (vowel sounds). It is realized in switched-capacitor technology and generates symmetrical bipolar pulses at the rate specified by the pitch parameter and controlled by the pitch counter.

Pseudo-random Noise Source—This is the signal source for unvoiced speech (fricatives and sibilants) and consists of a 15-bit linear code generator giving a periodicity of 32767 sampling periods (4.096sec.). The output of this generator is scaled to a lower value and used as a random sign, constant amplitude signal.

Voiced/Unvoiced Speech Selector Switch—This switch determines whether the voiced or unvoiced signal source is used to drive the filter during a given frame.

LPC-10 Parameter Stack—This stack of 10 filter coefficients is used to control the lattice filter. The coefficients have an accuracy of 8-bits plus sign.

10 Stage Lattice Filter—The filter which simulates the effect of the vocal tract on the sound source (glottis) in the human speaker is realized here as a switched-capacitor (analog sampled data) 10 stage lattice filter. The filter parameters are determined dynamically by the time varying coefficients in the Parameter Stack and the filter operates at a sampling frequency of 8KHz (clock frequency/80).

Gain Controller—This controls the input signal level to the lattice filter to vary the sound level, and is an integral part of the lattice filter.

Interpolation Filter—The output signal from the lattice filter is sampled at 8KHz, and consequently its spectrum is rich in aliasing (foldover) distortion components above 4KHz (See Figure 3). The signal is cleaned up by passing it through a 4KHz low pass filter sampled at 160KHz. The spectrum of the output signal contains no aliasing distortion components below 156KHz, making the output suitable for feeding directly into a loudspeaker after amplification. This filter is also realized using switched-capacitor filter technology.

Power Amplifier—The amplifier brings up the level of the signal to give an output level of 20mW RMS into a 100Ω load. The output is a balanced bridge configuration with anti-phase signals on the 2 output pins.

Clock Generators and Power-down Control—This block contains the oscillator and timing circuits and also generates the analog ground reference voltage.

Speech Data Compression

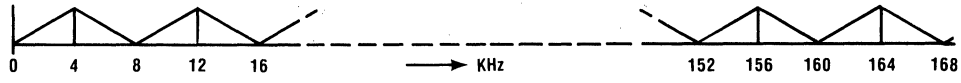
The speech data rate of the synthesizer is reduced to less than 2000 bits/sec for storage by means of a non-linear quantization technique. Each of the 12 coefficients is constrained to have a fixed set of values in an optimized manner. The actual values are dependent on the speech data and generated automatically in the analysis process. The parameters used to specify the coefficients are stored in the speech data ROM and

Figure 2. Packed Quantized Data Formats

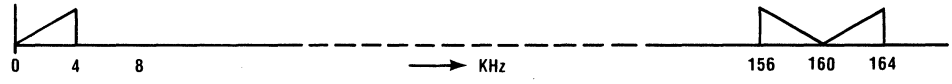
	BYTE 5								BYTE 4								BYTE 3								BYTE 2								BYTE 1							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
VOICED	← PITCH →								← K10,K9,K8,K7,K6,K5 →								← K4,K3, K2, K1 →																V/UV	REPT	← GAIN →					
UNVOICED	← NOT USED →																← K4,K3, K2, K1 →																V/UV	REPT	← GAIN →					
REPEAT	← NOT USED →																																← PITCH →			GAIN				REPT*
END OF WORD	← NOT USED →																																0	0	0	0	0	0	0	0

*NOTE: 0 = SINGLE (OR LAST) REPEAT. 1 = MULTIPLE REPEAT.

Figure 3.



(a) SPECTRUM OF SIGNAL OUTPUT OF LATTICE FILTER



(b) SPECTRUM OF SIGNAL AT OUTPUT OF INTERPOLATION FILTER.
NOTE: IN BOTH CASES A SIN x/x CHARACTERISTIC MODULATES THE SPECTRA. THIS IS OMITTED FOR SIMPLICITY.

used to address the coefficient look-up table ROM. The packing formats for the speech data are shown in Figure 2.

The speech data rate is further reduced by two other techniques shown in Figure 2. A substantial reduction is achieved by reducing the order of the lattice filter (the LPC order) to 4 during periods of unvoiced speech. This allows a 40% data reduction during these periods, which themselves typically account for 30-40% of speech (in the English language). A second reduction is obtained by detecting periods during which the filter parameters may be the same as those in the previous frame. Only the gain and pitch parameters are updated in such a frame, allowing an 80% data reduction.

Generation of Speech Data for the S3620

The speech data input to the S3620 is in a compressed format as explained in the previous section. AMI is able to provide a complete speech analysis service for this purpose and can supply the data programmed into EPROMs or mask programmed ROMs up to 128k bits. Customers who have LPC speech analysis facilities and wish to generate their own data should contact AMI for further details of the quantization technique used and the availability of software to accomplish this.

Interfacing

The S3620 is designed to be easily interfaced to an 8-bit microprocessor system such as the S6800 family. The timing requirements are shown in Figure 1. The first data byte should be present at the data input lines when the strobe line is taken to a logic 1 to begin enunciation and in response to each $\overline{IRQ}$. The busy output may be used to identify the $\overline{IRQ}$ source during polling in a multiple interrupt system. A typical system configuration is shown in Figure 4. The S3620 occupies a single address in the microprocessor's memory space and data is loaded by writing it into that address after reading it from memory. The Address decode function may be realized using a PIA. An alternative interface technique is to write the data directly into the S3620 while reading it from the memory. This can be accomplished by mapping the S3620 into the entire address space of the speech data portion of the memory, so that the strobe is generated each time a byte of data is read from the speech memory. This can save hardware, as well as microprocessor instructions, since the loading of each byte is now accomplished in a single Read cycle instead of a Read cycle followed by a Write cycle. An example of this interfacing is shown in Figure 5, where the speech data occupies the memory addresses 0000 to 7FFF.

Applications

Toys and Games
EDP
Instrumentation
Communications
Industrial Controls
Automotive
Appliances

Figure 4. Typical System Configuration

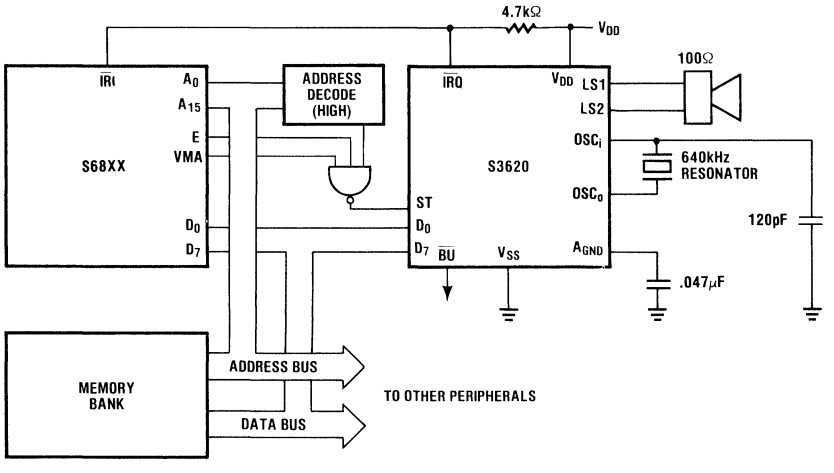
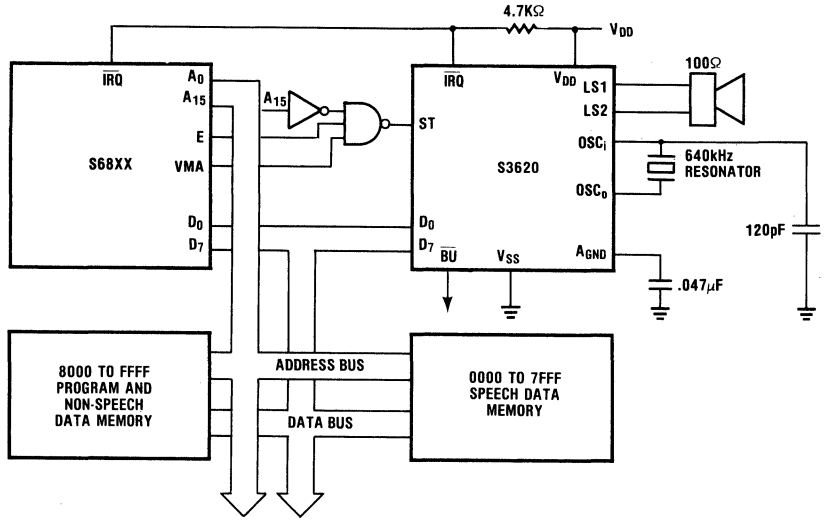


Figure 5.


4.7KΩ
VDD
100Ω
IRQ
A0
A15
E
S68XX
VMA
D0
D7
A15
IRQ
VDD
LS1
LS2
ST
OSCi
S3620
OSCo
640kHz
RESONATOR
120pF
D0
D7
BU
VSS
AGND
.047μF
8000 TO FFFF
PROGRAM AND
NON-SPEECH
DATA MEMORY
ADDRESS BUS
DATA BUS
0000 TO 7FFF
SPEECH DATA
MEMORY

AMI

A Subsidiary of Gould Inc.

Advanced Product Description **S2809**

UNIVERSAL DISPLAY DRIVER

Features

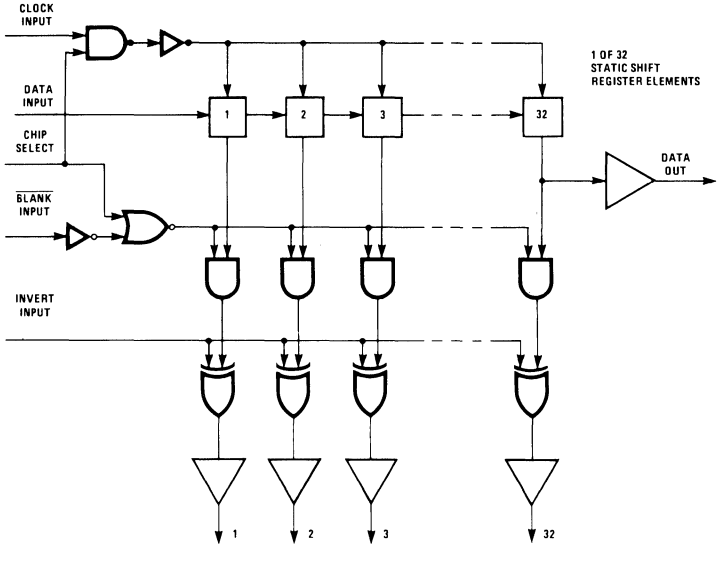
- ☐ 32 Bit Storage Register
- ☐ 32 Output Buffers
- ☐ Expansion Capability for More Bits
- ☐ Reduced RFI Emanation
- ☐ Wired OR Capability for Higher Current

General Description

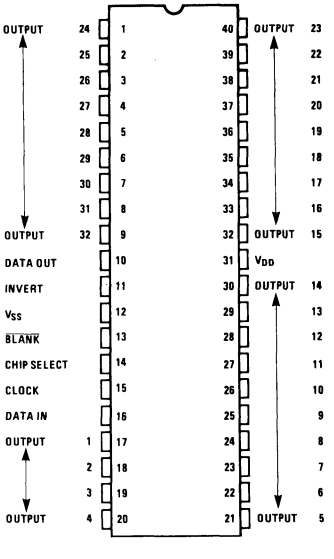
The S2809 Universal Driver is a P-Channel MOS integrated circuit. Data is clocked serially into a 32-bit master-slave static shift register. This provides static parallel drive to the output bits through drive buffers. To reduce RFI emanation, capacitors have been integrated on the circuit for reduction of output switching speeds. Serial interconnection of circuits is made possible by the Data Out Output, allowing additional bits to be driven.

Two or more outputs may be wired together for higher sourcing currents; useful in applications such as triac triggering or low voltage incandescent displays. The S2809 can also be used as a parallel output device for μC's such as AMI's S2000 series single chip microcomputer.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Operating Ambient Temperature T_A	10°C to +70°C
Storage Temperature	−65°C to +150°C
V_{SS} Supply Voltage	+25V
Positive Voltage on Any Pin	V_{SS} +0.3V

Electrical Characteristics (V_{DD} = 0V, 8V < V_{SS} < 22V, T_A = 10°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Logic 1 Level (Data, Clock, Invert, Chip Select Inputs)	V_{SS} −0.7		V_{SS} +0.3	V	
V_{IL}	Logic 0 Level (Data, Clock Invert, Chip Select Inputs)	V_{DD}		V_{SS} −7	V	
V_{BH}	Logic 1 Level ($\overline{\text{Blank}}$ Input)	V_{SS} −4.0		V_{SS} +0.3	V	
V_{BL}	Logic 0 Level ($\overline{\text{Blank}}$ Input)	V_{DD}		V_{SS} −7	V	
I_B	Current Sinked or Sourced by $\overline{\text{Blank}}$ Input			1.0	μA	Voltage applied to $\overline{\text{Blank}}$ Input between V_{DD} & V_{SS}
C_B	Capacitance of $\overline{\text{Blank}}$ Input			12	pF	
I_{OH}	Output Source Current	9.0			mA	$V_{OUT} = V_{SS}$ −3
I_{OH}	Output Source Current	4.0			mA	$V_{OUT} = V_{SS}$ −1.5
I_{OS}	Sink Current Output Load Device			50	μA	Output voltage = V_{SS}
I_{OS}	Sink Current Output Load Device	10			μA	Output voltage = V_{DD} +3V
I_L	Output Leakage Current (Output Off)			10.0	μA	
I_{DD}	Supply Current			3.0	mA	Not including output source and sink current
I_{OM}	Maximum Total Output Loading			300	mA	All outputs on
f_c	Clock Frequency	DC		100K	Hz	
t_{ON}	Clock Input Logic I Level Duration	3.0			μs	
t_{OFF}	Clock Input Logic 0 Level Duration	6.5			μs	
t_{ro}, t_{fo}	Display Output Current Rise and Fall Times	10		150	μs	*Measured between 10% and 90% of output current V_{SS}< +11V, I_{OH} = 9ma

* **NOTE:** With supply voltages higher than 11 volts, delay exists before an output rise or fall. This delay will not exceed 100μs with a 22 volt supply.

Functional Description

The 32-bit static shift register stores data to be used for driving 32 output buffers. Data is clocked serially into the register by the signal applied to the Clock Input whenever a logic 1 level is applied to the Chip Select Input; during this time, outputs are not driven by the shift register but will go to the logic level of the invert input. With a logic 0 level applied to the Chip Select Input, the 32 outputs are driven in parallel by the 32-bit register. It is possible to connect S2809 circuits in series to drive additional bits by use of the Data Output.

Clock Input

The Clock Input is used to clock data serially into the 32-bit shift register. The signal at the Clock Input may be continuous, since the shift register is clocked only when a logic 1 level is applied to the Chip Select Input. As indicated in Table 1, data is transferred from QN-1 to QN on the negative transition of the Clock Input.

Data Input

Whenever a logic 1 level is applied to the Chip Select Input, data present at the the Data Input is clocked into the 32-bit master-slave shift register. Data present at the input to the register is clocked into the master element during the logic 1 clock level and thus must be valid for the duration of the positive clock pulsewidth. This information is transferred to the slave section of each register bit during the clock logic 0 level.

Chip Select

The Chip Select Input is used to enable clocking of the shift register. When a logic 1 level is applied to this input, the register is clocked as described above. During this time, the output buffers are not driven by the register outputs, but will be driven to the logic level present at the Invert Input. With a logic 0 level at the Chip Select Input, clocking of the register is disabled, and the output buffers are driven by the 32 shift register elements.

Blank Input

This input may be used to control display intensity by varying the output duty cycles. With a logic 0 level at the Blank Input, all outputs will turn off (i.e., outputs will go to the logic level of the Invert Input). With a logic 1 level at the Blank Input, outputs are again driven in parallel by the 32 shift register elements (assuming the Chip Select Input is at logic 0).

The Blank Input has been designed with a high threshold to allow the use of a simple RC time constant to control the display intensity. This has been shown in Figure 1.

Invert Input

The Invert Input is used to invert the state of the outputs, if required. With a logic 0 level on this input, the logic level of the outputs is the same as the data clocked into the 32-bit shift register. A logic 1 level on the Invert Input causes all outputs to invert.

This input may also be used when driving liquid crystal displays, as shown in Figure 5.

Data Output

The Data Out signal is a bufferered output driven by element 32 of the shift register. It is of the same polarity as this last register bit and may be used to drive the Data Input of another S2809. In this manner, S2809 circuits may be cascaded to drive additional bits.

Table 1. Logic Truth Table

DATA IN	CLOCK	CHIP SELECT	$\overline{\text{BLANK}}$	INVERT	Q1	QN	DRIVER OUTPUT
X	X	0	0	0			0
X	X	0	0	1		NO CHANGE	1
X	X	0	1	0			QN
X	X	0	1	1			$\overline{\text{QN}}$
0	⌐	1	X	0	0	QN – 1→QN	0
1	⌐	1	X	0	1	QN – 1→QN	0
0	⌐	1	X	1	0	QN – 1→QN	1
1	⌐	1	X	1	1	QN – 1→QN	1

Figure 1. Typical Display Intensity Control

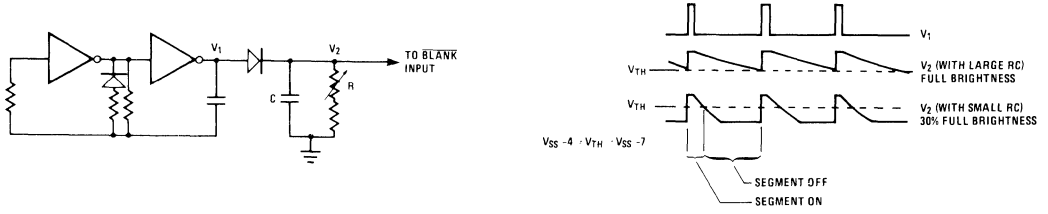


Figure 2. LED Drive — Series

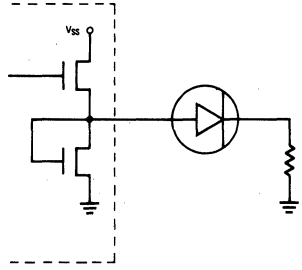


Figure 3. LED Drive — Shunt

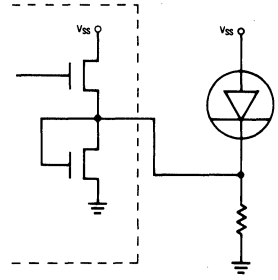


Figure 4. Vacuum Fluorescent Drive

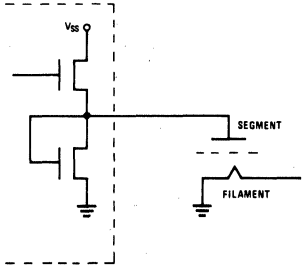


Figure 5. Liquid Crystal Drive

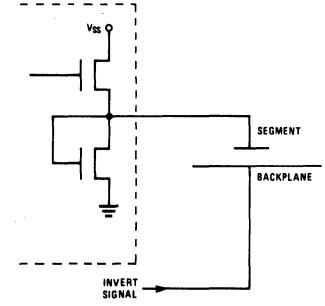
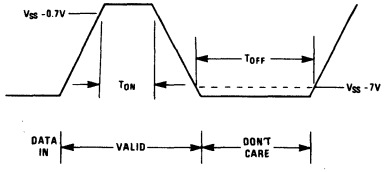
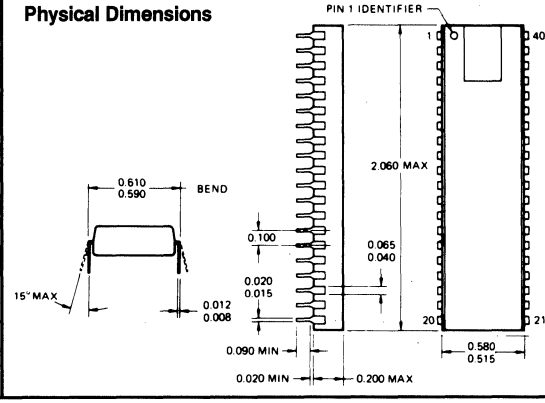


Figure 6. Clock Input Waveform



Physical Dimensions



AMI®

A Subsidiary of Gould Inc.

S4535

32 BIT, HIGH VOLTAGE DRIVER

CONSUMER PRODUCTS

Features

- ☐ High Voltage Outputs Capable of 60 Volt Swing
- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

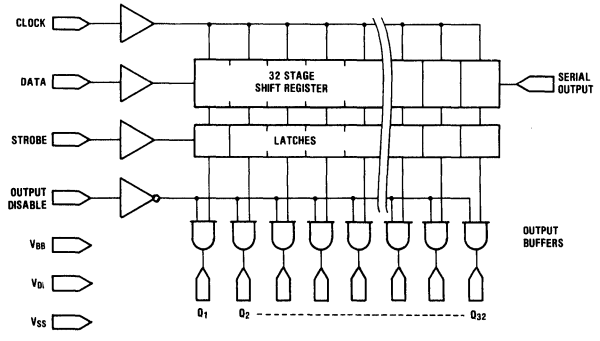
Applications:

- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

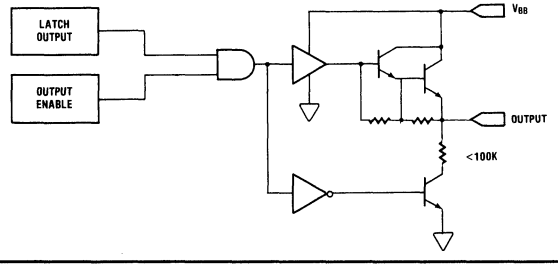
General Description

The AMI S4535 is a high voltage MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 25mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

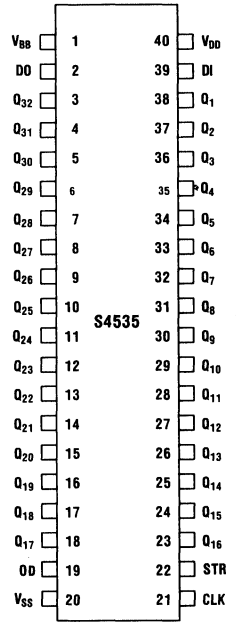
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



Absolute Maximum Ratings at 25°C

V_{BB}	65V
V_{DD}	12V
V_{IN}	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Logic)	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Display)	V_{SS} – .3V to V_{BB} + .3V
Power Dissipation	1.6W
Operating Temperature	– 40°C to + 85°C
Storage Temperature	– 65°C to + 125°C

Operational Specification: $-40°C \leq T_A \leq +85°C$ (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IL}	Input Zero Level	–0.3	0.8	V	
V_{IH}	Input One Level	3.5	$V_{DD}+0.3$	V	
V_{SL}	Signal Out Zero Level	V_{SS}	0.5	V	$I_{SO} = -20\mu A$
V_{SH}	Signal Out One Level	$V_{DD}-0.5$	V_{DD}	V	$I_{SO} = 20\mu A$
V_{DD}	Logic Voltage Supply	4.5	5.5	V	
V_{BB}	Display Voltage Supply	20	60	V	
I_{DD}	Logic Supply Current		35	mA	No Loads, T = 25°C
I_{BB}	Display Supply Current		10 168	mA mA	No Loads, T = 25°C With Load
V_{OL}	Output Zero Level	V_{SS}	1.0	V	$I_O = -20\mu A$
V_{OH}	Output One Level	$V_{BB}-2.5$ $V_{BB}-3.2$	V_{BB} V_{BB}	V V	$I_O = 5mA$ $I_O = 25mA$, One Output
t_{SD}	Serial Out Prop. Delay		500	ns	$C_L = 50pF$
t_{PD}	Parallel Out Prop. Delay		5	μs	$C_L = 50pF$
t_W	Input Pulse Width	500		ns	
t_{SU}	Data Set-Up Time	150		ns	
t_H	Data Hold Time	50		ns	

Functional Description

Serial data present at the input is transferred to the shift register on the Logic "0" to Logic "1" transition of the clock input signal. On succeeding clock pulses, the registers shift data information towards the serial data output. The input serial data must be presented prior to the rising edge of the clock input waveform.

Information present at any register is transferred to its respective latch when the strobe signal is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the strobe signal is held high.

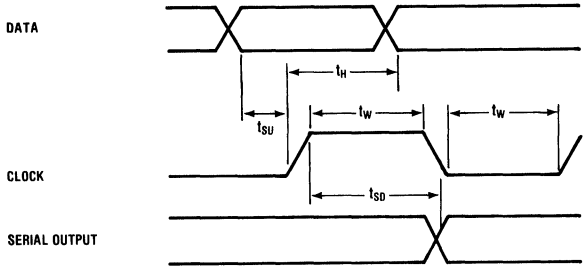
When the output disable input is high, all of the high voltage buffers are disabled without affecting the information stored in the latches or shift register. With the output disable signal low, the high voltage outputs are controlled by the state of the latches.

Pin Description

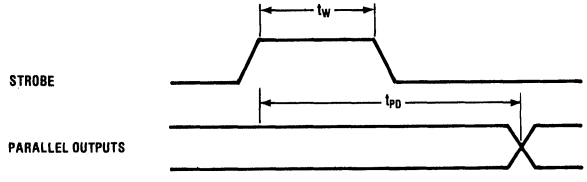
Pin #	Name	Description
20	V_{SS}	Ground Connection
2	DO	Output of Shift Register—primarily used for cascading
19	OD	Output Disable
1	V_{BB}	Q Output Drive Voltage
21	CLK	System Clock Input
40	V_{DD}	Logic Supply Voltage
22	STR	Strobe to Latch Data from Registers
39	DI	Data Input to Shift Register
3-18 and 23-38	Q_1-Q_{32}	Direct Drive Outputs

Signal Timing Diagrams

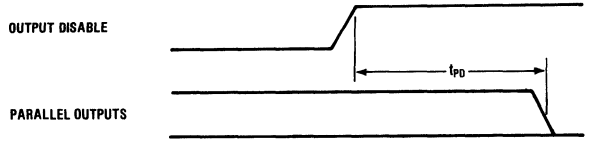
Data Write



Data Read



Output Inhibit



AMI®

A Subsidiary of Gould Inc.

S4534

10 BIT, HIGH VOLTAGE HIGH CURRENT DRIVER

Features

- ☐ Outputs Capable of 60 Volt Swings at 25mA
- ☐ Drives Up to 10 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

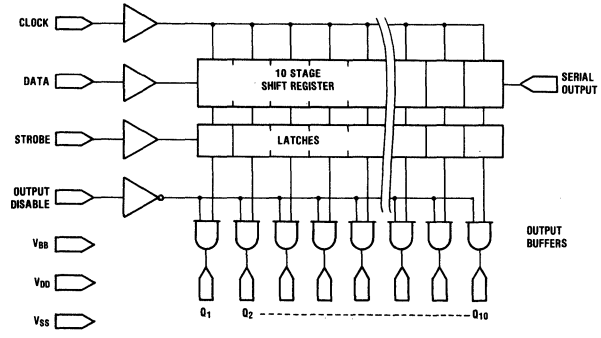
Applications:

- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

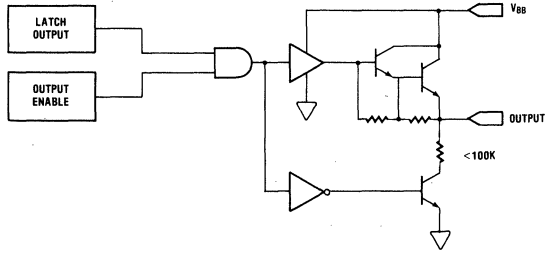
General Description

The AMI S4534 is a high voltage, high current MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 50mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 10 devices and more can be driven by cascading several drivers together.

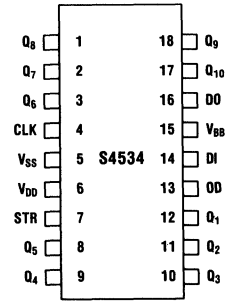
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



Absolute Maximum Ratings at 25°C

V_{BB}	65V
V_{DD}	4.5 to 15V
V_{IN}	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Logic)	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Display)	V_{SS} – .3V to V_{BB} + .3V
Power Dissipation	1.2W
Operating Temperature	0°C to + 70°C
Storage Temperature	– 65°C to + 125°C

Operational Specification: $0°C \leq T_A \leq 70°C$ (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IL}	Input Zero Level	– 0.3	1.1	V	
V_{IH}	Input One Level	3.4 3.6	V_{DD} + 0.3 V_{DD} + 0.3	V V	4.75V ≤ = V_{DD} < 5.25V 5.25V ≤ V_{DD} ≤ 12.0V
I_{IN}	Input Leakage Current		1.0	μA	V_{DD} = 5V
V_{SL}	Signal Out Zero Level	V_{SS}	0.7	V	I_{SO} = – 20μA
V_{SH}	Signal Out One Level	V_{DD} – .95 4.3	V_{DD} V_{DD}	V V	I_{SO} = 20μA, 4.75V ≤ V_{DD} < 5.25V I_{SO} = 20μA, 5.25V ≤ V_{DD} ≤ 12.0V
V_{DD}	Logic Voltage Supply	4.75	12	V	
V_{BB}	Display Voltage Supply	20	60	V	
I_{DD}	Logic Supply Current		20 30	mA mA	No Loads, V_{DD} = 5V No Loads, V_{DD} = 10V
I_{BB}	Display Supply Current		6	mA	No Loads, T = 25°C
V_{OL}	Output Zero Level	V_{SS}	1.0	V	I_O = – 20μA
V_{OH}	Output One Level	V_{BB} – 2.5	V_{BB}	V	I_O = 25mA
t_{SD}	Serial Out Prop. Delay	60	375	ns	C_L = 50pF
t_{PD}	Parallel Out Prop. Delay		5	μs	C_L = 50pF
t_W	Input Pulse Width	375		ns	
t_{SU}	Data Set-Up Time	150		ns	
t_H	Data Hold Time	40		ns	

Functional Description

Serial data present at the input is transferred to the shift register on the Logic "0" to Logic "1" transition of the clock input signal. On succeeding clock pulses, the registers shift data information towards the serial data output. The input serial data must be presented prior to the rising edge of the clock input waveform.

Information present at any register is transferred to its respective latch when the strobe signal is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the strobe signal is held high.

When the output disable input is high, all of the high voltage buffers are disabled without affecting the information stored in the latches or shift register. With the output disable signal low, the high voltage outputs are controlled by the state of the latches.

At low logic supply voltages, it is possible that the serial data output (DO) may be unstable for up to 2μs, after the rising edge of the strobe (STR) or output disable (OD) inputs.

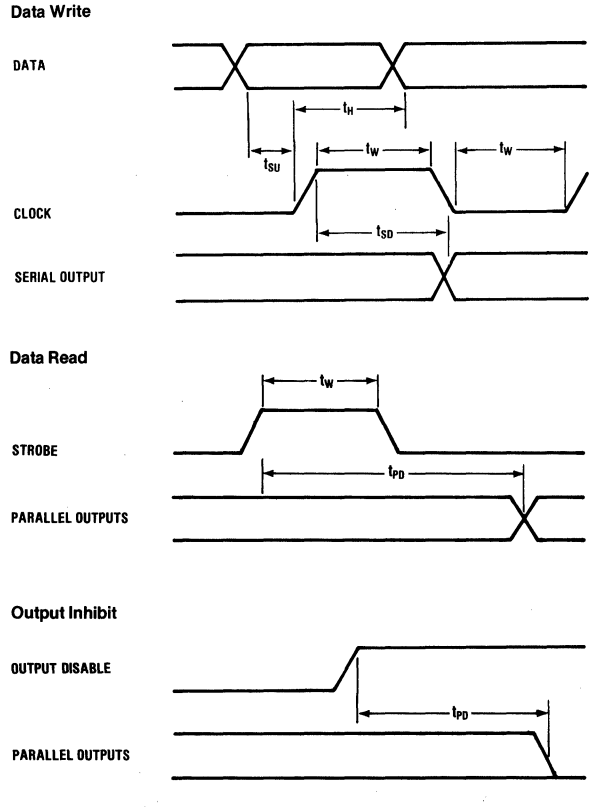
Table 1.

NUMBER OF OUTPUTS ON (I_{OUT} = 25mA)	MAX. ALLOWABLE DUTY CYCLE AT AMBIENT TEMPERATURE OF 25°C	40°C	50°C	60°C	70°C
10	100%	97%	85%	73%	62%
9	↑	100%	94%	82%	69%
8	↑	↑	100%	92%	78%
7	↑	↑	↑	100%	89%
6	↑	↑	↑	↑	100%
1	100%	100%	100%	100%	100%

Pin Description

Pin #	Name	Description
5	V_{SS}	Ground Connection
16	DO	Output of Shift Register—primarily used in cascading
13	OD	Output Disable
15	V_{BB}	Q Output Drive Voltage
4	CLK	System Clock Input
6	V_{DD}	Logic Supply Voltage
7	STR	Strobe to Latch Data from Registers
14	DI	Data Input to Shift Register
1-3, 8-12, 17-18	Q_1-Q_{10}	Direct Drive Outputs

Signal Timing Diagrams



A Subsidiary of Gould Inc.

Preliminary Data Sheet **S4521**

32 BIT DRIVER

Features

- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ On Chip Oscillator
- ☐ Requires Only 3 Control Lines
- ☐ CMOS Construction For:
  - Wide Supply Range
  - High Noise Immunity
  - Wide Temperature Range

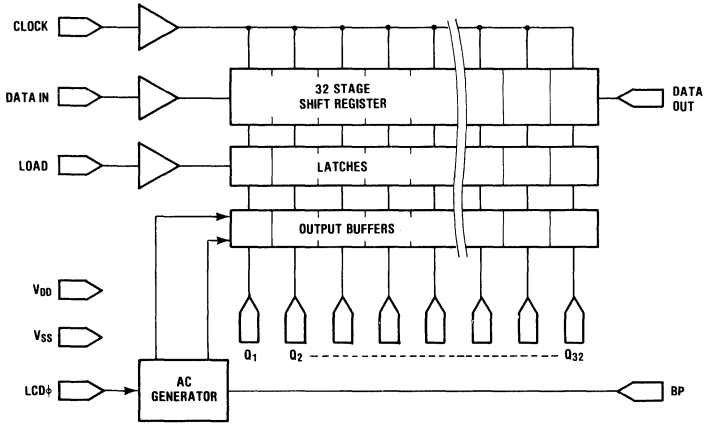
Applications:

- ☐ Liquid Crystal Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

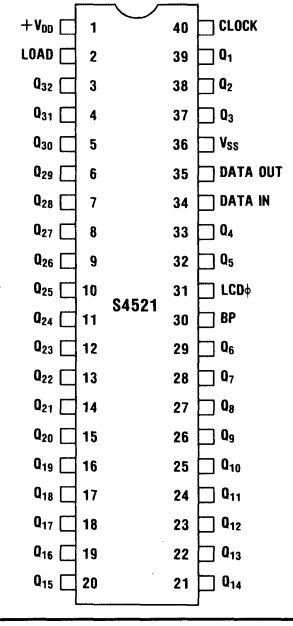
General Description

The AMI S4521 is an MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control. This device requires only three control lines due to its serial input construction. It latches the data to be output, relieving the microprocessor from the task of generating the required waveform, or it may be used to bring data directly to the drivers. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations. It is especially well suited to driving liquid crystal displays, with a backplane A.C. signal option that is provided. The A.C. frequency of the backplane output that can be user supplied or generated by attaching a capacitor to the LCDϕ input, which controls the frequency of the internal oscillator. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

Functional Block Diagram



Pin Configuration



Absolute Maximum Ratings at 25°C

V_{DD}	−0.3 to +17V
Inputs (CLK, DATA IN, LOAD, LCDϕ)	V_{SS} − 0.3 to V_{DD} + 0.3V
Power Dissipation	250mW
Storage Temperature	−65°C to +125°C
Operating Temperature	−40°C to +85°C

Electrical Characteristics: $3V \leq V_{DD} \leq 13V$, unless otherwise noted

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{DD}	Supply Voltage	3	13	V	
	Supply Current				
I_{DD1}	Operating		200	μA	f_{BP} = 120Hz, No Load, V_{DD} = 5V
I_{DD2}	Quiescent		200	μA	LCDϕ High or Low, f_{BP} = 0 Load @ Logic 0, V_{DD} = 5V
	Inputs (CLK, DATA IN, LOAD)				
V_{IH}	High Level	0.6 V_{DD} 0.5 V_{DD}	V_{DD} V_{DD}	V V	$3V \leq V_{DD} < 5V$ $5V \leq V_{DD} \leq 13V$
V_{IL}	Low Level	V_{SS}	0.2 V_{DD}	V	
I_L	Input Current		5	μA	
C_I	Input Capacitance		5	pF	
f_{CLK}	CLK Rate	DC	2	MHz	50% Duty Cycle
t_{DS}	Data Set-Up Time	100		ns	Data Change to CLK Falling Edge
t_{DH}	Data Hold Time	10		ns	Falling CLK Edge to Data Change
t_{PW}	Load Pulse Width	200		ns	
t_{PD}	Data Out Prop. Delay		220	ns	C_L = 30pF, From Rising CLK Edge
t_{LC}	Load Pulse Set-Up	300		ns	Falling CLK Edge to Rising Load Pulse
t_{LCD}	Load Pulse Delay	0		ns	Falling Load Pulse to Falling CLK Edge
V_{OAVG}	DC Bias (Average) Any Q Output to Backplane		±25	mV	f_{BP} = 120Hz
V_{IH}	LCDϕ Input High Level	.9 V_{DD}	V_{DD}	V	Externally Driven
V_{IL}	LCDϕ Input Low Level	V_{SS}	.1 V_{DD}	V	Externally Driven
	Capacitance Loads				
C_{LQ}	Q Output		50,000	pF	f_{BP} = 120Hz
C_{LBP}	Backplane		1.5	μF	f_{BP} = 120Hz, See Note 8
R_{ON}	Q Output Impedance		3.0	KΩ	I_L = 10μA, V_{DD} = 5V
R_{ON}	Backplane Output Impedance		100	Ω	I_L = 10μA, V_{DD} = 5V
R_{ON}	Data Out Output Impedance		3.0	KΩ	I_L = 10μA, V_{DD} = 5V

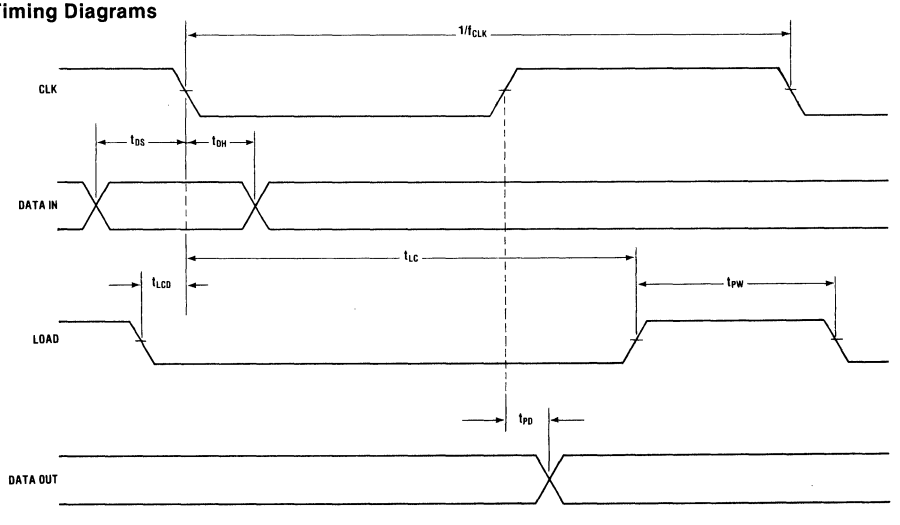
Operating Notes

1. The shift register shifts on the falling edge of CLK. It outputs on the rising edge of the CLK.
2. The buffer number corresponds to how many clock pulses have occurred since its data was present at the input (e.g., the data on Q10 was input 10 clock pulses earlier).
3. A logic 1 on Data In causes a Q output to be out of phase with the Backplane.
4. A logic 1 on Load causes a parallel load of the data in the shift register, into the latches that control the Q output drivers.
5. To cascade units, (a) connect the Data Out of one chip to Data In of next chip, and (b) either connect Backplane of one chip to LCDϕ of all other chips (thus one RC provides frequency control for all chips) or connect LCDϕ of all chips to a common driving signal. If the former is chosen, the Backplane that is tied to the LCDϕ inputs of the other chips should **not** also be connected to the Backplanes of those chips.
6. If LCDϕ is driven, it is in phase with the Backplane output.
7. The LCDϕ pin can be used in two modes, driven or self-oscillating. If LCDϕ is driven, the circuit will sense this condition. If the LCDϕ pin is allowed to oscillate, its frequency is determined by an external capacitor. The Backplane frequency is a divide by 32 of the LCDϕ frequency, in the self-oscillating mode.
8. In the self-oscillating mode, the backplane frequency is approximately defined by the relationship $f_{BP}(Hz) = 0.2 \div C(\text{in } \mu F)$ at $V_{DD} = 5V$.
9. If the total display capacitance is greater than 100,000 pF, a decoupling capacitor of 1μF is required across the power supply (pins 1 and 36).

Pin Description

Pin #	Name	Description
1	V_{DD}	Logic and Q Output Supply Voltage
2	LOAD	Signal to Latch Data from Registers
30	BP	Backplane Drive Output
31	LCDϕ	Backplane Drive Input
34	DATA IN	Data Input to Shift Register
35	DATA OUT	Data Output from Shift Register-primarily used in cascading
36	V_{SS}	Ground Connection
40	CLOCK	System Clock Input
3-29, 32-33, 37-39	Q_1-Q_{32}	Direct Drive Outputs

Signal Timing Diagrams



A Subsidiary of Gould Inc.

Advanced Product Description

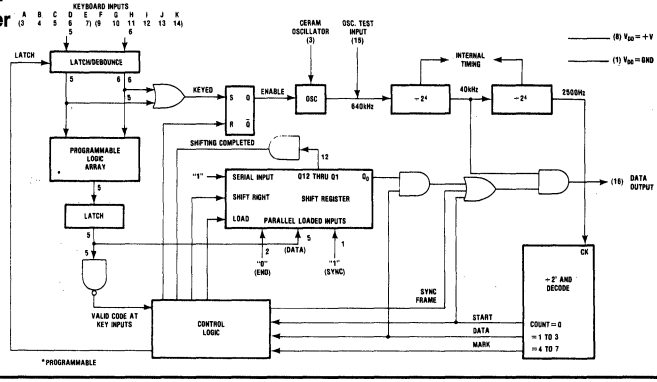
S2600/S2601

ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

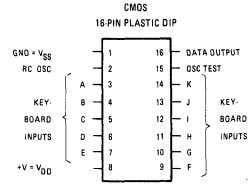
Features

- ☐ Small Parts Count — No Crystals Required
- ☐ Easily Used in LED, Ultrasonic, RF, or Hardwire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 31 Commands — 5-bit Output Bus With Data Valid
- ☐ 3 Analog (LP Filterable PWM) Outputs
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Indexing Output — 2½ Hz Pulse Train
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

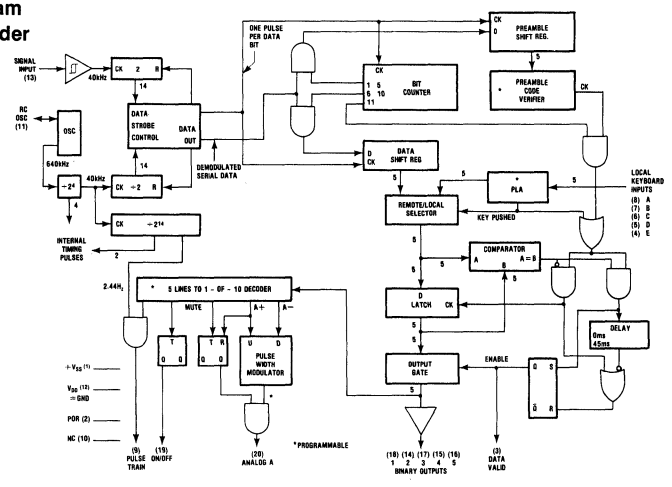
Block Diagram S2600 Encoder



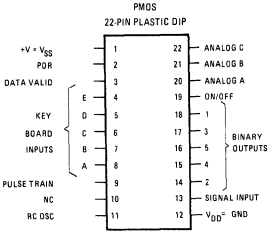
Pin Configuration S2600



Block Diagram S2601 Decoder



Pin Configuration S2601



Functional Description

The S2600/S2601 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a synchronizing marker technique has eliminated the need for highly accurate frequencies generated by crystals. The S2600 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 thru 6 constitute a fixed preamble which must be received correctly for the command bits to be received, and bits 7 through 11 contain the command data. The S2601 Decoder produces an output only after two complete, consecutive, identical, 12-bit transmissions. Marker pulses, preamble bits, and redundant transmissions, have given the S2600/S2601 system a very high immunity to noise, without a large number of discrete components.

S2600 Encoder

The S2600 is a CMOS device with an on-chip oscillator, 11 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator requires only an external resistor and capacitor, and to conserve power, **runs only during transmission.** Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group A through E is activated with one from the group F through K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2600/S2601 CODING," below. This code is loaded into a shift register in parallel with the sync, preamble, and end bits, to form the 12-bit message.

The transmitter output is a 40 kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in a 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The Test input is used for functional testing of the device. A low level input will cause the oscillator frequency to be gated to the Data Output pin. This input has an internal pull-up resistor to V_{DD}.

S2601 Decoder

The S2601 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40kHz signal input, and 11 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2601, overriding any 40kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40kHz signal from the local RC oscillator timing chain. A 40kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ± 24% with respect to the receiver oscillator frequency.

Decoded data bits from the next five bit frames following the initial synchronizing frame are compared with the fixed preamble code. The next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, and if the preamble bits are correct, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next 12-bit transmission. In the case where 2 identical, proper, 12-bit transmissions are immediately followed either by transmissions with erroneous preamble codes or by

nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

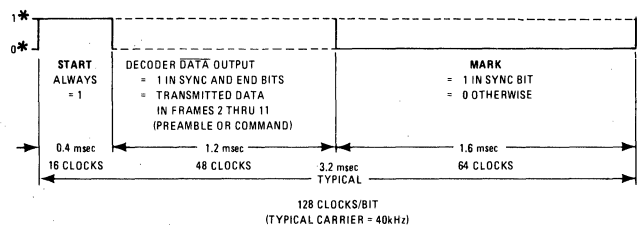
The S2601 has five other outputs: Pulse Train, On/Off, Analog A, Analog B, and Analog C. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated. The Pulse Train output provides a 2.44Hz square wave (50% duty factor) whenever 11011 appears at the Binary Outputs, but otherwise it remains at a logic "0". This pulse train can be used for indexing, e.g., for stepping a TV channel selector.

The On/Off ("mains") output changes state each time 01111 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

Analog Outputs A, B and C are 10kHz pulse trains whose duty factors are independently controllable. With a simple low-pass filter each of these outputs can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. Each Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code—6 codes in all. The entire range of 0% to 100% duty factor can be traversed in 6.5 seconds or at a rate of the oscillator frequency divided by 2^{12}. All three Analog Outputs are set to 50% duty factor whenever 01011 appears at the Binary Outputs. Analog A is mutable; 01100 sets it to 0% duty factor. If 01100 then disappears and reappears, the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2601 has an on-chip power-on reset (POR) circuit which sets the Pulse Train and On/Off Outputs to "0", sets the Analog Outputs at 50% duty factor, and insures that Analog A is muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

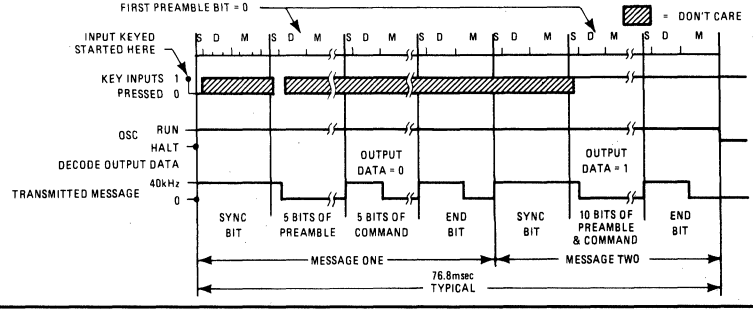
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

** IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



AMI®

A Subsidiary of Gould Inc.

Advanced Product Description **S2602/S2603**

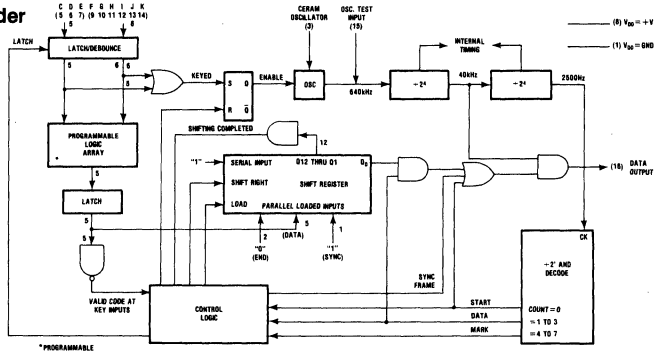
ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

CONSUMER PRODUCTS

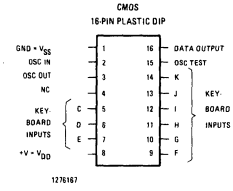
Features

- ☐ Accurate Data Transmission - No Frequency Trimming Required
- ☐ Easily Used in LED, Ultrasonic, RF, or Hardwire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 18 Commands—5-bit Output Bus with Data Valid
- ☐ Analog (LP Filterable PWM) Output
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

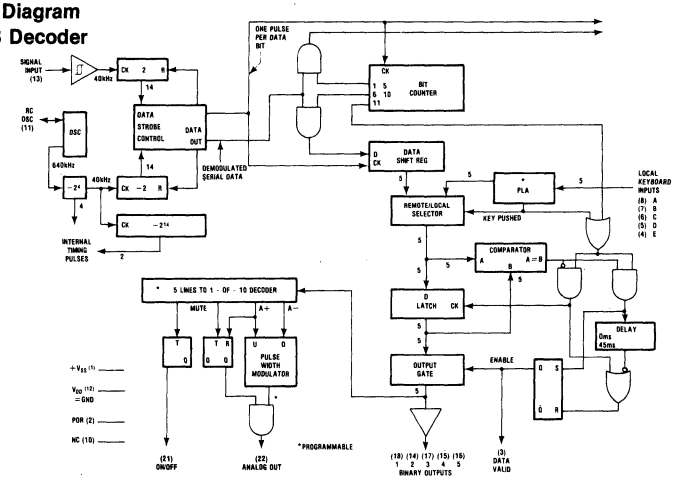
Block Diagram
S2602 Encoder



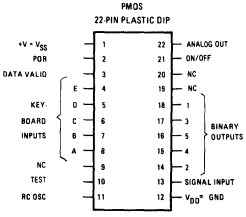
Pin Configuration
S2602



Block Diagram
S2603 Decoder



Pin Configuration
S2603



Functional Description

The S2602/S2603 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a ceramic resonator with the S2602 Encoder eliminates the need to trim the S2603 decoder oscillator.

The S2602 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 through 6 are place-holder bits, and bits 7 through 11 contain the command data. The S2603 Decoder produces an output only after two complete, consecutive, identical transmissions. Marker pulses and redundant transmissions have given the S2602/S2603 system a very high immunity to noise, without a large number of discrete components.

S2602 Encoder

The S2602 is a CMOS device with an on-chip oscillator, 9 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator uses an external ceramic resonator, and to conserve power, **runs only during transmission.** Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group C through E is activated with one from the group F through K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2602/ S2603 CODING," below. This code is loaded into a shift register in parallel with the sync and end bits to form the message.

The transmitter output is a 40kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The S2602 Encoder is silenced automatically by an on-chip duration limiter if a transmission persists for 6½ seconds (FOSC = 320kHz). The absence of a keyboard closure will reset the duration limiter so that a new 6½ second internal starts with the next key closure.

S2603 Decoder

The S2603 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40kHz signal input, and 8 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2603, overriding any 40kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40kHz signal from the local RC oscillator timing chain. A 40kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ± 24% with respect to the receiver oscillator frequency.

The decoded place-holder bits from the next five-bit frames following the initial synchronizing frame are not used. However, the next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next transmission. In the case where 2 identical, proper transmissions are immediately followed by nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

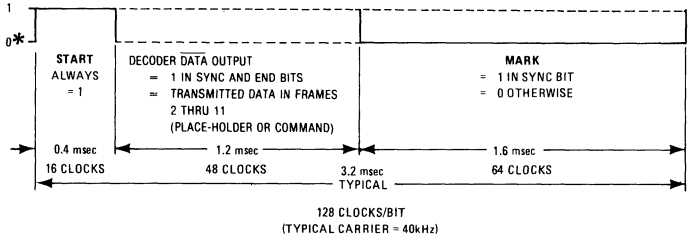
The S2603 has two other outputs: On/Off and Analog. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated.

The On/Off ("mains") output changes state each time 10011 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

The Analog Output is a 10kHz pulse train whose duty factor is digitally controllable. With a simple low-pass filter, this output can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. The Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code. The Analog Output is mutable; 11110 sets it to 0% duty factor. If 11110 then disappears and reappears, the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2603 has an on-chip power-on reset (POR) circuit which sets the On/Off Output to "0", sets the Analog Output at 50% duty factor, and insures that the Analog Output is muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

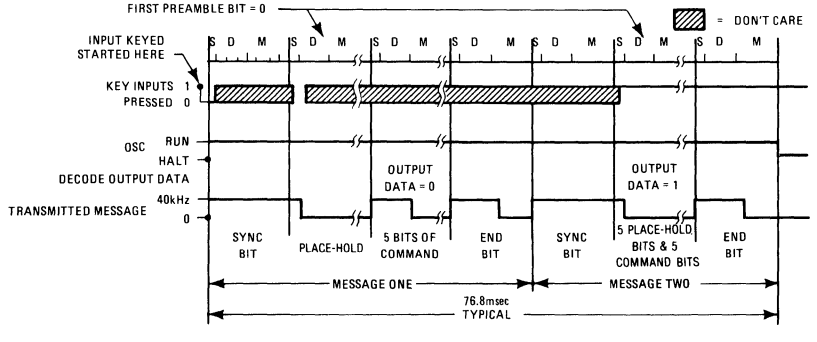
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



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Advanced Product Description

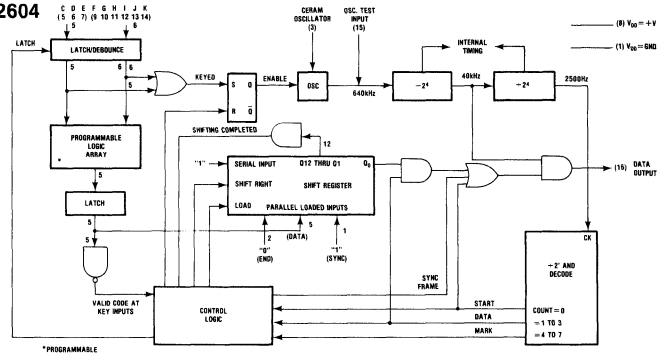
S2604/S2605

ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

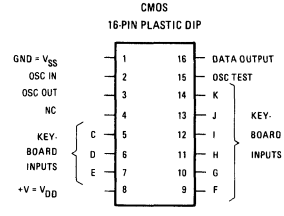
Features

- ☐ Accurate Data Transmission - No Frequency Trimming Required
- ☐ Easily Used in LED, Ultrasonic, RF, or Hardwire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 18 Commands—5-bit Output Bus with Data Valid
- ☐ Analog (LP Filterable PWM) Output
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

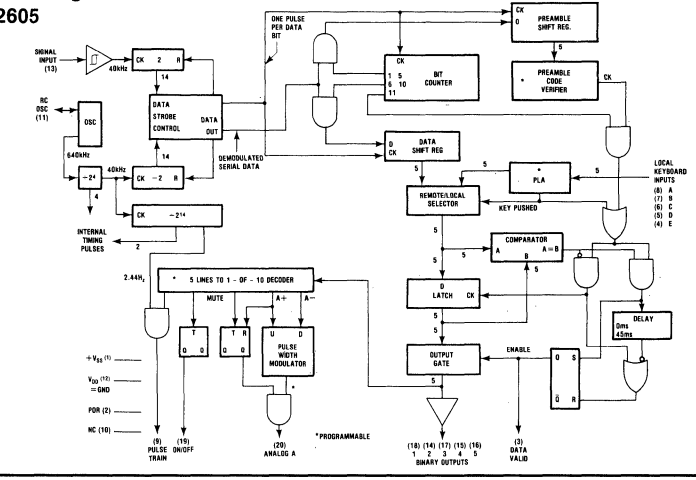
Block Diagram S2604



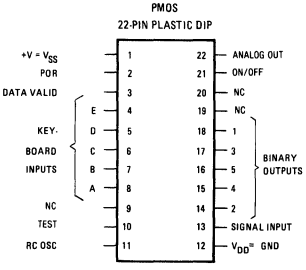
Pin Configuration S2604



Block Diagram S2605



Pin Configuration S2605



Functional Description

The S2604/S2605 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a ceramic resonator with the S2604 Encoder eliminates the need to trim the S2605 decoder oscillator.

The S2604 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 through 6 constitute a fixed preamble which must be received correctly for the command bits to be received, and bits 7 through 11 contain the command data. The S2605 Decoder produces an output only after two complete, consecutive, identical transmissions. Marker pulses, preamble bits, and redundant transmissions, have given the S2604/S2605 system a very high immunity to noise, without a large number of discrete components.

S2604 Encoder

The S2604 is a CMOS device with an on-chip oscillator, 9 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator uses an external ceramic resonator, and to conserve power, **runs only during transmission.** Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group C through E is activated with one from the group F through K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2604/S2605 CODING," below. This code is loaded into a shift register in parallel with the sync and end bits to form the message.

The transmitter output is a 40kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The S2604 Encoder is, however, silenced automatically by an on-chip duration limiter if a transmission persists for 6½ seconds (FOSC = 320kHz). The absence of a keyboard closure will reset the duration limiter so that a new 6½ second interval starts with the next key closure.

S2605 Decoder

The S2605 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40kHz signal input, and 8 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2605, overriding any 40kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40kHz signal from the local RC oscillator timing chain. A 40kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ± 24% with respect to the receiver oscillator frequency.

Decoded data bits from the next five bit frames following the initial synchronizing frame are compared with the fixed preamble code. The next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, and if the preamble bits are correct, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next 12-bit transmission. In the case where 2 identical, proper, 12-bit transmissions are immediately followed either by transmissions with erroneous preamble codes or by nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

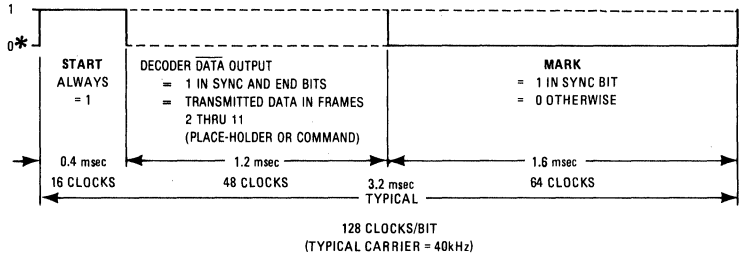
The S2605 has two other outputs: On/Off, and Analog. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated.

The On/Off ("mains") output changes state each time 10011 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

The Analog Output is a 10kHz pulse trains whose duty factors are independently controllable. With a simple low-pass filter each of these outputs can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. Each Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code. The Analog Output is mutable; 11110 sets it to 0% duty factor. If 11110 then disappears and reappears while the On/Off output is "On", the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2605 has an on-chip power-on reset (POR) circuit which sets the On/Off Outputs to "0", sets the Analog Outputs at 50% duty factor, and insures that Analog is not muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

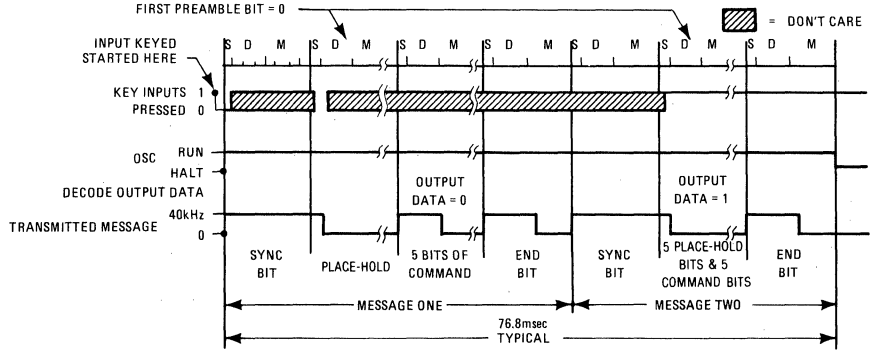
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



S2604/S2605 Coding

TRANSMITTER KEYBOARD INPUT PINS TIED TO V_{SS}	RECEIVER KEYBOARD INPUT PINS TIED TO V_{DD} (Note 1)	RESULTING RECEIVER BINARY OUTPUTS					RECEIVER DEDICATED FUNCTIONS
		1	2	3	4	5	
— (Note 2)		1	1	1	1	1	
DI		0	1	1	1	1	
CF		0	1	1	1	0	
DF		0	1	1	0	1	
EF		0	1	1	0	0	
CG		0	1	0	1	1	
DG		0	1	0	1	0	
EG		0	1	0	0	1	
CH		0	1	0	0	0	
DH		0	0	1	1	1	
EH		0	0	1	1	0	
EI	AE	1	0	1	0	0	
EJ	BE	1	1	0	0	0	
CI	A	1	1	1	0	0	INCREASE ANALOG (Note 5)
CJ	B	1	1	1	0	1	DECREASE ANALOG (Note 5)
CK	E	1	1	1	1	0	MUTE TOGGLE (Note 4)
EK	C	0	0	0	0	1	
DK	D	1	0	0	1	1	TOGGLE ON/OF OUTPUT
DJ	EC	0	0	0	0	0	
INVALID (Note 3)		1	1	1	1	1	(Note 3)
	AC	1	0	0	0	1	INCREASE ANALOG (Note 5)
	BC	1	0	0	1	0	DECREASE ANALOG (Note 5)

NOTES:

1. RECEIVER KEYBOARD INPUTS OVERRIDE ANY REMOTE SIGNAL.
2. REST STATE, "DATA VALID" OUTPUT **INACTIVE**
3. ANY SINGLE CLOSURE, INVALID COMBINATION OF 2 CLOSURES, OR COMBINATION OF 3 OR MORE CLOSURES OF S2604 TRANSMITTER INPUTS C, D, E, F,
4. THE MUTE TOGGLE WILL FUNCTION ONLY WHEN THE "ON/OFF" OUTPUT IS **ON.** HOWEVER MUTE IS **CLEARED** BY TURNING "ON/OFF" **OFF**, THEN **ON** AGAIN.
5. THE PULSEWIDTH OF THE ANALOG OUTPUT MAY BE CHANGED ONLY WHEN THE "ON/OFF" OUTPUT IS **ON.**

Electrical Specifications—2604 Encoder— All voltages measured with respect to V_{SS}

Absolute Maximum Ratings

Operating Ambient Temperature T_A	0 to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on any Pin	+14V
Negative Voltage on any Pin	−0.3V

Electrical Characteristics: Unless otherwise noted, $V_{DD} = 8.5 \pm 1.5V$ and $T_A = 0$ to +70°C.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f0	Oscillator Frequency	50	320	2000	kHz	
I_{DD}	Supply Current			2	mA	During Transmission, Data Output = 1mA
	Standby			10	μ	No transmission (25°C)
V_{IH}	Input "1" Threshold	20			$\%V_{DD}$	
V_{IL}	Input "0" Threshold			80	$\%V_{DD}$	
I_{LL}	Input Source Current	50		300	μA	$V_I = 0V$
I_{OH}	Output Source Current	1	1.5		mA	$V_O = V_{DD} - 3V$
I_{OL}	Output Sink Current	−.2	−.5		mA	$V_O = +0.5V$

Note: Circuit operates with V_{DD} from 3.0V to 12.0V.

Electrical Specifications—2605 Decoder— All voltages measured with respect to V_{DD}

Absolute Maximum Ratings

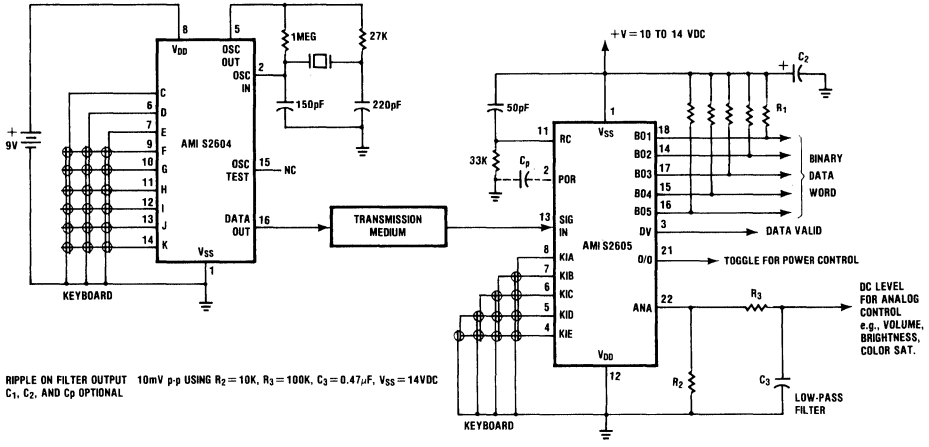
Operating Ambient Temperature T_A	0°C to 70°C
Storage Temperature	−65°C to +150°C
V_{SS} Power Supply Voltage	+31V
Positive Voltage on any Pin	V_{SS} +0.3V
Negative Voltage on any Pin	V_{SS} −31V

Electrical Characteristics: Unless otherwise noted, $V_{SS} = 12 \pm 2V$ and $T_A = 0$ to +70°C.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f0	Oscillator Frequency	512	640	768	kHz	
Δf0/f0	Frequency Deviation	−10		+10	%	Fixed R_{OSC}, C_{OSC}, V_{SS}
I_{SS}	Supply Current		34	50	mA	No Loads, $V_{DD} = 14V$
			28		mA	$V_{DD} = 10V$
Signal Input:						
V_{IH}	"1" Threshold			85	$\%V_{SS}$	
V_{IL}	"0" Threshold	30			$\%V_{SS}$	
V_{IH}-V_{IL}	Voltage Hysteresis	5		35	$\%V_{SS}$	
Keyboard and POR Inputs:						
V_{IH}	"1" Voltage	$V_{SS}-.5$	$V_{SS}-3.0$		V	
V_{IL}	"0" Voltage			$V_{SS}-5.5$	V	
I_{LL}	Source Current	50	150	300	μA	$V_I = V_{SS}-10V$
	Debounce Delay (Keyboard Inputs Only)	1.45		2.2	msec	
Binary Outputs (open source):						
I_{OL}	Sink Current	−0.7			mA	$V_0 = V_{SS}-5.2V$, $V_{SS} = 16V$
		−0.50	−0.60		mA	$V_0 = V_{SS}-5.2V$, $V_{SS} = 10V$
	Duration	34.9			msec	f0 = 704 kHz
Analog Output (open drain):						
ΔV_{step}	Step Voltage Change		$V_{SS}/64$		V	
I_{OH}	Source Current		1.04		mA	$V_0 = V_{SS}-0.5V$, $V_{SS} = 10V$
			1.15		mA	$V_0 = V_{SS}-0.5V$, $V_{SS} = 14V$
		1.0	1.2		mA	$V_0 = V_{SS}-1V$
f_{step}	Analog Step Rate		10		kHz	(f0 ÷ 64)
Data Valid and On/Off Outputs:						
I_{OH}	Source Current	1	1.5		mA	$V_0 = V_{SS}-2V$
I_{OL}	Sink Current	−30	−50		μA	$V_0 = .7V$
t_r	Risetime (.1 V_{SS} to .9 V_{SS})			10	μsec	$R_L = \infty$, C_L 50pF
t_f	Falltime (.9 V_{SS} to .1 V_{SS})			10	μsec	$R_L = \infty$, C_L 50pF

Note: Circuit operates with V_{SS} from 7.0V to 30.0V

Typical Bench Test Setup, Using a 320kHz Ceramic Resonator with S2604



RIPPLE ON FILTER OUTPUT 10mV p-p USING $R_2 = 10K$, $R_3 = 100K$, $C_3 = 0.47\mu F$, $V_{SS} = 14VDC$
C_1, C_2, AND C_P OPTIONAL

ENCODER/DECODER REMOTE CONTROL 2-CHIP SET

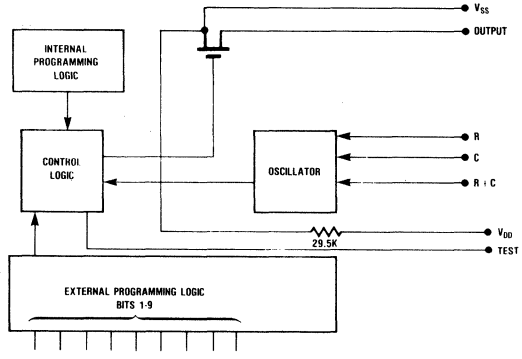
Features

- ☐ RC Oscillator Used—No Crystal Required
- ☐ Phase Locked Loop on Decoder for Reliable Operation
- ☐ 512 User Selectable Address Codes
- ☐ Encoder Operates on a Single Rail 9 Volt Supply — Suitable for Inexpensive and Convenient Battery Operation
- ☐ User can Determine the Type of Transmission Medium to Use

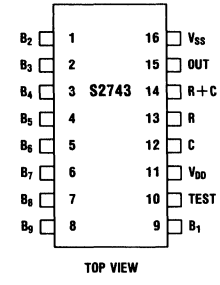
Applications

- ☐ Entry Access Systems
- ☐ Remote Engine Starting for Vehicles and Standby Generators
- ☐ Security Systems
- ☐ Traffic Control
- ☐ Paging Systems
- ☐ Remote Control of Domestic Appliances

Block Diagram 2743 Encoder

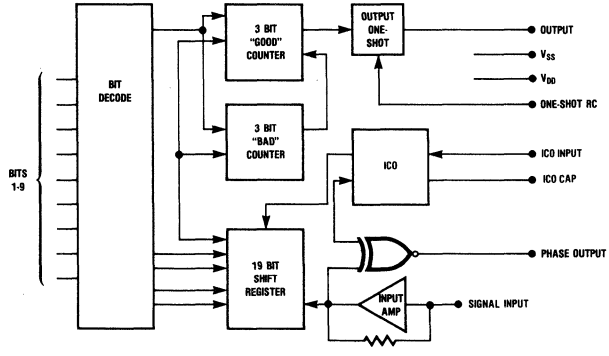


Pin Configuration 2743

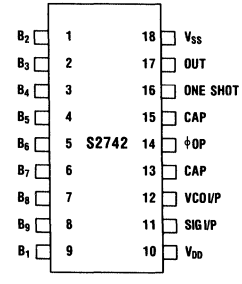


TOP VIEW

Block Diagram 2742 Decoder



Pin Configuration 2742



TOP VIEW

General Description—Encoder/Decoder

This two-chip PMOS set includes a user-programmable serial data encoder for use in a simple low-power transmitter and a serial data decoder for use in a user addressable receiver. The user can select the transmission medium (RF, infrared, or hardwire). The externally selectable message allows up to 512 codes or addresses; this is done with the nine binary inputs on each device. An additional 3 bits of address can be programmed on chip as a fixed preamble.

The serial data encoder encodes by means of a frequency-shift-keyed trinary data pattern composed of 16 data bits. Each data bit will have a length equivalent to 32 cycles of high frequency clock (20kHz typical). Each trinary data pattern will be 512 cycles of 1/2 the oscillator frequency length. The encoder frequency oscillator reference is controlled with an external RC network. The encoder transmitter can be powered by a single 9 volt battery so that a single momentary push button will activate the encoder and transmitter. In the off position there is no current flow.

The serial data decoder in conjunction with a receiver amplifier decodes the transmitted 16-bit coded signal. The on-chip phase-locked-loop locks in on the 20kHz signal even if the transmitted frequency differs from the receiver by up to ±15%. The coded signal input is compared with the externally selected code. The serial decoder looks at the transmitted signal a minimum of three times before validating a good message. A 3-bit "good" code counter or a 3-bit "bad" code counter accumulates the number of successive good and bad codes being received.

The decoder has an on-chip one-shot which is user programmed by an external RC combination. Whenever three complete good codes are received in the "good" counter a signal enables the one-shot which controls the signal valid output. If a series of three sequential bad codes enter the "bad" code counter the "bad" counter resets the "good" code counter and one-shot period and will not allow an active output until the end of the one-shot period. Any "good" code resets the "bad" code counter. If the "good" counter has accumulated three good codes and activated the output one shot, any occasional "good" code (occurring within the one-shot period) will maintain the output by retriggering the one-shot. The output appears like a single switch, on when "good" codes are received, off when not, with the minimum total period being determined by twice the one-shot period. The one-shot can be used to prevent the output from switching on and off too rapidly due to system noise. The typical RC components shown in the block diagram give a period of about one second.

Functional Description—Serial Data Encoder

The AMI serial data encoder is comprised of three sections: Oscillator, Programming Logic, and Control Logic. Specifically it will provide logical ones "1", logical zeroes "0", and synchronization pulses "S" and arrange them into a trinary data pattern composed of 16 data bits. Each data bit will be 32 cycles of the high frequency (HF-1/2 Oscillator Frequency) in length. Each trinary data pattern will be 512 cycles of 1/2 the Oscillator Frequency length.

A logical "1" is represented by 32 cycles of the high frequency.

A logical "0" is represented by 16 cycles of the high frequency followed directly by 8 cycles of the low frequency (LF = 1/2 HF).

A synchronization pulse "S" is represented by 16 cycles of the low frequency.

A 16-bit data pattern will be encoded in the device in such a manner as to have three (3) bits programmed internally and nine (9) bits programmed externally.

The Oscillator Frequency equals twice that of the High Frequency, and the High Frequency equals twice that of the Low Frequency.

The Oscillator circuit will require a maximum of three (3) external components (refer to Figure 2).

External programming inputs connected to the device $-V_{DD}$ supply will be considered as a logical "1". The bit programming current will not exceed 50μA. The programming resistance should not exceed 1kΩ. Unconnected external bit programming inputs will be considered at a logical "0".

A "1" ($-5V \leq$ "1" $\leq V_{DD}$) presented to the "Test" input sets the Internal counter and maintains the output of the device "On." The input impedance of the test input is greater than 5MΩ.

For portable operation a 9V transistor battery can be used for the DC voltage supply. Proper circuit polarity must be observed ($-V_{DD}$, $+V_{SS}$).

S2743 Absolute Maximum Ratings

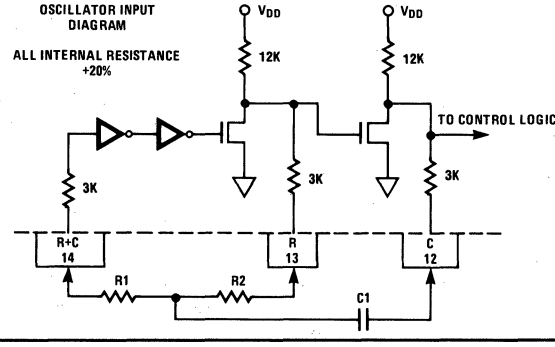
DC Supply Voltage	−15V
Input Voltage	V_{SS} + .3V to V_{SS} − 15V
Operating Temperature Range	−40°C to +100°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (During Soldering)	300°C for Max. 10sec.

S2743 Electrical Characteristics (25°C Air Temperature Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Operating Supply Voltage	−6.65	−9.5	−15	V	V_{DD}; V_{SS} = 0V
	Operating Power Dissipation		27	40	MW	−8V, −5mA, Max.
	Operating Frequency	2	40	60	kHz	Oscillator
	Programming Bits 1-9, Current			50	μA	Programming Input, R 1kΩ
	External Programming Resistance			1	kΩ	Bits 1-9
	(DC Bits 1-9) Program Logical "1"	V_{SS} −5V		V_{DD}	V	
	Input Levels Logical "0"	V_{SS} −1V		V_{SS}	V	
	Bits 1-9 Current		55		μA	Input R 9V>1.5M @ 5V
	Test and R + C Input Impedance	5		75	MΩ	
	(DC) Test Input Levels Test ON	V_{SS} −5V		V_{DD}	V	Maintains Output Device ON
	Test OFF (See Note 1)	V_{SS} −1V		V_{SS}	V	Permits Normal Operation
	R, C Resistance Logical "1"		12		kΩ	Resistance to V_{DD}, ±20%
	R, C Resistance Logical "0" (See Figure 1)		3		kΩ	Resistance to V_{SS} +20% −30%
	Output Current (See Note 2)	5			mA	Output Voltage = .8V W/V_{DD} = −7V

Notes: 1. Effect noted at Pin 15 to V_{SS}. 2. Output Voltage Pin 15 to V_{SS}. 3. All Voltages measured with respect to V_{SS}.

Figure 1. Serial Data Encoder



AMI®

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S2747/S2748

ENCODER/DECODER REMOTE CONTROL 2-CHIP SET

CONSUMER PRODUCTS

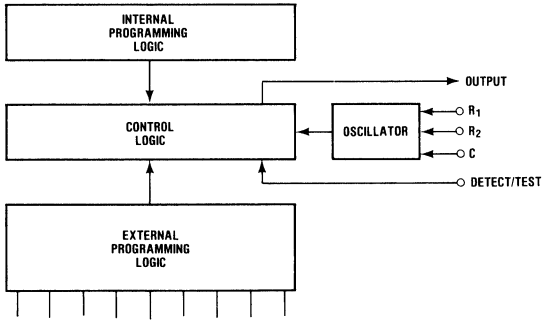
Features

- ☐ RC Oscillator Used—No Crystal Required
- ☐ 512 User Selectable Address Codes
- ☐ Low Power CMOS Encoder Operates on a Single Rail 9 Volt Supply
- ☐ Low Power CMOS Decoder Operates on a Single Rail 12 Volt Supply

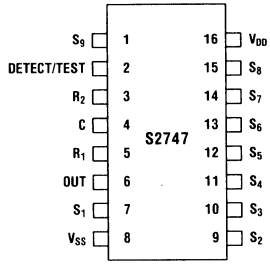
Applications

- ☐ Entry Access Systems
- ☐ Remote Engine Starting for Vehicles and Standby Generators
- ☐ Security Systems
- ☐ Traffic Control
- ☐ Paging Systems
- ☐ Remote Control of Domestic Appliances

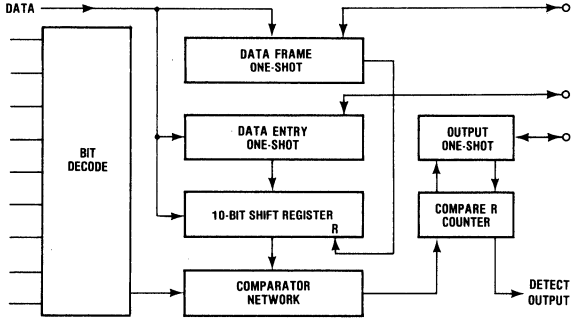
Block Diagram 2747 Encoder



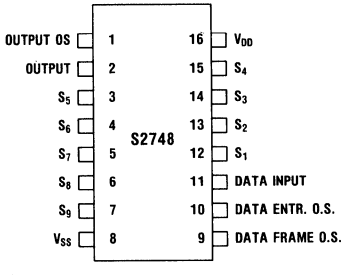
Pin Configuration 2747



Block Diagram 2748 Decoder



Pin Configuration 2748



General Description—Encoder/Decoder

This two-chip CMOS set includes a user-addressable serial data encoder for use in a simple low-power transmitter and a serial data decoder for use in a user-addressable low-power receiver. This chip set may be used with a variety of transmission media (RF, infrared, or hardwire). Up to 512 codes or addresses are externally selectable; this is done with the nine binary inputs on each device.

The serial data encoder outputs a train of ten pulses. The first pulse is a "marker" bit used to signal the decoder that a message is coming. The following nine pulses represent the encoded nine bits of binary information. The duration of the pulses output from the encoder is determined by a simple RC clock network. The encoder transmitter can be powered by a single 9-volt battery so that a single momentary push button will activate the encoder and transmitter. In the off position, there is no current flow.

The serial data decoder, in conjunction with a receiver amplifier, decodes the transmitted signal. The coded signal input is compared with the decoder's externally selected address. The serial decoder looks at the transmitted signal a minimum of four times before validating a good message and turning the receiver's detection output on.

The decoder has an on-chip output one-shot which is user programmed by an external RC combination. This one-shot is used to prevent the detection output from switching on and off too rapidly due to system noise.

Functional Description—Serial Data Encoder

The Serial Data Encoder is comprised of three sections: Oscillator, Programming Logic, and Control Logic. Specifically, it will provide a marker pulse and nine data pulses. This 10-bit message will be output from the encoder, then a DC logic "0" pulse will be output for a time corresponding to the length of the 10-bit message.

The encoder will continue to cycle the message and the logic "0" silence period as long as power is applied to it.

Each bit of the 10-bit message is four RC oscillator periods wide. The format of each bit is the same. First, a Logic "1" is output for one oscillator period. Then, the data (or marker) value is output for the next two oscillator periods. Lastly, a logic "0" is output for one oscillator period. Thus, Logic "1" for one period, data for two periods, and Logic "0" for the last period. After a 10-bit message (40 oscillator periods) has elapsed, there will be an equivalent period of silence (Logic "0") output from the encoder, as mentioned previously.

The marker bit is equivalent to a data bit with a value of Logic "1".

The RC oscillator circuit requires a maximum of three external components (see Figure 1). To directly drive the oscillator, let encoder Pins 3 and 4 float, and apply the direct drive signal to encoder Pin 5.

The typical R_1, R_2, and C components shown in Figure 2 provide an oscillator frequently of about 1ms.

External programming inputs connected to the device will be considered as a Logic "0". Unconnected external bit programming inputs are pulled up by the chip to a Logic "1".

A Logic "1" applied to "test detect", Pin 2, resets the internal logic and forces the encoder output to a Logic "0". After the "test detect" pin is back at a Logic "0", the encoder output will be a Logic "0" for 40 RC oscillator clock periods, then the 10-bit message will begin.

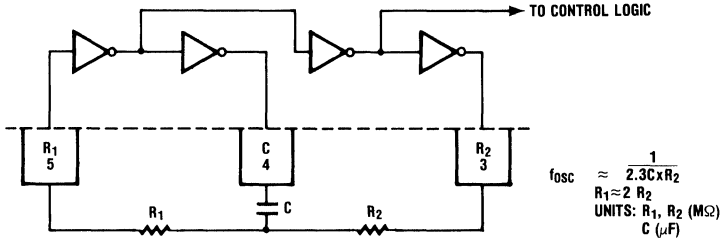
For portable operation, a 9V transistor battery with a 6V zener diode may be used for the DC voltage supply.

Functional Description—Serial Data Decoder

The Serial Data Decoder is comprised of four sections: Data Entry One-Shot, 9-Bit Digital Comparator, Good Detection Control Logic, and the Retriggerable Output One-Shot.

The Decoder is always on, looking for a "marker" pulse from the encoder. When a pulse is detected at the data input, the data entry one-shot clocks it into the first stage of a 10-bit shift register, after a user-selectable delay. As successive pulses are detected, they are similarly shifted into the shift register, with preceding shift register information shifted over one bit. As the marker bit is shifted into the tenth bit of the shift register, a comparison is made with the first nine bits of shift register information and the nine externally programmed address inputs. If a comparison is valid, a clock pulse is sent to the good detection counter logic. As mentioned in the Encoder Functional Description, a message lasts 40 encoder oscillator clock periods followed by 40 encoder oscillator clock periods of DC Logic "0". In the Decoder, it is necessary to clear the 10-bit shift register and associated logic after the message has been received and compared with the Decoder's external address bits. This is done using the

Figure 1. Serial Data Encoder RC Oscillator



data frame one-shot. The data frame one-shot provides a user-selectable delay from the end of a message until the shift register is reset. The typical RC components shown in Figure 2 provide data frame one-shot pulse width of about 10mS, while the components for the data entry one-shot will generate a 2ms pulse width clock delay during data entry.

The good detection counter circuit and the retriggerable output one-shot work together. Initially, as data begins to enter the Decoder, the output one-shot is refreshed to a Logic "1"; the detect output is off. As the output one-shot decays toward a Logic "0", the initial message is compared with the nine external address bits. If the comparison is true, a clock will increment the good detection control circuit. If four such comparisons occur, the detect output will turn on and the output one-shot will again be refreshed to a Logic "1". If less than four comparisons occur before the output one-shot decays to a Logic "0", the detect output will remain off, the output one-shot will not be refreshed to a Logic "1", and the good detection counter circuit will be reset. Once the detect output is turned on by four message detections in a single output one-shot period, it requires only one message detection per output one-shot period thereafter to keep the detect output continuously turned on. If no message detection occurs in a subsequent output one-shot period, the one-shot will decay to a Logic "0", turn off the detect output and reset the good detection counter circuit. The typical RC components shown in Figure 2 give an output one-shot period of about one second.

Also note that a logic inversion must take place external to the output of the Encoder before it is presented to the data input of the Decoder. Figure 2 shows a typical circuit to accomplish this.

S2747 Encoder Absolute Maximum Ratings

DC Supply Voltage	V_{DD} = +9V, V_{SS} = 0V
Input Voltage	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range (Ambient)	−35°C to +85°C
Storage Temperature Range (Ambient)	−55°C to +150°C
Lead Temperature (During Soldering)	300°C for Max. 10 sec.

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Preliminary Data Sheet **S10110**

ANALOG SHIFT REGISTER

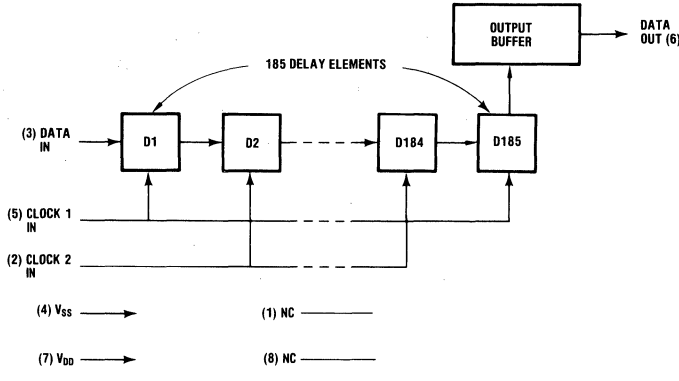
Features

- ☐ 185 Stage "Bucket Brigade" Delay Line
- ☐ Delays Audio Signals
- ☐ Accepts Clock inputs up to 500kHz
- ☐ Variable Delay
- ☐ Alternate to TCA 350

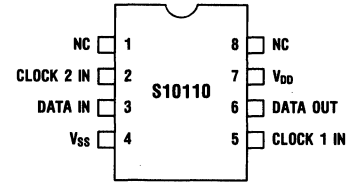
General Description

The S10110 analog shift register is a monolithic circuit fabricated with P-Channel ion-implanted MOS technology. The part differs from a digital shift register, which is capable of only digital input and output information, in that an audio signal is typically supplied as the data input to the analog register, and the output is the same audio signal delayed in time. The amount of signal delay is dependent on the number of bits of delay (185) and the frequency of the two symmetrical clock inputs. Since each negative-going clock edge transfers data from one stage to the next, the analog signal delay equals 185 ÷ 2 × clock frequency.

Block Diagram



Pin Configuration



Operation

Device operation may be understood by referring to Figure 1. This is an actual schematic diagram of the analog shift register, or "bucket brigade," showing typical external bias techniques.

Data In Input:

The analog signal, or audio signal, to be delayed is applied to pin 3. This input must be biased to a negative voltage of approximately – 8 volts, and two resistors may be used as a voltage divider to provide this bias. They must be chosen so that $(R_1) \pm (R_2) \div (R_1 + R_2)$ is less than 20kΩ. The input signal applied to this input through series capacitor C_{IN} may be as high as 6 volts peak-to-peak.

Clock 1 and Clock 2 Inputs:

Applied respectively to pins 5 and 2, Clock 1 and Clock 2 are two symmetrical non-overlapping negative-going clocks used to transfer the analog data along the 185 bit delay line. Although these clocks may have a duty cycle as low as 25% (i.e., each clock signal is at a negative level for 25% of its period), better output signals will be obtained with both clock duty cycles closer to 50%. It is important, however, that no overlap of the clock signals occurs at a level more negative than V_{SS} – 0.8 volts.

Referring again to Figure 1, it can be seen that when Clock 1 is negative, data is transferred from the data input to capacitor C1; likewise, data is transferred from each even-numbered capacitor to the capacitor to its right. When Clock 2 is negative, data is transferred from C1 to C2 and from each other odd-numbered capacitor to the capacitor to its right. In this manner, data is shifted from the input to C185 after a total of 185 negative clock pulses has occurred (i.e., 93 periods of Clock 1 and 92 periods of Clock 2).

Data Out Output:

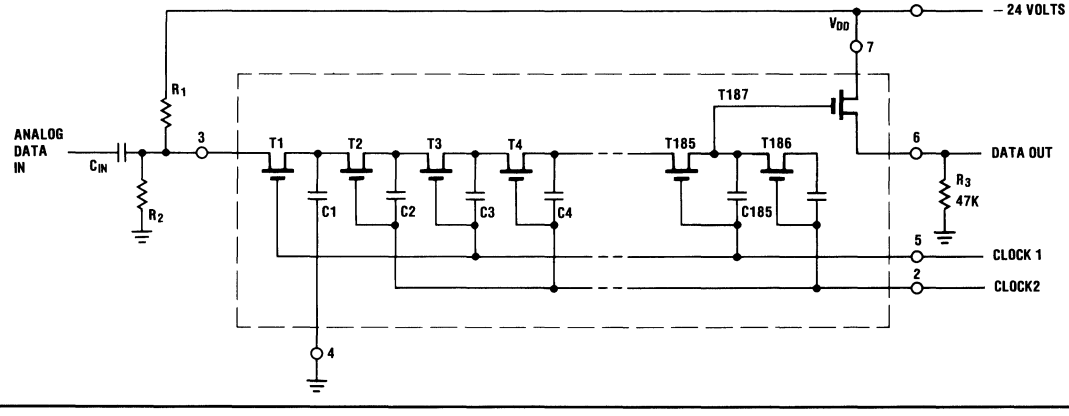
The output of the S10110 analog shift register is a single device, T187, with its drain at V_{DD} and its source connected to pin 6. If a 47K resistor to V_{SS} is supplied at this pin, T187 functions as a source follower.

Referring to Figure 3, it can be seen that the output potential during Clock 2 is a constant value near – 10 volts. When Clock 1 switches on (negative), the output instantaneously drops to a level of approximately – 30 volts; this is caused by the 20 volt swing of Clock 1 and C185. As Clock 1 remains on, device T185 transfers charge from C184 to C185, and the output voltage becomes more positive, depending on the charge previously stored on C184. It is during this part of Clock 1 that the output reflects the analog data stored on C1 185 bits earlier. Since the clock signal now appears on the output, it is necessary to apply the appropriate filtering to obtain the delayed analog signal.

Applications

- ☐ Delay of Audio Signals
- ☐ Rotating Speaker Simulation
- ☐ Electronic Chorus
- ☐ Electronic Vibrato
- ☐ String Ensemble
- ☐ Reverberation

Figure 1. Schematic Diagram and Pinouts of S10110



Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	+ 0.3V to − 30V
Operating temperature range	0°C to + 70°C
Storage temperature (ambient)	− 65°C to + 150°C

Electrical Characteristics

($0°C<T_A<70°C$; $V_{DD} = -24V \pm 2V$; $V_{SS} = 0V$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{CLK_L}	CLOCK 1 and CLOCK 2 Inputs Logic Level "0"	V_{SS}		$V_{SS} - 0.8$	V	No Overlap of Signals More Negative than $V_{SS} - 0.8V$
V_{CLK_H}	CLOCK 1 and CLOCK 2 Inputs Logic Level "1"	− 18		− 20	V	See Figure 2
t_{CLK_H}	Duration of CLOCK Logic "1" Level	$0.2 \times t_{CLK}$				See Figure 2
f_{CLK}	CLOCK Input Frequency	5		500	kHz	
V_{BIN}	Input Bias Voltage	− 7.5		− 8.5	V	See Figure 1
R_{BIN}	Resistance of the Bias Voltage Source at Input			20	KΩ	$R_{BIN} = (R1) \times (R2) \div (R1 + R2)$ See Figure 1
V_{DIN}	Signal Level at Data In Input			6	V (P-P)	
a	Analog Signal Attenuation			4	dB	
t_D	Signal Delay		$\frac{185}{2 \times f_{CLK}}$			
f_{3dB}	2dB Response Point		$0.1 \times f_{CLK}$			

Figure 1. Timing Diagram of Clock 1 and Clock 2 Signals

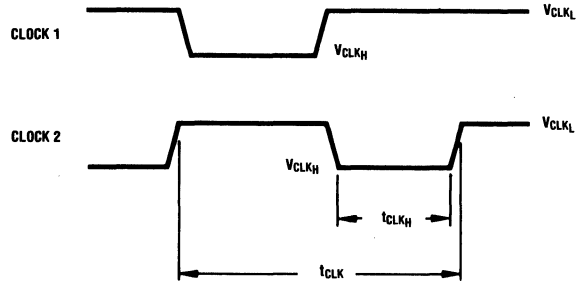
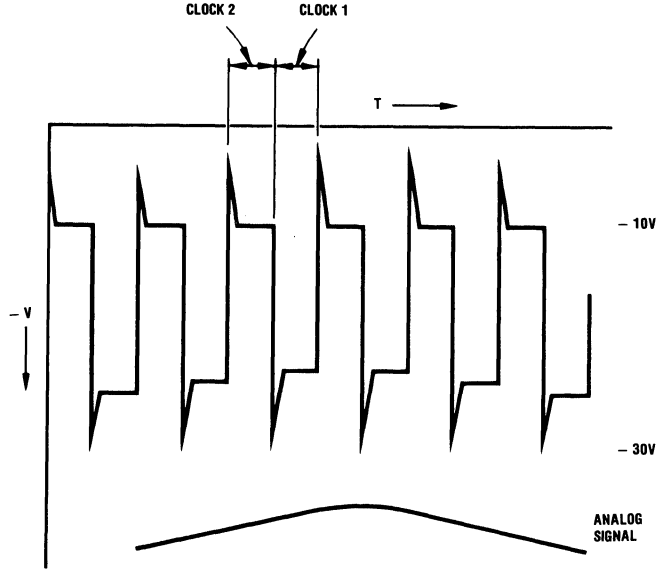


Figure 3. S10110 Output Waveform



Package Outline

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S10131

SIX STAGE FREQUENCY DIVIDER

Features

- ☐ Contains Six Binary Dividers
- ☐ Triggers on Negative-Going Edge
- ☐ High Impedance Inputs
- ☐ Schmidt Trigger on Inputs
- ☐ No Minimum Input Rise or Fall Time Requirements
- ☐ Low Impedance Push-Pull Outputs
- ☐ Low Power Dissipation
- ☐ Resettable

Applications

Electronic organ frequency generator, organ pedal frequency generator, electronic music synthesizers, N stage dividers, low frequency generation, binary counters.

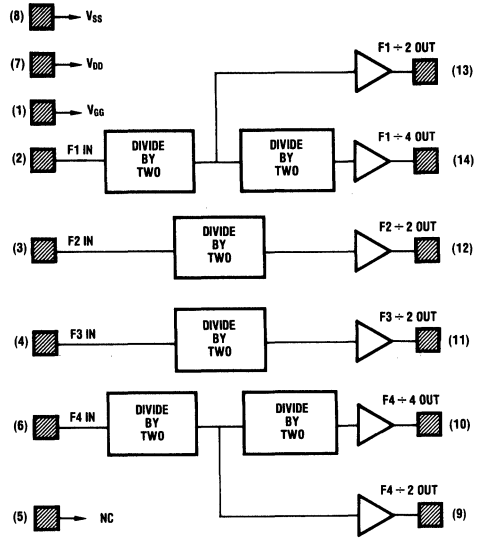
General Description

The S10131 is a monolithic frequency divider circuit fabricated with P-Channel ion-implanted MOS technology. The circuit provides six stages of binary division in a 2-2-1-1 configuration; the S10131 is ideally suited for tone generation in electronic organs.

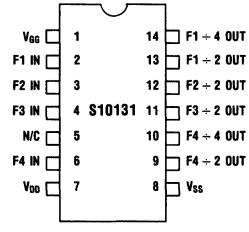
All inputs to the device are buffered to permit easy triggering of the divider stages. Outputs of each divider are buffered to provide low output impedance in both logic states to drive external circuitry as well as other dividers. The buffers have low standby current and are powered by V_{DD}. This voltage functions as a clamp voltage and thus sets the output amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

All divider outputs may be reset to a logic low level (V_{SS}) by momentarily applying a logic low level to the V_{GG} supply input. This is particularly desirable in some electronic organs in which phase relationships are important.

Block Diagram



Pin Configuration



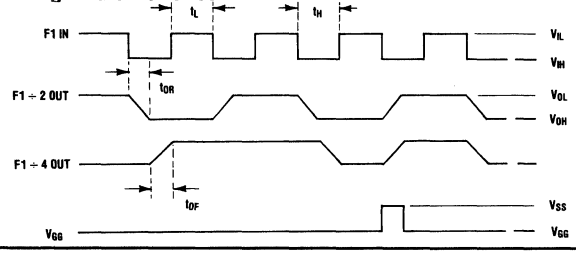
Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS}	+ 0.3V to − 20V
Voltage on V_{GG} Relative to V_{SS}	+ 0.3V to − 30V
Storage Temperature	− 55°C to + 150°C
Operating Temperature (ambient)	0°C to + 70°C

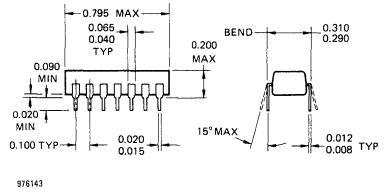
Electrical Characteristics ($0°C \leq T_A \leq 70°C$; V_{DD} = − 11V to − 16V; V_{GG} = − 25V to − 29V unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IL}	Input Clock Low	V_{SS} + 0.3		V_{SS} − 2.0	V	
V_{IH}	Input Clock High	V_{SS} − 8		V_{GG}	V	
f_{IN}	Input Clock Frequency	DC		250	kHz	
t_H, t_L	Input Clock On and Off Times	1.5			μs	
V_R	Voltage Applied to V_{GG} Input to Cause a Reset Condition	V_{SS}		V_{SS} − 0.5	V	
t_R	Duration of V_R to Cause Reset	10			μs	50% to 50% point
V_{OH}	Output High Level	− 11		V_{DD}	V	V_{DD} = − 12V V_{GG} = − 26V 5.5KΩ load to V_{SS}
V_{OL}	Output Low Level	V_{SS}		− 1	V	V_{DD} = − 12V V_{GG} = − 26V 5.5KΩ load to V_{DD}
C_{IN}	Input Capacitance		5	10	pF	Applies to clock inputs
t_{OR}, t_{OF}	Output Rise and Fall Time		1	2	μs	40pF load applied
I_{GG}	V_{GG} Supply Current		2	3	mA	V_{DD} = − 12V V_{GG} = − 26V No load
I_{DD}	V_{DD} Supply Current		5	7	mA	V_{DD} = − 12V V_{CC} = − 26V No load

Timing Characteristics



Physical Dimensions



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Preliminary Data Sheet **S10430**

DIVIDER-KEYER

Features

- ☐ 22 Keyboard Inputs
- ☐ 88 DC Keyer Circuits
- ☐ 34 Binary Dividers
- ☐ Provides Four Pitch Outputs
- ☐ All Key Inputs Sustainable for Percussion
- ☐ All Dividers Resettable
- ☐ Provides "Any Key Down" Indication
- ☐ Eliminates Multiple-Contact Key Switches

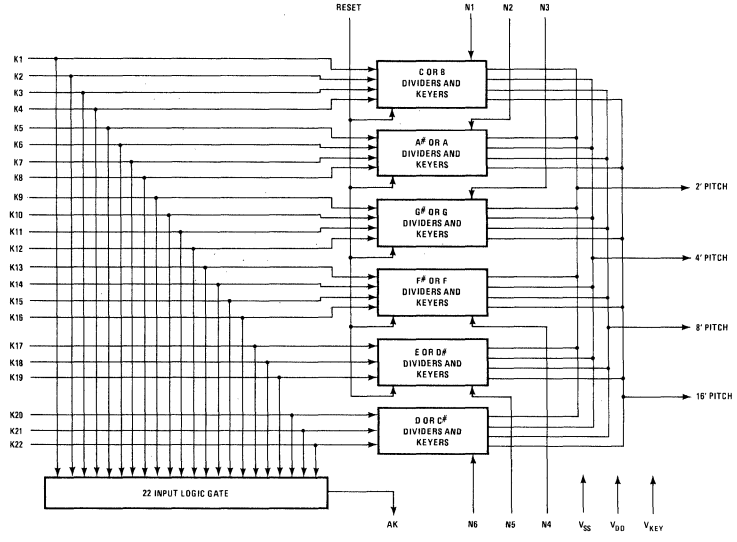
Typical Applications

- ☐ Generation and Keying of Musical Tones
- ☐ Standard Spinet Organ Keying (37 or 44 note keyboards)
- ☐ Keying of Sustained Tones
- ☐ Percussive Effects
- ☐ Generating Stair-stepped Waveforms
- ☐ Electronic Piano

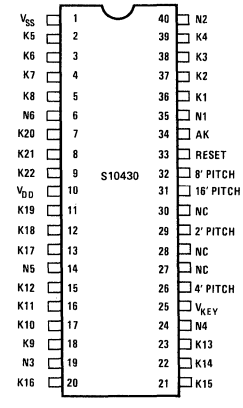
General Description

The S10430 divider-keyer is a monolithic integrated circuit fabricated with P-Channel ion-implanted MOS technology. It is intended for use in spinet organs or other electronic musical instruments having keyboards of up to 44 keys. This device has 22 key inputs, allowing all keying functions for a 44 note manual to be performed by two S10430 circuits. Each S10430 accepts six frequencies from a top octave synthesizer, such as an S50240, and provides squarewave outputs at 16 foot, 8 foot, 4 foot, and 2 foot pitches. For example, if a C key is depressed by itself a low C frequency appears at the 16 foot output, and a C frequency one octave higher appears at the 8 foot output; similarly, the 4 foot and 2 foot outputs provide C frequencies one and two octaves higher, respectively, than the C frequency of the 8 foot output. All appropriate frequency division is performed by the S10430, eliminating the need for external dividers.

Block Diagram



Pin Configuration



General Description (Continued)

The circuit also eliminates the need for multiple-contact key switches and discrete diode or transistor keyers. Because of the high input impedance of the MOS keyers used in this circuit, long sustain envelopes may be obtained by connecting low-value capacitors to the keying inputs.

Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS}	+ 0.3V to − 27.0V
Operating Temperature (ambient)	0°C to 70°C
Storage Temperature	− 65°C to 150°C

Electrical Characteristics

$0°C \leq T_A \leq 70°C$; $V_{SS} = 0V$; $V_{DD} = -12.6V$ to $-15.4V$; $V_{KEY} = -4.75V$ to $-5.25V$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IL}	Logic Low Level TOS and Reset Inputs	0.0		0.8	V	
V_{IH}	Logic High Level TOS and Reset Inputs	−4.2		V_{DD}	V	
t_r, t_f	Rise and Fall Times TOS Inputs			50	μsec	Measured between 10% and 90% points
V_{OL}	Logic Low Level AK Output		−0.5	−1.0	V	100KΩload to V_{DD}
t_{fo}	Transition of AK Output to 10% of V_{DD}			10	μs	100pF and 100KΩload to V_{DD}
F_T	Operating Frequency TOS Inputs	DC		50K	Hz	
D_O	Output Duty Factor	48		52	%	Measured between 10% and 90% points
I_{PA}	Peak Output Current Absolute (any pitch output with 1 keyer on)	350		650	μA	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -25V$ $T_A = 25°C$
I_P	Peak Output Current	85		115	$\%I_{AVE}$*	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -25V$ $T_A = 25°C$
I_P	Peak Output Current	50		75	$\%I_{AVE}$*	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -15V$ $T_A = 25°C$
I_P	Peak Output Current	0.5			μA	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -3.0V$ $T_A = 25°C$
I_P	Peak Output Current			0.5	μA	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -1.0V$ $T_A = 25°C$

*I_{AVE} is the average of all peak output current values within one circuit.

Functional Description

The S10430 Divider-Keyer circuit accepts six frequencies as inputs and uses these to clock six binary divider chains. Four of these chains consist of six binary dividers each and the remaining two have five. The six chains generate all frequencies necessary to obtain 2′, 4′, 8′, and 16′ pitches for half of a 44 key keyboard.

The outputs of the divider chains are routed to chopper keyer circuits like the one shown in figure 2. When a negative voltage is applied to any "K" input, four of these keyer circuits are turned on to route the appropriate frequencies to each of the four pitch outputs.

Figure 1:
Typical Time Constants For Sustain Keying

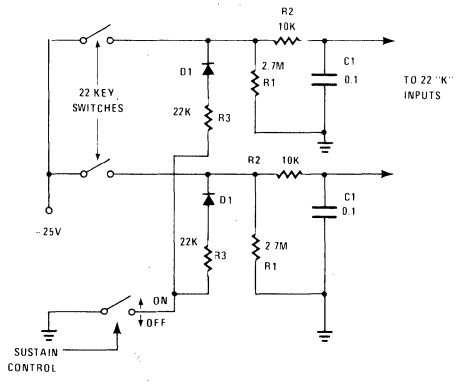
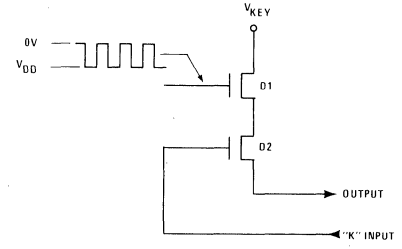


Figure 2:
Schematic Diagram of Chopper Keyer Circuit



N Inputs

Six of the twelve tempered scale frequencies are applied to the inputs N1 through N6. Typically, these frequencies would be six of the outputs of a top octave synthesizer, such as an S50240. In general, it doesn't matter which frequencies are applied to the N inputs, although this affects which keyboard keys should be connected to the K inputs. One exception to this arises from the fact that a 44 note keyboard contains more of some keys than others. Specifically, there are only three each of the keys, C#, D, D#, and E, but there are four each of the keys F, F#, G, G#, A, A#, and C. This results in the requirement that each of the two S10430 divider keyers in a system take two frequencies from the first group, and four from the second group. Stating this another way, the N1, N2, N3, and N4 inputs must have frequencies chosen from the group, F, F#, G, G#, A, A#, B, and C. The N5 and N6 inputs are chosen from the group, C#, D, D#, and E. The example in Figure 4 shows one divider keyer handling the notes, A, A#, B, C, C#, and D while the other does the keying for D#, E, F, F#, G, and G#.

Table 1: Relationship between K and N Inputs

INPUT	PIN NO.	OUTPUT (8′ PITCH)* PIN 32	INPUT	PIN NO.	OUTPUT (8′ PITCH)* PIN 32
K1	36	N1÷4	K12	15	N3÷32
K2	37	N1÷8	K13	23	N4÷4
K3	38	N1÷16	K14	22	N4÷8
K4	39	N1÷32	K15	21	N4÷16
K5	2	N2÷4	K16	20	N4÷32
K6	3	N2÷8	K17	13	N5÷4
K7	4	N2÷16	K18	12	N5÷8
K8	5	N2÷32	K19	11	N5÷16
K9	18	N3÷4	K20	7	N6÷4
K10	17	N3÷8	K21	8	N6÷8
K11	16	N3÷16	K22	9	N6÷16

*To determine outputs for 4′ pitch: multiply 8′ pitch output by 2.
To determine outputs for 2′ pitch: multiply 8′ pitch output by 4.
To determine outputs for 16′ pitch: multiply 8′ pitch output by

K Inputs

The twenty-two inputs are connected either directly to key switches or to an attack/decay circuit, such as the one shown in Figure 1. When a negative voltage is applied to any K input, four chopper keyer circuits are turned on, and the appropriate frequencies appear at the four pitch outputs. The amount of current at the output is determined by the voltage at the K input. As the voltage becomes more negative, more current appears at the output. This will be discussed further in the section on "Pitch Outputs."

Connection of the K inputs to the key switches is dependent on which frequencies are applied to which N inputs. Table 1 shows the relationship between the K and N inputs. If, for example, the top octave frequency F, 5588 Hz, is applied to the N2 input, K5 should then be connected to the highest F key on the keyboard, K6 to the next highest, K7 to the next, and K8 to the lowest F. If the highest F key is depressed, then N2÷4, or 1397 Hz would appear at the 8′ Pitch Output. At the same time, the 16′ pitch, 4′ pitch and 2′ pitch outputs would provide, respectively, 699 Hz, 2794 Hz, and 5588 Hz. An example of K and N input connections is given in Figure 4.

To control attack, decay, and sustain times, a circuit such as the one shown in Figure 1 may be used. When a keyswitch is closed, the K input charges to −25 volts through the time constant of R2 and C1. This causes the attack time to be about 1ms. If the sustain is on (sustain switch open), when the keyswitch is opened, the K input will charge slowly back to V_{SS} through the time constant of C1, R1, and R2. This results in a sustain envelope of 271ms. Longer sustains can be obtained with larger capacitors. If the sustain switch is closed, then the decay time is governed by the time constant of C1, R2, and R3 || R1. In this example, this non-sustain decay is about 3ms.

Pitch Outputs

The outputs labeled 2′ pitch, 4′ pitch, 8′ pitch, and 16′ pitch provide the appropriate frequencies for these four pitches depending on which K inputs have been selected. The selected frequencies of the outputs are shown in Table 1. The highest octave of frequencies is obtained directly from the N inputs. Although these top octave frequencies are buffered internally, their duty cycle depends on the duty cycle of the N inputs.

Each output is connected to the outputs of 22 of the chopper keyer circuits shown in Figure 2. The chopper device, D1, is much lower in impedance than the keyer device D2. The output voltage amplitude is dependent, therefore, on the ratio of D2 to the output load. Higher output sink resistor values result in higher output signal amplitudes. However, it is important to keep the output sink resistor low in order to minimize the effects of intermodulation distortion between keyers. Figure 3 shows a typical output waveform with a 100 sink resistor. Because of the need for a low value sink

resistor and the usual desirability of a high signal amplitude, it may be advisable in some cases to load the pitch outputs with operational amplifiers instead of resistors.

V_{KEY} Input

This supply input is used exclusively for the chopper keyer circuits (Figure 2). It is important that this be a low impedance supply in order to minimize intermodulation distortion between keyer circuits.

The voltage on the supply is kept low relative to V_{DD} and the K inputs to insure linear operation of the MOS keying circuits.

Reset Input

Applying a V_{SS} level to this input causes all binary dividers to be held in the reset state. A logic 1 applied to Reset causes the dividers to function normally. To prevent possible phase cancellation between upper and lower manual systems, it is suggested that an RC network be connected to this input so that the musical instrument will be locked into proper phase relationships when power is first applied. When in the reset condition, all chopper devices are turned on to facilitate testing.

AK Output

Whenever any key input is selected, the AK output is actively pulled to V_{SS} to indicated that a key is played. This output is open ended (i.e., no pull-up device is provided), and may be left unconnected if not needed.

Figure 3: Typical Keyer Output

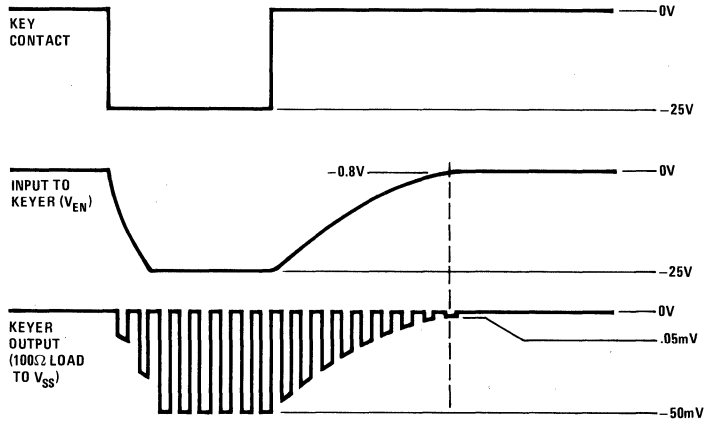
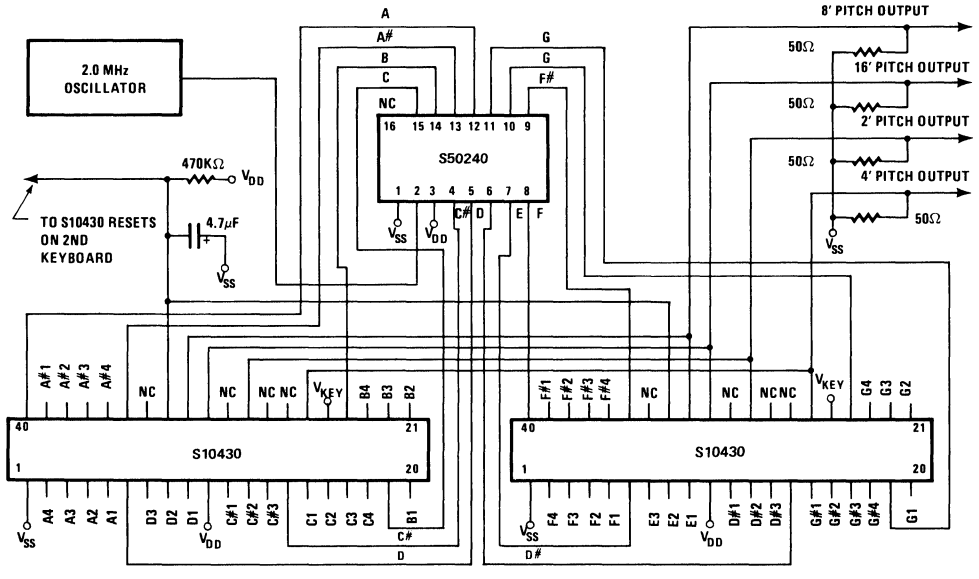


Figure 4: Schematic Diagram of Typical Divider—Keyer Application



V_{SS} = 0
V_{DD} = −14 VOLTS
V_{KEY} = −5 VOLTS

NOTE: ON ALL K INPUTS, THE LETTER REFERS TO THE KEY NAME, AND THE NUMBER TO ITS LOCATION ON THE KEYBOARD. FOR EXAMPLE, F1 WOULD BE THE LOWEST KEY ON A 44 NOTE MANUAL, AND C4 WOULD BE THE HIGHEST.

AMI

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S2567

RESETTABLE RHYTHM COUNTER

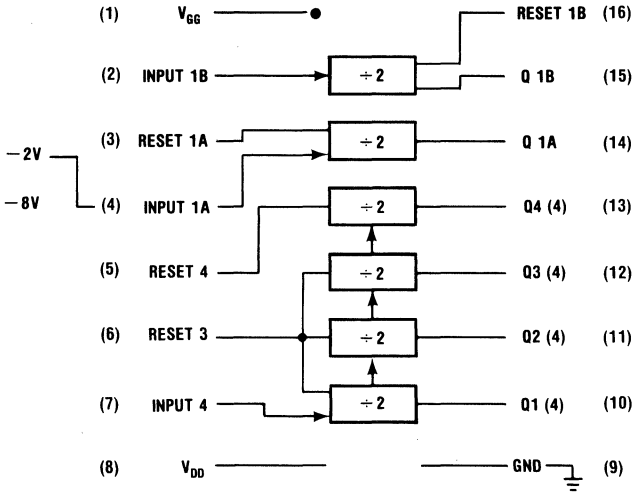
Features

- ☐ Pin for Pin Equivalent to GEM 567 and MC1181L
- ☐ Organ Rhythm Sections
- ☐ Portable Rhythm Sections
- ☐ Automatic Rhythm Organs

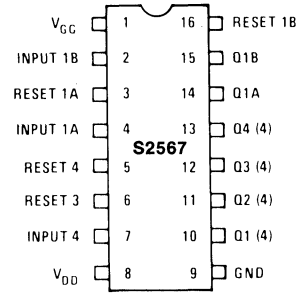
General Description

The S2567 Resettable Rhythm Counter is a six-stage asychronous binary counter designed for driving the count-address inputs of the S2566 Rhythm Generator. The internal partitioning and multiple-reset capability of the S2567 permit simultaneous generation of different meter rhythms. The S2567 Resettable Rhythm Counter is made by P-channel enhancement mode technology and is supplied in a 16-lead dual in-line package.

Block Diagram



Pin Configuration



Absolute Maximum Ratings: @25°C, unless otherwise noted

Logic Supply Voltages:

V_{GG}	+ 0.3V to − 33V
V_{DD}	+ 0.3V to − 25V
V_I Trigger Voltage	+ 0.3V to − 18V
P_D Power Dissipation	250mW
T_S Storage Temperature	− 55°C to + 100°C
T_A Operating Temperature	− 0°C to + 60°C

Dynamic Characteristics: $T_A = -25°C$

Operating Voltage Ranges:

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{GG}		− 25	− 27	− 29	V
V_{DD}		− 14	− 15	− 16	V
Inputs: (Pins 2 thru 7, and 16)					
f_I	Input Frequency	DC		100	kHz
V_{IH}	Logic "0" Level	+ 0.3		− 2.0	V
V_{IL}	Logic "1" Level	− 8.0		− 18	V
t_r, t_f	Rise and Fall Times			25	μs
PW_I	Pulse Width	2			μs
I_{IL}	Leakage Current ($V_{ILT} = -18V$)			1	μA
Outputs: (Pins 10 thru 15, each loaded 20K to GND and 20K to V_{DD})					
V_{OH}	Logic "0" Level	0		− 1.5	V
V_{OL}	Logic "1" Level	− 9.0		V_{DD}	V
Reset Propagation Delay				2.0	μA
Supply Currents: (no output loads)					
I_{GG}			4	6	mA
I_{DD}				20	μA

AMI®

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S2688

DIGITAL NOISE GENERATOR

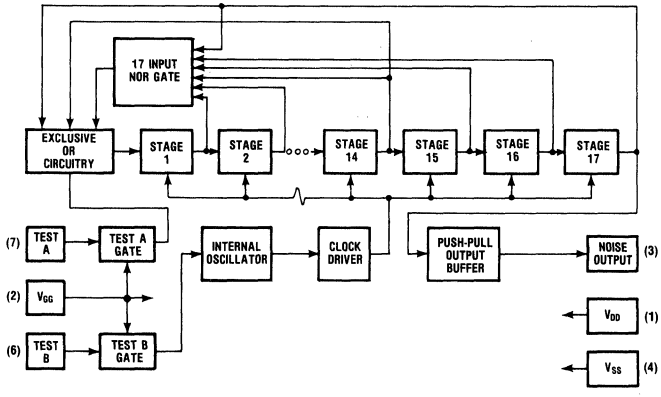
Features

- ☐ Internal Oscillator
- ☐ Consistent Noise Quality
- ☐ Consistent Noise Amplitude
- ☐ Zero State Lockup Prevention
- ☐ Zeros Can Be Externally Forced Into the Register
- ☐ Oscillator Can Be Driven Externally
- ☐ Operates With Single or Dual Power Supplies
- ☐ Eliminates Noise Preamps
- ☐ Alternate to MM5837

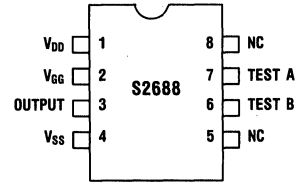
General Description

The S2688 noise generator circuit is fabricated in P-Channel ion implanted MOS technology and supplied in an eight-lead dual in-line plastic package. The device contains a 17-bit shift register which is continuously clocked by an internal oscillator. Exclusive OR feedback from the 14th and 17th stages causes the register to generate a pseudo-random noise pattern, and an internal gate is included to prevent the register from reaching an all zero lockup state. To facilitate testing, the device can be easily clocked by an external source.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Positive Voltage On Any Pin ..... V_{SS} + 0.3V
Negative Voltage On Any Pin Except V_{GG} ..... V_{SS} − 28V
Negative Voltage On V_{GG} Supply Pin ..... V_{SS} − 33V
Storage Temperature ..... − 65°C to + 150°C
Operating Ambient Temperature ..... 0°C to + 70°C

Electrical Specifications (0°C<T_A<70°C; V_{SS} = 0 Volts; V_{DD} = − 14.0V ± 1.0V; V_{GG} = 27.0V ± 2V; unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output Logic 1 Level	V_{SS} − 1.5		V_{SS}	Volts	20KΩ Load to V_{DD}
V_{OL}	Output Logic 0 Level	V_{DD}		V_{DD} + 1.5	Volts	20KΩ Load to V_{SS}
V_{OL}	Output Logic 0 Level	V_{DD}		V_{DD} + 3.5	Volts	20KΩ Load to V_{SS} $V_{GG} = V_{DD} = -14V \pm 1.0V$
Z_{IN}	Input Impedance (Test Inputs)		10		pF	
I_L	Leakage Current (Test Inputs)			500	nA	
f_o	Frequency of Internal Oscillator		100		kHz	
I_{DD}	V_{DD} Supply Current			4.0	mA	No Output Load
I_{GG}	V_{GG} Supply Current			500	μA	
f_{TEST}	Test Frequency	80		105	kHz	

Operation

The S2688 is a 17-bit digital shift register driven by an internal oscillator circuit. Outputs from the 14th and 17th stages are connected to an Exclusive OR circuit whose output provides the data input for the register. The 17th stage of the register is connected to a push-pull buffer, which is the circuit's output. This output provides continuous constant amplitude pseudo-random noise; that is, for any time slot, ones and zeroes have an almost equal probability of occurrence.

Typical Applications

- ☐ Percussion Instrument Voice Generators for Rhythm Units
- ☐ Electronic Music Synthesizers
- ☐ Simulated Pipe "Wind" Noise
- ☐ Acoustics Testing

Power Supplies

The S2688 noise generator may be operated with either one or two power supplies. In applications where a high output drive level is not critical, or where the output is loaded with a resistive load connected to V_{DD}, it is possible to operate the device from a single supply voltage; in this case, the V_{GG} supply pin is connected to the V_{DD} supply voltage. If a low impedance logic "0" level output is required, this can be achieved by connecting the V_{GG} supply pin to a more negative voltage.

Zero State Lockup Prevention

If the outputs of all 17 stages of the shift register were simultaneously to reach a "0" logic level, and no logic were provided to prevent this state from occurring, then the register would remain in the "all-zero" state.

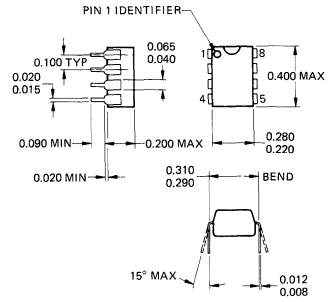
In this condition, the output would lockup and remain at a logic "0" level. This situation could occur when power is initially applied, or when triggered by noise spikes. To prevent this condition, a 17 input NOR gate is provided internally to decode the "all-zero" state and feed a logic "1" level into the register's data input.

Test Inputs

The S2688 has been designed to facilitate testing of the part. In the normal mode of operation, pins 6 and 7 are not used and appear to be open circuits. However, when the V_{GG} pin is connected to V_{SS}, these pins become test pins. Pin 7 (Test A) is used to force zeroes into the register, and pin 6 (Test B) becomes the clock input, driving the internal oscillator network. During the entire test period a 20KΩ load must be tied to V_{DD}.

Package Outline

8-Pin Plastic



AMI®

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S50240/S50241/S50242

TOP OCTAVE SYNTHESIZER

Features

- ☐ Single Power Supply
- ☐ Broad Supply Voltage Operating Range
- ☐ Low Power Dissipation
- ☐ High Output Drive Capability
- ☐ S50240 — 50% Output Duty Cycle
- ☐ S50241 — 30% Output Duty Cycle
- ☐ S50242 — 50% Output Duty Cycle

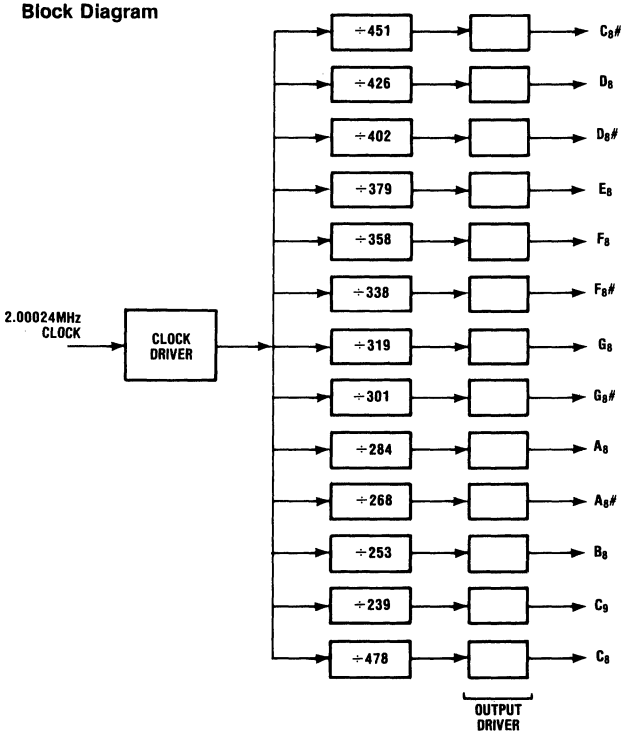
General Description

The S5024 is one of a family of ion-implanted, P-Channel MOS, synchronous frequency dividers.

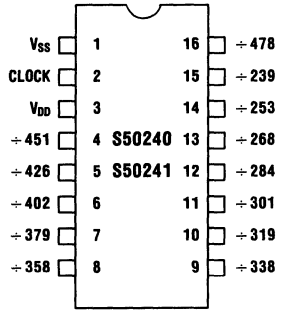
Each output frequency is related to the others by a multiple $12\sqrt{2}$ providing a full octave plus one note on the equal tempered scale.

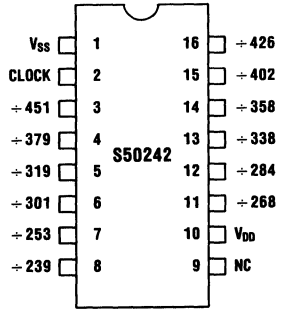
Low threshold voltage enhancement-mode, as well as depletion mode devices, are fabricated on the same chip allowing the S5024 family to operate from a single, wide tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 360mW of power. The circuits are packaged in 16-pin plastic dual-in-line packages.

Block Diagram



Pin Connections





RFI emination and feed-through are minimized by placing the input clock between the V_{DD} and V_{SS} pins. Internally the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise time under no load conditions to reduce the R.F. harmonic content of each output signal.

Absolute Maximum Ratings

Voltage On Any Pin Relative to V_{SS} ..... +0.3V to −20V
Operating Temperature (Ambient) ..... 0°C to 50°C
Storage Temperature (Ambient) ..... −65°C to +150°C

Recommended Operating Conditions ($0°C \leq T_A \leq 50°C$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Figure
V_{SS}	Supply Voltage	0		0	V	
V_{DD}	Supply Voltage	−11.0	−14.0	−16.0	V	

Electrical Characteristics ($0°C \leq T_A \leq 50°C$; V_{DD} = −11 to −16V unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Figure
V_{IL}	Input Clock, Low	0		−1.0	V	Figure 1
V_{IH}	Input Clock, High	−10.0		V_{DD}	V	Figure 1
f_1	Input Clock Frequency	100	2000.240	2500	kHz	
t_r, t_f	Input Clock Rise and Fall Times 10% to 90% @ 2.5MHz			50	nsec	Figure 1
t_{ON}, t_{OFF}	Input Clock On and Off times @ 2.5MHz		200		nsec	Figure 1
C_I	Input Capacitance		5	10	pF	
V_{OH}	Output, High @ 1.0mA	V_{DD} +1.5		V_{DD}	V	Figure 2
V_{OL}	Output, Low @ 1.0mA	V_{SS} −1.0		V_{SS}	V	Figure 2
t_{ro}, t_{fo}	Output Rise and Fall Times, 500pF Load 10% to 90%	250		2500	nsec	Figure 3
t_{ON}	Output Duty Cycle—S50240, S50242 S50241		50 30		% %	
I_{DD}	Supply Current		14	22	mA	Outputs Unloaded

Figure 1. Input Clock Waveform

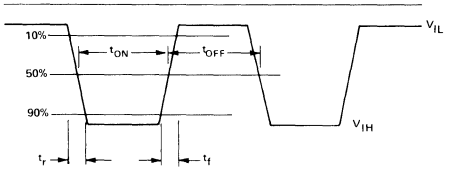


Figure 2. Output Signal DC Loading

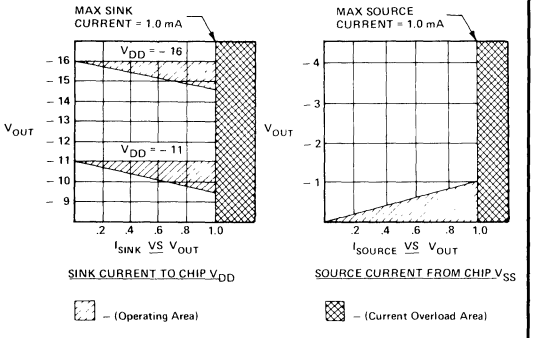
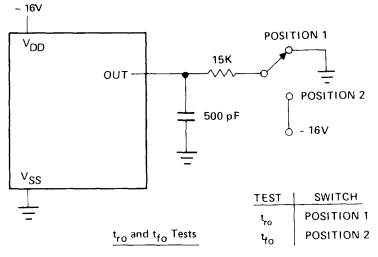
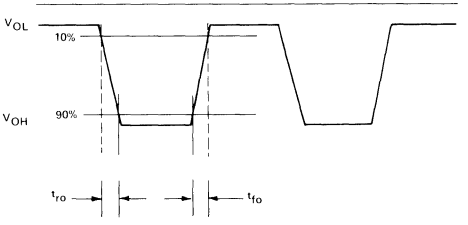


Figure 3. Output Rise and Fall Times





S4003

AUTO CLOCK

Features

- ☐ 12 Hour, 4 Digit Auto Clock
- ☐ Elapsed Time Counter (resettable, range to 99 hours)
- ☐ Calendar (4-year calendar with pin option for European date/month reversal)
- ☐ Ignition-Sensing Display Cut-off (to reduce battery drain when the auto is not operating)
- ☐ Crystal Input Accuracy (uses inexpensive 4.194mHz crystal)
- ☐ Direct Display Drive (4-digit vacuum fluorescent displays, 24 Volts)

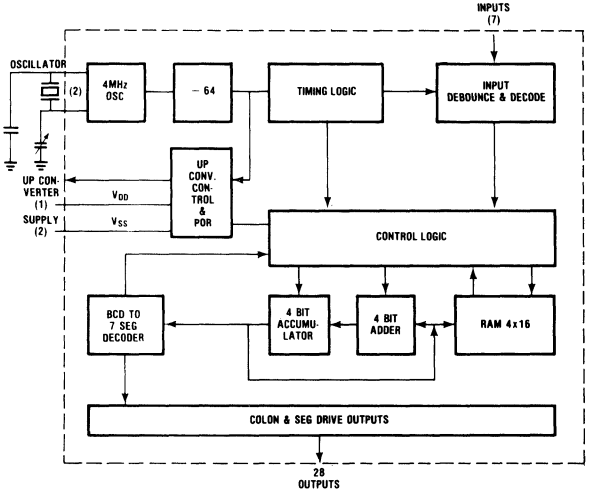
Applications/Markets

- ☐ Automotive
- ☐ Avionics
- ☐ Marine
- ☐ Portable Clocks
- ☐ Industrial

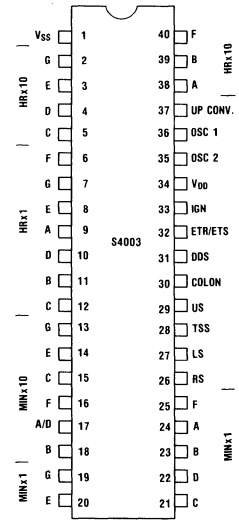
General Description

The S4003 Auto Clock is a PMOS integrated circuit which has found wide application in auto, avionic and marine applications as a portable or dashboard clock and as an industrial timer.

Block Diagram



Pin Configuration



A functional description of the inputs/outputs and registers follows:

1. Set Inputs—Left digits set and right digits set will index the selected register at a 2Hz rate. Indexing either input will not upset the unselected digits.

2. Time Set Select—Enables set inputs to the timekeeping register. When updating hours, the minutes display will blank out and MX1 digit will display A or P. Minutes will update in a normal manner and reset seconds to zero. Seconds will restart on release of the time set select line. When deselected, the time will continue to be displayed for 5 seconds ± 1 seconds. AM and PM indications will switch on the transfer from 11:59 to 12:00.

3. Elapsed Time Select—Displays contents of elapsed time register while active. Left set will stop E.T. accumulation, right set or E.T. reset will restart accumulation of E.T.

4. Elapsed Time Reset—Displays, zeros, and restarts the elapsed time register.

5. Date Select—Displays the contents of the calendar register and enables set inputs. When deselected, the date will continue to be displayed for 5 ± 1 seconds. If elapsed time select is true, the 5 seconds counter shall be inhibited.

6. Ignition Off—When ignition is off, all set inputs will be inactive and display outputs will be turned off. When ignition is turned on, the date will display for 5 seconds then revert to time.

7. Time Register—The time register is a 12 hour register. The time register shall be normally selected with no control inputs selected. When time set select and ignition sense are both true, the 5 seconds date counter shall be inhibited.

8. Elapsed Time Register—The elapsed time register shall be capable of accumulating time up to 99 hours and 59 minutes. The display shall be minutes and seconds to 59 minutes and 59 seconds then switch automatically to hours and minutes format. After 99 hours and 59 minutes, the elapsed time will reset to 00:00 and continue accumulation in minutes and seconds format as detailed above. All leading zeros shall be displayed.

9. Date Register—The date register will be a 4 year "smart" calendar. A month/date and date/month format will be pin selectable. The set inputs shall index the appropriate left or right digits regardless as to which format is selected. Date will advance on the transfer from PM to AM.

Date Setting—When date of month is set, the number will advance to the maximum allowed for the particular month being displayed. Further advance will reset the date to "01" and continue advancing as before. When the month is being set and the date is greater than that allowed for that month, (i.e., 02 30), the next timekeeping switch from PM to AM will advance the month and set the date to "01" (i.e., 03 01).

10. All registers are to be independent, i.e., setting time will not index calendar.

11. All registers will continue to accumulate while ignition is off.

12. Colons shall be non-flashing and displayed in the time display and elapsed time modes. Colons shall be extinguished in the date display mode.

13. On initial power up or in case of battery disconnect, the display shall read 0:00 on all functions until time is set. Voltage rise time to 10 volts will be greater than 10 mseconds.

14. Register Preference—If more than one register for display is selected at one time, time will have preference over date, date will have preference over elapsed time.

15. Illegal Conditions—If either date, time, or E.T. reset inputs are true at the same time, the clock display shall blank. All set inputs will be disabled while the clock is in an illegal mode.

16. Test Condition—When date select, elapsed time select, time set select, and both right and left set inputs are true, the clock may enter a test mode.

17. Switch Debounce Protection—All setting inputs shall be protected against switch debounce for a period of 13mseconds min.

Absolute Maximum Ratings

Positive voltage on any pin ..... V_{SS} + 0.3V
Negative voltage on any pin ..... V_{SS} – 30.0V
Storage Temperature ..... – 60°C to + 150°C
Operating Temperature ..... – 40°C to + 85°C

S4003 Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions
V_{SS} Supply Voltage Outputs Operational	9	20	24	Volts	V_{DD} = GND
V_{SS} Supply Voltage No Loss of Memory	7		24	Volts	V_{DD} = GND
V_{SS} Supply Voltage	7		24	Volts	Voltage to be ramped up from 0 volts (time constant 10ms from 0 to 10 volts)
I_{SS} Supply Current		5	6.5	mA	V_{SS} = 12V 25°C
No Output Loads		10	15	mA	V_{SS} = 20V
FO Crystal Frequency		4.194304		MHz	
Fc Converter Frequency		65.536		KHz	
Converter Frequency Start w/Ignition Sense Off		8		Volts	V_{DD} = GND
Input Voltage					
V_{IH}	V_{SS} – 1		V_{SS}	Volts	
V_{IL} (Except Ignition Sense)	V_{DD}		V_{DD} + 1	Volts	
Ignition Sense (On)	+ 5.0			Volts	V_{SS} = 9 to 20V
(Off)			+ 1.0	Volts	V_{DD} = GND
Output Currents					
Segment (Single) I_{OL}	0.5			mA	$V_{OH} = V_{SS} - 1$
I_{OH}	1.0			µA	Leakage to V_{DD} (Output Off)
(A&D MX10) I_{OL}	1.0			mA	$V_{OH} = V_{SS} - 1$
I_{OH}	1.0			µA	Leakage to V_{DD} (Output Off)
Converter I_{OH}	3.0			mA	$V_{SS} - 2$, V_{SS} = 18V
	1.0			mA	$V_{SS} - 2$, V_{SS} = 7V

AMI

A Subsidiary of Gould Inc.

S2709A

VACUUM FLUORESCENT DIGITAL CLOCK FOR AUTOMOTIVE APPLICATIONS

CONSUMER PRODUCTS

Features

- ☐ Uses Inexpensive 4MHz Crystal
- ☐ Direct Drive to Green or Blue Vacuum Fluorescent Display
- ☐ Low Standby Power Dissipation When Display is Switched Off With Ignition
- ☐ Variable Brightness Tracks Other Dash Lights

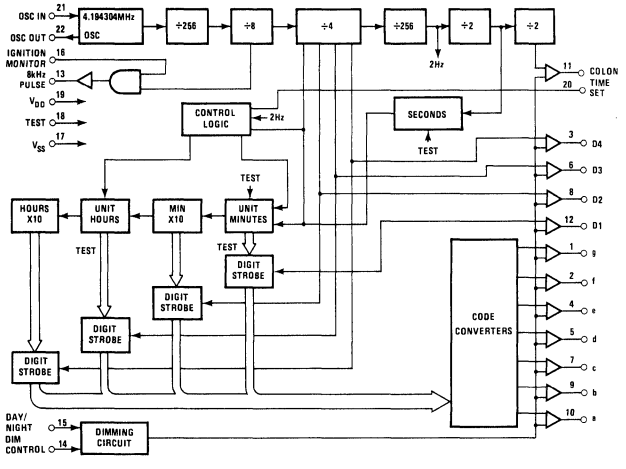
Applications

- ☐ In Dash Automobile Clocks
- ☐ Tape Players, CB Radio Units
- ☐ Automotive After Market Clocks
- ☐ Aircraft, Marine Panel Clocks
- ☐ Portable Instrumentation Clocks

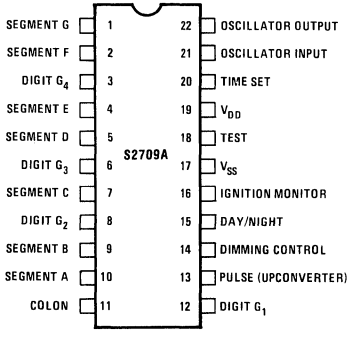
Functional Description

The S2709A vacuum fluorescent clock is a monolithic MOS integrated circuit utilizing P-Channel low threshold, enhancement mode and ion-implanted depletion mode devices. The circuit interfaces directly with 4 digit multiplexed vacuum fluorescent displays and requires only a single nominal 12V power supply. The timekeeping function operates from a 4MHz crystal controlled input. The display format is 12 hours with colon and leading zero blanking. An up-converter output is provided by the circuit to generate increased display driving voltage. A brightness control input allows variation of the display intensity. An ignition monitor input controls the upconverter operation and inhibits time setting. The S2709A is normally supplied in a 22-lead plastic dual-in-line package.

Block Diagram



Pin Configuration



Operational Description

Refer to the block diagram and Figure 1, Typical Application.

Oscillator Input (Pin 21) and Output (Pin 22) — The crystal controlled oscillator operates at a frequency of 4.194304 MHz to increase accuracy and reduce external component costs due to the less expensive quartz crystal. The frequency is controlled by a quartz crystal and fixed capacitor upconverter output (pin 13). This method allows accurate frequency tuning of the crystal oscillator without loading down the oscillator circuit. The feedback and phase shift resistors are integrated to further reduce external component costs. The internal oscillator inverter drives a counter chain that performs the timekeeping function.

Time Setting Input (Pin 20) — To prevent tampering, time setting is inhibited until the ignition monitor (pin 16) is held at a logic high level (V_{SS}).

Normal timekeeping is provided by allowing the time set pin to float externally. (Unloaded, this pin will alternate between V_{DD} and V_{SS} in phase with the unit minutes digit strobe [pin 12] during normal timekeeping.) If the time set pin is held at a logic high level (V_{SS}), the minutes counter advances at a 2Hz rate without carry to hours. If the time set pin is held at a logic low level (V_{DD}) the hours counter advances at a 2Hz rate.

It is possible to reset the hours, minutes and internal seconds counter by applying a logic low level (V_{DD}) to the test input (pin 18) during the time that the ignition monitor input is at a logic low level (V_{SS}). This reset state (time 1:00) is used for testing purposes.

Upconverter Pulse Output (Pin 13) — The clock circuit and vacuum fluorescent display drive normally operate at 25V when the ignition monitor pin is held at a logic high level (V_{SS}). The automobile battery voltage (12V) is doubled by an external upconverter circuit triggered by an 8kHz output pulse having a 28% duty cycle. The voltage, whether 12V or 25V, is applied to the circuit via the V_{SS} input (pin 17).

When the ignition monitor pin is held at a logic low level (V_{DD}) the upconverter is disabled. This drops the V_{SS} supply to 12V allowing the clock to operate while the display drive is decreased, lowering power dissipation. As the battery voltage drops (due to engine starting, cold temperature, or aging) timekeeping is maintained down to approximately 7V with no loss of the memory down to 5V. However, below 10V the upconverter will not be inhibited by the ignition monitor input.

Note that low standby power dissipation (60mW typical @ V_{SS} = 12V, and no output loads) is accomplished by turning off the filament voltage to the display when the auto ignition switch is off.

Ignition Monitor (Pin 16) — Along with preventing the already mentioned time setting function, the ignition monitor when held at a logic low level (V_{DD}) inhibits the 8kHz upconverter output pulse (pin 13) as long as the supply (V_{SS}) is above 10V. This pin is normally connected to the auto accessory switch.

The ignition monitor input can be protected against power supply transients by using 47KΩ external series resistance (See Figure 1).

Day/Night Display Control Input (Pin 15) — As seen in Figure 2, the display brightness is controlled via both pin 15 and the dimming control input (pin 14). The day/night input is connected to the automobile parking or headlights switch such that when these lights are off (V_{IN} low) the decoded segment and the digit outputs are from V_{SS} to V_{SS} – 2.0 volts. When the parking or headlights are switched on (V_{IN} high) the internal day/night logic enables the dimming input to control the segment and digit output voltage and brightness by allowing adjustable current to flow as controlled by the dash lights rheostat.

The day/night input can be protected from power supply transients by using 47KΩ external series resistance (See Figure 1).

Display Dimming Control Input (Pin 14) — The display dimming input is connected to the automobile dashboard light dimming rheostat through a series resistor. This allows the fluorescent display to track the dimming characteristics of the incandescent dashboard light (See Figure 2). The display dimming control is inhibited unless the day/night input (pin 15) is held at a logic high level (V_{SS}).

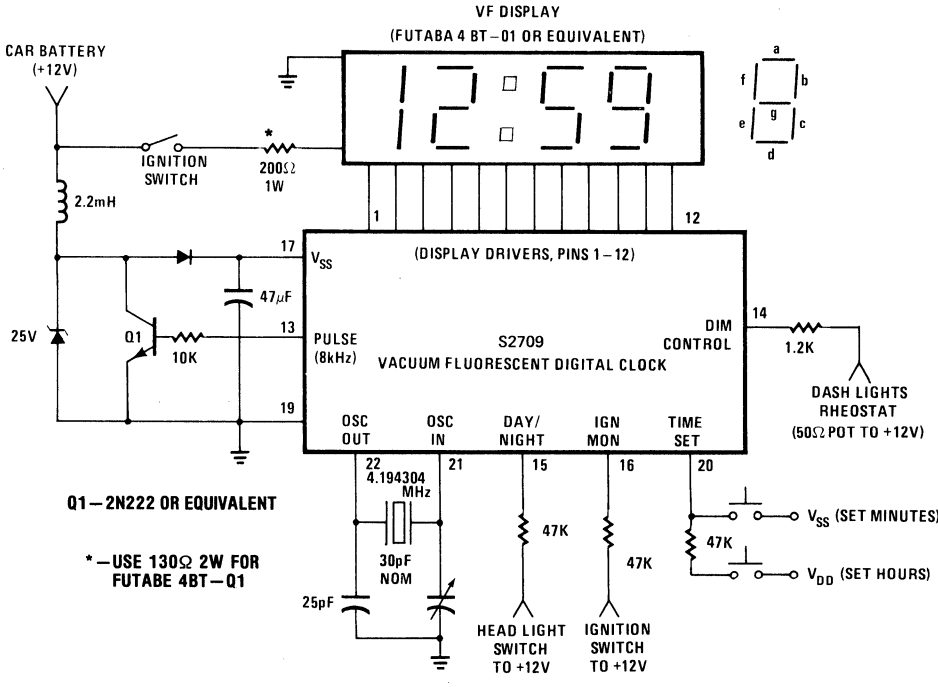
Display Drivers (Pins 1 through 12) — The 12 hour display format is comprised of four digits with leading zero blanking and a flashing colon. Each digit contains 7 segments with individual segments coded in the conventional manner (See Figure 1). The display is multiplexed with each digit output (G1, G2, G3 and G4) being strobed for a time period of approximately 0.5mS. Figure 3 shows the minimum output current as a function of output voltage for the digit (grid) and segment outputs.

The colon output (pin 11) is designed to have an unobtrusive flash while still indicating that the clock is functioning normally. The colon flash is accomplished in a 2 second period of 1-1/2 seconds on the 1/2 second off.

Electrical Characteristics

Symbol	Characteristics/Conditions	V_{DD} V	0°C to 70°C Min.	0°C to 70°C Typ.	0°C to 70°C Max.	Unit
V_{SS}	Operating Supply Range $V_{DD} = 0.0V$ (Refer to Upconverter Pulse Output)		7.0		28	V
I_{SS}	Supply Current	12			12	mA
	(No Loads On Outputs)	25			15	mA
	Oscillator Frequency			4.194304		MHz
	Display Outputs					
	Multiplex Rate			512		Hz
	Duty Cycle (Each Digit Per Cycle)			18.8		%
	Output Current (Day/Night = LOW)					
I_{OH}	Digits, $V_{OH} = 24V$	25			−6.0	mA
I_{OL}	$V_{OL} = 2V$	25	40			μA
I_{OH}	Segments & Colon, $V_{OH} = 24V$	25			−1.5	mA
I_{OL}	$V_{OL} = 2V$	25	10			μA
	Output Voltage (V[Pin 14]—V(Digit or Seg)					
	Day/Night = High, V(Pin 14 ⩾ /4V)					
ΔV_O	Digits ($R_L = 8.2K\Omega$ to V_{DD})	25			1	V
ΔV_O	Segment ($R_L = 100K\Omega$ to V_{DD})	25			1	V
	Upconverter Pulse Output					
	Pulse Frequency			8192		Hz
	Duty Cycle			25		%
	Output Current					
I_{OH}	$V_{OH} = 8V$	10			−1.5	mA
I_{OH}	$V_{OH} = 23V$	25			−3.0	mA
I_{OL}	$V_{OL} = 1V$	25	6.0			μA
	Time Set Input/Output					
	Input Voltage (No Load)					
V_{IH}	High	25	24		1	V
V_{IL}	Low	25	0		1	V
	Output Current					
I_{OH}	$V_{OH} = 18V$	25	−6.0		−2.0	mA
	Output Frequency			512		Hz
	Duty Cycle			25		%
	Ignition Monitor Input and Day/Night Input					
	Input Voltage					
V_{IH}	High	9.0 to 25	6.5		V_{SS}	V
V_{IL}	Low	9.0 to 25	0		2.0	V
I_{IH}	Input Current (Pull Down) $V_{IH} = 12V$	25	2		20	μA

Figure 1. Typical Application



S4036

GENERAL PURPOSE A/D CONVERTER AND DIGITAL SCALE CIRCUIT

Features

- ☐ On-Chip Voltage Regulator
- ☐ On-Chip Low Supply Detection
- ☐ On-Chip LED Display Drivers
- ☐ Pin Selectable Sensitivity
- ☐ Linearity ± 5 LSB/3000 Bits
- ☐ Repeatability ± 3 LSB/3000 Bits

Applications:

- ☐ Low Cost ADC
- ☐ Digital Scale
- ☐ Digital Thermometer
- ☐ Digital Voltmeter
- ☐ Digital Light Meter

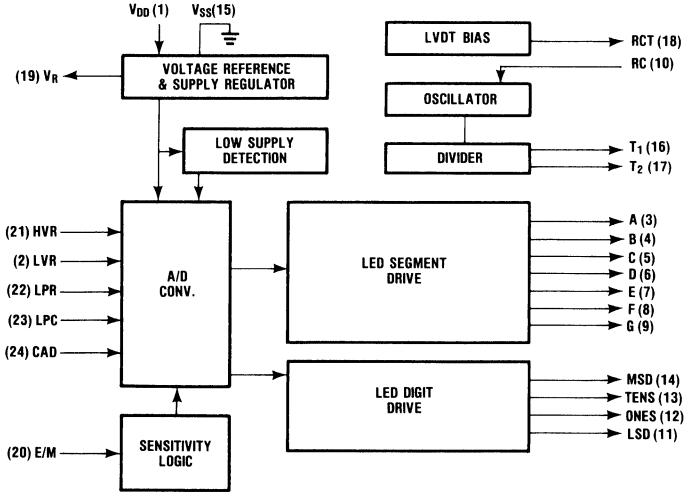
General Description

The S4036 General Purpose A/D Converter and Digital Scale Circuit provides a one chip solution to many Analog/Digital applications. Few external parts are needed as the S4036 provides an on-chip voltage reference, low supply detector, pin selectable sensitivity logic, and drivers for a multiplexed LED display.

The S4036 can begin to process analog data immediately upon presentation, or it can wait to sample the data after two seconds of settling time at user discretion.

In the sampled data mode of operation, a short pulse applied to the V_{DD} input signals the S4036 to start the

Block Diagram



Pin Configuration

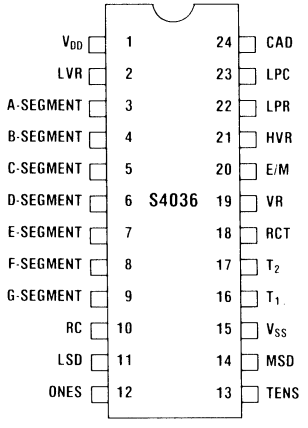


Figure 1. Typical ADC Application

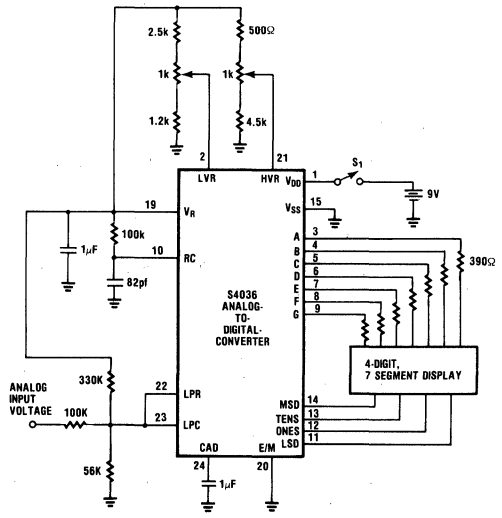
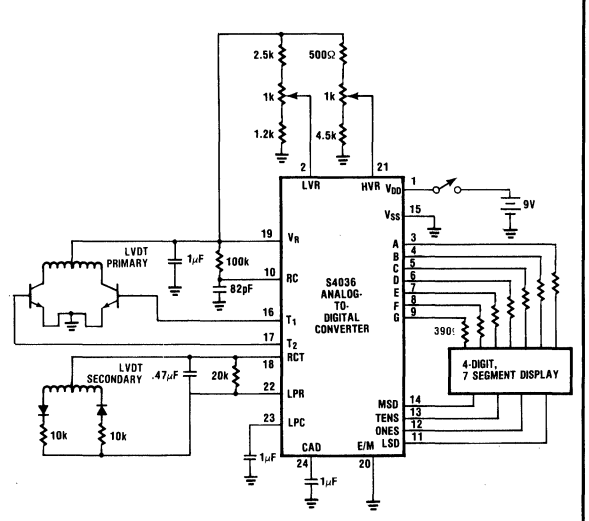


Figure 2. Typical Digital Scale Application



sample interval counter. The display clears to "000," with the most significant digit blanked. After two seconds, approximately, the S4036 begins to process the analog input. The display "rolls-up" from "000" to the digital value of the analog input. This "roll-up" process takes one second. The value on the display at the end of the conversion is held fixed until the V_{DD} line is pulsed to restart the process.

Here, a switch (S_1) pulses the V_{DD} input of the S4036 to begin the conversion process. When the analog voltage is more positive than the LVR voltage level, a non-zero reading will occur. If the analog voltage is more negative than the LVR level (underflow), a zero value reading will occur. If the analog voltage is more positive than the HVR voltage level (overflow), the S4036 will output a maximum value reading (2999 or 1360, depending on state of Pin 20). LVR is 1.5V to 2.5V, HVR is 4.5V to 5.5V.

The analog voltage is applied to Pins 22 and 23. Pins 16 (T_1), 17 (T_2), and 18 (RCT) are not connected. Notice the 390Ω resistors off Pins 3-9; these are used to limit the output current of the S4036.

A feature which can be user-programmed is the HVR and LVR voltages used by the ADC. The chip supplies a regulated voltage (Pin 19) which can be divided down and picked off via a potentiometer. Thus, the user can specify the lower reference ("0" value display point) and the upper reference (maximum value display point) merely by resistively dividing the regulated voltage output. This feature allows the S4036 to perform in many "non-standard" ADC situations.

A capacitor is required on Pin 24 to implement the Analog-to-Digital Converter. For most applications, the value of this capacitor is nominally 1µF, but this value is not critical to the conversion process.

Here, a mechanical input from the scale pulses the V_{DD} input of the S4036 to begin the conversion process. The same mechanical input from the scale also displaces the core of the Linear Variable Differential Transformer (LVDT) proportional to the weight of the object being measured. The LVDT primary is driven by 2NPN transistors controlled by S4036 timing outputs T_1 and T_2, which are 180° out of phase at a 50% duty cycle. The output (RCT) is used to bias the center tap of the LVDT secondary. The LVDT secondary presents an output which varies linearly with core position. This voltage is rectified, filtered, and presented to the analog inputs (LPR and LPC). (See Figure 3 for internal connection of S4036 pins RCT, LPR, and LPC.)

The S4036 has two pin-selectable modes of sensitivity. A Logic "0" on Pin 20 allows 3000 possible readings (0 to 2999), while a Logic "1" on Pin 20 allows 1361 possible readings (0 to 1360). This feature allows the sensitivity of the S4036 to be adapted to meet a wide range of ADC applications. In most digital scale applications, the pin-selectable sensitivity of the S4036 can be used to provide pounds (3000 readings) or kilograms (1361 readings) by providing a Logic "0" or "1" on Pin 20, respectively.

The chip also contains an RC oscillator amplifier which interfaces with an external resistor and capacitor to provide the timing for the Analog-to Digital Converter and multiplexed LED display drivers.

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} – 0.3V to V_{DD} + 0.3V
Storage Temperature Range	– 65°C to + 150°C
DC Supply Voltage	12 VDC
Power Dissipation (25°C)	1000mW
Safe Operation Temperature Range	0°C to 50°C
Lead Temperature (During Soldering)	300°C for Max. 10 Sec.

Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
T_{ACC}	Accurate Operation Temperature Range	10		35	°C	
V_{DD}	Operating Supply Voltage	V_{LS}		9.50	VDC	
f_{OSC}	Oscillator Frequency	91	104	117	KHz	R = 100K, C = 82pF
I_{DD}	Operating Supply Current			12	mA	Outputs Unloaded
t_{SAM}	2 Sec Data Sample Time	2.24	2.52	2.88	Sec	
t_{ADC}	ADC Calculation Internal	0.82	0.92	1.05	Sec	
f_{DISP}	Display MUX Frequency	355	406	457	Hz	
% MUX	Each Digit Minimum MUX Duty Cycle	20			%	
V_R	Regulated Voltage	5.5	6.00	6.5	V	Into 242 Ohm
V_{SEG}	V_{OUT}, Segment Drivers	7.2			V	Into 720 Ohm
V_{DIGIT}	V_{OUT}, Digit Drivers			1.2	V	From 91 Ohm
V_{LS}	Low Supply Detection & A/D Shutdown	6.3		7.3	V	
LVR	Low Voltage Reference	1.5		2.5	V	
HVR	High Voltage Reference	4.5		5.5	V	
f_{LVDT}	T_1 and T_2 Freq.	11	13	15	KHz	
V_{LVDT}	T_1 and T_2 Output Voltages @ V_{DD} = 8V			1	V	From 70K Ohm
		0.75			V	Into 1500 Ohm
	Linearity from Best Straight Line, V_{DD} = 8V			±5	Bits	2.3V ⩽ LPR ⩽ 4.7V LVR = 2V, HVR = 5V
	Reading Change Over Range of V_{DD}			±5	Bits	7.3V ⩽ V_{DD} ⩽ 9.0V, LVR = 2V, HVR = 5V, LPR = 3.5V
	Display Change Over Consecutive Readings			±3	Bits	V_{DD} = 8V, LVR = 2V, HVR = 5V, LPR = 3.5V

Figure 3. Internal Connection of S4036 Pins RCT, LPR, & LPC

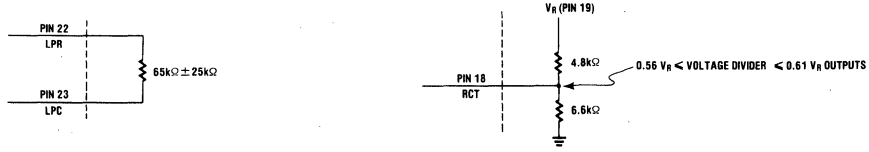
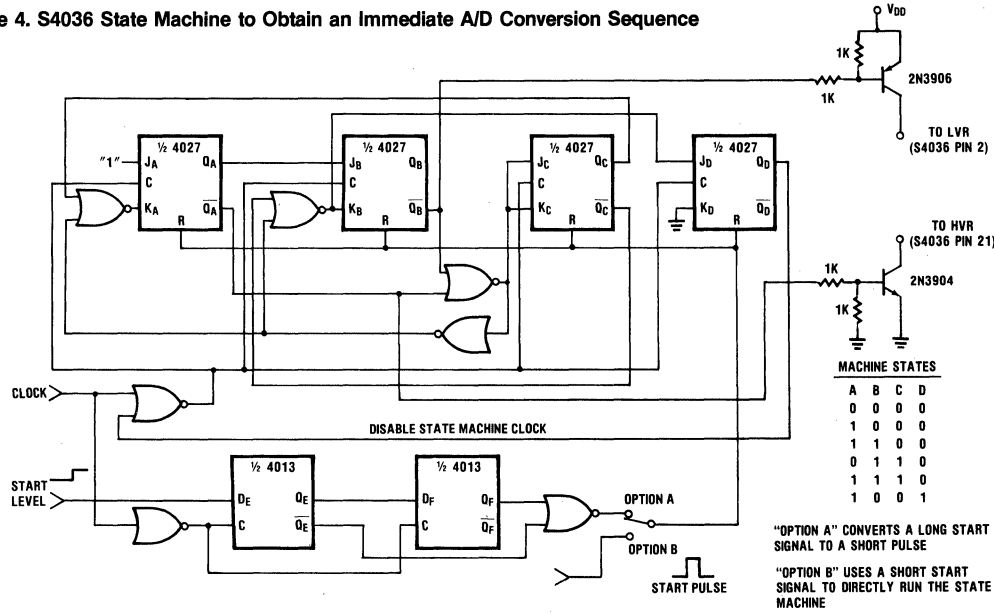


Figure 4. S4036 State Machine to Obtain an Immediate A/D Conversion Sequence



Immediate A/D Conversion Sequence

This sequence eliminates the analog data sample time, resets the S4036, and then proceeds directly with Analog-to-Digital conversion. This approach should be used for data which is steady when the S4036 is signaled to begin processing. It may be exercised by presenting the following logic series to LVR (Pin 2) and HVR (Pin 21):

Sequence Step	LVR	HVR
1	0	1
2	0	0
3	0	1
4	1	1
5	1	0
6	1	1
7	0	1

At the end of the signal sequence, the S4036 will sample the analog data input and "roll-up" the display to the digital value of the analog input. The sequence frequency should be greater than the oscillator frequency.

Logic "0": LVR $\leq$ 2.5V, HVR $\leq$ 1.0V

Logic "1": LVR $\geq V_{DD} - 1.0V$, HVR $\geq$ 4.5V

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Memories

Memory Products Selection Guide

STATIC MOS RANDOM ACCESS MEMORIES

Part No.	Organization	Process	Max. Access Time(ns)	Max. Active Power(mW)	Max. Standby Power(mW)	Power Supplies	Package
S68B10	128 × 8	NMOS	250	420	N/A	+ 5V	24 Pin
S68A10	128 × 8	NMOS	360	420	N/A	+ 5V	24 Pin
S6810	128 × 8	NMOS	450	400	N/A	+ 5V	24 Pin
S6810-1	128 × 8	NMOS	575	500	N/A	+ 5V	24 Pin

STATIC CMOS RANDOM ACCESS MEMORIES

Part No.	Organization	Max. Access Time(ns)	Max. Active Power(mW)	Max. Standby Power(mW)	Power Supplies	Package
S5101L-1	256 × 4	450	115	.055	+ 5V	22 Pin
S5101L	256 × 4	650	115	.055	+ 5V	22 Pin
S6501L-1	256 × 4	450	115	.055	+ 5V	22 Pin
S6501L	256 × 4	650	115	.055	+ 5V	22 Pin
S6514	1024 × 4	300	75	0.25	+ 5V	18 Pin
S6516	2048 × 8	230	55MHz	5.5	+ 5V	24 Pin

MOS READ ONLY MEMORIES

Part No.	Description	Organization	Process	Max. Access Time(ns)	Max. Active Power(mW)	Power Supplies	Package
S68A316	16,384 Bit Static ROM	2048 × 8	NMOS	350	370	+ 5	24 Pin
S68A332	32,768 Bit Static ROM	4096 × 8	NMOS	350	370	+ 5	24 Pin
S68B332	32,768 Bit Static ROM	4096 × 8	NMOS	250	370	+ 5	24 Pin
S2333	32,768 Bit Static ROM	4096 × 8	NMOS	350	385	+ 5	24 Pin
S9508A	40,960 Bit Static ROM	4096 × 10	NMOS	350	340	+ 5	28 Pin
S68A364	65,536 Bit Static ROM	8192 × 8	NMOS	350	385	+ 5	24 Pin
S68B364	65,536 Bit Static ROM	8192 × 8	NMOS	250	495	+ 5	24 Pin
S2364A	65,536 Bit Static ROM	8192 × 8	NMOS	350	385	+ 5	28 Pin
S2364B	65,536 Bit Static ROM	8192 × 8	NMOS	250	385	+ 5	28 Pin
S6364	65,536 Bit Static ROM	8192 × 8	CMOS	250	55	− 5	28 Pin
S9580B	81,920 Bit Static ROM	8192 × 10	NMOS	350	420	+ 5	28 Pin
S23128A	131,072 Bit Static ROM	16384 × 8	NMOS	350	385	+ 5	28 Pin
S23128B	131,072 Bit Static ROM	16384 × 8	NMOS	250	385	+ 5	28 Pin
S23256B	262,144 Bit Static ROM	32768 × 8	NMOS	250	220	+ 5	28 Pin
S23256C	262,144 Bit Static ROM	32768 × 8	NMOS	150	220	+ 5	28 Pin

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Preliminary Data Sheet **MILITARY 6514**

4096 BIT (1024x4) STATIC CMOS RAM

Features

- ☐ Address Access Time–300ns Maximum
- ☐ Read and Write Cycle Time—420ns Maximum
- ☐ Low Power Operation—39mW Maximum @1MHz
- ☐ Low Power Standby—28μW Maximum
- ☐ On-Chip Address Registers
- ☐ Low Voltage Data Retention—2 Volts
- ☐ TTL Compatible Inputs and Outputs
- ☐ Three-State Outputs
- ☐ Military Temperature/Voltage Range
- ☐ 883-B Processing

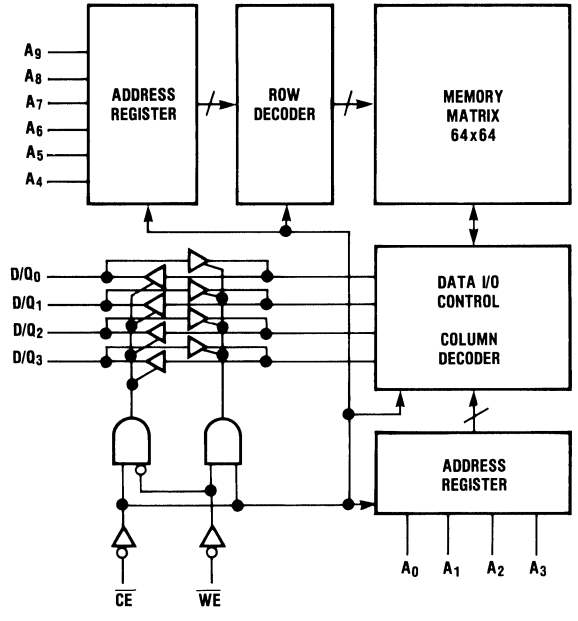
The S6514 is fabricated using AMI's CMOS Technology. This permits the manufacture of very high density, high performance CMOS RAMs.

General Description

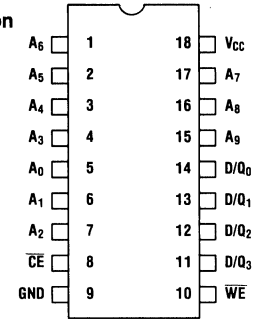
The AMI S6514 is a 4096 bit static CMOS RAM organized as 1024 words by 4 bits per word. The device offers low power and static operation from a single +5 Volt supply. All inputs and three-state outputs are TTL compatible. The common data I/O pins allow direct interface with common bus systems.

Data is latched into the on-chip Address Registers on the negative going edge of the Chip Enable signal. The data is then written into the cells on the negative going edge of Write Enable signal. The device is disabled and goes into a low power standby mode when the Chip Enable is High. Data in the memory will be maintained in this mode when V_{CC} is reduced to 2.0 Volts.

Block Diagram



Pin Configuration



Pin Names

A_0-A_9	Address Inputs
D/Q_0-D/Q_3	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	Data Out
Read	L	H	Data In
Write	L	L	HI-Z
Disable	H	X	HI-Z

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage $-V_{CC}$ ..... −0.3V to +7.0V
Input/Output Voltage Applied ..... −0.3V to V_{CC} +0.3V
Storage Temperature $-T_{stg}$ ..... −65°C to +150°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

D.C. Electrical Characteristics: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage Current	−1		1	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	−1		1	μA	V_{IN} = GND to V_{CC}
I_{SB}	Standby Supply Current			50	μA	V_{IN} = GND or V_{CC}
I_{CC}	Operating Supply Current			7	mA	V_{IN} = GND or V_{CC}, f = MHz
V_{IL}	Input Voltage LOW	−0.3		0.8	V	
V_{IH}	Input Voltage HIGH	2.4		V_{CC} +0.3	V	
V_{OL}	Output Voltage LOW			0.4	V	I_{OL} = 1.6mA
V_{OH}	Output Voltage HIGH	2.4			V	I_{OH} = −0.4mA

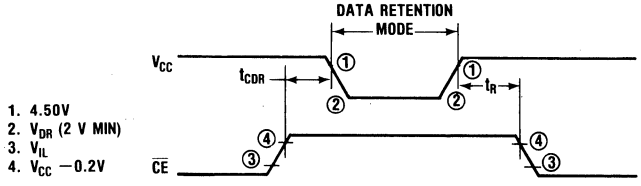
Capacitance: $T_A = 25°C$, f = 1MHz. Capacitance is sampled and guaranteed.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	GND to V_{CC}
C_{OUT}	Output Capacitance			10	pF	GND to V_{CC}

Low V_{CC} Data Retention Characteristics:

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{CCDR}	I_{CC} for Data Retention			50	μA	See Test Conditions and Waveforms
V_{CCDR}	V_{CC} for Data Retention	2.0			V	
t_{CDR}	Chip Deselect to Data Retention Time	0			ns	
t_R	Operation Recovery Time	TELEL			ns	

Low V_{CC} Data Retention Wave Form



1. 4.50V
2. V_{DR} (2 V MIN)
3. V_{IL}
4. V_{CC} −0.2V

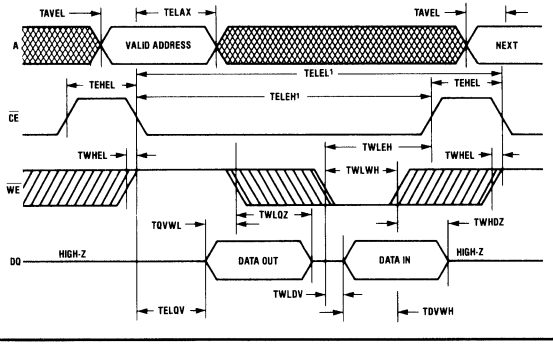
A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
trise/tfall	≤20ns
Output Load	1 TTL Load and 50pF
Timing Levels	1.5V

A.C. Electrical Characteristics: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
TELQV	Chip Enable Access Time			300	ns	
TAVQV	Adress Access Time			320	ns	
TWLQZ	Write Enable Output Disable Time			100	ns	
TEHQZ	Chip Enable Output Disable Time			100	ns	
TELEH	Chip Enable Pulse Negative Width	300			ns	
TEHEL	Chip Enable Pulse Positive Width	120			ns	See A.C. Test
TAVEL	Address Setup Time	20			ns	Conditions and
TELAX	Address Hold Time	50			ns	Waveforms
TWLWH	Write Enable Pulse Width	300			ns	
TWLEH	Write Enable Pulse Setup Time	300			ns	
TELWH	Write Enable Pulse Hold Time	300			ns	
TDVWH	Data Setup Time	200			ns	
TWHDZ	Data Hold Time	0			ns	
TWHEL	Write Enable Read Setup Time	0			ns	
TQVWL	Output Data Valid to Write Time	0			ns	
TWLDV	Write Data Delay Time	100			ns	
TELWL	Early Output High-Z Time			0	ns	
TWHEH	Late Output High-Z Time			0	ns	
TELEL	Read or Write Cycle Time	420			ns	

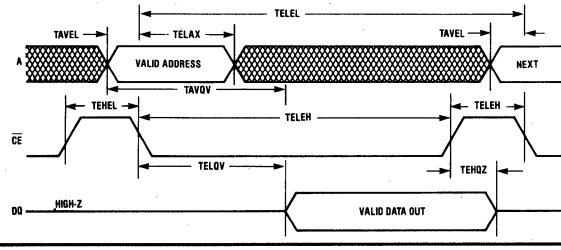
Read Modify Write Cycle



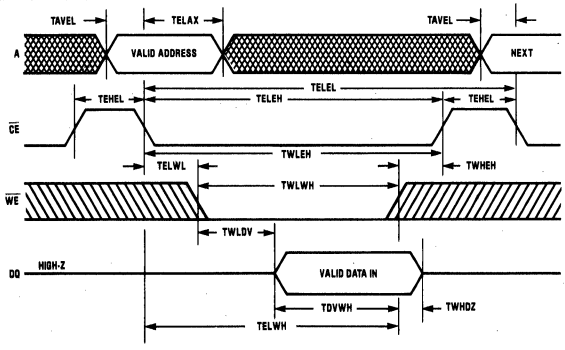
NOTE 1: TELEL & TELEH ARE LONGER THAN THE MINIMUM GIVEN FOR READ OR WRITE CYCLE.

MEMORIES

Read Cycle: $\overline{WE}$ = HIGH

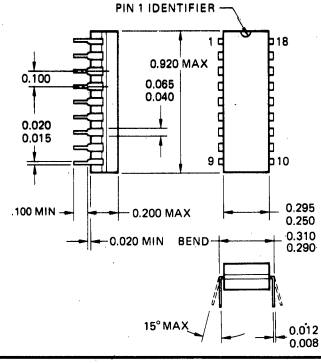


Write Cycle

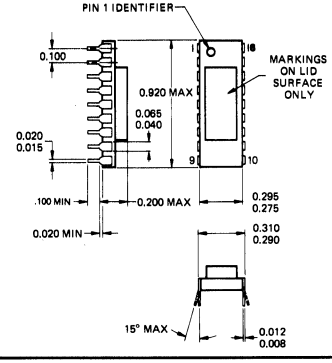


Package Outlines

18-Pin Cerdip



18-Pin Ceramic



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Preliminary Data Sheet **MILITARY 6516**

16,384 BIT (2048x8) STATIC CMOS RAM

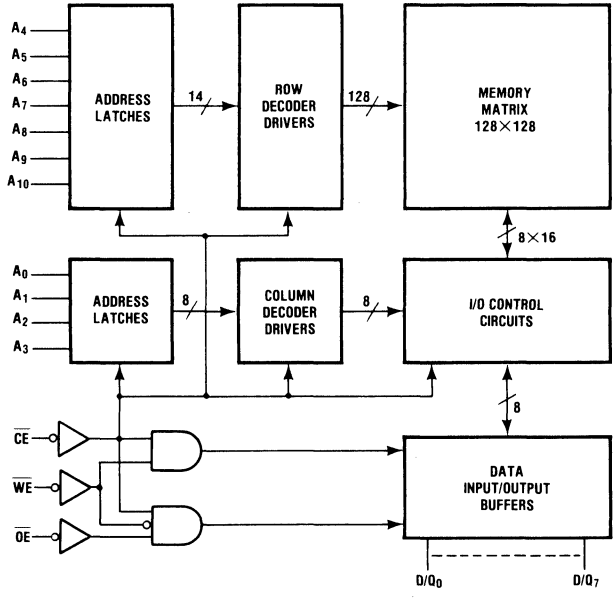
Features

- ☐ High Speed—150ns Maximum
- ☐ Low Power Standby—1.38mW Maximum
- ☐ Low Power Operation—83mW/MHz Maximum
- ☐ On-Chip Address Registers
- ☐ Fully TTL Compatible Inputs
- ☐ Three-State TTL Outputs
- ☐ Low Voltage Data Retention – 2V
- ☐ Standard 24 Pin Package
- ☐ EPROM and ROM Compatible Pinouts

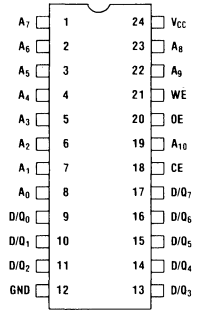
General Description

The AMI S6516 is a 16,384 bit static CMOS RAM organized as 2048 words by 8 bits. It offers low standby and operating power dissipation from a single + 5V power supply. All inputs and outputs are TTL compatible. The common data I/O pins allow direct interface with common bus systems. The output enable function facilitates memory expansion by allowing the outputs to be OR-tied to other devices. The device operates synchronously with address registers provided on-chip. The data is latched into the registers during the high to low transition of the chip enable pulse.

Block Diagram



Pin Configuration



Pin Names

A_0—A_{10}	Address Inputs
D/Q_0—D/Q_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Outputs
Read	L	H	L	Data Out
Write	L	L	H	High-Z
Chip Disable	H	X	X	High-Z
Output Disable	L	X	H	High-Z

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... −0°C to +70°C
Storage Temperature ..... −65°C to 150°C
Power Supply Voltage ..... −0.3V to 7V
Voltage on Any Pin with Respect to Ground ..... −0.3V to V_{CC} +0.3V
Power Dissipation 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device.

D.C. Electrical Characteristics: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage Current	−1		1	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	−1		1	μA	V_{OUT} = GND to V_{CC}
I_{SB}	Standby Supply Current			250	μA	V_{IN} = GND or V_{CC}
I_{CC}	Operating Supply Current			15	mA	V_{IN} = GND or V_{CC}, f = 1MHz
V_{IL}	Input Voltage LOW	−0.3		0.8	V	
V_{IH}	Input Voltage HIGH	2.2		V_{CC} +0.3	V	
V_{OL}	Output Voltage LOW			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output Voltage HIGH	2.4			V	I_{OH} = −1mA

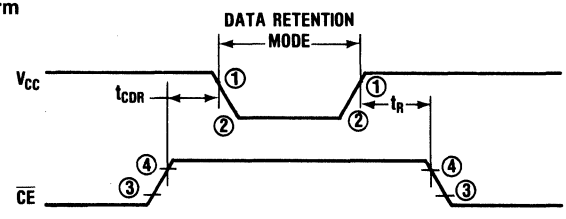
Capacitance: $T_A = 25°C$, t = 1MHz. Capacitance is sampled and guaranteed.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	GND to V_{CC}
C_{OUT}	Output Capacitance			10	pF	GND to V_{CC}

Low V_{CC} Data Retention Characteristics:

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{CCDR}	I_{CC} for Data Retention			250	μA	
V_{CCDR}	V_{CC} for Data Retention	2.0			V	
t_{CDR}	Chip Deselect to Data Retention Time	0			ns	
t_R	Operation Recovery Time	TELEL			ns	

Low V_{CC} Data Retention Wave Form



1. 4.50V
2. V_{DR} (2 V MIN)
3. V_{IL}
4. V_{CC} −0.2V

A.C. Test Conditions

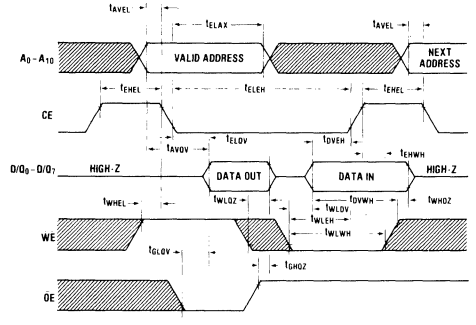
Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	≤10ns
Input Timing Level	0.8V and 2.2V
Output Timing Levels	0.6V and 2.2V
Output Load	1 TTL Load and 100pF

A.C. Electrical Characteristics: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

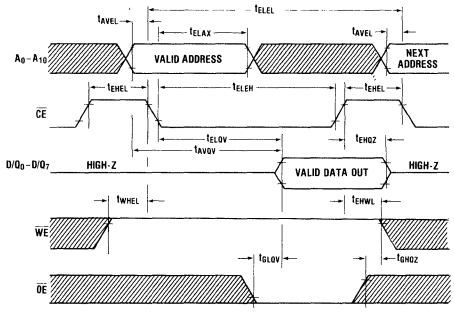
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{ELQV}	Chip Enable Access Time			150	ns	
t_{AVQV}	Address Access Time			150	ns	
t_{WLQZ}	Write Enable Output Disable Time			50	ns	
t_{EHQZ}	Chip Enable Output Disable Time			50	ns	
t_{ELEH}	Chip Enable Pulse Negative Width	150			ns	
t_{EHEL}	Chip Enable Pulse Positive Width	60			ns	
t_{AVEL}	Address Setup Time	0			ns	
t_{ELAX}	Address Hold Time	25			ns	
t_{WLWH}	Write Enable Pulse Width	140			ns	
t_{WLEH}	Write Enable Pulse Setup Time	140			ns	
t_{ELWH}	Write Enable Pulse Hold Time	140			ns	
t_{DVWH}	Data Setup Time	90			ns	
t_{WHDZ}	Data Hold Time	−10			ns	
t_{WHEL}	Write Enable Read Setup Time	0			ns	
t_{QVWL}	Output Data Valid to Write Time	−10			ns	
t_{WLDV}	Write Data Delay Time	40			ns	
t_{ELWL}	Early Output High-Z Time	−10			ns	
t_{WHEH}	Late Output High-Z Time	10			ns	
t_{ELEL}	Read or Write Cycle time	230			ns	

t_{EHWL}, Write Enable Read Hold Time ..... 0ns MIN.
t_{DVEH}, Data Setup Time to Chip Enable ..... 140ns MIN.
t_{GLQV}, Output Enable to Output Valid ..... 10ns MIN.
t_{GHQZ}, Output Enable to Output High-Z ..... 50ns MIN

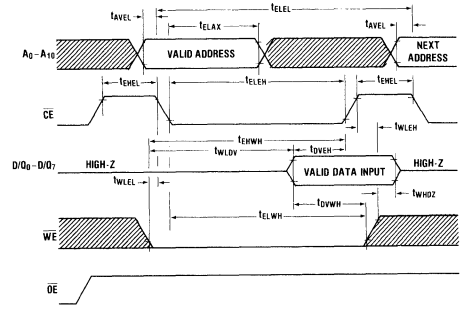
Read Modify Write Cycle



Read Cycle



Write Cycle



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ROM Ordering Information

ROM Ordering Information

Ordering Information

The following information should be included in the purchase order when ROM devices are being ordered.

- ☐ Part number
- ☐ Number of ROM patterns
- ☐ Quantity of prototypes for each pattern (if none, so state)
- ☐ Total quantity of each pattern
- ☐ Special marking (if required)
- ☐ *Method of ROM code entry (EPROM, punched paper tape, etc.)
- ☐ *Chip select definition —
- ☐ Pricing and delivery (pricing and delivery quotes can be obtained from any AMI Sales Office)

*If ordering a previously supplied pattern, the order should refer to the AMI C number (CXXXXX). This C number can be obtained from previous AMI billing or acknowledgement.

Unit Quantity Variance

AMI manufactures ROMs in a fully proven silicon gate N-Channel process. However, as in any semi-conductor production, yield variations do occur. Because of these normal yield variations a policy has been established that requires the customer to accept a small variation from the nominal quantity ordered.

Unit Quantity Variance ±5% or 50 units (whichever is greater)

Part Number

An AMI ROM part number consists of a device number followed by a single letter designating the package type.

P — designates plastic package
C — designates ceramic package (hermetic seal)

Device Numbers

S6831B/S68A316	2K×8	
S68A332/S68332	4K×8	Standard Pinout
S2333	4K×8	(Pin compatible with 2732 EPROM)
S68A364/S68B364	8K×8	(24 Pin)
S2364A/B	8K×8	(28 Pin-Compatible W/2764 EPROM)
S23128A/B	16K×8	(28 Pin)
S23256B/C	32K×8	(28 Pin)

ROM Sales Policy

Minimum Order Quantity

Capacity	Part No.	Architecture	Units/Pattern
16K	S6831B, S68A316	2K×8	1,000
32K	S68332, S68A332	4K×8	1,000
32K	S2333 (Alternate Pinout)	4K×8	1,000
64K	S68A364/S68B364 (24-Pin)	8K×8	500
64K	S2364A/B (28-Pin)	8K×8	500
128K	S23128A/B (28-Pin)	16K×8	250
256K	S23256B/C	32K×8	250

Unless otherwise requested by the customer, approximately 5 units will be assembled in a ceramic package for verification of the ROM pattern by the customer. These 5 units will be considered as part of the total quantity ordered.

Mask Charges*

Most ROM suppliers charge a mask charge to cover the expense of generating tooling that is unique to each ROM pattern. Current AMI mask charges are as follows.

		Min. Qty/Mask Charges		
Part No.	Architecture	499 Pcs.	999 Pcs.	1500 Pcs.
S6831B, S68A316	2K×8	N/A	N/A	$ 500
S68332, S68A332, S2333	4K×8	N/A	N/A	$ 750
S68A364, S2364	8K×8	N/A	$2000	$1500
S23128A/B	16K×8	$2500	$2000	$1500
S23256B/C	32K×8	$2500	$2000	$1500

*Subject to Change

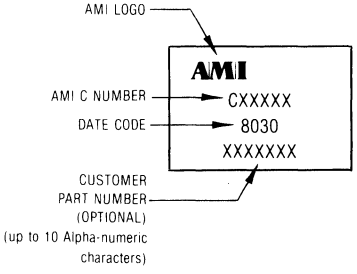
Reorder Policy

If a customer wishes to reorder the same ROM pattern, the following policy applies. If finished inventory exists, no minimum quantity limits will be imposed. However, if new wafer starts are required, the same minimum quantity as for a new pattern will apply. The 5 prototypes (supplied with new patterns) will not be supplied. No mask charge is applied to a reorder of a previously supplied ROM pattern.

ROM Package Marking

Unless otherwise specified, AMI ROMs are marked with a C number (the letter C followed by a 5 digit number) and a date code. This C number identifies both the device type and the specific pattern. This C number will be used on all AMI documents concerning the ROM.

A ROM can also be marked with a number supplied by the customer. A single number of up to 10 alpha numeric characters can be marked on the device without extra charge. Other customer markings are possible, but must be approved before the order is entered.



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to diskette and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested, AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitting ROM Code Data:

ROM		EPROM	
		PREFERRED	OPTIONAL
S6831B	2KX8	2716/2516	2-2708
S68332	4KX8	2532	2-2716/2516
S2333	4KX8	2732	2-2716/2516
S68A364	8KX8	68764	2-2532
S2364	8KX8	2764	2-2732
S23128	16KX8	27128	2-2764

If two EPROM's are used to specify one ROM pattern, (i.e., 2 16K EPROMs for one 32K ROM) two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Example: Two 2716 EPROMs for S68332 ROM
Marking: EPROM # 1 000-7FF
EPROM # 2 800-FFF

Pattern Data From ROMs

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitor's ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supplying ROM Code Data

If an EPROM or ROM cannot be supplied, the following other methods are acceptable.

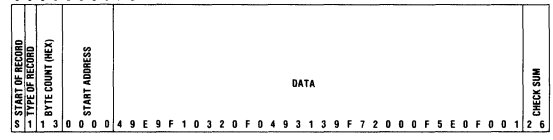
- ☐ 9 Track NRZ Magnetic Tape (2 each) odd parity, 800 BP1
- ☐ Paper Tape (AMI Hex format)
- ☐ Card Deck (AMI Hex format)

The AMI Hex format is described below. With its built-in address space mapping and error checking, this format is produced by the AMI Assembler.

Position	Description
1	Start of record (Letter S)
2	Type of record 0—Header record (comments) 1—Data record 9—End of file record
3, 4	Byte Count Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	Address Value The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9,..., N	Data Each data byte is represented by two hex characters. Most significant character first.
N + 1, N + 2	Checksum The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C
```



Paper tape format is the same as the card format above except:

a. The record should be a maximum of 80 characters.
b. Carriage return and line feed after each record followed by another record.
c. There should NOT be any extra line feed between records at all.
d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

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Preliminary Data Sheet **S68A316**

16,384 BIT (2048X8) STATIC NMOS ROM

Features

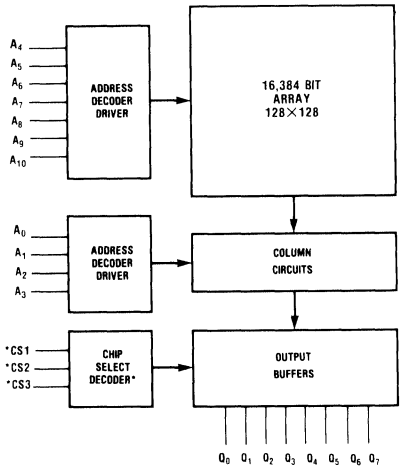
- ☐ Fast Address Access Time: S68A316 - 350ns Max.
- ☐ EPROM Pin Compatible
- ☐ Fully Static Operation
- ☐ Three Programmable Chip Selects
- ☐ TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Late Mask Programmable

General Description

The AMI S68316 family of 16,384 bit mask programmable Read-Only-Memories organized as 2048 words by 8 bits offers fully static operation with a single +5V power supply. The device is fully TTL compatible on all inputs and three-state outputs. The three chip selects are mask programmable, the active level is specified by the user. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

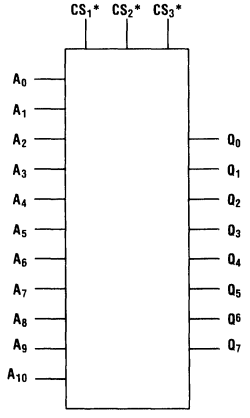
The devices are fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

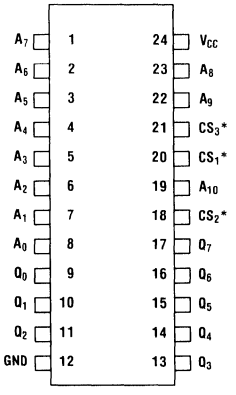


*USER DEFINED CHIP SELECTS
MAY BE DEFINED AS ACTIVE HIGH (CS) OR ACTIVE LOW (CS) OR NO CONNECTION (NC)

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{10}$	Address Inputs
$Q_0 - Q_7$	Data Outputs
$CS_1 - CS_3$	Chip Select Inputs
V_{CC}	+5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−10°C to 80°C
Storage Temperature	65°C to 150°C
Output or Supply Voltage	0.5V to 7V
Input Voltage	0.5V to 5.5V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 5%; T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0 to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current S68A316			80	mA	

Capacitance: f = 1.0MHz; T_A = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7.5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

A.C. Characteristics: V_{CC} = +5V ± 5%; T_A = 0°C to +70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S68A316			350	ns	See A.C. Test
t_{ACS}	Chip Select Access Time	S68A316			120	ns	Conditions and
t_{OFF}	Chip Deselect Time	S68A316			120	ns	Waveforms

NOTES:

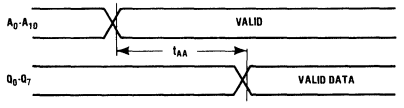
1. Only positive logic formats for CS_1—CS_3 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.

A.C. Test Conditions

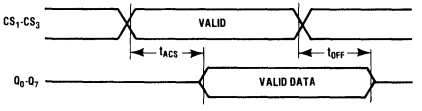
Input Pulse Levels	0.8V to 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms

Propagation From Addresses



Propagation From Chip Selects



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 2716; Optional (2) 2708

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

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S68A332/S68B332

32,768 BIT (4096X8) STATIC NMOS ROM

Features

- ☐ Fast Access Time:
  S68A332: 350ns Maximum
  S68B332: 250ns Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±5% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Selects
- ☐ EPROM Pin Compatible—2532
- ☐ Extended Temperature Range Available

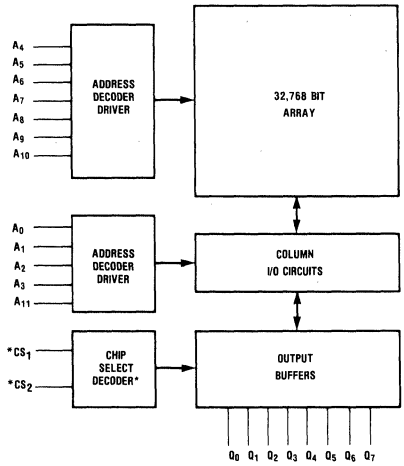
General Description

The AMI S68332 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single + 5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S68332 is pin compatible with UV EPROMs making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The two chip selects are mask programmable, the active level for each being specified by the user.

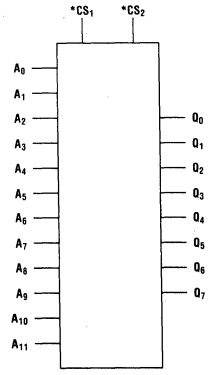
The S68332 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

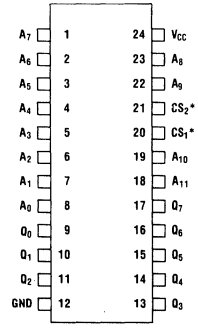


*PROGRAMMABLE CHIP SELECTS
MAY BE SPECIFIED AS ACTIVE LOW ($\overline{CS}$) OR ACTIVE HIGH (CS) OR NO CONNECT (NC)

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{11}$	Address Inputs
$Q_0 - Q_7$	Data Outputs
$CS_1 - CS_2$	Chip Select Inputs
V_{CC}	+ 5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part) ..... 0°C to + 70°C
(Industrial temp part) ..... − 40°C to + 85°C
Storage Temperature ..... − 65°C to 150°C
Output or Supply Voltages ..... − 0.5V to 7V
Input Voltages ..... − 0.5V to 7V
Power Dissipation 1W

* COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = + 5V ± 5%, T_A = 0°C to 70°C (Standard part); − 40°C to + 85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = − 220μA
V_{IL}	Input LOW Voltage	− 0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current			70	mA	

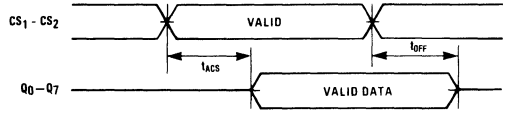
Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

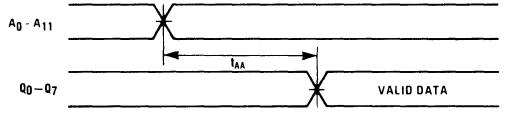
A.C. Characteristics: V_{CC} = + 5V ± 5%, T_A = 0°C to + 70°C (Standard part); − 40°C to + 85°C (Industrial temp part)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S68A332			350	ns	See A. C. Test Conditions Waveforms
		S68B332			250	ns	
t_{ACS}	Chip Select Access Time	S68A332			150	ns	
		S68B332			150	ns	
t_{OFF}	Chip Deselect Time	S68A332			150	ns	
		S68B332			150	ns	

Waveforms



Propagation From Chip Select



Propagation From Address

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Rise and Fall Times	≤20ns
Input Timing Level	1.5V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Custom Programming

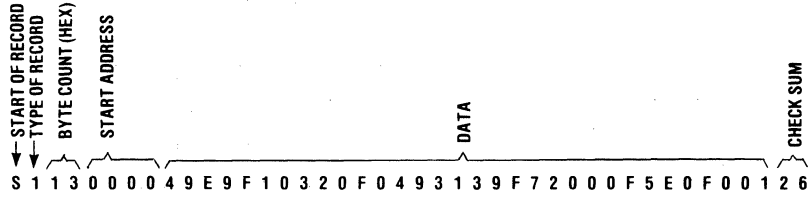
The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	Start of record (Letter S)
2	Type of record 0 — Header record (comments) 1 — Data record 9 — End of file record
3, 4	Byte Count Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	Address Value The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . . , N	Data Each data byte is represented by two hex characters. Most significant character first.
N + 1, N + 2	Checksum The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6

S 9 0 3 0 0 0 0 F C
```



NOTES:

1. Only positive logic formats for CS_1 and CS_2 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carraige return and line feed indicating end of file.

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Preliminary Data Sheet **S2333**

32,768 BIT (4096x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: 350ns Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±5% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Selects
- ☐ EPROM Pin Compatible (2732)
- ☐ Extended Temperature Range Available

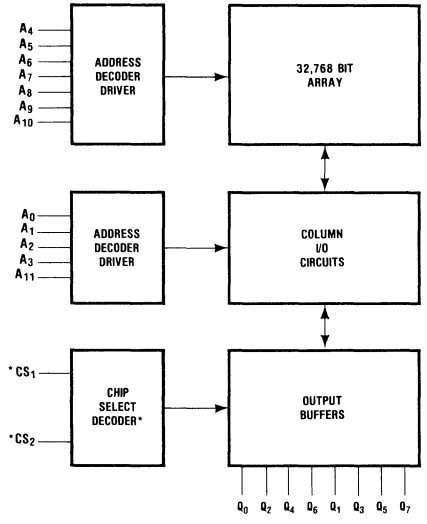
General Description

The AMI S2333 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2333 is pin compatible with UV EPROMs making system development much easier and more cost effective. The fully static S2333 requires no clocks for operation. The two chip selects are mask programmable with the active level for each being specified by the user.

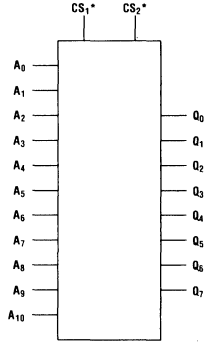
The S2333 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

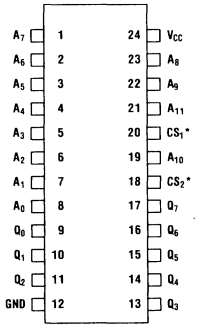


*PROGRAMMABLE CHIP SELECTS
MAY BE SPECIFIED AS ACTIVE LOW ($\overline{CS}$) OR ACTIVE HIGH (CS)
OR NO CONNECT (NC)

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{11}$	Address Inputs
$Q_0 - Q_7$	Data Outputs
$CS_1 - CS_2$	Chip Select Inputs
V_{CC}	+5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to + 70°C
(Industrial temp part)	− 40°C to + 85°C
Storage Temperature	− 65°C to 150°C
Output or Supply Voltages	− 0.5V to 7V
Input Voltages	− 0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = + 5V ± 5%, T_A = 0°C to 70°C (Standard part); − 40°C to + 85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = − 220μA
V_{IL}	Input LOW Voltage	− 0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current			70	mA	

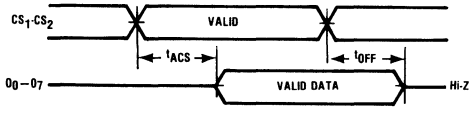
Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

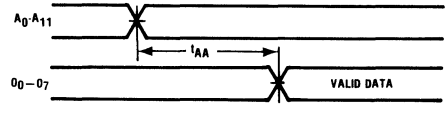
A.C. Characteristics: V_{CC} = + 5V ± 5%, T_A = 0°C to 70°C (Standard part); − 40°C to + 85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			350	ns	See A.C. Test Conditions and Waveform
t_{ACS}	Chip Select Access Time			120	ns	
t_{OFF}	Chip Deselect Time			120	ns	

Waveforms



Propagation From Chip Select



Propagation From Address

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Rise and Fall Times	≤20ns
Input Timing Level	1.5V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 1-2732; Optional 2-2716

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

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Preliminary Data Sheet **S9508A**

40,960 BIT (4096x10) STATIC NMOS ROMs

Features

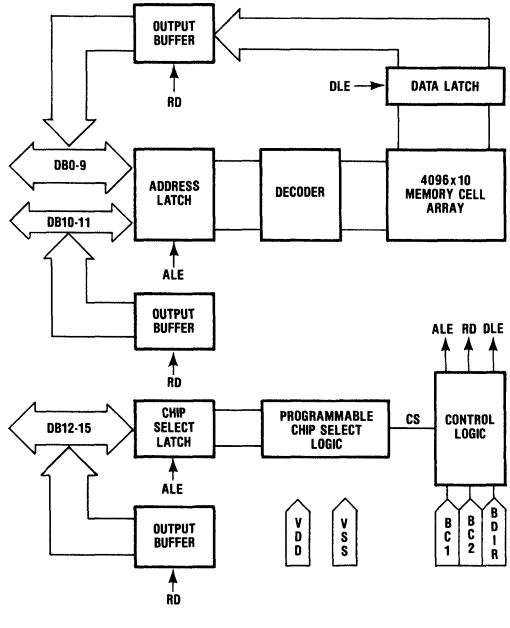
- ☐ Fully Static Operation
- ☐ Single +5V ±5% Power Supply
- ☐ TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Four Programmable Chip Selects
- ☐ CP1600 Microprocessor Compatible

General Description

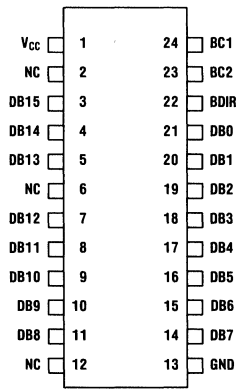
The AMI S9508A is a 40,960 bit mask programmable Read-Only Memory organized as 4,096 words by 10 bits. It offers fully static operation and a single +5V power supply. The device is TTL compatible on all inputs and input/output pins. The four chip selects are mask programmable for user specified code. The S9508A is designed to operate as program memory for systems using the CP1600 series microprocessor.

The S9508A is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

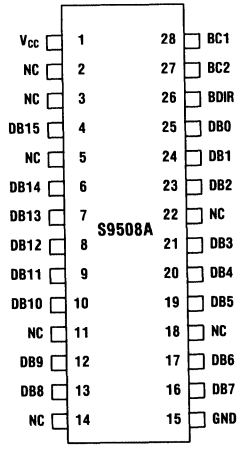
Block Diagram



24-Pin Configuration (Not Released)



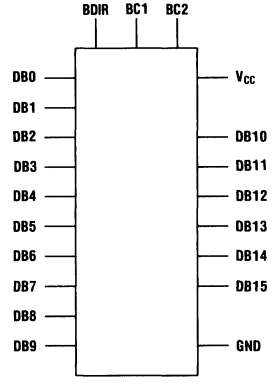
28-Pin Configuration



Pin Names

DB0-9	DATA BUS — ADDRESS INPUTS/MEMORY DATA OUTPUTS
DB10-11	DATA BUS — ADDRESS INPUTS
DB12-15	DATA BUS — CHIP SELECT INPUTS
BDIR	BUS DIRECTION
BC1	BUS CONTROL1
BC2	BUS CONTROL2
NC	NO CONNECTION
V_{CC}	POWER SUPPLY (+5V)

Logic Symbol



Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Input/Output or Supply Voltages	−0.2V to 7V
Power Dissipation	1W

*NOTE: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operational Specification

Ambient Temperature	0°C to 70°C
Supply Voltage	4.75V to 5.25 Volts

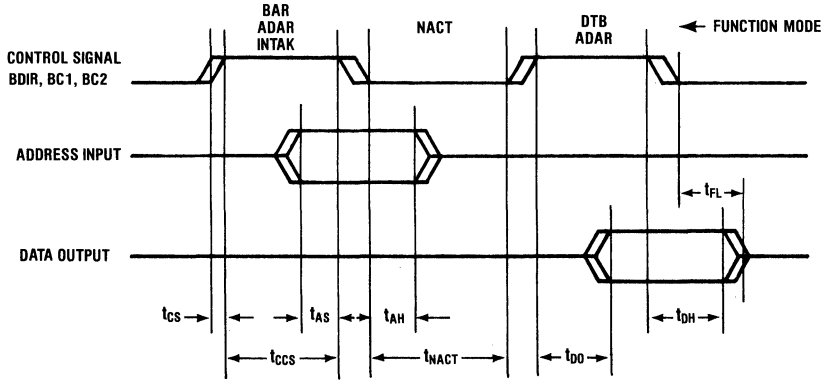
D.C. Characteristics: V_{CC} = +5V ± 5%, T_A = 0°C to +70°C

Symbol	Characteristic	Min.	Max.	Units	Conditions
	Inputs				
V_{IL}	Input LOW Voltage	0	0.7	V	
V_{IH}	Input HIGH Voltage	2.4	V_{CC}	V	
I_{LI}	Input Leakage Current	–	10	μA	V_{IN} = 0V to V_{CC}
C_{IN}	Capacitance		10	pF	V_{IN} = 0V @ 1MHz
	Outputs				
V_{OL}	Output LOW Voltage	0	0.5	V	I_{OL} = 1.5mA
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	V	I_{OH} = −80μA
	Supply Current				
I_{CC}	V_{CC} Supply Current	–	65	mA	T_A = 70°C V_{CC} = +5.25V

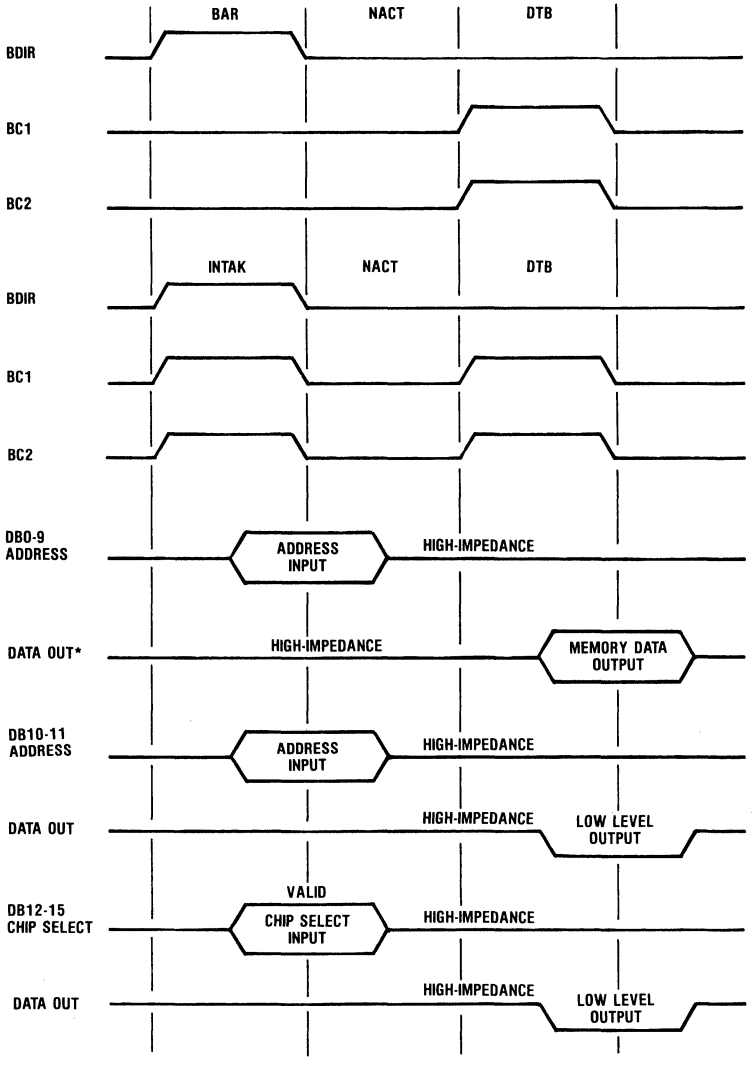
A.C. Characteristics

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{CS}	Control Signal Skew		50	ns	
t_{CCS}	Control Code Stable Time	885		ns	
t_{AS}	Address Set-Up Time	300		ns	
t_{AH}	Address Hold Time		65	ns	
t_{NACT}	No Action Time	885		ns	
t_{DO}	Data Out Delay Time		350	ns	
t_{DH}	Data Hold Time	80		ns	
t_{FL}	Bus Float Delay Time		300	ns	

Timing Waveforms



BAR/INTAK-DTB Timing



*IF THERE ARE INVALID CHIP SELECT INPUTS DURING BAR OR INTAK INSTRUCTION, I/O PINS ARE IN HIGH-IMPEDANCE STATE AND ARE NOT READ DURING DTB INSTRUCTION.

ROM Code Data

AMI's preferred method of receiving ROM Code Data is in EPROMs. Two sets of EPROMs should be submitted. One set is programmed to the desired code and the other set is blank. AMI will read the programmed EPROM set, transfer the data to disk and then use the data on disk to program the blank EPROM set. This set is then returned to the customer for verification of ROM program data. This procedure insures that the EPROM data has been properly entered into the AMI computer system.

EPROM Requirements

The following EPROMs should be used for ROM Code Data submission:

Preferred 2 each 2732's or optional 4 each 2716's.

2732

A. Two EPROMs required.

1. First should be labelled LOW.
   a. Contains data for DB0 through DB7.
2. Second should be labelled HIGH.
   a. Contains data for DB8 and DB9.
   b. All unused bits in this EPROM must be zeroes.

2716

A. Four EPROMs required.

1. First should be labelled LOW, addresses 0_{16} through 7 F F_{16}.
   a. Contains data for DB0 through DB7, addresses 0_{16} through 7 F F_{16}.
2. Second should be labelled LOW, addresses 800_{16} through F F F_{16}.
   a. Contains data for DB0 through DB7, addresses 800_{16} through F F F_{16}.
3. The Third EPROM should be labelled HIGH, addresses 0_{16} through 7 F F_{16}.
   a. This contains the data for DB8 and DB9, addresses 0_{16} through 7 F F_{16}.
   b. All unused bits in this EPROM must be zeroes.
4. The fourth EPROM should be labelled HIGH, addresses 800_{16} through F F F_{16}.
   a. This contains the data for DB8 and DB9, addresses 800_{16} through F F F_{16}.
   b. All unused bits in this EPROM must be zeroes.

The chip select/starting address (DB12 through DB15) for the ROM must be provided in hexadecimal format.

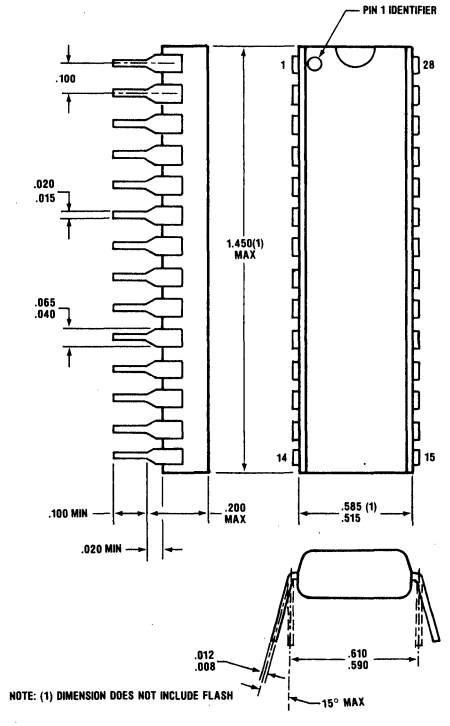
Pattern Data from ROMs

A ROM produced by another supplier may be submitted for ROM pattern data instead of EPROMs. ROMs submitted must be pin compatible with the AMI device. The programmable chip select/starting address must be defined.

Package Configuration

The package configuration and dimensions shall conform to the figure below. The package construction shall be ceramic, epoxy (plastic), or equivalent material which is moisture-resistant but not necessarily hermetically sealed.

28 Lead Plastic Package



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Preliminary Data Sheet **S68A364/S68B364**

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S68A364-350ns Maximum
  S58B364-250ns Maximum
- ☐ Low Standby Power: 85mW Maximum
- ☐ Late Mask Programmable
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Programmable Chip Enable

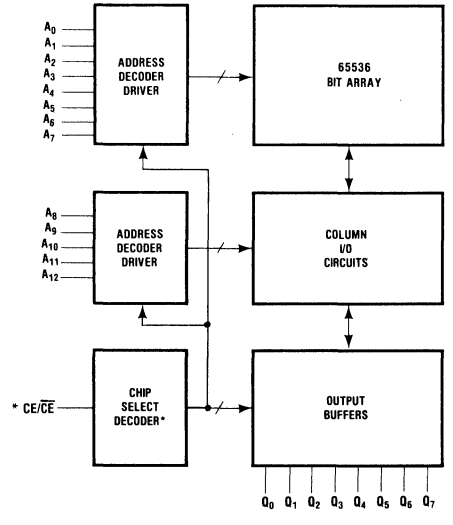
General Description

The AMI S68364 family are 65,536 bit static mask programmable NMOS ROMs organized as 8192 words by 8 bits. The devices are fully TTL compatible on all inputs and outputs and have a single + 5V power supply. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The devices are fully static, requiring no clocks for operation. The chip enable is mask programmable, the active level being specified by the user. When not enabled, power supply current is reduced to a maximum of 15mA.

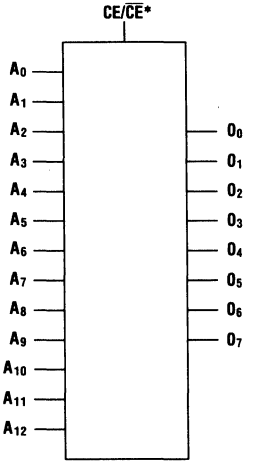
The S68364 family of devices are fabricated using AMI's NMOS ROM technology. This permits the mask programmable ROMs.

Block Diagram

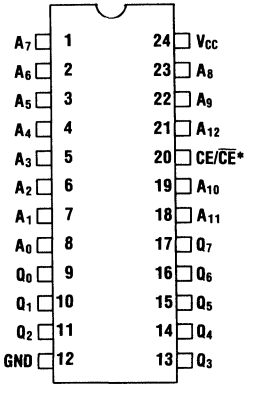


*USER DEFINED MASK PROGRAMMABLE CHIP ENABLE—MAY BE DEFINED AS ACTIVE HIGH, ACTIVE LOW, OR NO CONNECT.

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{12}	Address Inputs
Q_0—Q_7	Data Outputs
CE/$\overline{CE}$	Programmable Chip Enable
V_{CC}	+ 5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage				0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = −220μA
V_{IL}	Input LOW Voltage		−0.5		0.8	V	
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current				10	μA	V_{IN} = 0V to V_{CC}
$\|I_{LO}\|$	Output Leakage Current				10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current	S68A364			70	mA	
		S68B364			90	mA	
I_{SB}	Power Supply Current				15	mA	Chip Deselected

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

A.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S68A364			350	ns	See A.C. Test Conditions and Waveforms
		S68B364			250	ns	
t_{ACE}	Chip Enable Access Time	S68A364			350	ns	
		S68B364			250		
t_{OFF}	Chip Deselect Time	S68A364			200	ns	
		S68B364			100	ns	

NOTES:

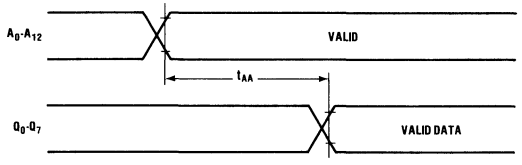
1. Only positive logic formats for CE/CE are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.

A.C. Test Conditions

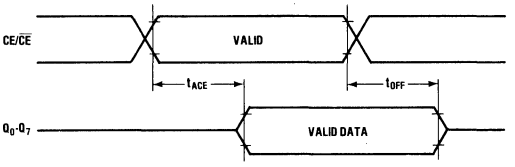
Input Pulse Levels	0.8V and 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms

Propagation From Addresses



Propagation From Chip Enable



MEMORIES

ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 68A764

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

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Preliminary Data Sheet **S2364A/S2364B**

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S2364A 350ns Maximum
  S2364B 250ns Maximum
- ☐ Low Standby Power: 85mW Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Chip Enables/Selects
- ☐ EPROM Pin Compatible (2764)
- ☐ Late Mask Programmable

General Description

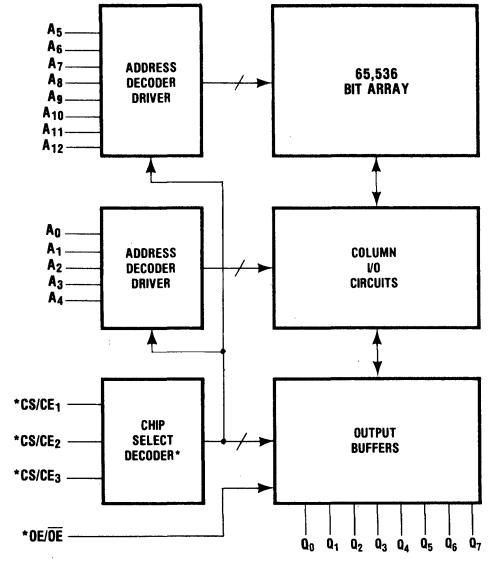
The AMI S2364 is a 65,536 bit static mask programmable NMOS ROM organized as 8192 words by 8 bits.

The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2364 is pin compatible with the 2764 UV EPROM making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The three chip enables are mask programmable; the active level for each being specified by the user. When not enabled, power supply current is reduced to a 10mA maximum.

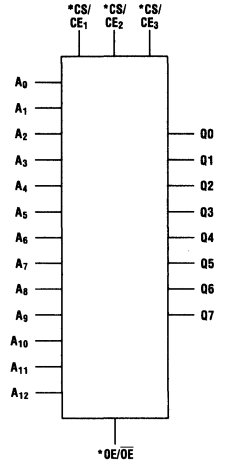
The S2364 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

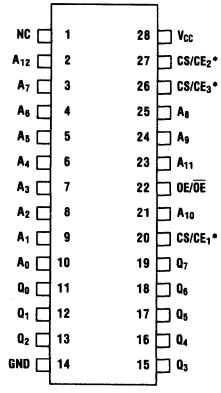


*CONTROL FUNCTION AND ACTIVE LEVEL IS USER DEFINED

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{12}	Address Inputs
Q_0—Q_7	Data Outputs
CS/CE_1-CS/CE_3	Chip Selects/Enables
$OE/\overline{OE}$	Output Enable
V_{CC};GND;NC	5V;Ground;No Connect

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin With Respect to Ground	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	μA	V_{IN} = 0V to 5.5V
$\|I_{LO}\|$	Output Leakage Current			10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			90	mA	Chip Enabled
I_{SB}	Power Supply Current—Standby			15	mA	Chip Disabled

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

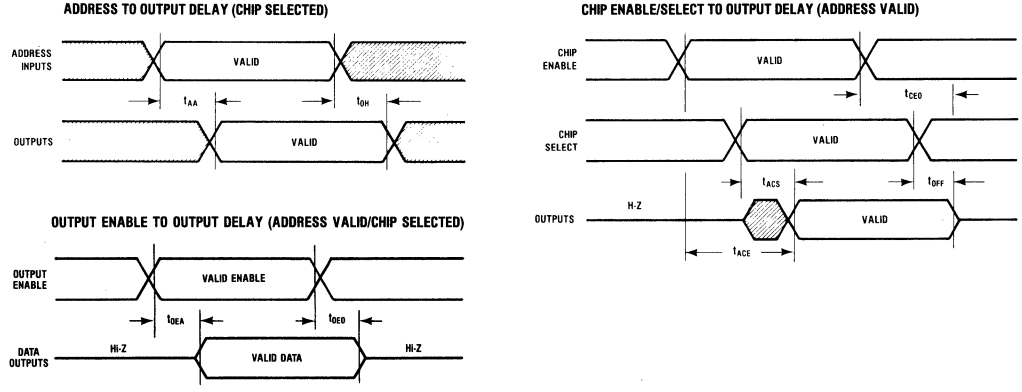
A.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S2364A S2364B			350 250	ns	See A.C. Test Conditions and Waveforms
t_{ACE}	Chip Enable Access Time	S2364A S2364B			350 250	ns	
t_{ACS}	Chip Select Access Time	S2364A S2364B			120 80	ns	
t_{OEA}	Output Enable Access Time	S2364A S2364B			100 80	ns	
t_{CEO}	Disable Time From Chip Enable	S2364A S2364B			200 80	ns	
t_{OEO}	Disable Time From Output Enable	S2364A S2364B			100 80	ns	
t_{OFF}	Chip Deselect Time	S2364A S2364B			120 80	ns	
t_{OH}	Output Hold Time	S2364A S2364B	10 0			ns	

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 1-2764; Optional 2-2732

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

Truth Table:

CS/CE1	CS/CE2	CS/CE3/	OE/$\overline{OE}$	OUTPUTS	POWER
$\overline{CE1}$	X	X	OE/$\overline{OE}$	HI-Z	STANDBY
X	$\overline{CE2}$	X	OE/$\overline{OE}$	HI-Z	STANDBY
X	X	$\overline{CE3}$	OE/$\overline{OE}$	HI-Z	STANDBY
$\overline{CS1}$	CS/CE2	CS/CE3	OE/$\overline{OE}$	HI-Z	ACTIVE
CS/CE1	$\overline{CS2}$	CS/CE3	OE/$\overline{OE}$	HI-Z	ACTIVE
CS/CE1	CS/CE2	$\overline{CS3}$	OE/$\overline{OE}$	HI-Z	ACTIVE
CS/CE1	CS/CE2	CS/CE3	$\overline{OE}$/OE	HI-Z	ACTIVE
CS/CE1	CS/CE2	CS/CE3	OE/$\overline{OE}$	DATA OUT	ACTIVE

The user decides between a CS or CE function and then defines the active level. The functions may also be defined as No Connections (NC). The chip is enabled when the inputs match the user defined states.

Pins	Control Functions Available
27	CS2, $\overline{CS2}$, CE2, $\overline{CE2}$, NC
26	CS3, $\overline{CS3}$, CE3, $\overline{CE3}$, NC
22	OE, $\overline{OE}$, NC
21	CS1, $\overline{CS1}$, CE1, $\overline{CE1}$, NC

AMI®

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Preliminary Data Sheet **S6364**

65,536 BIT (8192x8) STATIC CMOS ROM

Features

- ☐ Fast Access Time: 250ns Maximum
- ☐ Low Standby Power 5.5mW Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Chip Enables/Selects
- ☐ EPROM Pin Compatible (2764)
- ☐ Programmable Output/Chip Enable

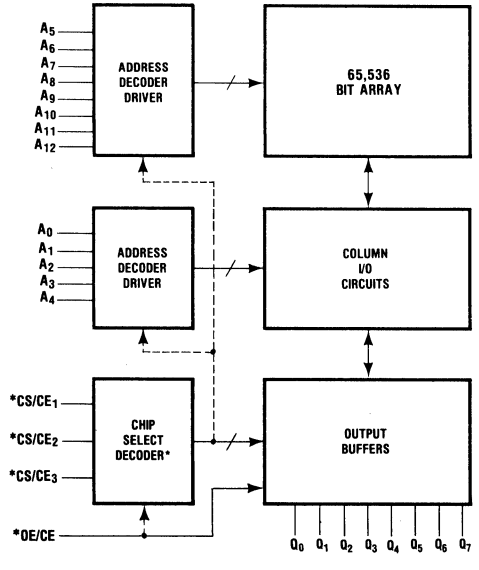
General Description

The AMI S6364 device is a 65,536 bit static mask programmable CMOS ROM organized as 8192 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S6364 is pin compatible with the 2764 UV EPROM making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The three chip enables are mask programmable; the active level for each being specified by the user. When not enabled, the power supply current is reduced to a 10mA maximum.

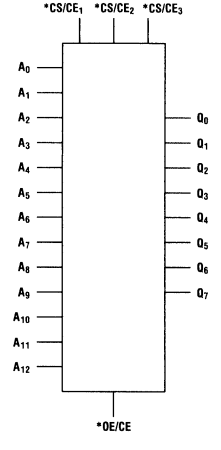
The S6364 is fabricated using AMI's CMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

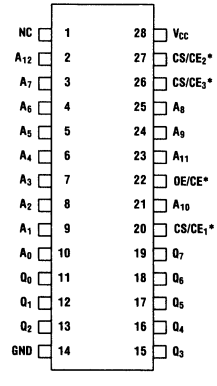


* THE USER DECIDES BETWEEN A CS OR CE FUNCTION AND OE OR CE FUNCTION THEN DEFINES THE ACTIVE LEVEL FOR CS/CE AND OE/CE.

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{12}	Address Inputs
Q_0—Q_7	Data Outputs
CS/CE_1-CS/CE_3	Chip Selects/Enables
OE/CE	Output Enable/Chip Enable
V_{CC}; GND; NC	5V; Ground; No Contact

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−40°C to 85°C
Storage Temperature	−65°C to 150°C
Output or Supply Voltages	−0.3V to 6V
Input Voltages	−0.3V to V_{CC} + 0.3V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −400μA
V_{IL}	Input LOW Voltage	−0.1		0.8	V	
V_{IH}	Input HIGH Voltage	2.2		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
$\|I_{LO}\|$	Output Leakage Current			10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			10	mA	f = 1.0MHz
I_{SB}	Power Supply Current—Standby			1	mA	Chip Disabled

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

A.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			250	ns	See A.C.
t_{ACE}	Chip Enable Access Time			250	ns	Test Conditions
t_{OE}	Output Enable Access Time	0		80	ns	
t_{ACS}	Chip Select Access Time	0		80	ns	and
t_{CEO}	Disable Time From Chip Enable	0		80	ns	Waveforms
t_{OFF}	Chip Deselect Time	0		80	ns	
t_{OEO}	Disable Time From Output Enable	0		80	ns	
t_{OH}	Output Hold Time	0			ns	

TRUTH TABLE

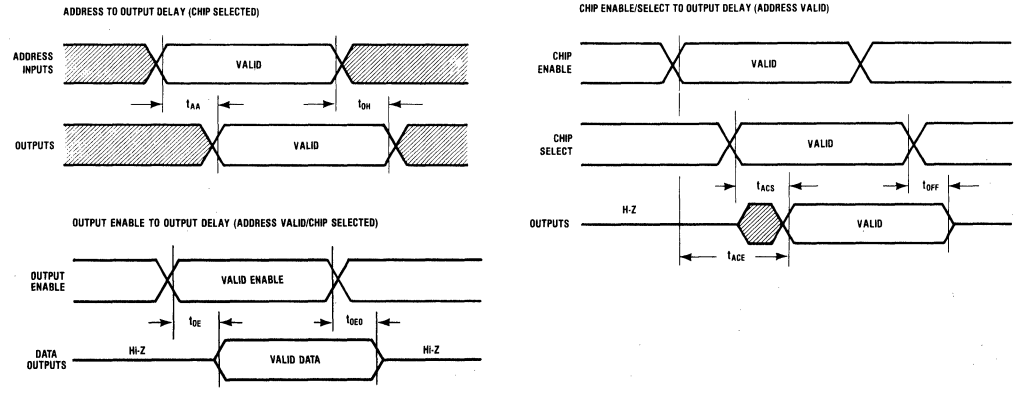
CS/CE1	CS/CE2	CS/CE3	OE/CE	OUTPUTS	POWER
$\overline{CET}$	X	X	X	HI-Z	STANDBY
X	$\overline{CE2}$	X	X	HI-Z	STANDBY
X	X	$\overline{CE3}$	X	HI-Z	STANDBY
X	X	X	$\overline{CE}$	HI-Z	STANDYB
$\overline{CS1}$	CS/CE2	CS/CE3	OE/CE	HI-Z	ACTIVE
CS/CE1	$\overline{CS2}$	CS/CE3	OE/CE	HI-Z	ACTIVE
CS/CE1	CS/CE2	$\overline{CS3}$	OE/CE	HI-Z	ACTIVE
CS/CE1	CS/CE2	CS/CE3	$\overline{OE}$	HI-Z	ACTIVE
CS/CE1	CS/CE2	CS/CE3	OE/CE	DATA OUT	ACTIVE

The user decides between a CS/CE and OE/CE function and then defines the active level. The functions may also be defined as a NO CONNECT NC). The chip is enabled when the inputs match the user defined states.

A.C. Test Conditions

Input Pulse Levels	0.8V to 2.2V
Input Timing Level	1.0V and 2.0V
Output Timing Levels	0.65V and 2.2V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 2764

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMs

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may only have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

S9580B

81,920 BIT (8192x10) STATIC NMOS ROM

Features

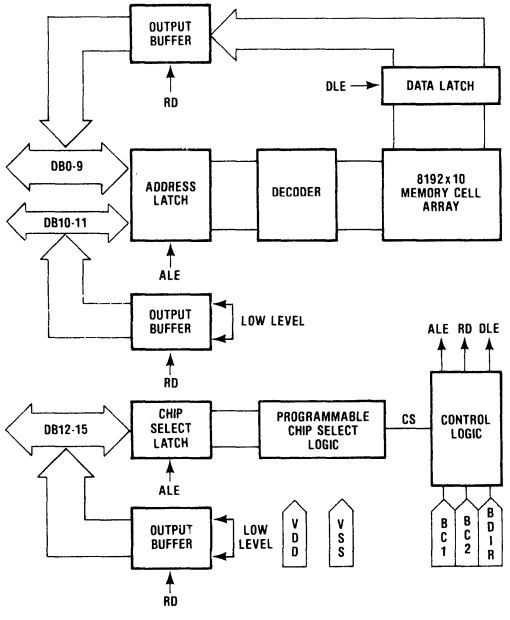
- ☐ Fully Static Operation
- ☐ Single +5V ±5% Power Supply
- ☐ TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Four Programmable Chip Selects
- ☐ CP1600 Microprocessor Compatible

General Description

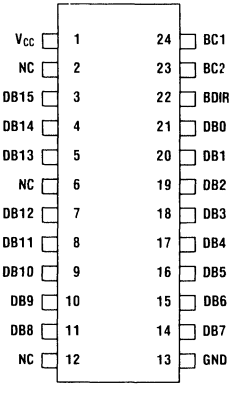
The AMI S9580B is a 81,920 bit mask programmable Read-Only Memory organized as 8,192 words by 10 bits. It offers fully static operation and a single +5V power supply. The device is TTL compatible on all inputs and input/output pins. The S9580B consists of two 4096x10 bit ROMs, each with its own four bit mask programmable chip select code. It is designed to operate as program memory for systems using the CP1600 series microprocessor.

The S9580B is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

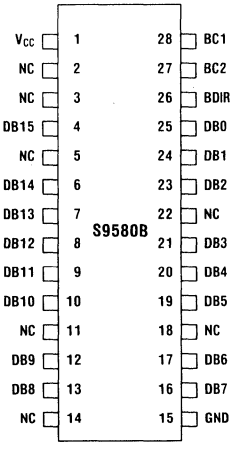
Block Diagram



24-Pin Configuration (Not Released)



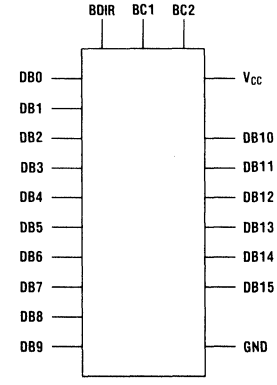
28-Pin Configuration



Pin Names

DB0-9	DATA BUS — ADDRESS INPUTS/MEMORY DATA OUTPUTS
DB10-11	DATA BUS — ADDRESS INPUTS
DB12-15	DATA BUS — CHIP SELECT INPUTS
BDIR	BUS DIRECTION
BC1	BUS CONTROL1
BC2	BUS CONTROL2
NC	NO CONNECTION
V_{CC}	POWER SUPPLY (+5V)

Logic Symbol



Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +100°C
Storage Temperature	−65°C to +150°C
Input/Output or Supply Voltages	−0.2V to 6.5V
Power Dissipation	1W

*NOTE: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operational Specification

Ambient Temperature	0°C to 70°C
Supply Voltage	4.75V to 5.25 Volts

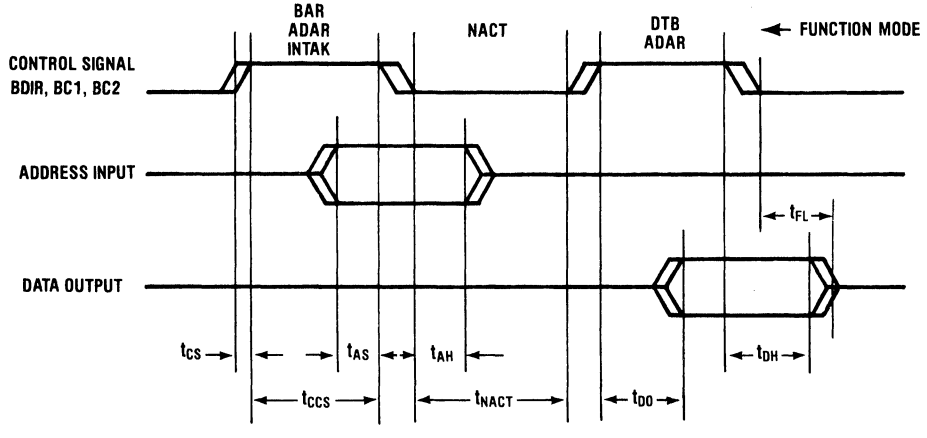
D.C. Characteristics: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C

Symbol	Characteristic	Min.	Max.	Units	Conditions
	Inputs				
V_{IL}	Input LOW Voltage	0	0.7	V	
V_{IH}	Input HIGH Voltage	2.4	V_{CC}	V	
I_{LI}	Input Leakage Current	–	10	μA	V_{IN} = 0V to V_{CC}
C_{IN}	Capacitance		10	pF	V_{IN} = 0V @ 1MHz
	Outputs				
V_{OL}	Output LOW Voltage	0	0.5	V	I_{OL} = 1.5mA
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	V	I_{OH} = −80μA
	Supply Current				
I_{CC}	V_{CC} Supply Current	–	80	mA	T_A = 70°C V_{CC} = +5.25V

A.C. Characteristics

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{CS}	Control Signal Skew		50	ns	
t_{CCS}	Control Code Stable Time	885		ns	
t_{AS}	Address Set-Up Time	300		ns	
t_{AH}	Address Hold Time	65		ns	
t_{NACT}	No Action Time	885		ns	
t_{DO}	Data Out Delay Time		350	ns	
t_{DH}	Data Hold Time	80		ns	
t_{FL}	Bus Float Delay Time		300	ns	

Timing Waveforms



Functional Description

The AMI S9580B 8Kx10 ROM has 16 input/output pins (DB0-DB15) to bring address in and output data, along with three inputs (BC1, BC2, BDIR) for control functions. When in the output mode, the programmed data will be on pins DB0 through DB9, while pins DB10 through DB15 will all be driven to a logic "zero" level. Of the 16 bits of address input, DB0 through DB11 are used for addressing different locations within the selected 4K segment of the ROM, while DB12 through DB15 form a programmable chip enable. A valid input code on the control pins will cause the address present on the I/O pins to be loaded into the input address register. A valid output code on the control inputs will allow the output buffers to drive the I/O pins only if the previous input address contained a valid chip enable code in bits 12 through 15.

Functional Description (continued)

From initialization, the ROM waits for the first address code, i.e., BAR. For this address code and all subsequent address sequences, the ROM reads the 16 bit external bus and latches the value into its address register.

The ROM contains a programmable memory location for its own 4K page, and if a valid address and chip enable is detected, the particular address located will transfer its contents to the chip output buffers. If the control code following the address cycle was a READ, the ROM will output the 10 bits of addressed data and drive logic zero on the top six bits of the bus.

ROM RESPONSE	CODE ON INPUT PINS			CONTROL FUNCTION	I/O PINS			FUNCTION
	BDIR	BC1	BC2		DB 0-9	DB 10-11	DB 12-15	
A	0	0	0	NACT	HIGH IMPEDANCE, NOT BEING READ			NO ACTION
B	0	0	1	IAB	HIGH IMPEDANCE, NOT BEING READ			IGNORED BY ROM
	1	0	1	DWS				
	1	1	0	DW				
C	0	1	0	ADAR	1) MEMORY DATA OUTPUT 2) MEMORY DATA IS LOADED INTO THE ADDRESS REGISTER	1) LOW LEVEL DATA OUTPUT 2) LOW LEVEL DATA IS LOADED INTO THE ADDRESS REGISTER	1) LOW LEVEL DATA OUTPUT 2) LOW LEVEL DATA IS LOADED INTO THE CHIP SELECT REGISTER	OUTPUT AND INPUT
D	0	1	1	DTB	MEMORY DATA OUTPUT	LOW LEVEL DATA OUTPUT	LOW LEVEL DATA OUTPUT	DATA TO BUS
E	1	0	0	BAR	ADDRESS INPUT AND ADDRESS LATCH	ADDRESS INPUT AND ADDRESS LATCH	CHIP SELECT INPUT AND CHIP SELECT LATCH	BUS TO ADDRESS REGISTER
	1	1	1	INTAK				

Responses

A. No action. Waiting state. Signals may be propagating internally, but I/O pins are in a high-impedance state, and are not being read.

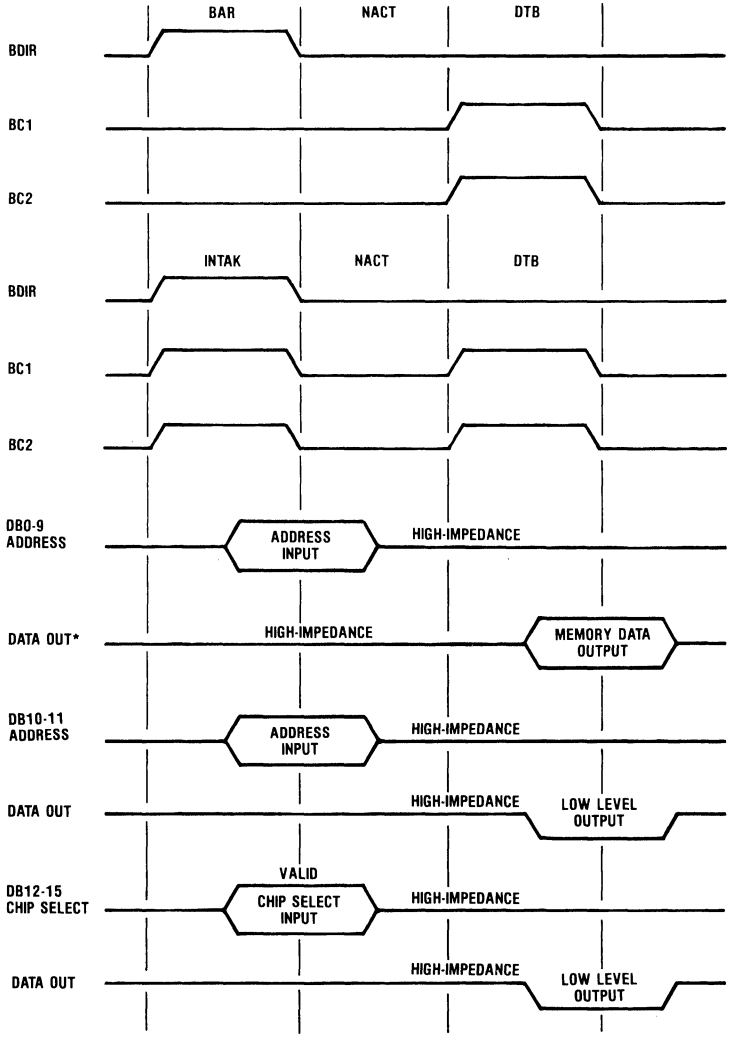
B. Ignored by ROM. Basically same response as A.

C. Output and Input. Output buffers drive I/O pins (if there is a valid chip enable from address previously loaded), and whatever appears on the I/O pins is loaded into the address register. If there is not a valid chip enable from address previously loaded, I/O pins are in a high-impedance state and whatever appears on the I/O pins is loaded into the address register.

D. Data to Bus. Output buffers drive I/O pins according to data in output register (if there is a valid chip enable). I/O pins are not read. Address previously loaded into address register remains unchanged. If there is not a valid chip enable from address previously loaded, I/O pins are in a high-impedance state and are not read.

E. Bus to Address Register. Output buffers are in high-impedance state. Address present on I/O pins is loaded into address register.

BAR/INTAK-DTB Timing



*IF THERE ARE INVALID CHIP SELECT INPUTS DURING BAR OR INTAK INSTRUCTION, I/O PINS ARE IN HIGH-IMPEDANCE STATE AND ARE NOT READ DURING DTB INSTRUCTION.

ROM Code Data

AMI's preferred method of receiving ROM Code Data is in EPROMs. Two sets of EPROMs should be submitted. One set is programmed to the desired code and the other set is blank. AMI will read the programmed EPROM set, transfer the data to disk and then use the data on disk to program the blank EPROM set. This set is then returned to the customer for verification of ROM program data. This procedure insures that the EPROM data has been properly entered into the AMI computer system.

EPROM Requirements

The following EPROMs should be used for ROM Code Data submission:

Required 4 each 2732 EPROMs.

1. First should be labelled LOW 1.
   a. Contains data for DB0 through DB7 for the first 40K.
2. Second should be labelled HIGH 1.
   a. Contains data for DB8 and DB9 for the first 40K.
   b. All unused bits in this EPROM must be zeroes.
3. Third should be labelled LOW 2.
   a. Contains data for DB0 through DB7 for the second 40K.
4. Fourth should be labelled HIGH 2.
   a. Contains data for DB8 and DB9 for the second 40K.
   b. All unused bits in this EPROM must be zeroes.

The chip select/starting address (DB12 through 15) for the ROM must be provided in hexidecimal format.

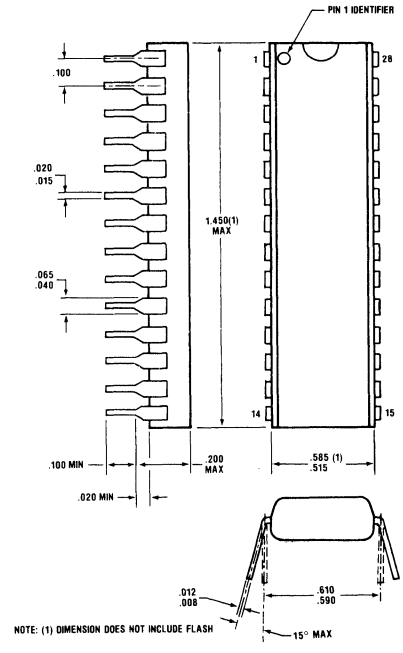
Pattern Data from ROMs

A ROM produced by another supplier may be submitted for ROM pattern data instead of EPROMs. ROMs submitted must be pin compatible with the AMI device. The programmable chip select/starting address must be defined.

Package Configuration.

The package configuration and dimensions shall conform to the figure below. The package construction shall be ceramic, epoxy (plastic), or equivalent material which is moisture-resistant but not necessarily hermetically sealed.

Package Outline



AMI

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S23128A/S23128B**

131,072 BIT (16384x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S23128A-350ns Maximum
  S23128B-250ns Maximum
- ☐ Low Standby Power: 110mW Max.
- ☐ Fully Static Operation
- ☐ Single +5V ± 10% Power Supply
- ☐ Directly TTL Compatible Outputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Enables/Selects
- ☐ EPROM Pin Compatible (27128)
- ☐ Late Mask Programmable
- ☐ Programmable Output/Chip Enable

General Description

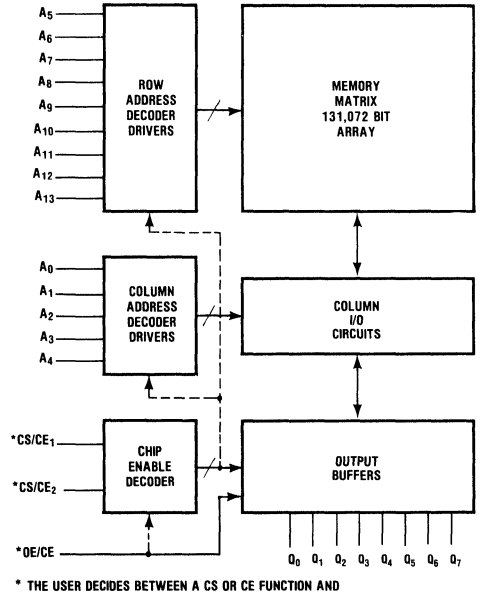
The AMI S23128 is a 131,072 bit static mask programmable NMOS ROM organized as 16,384 words by 8 bits.

The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S23128 is pin compatible with the 27128 EPROM making system development easier and more cost effective. The fully static S23128 requires no clocks for operation. The three control pins are mask programmable with the active level and function being specified by the user. The pins can also be programmed as no connections. If CE functions are selected, automatic powerdown is available. The power supply current is reduced to 12mA when the chip is disabled.

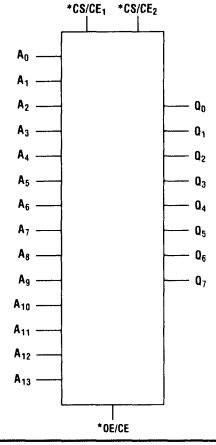
The S23128 is fabricated using AMI's NMOS technology. This permits the manufacture of high density, high performance ROMs.

Block Diagram

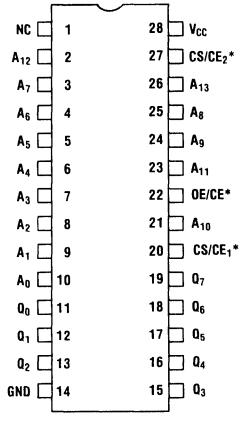


* THE USER DECIDES BETWEEN A CS OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL FOR CS/CE AND OE/CE.

Logic Symbol



Pin Configuration



Pin Names

A_0-A_{13}	Address Inputs
Q_0-Q_7	Data Outputs
CS/CE_1-CS/CE_2	Chip Selects/Enables
OE/CE	Output Enable/Chip Enable
V_{CC};GND;NC	5V;Ground; No Connect

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin With Respect to Ground	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current	−10		10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current	−10		10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			40	mA	Chip Enabled
I_{SB}	Power Supply Current—Standby			20	mA	Chip Disabled

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

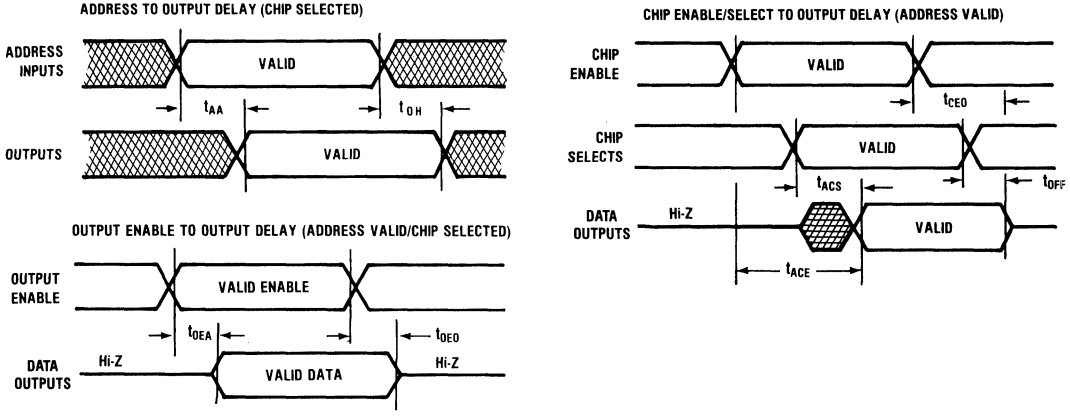
A.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S23128A S23128B			350 250	ns	See A.C. Test Conditions and Waveforms
t_{ACE}	Chip Enable Access Time	S23128A S23128B			350 250	ns	
t_{ACS}	Chip Select Access Time	S23128B S23128B			120 80	ns	
t_{OEA}	Output Enable Access Time	S23128A S23128B			120 80	ns	
t_{OFF}	Chip Deselect Time	S23128A S23128B			120 80	ns	
t_{CEO}	Disable Time From Chip Enable	S23128A S23128B			120 80	ns	
t_{OEO}	Disable Time From Output Enable	S23128A S23128B			120 80	ns	
t_{OH}	Output Hold Time	S23128A S23128B	0 0			ns	

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 1-27128; Optional 2-2764

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

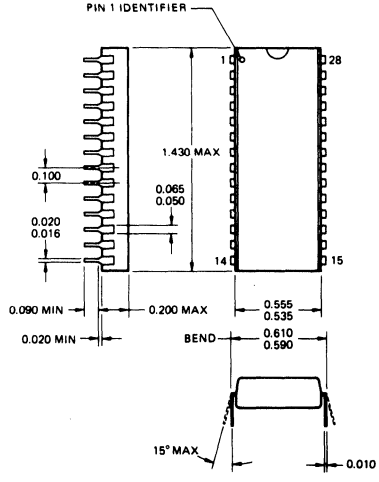
Truth Table:

CS/CE1	CS/CE2	OE/CE	Outputs	Power
$\overline{CE1}$	X	X	Hi-Z	Standby
X	$\overline{CE2}$	X	Hi-Z	Standby
X	X	$\overline{CE}$	Hi-Z	Standby
$\overline{CS1}$	CS/CE2	OE/CE	Hi-Z	Active
CS/CE1	$\overline{CS2}$	OE/CE	Hi-Z	Active
CS/CE1	CS/CE2	$\overline{OE}$	Hi-Z	Active
CS/CE1	CS/CE2	OE/CE	Data Out	Active

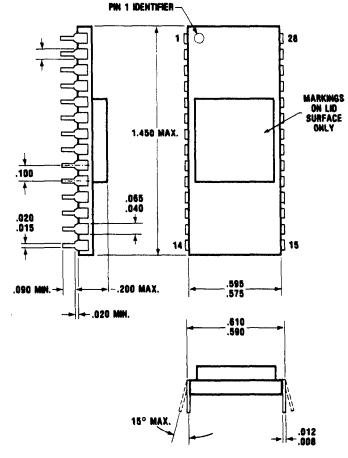
The user decides between a CS/CE and OE/CE function and then defines the active level. The functions may also be defined as No Connections (NC). The chip is enabled when the inputs match the user defined states.

Package Outlines

28-Pin Plastic



28-Pin Ceramic



AMI

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Preliminary Data Sheet **S23256B/S23256C**

262,144 BIT (32,768x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time:
  S23256B: 250ns Maximum
  S23256C: 150ns Maximum
- ☐ Low Power Dissipation
  Active Current:
  40mA Maximum
  Standby Current: 10mA Maximum
- ☐ Fully Static Operation
- ☐ Two User-Defined and Programmable Control Lines: CE/CS, OE/CE
- ☐ EPROM Pin Compatible
- ☐ Late Mask Programmable
- ☐ Three-State TTL Compatible Outputs

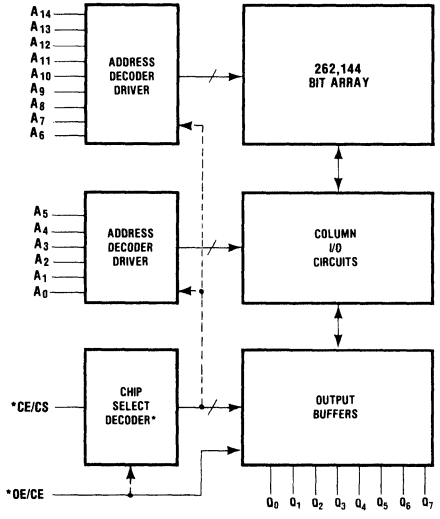
General Description

The AMI S23256 is a 262,144 bit static mask programmable NMOS ROM organized as 32,768 words by 8 bits. The devices are fully TTL compatible on all inputs and outputs and operate from a single +5V ±10% power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S23256 is pin compatible with the 27128 UV EPROM making system development much easier and more cost effective. It is fully static, requiring no clocks for operation.

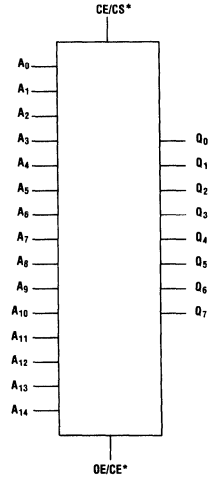
The S23256 is fabricated using AMI's N-Channel MOS ROM technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

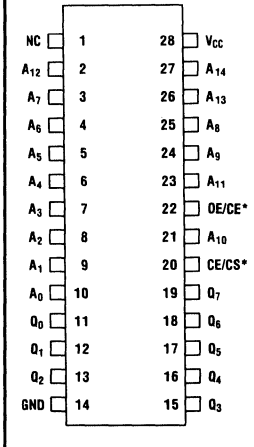


*THE USER DECIDES BETWEEN A CE OR CS AND OE OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{14}	Address Inputs
Q_0—Q_7	Data Outputs
CE/CS	Chip Enable/Chip Select
OE/CE	Output/Chip Enable
V_{CC};GND;NC	5V;Ground;No Connect

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
$\|I_{LO}\|$	Output Leakage Current			10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			40	mA	Chip Enabled
I_{SB}	Power Supply Current—Standby			10	mA	Chip Disabled

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

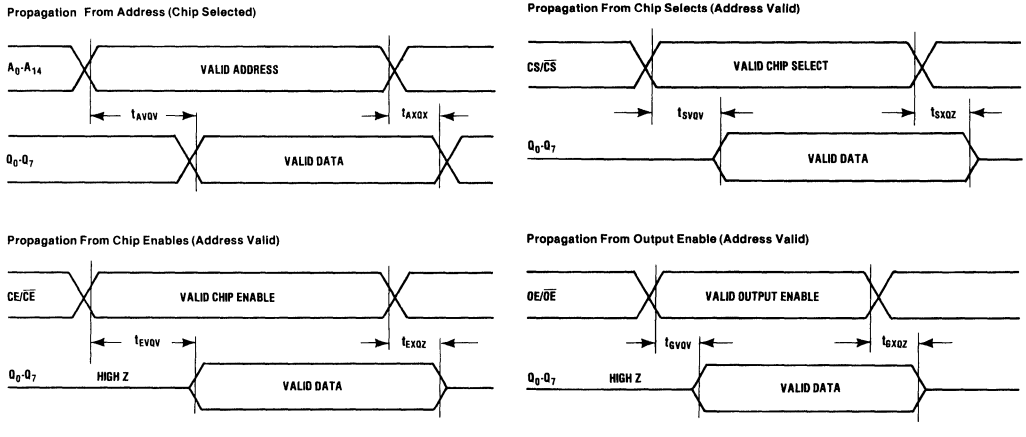
A.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Address Access Time S23256B S23256C			 250 150	 ns	See A.C. Test Conditions and Waveforms
t_{EVQV}	Chip Enable Access Time S23256B S23256C			 250 150	 ns	
t_{SVQV}	Chip Select Access Time S23256B S23256C			 120 80	 ns	
t_{GVQV}	Output Enable Access Time S23256B S23256C			 120 80	 ns	
t_{AXQX}	Output Hold/Address Change S23256B S23256C	 10 10			 ns	
t_{EXQZ} t_{SXQZ} t_{GXQZ}	Deselect Times S23256B S23256C			 120 80	 ns	

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 2-27128

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

Truth Table

CE/CS	OE/CE	OUTPUTS	POWER
CE/CS	OE/CE	DATA OUT	ACTIVE
$\overline{CE}$	X	HIGH Z	STANDBY
$\overline{CS}$	X	HIGH Z	ACTIVE
X	$\overline{OE}$	HIGH Z	ACTIVE
X	$\overline{CE}$	HIGH Z	STANDBY

THE DEVICE IS ENABLED WHEN THE CONTROL LINES MATCH THE USER DEFINED STATES.

AMI

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S6800

MICROPROCESSOR COMPONENT FAMILY

Contact factory for complete data sheet

S6800 Family Selection Guide

MICROPROCESORS

S6800/S68A00/S68B00	8-Bit Microprocessor (1.0/1.5/2.0MHz Clock)
S6801	Single Chip Microcomputer 2K ROM, 128 x 8 RAM, 31 I/O Lines, Enhanced Instruction (External [E] or Internal Clock)
S6802/A/B/S6808/A/B	Microprocessor with Clock and RAM (1.0/1.5/2.0MHz Clock (S6808 Models—No RAM)
S6803/S6803N/R	S6801 Without ROM (N/R Model—No ROM and RAM)
S6805	Single Chip Microcomputer 1.152 x 8 ROM, 64 x 8 RAM, Timer, Pre-scaler, Bit Level Instructions.
S6809(E)/S68A09(E)/S68B09(E)	Pseudo 16-Bit Microprocessor (1.0/1.5/2.0MHz Clock) (E Models—External Clock Mode)

PERIPHERALS

S1602	Universal Asynchronous Receiver/Transmitter (UART)
S2350	Universal Synchronous Receiver/Transmitter (USRT)
S6551/S6551A	UART With Baud Rate Generator
S6821/S68A21/S68B21	Peripheral Interface Adapter (PIA) (1.0/1.5/2.0MHz Clock)
S6840/S68A40/S68B40	Programmable Timer (1.0/1.5/2.0MHz)
S68045	CRT Controller (CRTC)
S6846	2K ROM, Parallel I/O, Programmable Timer
S6850/S68A50/S68B50	Asynchronous Communication Interface Adapter (ACIA)
S6852/S68A52/S68B52	Synchronous Serial Data Adapter (SSDA) (1.0/1.5/2.0MHz Clock)
S6854/S68A54/S68B54	Advanced Data Link Controller (ADLC) (1.0/1.5/2.0MHz Clock)

MEMORIES

S6810/S68A10/S68B10	128 x 8 Static RAM (450/360/250ns Access Time)

AMI

A Subsidiary of Gould Inc.

S6800/S68A00/S68B00

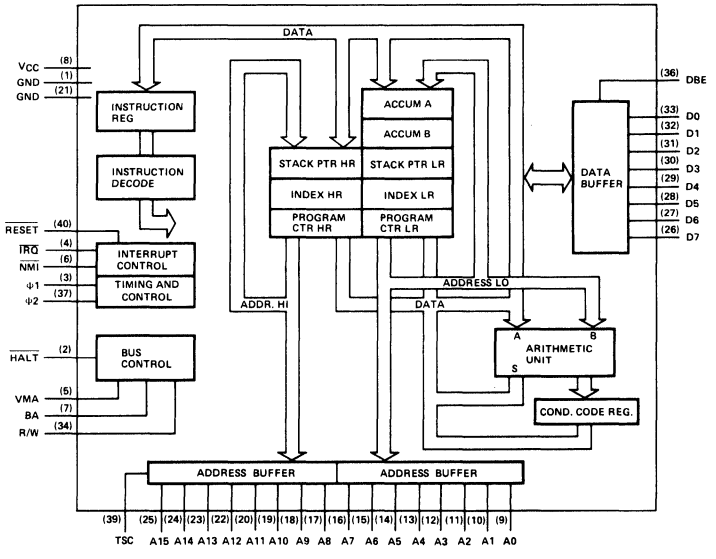
8-BIT MICROPROCESSOR

Features

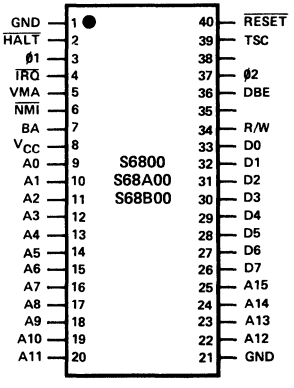
- ☐ Eight-Bit Parallel Processing
- ☐ Bi-Directional Data Bus
- ☐ Sixteen-Bit Address Bus — 65536 Bytes of Addressing
- ☐ 72 Instructions — Variable Length
- ☐ Seven Addressing Modes — Direct, Relative Immediate, Indexed, Extended, Implied and Accumulator
- ☐ Variable Length Stack
- ☐ Vectored Restart
- ☐ 2 Microsecond Instruction Execution
- ☐ Maskable Interrupt Vector
- ☐ Separate Non-Maskable Interrupt — Internal Registers Saved in Stack
- ☐ Six Internal Registers — Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- ☐ Direct Memory Access (DMA) and Multiple Processor Capability
- ☐ Clock Rates — S6800 — 1.0MHz
  — S68A00 — 1.5MHz
  — S68B00 — 2.0MHz
- ☐ Simple Bus Interface Without TTL
- ☐ Halt and Single Instruction Execution Capability

S6800 FAMILY

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3 to +7.0V
Input Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

Electrical Characteristics

(V_{CC} = 5.0V, ± 5%, V_{SS} = 0, T_A = 0 to +70°C unless otherwise noted.)

Symbol	Characteristics		Min.	Typ.	Max.	Unit
V_{IH} V_{IHC}	Input High Voltage (Normal Operating Levels)	Logic $\phi1$, $\phi2$	V_{SS} +2.0 V_{CC} −0.6	— —	V_{CC} V_{CC} +0.3	Vdc
V_{IL} V_{ILC}	Input Low Voltage (Normal Operating Levels)	Logic $\phi1$, $\phi2$	V_{SS} −0.3 V_{SS} −0.3	— —	V_{SS} +0.8 V_{SS} +0.4	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max) (V_{IN} = 0 to 5.25V, V_{CC} = 0.0V)	 Logic* $\phi1$, $\phi2$	 — —	 1.0 —	 2.5 100	μAdc
I_{TSI}	Three-State (Off State) Input Current V_{IN} = 0.4 to 2.4V, V_{CC} = Max	D0 — D7 A0 — A15, R/W	— —	2.0 —	10 100	μAdc
V_{OH}	Output High Voltage (I_{LOAD} = 205μAdc, V_{CC} = Min) (I_{LOAD} = 145μAdc, V_{CC} = Min) (I_{LOAD} = −100μAdc, V_{CC} = Min)	 D0 — D7 A0 — A15, R/W, VMA BA	 V_{SS} +2.4 V_{SS} +2.4 V_{SS} +2.4	 — —	 — —	Vdc
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = Min)		—	—	V_{SS} +0.4	Vdc
P_D	Power Dissipation		—	0.5	1.0	W
C_{IN}	Capacitance# (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	 $\phi1$ $\phi2$ D0 — D7 Logic Inputs	 — — — —	 — — 10 6.5	 35 70 12.5 10	pF
C_{OUT}		A0 — A15, R/W, VMA	—	—	12	pF
f	Frequency of Operation	S6800 S68A00 S68B00	0.1 0.1 0.1	— — —	1.0 1.5 2.0	MHz
t_{CYC}	Clock Timing (Figure 1) Cycle Time	S6800 S68A00 S68B00	1.000 0.666 0.50	— — —	10 10 10	μs
$PW_{\phi H}$	Clock Pulse Width Measured at V_{CC} − 0.6V	$\phi1$, $\phi2$ — S6800 $\phi1$, $\phi2$ — S68A00 $\phi1$, $\phi2$ — S68B00	400 230 180	— — —	9500 9500 9500	ns ns
t_{UT}	Total $\phi1$ and $\phi2$ Up Time	S6800 S68A00 S68B00	900 600 440	— — —	— — —	ns
$t_{\phi r}$, $t_{\phi f}$	Rise and Fall Times Measured between V_{SS} +0.4 and V_{CC} − 0.6			—	100	ns
t_d	Delay Time or Clock Separation Measured at V_{OV} = V_{SS} +0.6V		0	—	9100	ns

*Except $\overline{IRQ}$ and $\overline{NMI}$, Which require kΩ pullup load resistor for wire-OR capability at optimum operation.
#Capacitances are periodically sampled rather than 100% tested.

Read/Write Timing

Symbol	Characteristics	S6800			S68A00			S68B00			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AD}	Address Delay										ns
	C = 90pF	—	—	270	—	—	180	—	—	150	
	C = 30pF	—	—	250	—	—	165	—	—	135	
t_{ACC}	Periph. Read Access Time $t_{AC} = t_{UT} - (t_{AD} + t_{DSR})$	530	—		360	—		250	—		ns
t_{DSR}	Data Setup Time (Read)	100	—	—	60	—	—	40	—	—	ns
t_H	Input Data Hold Time	10	—	—	10	—	—	10	—	—	ns
t_H	Output Data Hold Time	10	25	—	10	25	—	10	25	—	ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	30	50	—	30	50	—	30	50	—	ns
t_{EH}	Enable High Time for DBE Input	450	—	—	280	—	—	220	—	—	ns
t_{DDW}	Date Delay Time (Write)	—	—	225	—	165	200	—	—	160	ns
	Processor Controls										
t_{PCS}	Proc. Control Setup Time	200	—	—	140	—	—	110	—	—	ns
t_{PCr}; t_{PCf}	Processor Control Rise and Fall Time	—	—	100	—	—	100	—	—	100	ns
t_{BA}	Bus Available Delay	—	—	250	—	—	165	—	—	135	ns
t_{TSE}	Three-State Enable	—	—	40	—	—	40	—	—	40	ns
t_{TSD}	Three-State Delay	—	—	270	—	—	270	—	—	270	ns
$t_{\overline{DBE}}$	Data Bus Enable Down Time During $\phi 1$ Up Time	150	—	—	120	—	—	75	—	—	ns
t_{DBEr}, t_{DBEf}	Data Bus Enable Rise and Fall Times	—	—	25	—	—	25	—	—	25	ns

Figure 1. Clock Timing Waveform

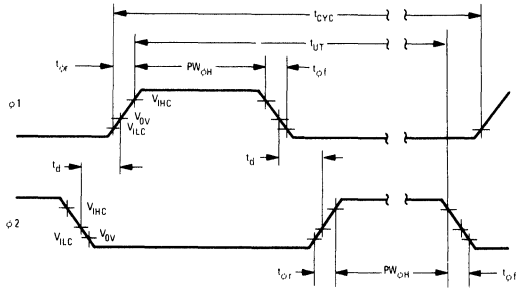
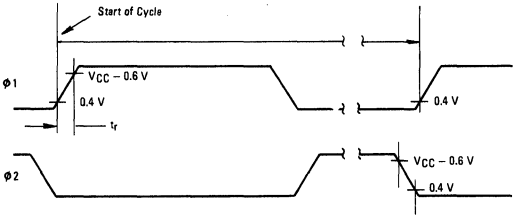


Figure 2. Read/Write Timing Waveform



Measurement point for $\phi 1$ and $\phi 2$ are shown above. Other measurements are the same as for MC6800.

Figure 3. Read Data from Memory or Peripherals

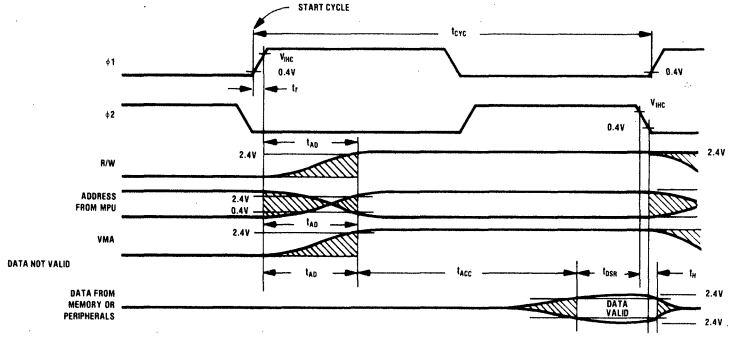


Figure 4. Write Data in Memory or Peripherals

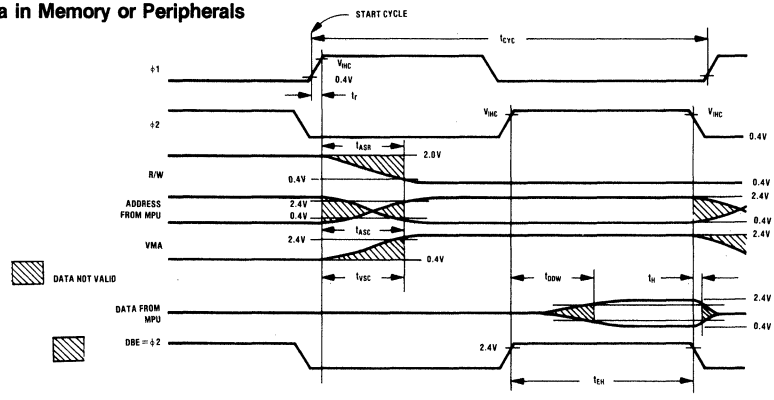
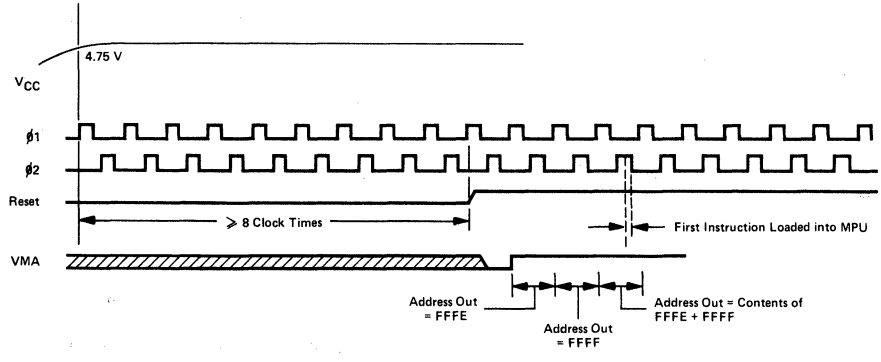


Figure 5. Initialization of MPU After Restart



Interface Description

Label	Pin	Function
ϕ1 ϕ2	(3) (37)	**Clocks Phase One and Phase Two** — Two pins are used for a two-phase non-overlapping clock that runs at the V_{CC} voltage level.
$\overline{\text{RESET}}$	(40)	**$\overline{\text{Reset}}$** — this input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. $\overline{\text{Reset}}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts (Figure 4). If $\overline{\text{Reset}}$ goes high prior to the leading edge of ϕ2, on the next ϕ1 the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.
VMA	(5)	**Valid Memory Address** — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 30pF may be directly driven by this active high signal.
A0 • • •	(9)	**Address Bus** — Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.
A15	(25)	
TSC	(39)	**Three-State Control** — This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 500ns after TSC = 2.4V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The ϕ1 clock must be held in the high state and the ϕ2 in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 50μs or destruction of data will occur in the MPU.
D0 • •	(33)	**Data Bus** — Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load at 130pF.
D7	(26)	
DBE	(36)	**Data Bus Enable** — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it can be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.
R/W	(34)	**Read/Write** — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will Read/Write to the off (high-impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 130pF.
$\overline{\text{HALT}}$	(2)	**$\overline{\text{Halt}}$** — When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction. Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode.

Label	Pin	Function
		Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250ns of phase one. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one Phase One Clock cycle.
BA	(7)	**Bus Available** — The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or non-maskable interrupt. This output is capable of driving one standard TTL load and 30pF.
$\overline{\text{IRQ}}$	(4)	**$\overline{\text{Interrupt Request}}$** — This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An adress loaded at these locations causes the MPU to branch to an interrupt routine in memory. The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be recognized. The $\overline{\text{IRQ}}$ has a high impedance pullup device internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.
$\overline{\text{NMI}}$	(6)	**Non-Maskable Interrupt** —A low-going edge on this input requests that a non-mask interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away in the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory. $\overline{\text{NMI}}$ has a high impedance pullup resistor internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts. Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are acknowledged during $\phi 2$ and will start the interrupt routine on the $\phi 1$ following the completion of an instruction. **INTERRUPTS** — As outlined in the interface description the S6800 requires a 16-bit vector address to indicate the location of routines for Restart, Non-maskable Interrupt, and Maskable Interrupt. Additionally an address is required for the Software Interrupt Instruction (SWI). The processor assumes the uppermost eight memory locations, FFF8 — FFFF, are assigned as interrupt vector addresses as defined in Figure 6. After completing the current instruction execution the processor checks for an allowable interrupt request via the $\overline{\text{IRQ}}$ or $\overline{\text{NMI}}$ inputs as shown by the simplified flow chart in Figure 7. Recognition of either external interrupt request or a Wait for Interrupt (WAI) or Software Interrupt (SWI) instruction causes the contents of the Index Register, Program Counter, Accumulators and Condition Code Register to be transferred to the stack as shown in Figure 8.

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S6801

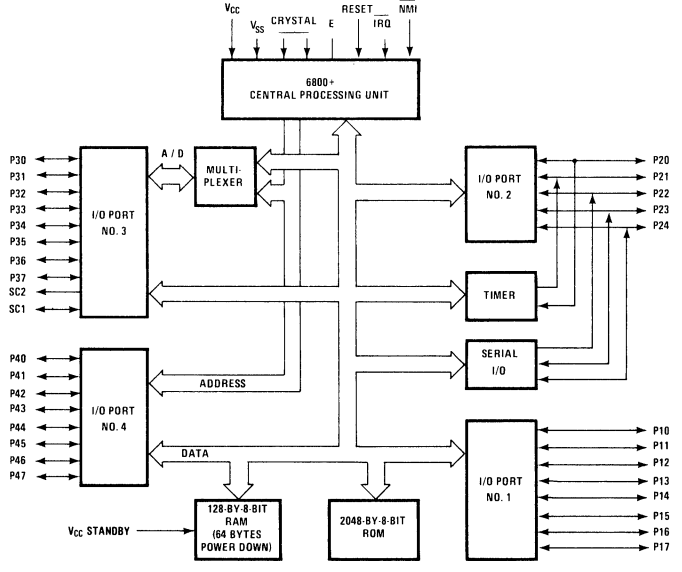
SINGLE CHIP MICROCOMPUTER

Features

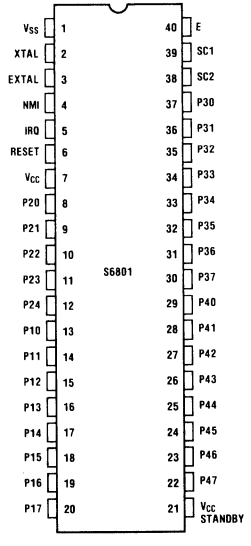
- ☐ Instruction and Addressing Compatible
- ☐ Object Code Compatible
- ☐ 16-Bit Programmable Timer
- ☐ Single Chip or Expandable to 65K Words
- ☐ On-Chip Serial Communications Interface (SCI)
  - — Simplex
  - — Half Duplex
    Mark/Space (NRZ)
    Biphase (FM)
  - — Port Expansion
    Full/Half Duplex
- ☐ Four Internal Baud Rates Available
  $\phi 2 \div 16, 128, 1024, 4096$
- ☐ 2K Bytes of ROM
- ☐ 128 Bytes of RAM
  (64 Bytes Power Down Retainable)
- ☐ 31 Parallel I/O Lines
- ☐ Divide-by-Four Internal Clock
- ☐ Hardware 8 x 8 Multiply
- ☐ Three Operating Modes
  - — Single Chip
  - — Expanded Multiplex (up to 65K Addressing)
  - — Expanded Non-Multiplex
- ☐ Expanded Instruction Set
- ☐ Interrupt Capability
- ☐ Low Cost Versions
  - — S6803—No ROM Version
  - — S6803NR—No ROM or RAM
- ☐ TTL-Compatible with Single 5 Volt Supply

S6800 FAMILY

Block Diagram



Pin Configuration



General Description

The S6801 MCU is an 8-bit single-chip microcomputer system which is compatible with the S6800 family of parts. The S6801 is object code compatible with the S6800 instruction set.

The S6801 features improved execution times of key S6800 instructions including Jump to Subroutine (JSR) and all Conditioned Branches (BRA, etc.). In addition, several new 16-bit and 8-bit instructions have been added including Push/Pull to/from Stack, Hardware 8 × 8 Multiply, and store concatenated A and B accumulators (D accumulator).

The S6801 MCU can be operated in three modes: Single-Chip, Expanded Multiplex (up to 65K Byte Addressing), and Expanded Non-Multiplex. In addition, the S6801 is available with two mask options: an on-chip (÷ 4) Clock, or an external (÷ 1) Clock. The external mode is especially useful in Multiprocessor Applications. The S6801E can be configured as a peripheral by using the Read/Write (R/W), Chip Select (CS), and Register Select (RS). The Read/Write line controls the direction of data on Port 3 and the Register Select (RS) allows for access to either Port 3 data register or control register.

The S6801 Serial Communications Interface (SCI) permits full serial communication using no external components in several operating modes — Full and/or Half Duplex operation — and two formats — Standard Mark/Space for typical Terminal/Modem interfaces and the Bi-Phase (FM, F2F, and Manchester) Format primarily for use between processors. Four software addressable registers are provided to configure the Serial Port; to provide status information; and as transmit/receive data buffers.

The S6801 includes a 16-bit timer with three effectively independent timing functions: (1) Variable pulse width measurement, (2) Variable pulse width generation, and (3) A Timer Overflow — Find Time Flag. This makes the S6801 ideal for applications such as Industrial Controls, Automotive Systems, A/D or D/A Converters, Modems, Real-Time Clocks, and Digital Voltage Controlled Oscillators (VCO).

The S6801 is fully TTL-compatible and requires only a single + 5 volt supply.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	− 0.3V to + 7.0V
Input Voltage, V_{IN}	− 0.3V to + 7.0V
Operating Temperature Range, T_A	0° to + 70°C
Storage Temperature Range, T_{stg}	− 55°C to + 150°C
Thermal Resistance, θ_{JA}	
Plastic	100°C/W
Ceramic	50°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range V_{SS} (V_{IN} or V_{OUT}) V_{DD}.

Electrical Operating Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0 to + 70°C, unless otherwise noted)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage $\overline{\text{Reset}}$	V_{SS} + 2.0 V_{SS} + 4.0		V_{CC} V_{CC}	Vdc
V_{IL}	Input Low Voltage	V_{SS} − 0.3		V_{SS} + 0.8	Vdc
I_{TSI} I_{TSI}	Three-State (Off State) Input Current P10-P17, P30-P37 (V_{IN} = 0.4 to 2.4 Vdc) P20-P24		2.0 10.0	10 100	μAdc μAdc
V_{OH}	Output High Voltage All Outputs Except XTAL 1 and EXTAL 2 I_{LOAD} = 200μAdc	V_{SS} + 2.4			Vdc

Electrical Operating Characteristics (Continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{OL}	Output Low Voltage All Outputs Except XTAL 1 and EXTAL 2 $I_{LOAD} = 1.6$mAdc			$V_{SS} + 0.4$	Vdc
P_D	Power Dissipation			1200	mW
C_{IN}	Capacitance $V_{IN} = 0$, $T_A = 25°C$, $f = 1.0$MHz P10-P17, P20-P24, P40-P47, P30-P37 Reset SC1, SC2, IRQ			 12.5 10 7.5	pF
t_{PDSU}	Peripheral Data Setup Time (Figure 3)	200			ns
t_{PDH}	Peripheral Data Hold Time (Figure 3)	0			ns
t_{OSD1}	Delay Time, Enable Negative Transition to OS3 Neg. Trans.			1.0	μs
t_{OSD2}	Delay Time, Enable Neg. Trans. to OS3 Positive Transition			1.0	μs
t_{PWD}	Delay Time, Enable Negative Transition to Peripheral Data Valid (Figure 4)			350	ns
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral Data Valid ($V_{SS} - 30\%$ V_{CC}, P20-P24 (Figure 4)			2.0	μs
I_{OH}	Darlington Drive Current $V_O = 1.5$Vdc — P10-P17	−10	−2.5	−10	mAdc
V_{SBB} V_{SB}	Standby Voltage (Not Operating) (Operating)	4.00 4.75		5.25 5.25	Vdc

NOTE: The above electricals satisfy Ports 1 and 2 always, and Ports 3 and 4 in the single chip mode only.

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S6802/A/B/S6808/A/B

MICROPROCESSOR WITH CLOCK AND RAM

Features

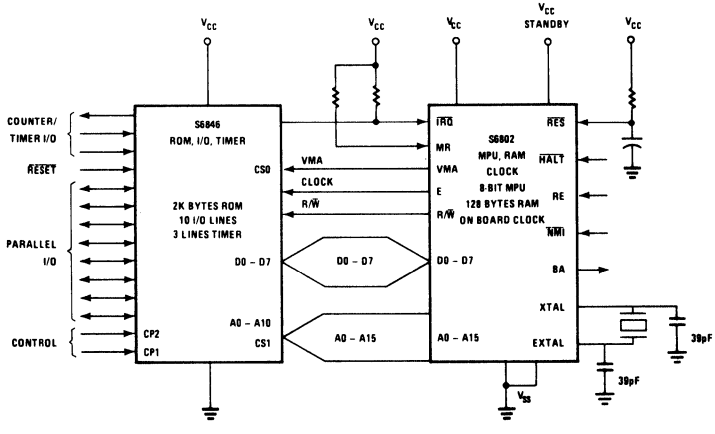
- ☐ On-Chip Clock Circuit
- ☐ 128x8-Bit On-Chip RAM (S6802)
- ☐ 32 Bytes of RAM Are Retainable (S6802)
- ☐ Software-Compatible With the S6800
- ☐ Expandable to 65K Words
- ☐ Standard TTL-Compatible Inputs and Outputs
- ☐ 8-Bit Word Size
- ☐ 16-Bit Memory Addressing
- ☐ Interrupt Capability
- ☐ Clock Rates:
  S6802/S6808—1.0MHz
  S68A02/S68A08—1.5MHz
  S68B02/S68B08—2.0MHz

General Description

The S6802/S6808 are monolithic 8-bit microprocessors that contain all the registers and accumulators of the present S6800 plus an internal clock oscillator and driver on the same chip. In addition, the S6802 has 128 bytes of RAM on board located at hex addresses 0000 to 007E. The first 32 bytes of RAM, at addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation. The S6808 is functionally identical to the S6802 except for the 128 bytes of RAM. The S6808 does not have any RAM.

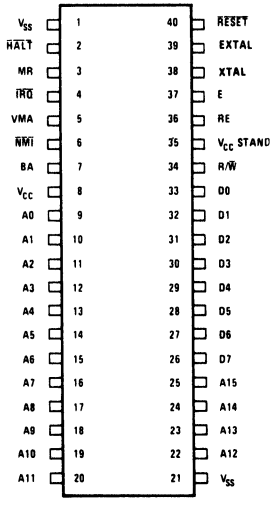
The S6802/S6808 are completely software compatible with the S6800 as well as the entire S6800 family of parts. Hence, the S6802/S6808 are expandable to 65K words. When the S6802 is interfaced with the S6846 ROM-I/O-Timer chip, as shown in the Block Diagram below, a basic 2-chip microcomputer system is realized.

Typical Microcomputer Block Diagram



BLOCK DIAGRAM OF A TYPICAL COST EFFECTIVE MICROCOMPUTER. THE MPU IS THE CENTER OF THE MICROCOMPUTER SYSTEM AND IS SHOWN IN A MINIMUM SYSTEM INTERFACING WITH A ROM COMBINATION CHIP. IT IS NOT INTENDED THAT THIS SYSTEM BE LIMITED TO THIS FUNCTION BUT THAT IT BE EXPANDABLE WITH OTHER PARTS IN THE S6800 MICROCOMPUTER FAMILY.

Pin Configuration



Non-Maskable Interrupt (NMI)—A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the $\overline{\text{Interrupt Request}}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations caused the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{\text{NMI}}$ has a high impedance pull-up resistor internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{MMI}}$ are hardware interrupt lines that are sampled when E is high and will start the interrupt routine on a low E following the completion of an instruction.

Figure 12 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 2 gives the memory map for interrupt vectors.

RAM Enable (RE)—A TTL-compatible RAM enable input controls the on-chip RAM of the S6802. When placed in the high state, the on-chip memory is enabled to respond to the MPU controls. In the low state, RAM is disabled. This pin may also be utilized to disable reading and writing the on-chip RAM during power-down situation. RAM enable must be low three clock cycles before V_{CC} goes below 4.75V during power-down to retain the on board RAM contents during V_{CC} standby.

The Data Bus will be in the output mode when the internal RAM is accessed, which prohibits external data from entering the MPU. Note that the internal RAM is fully decoded from $0000 to $007F and these locations must be disabled when internal RAM is accessed.

Extal and Xtal—The S6802/S6808 has an internal oscillator that may be crystal controlled. These connections are for a parallel resonant fundamental crystal. (AT cut) A divide-by-four circuit has been added to the S6802 so that a 4MHz crystal may be used in lieu of a 1MHz crystal for a more cost effective system. Pin 39 of the S6802/S6808 may be driven externally by a TTL input signal if a separate clock is required. Pin 38 is to be left open in this mode. If the external clock is used it may not be halted for more than 4.5μs. The S6802/S6808 is a dynamic part except for internal RAM, and requires the external clock to retain information. Figure 11a shows the crystal parameters. In applications where other than a 4.0MHz crystal is used, Table 1 gives the designer the crystal parameters to be specified. The table contains the entire spectrum of usable crystals for the S6802/S6808. Crystal frequencies not shown (that lie between 1.0MHz and 4.0MHz) may be interpolated from the table. Figure 11b shows the crystal connection.

Table 1. Crystal Parameters

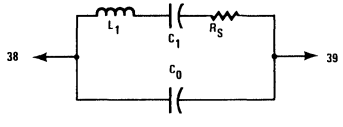
Y1 CRYSTAL FREQUENCY	C1 & C2	C LOAD	R1 (MAX)	C_0 (MAX)
4.0MHz	27pF	24pF	50 ohms	7.0pF
3.58MHz	27pF	20pF	50 ohms	7.0pF
3.0MHz	27pF	18pF	75 ohms	6.7pF
2.5MHz	27pF	18pF	74 ohms	6.0pF
2.0MHz	33pF	24pF	100 ohms	5.5pF
1.5MHz	39pF	27pF	200 ohms	4.5pF
1.0MHz	39pF	30pF	250 ohms	4.0pF

Table 2. Memory Map for Interrupt Vectors

VECTOR MS	VECTOR LS	DESCRIPTION
FFFE	FFFF	RESTART
FFFC	FFFD	NON-MASKABLE INTERRUPT
FFFA	FFFB	SOFTWARE INTERRUPT
FFF8	FFF9	INTERRUPT REQUEST

Note: Memory Read (MR), Halt, RAM Enable (RE) and Non-Maskable interrupt should always be tied to the correct high or low state if not used.

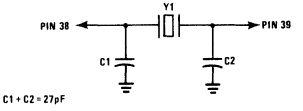
Figure 11a. Crystal Parameters



AT – Cut Parallel Resonance Crystal
C0 = 7pF Max.
FREQ = 4.0MHz @ C_L = 24pF
R_S = 50 ohms Max.
Frequency Tolerance – ±5% to ±0.02%
The best E output "Worst Case Design" tolerance is ± 0.05% (500ppM) using A ±0.02 crystal.

Tolerance Note:
Critical timing loops may require a better tolerance than ±5%. Because of production deviations and the Temperature Coefficient of the S6802, the best "worst case design" tolerance is ±0.05%. (500 ppm) using a ±0.02% crystal. If the S6802 is not going to be used over its entire temperature range of 0°C to 70°C, a much tighter overall tolerance can be achieved.

Figure 11b. Crystal Connection



C1 + C2 = 27pF

S6800 FAMILY

AMI®

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S6805**

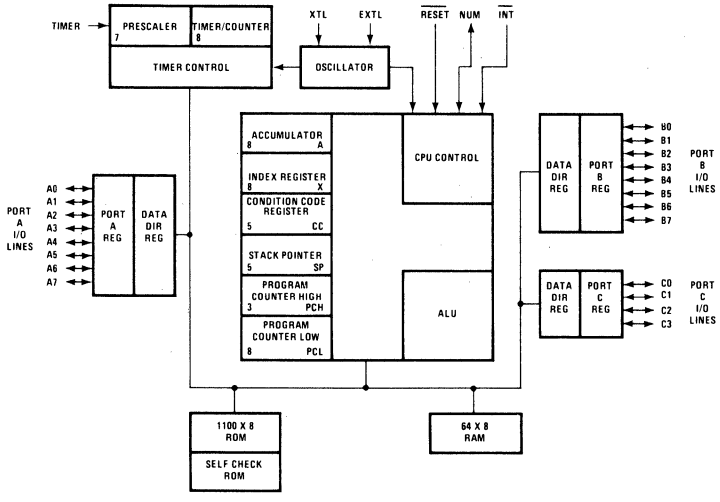
MICROCOMPUTER

Features

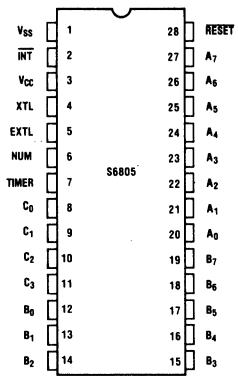
☐ Hardware
- 8-Bit Architecture
- 64 Bytes RAM
- 1100 Bytes ROM
- 116 Bytes of Self Check ROM
- 28-Pin Package
- Memory Mapped I/O
- Internal 8-Bit Timer with 7-Bit Prescaler
- Vectored Interrupts—External, Timer, Software, Reset
- 20 TTL/CMOS Compatible I/O Line 8 Lines LED Compatible
- On-Chip Clock Circuit
- Self-Check Capability
- Low Voltage Inhibit
- 5 Vdc Single Supply

☐ Software
- Similar to 6800
- Byte Efficient Instruction Set
- Versatile Interrupt Handling
- True Bit Manipulation
- Bit Test and Branch Instruction
- Indexed Addressing for Tables
- Memory Usable as Registers/Flags
- 10 Addressing Modes
- Powerful Instruction Set
  - — All 6800 Arithmetic Instructions
  - — All 6800 Logical Instructions
  - — All 6800 Shift Instructions
  - — Single Instruction Memory Examine/Change
  - — Full Set of Conditional Branches

Block Diagram



Pin Configuration



General Description

The S6805 is an 8-bit single chip microcomputer. It is the first member of the growing microcomputer family that contains a CPU, on-chip clock, ROM, RAM, I/O and timer. A basic feature of the 6805 is an instruction set very similar to the S6800 family of microprocessors. Although the 6805 is not strictly source nor object code compatible, an experienced 6800 user can easily write 6805 code. Also a 6805 user will have no trouble moving up to the 6801 or 6809 for more complex tasks.

Absolute Maximum Ratings

Supply Voltage, V_{CC} ..... −0.3V to +7.0V
Input Voltage, V_{IN} ..... −0.3V to +7.0V
Operating Temperature Range, T_A ..... 0° to +70°C
Storage Temperature Range, T_{stg} ..... −55°C to +150°C
Thermal Resistance, θ_{JA}
Plastic ..... 85°C/W
Ceramic ..... 50°C/W
Cerdip ..... 51°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range V_{SS} (V_{IN} or V_{OUT}) + V_{CC}

Electrical Characteristics: V_{CC} = + 5.25 Vdc ± 0.5Vdc, V_{SS} = GND, T_A = 0° —70°C unless otherwise noted

Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	$\overline{RESET}$	4.0	—	V_{CC}	Vdc
V_{IH}		$\overline{INT}$	4.0		V_{CC}	Vdc
V_{IH}		All Other	V_{SS} + 2.0	—	V_{CC}	Vdc
V_{IH}	Input High	Timer Mode	V_{SS} + 2.0	—	V_{CC}	Vdc
V_{IH}	Voltage Timer	Self-Check Mode	—	9.0	15.0	Vdc
V_{IL}	Input Low Voltage	$\overline{RESET}$	V_{SS} − 0.3	—	0.8	Vdc
V_{IL}		$\overline{INT}$	V_{SS} − 0.3		1.5	Vdc
V_{IL}		All Other	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc
V_H	$\overline{INT}$ Hysteresis		—	100	—	mV_{CC}
P_D	Power Dissipation		—	350	—	mW
C_{IN}	Input Capacitance	EXTL	—	25	—	pF
C_{IN}		All Other	—	10	—	pF
LVR	Low Voltage Recover		—	—	4.75	Vdc
LVI	Low Voltage Inhibit		—	4.5	—	

Switching Characteristics: V_{CC} = + 5.25 V ± 0.5 Vdc, V_{SS} = GND, T_A = 0° — + 70°C unless otherwise noted

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{cl}	Clock Frequency	0.4	—	4.0	MHz
t_{CYC}	Cycle Time	1.0	—	10	μs
t_{IWL}	$\overline{INT}$ Pulse Width	t_{CYC} + 250	—	—	ns
t_{RWL}	$\overline{RESET}$ Pulse Width	t_{CYC} + 250	—	—	ns
t_{RHL}	Delay Time Reset (External Cap. = 0.47μF)	20	50	—	ms

Port Electrical Characteristics: V_{CC} = + 5.25 Vdc ± 0.5 Vdc, V_{SS} = GND, T_A = 0° — + 70°C unless otherwise noted

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Condition
			Port A			
V_{OL}	Output Low Voltage	—	—	0.4	Vdc	I_{LOAD} = 1.6mAdc
V_{OH}	Output High Voltage	2.4	—	—	Vdc	I_{LOAD} = 100μAdc
V_{OH}	Output High Voltage	3.5	—	—	Vdc	I_{LOAD} = − 10μAdc
V_{IH}	Input High Voltage	V_{SS} + 2.0	—	V_{CC}	Vdc	I_{LOAD} = − 300μAdc (max)
V_{IL}	Input Low Voltage	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc	I_{LOAD} = 500μAdc (max)
			Port B			
V_{OL}	Output Low Voltage	—	—	0.4	Vdc	I_{LOAD} = 3.2mAdc
V_{OL}	Output Low Voltage	—	—	1.0	Vdc	I_{LOAD} = 10mAdc(sink)
V_{OH}	Output High Voltage	2.4	—	—	Vdc	I_{LOAD} = − 200μAdc
I_{OH}	Darlington Current Drive (Source)	− 1.0	—	− 10	mAdc	V_O = 1.5Vdc
V_{IH}	Input High Voltage	V_{SS} + 2.0	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc	
			Port C			
V_{OL}	Output Low Voltage	—	—	0.4	Vdc	I_{LOAD} = 1.6mAdc
V_{OH}	Output High Voltage	2.4	—	—	Vdc	I_{LOAD} − − 100μAdc
V_{IH}	Input High Voltage	V_{SS} + 2.0	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc	
			Off-State Input Current			
I_{TSI}	Three-State Ports B & C	—	2	20	μAdc	
			Input Current			
I_{IN}	Timer at V_{IN} = (0.4 to 2.4 Vdc)	—	—	20	μAdc	

Figure 1. TTL Equiv. Test Load (Port B)

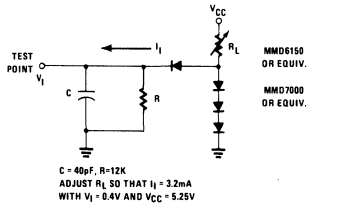


Figure 2. CMOS Equiv. Test Load (Port A)

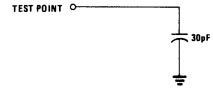
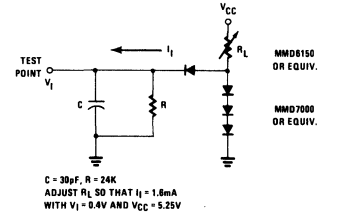


Figure 3. TTL Equiv. Test Load (Ports A and C)



Pin Description

Pin	Symbol	Description
1 and 3	V_{CC} and V_{SS}	Power is supplied to the MCU using these two pins. V_{CC} is 5.25V ± .5V, and V_{SS} is the ground connection.
2	$\overline{INT}$	External Interrupt provides capability to apply an external interrupt to the MCU.
4 and 5	XTL and EXTL	Provide control input for the on-chip clock circuit. The use of crystal (at cut 4MHz maximum), a resistor or a wire jumper is sufficient to drive the internal oscillator with varying degrees of stability. (See Internal Oscillator Options for recommendations) An internal divide by 4 prescaler scales the frequency down to the appropriate f2 clock rate (1MHz maximum).
6	NUM	This pin is not for user application and should be connected to ground.
7	TIMER	Allows an external input to be used to decrement the internal timer circuitry. See TIMER for detailed information about the timer circuitry.
8-11 12-19 20-27	C0-C3 B0-B7 A0-A7	Input/Output lines (A0-A7, B0-B7, C0-C3). The 20 lines are arranged into two 8-bit ports (A and B) and one 4-bit port (C). All lines are programmed as either inputs or outputs under software control of the data direction registers. See Inputs/Outputs for additional information.
28	RESET	This pin allows resetting of the MCU. A low voltage detect feature responds to a dip in voltage by forcing a RESET condition to clear all Data Direction Registers, so that all I/O pins are set as inputs.

Memory

The MCU memory is configured as shown in Figure 4. During the processing of an interrupt, the contents of the MCU registers are pushed onto the stack in the order shown in Figure 5. Since the stack pointer decrements during pushes, the low order byte (PCL) of the program counter is stacked first, then the high order three bits (PCH) are stacked first, then the high order three bits (PCH) are stacked. This ensures that the program counter is loaded correctly as the stack pointer increments when it pulls data from the stack. A subroutine call will cause only the program counter (PCH, PCL) contents to be pushed onto the stack.

Figure 4. MCU Memory Configuration

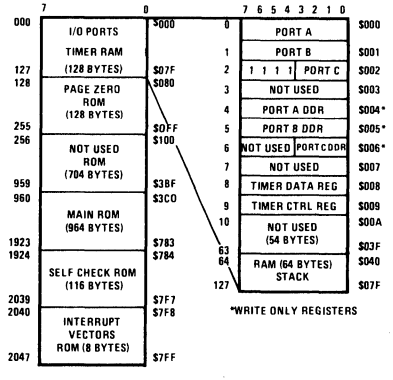


Figure 5. Interrupt Stacking Order

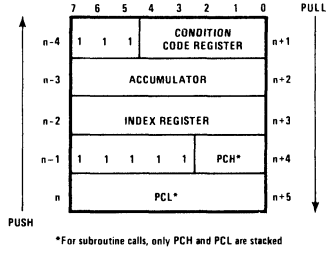
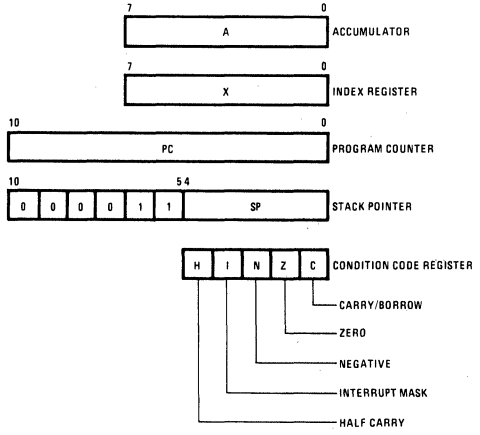


Figure 6. Programming Model



Registers

The S6805 MCU contains two 8-bit registers (A and X), one 11-bit register (PC), two 5-bit registers (SP and CC) that are visible to the programmer (see Figure 6).

Accumulator (A)

The A-register is an 8-bit general purpose accumulator used for arithmetic calculations and data manipulation.

Index Register (X)

This 8-bit register is used for the indexed addressing mode. It provides an 8-bit address that may be added to an offset to create an effective address. The index register can also be used for limited calculations and data manipulations when using the read/modify/write instructions. In code sequences not employing the index register it can be used as a temporary storage area.

Program Counter (PC)

This 11-bit register contains the address of the next instruction to be executed.

Stack Pointer (SP)

The stack pointer is an 11-bit register that contains the address of the next free location on the stack. Initially, the stack pointer is set to location $07F and is decremented as data is being pushed onto the stack and incremented as data is being pulled from the stack. The six most significant bits of the stack pointer are permanently set to 000011. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $07F. Subroutines and interrupts may be nested down to location $061 which allows the programmer to use up to 15 levels of subroutine calls. A 16th subroutine call would save the return address correctly, but the stack pointer would not remain pointing into the stack area and there would be no way to return from any of the subroutines.

Condition Code Register (CC)

The condition code register is a 5-bit register in which each bit is used to indicate or flag the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each individual condition code register bit is explained in the following paragraphs.

HALF CARRY (H)—Used during arithmetic operations (ADD and ADC) to indicate that a carry occurred between bits 3 and 4.

INTERRUPT (I)—This bit is set to mask the timer and external interrupt ($\overline{INT}$). If an interrupt occurs while this bit is set it is latched and will be processed as soon as the interrupt bit is reset.

NEGATIVE (N)—USED TO INDICATE that the result of the last arithmetic, logical or data manipulation was negative (bit 7 in result equal to a logical one).

ZERO (Z)—Used to indicate that the result of the last arithmetic, logical or data manipulation was zero.

CARRY/BORROW (C)—Used to indicate that a carry or borrow out of the arithmetic logic until (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts and rotates.

Timer

The MCU timer circuitry is shown in Figure 7. The 8-bit counter is loaded under program control and counts down toward zero as soon as the clock input is applied. When the timer reaches zero the timer interrupt request bit (bit 7) in the timer control register is set. The MCU responds to this interrupt by saving the present MCU state in the stack, fetching the timer interrupt vector from locations $7F8 and $7F9 and executing the interrupt routine. The timer interrupt can be masked by setting the timer interrupt mask bit (bit 6) in the timer control register. The interupt bit (bit 1) in the condition code register will also prevent a timer interrupt from being processed.

The clock input to the timer can be from an external source applied to the TIMER input pin or it can be the internal ϕ2 signal. Note that when ϕ2 signal is used as the source it can be gated by an input applied to the TIMER input pin allowing the user to easily perform pulse-width measurements. The source of the clock input is one of the options that has to be specified before manufacture of the MCU. A prescaler option can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before being applied to the counter. This prescaling option must also be specified before manufacturing begins. The timer continues to count past zero and its present count can be monitored at any time by monitoring the timer data register. This allows a program to determine the length of time since a timer interrupt has occurred and not disturb the counting process.

At power up or reset the prescaler and counter are initialized with all logical ones; the timer interrupt request bit (bit 7) is cleared and the timer request mask bit (bit 6) is set.

Self Check Mode:

The MCU includes a non-user mode pin that replaces the normal operating mode with one in which the internal data and address buses are available at the I/O ports. The ports are configured as follows in the test mode (some multiplexing of the address and data lines is necessary):

- The internal ROM and RAM are disabled and Port A becomes the input data bus on the ϕ2 of the clock and can be used to supply instructions of data to the MCU.
- Port B is also multiplexed. When ϕ2 is high, Port B is the output data bus, and when ϕ2 is low Port B is the address lines. The output data bus can be used to monitor the internal ROM or RAM.
- Port C becomes the last three address lines and a read/write control line.

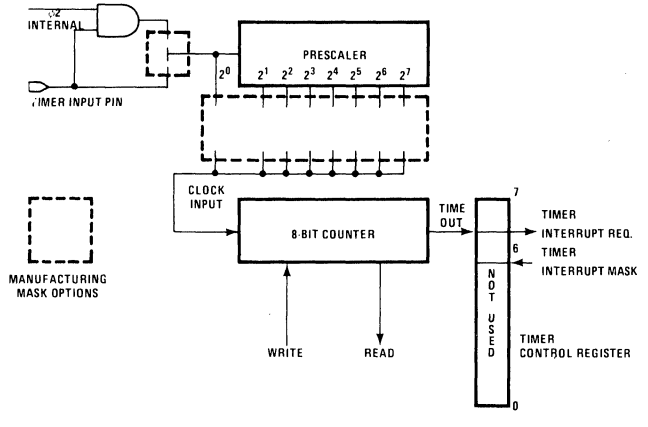
The MCU incorporates a self test program within a 116 byte non-user accessable test program and some control logic on-chip. These 116 bytes of ROM test every addressing mode and nearly every CPU instruction (95% of the total microprocessor capability) while only adding 1% to the total overall die size.

To perform the self test, the MCU output lines of Port A and B must be externally interconnected (Figure 7) and LED's are connected to Port C to provide both a pass/fail indication (3Hz square wave).

The flowchart for the self test program (Figure 8) runs four tests:

- **I/O TEST:** Tests for I/O lines that are stuck in high, low, shorted state, or are missing a connection. The I/O lines are all externally wired together so that the program can look for problems by testing for the correct operation of the lines as inputs and outputs and for shorts between two adjacent lines.
- **ROM ERROR:** (Checksum wrong). The checksum value of the user program must be masked into the self check ROM when the microcomputer is built. The self check program then tests the user ROM by computing the checksum value, which should be equal to the masked checksum if all the bits in the ROM are prop-

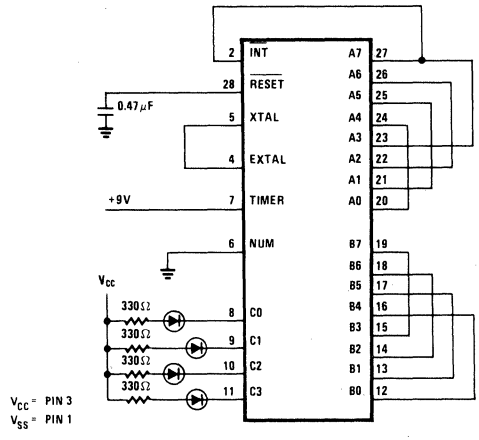
Figure 7. Timer Block Diagram



erly masked. Address and data lines that are stuck high, low or to each other are also detected by this test. An inoperable ROM will (in most cases) prevent the running of the self check program.

• **RAM Bits Non-Functional**: The RAM is tested by the use of a walking bit pattern that is written into memory and then verified. Every in RAM is set to one and then to zero by using 9 different patterns as shown in Figure 9.

Figure 8. Interconnected Ports for Self Check Mode. Port C Gives Go/No Go and Diagnostic Information.



Self Test Routines

Program performs four main tests in the major loops and provides an output signal to indicate that the part is functional.

Interrupt Logic Failure: Using an I/O line the interrupt pin is toggled to create an interrupt. The main program runs long enough to allow the timer to underflow and causes the timer interrupt to be enabled.

If all of these tests are successful the program, then loops back to the beginning and starts testing again.

The self check program initially tries to get the MCU out of the reset state to indicate that the processor is at least working. The non-functional parts are thus immediately eliminated, and if the part fails at this first stage the program provides a means of determining the faulty section.

To place the MCU in the self check mode the voltage on the timer input (Figure 7) is raised to 8 volts which causes several operations to take place:

Figure 9. Flowchart of Self Test Routine

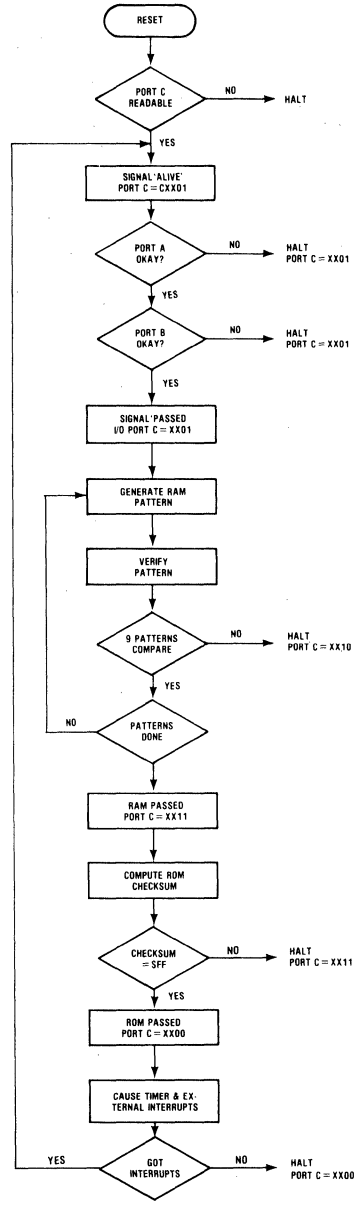


Figure 10. RAM Test Pattern

PATTERN #1

0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	0	0	1	0	0	0	0
•							
•							
•							
•							
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0

PATTERN #2

1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	0
•							
•							
•							
•							
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0

PATTERN #8

0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
•							
•							
•							
•							
0	0	0	0	1	0	0	0
0	0	0	0	0	1	0	0
0	0	0	0	0	0	1	0

PATTERN #9

0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0
•							
•							
•							
•							
0	0	0	0	0	1	0	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1

- The clocking source for the timer is shunted to the MCU internal clock to insure that the timer will run an underflow during the course of the program, no matter which clocking rate is masked.
- The address of the interrupt vectors (including the reset vector) are mapped into the self check ROM area. This allows the self check to test the interrupt structure.

The self check program is started by the reset signal instead of the normal program because the vectors (including the reset vector) have been overlaid. The self check program runs in an endless loop testing and retesting the processor as long as there are no errors. Signals on the I/O lines indicate that the test has passed, and if any test fails, the program stops by executing a branch to self instruction. The output lines then cease to toggle and two of the I/O lines will indicate the cause of failure.

RAM Test Pattern

"Walking bit" patterns test sequence sets and resets every bit in memory. (See Figure 10.)

Low Voltage Inhibit

As soon as the voltage at pin 3 (V_{CC}) falls to 4.5 volts, all I/O lines are put into a high impedance state. This prevents erroneous data from being given to an external device. When V_{CC} climbs back up to 4.6 volts a vectored reset is performed.

Table 1. Cause of Chip Failure as Shown in Bits 0 and 1 of I/O Port C

BIT 1	BIT 0	REASON FOR FAILURE
0	0	INTERRUPTS
0	1	I/O PORTS A OR B
1	0	RAM
1	1	ROM

Figure 11. Power Up and Reset Timing

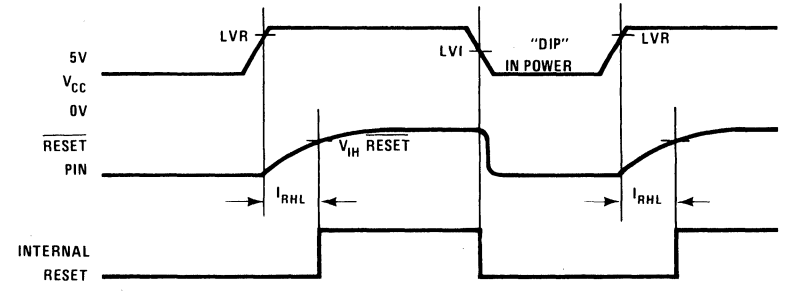
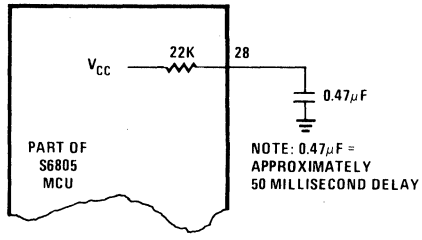


Figure 12. Power Up Reset Delay Circuit



Resets

The MCU can be reset three ways; by the external reset input ($\overline{\text{RESET}}$), by the internal low voltage detect circuit already mentioned, and during the power up time. (See Figure 11.)

Upon power up, a minimum of 20 milliseconds is needed before allowing the reset input to go high. This time allows the internal oscillator to stabilize. Connecting a capacitor to the $\overline{\text{RESET}}$ input as shown in Figure 12 will provide sufficient delay.

Internal Oscillator Options

The internal oscillator circuit has been designed to require a minimum of external components. The use of a crystal (AT cut, 4MHz max) or a resistor is sufficient to drive the internal oscillator with varying degrees of stability. A manufacturing mask option is available to provide better matching between the external components and the internal oscillator.

The different connection methods are shown in Figure 13. Crystal specifications are given in Figure 14. A resistor selection graph is given in Figure 15.

Figure 13. Internal Oscillator Options

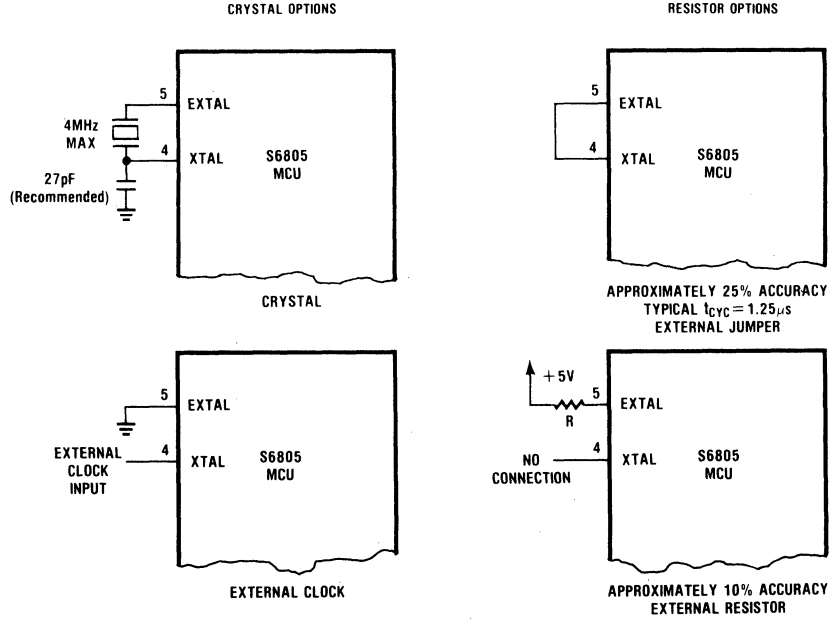
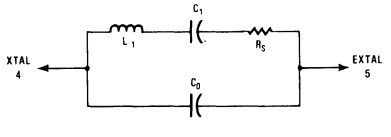
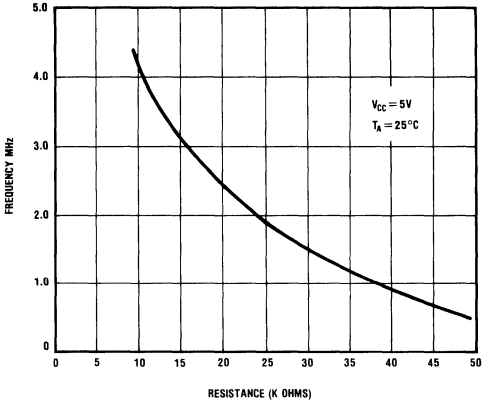


Figure 14. Crystal Parameters



AT–CUT PARALLEL RESONANCE CRYSTAL
C_0 = 7pF MAX
FREQ = 4.0MHz @ C_L = 24pF
R_S = 50 OHMS MAX

Figure 15. Typical Resistor Selection Graph



Interrupts

The MCU can be interrupted three different ways; through the external interrupt ($\overline{INT}$) input pin, the internal timer interrupt request, and a software interrupt instruction (SWI). When any interrupt occurs, processing is suspended, the present MCU state is pushed onto the stack, the interrupt bit (I) in the condition code register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. The interrupt service routines normally end with a return from interrupt (RTI) instruction which allows the MCU to resume processing of the program prior to the interrupt. Table 2 provides a listing of the interrupts, their priority, and the vector address that contain the starting address of the appropriate interrupt routine.

A sinusodial signal (1kHz maximum) can be used to generate an external interrupt ($\overline{INT}$) as shown in Figure 16.

A flowchart of the interrupt processing sequence is given in Figure 17.

Table 2. Interrupt Priorities

Interrupt	Priority	Vector Address
$\overline{RESET}$	1	$7FE AND $7FF
SWI	2	$7FC AND $7FD
$\overline{INT}$	3	$7FA AND $7FB
TIMER	4	$7F8 AND $7F9

Input/Output

There are 20 input/output pins. All pins are programmable as either inputs or outputs under software control of the data direction registers. When programmed as outputs, all I/O pins read latched output data regardless of the logic level at the output pin due to output loading (see Figure 18). When port B is programmed for outputs, it is capable of sinking 10 milliamperes on each pin (one volt maximum). All input/output lines are TTL compatible as both inputs and outputs. Port A lines are CMOS compatible as outputs while Port B and C lines are CMOS compatible as inputs. Figure 19 provides some examples of port connections.

Figure 16. Typical Sinusodial Interrupt Circuits

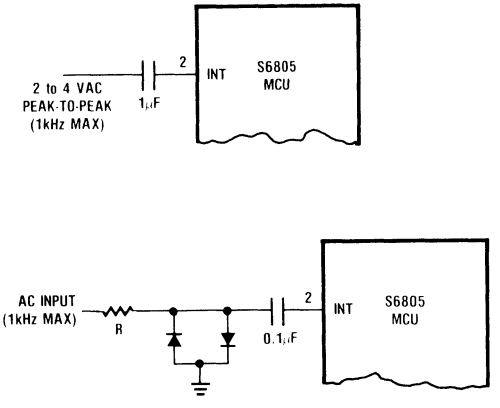


Figure 17. Interrupt Processing Flowchart

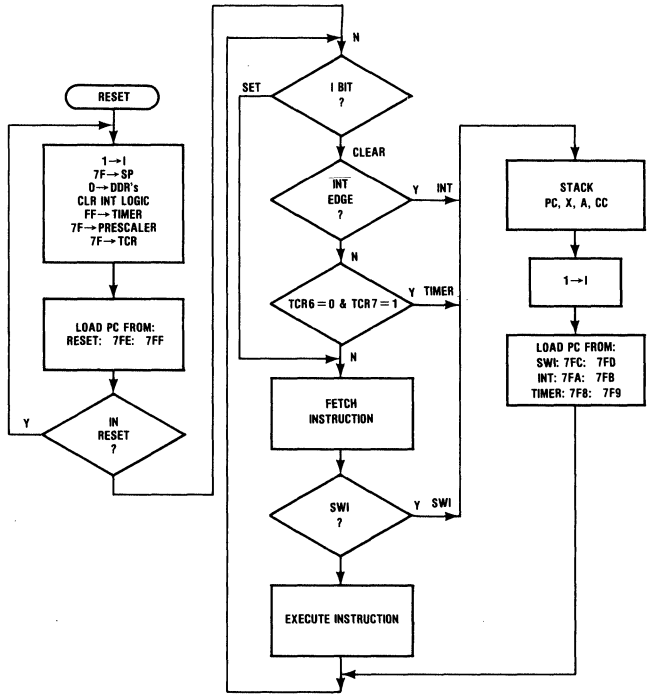
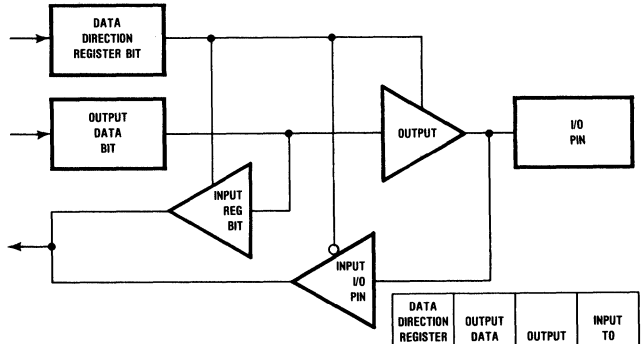
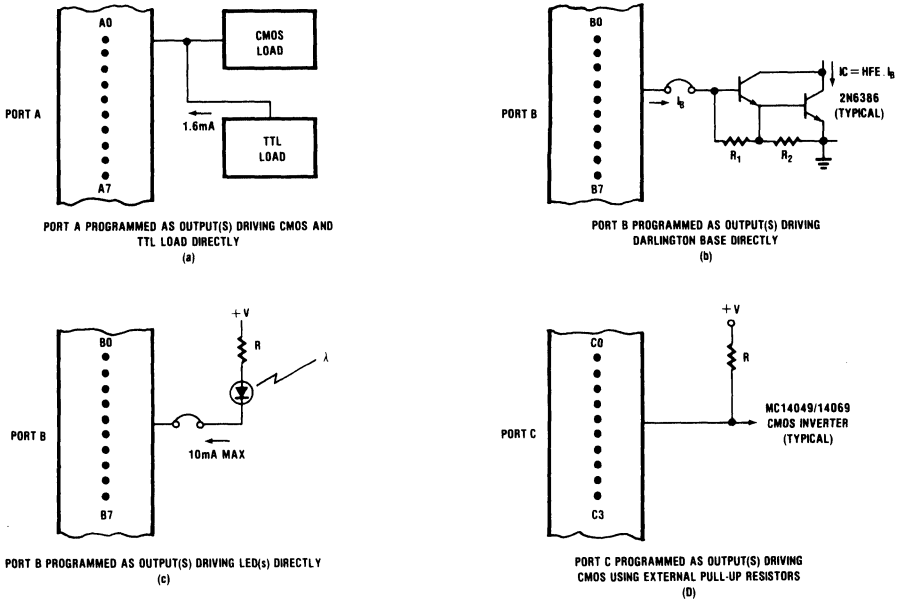


Figure 18. Typical Port I/O Circuitry



DATA DIRECTION REGISTER BIT	OUTPUT DATA BIT	OUTPUT STATE	INPUT TO MCU
1	0	0	0
1	1	1	1
0	X	3-STATE	PIN

Figure 19. Typical Port Connections



Bit Manipulation

The MCU has the ability to set or clear any single random access memory or input/output bit (except the data direction registers) with a single instruction (BSET, BCLR). Any bit in the page zero read only memory can be tested, using the BRSET and BRCLR instructions, and the program branches as a result of its state. This capability to work with any bit in RAM, ROM or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines. The example in Figure 20 illustrates the usefulness of the bit manipulation and test instructions. Assume that bit 0 of port A is connected to a zero crossing detector circuit and that bit 1 of port A is connected to the trigger of a TRIAC which powers the controlled hardware.

This program, which uses only seven ROM locations, provides turn-on of the TRIAC within 14 microseconds of the zero crossing. The timer could also be incorporated to provide turn-on at some later time which would permit pulse-width modulation of the controlled power.

Addressing Modes

The MCU has ten addressing modes available for use by the programmer. They are explained and illustrated briefly in the following paragraphs.

Figure 20. Bit Manipulation Example

```
        •
        •
        •
        •
        •
SELF 1  BRCLR 0, PORTA, SELF 1
        BSET 1, PORTA
        BCLR 1, PORTA
        •
        •
        •
        •
        •
```

Immediate—Refer to Figure 21. The immediate addressing mode accesses constants which do not change during program execution. Such instructions are two bytes long. The effective address (EA) is the PC and the operand is fetched from the byte following the opcode.

Direct—Refer to Figure 22 in direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in memory. All RAM space, I/O registers and 128 bytes of ROM are located in page zero to take advantage of this efficient memory addressing mode.

Extended—Refer to Figure 23. Extended addressing is used to reference any location in memory space. The EA is the contents of the two bytes following the opcode. Extended addressing instructions are three bytes long.

Relative—Refer to Figure 24. The relative addressing mode applies only to the branch instructions. In this mode the contents of the byte following the opcode is added to the program counter when the branch is taken. EA = (PC) + 2 + Rel. Rel is the contents of the location following the instruction opcode with bit 7 being the sign bit. If the branch is not tken Rel = 0, when a branch takes place, the program goes to somewhere within the range of + 129 bytes to − 127 of the present instruction. These instructions are two bytes long.

Indexed (No Offset)—Refer to Figure 25. This mode of addressing accesses the lowest 256 bytes of memory. These instructions are one byte long and their EA is the contents of the index register.

Indexed (8-Bit Offset)—Refer to Figure 26. The EA is calculated by adding the contents of the byte following the opcode to the contents of the index register. In this mode, 511 low memory locations are accessable. These instructions occupy two bytes.

Indexed (16-Bit Offset)—Refer to Figure 27. This addressing mode calculates the EA by adding the contents of the two bytes following the opcode to the index register. Thus, the entire memory space may be accessed. Instructions which use this addressing mode are three bytes long.

Bit Set/Clear—Refer to Figure 28. This mode of addressing applies to instructions which can set or clear any bit on page zero. The lower three bits in the opcode specify the bit to be set or cleared while the byte following the opcode specifies the address in page zero

Bit Test and Branch—Refer to Figure 29. This mode of addressing applies to instructions which can test any bit in the first 256 locations ($00-$FF) and branch to any location relative to the PC. The byte to be tested is addressed by the byte following the opcode. The individual bit within that byte to be tested is addressed by the lower three bits of the opcode. The third byte is the relative address to be added to the program counter if the branch condition is met. These instructions are three bytes long. The value of the bit tested is written to the carry bit in the condition code register.

Inherent—Refer to Figure 30. The inherent mode of addressing has no EA. All the information necessary to execute an instruction is contained in the opcode. Direct operations on the accumulator and the index register are included in this mode of addressing. In addition, control instructions such as SWI. RTI belong to this group. All inherent addressing instructions are one byte long.

Figure 21. Immediate Addressing Example

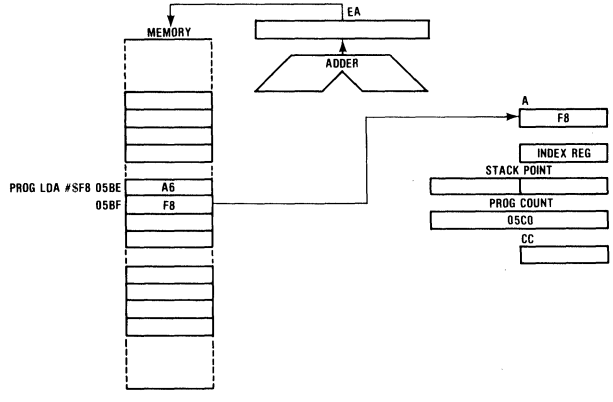


Figure 22. Direct Addressing Example

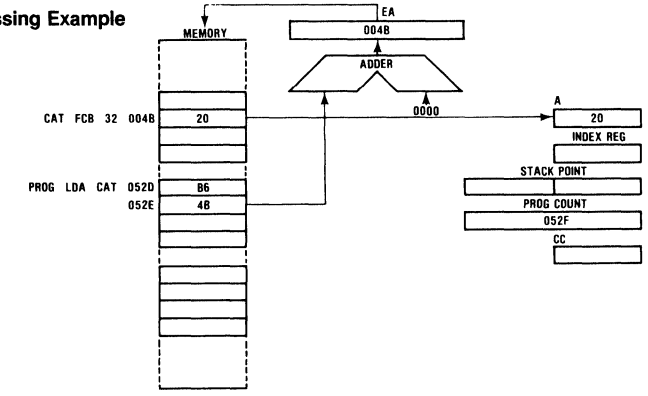


Figure 23. Extended Addressing Example

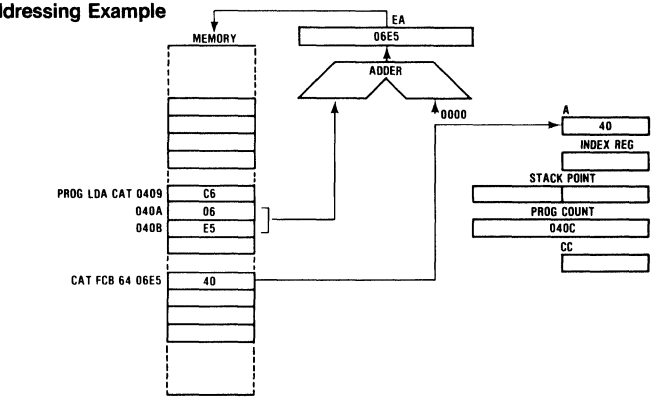


Figure 24. Relative Addressing Example

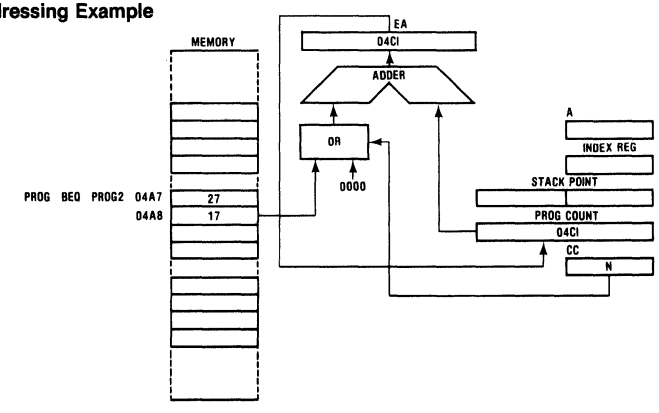


Figure 25. Indexed (No Offset) Addressing Example

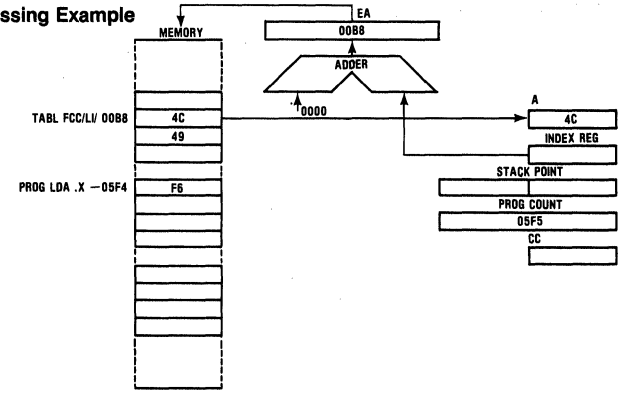


Figure 26. Indexed (8-Bit Offset) Addressing Example

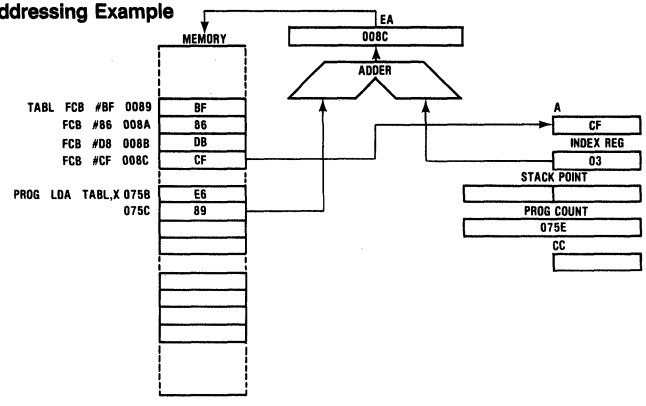


Figure 27. Indexed (16-Bit Offset) Addressing Example

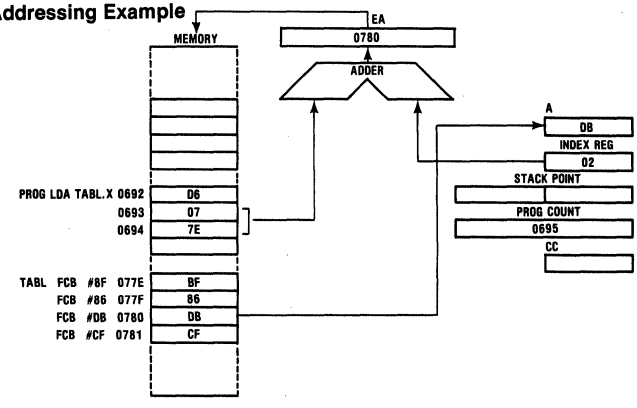


Figure 28. Bit Set/Clear Addressing Example

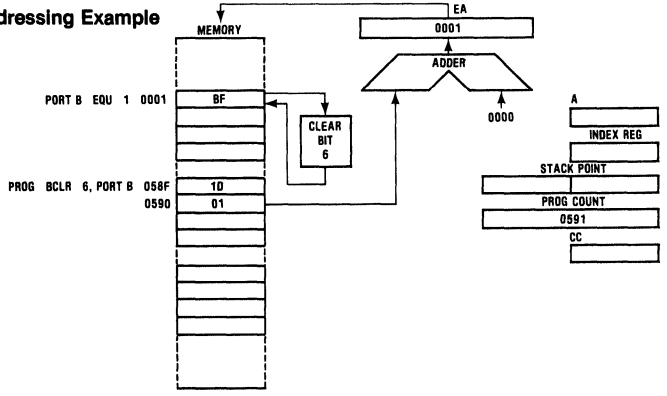


Figure 29. Bit Test and Branch Addressing Example

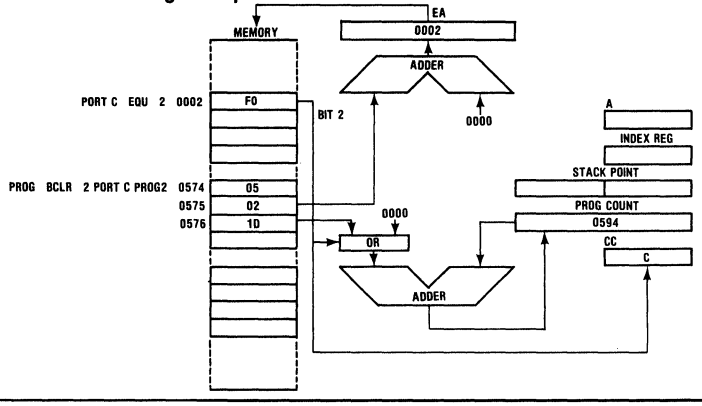
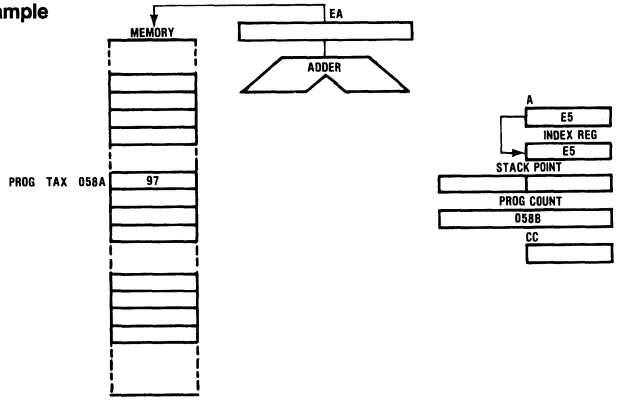


Figure 30. Inherent Addressing Example



Instruction Set

The MCU has a set of 59 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

Register/Memory Instructions—Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 3.

Read/Modify/Write Instructions—These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read/modify/write instructions since it does not perform the write. Refer to Table 4.

Branch Instructions—The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 5.

Bit Manipulation Instructions—These instructions are used on any bit in the first 256 bytes of the memory. One group either sets or clears. The other group performs the bit test and branch operations. Refer to Table 6.

Control Instructions—The control instructions control the MCU operations during program execution. Refer to Table 7.

Alphabetical Listing—The complete instruction set is given in alphabetical order in Table 8.

Opcode Map—Table 9 is an opcode map for the instructions used on the MCU.

Table 3. Register/Memory Instructions

		ADDRESSING MODES																	
		IMMEDIATE			DIRECT			EXTENDED			INDEXED (No Offset)			INDEXED (8-Bit Offset)			INDEXED 16-Bit Offset		
Function	Mnemonic	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles
LOAD A FROM MEMORY	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6
LOAD X FROM MEMORY	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6
STORE A IN MEMORY	STA	—	—	—	B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7
STORE X IN MEMORY	STX	—	—	—	BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7
ADD MEMORY TO A	ADD	AE	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
ADD MEMORY AND CARRY TO A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6
SUBTRACT MEMORY	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6
SUBTRACT MEMORY FROM A WITH BORROW	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6
AND MEMORY TO A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6
OR MEMORY WITH A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6
EXCLUSIVE OR MEMORY WITH A	EOR	A8	2	2	B8	2	4	C8	3	5	F8	1	4	E8	2	5	D8	3	6
ARITHMETIC COMPARE A WITH MEMORY	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6
ARITHMETIC COMPARE X WITH MEMORY	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6
BIT TEST MEMORY WITH A (Logical Compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6
JUMP UNCONDITIONAL	JMP	—	—	—	BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5
JUMP TO SUBROUTINE	JSR	—	—	—	BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9

Table 4. Read/Modify/Write Instructions

		ADDRESSING MODES														
		INHERENT (A)			INHERENT (X)			DIRECT			INDEXED (No Offset)			INDEXED (8-Bit Offset)		
Function	Mnemonic	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	OP Cycles	# Code	# Bytes	Cycles
INCREMENT	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
DECREMENT	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
CLEAR	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
COMPLEMENT	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
NEGATE (2's COMPLEMENT)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
ROTATE LEFT THRU CARRY	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
ROTATE RIGHT THRU CARRY	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
LOGICAL SHIFT LEFT	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
LOGICAL SHIFT RIGHT	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
ARITHMETIC SHIFT RIGHT	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
TEST FOR NEGATIVE OR ZERO	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

Table 5. Branch Instructions

		RELATIVE ADDRESSING MODE		
Function	Mnemonic	OP Code	# Bytes	# Cycles
BRANCH ALWAYS	BRA	20	2	4
BRANCH NEVER	BRN	21	2	4
BRANCH IFF HIGHER	BHI	22	2	4
BRANCH IFF LOWER OR SAME	BLS	23	2	4
BRANCH IFF CARRY CLEAR	BCC	24	2	4
(BRANCH IFF HIGHER OR SAME)	(BHS)	24	2	4
BRANCH IFF CARRY SET	BCS	25	2	4
(BRANCH IFF LOWER)	(BLO)	25	2	4
BRANCH IFF NOT EQUAL	BNE	26	2	4
BRANCH IFF EQUAL	BEQ	27	2	4
BRANCH IFF HALF CARRY CLEAR	BHCC	28	2	4
BRANCH IFF HALF CARRY SET	BHCS	29	2	4
BRANCH IFF PLUS	BPL	2A	2	4
BRANCH IFF MINUS	BMI	2B	2	4
BRANCH IFF INTERRUPT MASK BIT IS CLEAR	BMC	2C	2	4
BRANCH IFF INTERRUPT MASK BIT IS SET	BMS	2D	2	4
BRANCH IFF INTERRUPT LINE IS LOW	BIL	2E	2	4
BRANCH IFF INTERRUPT LINE IS HIGH	BIH	2F	2	4
BRANCH TO SUBROUTINE	BSR	AD	2	8

AMI

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S6809/S68A09/S68B09**

8-BIT MICROPROCESSING UNIT

Features

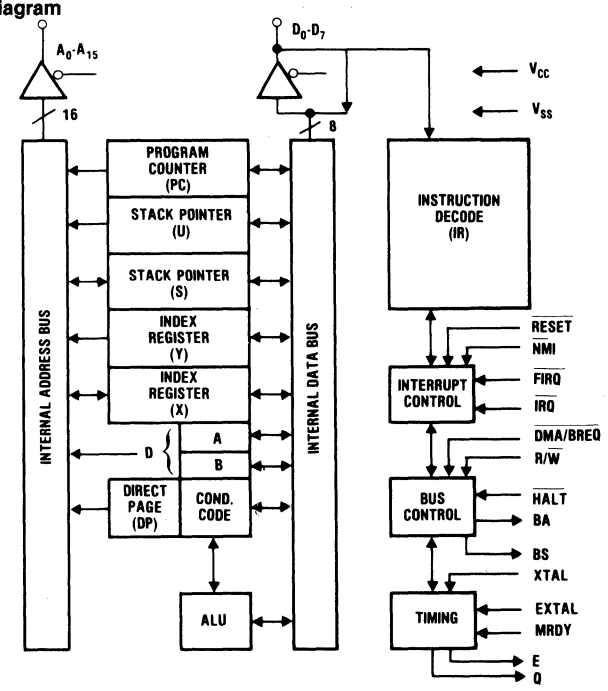
- ☐ Interfaces With All S6800 Peripherals
- ☐ Upward Compatible Instruction Set and Addressing Modes
- ☐ Upward Source Compatible Instruction Set and Addressing Modes
- ☐ Two 8-Bit Accumulators Can Be Concatenated Into One 16-Bit Accumulator
- ☐ On-Chip Crystal Oscillator (4 times XTAL)

General Description

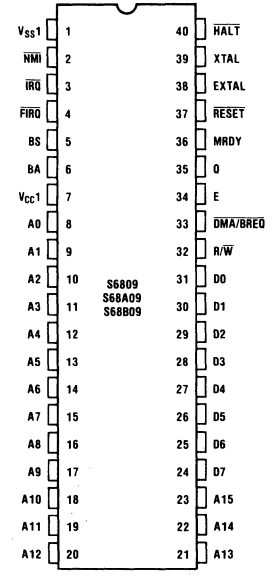
The S6809 is an advanced processor within the S6800 family offering greater throughput, improved byte efficiency, and increased adaptability to various software disciplines. These include position independence, reentrancy, recursion, block structuring, and high level language generation.

Because the S6809 generates position-independent code, software can be written in modular form for easy user expansion as system requirements increase. The S6809 is hardware compatible with all S6800 peripherals, and any assembly language code prepared for the S6800 can be passed through the S6809 assembler to produce code which will run on the S6809.

Block Diagram



Pin Configuration



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Preliminary Data Sheet | **S6809E/S68A09E/S68B09E**

8-BIT MICROPROCESSING UNIT

Features

- ☐ Interfaces With All S6800 Peripherals
- ☐ Upward Compatible Instruction Set and Addressing Modes
- ☐ Upward Source Compatible Instruction Set and Addressing Modes
- ☐ Two 8-Bit Accumulators Can Be Concatenated Into One 16-Bit Accumulator
- ☐ External Clock Inputs, E and Q, Allow System Synchronization

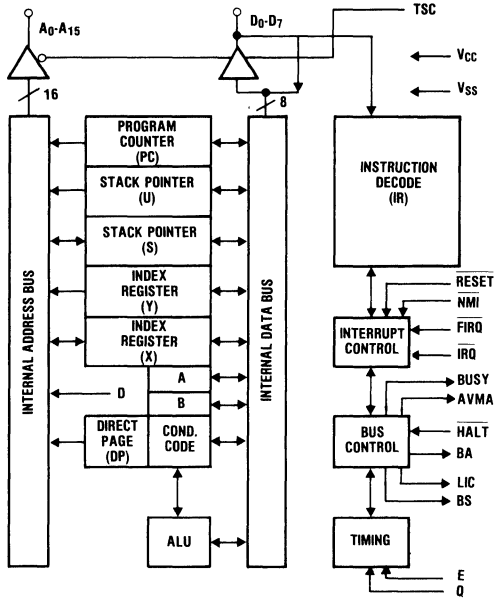
General Description

The S6809E is an advanced processor within the S6800 family offering greater throughput, improved byte efficiency, and increased adaptability to various software disciplines. These include position independence, reentrancy, recursion, block structuring, and high level language generation.

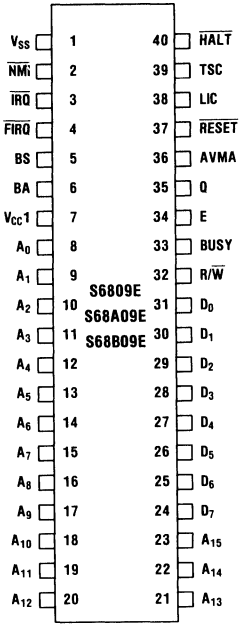
Because the S6809E supports **position-independent** code, software can be written in modular form for easy user expansion as system requirements increase. The S6809E is hardware compatible with all S6800 peripherals, and any assembly language code prepared for the S6800 can be passed through the S6809 assembler to produce code which will run on the S6809E.

S6800 FAMILY

Block Diagram



Pin Configuration



S6809E Hardware Features

- ☐ Fast Interrupt Request Input: Stacks Only Program Counter and Condition Code
- ☐ Interrupt Acknowledge Output Allows Vectoring by Devices
- ☐ Three Vectored Priority Interrupt Levels
- ☐ SYNC Acknowledge Output Allows for Synchronization to External Event
- ☐ NMI Blocked After RESET Until After First Load of Stack Pointer
- ☐ Early Address Valid Allows Use With Slow Memories
- ☐ Last Instruction Cycle Output (LIC) for Signalling Opcode Fetch
- ☐ Busy Output Eases Multiprocessor Design

Instruction Set

- ☐ Extended Range Branches
- ☐ Load Effective Address
- ☐ 16-Bit Arithmetic
- ☐ 8 × 8 Unsigned Multiply (AccumulatorA * B)
- ☐ SYNC Instruction—Provides Software Sync With an External Hardware Process
- ☐ Push and Pull on 2 Stacks
- ☐ Push/Pull Any or All Registers
- ☐ Index Registers May be Used as a Stack Pointer
- ☐ Transfer/Exchange all Registers

Addressing Modes

- ☐ All S6800 Modes Plus PC Relative Extended Indirect, Indexed Indirect, and PC Relative Indirect
- ☐ Direct Addressing Available Anywhere in Memory Map
- ☐ PC Relative Addressing: Byte Relative (± 32,768 Bytes From PC)
- ☐ Complete Indexed Addressing Including Automatic Increment and Decrement, Register Offsets, and Four Indexable Register (X, Y, U and S)
- ☐ Expanded Index Addressing
  - ☐ 0, 5, 8, 16-Bit Constant Offset
  - ☐ 8, 16-Bit Accumulator Offsets

The S6809E gives the user 8- and 16-bit word capability with several hardware enhancements in the design such as the Fast Interrupt Request ($\overline{FIRQ}$), Memory Ready (MRDY), and Quadrature (Q_{OUT}) and System Clock Outputs (E_{OUT}). With the Fast Interrupt Request ($\overline{FIRQ}$) the S6809E places **only** the Program Counter and Condition Code Register on the stack prior to accessing the $\overline{FIRQ}$ vector location. The Memory Ready ($\overline{MRDY}$) input allows extension of the data access time for use with slow memories. The System Clock (E_{OUT}) operates at the basic processor frequency and can be as the synchronization signal for the entire system. The Quadrature Output (Q_{OUT}) provides additional system timing by signifying that address and data are stable.

The External Clock mode of the S6809E is particularly useful when synchronizing the processor to an externally generated signal. The Three-State Control input ($\overline{TSC}$) places the Address and R/W line in the high impedance state for DMA or Memory Refresh. The last Instruction Cycle (LIC) is activated during the last cycle of any instruction. This signifies that the next instruction cycle is the opcode fetch. The Processor Busy signal (BUSY) facilitates multiprocessor applications by allowing the designer to insure that flags being modified by one processor are not accessed by another simultaneously.

The S6809E features a family of addressing capabilities which can use any of the four index registers and stack pointers as a pointer to the operand (or the operand address). This pointer can have a fixed or variable signed offset that can be automatically incremented or decremented. The eight-bit direct page register permits a user to determine which page of memory is accessed by the instructions employing "page zero" addressing. This quick access to any page is especially useful in multitasking applications.

The S6809E has three vectored priority-interrupt levels, each of which automatically disables the lower priority interrupt while leaving the higher priority interrupt enabled.

The S6809E gives the system designer greater flexibility (through modular relocatable code) to enable the user to reduce system software costs while at the same time increasing software reliability and efficiency.

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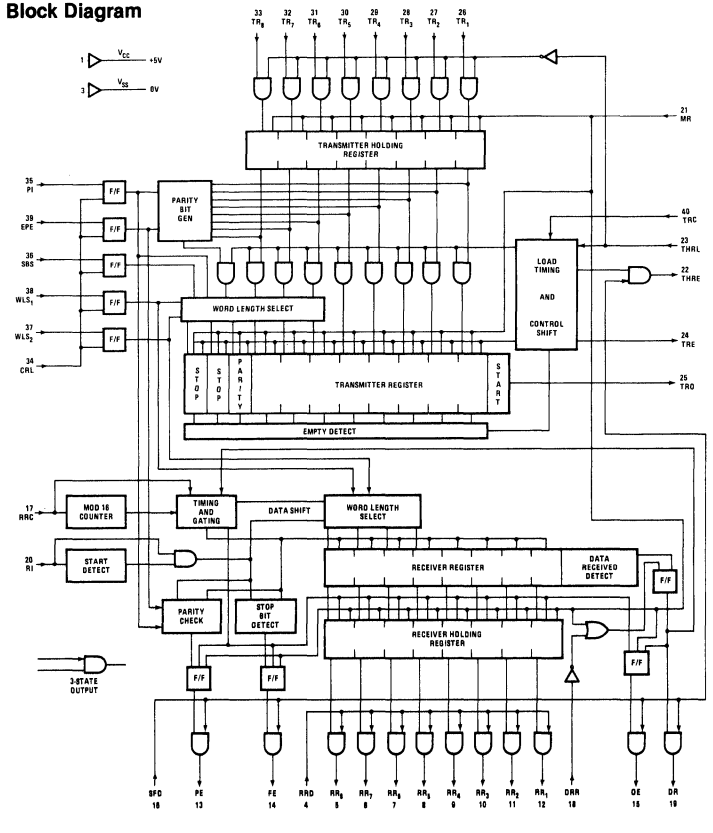
S1602

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

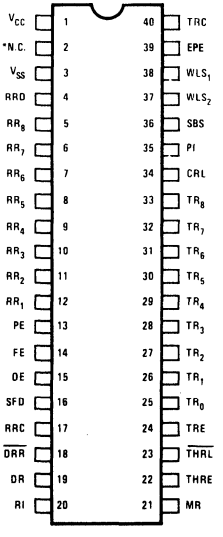
Features

- ☐ Full or Half Duplex Operation Transmits and Receives Serial Data Simultaneously or at Different Baud Rates
- ☐ Completely Programmable—Data Word Length, Number of Stop Bits, Parity
- ☐ Automatic Start Bit Generation
- ☐ Data and Clock Synchronization Performed Automatically
- ☐ Double Buffered—Eliminates Timing Difficulties
- ☐ Completely Static Circuitry
- ☐ Fully TTL Compatible
- ☐ Three-State Output Capability
- ☐ Single Power Supply: + 5 V
- ☐ Standard 40-Pin Dual-in-Line Package
- ☐ Plug In Compatible with Western Digital TR1602A, TR1863, Fujitsu 8868A

Block Diagram



Pin Configuration



S6800 FAMILY

General Description

The AMI S1602 is a programmable Universal Asynchronous Receiver/Transmitter (UART) fabricated with N-Channel silicon gate MOS technology. All control pins, input pins and output pins are TTL compatible, and a single + 5 volt power supply is used. The UART interfaces asynchronous serial data from terminals or other peripherals, to parallel data for a microprocessor, computer, or other terminal. Parallel data is converted by the transmitter section of the UART into a serial word consisting of the data as well as start, parity, and stop bit(s). Serial data is converted by the receiver section of the UART into parallel data. The receiver section verifies correct code transmission by parity checking and receipt of a valid stop bit. The UART can be programmed to accept word lengths of 5, 6, 7, or 8 bits. Even or odd parity can be set. Parity generation checking can be inhibited. The number of stop bits can be programmed for one, two, or one and one half when transmitting a 5-bit code.

Absolute Maximum Ratings*

V_{CC} Pin Potential to V_{SS} Pin	− 0.3V to + 7.0V
Input Voltage	− 0.3V to + 7.0V
Operating Temperature	0°C to + 70°C
Storage Temperature	− 55°C to + 150°C

*Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheets. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance: $T_A = 25°C$; $f = 1MHz$; $V_{IN} = 0V$

Symbol	Parameter	Typ.	Max.	Unit
C_{IN}	Input Capacitance for all Inputs	10		pF

Guaranteed Operating Conditions (Referenced to V_{SS})

Symbol	Parameter	Operating Temperature	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	0°C to + 70°C	4.75	5.0	5.25	V
V_{SS}			0.0	0.0	0.0	V
V_{IH}	Logic Input High Voltage	0°C to + 70°C	2.2		V_{CC}	V
V_{IL}	Logic Input Low Voltage	0°C to + 70°C	− 0.3		+ 0.8	V

D.C. Characteristics (Guaranteed Operating Ranges Unless Otherwise Noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = 5.25V)			1.4	mA
I_{LZ}	Output Leakage Current for 3- State (V_{OUT} = 0V to V_{CC}, SFD = RRD = V_{IH}	− 20		+ 20	μA
V_{OL}	Output Low Voltage (I_{OL} = 1.8mA)			0.4	V
V_{OH}	Output High Voltage (I_{OL} = − 200μA)	2.4			V
I_{CC}	V_{CC} Supply Current		70		mA

A.C. Characteristics (Guaranteed Operating Ranges Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_C	Clock Frequency for RRC and TRC (Duty Cycle = 50%)	DC		800	kHz
t_{PWC}	CRL Pulse Width, High	200			ns
t_{PWT}	THRL Pulse Width, Low	180			ns
t_{PWR}	DRR Pulse Width, Low	180			ns
t_{PWM}	MR Pulse Width, High	150			ns
t_C	Coincidence Time (Figure 3 and Figure 8)	180			ns
t_{HOLD}	Hold Time (Figure 3 and Figure 8)	20			ns
t_{SET}	Setup Time (Figure 3 and Figure 8)	0			ns
t_{PD0}	Propagation Delay Time High to Low, Output (C_L = 130pF +1TTL)			350	ns
t_{PD1}	Propagation Delay Time Low to High, Output (C_L = 130pF +1TTL)			350	ns

Pin Description

Pin	Label	Function
1	V_{CC}	**Power Supply**—normally at +5V.
2	N.C.	**No Connection**. On the S1602 this is an unconnected pin. On the TR1602A this is a −12V supply. −12V is not needed on the S1602 and thus the N.C. pin allows the S1602 to be compatible with the TR1602A.
3	V_{SS}	This is normally at 0V or ground.
4	RRD	**Receive Register Disconnect**. A high logic level, V_{IH}, on this pin disconnects the Receiver Holding Register outputs from the data outputs RR_8–RR_1 on pin 5–12.
5–12	RR_8–RR_1	**Receiver Holding Register Data**. These are the parallel outputs from the Receiver Holding Register, if the RRD input is low (V_{IL}). Data is (LSB) right justified for character formats of less than eight bits, with RR_1 being the least significant bit. Unused MSBs are forced to a low logic output level, V_{OL}.
13	PE	**Parity Error**. This output pin goes to a high level if the received parity does not agree with that programmed by the Even Parity Enable input (pin 39). This output is updated as each character is transferred to the Receiver Holding Register. The Status Flag Disconnect input (pin 16) allows additional PE lines to be tied together by providing an output disconnect capability.
14	FE	**Framing Error**. This output pin goes high if the received character has no valid stop bit. Each time a character is transferred to the Receiver Holding Register, this output is updated. The Status Flag Disconnect input (pin 16) allows additional FE lines to be tied together by providing an output disconnect capability.
15	OE	**Overrun Error**. This output pin goes high if the Data Received Flag (pin 19) did not get reset before the next character was transferred to the Receive Holding Register. The Status Flag Disconnect input (pin 16) allows additional OE lines to be tied together providing an output disconnect capability.
16	SFD	**Status Flag Disconnect**. When this input is high, PE, FE, OE, DR and THRE outputs are forced to high impedance Three-State allowing bus sharing capability.
17	RRC	**Receive Register Clock**. This clock input is 16x the desired receiver shift rate.
18	$\overline{DRR}$	**Data Received Reset**. A low level input, V_{IL}, clears the Data Received (DR) line.
19	DR	**Data Received**. When a complete character has been received and transferred to the Receiver Holding Register, this output goes to the high level, V_{OH}.
20	RI	**Receiver Input**. Serial input data enters on this line. It is transferred to the Receiver Register as determined by the character length, parity and number of stop bits. When data is not being received, this input must remain high, V_{IH}.

Pin Description

Pin	Label	Function
21	MR	**Master Reset**. A high level pulse, V_{IH}, on this input clears the internal logic. The transmitter and Receive Registers, Receiver Holding Register, FE, OE, PE, DRR are reset. In addition, the serial output line is set to a high level, V_{OH}.
22	THRE	**Transmitter Holding Register Empty**. This output will go high when the Transmitter Holding Register completes transfer of its contents to the Transmitter Register. The high level indicates a new character may be loaded into the Transmitter Holding Register.
23	$\overline{\text{THRL}}$	**Transmitter Holding Register Load**. When a low level, V_{IL}, is applied to this input, a character is loaded into the Transmitter Holding Register. The character is transferred to the Transmitter Register on a low to high level, V_{IH}, transition as long as the Transmitter Register is not currently in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until the transmission is completed. The new character is then transferred simultaneously with the start of the serial transmission of the new character.
24	TRE	**Transmitter Register Empty**. Goes high when the Transmitter Register has completed the serial transmission of a full character including the required number of stop bits. A high will be maintained until the start of transmission of the next character.
25	TRO	**Transmitter Register Output**. Transmits the Transmitter Register contents (Start bit, Data bits, Parity bit and Stop bit(s) serially. Remains high, V_{OH}, when no data is being transmitted. Therefore, start of transmission is determined by transition of the Start bit from high to low level voltage, V_{OL}.
26–33	TR_1–TR_8	**Transmitter Register Data Inputs**. The THRL strobe loads the character on these lines into the Transmitter Holding Register. If WLS_1 and WLS_2 have selected a character of less than 8 bits, the character is right justified to the least significant bit, TR_1 with the excess bits not used. A high input level, V_{IH}, will cause a high output level, V_{OH}, to be transmitted.
34	CRL	**Control Register Load**. The control bits, (WLS_1, WLS_2, EPE, PI, SBS), are loaded into the Control Register when the input is high. This input may be either strobed or hard wired to the high level.
35	PI	**Parity Inhibit**. Parity generation and verification circuitry are inhibited when this input is high. The PE output will be held low as well. When in the inhibit condition the Stop bit(s) will follow the last data bit on transmission.
36	SBS	**Stop Bit(s) Select**. A high level will select two Stop bits, and a low level selects one Stop bit. If 5—bit words are selected, a high level will generate one and one-half Stop bits.
37, 38	WLS_2, WLS_1	**Word Length Select**. The state of these two (2) inputs determines the character length (exclusive of parity) as follows:

WLS_2	WLS_1	WORD LENGTH
LOW	LOW	5 bits
LOW	HIGH	6 bits
HIGH	LOW	7 bits
HIGH	HIGH	8 bits

39	EPE	**Even Parity Enable**. A high voltage level, V_{IH}, on this input will select even parity, while a low voltage level, V_{IL}, selects odd parity.
40	TRC	**Transmitter Register Clock**. The frequency of this clock input should be 16 times the desired baud rate.

Figure 1. Receiver Operator Timing

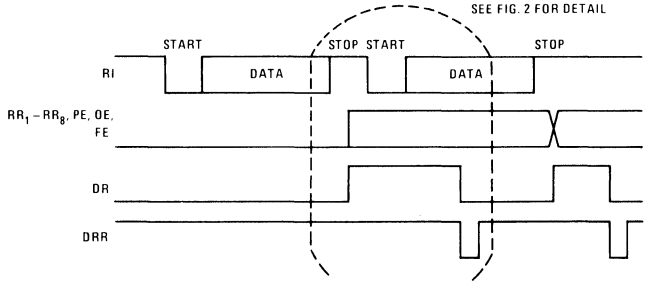


Figure 2. Timing for Status Flags, RR_1 thru RR_8 and DR

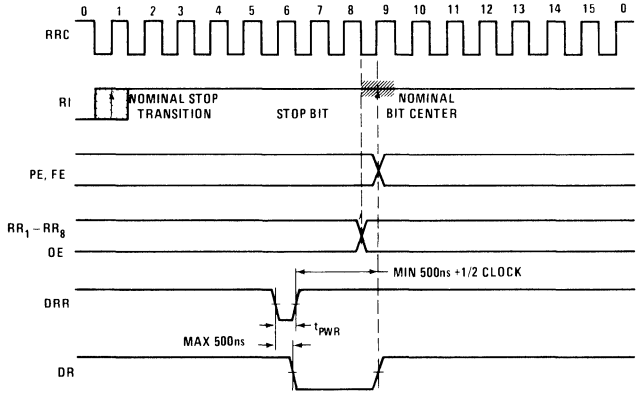


Figure 3. Transmitter Operator Timing

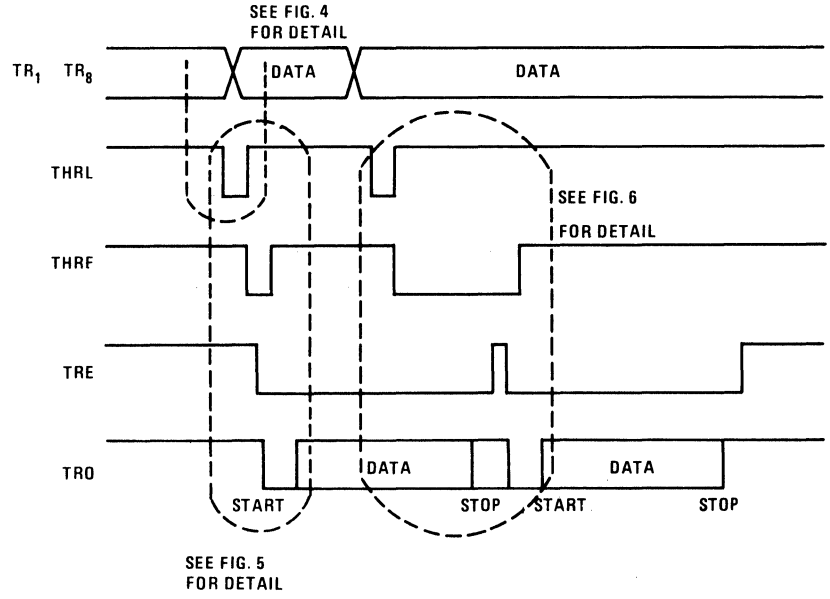


Figure 4. Data Input Load Cycle

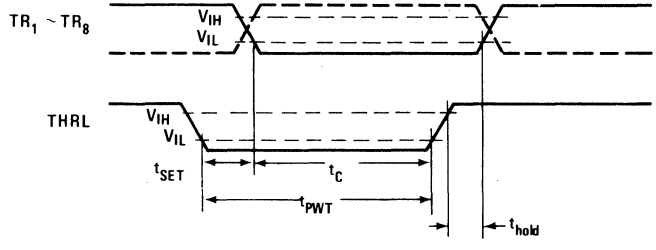
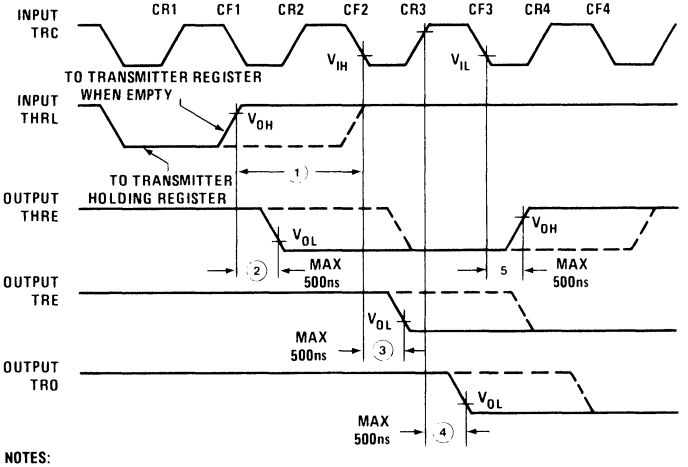


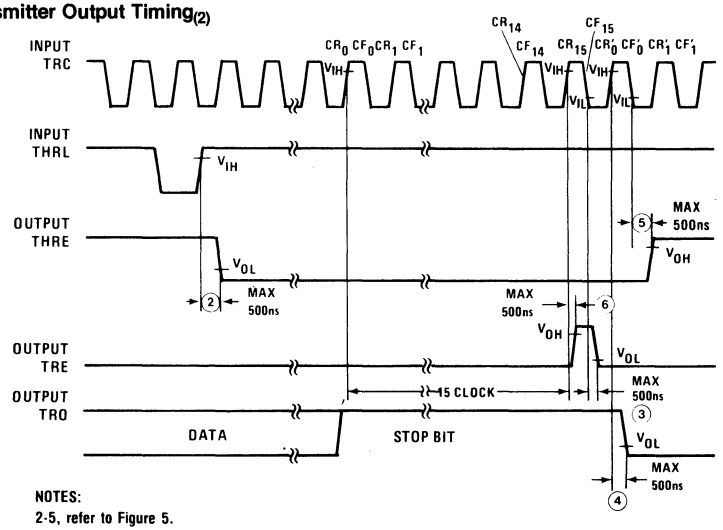
Figure 5. Transmitter Output Timing(1)



NOTES:

1. When the positive transition of THRL is 500ns or more before the falling edge of TRC (CF2 in the figure), TRE is enabled at CF2. But, when 500ns>①>0ns, TRE is invalid between CF2 and CF3.
2. THRE goes to low during 500ns Max. from the positive transition of THRL.
3. TRE goes to low during 500ns Max. from the first falling edge of TRC after THRE goes to low with TRE high.
4. TRO goes to low (START BIT) during 500ns Max. from the first rising edge of TRC after TRE goes to low.
5. THRE goes to high during 500ns Max. from the falling edge of TRC after START BIT is enabled.

Figure 6. Transmitter Output Timing(2)



NOTES:

2-5, refer to Figure 5.

6. TRANSMITTER REGISTER EMPTY goes to high during 500ns Max. from the 15th rising edge of TRC after STOP BIT is enables.

Figure 7. Input After Master Reset

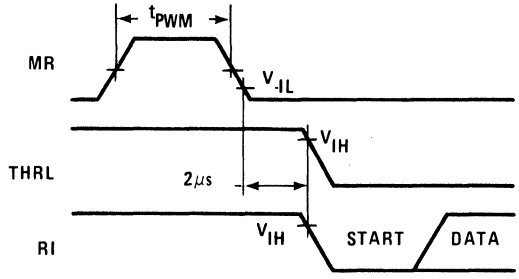


Figure 8. Control Register Load Cycle

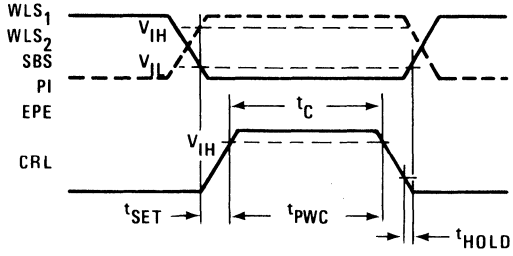


Figure 9. Status Flag Output

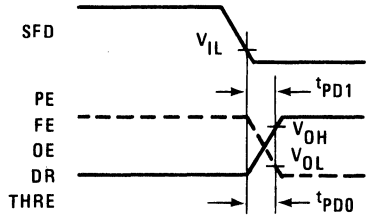
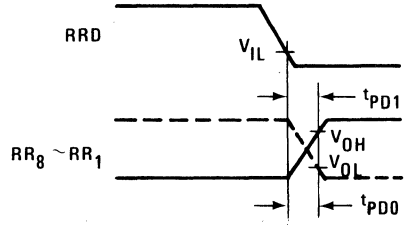


Figure 10. Data Output



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S2350

UNIVERSAL SYNCHRONOUS RECEIVER/TRANSMITTER

Features

- ☐ 500kHz Data Rates
- ☐ Internal Sync Detection
- ☐ Fill Character Register
- ☐ Double Buffered Input/Output
- ☐ Bus Oriented Outputs
- ☐ 5-8 Bit Characters
- ☐ Odd/Even or No Parity
- ☐ Error Status Flags
- ☐ Single Power Supply (+ 5V)
- ☐ Input/Output TTL-Compatible

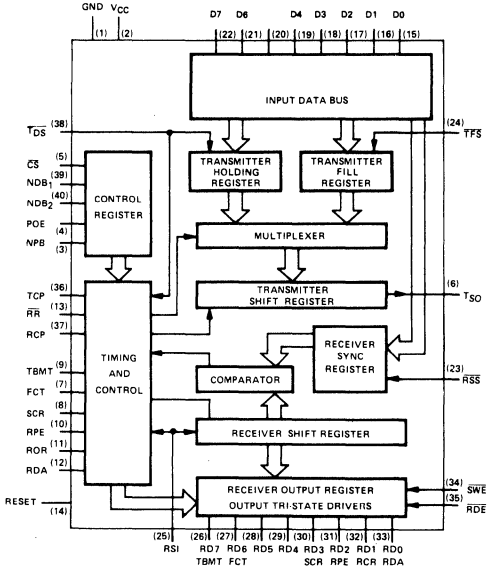
General Description

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial-to-parallel and parallel-to-serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

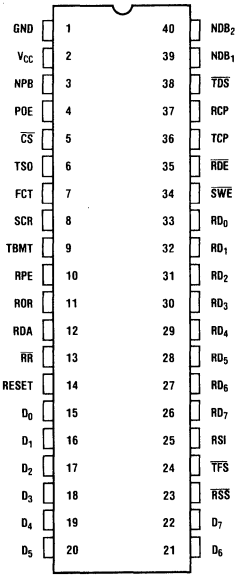
The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

S6800 FAMILY

Block Diagram



Pin Configuration



Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8-bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8-bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

Typical Applications

- ☐ Computer Peripherals
- ☐ Communication Concentrators
- ☐ Integrated Modems
- ☐ High Speed Terminals
- ☐ Time Division Multiplexing
- ☐ Industrial Data Transmission

Absolute Maximum Ratings

Ambient Temperature Under Bias	0°C to + 70°C
Storage Temperature	− 65°C to + 150°C
Positive Voltage on Any Pin With Respect to GROUND	+ 7V
Negative Voltage on Any Pin With Respect to GROUND	− 0.5V
Power Dissipation	0.75W

D.C. (Static) Electrical Characteristics* (V_{CC} = 5.0V ± 5%; T_A = 0°C to + 70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	− 0.5		+ 0.8	V	
I_{IL}	Input Leakage Current			10	μA	V_{IN} = 0_{TO} V_{CC} V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = − 100μA
V_{OL}	Output Low Voltage			+ 0.4	V	I_{OL} = 1.6mA
C_{IN}	Input Capacitance			10	pF	V_{IN} = 0V; f = 1.0MHz
C_{OUT}	Output Capacitance			12	pF	V_{IN} = 0V; f = 1.0MHz
I_{CC}	V_{CC} Supply Current			100	mA	No Load; V_{CC} = 5.25V

* Electrical Characteristics included in this advanced product description are objective specifications and may be subject to change.

A.C. (Dynamic) Electrical Characteristics* (V_{CC} = 5.0V ± 5%; T_A = 0°C to + 70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC		500	kHz	

A.C. (Dynamic) Electrical Charcteristics* (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
Input Pulse Width						
P_{TCP}	Transmit Clock	900			nsec	CL = 20pF
P_{RCP}	Receive Clock	900			nsec	1TTL Load
P_{RST}	Reset	500			nsec	
P_{TDS}	Transmit Data Strobe	200			nsec	
P_{TFS}	Transmit Fill Strobe	200			nsec	
P_{RSS}	Receive Sync Strobe	200			nsec	
P_{CS}	Control Strobe	200			nsec	
P_{RDE}	Receive Data Enable	400			nsec	Note 1
P_{SWE}	Status Word Enable	400			nsec	Note 1
P_{RR}	Receiver Restart	500			nsec	
Switching Characteristics						
T_{TSO}	Delay, TCP Clock to Serial Data Out			700	nsec	
T_{TBMT}	Delay, TCP Clock to TBMT Output			1.4	μsec	
T_{TBMT}	Delay, TDS to TBMT			700	nsec	
T_{STS}	Delay, SWE to Status Reset			700	nsec	
T_{RDO}	Delay, SWE, RDE to Data Output			400	nsec	1TTL Load
T_{HRDO}	Hold Time SWE, RDE to Off State			400	nsec	C_L = 130pF
T_{DTS}	Data Set Up Time TDS, TFS, RSS, CS	0			nsec	
T_{DTH}	Data Hold Time TDS	700			nsec	
T_{DTI}	Data Hold time TFS, RSS	200			nsec	
T_{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0			nsec	
T_{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200			nsec	
T_{RDA}	Delay RDE to RDA Output	700			nsec	

NOTE 1: Required to reset status and flags.

AMI®

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S6551/S6551A

ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

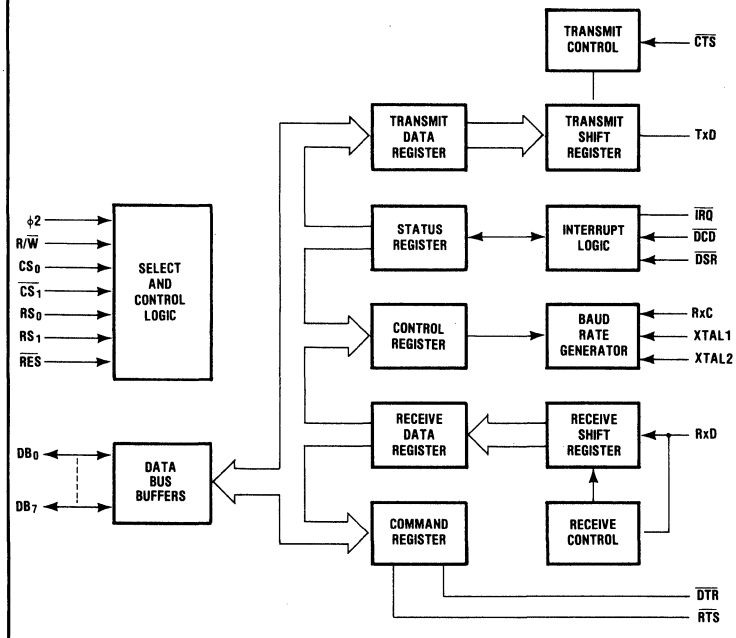
Features

- ☐ On-Chip Baud Rate Generator: 15 Programmable Baud Rates Derived from a Standard 1.8432MHz External Crystal (50 to 19,200 Baud)
- ☐ Programmable Interrupt and Status Register to Simplify Software Design
- ☐ Single + 5 Volt Power Supply
- ☐ Serial Echo Mode
- ☐ False Start Bit Detection
- ☐ 8-Bit Bi-Directional Data Bus for Direct Communication With the Microprocessor
- ☐ External 16X Clock Input for Non-Standard Baud Rates (Up to 125K Baud)
- ☐ Programmable: Word Lengths; Number of Stop Bits; and Parity Bit Generation and Detection
- ☐ Data Set and Modem Control Signals Provided
- ☐ Parity: (Odd, Even, None, Mark, Space)
- ☐ Full-Duplex or Half-Duplex Operation
- ☐ 5, 6, 7, 8 and 9-Bit Transmission

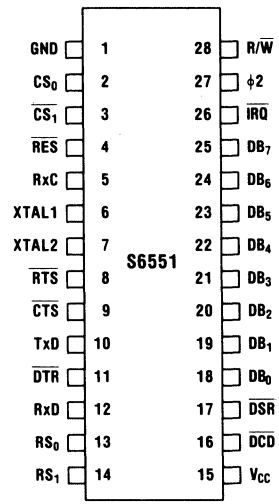
General Description

The S6551/S6551A is an Asynchronous Communication Adapter (ACIA) intended to provide interfacing for the microprocessors to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3V to +7.0V
Input/Output Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Operating Characteristics (V_{CC} = 5.0V ± 5, T_A = 0C to +70°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0	—	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
I_{IN}	Input Leakage Current: V_{IN} = 0 to 5V (ϕ2, R/$\overline{W}$, $\overline{RES}$, CS_0, $\overline{CS_1}$, RS_0, RS_1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	—	±1.0	±2.5	μA
I_{TSI}	Input Leakage Current for High Impedance State (Three State)	—	±2.0	±10.0	μA
V_{OH}	Output High Voltage: I_{LOAD} = −100μA (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	2.4	—	—	V
V_{OL}	Output Low Voltage: I_{LOAD} = 1.6mA (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	—	—	0.4	V
I_{OH}	Output High Current (Sourcing): V_{OH} = 2.4V (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	−100	—	—	μA
I_{OL}	Output Low Current (Sinking): V_{OL} = 2.4V (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	1.6	—	—	mA
I_{OFF}	Output Leakage Current (Off State): V_{OUT} = 5V ($\overline{IRQ}$)	—	1.0	10.0	μA
C_{CLK}	Clock Capacitance (ϕ2)	—	—	20	pF
C_{IN}	Input Capacitance (Except XTAL1 and XTAL2)	—	—	10	pF
C_{OUT}	Output Capacitance	—	—	10	pF
P_D	Power Dissipation (See Graph) (T_A = 0°C)	—	170	300	mW

Write Cycle (V_{CC} = 5.0V ± 5, T_A = 0C to +70°C, unless otherwise noted)

		S6551		S6551A		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	ϕ2 Pulse Width	400	—	200	—	ns
t_{ACW}	Address Set-Up Time	120	—	70	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	150	—	60	—	ns
t_{HW}	Data Bus Hold Time	20	—	20	—	ns

(t_r and t_f = 10 to 30ns)

Figure 1. Power Dissipation vs. Temperature

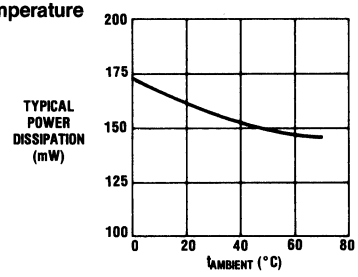
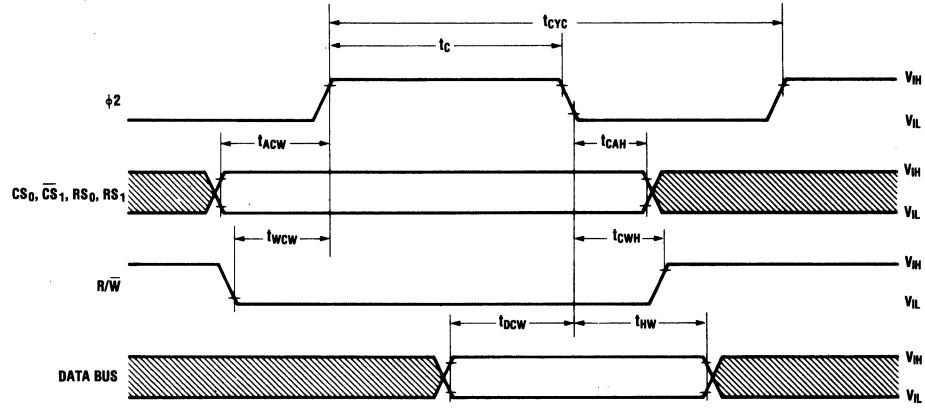


Figure 2. Write Timing Characteristics



Read Cycle (V_{CC} = 5.0V ± 5, T_A = 0C to + 70°C, unless otherwise noted)

Symbol	Parameter	S6551		S6551A		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	$\phi 2$ Pulse Width	400	—	200	—	ns
t_{ACR}	Address Set-Up Time	120	—	70	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	$R/\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	200	—	150	ns
t_{HR}	Read Hold Time	20	—	20	—	ns
t_{CDA}	Bus Active Time (Invalid Data)	40	—	40	—	ns

Figure 3. Clock Generation

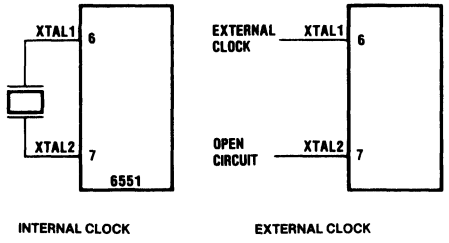
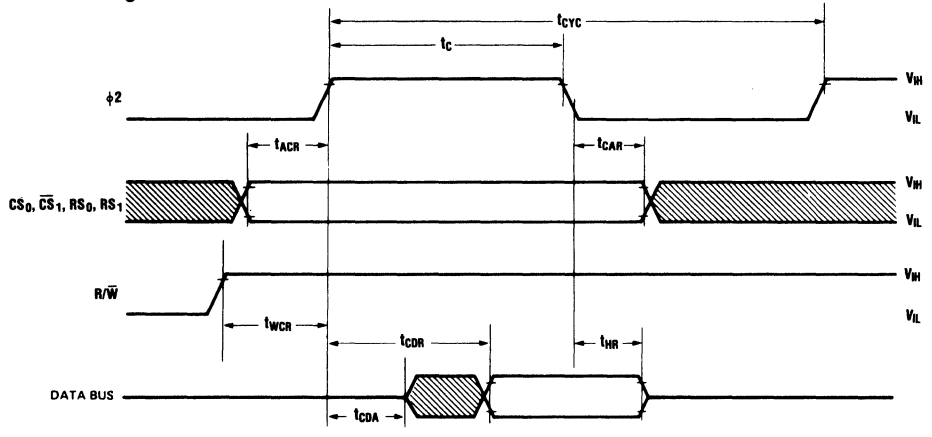


Figure 4. Read Timing Characteristics



Transmit/Receive Characteristics

Symbol	Parameter	S6551 Min.	S6551 Max.	S6551A Min.	S6551A Max.	Unit
t_{CCY}	Transmit/Receive Clock Rate	400*	—	400*	—	ns
t_{CH}	Transmit/Receive Clock High Time	175	—	175	—	ns
t_{CL}	Transmit/Receive Low Time	175	—	175	—	ns
t_{DD}	EXTAL1 to TxD Propagation Delay	—	500	—	500	ns
t_{DLY}	Propagation Delay ($\overline{RTS}$, DTR)	—	500	—	500	ns
t_{IRQ}	$\overline{IRQ}$ Propagation Delay (Clear)	—	500	—	550	ns

(t_r and t_f = 10 to 30ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

Figure 5. Test Load for Data Bus (DB_0-DB_7), $\overline{TxD}$, $\overline{DTR}$, RTS Outputs

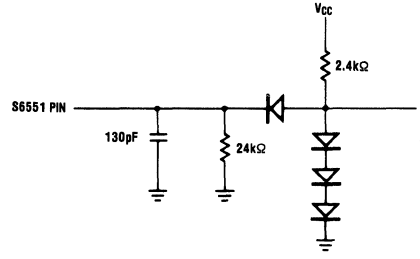


Figure 6a. Interrupt and Output Timing

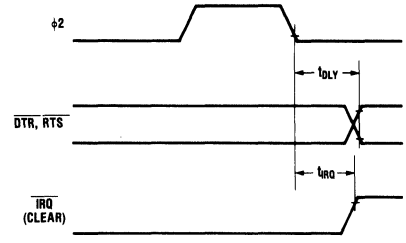


Figure 6b. Transmit Timing with External Clock

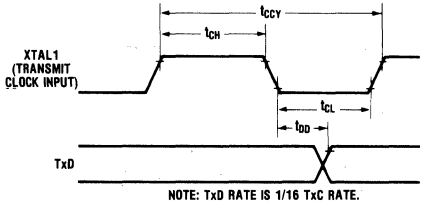
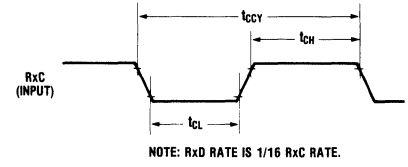


Figure 6c. Receive External Clock Timing



Pin Description

$\overline{RES}$ (Reset). During system initialization a low on the RES input will cause internal registers to be cleared.

ϕ2 Input Clock. The input clock is the system ϕ2 clock and is used to trigger all data transfers between the system microprocessor and the S6551.

R/$\overline{W}$ (Read/Write). The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the S6551. A low on the R/$\overline{W}$ pin allows a write to the S6551.

$\overline{IRQ}$ (Interrupt Request). The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0-DB_7 (Data Bus). The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the S6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0-$\overline{CS_1}$ (Chip Selects). The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The S6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_0, RS_1 (Register Selects). The two register select lines are normally connected to the processor address lines to allow the processor to select the various S6551 internal registers. The following table indicates the internal register select coding:

Table 1

RS_1	RS_0	WRITE	READ
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the S6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these diferences are described in the individual register definitions.

XTAL1, XTAL2 (Crystal Pins). These pins are normally directly connected to the external crystal (1.8432MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float. The choice of crystal is not critical, but NYMPH PO18 (series resonant) is recommended.

TxD (Transmit Data). The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data). The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock). The RxC is a bi-directional pin which serves as either the receiver 16xclock input or the receiver 16xclock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{\text{RTS}}$ (Request to Send). The $\overline{\text{RTS}}$ output pin is used to control the modem from the processor. The state of the $\overline{\text{RTS}}$ pin is determined by the contents of the Command Register.

$\overline{\text{CTS}}$ (Clear to Send). The $\overline{\text{CTS}}$ input pin is used to control the transmitter operation. The enable state is with $\overline{\text{CTS}}$ low. The transmitter is automatically disabled if $\overline{\text{CTS}}$ is high.

$\overline{\text{DTR}}$ (Data Terminal Ready). This output pin is used to indicate the status of the S6551 to the modem. A low on $\overline{\text{DTR}}$ indicates the S6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{\text{DSR}}$ (Data Set Ready). The $\overline{\text{DSR}}$ input pin is used to indicate to the S6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{\text{DSR}}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

$\overline{\text{DCD}}$ (Data Carrier Detect). The $\overline{\text{DCD}}$ input pin is used to indicate to the S6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{\text{DCD}}$, like $\overline{\text{DSR}}$, is a high-impedance input and must not be a no-connect.

Internal Organization

The Transmitter/Receiver sections of the S6551 are depicted by the block diagram in Figure 7.

Figure 7. Transmitter/Receiver Clock Circuits

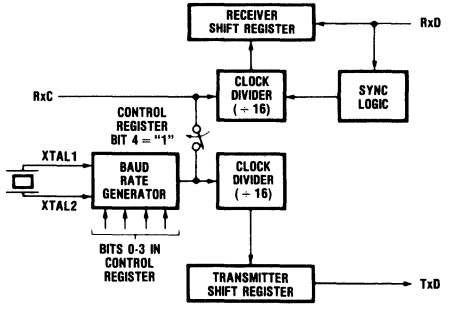


Figure 8. Control Register Format

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 STOP BIT
1 = 2 STOP BITS
1 STOP BIT IF WORD LENGTH = 5 BITS AND NO PARITY
1½ STOP BITS IF WORD LENGTH = 5 BITS AND NO PARITY

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = EXTERNAL RECEIVER CLOCK
1 = BAUD RATE GENERATOR

BAUD RATE GENERATOR

0	0	0	0	16x EXTERNAL CLOCK
0	0	0	1	50 BAUD
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	0	0	0	0	0

*THIS ALLOWS FOR 9-BIT TRANSMISSION (8 DATA BITS PLUS PARITY).

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the S6551.

Control Register

The Control Register is used to select the desired mode for the S6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 8.

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 9.

Figure 9. Command Register Format

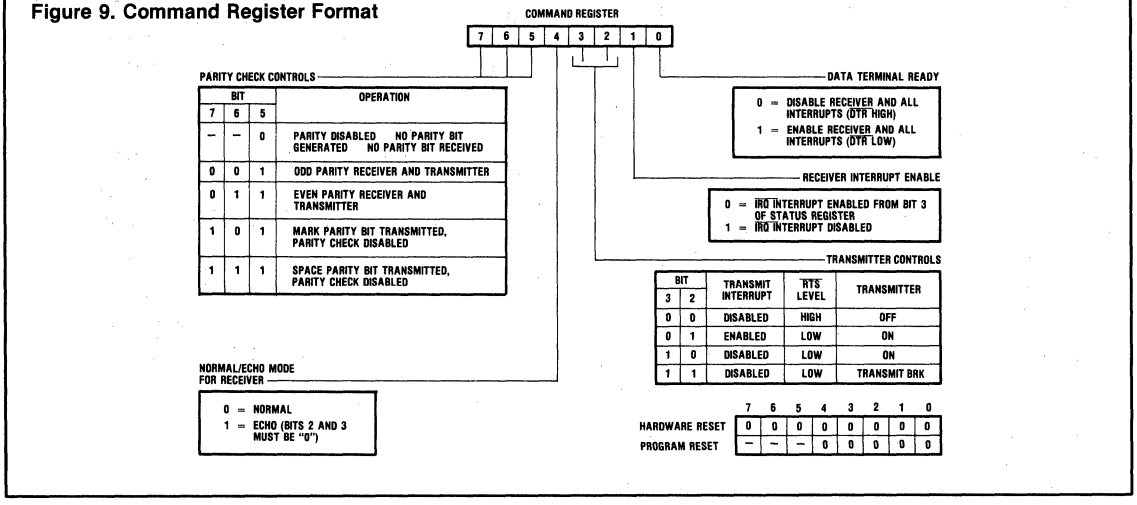
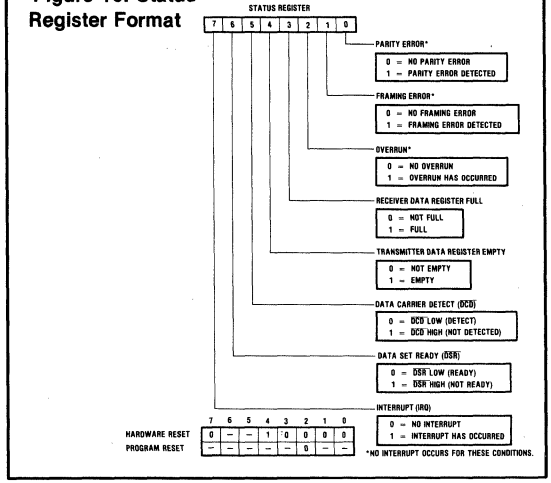


Figure 10. Status Register Format



Status Register

The Status Register is used to indicate to the processor the status of various S6551 functions and is outlined in Figure 10.

Transmit and Receive Data Registers

These registers are used as temporary data storage for the S6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

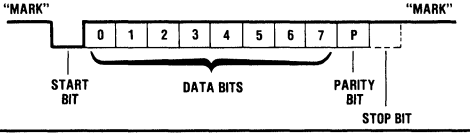
- ☐ Bit 0 is the leading bit to be transmitted.
- ☐ Unused data bits ae the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- ☐ Bit 0 is the leading bit received.
- ☐ Unused data bits are the high-order bits and are "0" for the receiver.
- ☐ Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 11 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

Figure 11. Serial Data Stream Example



AMI

A Subsidiary of Gould Inc.

S6821/S68A21/S68B21

PERIPHERAL INTERFACE ADAPTER (PIA)

Features

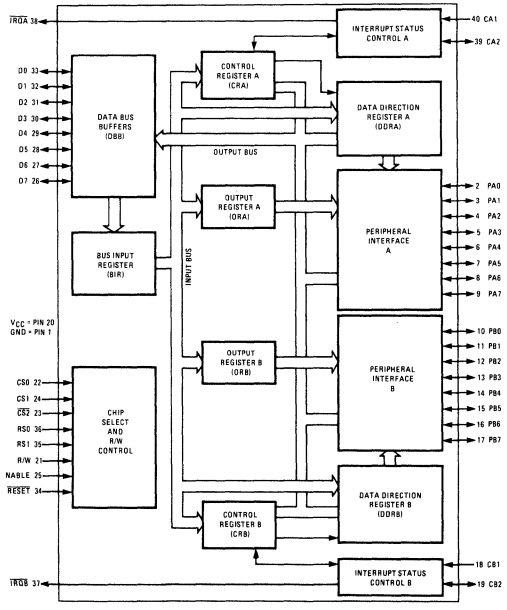
- ☐ 8-Bit Bidirectional Bus for Communication with the MPU
- ☐ Two Bidirectional 8-Bit Buses for Interface to Peripherals
- ☐ Two Programmable Control Registers
- ☐ Two Programmable Data Direction Registers
- ☐ Four Individually-Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs
- ☐ Handshake Control Logic for Input and Output Peripheral Operation
- ☐ High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- ☐ Program Controlled Interrupt and Interrupt Disable Capability
- ☐ CMOS Compatible Peripheral Lines
- ☐ Two TTL Drive Capability on all A and B Side Buffers
- ☐ TTL Compatible
- ☐ Static Operation

General Description

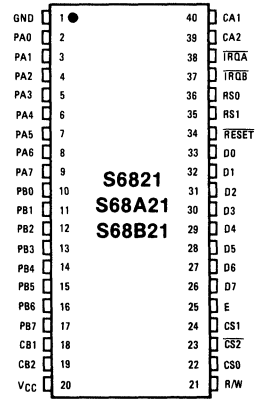
The S6821/S68A21/S68B21 are peripheral Interface Adapters that provide the universal means of interfacing peripheral equipment to the S6800/S68A00/S68B00 Microprocessing Units (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization Each of the

Block Diagram



Pin Configuration



General Description (Continued)

peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The PIA interfaces to the S6800/S68A00/S68B00 MPUs with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with S6800/S68A00/S68B00 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

Absolute Maximum Ratings:

Symbol	Rating	Value	Unit
V_{CC}	Supply Voltage	−0.3 to +7.0	Vdc
V_{IN}	Input Voltage	−0.3 to +7.0	Vdc
T_A	Operating Temperature Range	0° to +70°	°C
T_{stg}	Storage Temperature Range	−55° to +150°	°C
θ_{ja}	Thermal Resistance	82.5	°C/W

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

S6800 FAMILY

Electrical Characteristics

V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Conditions
Bus Control Inputs (R/$\overline{W}$, Enable, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$)						
V_{IH}	Input High Voltage	V_{SS} + 2.0	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc	
I_{IN}	Input Leakage Current	—	1.0	2.5	μAdc	V_{IN} = 0 to 5.25 Vdc
C_{IN}	Capacitance	—	—	7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
Interrupt Outputs ($\overline{IRQA}$, $\overline{IRQB}$)						
V_{OL}	Output Low Voltage	—	—	V_{SS} + 0.4	Vdc	I_{LOAD} = 3.2 mAdc
I_{LOH}	Output Leakage Current (Off State)	—	1.0	10	μAdc	V_{OH} = 2.4 Vdc
C_{OUT}	Capacitance	—	—	5.0	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
Data Bus (D0-D7)						
V_{IH}	Input High Voltage	V_{SS} + 2.0	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc	
I_{TSI}	Three State (Off State) Input Current	—	2.0	10	μAdc	V_{IN} = 0.4 to 2.4 Vdc
V_{OH}	Output High Voltage	V_{SS} + 2.4	—	—	Vdc	I_{LOAD} = − 205μAdc
V_{OL}	Output Low Voltage	—	—	V_{SS} + 0.4	Vdc	I_{LOAD} = 1.6mAdc
C_{IN}	Capacitance	—	—	12.5	pF	V_{IN} = 0, T_A = 25°C f = 1.0MHz

Electrical Characteristics (Continued)

Symbol	Characteristic		Min.	Typ.	Max.	Unit	Conditions
Peripheral Bus (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)							
I_{IN}	Input Leakage Current	R/$\overline{W}$, $\overline{Reset}$, RS0, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable		1.0	2.5	μAdc	V_{IN} = 0 to 5.25 Vdc
I_{TSI}	Three-State (Off State) Input Current	PB0-PB7, CB2		2.0	10	μAdc	V_{IN} = 0.4 to 2.4 Vdc
I_{IH}	Input High Current	PA0-PA7, CA2	−200	−400		μAdc	V_{IH} = 2.4 Vdc
I_{OH}	Darlington Drive Current	PB0-PB7, CB2	−1.0		−10	mAdc	V_O = 1.5 Vdc
I_{IL}	Input Low Current	PA0-PA7, CA2		−1.3	−2.4	mAdc	V_{IL} = 0.4Vdc
V_{OH}	Output High Voltage	PA0-P7, PB0-PB7, CA2, CB2 PA0-PA7, CA2	V_{SS} + 2.4 V_{CC} − 1.0			Vdc	I_{LOAD} = −200μAdc I_{LOAD} = −10μAdc
V_{OL}	Output Low Voltage				V_{SS} + 0.4	Vdc	I_{LOAD} = 3.2mAdc
C_{IN}	Capacitance				10	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
Power Requirements							
P_D	Power Dissipation				550	mW	

A.C. (Dynamic) Characteristics Loading = 30pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2 = 130pF and one TTL load for D0-D7, $\overline{IRQA}$, $\overline{IRQB}$ (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise specified)

Peripheral Timing Characteristics: V_{CC} − 5.0V ± 5%, V_{SS} = 0V, T_A = 0°C to +70°C unless otherwise specified

Symbol	Parameter	S6821		S68A21		S68B21		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PDSU}	Peripheral Data Setup Time	200		135		100		ns
t_{PDH}	Peripheral Data Hold Time	0		0		0		ns
t_{CA2}	Delay Time, Enable Negative Transition to CA2 Negative Transition		1.0		0.670		0.5	μs
t_{RS1}	Delay Time, Enable Negative Transition to CA2 Positive Transition		1.0		0.670		0.50	μs
t_r, t_f	Rise and Fall Times for CA1 and CA2 Input Signals	1.0		1.0		1.0	μs	
t_{RS2}	Delay Time from CA1 Active Transition to CA2 Positive Transition		2.0		1.35		1.0	μs
t_{PDW}	Delay Time, Enable Negative Transition to Peripheral Data Valid		1.0		0.670		0.5	μs
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid PA0-PA7, CA2		2.0		1.35		1.0	μs

Peripheral Timing Characteristics (Continued)

Symbol	Parameter	S6821 Min.	S6821 Max.	S68A21 Min.	S68A21 Max.	S68B21 Min.	S68B21 Max.	Units
t_{CB2}	Delay Time, Enable Positive Transition to CB2 Negative Transition		1.0		0.670		0.5	μs
t_{DC}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	2.0		20		20		ns
t_{RS1}	Delay Time, Enable Positive Transition to CB2 Positive Transition		1.0		0.670		0.5	μs
PW_{CT}	Peripheral Control Output Pulse Width, CA2/CB2	550		550		550		ns
t_r, t_f	Rise and Fall Times for CB1 and CB2 Input Signals		1.0		1.0		1.0	μs
t_{RS2}	Delay Time, CB1 Active Transition to CB2 Positive Transition		2.0		1.35		1.0	μs
t_{IR}	Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$		1.60		1.1		0.85	μs
t_{RS3}	Interrupt Response Time		1.0		1.0		1.0	μs
PW_I	Interrupt Input Pulse Width	500		500		500		ns
t_{RL}	Reset Low Time*	1.0		0.66		0.5		μs

*The Reset line must be high a minimum of 1.0μs before addressing the PIA.

S6800 FAMILY

Figure 1. Enable Signal Characteristics

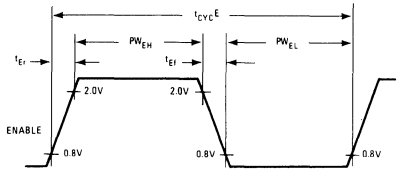


Figure 2. Bus Read Timing Characteristics (Read Information from PIA)

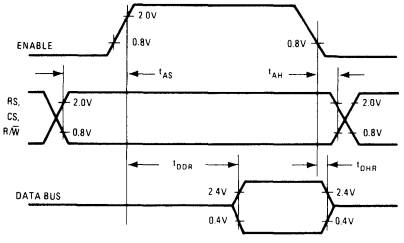


Figure 3. Bus Write Timing Characteristics (Write Information into PIA)

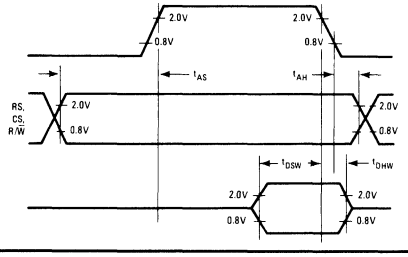
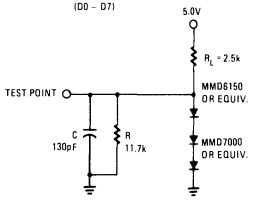


Figure 4. Bus Timing Test Loads



Bus Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Symbol	Parameter	S6821		S68A21		S68B21		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{cyc(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er}, t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DDR}	Data Delay Time, Read		320		220		180	ns
t_{DHR}	Data Hold Time, Read	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Figure 5. TTL Equiv. Test Load

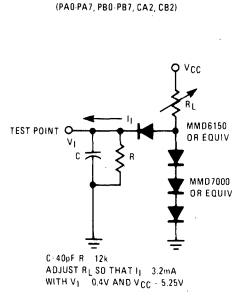


Figure 6. CMOS Equiv. Test Load

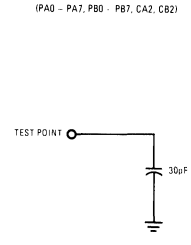


Figure 7. NMOS Equiv. Test Load

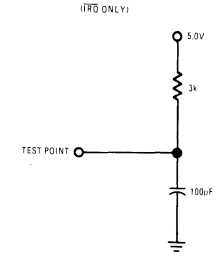


Figure 8. Peripheral Data Setup and Hold Times (Read Mode)

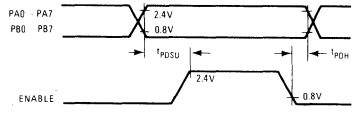
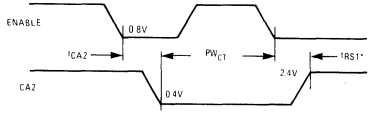


Figure 9. CA2 Delay Time (Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

Figure 10. CA2 Delay Time
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

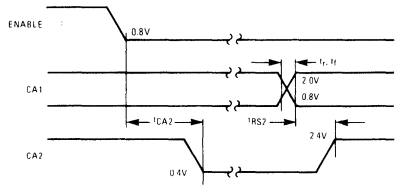


Figure 11. Peripheral CMOS Delay Times
(Write Mode; CRA-5 = CRA-3 = CRA-4 = 0)

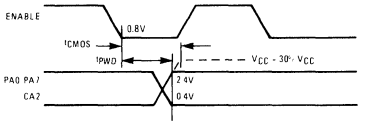
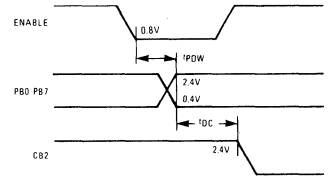


Figure 12. Peripheral Data and CB2 Delay Times
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



CB2 Note:
CB2 goes low as a result of the positive transition of Enable.

Figure 13. CB2 Delay Time
(Read Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)

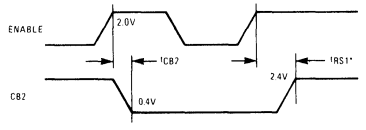
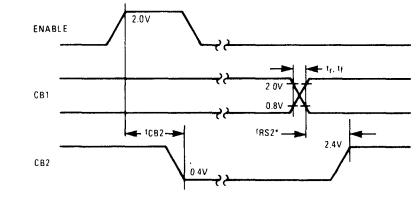
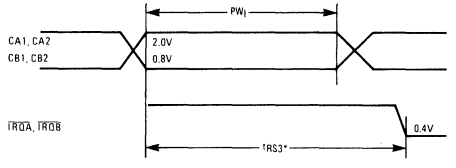


Figure 14. Delay Time
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

Figure 15. Interrupt Pulse Width and $\overline{IRQ}$ Response



*Assumes Interrupt Enable Bits are set.

Figure 16. $\overline{IRQ}$ Release Time

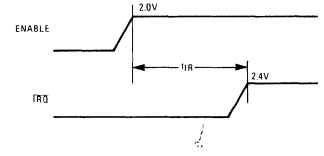
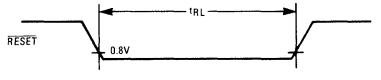


Figure 17. $\overline{Reset}$ Low Time



*The $\overline{Reset}$ line must be a V_{IH} for a minimum of 1.0μs before addressing the PIA.

A Subsidiary of Gould Inc.

S6840/S68A40/S68B40

PROGRAMMABLE TIMER

Features

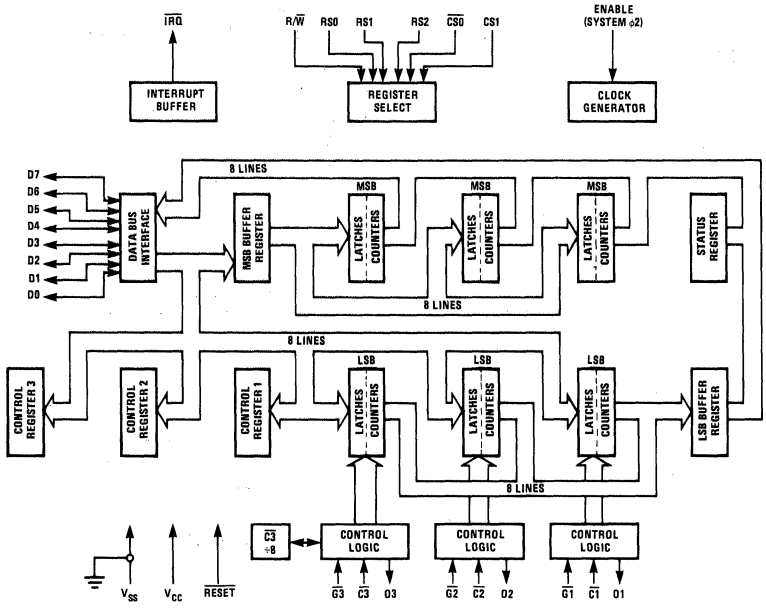
- ☐ Operates from a Single 5 Volt Supply
- ☐ Fully TTL Compatible
- ☐ Single System Clock Required (Enable)
- ☐ Selectable Prescaler on Time 3 Capable of 4MHz for the S6840, 6MHz for the S68A40 and 8MHz for the S68B40
- ☐ Programmable Interrupts ($\overline{IRQ}$) Output to MPU
- ☐ Readable Down Counter Indicates Counts to Go to Time-Out
- ☐ Selectable Gating for Frequency or Pulse-Width Comparison
- ☐ $\overline{RESET}$ Input
- ☐ Three Asynchronous External Clock and Gate/ Trigger Inputs Internally Synchronized
- ☐ Three Maskable Outputs

General Description

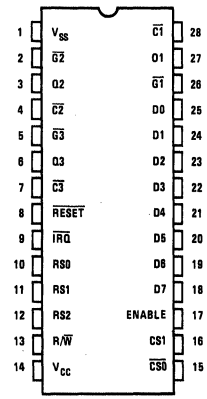
The S6840 is a programmable subsystem component of the S6800 family designed to provide variable system time intervals.

The S6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The S6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC} ..... − 0.3 to + 7.0V
Input Voltage V_{IN} ..... − 0.3 to + 7.0V
Operating Temperature Range T_A ..... 0° to + 70°C
Storage Temperature Range T_{stg} ..... − 55° to + 150°C
Thermal Resistance θ_{JA} ..... 82.5°C/W

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics: (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage		V_{SS} + 2.0		V_{CC}		V
V_{IL}	Input Low Voltage		V_{SS} − 0.3		V_{SS} + 0.8	V	
I_{IN}	Input Leakage Current			1.0	2.5	μA	V_{IN} = 0 to 5.25 V
I_{TSI}	Three-State (Off State) Input Current	D_0-D_7		2.0	10	μA	V_{IN} = 0.4 to 2.4 V
V_{OH}	Output High Voltage	D_0-D_7 All Others	V_{SS} + 2.4 V_{SS} + 2.4			V V	I_{LOAD} = − 205μA I_{LOAD} = − 200μA
V_{OL}	Output Low Voltage	D_0-D_7 01-03, $\overline{IRQ}$			V_{SS} + 0.4 V_{SS} + 0.4	V V	I_{LOAD} = 1.6mA I_{LOAD} = 3.2mA
I_{LOH}	Output Leakage Current (Off State)	$\overline{IRQ}$		1.0	10	μA	V_{OH} = 2.4V
P_D	Power Dissipation				550	mW	
C_{IN}	Capacitance	D_0-D_7 All Others			12.5 7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
C_{OUT}		$\overline{IRQ}$ 01, 02, 03			5.0 10	pF	V_{IN} = 0, T_A = + 25°C, f = 1.0MHz

Bus Timing Characteristics

Read (See Figure 1)

Symbol	Characteristic	S6840		S68A40		S68B40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYCE}	Enable Cycle Time	1.0	10	0.666	10	0.5	10	μs
PW_{EH}	Enable Pulse Width, High	0.45	4.5	0.280	4.5	0.22	4.5	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Times for Enable Input		25		25		25	ns
t_{CYCE}	Enable Cycle Time	1.0	10	0.666	10	0.5	10	μs
PW_{EH}	Enable Pulse Width, High	0.45	4.5	0.280	4.5	0.22	4.5	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns

Bus Timing Characteristics (Continued)

Read (See Figure 1)

Symbol	Characteristic	S6840		S68A40		S68B40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{DSW}	Data Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Times for Enable Input		25		25		25	ns

AC Operating Characteristics (See Figures 3 and 7)

Symbol	Characteristic	S6840		S68A40		S68B40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_r, t_f	Input rise and Fall Times (Figures 4 and 5) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$		1.0		0.666*		0.500*	μs
PW_L	Input Pulse Width (Figure 4) (Asynchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$	$t_{CYCE} + t_{su} + t_{hd}$		$t_{CYCE} + t_{su} + t_{hd}$		$t_{CYCE} + t_{su} + t_{hd}$		ns
PW_H	Input Pulse Width (Figure 5) (Asynchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$	$t_{CYCE} + t_{su} + t_{hd}$		$t_{CYCE} + t_{su} + t_{hd}$		$t_{CYCE} + t_{su} + t_{hd}$		ns
t_{su}	Input Setup Time (Figure 6) (Synchronous Mode) C, G and $\overline{Reset}$ $\overline{C3}$ (÷8 Prescaler Mode only)	200		120		75		ns
t_{hd}	Input Hold Time (Figure 6) (Synchronous Mode) C, G and $\overline{Reset}$ $\overline{C3}$ (÷8 Prescaler Mode only)	50		50		50		ns
PW_L, PW_H	Input Pulse Width (Synchronous Mode) $\overline{C3}$ (÷8 Prescaler Mode only)	125		84		62.5		ns
	Output Delay, 01-03 (Figure 7)							
t_{co}	(V_{OH} = 2.4V, Load B) TTL		700		460		340	ns
t_{cm}	(V_{OH} = 2.4V, Load D) MOS		450		450		340	ns
t_{cmos}	(V_{OH} = 0.7 V_{DD}, Load D) CMOS		2.0		1.35		1.0	μs
t_{IR}	Interrupt Release Time		1.2		0.9		0.7	μs

*t_r and $t_f \leq t_{CYCE}$

Figure 1. Bus Read Timing Characteristics (Read Information from PTM)

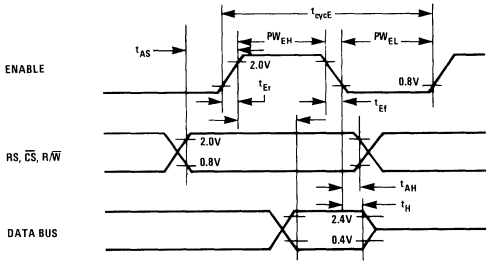


Figure 2. Bus Write Timing Characteristics (Write Information into PTM)

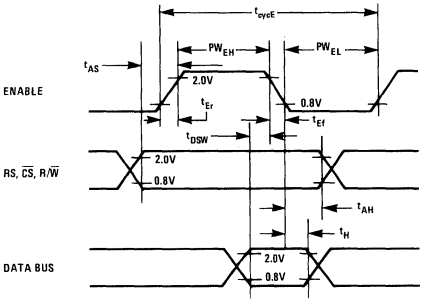


Figure 3. Input Pulse Width Low

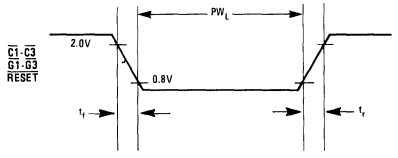


Figure 4. Input Pulse Width High

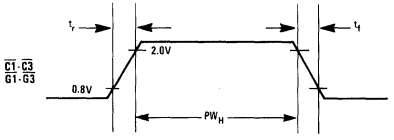


Figure 5. Input Setup and Hold Time

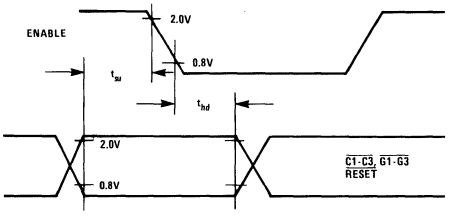
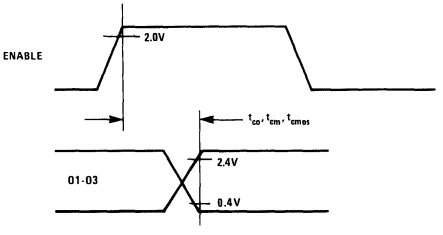


Figure 6. Output Delay



AMI

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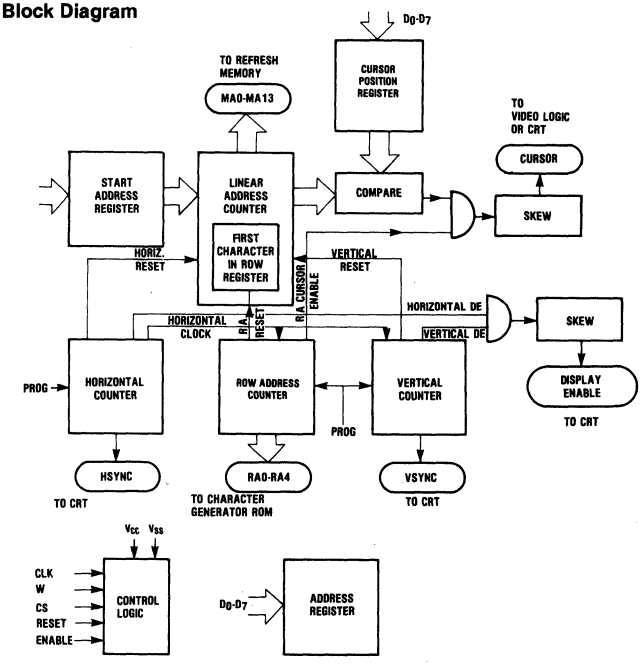
Preliminary Data Sheet **S68045/S68A045/S68B045**

CRT CONTROLLER (CRTC)

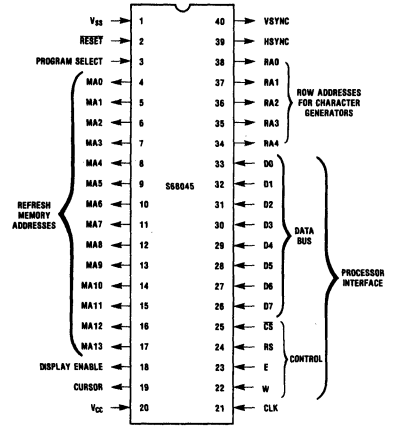
Features

- ☐ Generates Refresh Addresses and Row Selects
- ☐ Generates Video Monitor Inputs: Horizontal and Vertical Sync and Display Enable
- ☐ Low Cost; MC6845/SY6545 Pin Compatible
- ☐ Text Can Be Scrolled on a Character, Line or Page Basis
- ☐ Addresses 16K Bytes of Memory
- ☐ Screen Can Be Up to 128 Characters Tall By 256 Wide
- ☐ Character Font Can Be 32 Lines High With Any Width
- ☐ Two Complete ROM Programs
- ☐ Cursor and/or Display Can Be Delayed 0, 1 or 2 Clock Cycles
- ☐ Four Cursor Modes:
  - Non-Blink
  - Slow Blink
  - Fast Blink
  - Reverse Video With Addition of a Single TTL Gate
- ☐ Three Interlace Modes
  - Normal Sync
  - Interlace Sync
  - Interlace Sync and Video
- ☐ Full Hardware Scrolling
- ☐ NMOS Silicon Gate Technology
- ☐ TTL-Compatible, Single + 5 Volt Supply

Block Diagram



Pin Configuration



General Description

The S68045 CRT Controller performs the complex interface between an S6800 Family microprocessor and a raster scan display CRT system. The S68045 is designed to be flexible yet low cost. It is configured to both simplify the development and reduce the cost of equipment such as intelligent terminals, word processing, and information display devices.

The CRT Controller consists of both horizontal and vertical counting circuits, a linear address counter, and control registers. The horizontal and vertical counting circuits generate the Display Enable, HSYNC, VSYNC, and RA0-RA4 signals. The RA0-RA4 lines are scan line count signals to the external character generator ROM. The number of characters per character row, scan lines per character row, character rows per screen, and the horizontal and vertical SYNC position and width are all mask programmable. The S68045 is capable of addressing 16K of memory for display. The CRT may be scrolled or paged through the entire display memory under MPU control. The cursor control register determines the cursor location on the screen, and the cursor format can be programmed for fast blink, slow-blink, or non-blink appearance, with programmable size. By adding a single TTL gate, the cursor can even be reversed video. The device features two complete, independent programs implemented in user-specified ROM. Either set of programmable variables (50/60Hz refresh rate, screen format, etc.) is available to the user at any time.

The S68045 is pin compatible with the MC6845, operates from a single 5-volt supply, and is designed using the latest in minimum-geometry NMOS technology.

Absolute Maximum Ratings

Supply Voltage V_{CC} ..... −0.3°C to +7.0°C
Input Voltage V_{IN} ..... −0.3V to +7.0V
Operating Temperature Range T_A ..... 0°C to +70°C
Storage Temperature Range T_{stg} ..... −55°C to +150°C

Bus Timing Characteristics

Symbol	Parameter	S68045		S68A045		S68B045		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{cyc(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er}, t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Electrical Characteristics

$V_{CC} = 5.0V \pm 5\%$; $V_{SS} = 0$, $T_A = 0°C$ to $+70°C$ unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	−0.3		0.8	Vdc	
I_{IN}	Input Leakage Current		1.0	2.5	μAdc	
V_{OH}	Output High Voltage	2.4			Vdc	$I_{LOAD} = -100\mu A$
V_{OL}	Ouput Low Voltage			0.4	Vdc	$I_{LOAD} = 1.6mA$
P_D	Power Dissipation		600		mW	
C_{IN}	Input Capacitance D0-D7 All Others			12.5 10	pF pF	
C_{OUT}	Output Capacitance—All Outputs			10	pF	
P_{WCL}	Minimum Clock Pulse Width, Low	160			ns	
P_{WCH}	Clock Pulse Width, High	200		10,000	ns	
f_C	Clock Frequency			2.5	MHz	
t_{cr}, t_{cf}	Rise and Fall Time for Clock Input			20	ns	
t_{MAD}	Memory Address Delay Time			200	ns	
t_{RAD}	Raster Address Delay Time			200	ns	
t_{DTD}	Display Timing Delay Time			300	ns	
t_{HSD}	Horizontal Sync Delay Time			300	ns	
t_{VSD}	Vertical Sync Delay Time			300	ns	
t_{CDD}	Cursor Display Timing Delay Time			300	ns	

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S6846

ROM-I/O-TIMER

Features

- ☐ 2048 x 8-Bit Bytes of Mask-Programmable ROM
- ☐ 8-Bit Bidirectional Data Port for Parallel Interface Two Control Lines
- ☐ Programmable Interval Timer-Counter Functions
- ☐ Programmable I/O Peripheral Data, Control and Direction Registers
- ☐ Compatible With the Complete S6800 Microcomputer Product Family
- ☐ TTL-Compatible Data and Peripheral Lines
- ☐ Single 5 Volt Power Supply

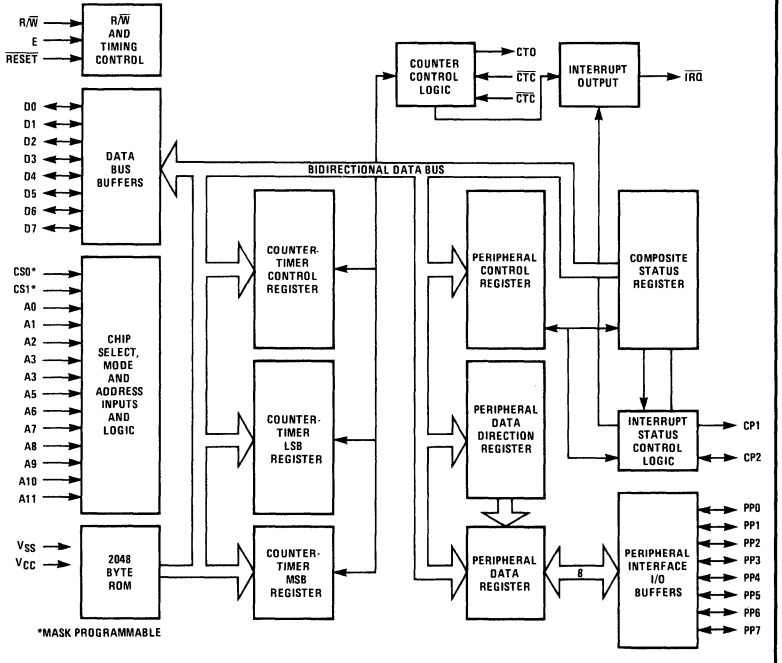
General Description

The S6846 combination chip provides the means, in conjunction with the S6802, to develop a basic 2-chip microcomputer system. The S6846 consists of 2048 bytes of mask-programmable ROM, an 8-bit bidirectional data port with control lines, and a 16-bit programmable timer-counter.

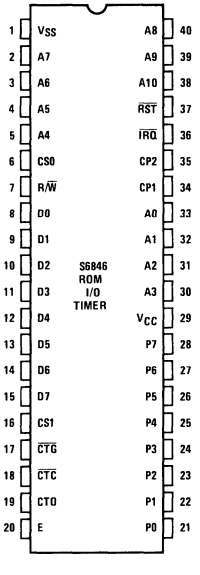
This device is capable of interfacing with the S6802 (basic S6800, clock and 128 bytes of RAM) as well as the S6800 if desired. No external logic is required to interface with most peripheral devices.

S6800 FAMILY

Block Diagram



Pin Configuration



General Description (Continued)

The S6846 combination chip may be partitioned into three functional operating sections: programmed storage, timer-counter functions, and a parallel I/O port.

Programmed Storage

The mask-programmable ROM section is similar to other AMI ROM products. The ROM is organized in a 2048 by 8-bit array to provide read only storage for a minimum microcomputer system. Two mask-programmable chip selects are available for user definition.

Address inputs A_0-A_{10} allow any of the 2048 bytes of ROM to be uniquely addressed. Internal registers associated with the I/O functions may be selected with A_0, A_1 and A_2. Bidirectional data lines (D_0-D_7) allow the transfer of data between the MPU and the S6846.

Timer-Counter Functions

Under software control this 16-bit binary counter may be programmed to count events, measure frequencies and time intervals, or similar tasks. It may also be used for square wave generation, single pulses of controlled duration, and gated delayed signals. Interrupts may be generated from a number of conditions selectable by software programming.

The timer-counter control register allows control of the interrupt enables, output enables, and selection of an internal or external clock source. Input pin CTC (counter-timer clock) will accept an asynchronous pulse to be used as a clock to decrement the internal register for the counter-timer. If the divide-by-8 prescaler is used, the maximum clock rate can be four times the master clock frequency with a maximum of 4MHz. Gate input ($\overline{CTG}$) accepts an asynchronous TTL-compatible signal which may be used as a trigger or gating function to the counter-timer. A counter-timer output ($\overline{CTO}$) is also available and is under software control via selected bits in the timer-counter control register. This mode of operation is dependent on the control register, the gate input, and the external clock.

Parallel I/O Port

The parallel bidirectional I/O port has functional operational characteristics similar to the B port on the S6821 PIA. This includes 8 bidirectional data lines and two handshake control signals. The control and operation of these lines are completely software programmable.

The interrupt input (CP1) will set the interrupt flags of the peripheral control register. The peripheral control (CP2) may be programmed to act as an interrupt input or as a peripheral control output.

Figure 1. Typical Microcomputer

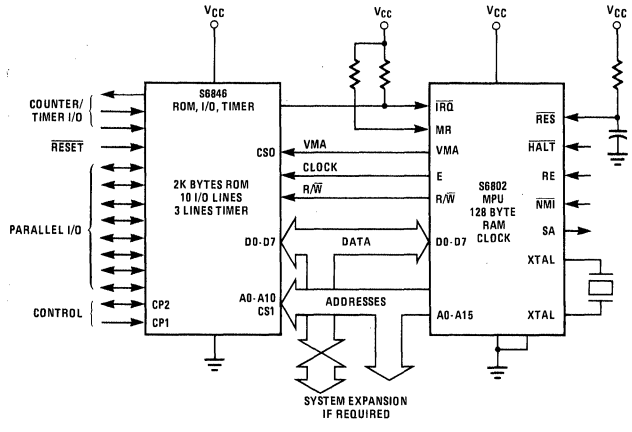


Figure 1 is a block diagram of a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the S6800 Microcomputer family if desired.

Absolute Maximum Ratings

Supply Voltage	− 0.3Vdc to + 7.0Vdc
Input Voltage	− 0.3Vdc to + 7.0Vdc
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	− 55°C to + 150°C
Thermal Resistance	70° C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics: (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage — All Inputs	V_{SS} + 2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage — All Inputs	V_{SS} − 0.3		V_{SS} + 0.8	Vdc	
V_{OS}	Clock Overshoot/Undershoot — Input High Level	V_{CC} − 0.5		V_{CC} + 0.5	Vdc	
	— Input Low Level	V_{SS} − 0.5		V_{SS} + 0.5		
I_{IN}	Input Leakage Current — R/$\overline{W}$, $\overline{Reset}$, CS_0, CS_1		1.0	2.5	μAdc	V_{IN} = 0 to 5.25 Vdc
	CP_1, $\overline{CTG}$, $\overline{CTC}$, E, A_0-A_{11}			100		
I_{TSI}	Three-State (Off State) Input Current — D_0-D_7		2.0	10	μAdc	
	PP_0-PP_7, CR_2			100		V_{IN} 0.4 to 2.4Vdc
V_{OH}	Output High Voltage				Vdc	
	D_0-D_7	V_{SS} + 2.4				I_{LOAD} = − 205μAdc,
	CP_2, PP_0-PP_7	V_{SS} + 2.4			Vdc	I_{LOAD} = − 145μAdc,
	Other Outputs	V_{SS} + 2.4				I_{LOAD} = − 100μAdc
V_{OL}	Output Low Voltage				Vdc	
	D_0-D_7			V_{SS} + 0.4		I_{LOAD} = 1.6mAdc
	Other Outputs			V_{SS} + 0.4		I_{LOAD} = 3.2mAdc
I_{OH}	Output High Current (Sourcing)				μAdc	
	D_0-D_7	− 205				V_{OH} = 2.4Vdc
	Other Outputs	− 200				
	CP_2, PP_0-PP_7	− 1.0		− 10	mADC	V_O = 1.5Vdc, the current for driving other than TTL, e.g., Darlington Base
I_{OL}	Output Low Current (Sinking)				mAdc	
	D_0-D_7	1.6				V_{OL} = 0.4Vdc
	Other Outputs	3.2				
I_{LOH}	Output Leakage Current (Off State) — $\overline{IRQ}$			10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation			1000	mW	
C_{IN}	Capacitance			20	pF	
	D_0-D_7			12.5		V_{IN} = 0, T_A = 25°C,
						f = 1.0MHz
	PP_0-PP_7, CP_2			10		
	A_0-A_{10}, R/$\overline{W}$, $\overline{Reset}$, CS_0, CS_1, CP_1, $\overline{CTC}$, $\overline{CTG}$			7.5		
	$\overline{IRQ}$					
C_{OUT}	PP_0-PP_7, CP_2, CTO			5.0	pF	
				10		
f	Frequency of Operation	0.1		1.0	MHz	
	Clock Timing					
t_{cycE}	Cycle Time	1.0			μs	
t_{RL}	Reset Low Time	2			μs	
t_{IR}	Interrupt Release			1.6	μs	

S6800 FAMILY

S6850/S68A50/S68B50

ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER (ACIA)

Features

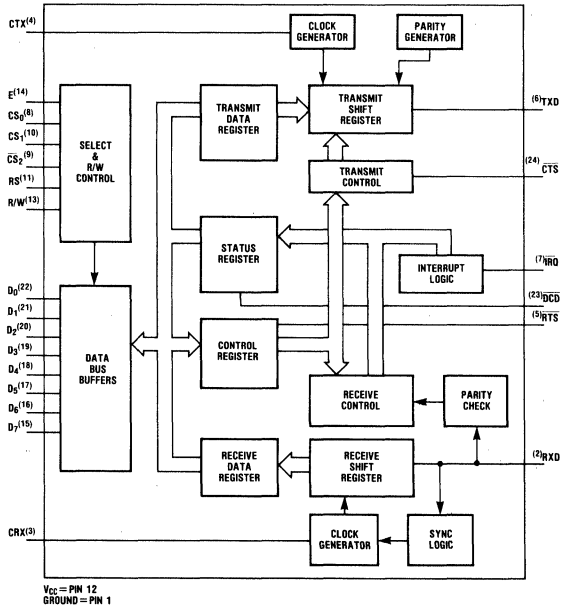
- ☐ 8-Bit Bi-directional Data Bus for Communication with MPU
- ☐ False Start Bit Deletion
- ☐ Peripheral/Modem Control Functions
- ☐ Double Buffered Receiver and Transmitter
- ☐ One or Two Stop Bit Operation
- ☐ Eight and Nine-Bit Transmission With Optional Even and Odd Parity
- ☐ Parity, Overrun and Framing Error Checking
- ☐ Programmable Control Register
- ☐ Optional ÷1, ÷16, and ÷64 Clock Modes
- ☐ Up to 500,000 bps Transmission

Functional Description

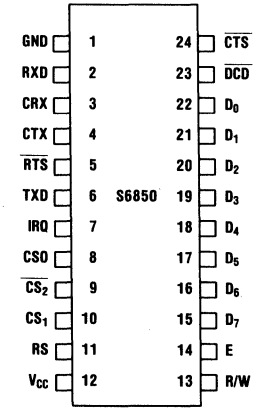
The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

Block Diagram



Pin Configuration



Absolute Maximum Ratings*

Supply Voltage	−0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Input Voltage	−0.3V to +7.0V
Storage Temperature Range	−55°C to +150°C

*NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (Static) Characteristics: (V_{CC} = 5.0V ±5%, T_A = 25°C, unless otherwise noted.)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage (Normal Operating Levels)	+2.0	—	V_{CC}	Vdc
V_{IL}	Input Low Voltage (Normal Operating Levels)	−0.3	—	+0.4	Vdc
V_{IHT}	Input High Threshold Voltage — All Inputs Except Enable	+2.0	—	—	Vdc
V_{ILT}	Input Low Threshold Voltage — All Inputs Except Enable	—	—	+0.8	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.0 Vdc) R/W, RS, CS_0, CS_1, $\overline{CS}_2$, Enable	—	1.0	2.5	μAdc
I_{TSI}	Three-State (Off State) Input Current (V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = max) D_0, D_7	—	2.0	10	μAdc
V_{OH}	Output High Voltage (I_{LOAD} = 100μAdc, Enable Pulse Width 25μs) — All Outputs Except $\overline{IRQ}$	+2.4	—	—	Vdc
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc) Enable Pulse Width 25μs	—	—	+0.4	Vdc
I_{LOH}	Output Leakage Current (Off State) — $\overline{IRQ}$				
P_D	Power Dissipation	—	300	525	mW
C_{IN}	Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)				pF
	D_0 - D_7		—	10	12.5
	R/W, RS, CS_0, CS_1, $\overline{CS}_2$, RXD, $\overline{CTD}$, $\overline{DCD}$, CTX, CRX		—	7.0	7.5
	Enable		—	7.0	7.5
C_{OUT}	Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	—	—	10	pF

Figure 1. Enable Signal Characteristics

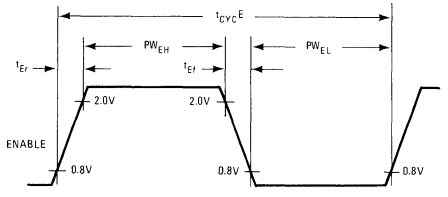
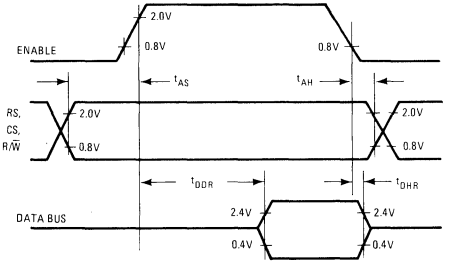


Figure 2. Bus Read Timing Characteristics



S6800 FAMILY

AC (Dynamic) Characteristics

Loading = 130pF and one TTL load for D_0-D_7 = 20pF and 1 TTL load for RTS and TXD = 100pF and 3KΩ to V_{CC} for IRQ.

		S6850		S68A50		S68B50		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
$t_{cyc(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er}, t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DDR}	Data Delay Time, Read		320		220		180	ns
t_{DHR}	Data Hold Time, Read	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Transmit/Receive Characteristics

Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
f_C					
	÷1 mode			500	KHz
	÷16 mode			800	KHz
	÷64 mode			800	KHz
PW_{CL}	Clock Pulse Width, Low State	600			nsec
PW_{CH}	Clock Pulse Width, High State	600			nsec
t_{TDD}	Delay Time, Transmit Clock to Data Out			1.0	μsec
t_{RDSU}	Set Up Time, Receive Data	500			nsec
t_{RDH}	Hold Time, Receive Data	500			nsec
t_{IRQ}	Delay Time, Enable to $\overline{IRQ}$ Reset			1.2	μsec
t_{RTS}	Delay Time, Enable to $\overline{RTS}$			1.0	μsec

Figure 3. Bus Write Timing Characteristics

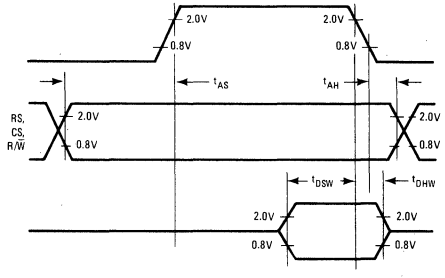
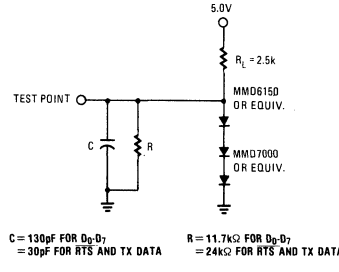


Figure 4. Bus Timing Test Loads



AMI

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S6852/S68A52/S68B52

SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

Features

- ☐ Programmable Interrupts From Transmitter, Receiver, and Error Detection Logic
- ☐ Character Synchronization on One or Two Sync Codes
- ☐ External Synchronization Available for Parallel-Serial Operation
- ☐ Programmable Sync Code Register
- ☐ Up to 600k bps Transmission
- ☐ Peripheral/Modem Control Functions
- ☐ Three Bytes of FIFO Buffering on Both Transmit and Receive
- ☐ Seven, Eight, or Nine Bit Transmission
- ☐ Optional Even and Odd Parity
- ☐ Parity, Overrun, and Underflow Status
- ☐ Clock Rates:
  - 1.0MHz
  - 1.5MHz
  - 2.0MHz

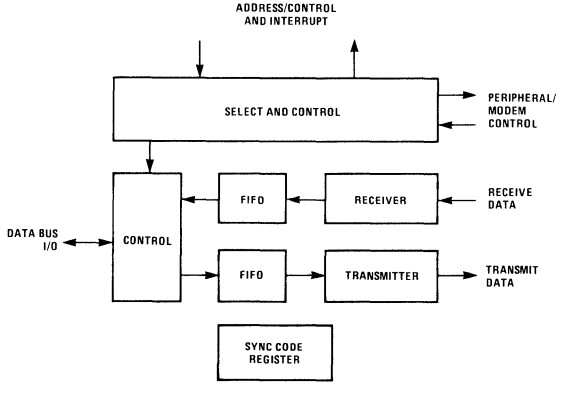
General Description

The S6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the S6800 Microprocessor systems.

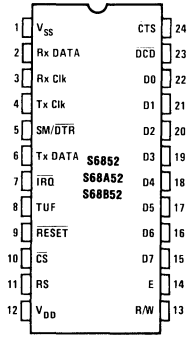
The bus interface of the S6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus sytem is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control,

S6800 FAMILY

Block Diagram



Pin Configuration



General Description (Continued)

receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

Absolute Maximum Ratings:

Supply Voltage	−0.3 to +7.0V
Input Voltage	−0.3 to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55° to +150°C
Thermal Resistance	+70°C/W

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted.)

Symbol	Characteristics		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage		V_{SS} + 2.0			V_{dc}
V_{IL}	Input Low Voltage				V_{SS} + 0.8	V_{dc}
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25Vdc)	Tx Clk, Rx Clk, Rx Data, Enable $\overline{Reset}$, RS, R/$\overline{W}$, $\overline{CS}$, $\overline{DCD}$, $\overline{CTS}$		1.0	2.5	μAdc
I_{TSI}	Three State (Off State) Input Current (V_{IN} = 0.4 to 2.4Vdc, V_{CC} = 5.25Vdc)	D_0-D_7		2.0	10	μAdc
V_{OH}	Output High Voltage I_{LOAD} = −205μAdc, Enable Pulse Width<25μs I_{LOAD} = −100μAdc, Enable Pulse Width<25μs	D_0-D_7 Tx Data, $\overline{DTR}$, TUF	 V_{SS} + 2.4 V_{SS} + 2.4		 Vdc	Vdc
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mAdc, Enable Pulse Width<25μs				V_{SS} + 0.4	Vdc
I_{LOH}	Output Leakage Current (Off State) V_{OH} = 2.4Vdc	$\overline{IRQ}$		1.0	10	μAdc
P_D	Power Dissipation			300	525	mW
C_{IN}	Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	D_0-D_7 All Other Inputs			12.5 7.5	pF
C_{OUT}	Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	Tx Data, SM/$\overline{DTR}$, TUF $\overline{IRQ}$			10 5.0	pF

Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C unless otherwise noted.)

Symbol	Characteristic	S6852		S68A52		S68B52		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
PW_{CL}	Minimum Clock Pulse Width, Low	700		400		280		ns
PW_{CH}	Minimum Clock Pulse Width, High	700		400		280		ns
f_C	Clock Frequency		600		1000		1500	kHz
t_{RDSU}	Receive Data Setup Time	350		200		160		ns

* 10μs or 10% of the pulse width, whichever is smaller.

Electrical Characteristics (Continued) (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C unless otherwise noted.)

Symbol	Characteristic	S6852		S68A52		S68B52		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RDH}	Receive Data Hold Time	350		200		160		ns
t_{SM}	Sync Match Delay Time		1.0		0.666		0.500	µs
t_{TDD}	Clock-to-Data Delay for Transmitter		1.0		0.666		0.500	µs
t_{TUF}	Transmitter Underflow		1.0		0.666		0.500	µs
t_{DTR}	$\overline{DTR}$ Delay Time		1.0		0.666		0.500	µs
t_{IR}	$\overline{Interrupt\ Request}$ Release Time		1.2		0.800		0.600	µs
t_{Res}	$\overline{Reset}$ Minimum Pulse Width	1.0		0.666		0.500		µs
t_{CTS}	$\overline{CTS}$ Setup Time	200		150		120		ns
t_{DCD}	$\overline{DCD}$ Setup Time	500		350		250		ns
t_r, t_f	Input Rise and Fall Times (except Enable) (0.8V to 2.0V)		1.0		1.0		1.0	µs

Bus Timing Characteristics

Symbol	Characteristic	S6852		S68A52		S68B52		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read								
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.5		µs
PW_{EH}	Enable Pulse Width, High	0.45	25	0.28	25	0.22	25	µs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		µs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns
Write								
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.5		µs
PW_{EH}	Enable Pulse Width, High	0.45	25	0.28	25	0.22	25	µs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		µs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Er}	Rise and Fall Time for Enable Input		25		25		25	ns

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S6854/S68A54/S68B54

ADVANCED DATA LINK CONTROLLER

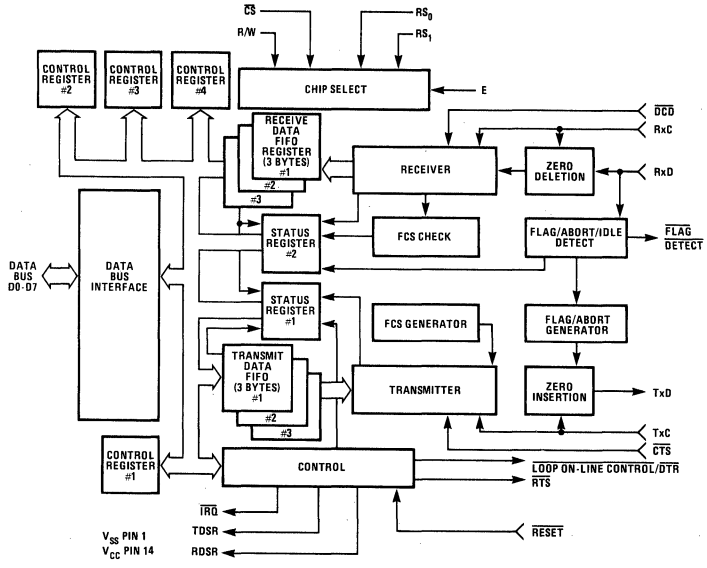
Features

- ☐ S6800 Compatible
- ☐ Protocol Features
  - ☐ Automatic Flag Detection and Synchronization
  - ☐ Zero Insertion and Deletion
  - ☐ Extendable Address, Control and Logical Control Fields (Optional)
  - ☐ Variable Word Length Info Field — 5, 6, 7, or 8-bits
  - ☐ Automatic Frame Check Sequence Generation and Check
  - ☐ Abort Detection and Transmission
  - ☐ Idle Detection and Transmission
- ☐ Loop Mode Operation
- ☐ Loop Back Self-Test Mode
- ☐ NRZ/NRZI Modes
- ☐ Quad Data Buffers for Each Rx and Tx
- ☐ Prioritized Status Register (Optional)
- ☐ MODEM/DMA/Loop Interface

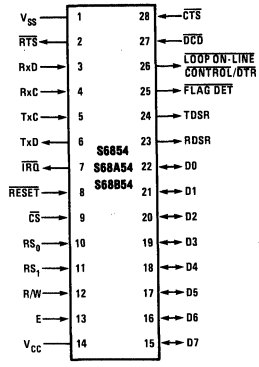
General Description

The S6854 ADLC performs the complex MPU/data communication link function for the "Advanced Data Communication Control Procedure" (ADCCP), High Level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations.

Block Diagram



Pin Configuration



Absolute Maximum Ratings*

Supply Voltage	− 0.3 to + 7.0V
Input Voltage	− 0.3 to + 7.0V
Operating Temperature Range	0° to + 70°C
Storage Temperature Range	− 55° to + 150°C
Thermal Resistance	70° C/W

* This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics: (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage		V_{SS} + 2.0		Vdc		
V_{IL}	Input Low Voltage				V_{SS} + 0.8	Vdc	
I_{IN}	Input Leakage Current	All Inputs Except D_0-D_7		1.0	2.5	μAdc	V_{IN} = 0 to 5.25 Vdc
I_{TSI}	Three-State (Off State) Input Current	D_0-D_7		2.0	10	μAdc	V_{IN} = 0.4 to 2.4 Vdc V_{CC} = 5.25 Vdc
V_{OH}	Output High Voltage	D_0-D_7 All Others	V_{SS} + 2.4 V_{SS} + 2.4			Vdc Vdc	I_{LOAD} = − 205μAdc I_{LOAD} = − 100μAdc
V_{OL}	Output Low Voltage				V_{SS} + 0.4	Vdc	I_{LOAD} = 1.6mAdc
I_{LOH}	Output Leakage Current (Off State)	$\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation				850	mW	
C_{IN}	Capacitance	D_0-D_7 All Other Inputs			12.5 7.5	pF pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
C_{OUT}		$\overline{IRQ}$ All Others			5.0 10	pF pF	

Symbol	Characteristic	S6854		S68A54		S68B54		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
PW_{CL}	Minimum Clock Pulse Width, Low	700		450		280		ns
PW_{CH}	Minimum Clock Pulse Width, High	700		450		280		ns
f_C	Clock Frequency		0.66		1.0		1.5	MHz
t_{RDSU}	Receive Data Setup Time	250		200		120		ns
t_{RDH}	Receive Data Hold Time	120		100		60		ns
t_{RTS}	Request-to-Send Delay Time		680		460		340	ns
t_{TDD}	Clock-to-Data Delay for Transmitter		460		320		250	ns
t_{FD}	Flag Detect Delay Time		680		460		340	ns
t_{DTR}	DTR Delay Time		680		460		340	ns
t_{LOC}	Loop On-Line Control Delay Time		680		460		340	ns
t_{RDSR}	RDSR Delay Time		540		400		340	ns
t_{TDSR}	TDSR Delay Time		540		400		340	ns
t_{IR}	Interrupt Request Release Time		1.2		0.9		0.7	μs
t_{RES}	Reset Minimum Pulse Width	1.0		0.65		0.40		μs
t_r, t_f	Input Rise and Fall Times (except Enable) (0.8V to 2.0V)		1.0*		1.0*		1.0*	μs

* 1.0μs or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics (V_{CC} = + 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + + 70°C unless otherwise noted.)

Symbol	Characteristic	S6854		S68A54		S68B54		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read								
t_{CYC}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns
Write								
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		0.22		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

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S6810/S68A10/S68B10

128x8 STATIC READ/WRITE MEMORY

Features

- ☐ Organized as 128 Bytes of 8 Bits
- ☐ Static Operation
- ☐ Bidirectional Three-State Data Input/Output
- ☐ Six Chip Enable Inputs (Four Active Low, Two Active High
- ☐ Single 5 Volt Power Supply
- ☐ TTL Compatible
- ☐ Maximum Access Time
  - 450ns for S6810
  - 360ns for S68A10
  - 250ns for S68B10

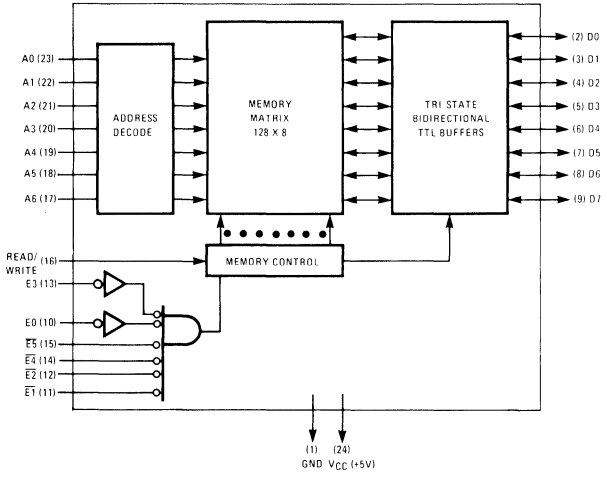
General Description

The S6810/S68A10 and S68B10 are static 128x8 Read/Write Memories designed and organized to be compatible with the S6800/S68A00 and S68B00 Microprocessors. Interfacing to the S6810/S68A10 and S68B10 consists of an 8-bit bidirectional data bus, seven address lines, s single Read/Write control line and six chip enable lines, four negative and two positive.

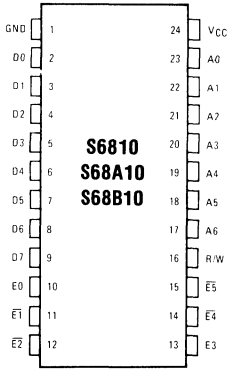
For ease of use, the S6810/S68A10 and S68B10 are a totally static memory requiring no clocks or cell refresh. The S6810/S68A10 and S68B10 are fabricated with N-Channel silicon gate depletion load technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

S6800 FAMILY

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage ..... – 0.3V to + 7.0V
Input Voltage ..... – 0.3V to + 7.0V
Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... – 55°C to + 150°C

D.C. Characteristics:

(V_{CC} = + 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{IN}	Input Current (A_n, R/W, CS_n, $\overline{CS_n}$)			2.5	μAdc	V_{IN} = 0V to 5.25V
V_{OH}	Output High Voltage	2.4			Vdc	I_{OH} = – 205μA
V_{OL}	Output Low Voltage			0.4	Vdc	I_{OL} = 1.0mA
I_{LO}	Output Leakage Current			10	μAdc	CS = 0.8V or CS = 2.0V, (Three State) V_{OUT} = 0.4V to 2.4V
I_{CC}	Supply Current S6810 S68A10/S68B10			80 100	mAdc mAdc	V_{CC} = 5.25V, all other pins grounded, T_A = 0°C

A.C. Characteristics:

Read Cycle

(V_{CC} = + 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

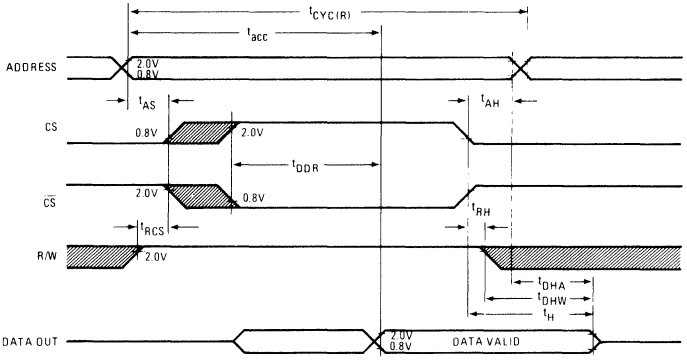
		S6810		S68A10		S68B10		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
$t_{CYC(R)}$	Read Cycle Time	450		360		250		ns
t_{ACC}	Access Time		450		360		250	ns
t_{AS}	Address Setup Time	20		20		20		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{DDR}	Data Delay Time (Read)		230		220		180	ns
t_{RCS}	Read to Select Delay Time	0		0		0		ns
t_{DHA}	Data Hold from Address	10		10		10		ns
t_H	Output Hold Time	10		10		10		ns
t_{DHW}	Data Hold from Write	10	60	10	60	10	60	ns
t_{RH}	Read Hold from Chip Select	0		0		0		ns

Write Cycle

(V_{CC} = +5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	S6810		S68A10		S68B10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{CYC(W)}$	Write Cycle Time	450		360		250		ns
t_{AS}	Address Setup Time	20		20		20		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{CS}	Chip Select Pulse Width	300		250		210		ns
t_{WCS}	Write to Chip Select Delay Time	0		0		0		ns
t_{DSW}	Data Setup Time (Write)	190		80		60		ns
t_H	Input Hold Time	10		10		10		ns
t_{WH}	Write Hold Time from Chip Select	0		0		0		ns

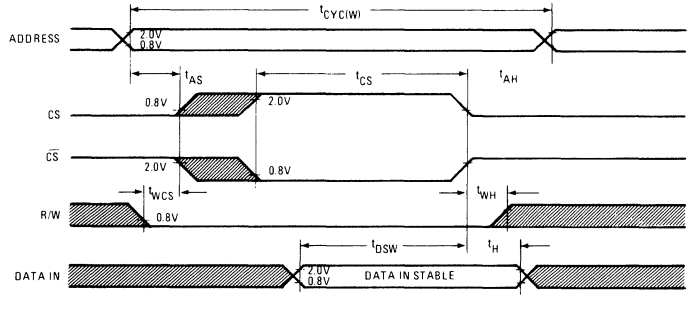
Read Cycle Timing



DON'T CARE

NOTE: CS AND $\overline{CS}$ CAN BE ENABLED FOR CONSECUTIVE READ CYCLES PROVIDED R/W REMAINS AT V_{IH}.

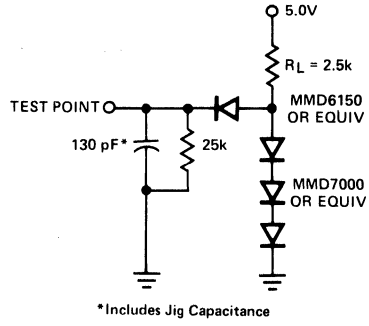
Write Cycle Timing



DON'T CARE

NOTE: CS AND $\overline{CS}$ CAN BE ENABLED FOR CONSECUTIVE WRITE CYCLES PROVIDED R/W IS STROBED TO V_{IH} BEFORE OR COINCIDENT WITH THE ADDRESS CHANGE, AND REMAINS HIGH FOR TIME t_{AS}.

AC Test Load



*Includes Jig Capacitance

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S9900

HIGH PERFORMANCE MICROPROCESSOR FAMILY

Contact factory for complete data sheets

S9900 Family Selection Guide

Microprocessors

S9900	16-Bit Microprocessor
S9980A	16-Bit Microprocessor 8-Bit Data Bus
S9995	16-Bit Microprocessor

Peripherals

S9901/S9901-4	Programmable Systems Interface (PSI)
S9902/S9902-4	UART/Asynchronous Communications Controller (USRT/ACC)

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S9900

16-BIT MICROPROCESSOR

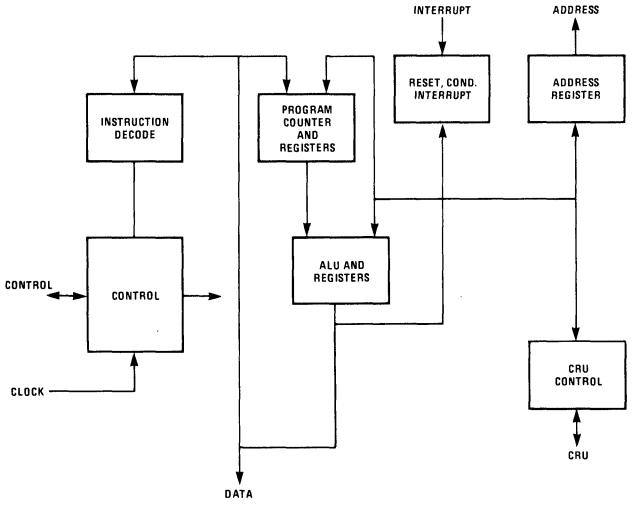
Features

- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability Including Multiply and Divide
- ☐ Up to 65,536 Bytes of Memory
- ☐ 3.3MHz Speed
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 16 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ N-Channel Silicon-Gate Technology

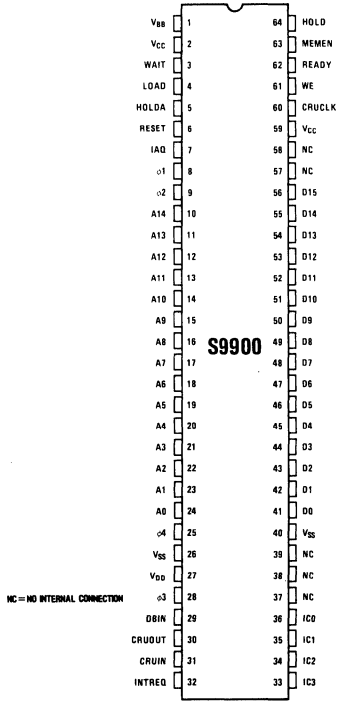
General Description

The S9900 microprocessor is a single-chip 16-bit central processing unit (CPU) produced using N-Channel silicon-gate MOS technology. The instruction set of the S9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. AMI provides a compatible set of MOS memory and support circuits to be used with an S9900 system. The system is fully supported by software and complete prototyping systems.

Block Diagram



Pin Configuration



S9900 FAMILY

S9900 Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply Voltage, V_{CC} (See Note 1)	−0.3V to +20V
Supply Voltage, V_{DD} (See Note 1)	−0.3V to +20V
Supply Voltage, V_{SS} (See Note 1)	−0.3V to +20V
All Input Voltages (See Note 1)	−0.3V to +20V
Output Voltage, (With Respect to V_{SS})	−2V to +7V
Continuous Power Dissipation	1.2W
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the most negative supply, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this section, voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage	−5.25	−5	−4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage (all inputs except clocks)	2.2	2.4	$V_{CC}+1$	V	
$V_{IH(\phi)}$	High-level clock input voltage	$V_{DD}-2$		V_{DD}	V	
V_{IL}	Low-level input voltage (all inputs except clocks)	−1	0.4	0.8	V	
$V_{IL(\phi)}$	Low-level clock input voltage	−0.3	0.3	0.6	V	
T_A	Operating free-air temperature	0		70	°C	

Timing Requirements Over Full Range of Recommended Operating Conditions (See Figures 1 and 2)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
t_C (ϕ)	Clock Cycle time	0.3	0.333	0.5	μs	
t_r (ϕ)	Clock rise time	10	12		ns	
t_f (ϕ)	Clock fall time	10	12		ns	
t_W (ϕ)	Pulse width, any clock high	40	45	100	ns	
$t_{\phi 1L, \phi 2L}$	Delay time, clock 1 low to clock 2 low**	0	5		ns	
$\tau_{\phi 2L, \phi 3L}$	Delay time, clock 2 low to clock 3 low**	0	5		ns	
$t_{\phi 3L, \phi 4L}$	Delay time, clock 3 low to clock 4 low**	0	5		ns	
$t_{\phi 4L, \phi 1L}$	Delay time, clock 4 low to clock 1 low**	0	5		ns	
$t_{\phi 1H, \phi 2H}$	Delay time, clock 1 high to clock 2 high***	73	83		ns	
$t_{\phi 2H, \phi 3H}$	Delay time, clock 2 high to clock 3 high***	73	83		ns	
$t_{\phi 3H, \phi 4H}$	Delay time, clock 3 high to clock 4 high***	73	83		ns	
$t_{\phi 4H, \phi 1H}$	Delay time, clock 4 high to clock 1 high***	73	83		ns	
t_{su}	Data or control setup time before clock 1	30			ns	
t_h	Data hold time after clock 1	10			ns	

** = Time between clock pulses

*** = Time between leading edges

Electrical Characteristics Over Full Range of Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter		Min.	Typ.†	Max.	Unit	Conditions
I_I	Input Current	Data Bus during DBIN		± 50	± 100	μA	$V_I = V_{SS}$ to V_{CC}
		$\overline{WE}$, $\overline{MEMEN}$, DBIN, Address bus, Data bus during HOLDA		+ 50	± 100		$V_I = V_{SS}$ to V_{CC}
		Clock*		± 25	± 75		$V_I = -0.3$ to 12.6V
		Any other inputs		± 1	± 10		$V_I = V_{SS}$ to V_{CC}
V_{OH}	High-level output voltage		2.4		V_{CC}	V	$I_O = -0.4$mA
V_{OL}	Low-level output voltage				0.65 0.50	V	$I_O = 3.2$mA $I_O = 2$mA
I_{BB}	Supply current from V_{BB}			0.1	1	mA	
I_{CC}	Supply current from V_{CC}			50	75	mA	
I_{DD}	Supply current from V_{DD}			25	45	mA	
C_i	Input capacitance (any inputs except clock and data bus)			10	15	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 1)}$	Clock-1 input capacitance			100	150	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 2)}$	Clock-2 input capacitance			150	200	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 3)}$	Clock-3 input capacitance			100	150	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 4)}$	Clock-1 input capacitance			100	150	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
C_{DB}	Data bus capacitance			15	25	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
C_O	Output capacitance (any output except data bus)			10	15	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}

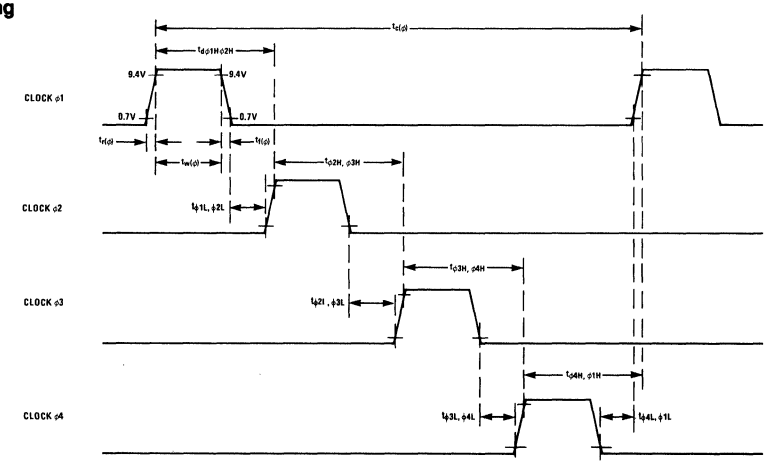
† All typical values are at $T_A = 25°C$ and nominal voltages

* D.C. Component of Operating Clock

Switching Characteristics Over Full Range of Recommended Operating Conditions (See Figure 2)

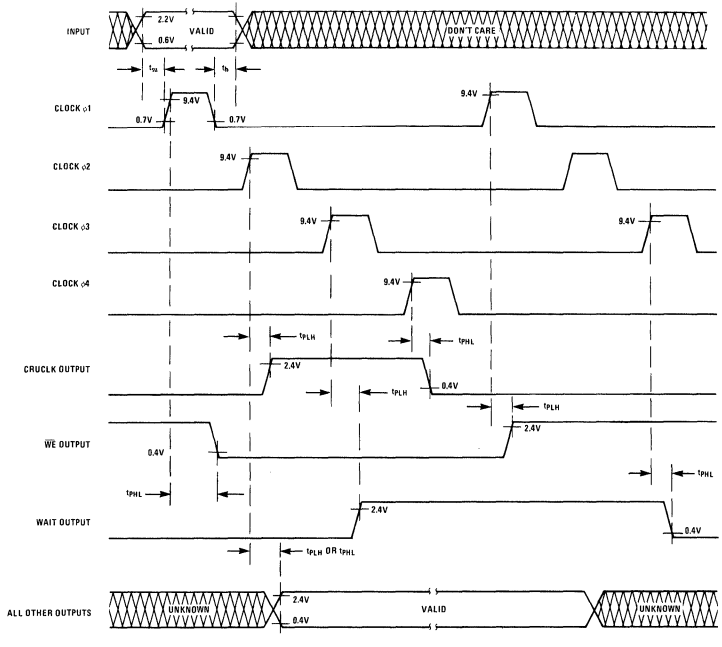
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PLH} or t_{PHL}	Propagation delay time, clocks to outputs					$C_L = 200$pF
	CRUCLK, WE, MEMEN, WAIT, DBIN			30	ns	
	All other outputs		20	40	ns	

Figure 1. Clock Timing



Note: All timing and voltage levels shown on ϕ1 apply to ϕ2, ϕ3, and ϕ4 in the same manner.

Figure 2. Signal Timing



†The number of cycles over which input/output data must/will remain valid can be determined from the number of wait states required for memory access. Note that in all cases data should not change during ϕ1.

Pin Description

Table 1 defines the S9900 pin assignments and describes the function of each pin.

Table 1. S9900 Pin Assignments and Functions

Signature	Pin	I/O	Description
			ADDRESS BUS
A0 (MSB)	24	OUT	A0 through A14 comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when $\overline{\text{MEMEN}}$ is active and I/O-bit addresses and external-instruction addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A1	23	OUT	
A2	22	OUT	
A3	21	OUT	
A4	20	OUT	
A5	19	OUT	
A6	18	OUT	
A7	17	OUT	
A8	16	OUT	
A9	15	OUT	
A10	14	OUT	
A11	13	OUT	
A12	12	OUT	
A13	11	OUT	
A14 (LSB)	10	OUT	
			DATA BUS
D0 (MSB)	41	I/O	D0 through D15 comprise the bidirectional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is active. The data bus assumes the high-impedance state when HOLDA is active.
D1	42	I/O	
D2	43	I/O	
D3	44	I/O	
D4	45	I/O	
D5	46	I/O	
D6	47	I/O	
D7	48	I/O	
D8	49	I/O	
D9	50	I/O	
D10	51	I/O	
D11	52	I/O	
D12	53	I/O	
D13	54	I/O	
D14	55	I/O	
D15 (LSB)	56	I/O	
			POWER SUPPLIES
V_{BB}	1		Supply voltage (-5V NOM)
V_{CC}	2,59		Supply voltage (5V NOM). Pins 2 and 59 must be connected in parallel.
V_{DD}	27		Supply volage (12V NOM)
V_{SS}	26,40		Ground reference. Pins 26 and 40 must be connected in parallel.
			CLOCKS
$\phi 1$	8	IN	Phase-1 clock
$\phi 2$	9	IN	Phase-2 clock
$\phi 3$	28	IN	Phase-3 clock
$\phi 4$	25	IN	Phase-4 clock

Table 1. S9900 Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
			BUS CONTROL
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the S9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains low in all other cases except when HOLDA is active.
$\overline{\text{MEMEN}}$	63	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	61	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the S9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0 through A2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	Interrupt request. When active (low), $\overline{\text{INTREQ}}$ indicates that an external-interrupt is requested. If $\overline{\text{INTREQ}}$ is active, the processor loads the data on the interrupt-code-input lines IC0 through IC3 into the internal interrupt-code-storage register. The code is compared to the interrupt mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15) the S9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. $\overline{\text{INTREQ}}$ should remain active and the processor will continue to sample IC0 through IC3 until the program enables a sufficiently low priority to accept the request interrupt.
IC0 (MSB)	36	IN	Interrupt codes. IC0 is the MSB of the interrupt code, which is sampled when $\overline{\text{INTREQ}}$ is active. When IC0 through IC3 are LLLH, the highest external-priority interrupt is being requested and when HHHH, the lowest-priority interrupt is being requested.
IC1	35	IN	
IC2	34	IN	
IC3 (LSB)	33	IN	
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9900 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.

*If the cycle following the present memory cycle is also a memory cycle, it, too, is completed before the S9900 enters the hold state. The maximum number of consecutive memory cycles is three.

Table 1. S9900 Assignments and Functions (Continued)

Signature	Pin	I/O	Description
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs (WE, MEMEN, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the S9900 has entered a wait state because of a not-ready condition from memory.
			TIMING AND CONTROL
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9900 is acquiring an instruction. IAQ can be used to detect illegal op codes.
LOAD	4	IN	Load. When active (low), LOAD causes the S9900 to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. LOAD will also terminate an idle state. If LOAD is active during the time RESET is released, then the LOAD trap will occur after the RESET fuction is completed. LOAD should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold-start ROM loaders. Additionally, front-panel routines can be implemented using CRU bits as front-panel-interface signals and software-control routines to control the panel operations.
RESET	6	IN	Reset. When active (low), RESET causes the processor to be reset and inhibits WE and CRUCLK. When RESET is released, the S9900 then initiates a level-zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. RESET will also terminate an idle state. RESET must be held active for a minimum of three clock cycles.

*If the cycle following the present memory cycle is also a memory cycle it, too, is completed before the S9900 enters the hold state. The maximum number of consecutive memory cycles is three.

AMI

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S9980A

16-BIT MICROPROCESSOR

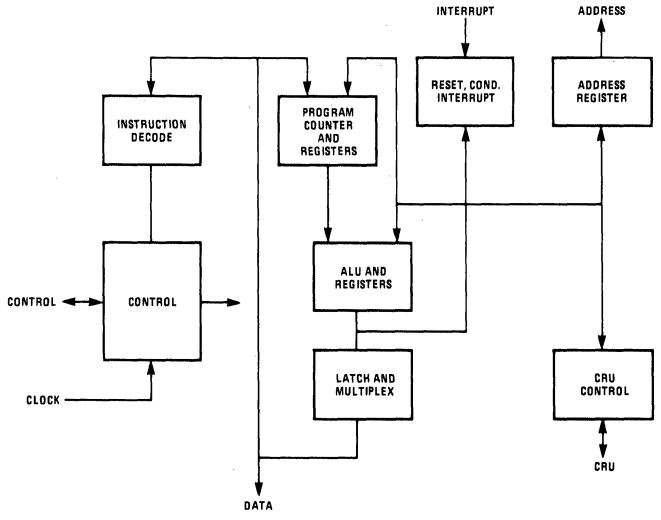
Features

- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability Including Multiply and Divide
- ☐ Up to 16,384 Bytes of Memory
- ☐ 8-Bit Memory Data Bus
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 4 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ On-Chip 4-Phase Clock Generator
- ☐ 40-Pin Package
- ☐ N-Channel Silicon-Gate Technology

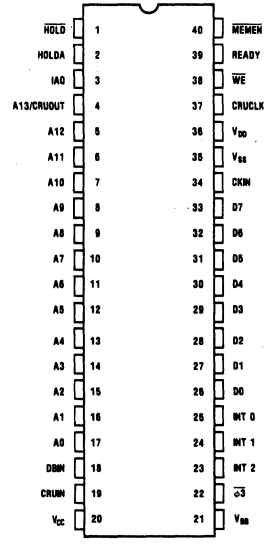
General Description

The S9980A microprocessor is a software-compatible member of AMI's 9900 family of microprocessors. Designed to minimize the system cost for smaller systems, the S9980A is a single-chip 16-bit central processing unit (CPU) which has an 8-bit data bus, on-chip clock, and is packaged in a 40-pin package. The instruction set of the S9980A includes the capabilities offered by full minicomputers and is exactly the same as the 9900s. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort.

Block Diagram



Pin Configuration



S9980A Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply Voltage, V_{CC} (See Note 1)	−0.3V to +15V
Supply Voltage, V_{DD} (See Note 1)	−0.3V to +15V
Supply Voltage, V_{BB} (See Note 1)	−5.25V to +0V
All Input Voltages (See Note 1)	−0.3V to +15V
Output Voltage, (See Note 1)	−2V to +7V
Continuous Power Dissipation	1.4W
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the most negative supply, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this section, voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage	−5.25	−5	−4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage	2.2	2.4	$V_{CC}+1$	V	
V_{IL}	Low-level input voltage	−1	0.4	0.8	V	
T_A	Operating free-air temperature	0	20	70	°C	

Electrical Characterisitcs Over Full Range of Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter		Min.	Typ.*	Max.	Unit	Conditions
I_I	Input Current	Data Bus during DBIN			±75	μA	$V_I = V_{SS}$ to V_{CC}
		$\overline{WE}$, $\overline{MEMEN}$, $\overline{DBIN}$, during HOLDA			±75	μA	$V_I = V_{SS}$ to V_{CC}
		Any other inputs			±10	μA	$V_I = V_{SS}$ to V_{CC}
V_{OH}	High-level output voltage		2.4			V	$I_O = -0.4$mA
V_{OL}	Low-level output voltage				0.5 0.65	V	$I_O = 2$mA $I_O = 3.2$mA
I_{BB}	Supply current from V_{BB}				1	mA	
I_{CC}	Supply current from V_{CC}			50 40	60 50	mA	0°C 70°C
I_{DD}	Supply current from V_{DD}			70 65	80 75	mA	0°C 70°C
C_i	Input capacitance (any inputs except data bus)			15		pF	f = 1MHz, unmeasured pins at V_{SS}
C_{DB}	Data bus capacitance			25		pF	f = 1MHz, unmeasured pins at V_{SS}
C_o	Output capacitance (any output except data bus)			15		pF	f = 1MHz, unmeasured pins at V_{SS}

* All typical values are at $T_A = 25°C$ and nominal voltages

External Clock

The external clock on the S9980 uses the CKIN pin. The external clock source must conform to the following specifications:

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
f_{ext}	External source frequency*	6		10	MHz	
V_H	External source high level	2.2			V	
V_L	External source low level			0.8	V	
t_r/t_f	External source rise/fall time		10		ns	
t_{WH}	External source high level pulse width	40			ns	
t_{WL}	External source low level pulse width	40			ns	

*This allows a system speed of 1.5MHz to 2.5MHz

Switching characteristics Over Full Range of Recommended Operating Conditions

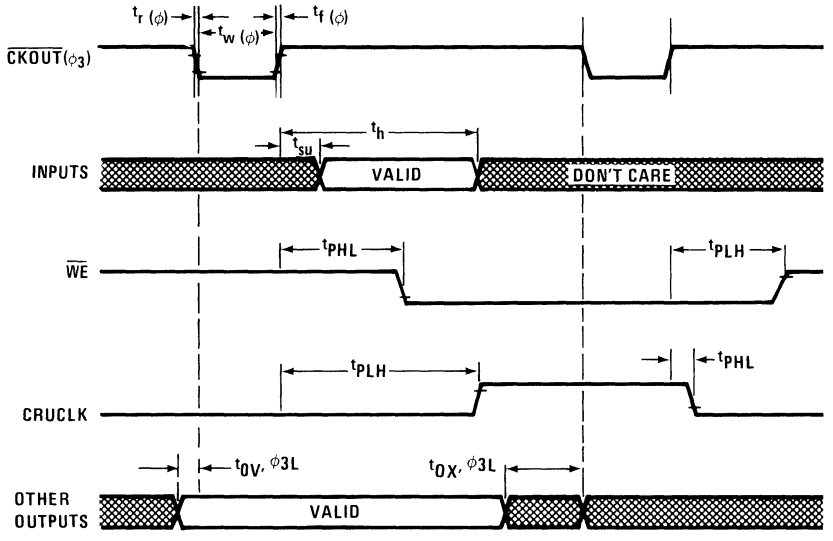
The timing of all the inputs and outputs is controlled by the internal 4 phase clock; thus all timings are based on the width of one phase of the internal clock. This is $1/f_{(CKIN)}$ (whether driven or from a crystal). This is also $1/4 f_{system}$. In the following table this phase time is denoted t_w.

All external signals are with reference to $\phi 3$ (see Figure 1).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_r ($\phi 3$)	Rise time of $\phi 3$	3	5	10	ns	
t_r ($\phi 3$)	Fall time of $\phi 3$	5	7.5	15	ns	
t_w ($\phi 3$)	Pulse width of $\phi 3$	t_w-15	t_w-10	t_w+10	ns	
t_{su}	Data or control setup time*	t_w-30			ns	
t_h	Data hold time*	$2t_{tw}+10$			ns	$t_w = 1/f_{(CKIN)}$
$t_{PHL}(\overline{WE})$	Propagation delay time WE high to low	t_w-10	t_w	t_w+20	ns	$= 1/4 f_{system}$
$t_{PLH}(\overline{WE})$	Propagation delay time WE low to high	t_w	t_w+10	t_w+30	ns	$C_L = 200pF$
$t_{PHL(CRUCLK)}$	Propagation delay time, CRUCLK high to low	-20	-10	$+10$	ns	
$t_{PHL(CRUCLK)}$	Propagation delay time, CRUCLK low to high	$2t_w-10$	$2t_w$	$2t_w+20$	ns	
t_{OV}	Delay time from output valid to $\phi 3$ low	t_w-50	t_w-30		ns	
t_{OX}	Delay time from output invalid to $\phi 3$ low		t_w-20	t_w	ns	

*All inputs except IC0–IC2 must be synchronized to meet these requirements. IC0–IC2 may change synchronously.

Figure 1. External Signal Timing



Pin Description

Table 1 defines the S9980A pin assignments and describes the function of each pin.

Table 1. S9980A Pin Assignments and Functions

Signature	Pin	I/O	Description
A0 (MSB)	17	OUT	**ADDRESS BUS**
A1	16	OUT	A0 through A13 comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when MEMEN is active and I/O-bit addresses and external-instruction addresses to the I/O system when MEMEN is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A2	15	OUT	
A3	14	OUT	
A4	13	OUT	
A5	12	OUT	
A6	11	OUT	
A7	10	OUT	
A8	9	OUT	
A9	8	OUT	
A10	7	OUT	
A11	6	OUT	
A12	5	OUT	
A13/CRUOUT	4	OUT	**CRUOUT** Serial I/O data appears on A13 when an LDCR, SBZ and SBO instruction is executed. This data should be sampled by the I/O interface logic when CRUCLK goes active (high). One bit of the external instruction code appears on A13 during external instruction execution.
D0 (MSB)	26	I/O	**DATA BUS**
D1	27	I/O	D0 through D7 comprise the bidirectional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when MEMEN is active. The data bus assumes the high-impedance state when HOLDA is active.
D2	28	I/O	
D3	29	I/O	
D4	30	I/O	
D5	31	I/O	
D6	32	I/O	
D7 (LSB)	33	I/O	

Table 1. S9980A Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
			POWER SUPPLIES
V_{BB}	21		Supply voltage (−5V NOM)
V_{CC}	20		Supply voltage (5V NOM)
V_{DD}	36		Supply voltage (12V NOM)
V_{SS}	35		Ground reference
			CLOCKS
CKIN	34	IN	Clock In. A TTL compatible input used to generate the internal 4-phase clock. CKIN frequency is 4 times the desired system frequency.
$\overline{\phi 3}$	22	OUT	Clock phase 3 ($\phi 3$) inverted; used as a timing reference.
			BUS CONTROL
DBIN	18	OUT	Data bus in. When active (high), DBIN indicates that the S9980A has disabled its output buffers to allow the memory to place memory-read data on the data bus during MEMEN. DBIN remains low in all other cases except when HOLDA is active at which time it is in the high-impedance state.
$\overline{\text{MEMEN}}$	40	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address. When HOLDA is active, $\overline{\text{MEMEN}}$ is in the high impedance state.
$\overline{\text{WE}}$	38	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the S9980 to be written into memory. When HOLDA is active, $\overline{\text{WE}}$ is in the high-impedance state.
CRUCLK	37	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0, A1, A13.
CRUIN	19	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A2 through A12).
INT2	23	IN	Interrupt code. Refer to interrupt discussion for detailed description.
INT1	24	IN	
INT0	25	IN	
			MEMORY CONTROL
$\overline{\text{HOLD}}$	1	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9980A enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.
HOLDA	2	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) are in the high-impedance state.
READY	39	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9980A enters a wait state and suspends internal operation until the memory systems indicated ready.
			TIMING AND CONTROL
IAQ	3	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9980A is acquiring an instruction. IAQ can be used to detect illegal op codes. It may also be used to synchronize LOAD stimulus.

*If the cycle following the present memory cycle is also a memory cycle it, too, is completed before S9980 enters hold state

AMI

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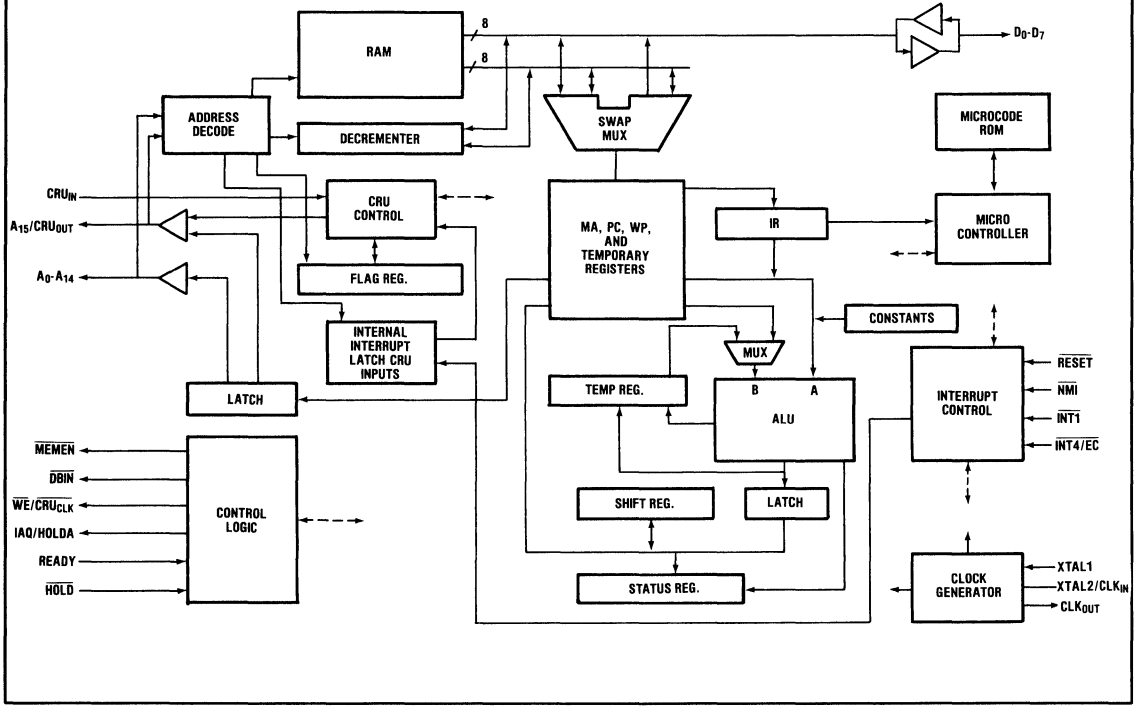
Preliminary Data Sheet **S9995**

16-BIT MICROPROCESSOR

Features

- ☐ 16-Bit Instruction Word
- ☐ Memory-to-Memory Architecture
- ☐ 65,536 Byte/32,768 Word Directly Addressable Memory Address Space
- ☐ Minicomputer Instruction Set Including Signed Multiply and Divide Instructions
- ☐ Multiple 16-Word Register Files (Workspaces) Residing in Memory
- ☐ 256 Bytes of On-Chip RAM
- ☐ Separate Memory and Interrupt Bus Structures
- ☐ 8-Bit Memory Data Bus
- ☐ 7 Prioritized Hardware Interrupts
- ☐ 16 Software Interrupts (XOPS)
- ☐ Programmed and DMA I/O Capability
- ☐ Serial I/O Via Communication Register Unit (CRU)
- ☐ On-Chip Time/Event Counter
- ☐ On-Chip Programmable Flags (16)
- ☐ Macro Instruction Detection (MID) Feature
- ☐ Automatic First Wait State Generation Feature
- ☐ Single 5V Supply
- ☐ 40-Pin Package
- ☐ N-Channel Silicon Gate MOS Technology
- ☐ On-Chip Clock Generator

Block Diagram



S9900 FAMILY

General Description

The S9995 microcomputer is a single-chip 16-bit central processing unit (CPU) with 256 bytes of on-chip random access memory (RAM). A member of the S9900 family of microprocessor and peripheral circuits, the S9995 is fabricated using N-channel silicon-gate MOS technology. The rich instruction set of the S9995 is based upon a unique memory-to-memory architecture that features multiple register files resident in memory. Memory-resident register files allow faster response to interrupts and increased programming flexibility. The inclusion of RAM, timer function, clock generator, interrupt interface, and a flexible flag register on-chip facilitates support of small system implementations.

All members of the S9900 family of peripheral circuits are compatible with the S9995. Providing a performance upgrade to the S9900 microprocessor, the S9995 instruction set is an opcode-compatible superset of the S9900 processor family.

S9995 Preliminary Electrical Specifications Absolute Maximum Ratings Over operating free-air temperature range (unless other wise noted)†

Supply Voltage, V_{CC}‡	− 0.3 to 7V
All Input Voltages	− 0.3 to 20V
Output Voltage	− 0.3 to 7V
Continuous Power Dissipation	1W
Operating Free-air Temperature Range	0°C to 70°C
Storage Temperature Range	− 55°C to + 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	4.5	5	5.5	V
Supply Voltage, V_{SS}		0		V
High-level Input Voltage V_{IH} (all inputs)	2			V
Low-level Input Voltage, V_{IL} (all inputs)			0.8	V
High-level Output Current, I_{OH} (all outputs)			100	μA
Low-level Output Current, I_{OL} (all outputs)			2	mA
Operating Free-air Temperature, T_A	0		70	°C

Electrical Characteristics Over recommended free-air temperature (unless otherwise noted)

Symbol	Parameter		Min.	Typ.†	Max.	Unit	Test Conditions
V_{OH}	High-level Output Voltage		2.4	3		V	V_{CC} = Min. I_{OH} = Max.
V_{OL}	Low-level Output Voltage			0.3	0.4	V	V_{CC} = Min. I_{OL} = Max.
I_{OZ}	Off-state Output Current				20	μA	V_{CC} = Max. V_O = 2.4V
					− 20	μA	V_O = 0.4V
I_I	Input Current				± 50	μA	$V_I = V_{SS}$ to V_{CC}
I_{CC}	Supply Current			150	180	mA	V_{CC} = Max.
C_I	Input Capacitance	Data Bus		25		pF	f = 1MHz, All other pins 0V
		All others		15			
C_O	Output Capacitance	Data Bus				pF	f = 1MHz, All other pins 0V
		All others		10			

† All typical values are at V_{CC} = 5V, T_A = 25°C

Timing Requirements Over recommended operating conditions

Symbol	Parameter	Min.	Nom.	Max.	Units
t_{su1}	Setup Time, READY prior to ↓ CLK_{OUT} (memory cycles)	100			ns
t_{h1}	Hold Time, READY after ↓ CLK_{OUT} (memory and CRU cycles)	0			ns
t_{su1}	Setup Time, Data Prior to ↓ CLK_{OUT}	65			ns
t_{h2}	Hold Time, Data After ↓ CLK_{OUT}	0			ns
t_{su3}	Setup Time, CRU_{IN} Prior to ↓ CLK_{OUT}	100			ns
t_{h3}	Hold Time, CRU_{IN} Prior to ↓ CLK_{OUT}	0			ns
t_{su4}	Setup Time, READY Prior to ↓ CLK_{OUT} (CRU cycles)	200			ns
t_{su5}	Setup Time, HOLD Prior to ↓ CLK_{OUT}	125			ns
t_{su6}	Setup Time, RESET and NMI Prior to ↓ CLK_{OUT}	140			ns
t_{WL4}	Pulse Width, Interrupt Inputs	$\frac{1}{2}t_{C2}$			ns
t_{f3}	Fall Time, INT1, INT4/EC Inputs			15	ns
t_{WH3}	Pulse Width, EC Input High	160			ns
t_{WL5}	Pulse Width, EC Input Low	160			ns
t_{C3}	Cycle Time, EC Input	$3t_{C2}$			ns

Switching Characteristics Over recommended operating conditions (See Figure 1)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t_{d1}	Delay Time, CLK_{IN} ↓ to CLK_{OUT} ↓	5	150		ns	
t_{C2}	CLK_{OUT} Cycle Time External Clock Source Internal Oscillator XTAL Freq = f_{XX}		$4t_{C1}$ $4/f_{XX}$		ns ns	
t_{r2}	Rise Time, CLK_{OUT} Output		20	30	ns	
t_{f2}	Fall Time, CLK_{OUT} Output		10	20	ns	
t_{WH2}	Pulse Width High, CLK_{OUT} Output		$\frac{1}{2}t_{C2}-t_{r2}$		ns	
t_{WL2}	Pulse Width Low, CLK_{OUT} Output		$\frac{1}{2}t_{C2}-t_{f2}$		ns	
t_{d2}	Delay Time, ↓ CLK_{OUT} to Address Valid	$\frac{1}{4}t_{C2}$		$\frac{1}{4}t_{C2}+45$	ns	SEE FIGURE 2 $R_1 = 2.4k\Omega$ $R_2 = 24k\Omega$ $C_L = 100pF$
t_{d3}	Delay Time, ↓ CLK_{OUT} to MEMEN Low	$\frac{1}{4}t_{C2}$		$\frac{1}{4}t_{C2}+40$	ns	
t_{d4}	Delay Time, ↓ CLK_{OUT} to MEMEN High	$\frac{1}{4}t_{C2}$		$\frac{1}{4}t_{C2}+50$	ns	
t_{d5}	Delay Time, ↑ CLK_{OUT} to DBIN Low	0		40	ns	
t_{d6}	Delay Time, ↑ CLK_{OUT} to DBIN High	0		50	ns	
t_{d7}	Delay Time, ↑ CLK_{OUT} to IAQ/HOLDA High	0		40	ns	
t_{d8}	Delay Time, ↑ CLK_{OUT} to IAQ/HOLDA Low	0		50	ns	
t_{d9}	Delay Time, ↑ CLK_{OUT} to Data Output Valid	0		40	ns	
t_{d10}	Delay Time, ↑ CLK_{OUT} to WE/CRU_{CLK} Low	0		40	ns	
t_{d11}	Delay time, ↑ CLK_{OUT} to WE/CRU_{CLK} High	0		50	ns	
t_{r3}	Rise Time, WE/CRU_{CLK} Outputs		20	50	ns	
t_{ACC}	Access Time, Memory Read Cycles		$\frac{3}{4}t_{C2}-135$		ns	
t_{h4}	Hold Time, Address and CRU_{OUT} Outputs	$\frac{1}{4}t_{C2}-40$			ns	
t_{h5}	Hold Time, Data Output	$\frac{1}{4}t_{C2}-40$			ns	
t_{WL3}	Pulse Width Low, WE/CRU_{CLK} Output	$\frac{1}{2}t_{C2}-40$			ns	
t_{dz}	Output Disable Time			$\frac{1}{4}t_{C2}+60$	ns	

Figure 1. Measurement Points for Switching Characteristics

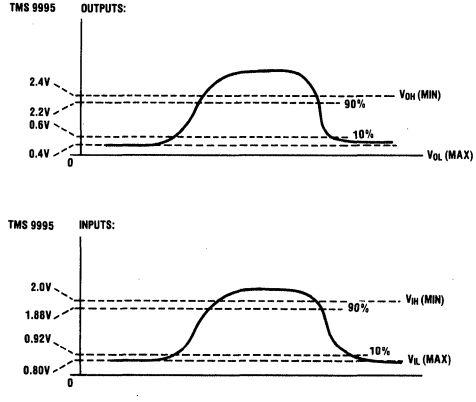
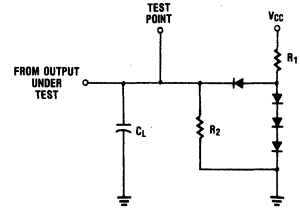


Figure 2. Switching Characteristics Test Load Circuit



NOTE: SEE SWITCHING CHARACTERISTICS FOR VALUES OF C_L, R_1, R_2. ALL DIODES ARE IN916 or IN3064.

Clock Characteristics

The S9995 can use either its internal oscillator or an external frequency source for a clock.

Internal Clock Option

The internal oscillator is enabled by connecting a crystal across XTAL1 and XTAL2/CLK_{IN} (See Figure 3). The frequency of CLK_{OUT} is one-fourth the crystal fundamental frequency.

Internal Oscillator

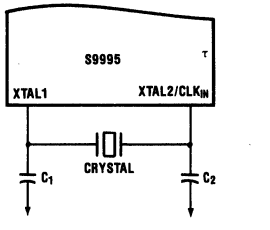
Parameter	Min.	Nom.	Max.	Unit	Test Conditions
Crystal Frequency, f_X	4	12	12.1	MHz	0°C — 70°C
C_1-C_2	10	15	25	pF	0°C — 70°C

External Clock Option

An external frequency source can be used by injecting the frequency directly into XTAL2/CLK_{IN} with XTAL1 left unconnected (See Figure 4). The external frequency must conform to the following specifications. The frequency of CLK_{OUT} is one-fourth of the frequency injected.

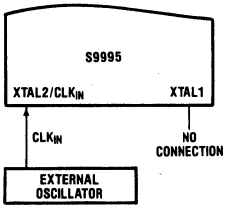
Symbol	Parameter	Min.	Nom.	Max.	Units
f_{ext}	External Source Frequency	4	12	12.1	MHz
t_{C1}	Input Oscillator Cycle Time	82	83.5	250	ns
t_{r1}	Input Oscillator Rise Time		5	15	ns
t_{WH1}	Input Oscillator Pulse Width High		$\frac{1}{2}t_{C1}-t_{R1}$		ns
t_{f1}	Input Oscillator Fall Time		5	15	ns
t_{WL1}	Input Oscillator Pulse Width Low		$\frac{1}{2}t_{C1}-t_{f1}$		ns

Figure 3. Internal Oscillator

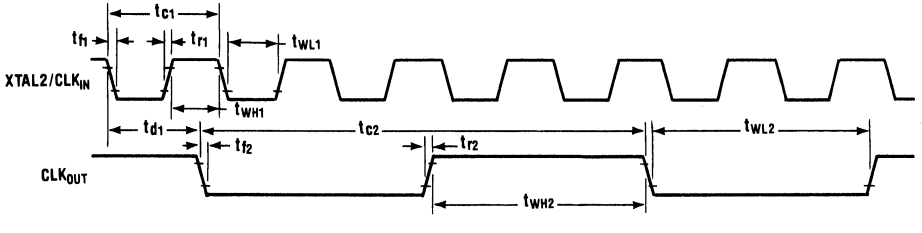


NOTE: C_1 AND C_2 REPRESENT THE TOTAL CAPACITANCE ON THESE PINS INCLUDING STRAYS AND PARASITICS.

Figure 4. External Oscillator

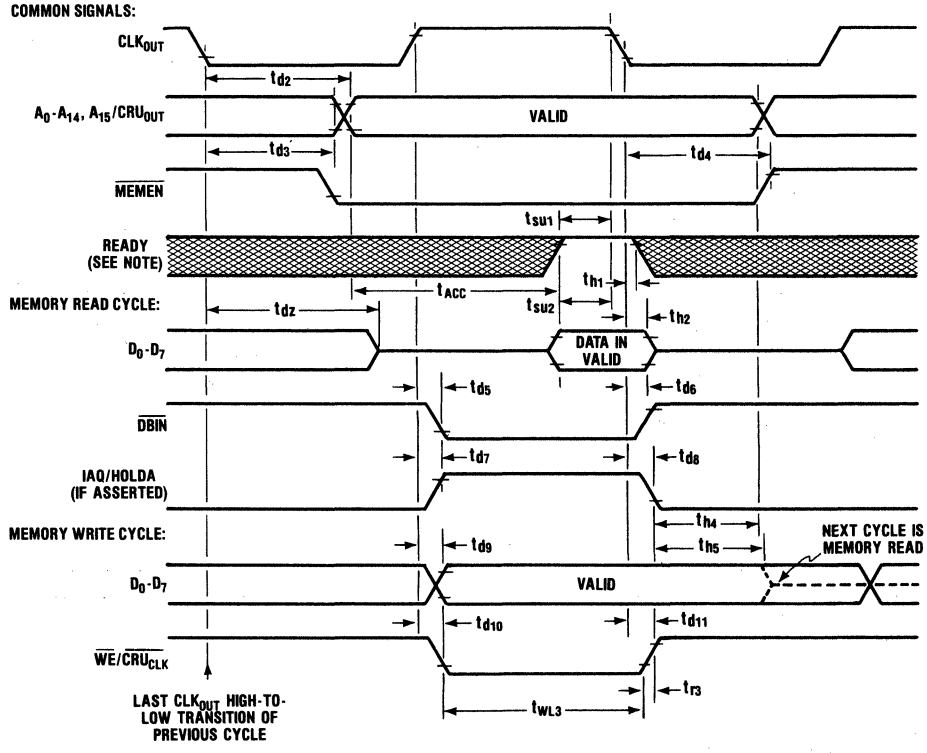


S9995 Clock Timing



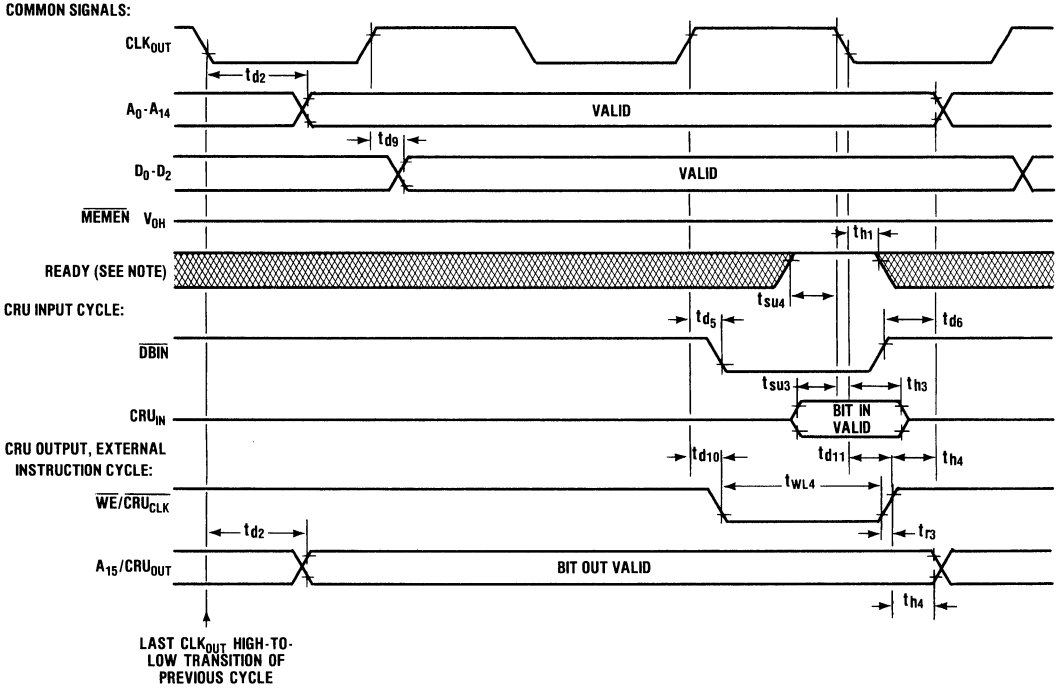
NOTE: t_{C1}, t_{f1}, t_{r1}, t_{WH1}, t_{WL1}, AND t_{d1} BECOME UNDEFINED PARAMETERS WHEN A CRYSTAL IS CONNECTED BETWEEN XTAL1 AND XTAL2/CLKIN AND THE INTERNAL OSCILLATOR IS CONSEQUENTLY ENABLED.

S9995 Memory Interface Timing



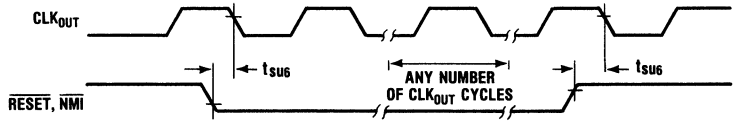
NOTE: CYCLE SHOWN IS FOR NO WAIT STATES (WITH WAIT STATES, CLK_{OUT} CYCLES ARE ADDED, BUT THE SWITCHING PARAMETERS DO NOT CHANGE).

S9995 CRU, External Instruction Timing

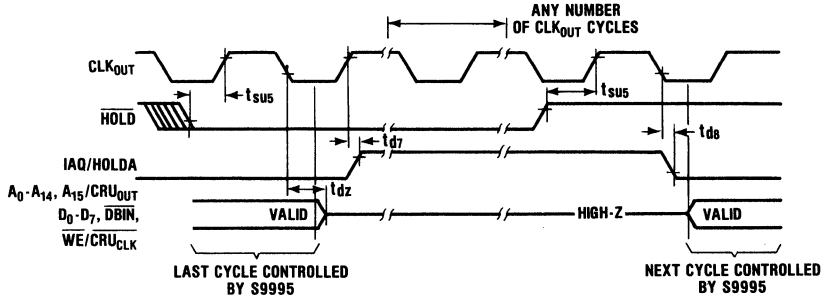


NOTE: CYCLE SHOWN IS FOR NO WAIT STATES (WITH WAIT STATES, CLK_{OUT} CYCLES GET ADDED, BUT THE SWITCHING PARAMETERS DO NOT CHANGE).

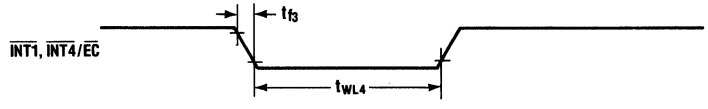
S9995 Reset and NMI Timing



S9995 HOLD Timing

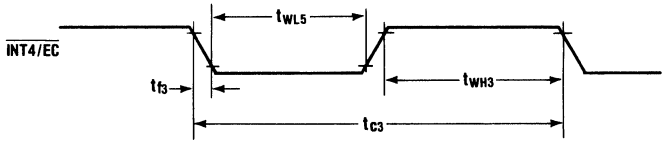


S9995 Interrupt Input Timing



NOTE: FOR INT4/EC, DECREMENTER IS CONFIGURED AS A TIMER OR IS DISABLED.

S9995 Event Counter Input Timing



NOTE: DECREMENTER IS CONFIGURED AS AN EVENT COUNTER AND IS ENABLED.

S9995 Pin Description

Table 1 defines the S9995 pin assignments and describes the function of each pin. Figure 5 illustrates the S9995 pin assignment information.

S9995 Pin Configuration

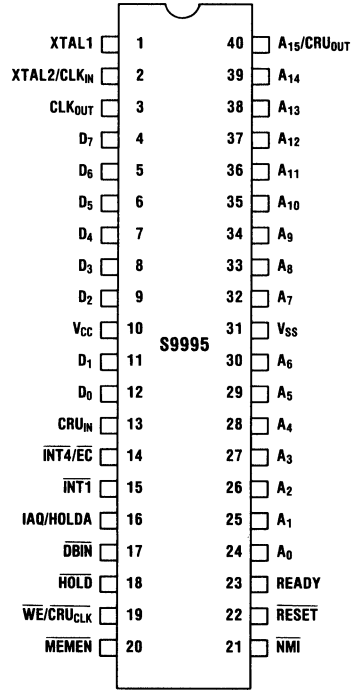


Table 1. S9995 Pin Description

Signal	Pin	I/O	Description
			Power Supplies
V_{CC}	10		Supply voltage (+ 5V Nom)
V_{SS}	31		Ground reference
			Clocks
XTAL2/CLK_{IN}	2	IN	Crystal input pin for internal oscillator. Also input pin for external oscillator.
XTAL1	1	IN	Crystal input pin for internal oscillator.
CLK_{OUT}	3	OUT	Clock output signal. The frequency of CLK_{OUT} is one fourth the oscillator input (external oscillator) or crystal (internal oscillator) frequency.
			Control
MEMEN	20	OUT	Memory enable. When active (low) MEMEN indicates that WE/CRU_{CLK}, DBIN, and the address and data buses are being used for a memory cycle. When inactive (high) MEMEN indicates that WE/CRU_{CLK}, DBIN, and the address and data buses are being used for a CRU cycle, or are indicating that the S9995 is performing an external instruction. MEMEN does not assume the high impedance state when the S9995 is in the Hold state.
DBIN	17	OUT	Data bus in. During memory read cycles, DBIN is active (low) to indicate that the S9995 has disabled its data bus output buffers to allow external memory to enable 3-state drivers that output data onto the data bus. During CRU input cycles, DBIN is also active to indicate that the CRU cycle is an input cycle. DBIN assumes the high impedance state when the S9995 is in the Hold state.
WE/CRU_{CLK}	19	OUT	Write enable/inverted CRU clock. When active (low), WE/CRU_{CLK} indicates that memory write data is available on the data bus (when MEMEN = 0); or that CRU data out is available on A_{15}/CRU_{OUT} (when MEMEN = 1 and $D_0 = D_1 = D_2 = 0$); or that an external interface should decode External instructions (when MEMEN = 1 and D_0, D_1, and D_2 are not all equal to 0). WE/CRU_{CLK} assumes the high impedance state when the S9995 is in the Hold state.
READY	23	IN	Ready. When active (high), READY indicates that the present external memory, CRU, or external instruction cycle is ready to be completed. When not ready is indicated, a Wait state (defined as extension of the present cycle by one CLK_{OUT} cycle) is entered. At the end of each Wait state READY is examined to determine if another Wait state is to be generated or if the cycle is to be completed.
HOLD	18	IN	Hold state request. When active (low), HOLD indicates to the S9995 that an external controller desires to use the address and data buses. Upon sensing a Hold request, the S9995 will enter a Hold state (defined as suspension of instruction execution) after it has completed its present cycle (see Section 2.3.1.1.3 for details of entry into a Hold state). At the beginning of the Hold state, the S9995 places DBIN, WE/CRU_{CLK}, and the address and data buses in the high impedance state, and then responds by asserting IAQ/HOLDA. When HOLD is removed, the S9995 returns to normal operation.
IAQ/HOLDA	16	OUT	Instruction acquisition/hold acknowledge. If IAQ/HOLDA is active (high) when MEMEN = 0, the S9995 is indicating that the memory read cycle in progress is that of reading an instruction opcode. If IAQ/HOLDA is active when MEMEN = 1, the S9995 is indicating that it is in the Hold state and that DBIN, WE/CRU_{CLK}, and the address and data buses are in the high impedance state.

Table 1. S9995 Pin Description (Continued)

Signal	Pin	I/O	Description
			Interrupts
RESET	22	IN	Reset. When active (low) RESET causes the S9995 to enter a RESET state (see Section 2.3.2.1.1) and inhibit MEMEN, DBIN, and WE/CRU_{CLK}. When RESET is released, the S9995 initiates a level zero interrupt sequence that acquires WP and PC from memory word addresses 0000 and 0002, and begins execution using this vector. RESET will terminate an idle state. RESET is a Schmitt-trigger input.
NMI	21	IN	Non-maskable Interrupt. When active (low), NMI causes the S9995 to execute a non-maskable interrupt sequence with the trap vector (WP and PC) in memory word addresses FFFC and FFFE. NMI will terminate an Idle state. NMI is recognized only once for each high-to-low transition. (NMI must be taken inactive before it will be recognized again.)
INT1	15	IN	Interrupt one. When active (low), INT1 will cause the S9995 to execute a level one interrupt trap if level one is not masked by the status register.
INT4/EC	14	IN	Interrupt four/event counter. When either the decrementer is not enabled or the decrementer is enabled and configured as an interval timer, INT4/EC being active (low) will cause the S9995 to execute a level four interrupt trap if level four is not masked by the status register. When the decrementer is enabled and configured as an event counter, a high-to-low transition on INT4/EC will cause the count in the decrementer to be decremented by one. (see Section 2.3.1.2.2 for details of enabling and configuring the decrementer.)
			Address Bus
A_0	24	OUT	Address Bus. A_0 is the most significant bit of the 16 bit memory address bus and the 15 bit CRU address bus. A_{14} is the 2nd least significant bit of the 16 bit memory address bus and the LSB of the 15 bit CRU address bus. The address bus assumes the high impedance state when the S9995 is in the Hold state.
A_1	25	OUT	
A_2	26	OUT	
A_3	27	OUT	
A_4	28	OUT	
A_5	29	OUT	
A_6	30	OUT	
A_7	32	OUT	
A_8	33	OUT	
A_9	34	OUT	
A_{10}	35	OUT	
A_{11}	36	OUT	
A_{12}	37	OUT	
A_{13}	38	OUT	
A_{14}	39	OUT	
A_{15}/CRU_{OUT}	40	OUT	Address bit 15/CRU output data. A_{15}/CRU_{OUT} is the LSB of the 16 bit memory address bus and the output data line for CRU output instructions. A_{15}/CRU_{OUT} assumes the high impedance state when the S9995 is in the Hold state.
			Data Bus
D_0	12	I/O	Data Bus. During memory cycles (MEMEN active) D_0 (the MSB) through D_7 (the LSB) are used to transfer data to/from the external memory system. During non-memory cycles (MEMEN inactive) D_0, D_1 and D_2 are used to indicate whether the S9995 is performing a
D_1	11	I/O	
D_2	9	I/O	

Table 1. S9995 Pin Description (Continued)

Signal	Pin	I/O	Description
			Data Bus (Continued)
D_3	8	I/O	CRU cycle or an external instruction. The data bus assumes the high impedance state
D_4	7	I/O	when the S9995 is in the Hold state.
D_5	6	I/O	
D_6	5	I/O	
D_7	4	I/O	
			CRU
CRU_{IN}	13	IN	CRU input data. During CRU cycles, CRU_{IN} is the input data line for CRU input data.

S9901/S9901-4

PROGRAMMABLE SYSTEMS INTERFACE CIRCUIT

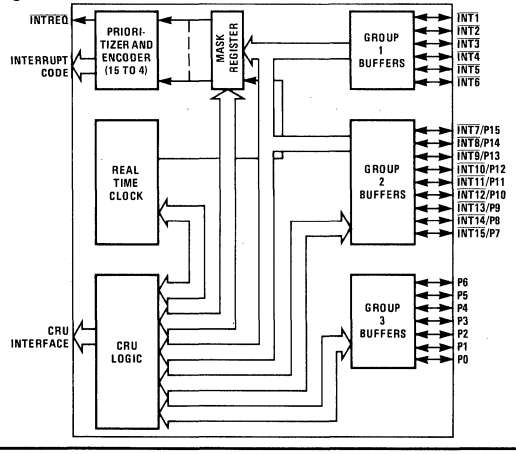
Features

- ☐ N-Channel Silicon-Gate Process
- ☐ 9900 Series CRU Peripheral
- ☐ Performs Interrupt and I/O Interface Functions
  - 6 Dedicated Interrupt Input Lines
  - 7 Dedicated I/O Ports
  - 9 Ports Programmable as Interrupts or I/O
- ☐ Easily Stacked for Interrupt and I/O Expansion
- ☐ Interval and Event Timer
- ☐ Single 5V Supply

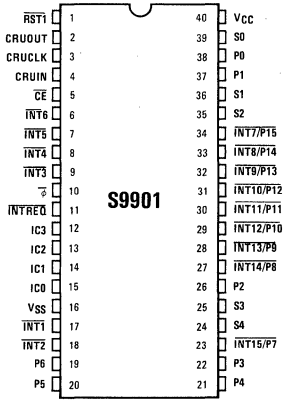
General Description

The S9901 Programmable Systems Interface is a multi-functioned component designed to provide low cost interrupts and I/O ports in a 9900/9980 microprocessor system. It is fabricated with N-channel silicon-gate technology and is completely TTL compatible on all inputs including the power supply (+5V) and single-phase clock. The Programmable Systems Interface provides a 9900/9980 system with interrupt control, I/O ports, and a real-time clock as shown on page 1.

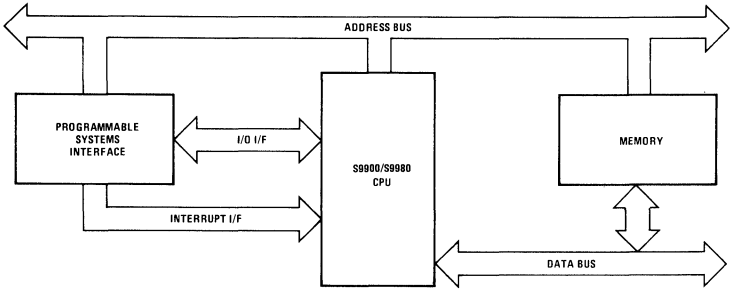
Block Diagram



S9901 Pin Configuration



S9900/9980 System



S9900 FAMILY

S9901 Electrical Specifications

Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply Voltages, V_{CC} and V_{SS} ..... −0.3V to +10V
All Input and Output Voltages ..... −0.3V to +10V
Continuous Power Dissipation 0.75W
Operating Free-Air Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_{SS}		0		V
High-Level Input Voltage, V_{IH}		2		V
Low-Level Input Voltage, V_{IL}		0.8		V
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics

Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_I	Input Current (Any Input)		±10		μA	$V_I = 0V$ to V_{CC}
V_{OH}	High Level Output Voltage		2.4		V	$I_{OH} = 100\mu A$
			2		V	$I_{OH} = -400\mu A$
V_{OL}	Low Level Output Voltage		0.4		V	$I_{OL} = 3.2mA$
I_{CC}	Supply Current from V_{CC}		100		mA	
I_{SS}	Supply Current from V_{SS}		200		mA	
$I_{CC(av)}$	Average Supply Current from V_{CC}		60		mA	$t_{C(0)} = 333ns$, $T_A = 25°C$
C_i	Capacitance, Any Input		10		pF	f = 1MHz,
C_o	Capacitance, Any Output		20		pF	All Other Pins at 0V

Timing Requirements

Over Full Range of Operating Conditions

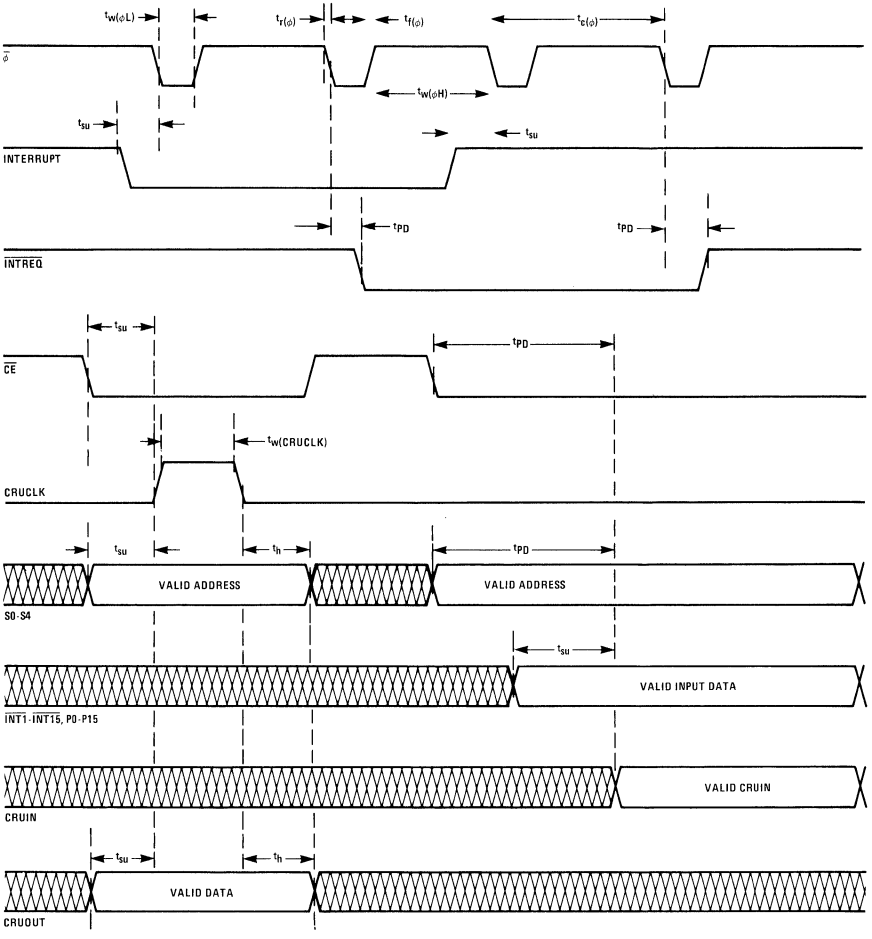
Symbol	Parameter	S9901			S9901-4			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
$t_{C(0)}$	Clock Cycle Time	300	333	2000	240	250	667	ns
$t_{r(0)}$	Clock Rise Time	5	10	40	5		40	ns
$t_{f(0)}$	Clock Fall Time	5	10	40	10		40	ns
$t_{W(0L)}$	Clock Pulse Low Width	45	55	300	40		300	ns
$t_{W(0H)}$	Clock Pulse High Width	225	240		180			ns
t_{su_1}	Setup Time for S_0-S_4, CE, or CRU_{OUT} Before CRU_{CLK}	100	200		80	80		ns
t_{su_3}	Setup Time, Input Before Valid CRU_{IN}	200	200		180	180		ns
t_{su_2}	Setup Time, Interrupt Before 0 Low	60	80		50	50		ns
$t_{W(CRUCLK)}$	CRU Clock Pulse Width	100			80			ns
t_h	Address Hold Time	60	80		50			ns

Switching Characteristics

Over Full Range of Recommended Operating Conditions

Symbol	Parameter	S9901 Min.	S9901 Typ.	S9901 Max.	S9901-4 Min.	S9901-4 Typ.	S9901-4 Max.	Unit	Test Conditions
t_{PD}	Propagation Delay, 0 Low to Valid $\overline{INTREQ}$, I_{C0}-I_{C3}		110	110		80	80	ns	C_L = 100pF, 2 TTL Loads
t_{PD}	Propagation Delay, S_0-S_4 or $\overline{CE}$ to Valid CRU_{IN}		320	320		240	240	ns	C_L = 100pF

Figure 1. Switching Characteristics



NOTE 1: ALL TIMING MEASUREMENTS ARE FROM 10% and 90% POINTS

S9900 FAMILY

Pin Definitions

Table 1 defines the S9901 pin assignments and describes the function of each pin.

Table 1.S9901 Pin Assignments and Functions

Signature	Pin	I/O	Description
$\overline{\text{INTREQ}}$	11	OUT	INTERRUPT Request. When active (low) $\overline{\text{INTREQ}}$ indicates that an enabled interrupt has been received. $\overline{\text{INTREQ}}$ will stay active until all enabled interrupt inputs are removed.
IC0 (MSB)	15	OUT	Interrupt Code lines. IC0–IC3 output the binary code corresponding to the highest priority enabled interrupt. If no enabled interrupts are active IC0–IC3 = (1,1,1,1)
IC1	14	OUT	
IC2	13	OUT	
IC3 (LSB)	12	OUT	
CE	5	IN	Chip Enable. When active (low) data may be transferred through the CRU interface to the CPU. CE has no effect on the interrupt control section.
S0	39	IN	Address select lines. The data bit being accessed by the CRU interface is specified by the 5-bit code appearing on S0–S4
S1	36	IN	
S2	35	IN	
S3	25	IN	
S4	24	IN	
CRUIN	4	OUT	CRU data in (to CPU). Data specified by S0–S4 is transmitted to the CPU by CRUIN. When $\overline{\text{CE}}$ is not active CRUIN is in a high-impedance state.
CRUOUT	2	IN	CRU data out (from CPU). When $\overline{\text{CE}}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the command bit specified by S0–S4.
CRUCLK	3	IN	CRU Clock (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{\text{RST1}}$	1	IN	Power Up Reset. When active (low) $\overline{\text{RST1}}$ resets all interrupt masks to "0", disables the clock, and programs all I/O ports to inputs. $\overline{\text{RST1}}$ has a Schmitt-Trigger input to allow implementation with an RC circuit as shown in Figure 6.
V_{CC}	40		Supply Voltage. + 5V nominal.
V_{SS}	16		Ground Reference.
ϕ	10		System Clock (ϕ3 in S9900 system, $\overline{\text{CKOUT}}$ in S9980 system).
$\overline{\text{INT1}}$	17	IN	Group 1, interrupt inputs. When active (low) the signal is ANDed with its corresponding mask bit and if enabled sent to the interrupt control section. INT1 has highest priority.
$\overline{\text{INT2}}$	18	IN	
$\overline{\text{INT3}}$	9	IN	
$\overline{\text{INT4}}$	8	IN	
$\overline{\text{INT5}}$	7	IN	
$\overline{\text{INT6}}$	6	IN	
$\overline{\text{INT7}}$/P15	34	I/O	Group 2. Programmable interrupt (active low) or I/O pins (true logic). Each pin is individually programmable as an interrupt, as input port, or an output port.
$\overline{\text{INT8}}$/P14	33	I/O	
$\overline{\text{INT9}}$/P13	32	I/O	
$\overline{\text{INT10}}$/P12	31	I/O	
$\overline{\text{INT11}}$/P11	30	I/O	
$\overline{\text{INT12}}$/P10	29	I/O	
$\overline{\text{INT13}}$/P9	28	I/O	
$\overline{\text{INT14}}$/P8	27	I/O	
$\overline{\text{INT15}}$/P7	23	I/O	
P0	38	I/O	Group 3, I/O ports (true logic). Each pin is individually programmable as an input port or an output port.
P1	37	I/O	
P2	26	I/O	
P3	22	I/O	
P4	21	I/O	
P5	20	I/O	
P6	19	I/O	

Functional Description

CPU Interface

The S9901 interfaces to the CPU through the Communications Register Unit (CRU) and the interrupt control lines as shown on page 1. The CRU interface consists of 5 address select lines (S_0-S_4), chip enable ($\overline{CE}$), and 3 CRU lines ($CRU_{\overline{IN}}$, CRU_{OUT}, CRU_{CLK}). When $\overline{CE}$ becomes active (low), the 5 select lines point to the CRU bit being accessed (see Table 2). In the case of a write, the datum is strobed off the CRU_{OUT} line by the CRU_{CLK} signal. For a read, the datum is sent to the CPU on the CRU_{IN} line. The interrupt control lines consist of an interrupt request line ($\overline{INTREQ}$) and 4 code lines (IC_0 -IC_3). The interrupt section of the S9901 prioritizes and encodes the highest priority active interrupt into the proper code to present to the CPU, and outputs this code on the IC_0-IC_3 code lines along with an active $\overline{INTREQ}$. Several S9901's can be used with the CPU by connecting all CRU and address lines in parallel and providing a unique chip select to each device.

System Interface

The system interface consists of 22 pins divided into 3 groups. The 6 pins in Group 1 ($\overline{INT_1}$-$\overline{INT_6}$) are normally dedicated to interrupt inputs (active low), but may also be used as input ports (true data in). Group 2 ($\overline{INT_7}/P_{15}$-$\overline{INT_{15}}/P_7$) consists of 9 pins which can be individually programmed as interrupt inputs (active low), input ports (true data in), or output ports (true data out). The remaining 7 pins which comprise Group 3 (P_0-P_6) are dedicated as individually programmable I/O ports (true data).

Interrupt Control

A block diagram of the interrupt control section is shown in Figure 2. The interrupt inputs (6 dedicated, 9 programmable) are sampled by ϕ (active low) and are ANDed with their respective mask bits. If an interrupt input is active (low) and enabled (MASK = 1), the signal is passed through to the priority encoder where the highest priority signal is encoded into a 4-bit binary code as shown in Table 3. The code along with the interrupt request is then output via the CPU interface on the leading edge of the next ϕ to ensure proper synchronization to the processor.

The output signals will remain valid until the corresponding interrupt input is removed, the interrupt is disabled (MASK = 0), or a higher priority enabled interrupt becomes active. When the highest priority enabled interrupt is removed, the code corresponding to the next highest priority enabled interrupt is output. If no enabled interrupt is active, all CPU interface lines ($\overline{INTREQ}$, IC_0-IC_3) are held high. $\overline{RST_1}$ (power-up-reset) will force the output code to (0,0,0,0) with $\overline{INTREQ}$ held high and will reset all mask bits low (interrupts disabled). Individual interrupts can be subsequently enabled (disabled) by programming the appropriate command bits. Unused interrupt inputs may be used as datum inputs by disabling the interrupt (MASK = 0).

Input/Output

A block diagram of the I/O section is shown in Figure 3. Up to 16 individually controlled I/O ports are available (7 dedicated, 9 programmable). $\overline{RST_1}$ or $\overline{RST_2}$ (a command bit) will program all ports to the input mode. Writing a datum to any port will program that port to the output mode and latch out the datum. The port will then remain in the output mode until either $\overline{RST_1}$ or $\overline{RST_2}$ is executed. Data present on the Group 2 pins can be read by either the Read Interrupt Commands or the Read Input Commands. Group 2 pins being used as input ports should have their respective Interrupt Mask values reset (low) to prevent false interrupts from occurring. In applications where Group 1 pins are not required as interrupt inputs, they may be used as input ports and read using the Read Input commands. As with Group 2 ports, any pins being used as input ports should have their respective Interrupt Masks disabled.

Table 2. CRU Bit Assignments

CRU Bit	S_0	S_1	S_2	S_3	S_4	CRU Read Data	CRU Write Data
0	0	0	0	0	0	CONTROL BIT(1)	CONTROL BIT(1)
1	0	0	0	0	1	$\overline{INT}_1/CLK_1$(2)	Mask $1/CLK_1$(3)
2	0	0	0	1	0	$\overline{INT}_2/CLK_2$	Mask $2/CLK_2$
3	0	0	0	1	1	$\overline{INT}_3/CLK_3$	Mask $3/CLK_3$
4	0	0	1	0	0	$\overline{INT}_4/CLK_4$	Mask $4/CLK_4$
5	0	0	1	0	1	$\overline{INT}_5/CLK_5$	Mask $5/CLK_5$
6	0	0	1	1	0	$\overline{INT}_6/CLK_6$	Mask $6/CLK_6$
7	0	0	1	1	1	$\overline{INT}_7/CLK_7$	Mask $7/CLK_7$
8	0	1	0	0	0	$\overline{INT}_8/CLK_8$	Mask $8/CLK_8$
9	0	1	0	0	1	$\overline{INT}_9/CLK_9$	Mask $9/CLK_9$
10	0	1	0	1	0	$\overline{INT}_{10}/CLK_{10}$	Mask $10/CLK_{10}$
11	0	1	0	1	1	$\overline{INT}_{11}/CLK_{11}$	Mask $11/CLK_{11}$
12	0	1	1	0	0	$\overline{INT}_{12}/CLK_{12}$	Mask $12/CLK_{12}$
13	0	1	1	0	1	$\overline{INT}_{13}/CLK_{13}$	Mask $13/CLK_{13}$
14	0	1	1	1	0	$\overline{INT}_{14}/CLK_{14}$	Mask $14/CLK_{14}$
15	0	1	1	1	1	$\overline{INT}_{15}/\overline{INTREQ}$	Mask $15/\overline{RST}_2$(4)
16	1	0	0	0	0	P_0 INPUT(5)	P_0 Output(6)
17	1	0	0	0	1	P_1 Input	P_1 Output
18	1	0	0	1	0	P_2 Input	P_2 Output
19	1	0	0	1	1	P_3 Input	P_3 Output
20	1	0	1	0	0	P_4 Input	P_4 Output
21	1	0	1	0	1	P_5 Input	P_5 Output
22	1	0	1	1	0	P_6 Input	P_6 Output
23	1	0	1	1	1	P_7 Input	P_7 Output
24	1	1	0	0	0	P_8 Input	P_8 Output
25	1	1	0	0	1	P_9 Input	P_9 Output
26	1	1	0	1	0	P_{10} Input	P_{10} Output
27	1	1	0	1	1	P_{11} Input	P_{11} Output
28	1	1	1	0	0	P_{12} Input	P_{12} Output
29	1	1	1	0	1	P_{13} Input	P_{13} Output
30	1	1	1	1	0	P_{14} Input	P_{14} Output
31	1	1	1	1	1	P_{15} Input	P_{15} Output

NOTES:

(1) 0 = Interrupt Mode 1 = Clock Mode

(2) Data present on INT input pin (or clock value) will be read regardless of mask value.

(3) While in the Interrupt Mode (Control Bit = 0) writing a "1" into mask will enable interrupt; a "0" will disable.

(4) Writing a zero to bit 15 while in the clock mode (Control Bit = 1) executes a software reset of the I/O pins.

(5) Data present on the pin will be read. Output data can be read without affecting the data.

(6) Writing data to the port will program the port to the output mode and output the data.

Figure 2. Interrupt Control Logic

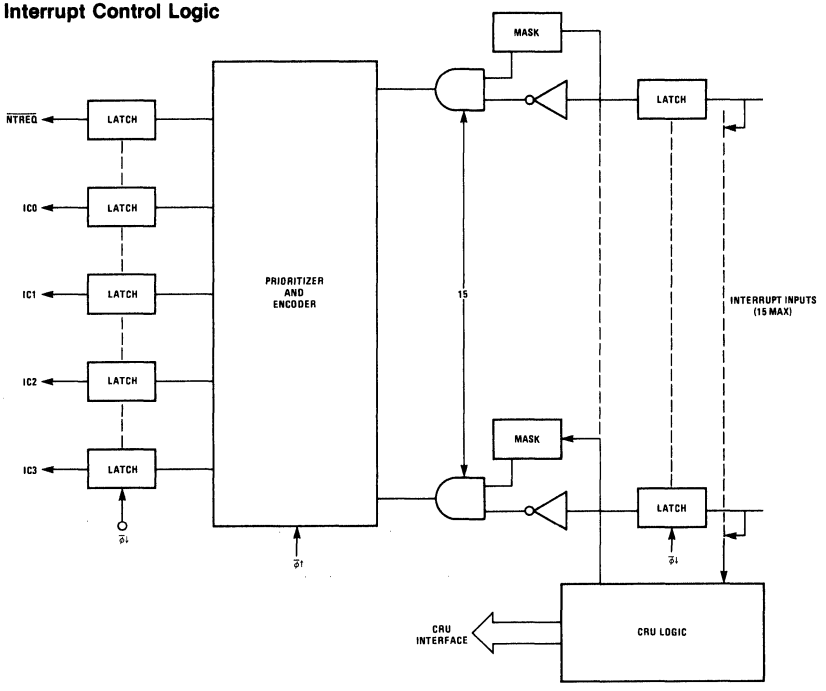


Table 3. Interrupt Code Generation

Interrupt/State	Priority	IC_0	IC_1	IC_2	IC_3	$\overline{INTREQ}$
$\overline{INT}_1$	1 (HIGHEST)	0	0	0	1	0
$\overline{INT}_2$	2	0	0	1	0	0
$\overline{INT}_3$/CLOCK	3	0	0	1	1	0
$\overline{INT}_4$	4	0	1	0	0	0
$\overline{INT}_5$	5	0	1	0	1	0
$\overline{INT}_6$	6	0	1	1	0	0
$\overline{INT}_7$	7	0	1	1	1	0
$\overline{INT}_8$	8	1	0	0	0	0
$\overline{INT}_2$	2	0	0	1	0	0
$\overline{INT}_9$	9	1	0	0	1	0
$\overline{INT}_{10}$	10	1	0	1	0	0
$\overline{INT}_{11}$	11	1	0	1	1	0
$\overline{INT}_{12}$	12	1	1	0	0	0
$\overline{INT}_{13}$	13	1	1	0	1	0
$\overline{INT}_{14}$	14	1	1	1	0	0
$\overline{INT}_{15}$	15 (LOWEST)	1	1	1	1	0
NO INTERRUPT	—	1	1	1	1	1

Programmable Real Time Clock

A block diagram of the programmable real time clock section is shown in Figure 4. The clock consists of a 14-bit counter that decrements at a rate of F(ϕ)64 (at 3MHz this results in a maximum interval of 349ms with a resolution of 21.3μs) and can be used as either an interval timer or as an event timer.

The clock is accessed by writing a one into the control bit (address 0) to force CRU bits 1-15 to clock mode (See Table 1). Writing a nonzero value into the clock register then enables the clock and sets its frequency. During system set up this entire operation can be accomplished with one additional I/O instruction (LCDR) as shown in Table 4. The clock functions as an interval timer by decrementing to zero, issuing an interrupt, and restarting at the programmed start value. When the clock interrupt is active, the clock mask (mask bit 3) must be written into (with either a "1' or a "0") to clear the interrupt.

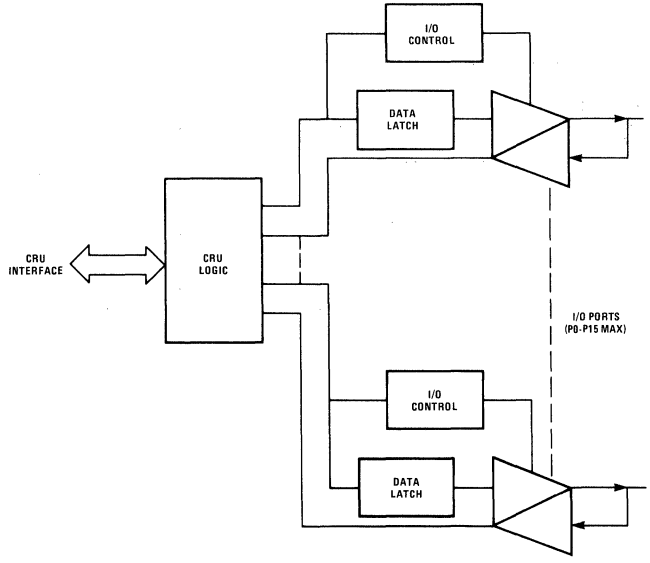
If a value other than that initially progammed is required, a new 14-bit clock start value is similarly programmed by executing a CRU write operation to the same locations. During programming the decrementer is restarted with the current start value after each start value bit is written. A timer restart can be easily implemented by writing a single bit to any of the clock bits.

The clock is disabled by $\overline{RST}_1$ (power-up-clear) or by writing a zero value into the clock register. Enabling the clock programs the third priority interrupt ($\overline{INT}_3$) as the clock interrupt and disables generation of interrupts from the $\overline{INT}_3$ input pin. When accessing the clock, all interrupts should be disabled to ensure that system integrity is maintained.

The clock can also function as an event timer since whenever the device is switched to the clock mode, by writing a one to the control bit, the current value of the clock is stored in the clock read register. Reading this value, and thus the elapsed event time, is accomplished by executing a 14-bit CRU read operation (addresses 1-14). The software example (Table 3) shows a read of the event timer.

The current status of the machine can always be obtained by reading the control (address zero) bit. A "0" indicates the machine is in an interrupt mode. Bits 1

Figure 3. I/O Interface



through 15 would normally be the interrupt input lines in this mode, but if any are not needed for interrupts, they may also be read with a CRU input command and interpreted as normal data inputs. A "1" read on the control bit indicates that the 9901 is in the clock mode. Reading bits 1 through 14 completes the event timer operation as described above. Reading bit 15 indicates whether the interrupt request line is active.

A software reset $\overline{RST}_2$ can be performed by writing a "1" to the control bit followed by writing a "1" to bit 15, which forces all I/O ports to the input mode.

Table 4. Software Examples

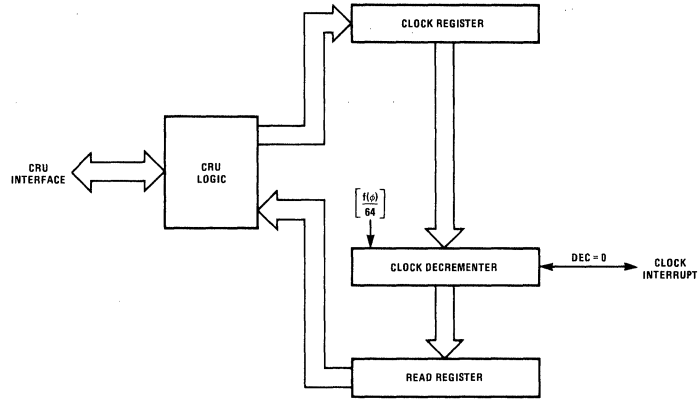
Assumptions

—System uses clock at maximum interval
—Total of 6 interrupts are used
—8 bits are used as output port
—8 bits are used as input port
—RST_1 (power up reset) has already been applied

System Setup for Interrupt	LI	R12,PSIBAS	Setup CRU Base Address to point 9901
	LDCR	@X,0	Program Clock with maximum interval
	LDCR	@Y,7	Re-enter interrupt mode and enable top 6 interrupts
System Setup for Output Ports	LI	R12,PSIBAS+16	Move CRU Base to point I/O port
	LDCR	R1,8	Move most significant byte of R_1 to output port
Read Programmed Inputs	LI	R12,PSIBAS+24	Move CRU Base to point to input ports
	STCR	R2,8	Move input port to most significant byte of R2
	(X) ⟶ FFFF		
	(Y) ⟶ 7FXX		
		Don't cares	
	BLWP	CLKVCT	Save Interrupt Mask
	•		
	•		
	•		
CLKPC	LIMI	0	Disable INTERRUPTS
	LI	R12,PSIBAS+1	Set up CRU Base
	SBO	−1	Set 9901 into Clock Mode, Latch Clock Value
	STCR	R4,14	Store Read Register Latch Value into R_4
	SBZ	−1	Reenter Interrupt Mode and Restarting Clock
	RTWP		Restore Interrupt Mask
	o		
	•		
	•		
CLKVCT	DATA	CLKWP, CLKPC	

S9900 FAMILY

Figure 4. Real Time Clock



System Operation

During power up, $\overline{RST}_1$ must be activated (low) for a minimum of 2 clock cycles to force the S9901 into a known state. $\overline{RST}_1$ will disable all interrupts, disable the clock, program all I/O ports to the mode, and force IC_0-IC_3 to (0,0,0,0) with $\overline{INTREQ}$ held high. System software must then enable the proper interrupts, program the clock (if used), and configure the I/O ports as required (see Table 4 for an example). After initial power up, the S9901 will be accessed only as needed to service the clock, enable (disable) interrupts, or read (write) data to the I/O ports. The I/O ports can be reconfigured by use of the $\overline{RST}_2$ command bit.

Figure 5 illustrates the use of an S9901 with an S9900. The S9904 is used to generate RST to reset the 9900 and the 9901 (connected to $\overline{RST}_1$). Figure 6 shows an S9980 system using the S9901. The reset function, load interrupt, and 4 maskable interrupts allowed in a 9980 are encoded as shown in Table 5. Connecting the system as shown ensures that the proper reset will be applied to the 9980.

Table 5. 9980 Interrupt Level Data

Interrupt Code (IC_0-IC_2)	Function	Vector Location (Memory Address In Hex)	Device Assignment	Interrupt Mask Values To Enable (ST_{12} through ST_{15})
1 1 0	Level 4	0 0 1 0	External Device	4 Through F
1 0 1	Level 3	0 0 0 C	External Device	3 Through F
1 0 0	Level 2	0 0 0 8	External Device	2 Through F
0 1 1	Level 1	0 0 0 4	External Device	1 Through F
0 0 1	Reset	0 0 0 0	Reset Stimulus	Don't Care
0 1 0	Load	3 F F C	Load Stimulus	Don't Care
0 0 0	Reset	0 0 0 0	Reset Stimulus	Don't Care
1 1 1	No-Op	—	—	Don't Care

Figure 5. S9900-S9901 Interface

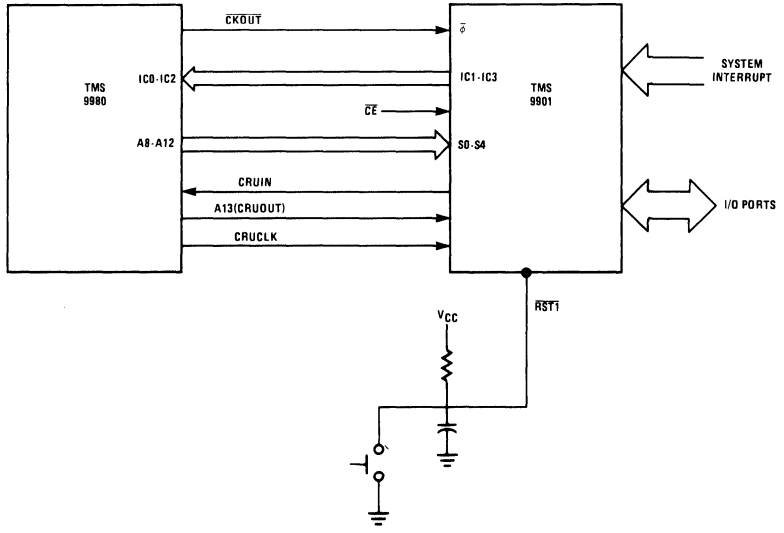
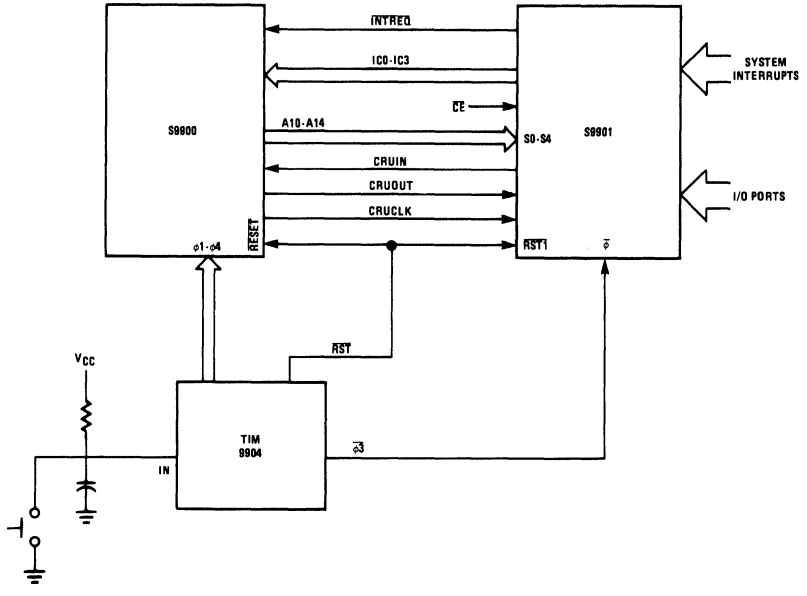


Figure 6. S9980-S9901 Interface



AMI

A Subsidiary of Gould Inc.

Advanced Product Description **S9902/S9902-4**

ASYNCHRONOUS COMMUNICATIONS CONTROLLER (ACC)

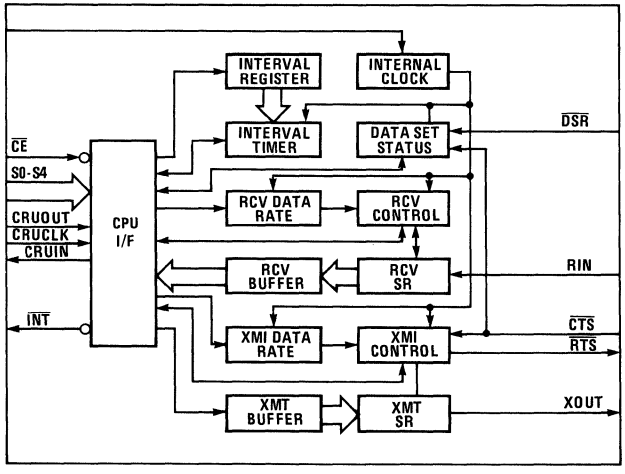
Features

- ☐ 5- to 8-Bit Character Length
- ☐ 1, 1½, or 2 Stop Bits
- ☐ Even, Odd, or No Parity
- ☐ Fully Programmable Data Rate Generation
- ☐ Interval Timer with Resolution from 64 to 16,320 μs
- ☐ Fully TTL Compatible, Including Single Power Supply

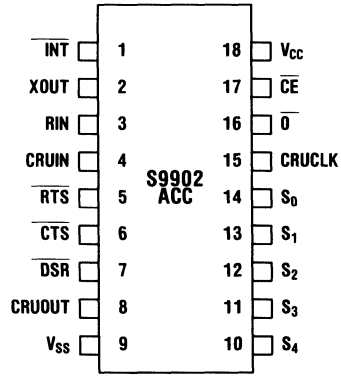
General Description

The S9902 Asynchronous Communication Controller (ACC) is a peripheral device for the S9900 family of microprocessors. The ACC provides an interface between the microprocessor and a serial asynchronous communication channel, performing the timing and data serialization and deserialization, thus facilitating the control of the asynchronous channel by the microprocessor.

Block Diagram



Pin Configuration



S9902 Electrical Specifications

Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply Voltage, V_{CC} ..... −0.3V to +10V
All Input and Output Voltages ..... −0.3V to +10V
Continuous Power Dissipation 0.7W
Operating Free-Air Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_{SS}		0		V
High-Level Input Voltage, V_{IH}	2.2	2.4	V_{CC}	V
Low-Level Input Voltage, V_{IL}		0.4	0.8	V
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics

Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_I	Input Current (Any Input)			±10	μA	$V_I = 0V$ to V_{CC}
V_{OH}	High Level Output Voltage	2.2 2.0	3.0 2.5		V	$I_{OH} = 100\mu A$ $I_{OH} = -400\mu A$
V_{OL}	Low Level Output Voltage		0.4	0.85	V	$I_{OL} = 3.2mA$
$I_{CC(AV)}$	Average Supply Current from V_{CC}		2.5	100	mA	$t_{C(0)} = 250ns$, $T_A = 25°C$
C_i C_o	Capacitance, Any Input Capacitance, Any Output		10 20		pF	f = 1MHz, All other pins at 0V

Timing Requirements

Over Full Range of Operating Conditions

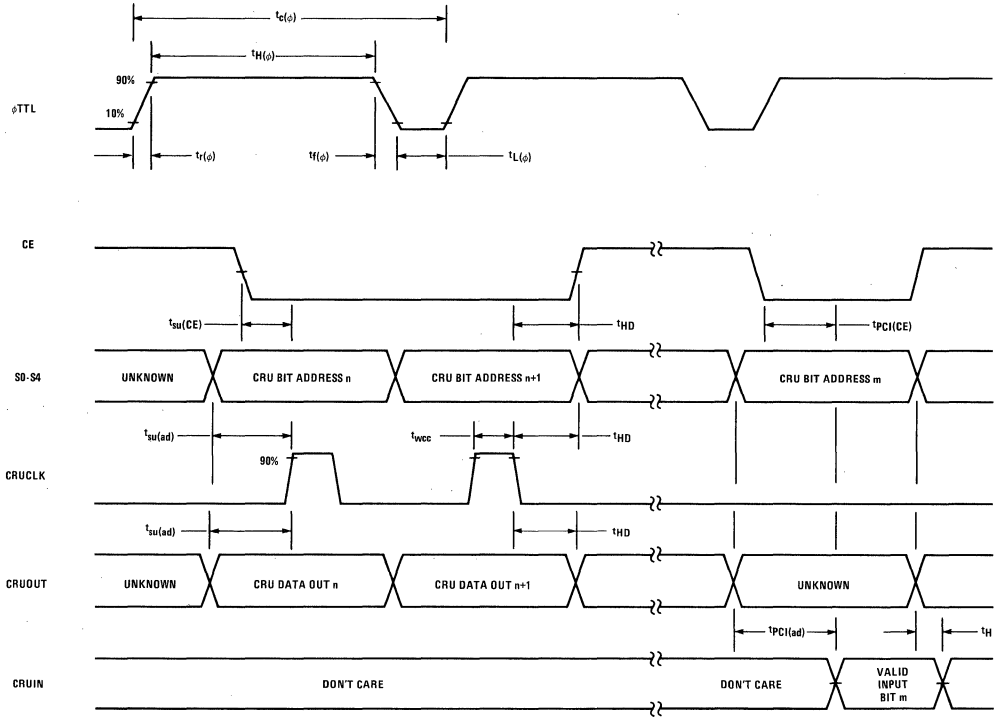
Symbol	Parameter	S9902			S9902-4			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{C(0)}$	Clock Cycle Time	300	333	2000	240	250	667	ns
$t_{r(0)}$	Clock Rise Time	5	10	12	8		40	ns
$t_{f(0)}$	Clock Fall Time	225	10	12	10		40	ns
$t_{H(0)}$	Clock Pulse Low Width (High Level)		225	240	180			ns
$t_{L(0)}$	Clock Pulse Width (Low Level)	45	45	55	40			ns
tsu(ad)	Setup Time for Address and CRU_{OUT} Before CRU_{CLK}	180	220		150	150		ns
$t_{su(CE)}$	Setup Time for CE Before CRU_{CLK}	100	185		110	110		ns
t_{HD}	Hold Time for Address, CE and CRU_{OUT} After CRU_{CLK}	60	90		50	50		ns
twcc	CRU_{CLK} Pulse Width	100	120		80			ns

Switching Characteristics

Over Full Range of Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{PCI(cd)}$	Propagation Delay, Address-to-Valid CRU_{IN}			400	ns	$C_L = 100pF$,
$t_{PCI(CE)}$	Propagation Delay, $\overline{CE}$-to-Valid CRU_{IN}			400	ns	$C_L = 100pF$
t_H	CRU_{IN} Hold Time After Address			20	ns	

Figure 3. Switching Characteristics



S9902 Pin Description

Table 1 defines the S9902 pin assignments and describes the function of each pin as shown on page 1.

Table 1.

Signature	Pin	I/O	Description
$\overline{INT}$	1	O	Interrupt—when active (low), the $\overline{INT}$ output indicates that at least one of the interrupt conditions has occurred.
X_{OUT}	2	O	Transmitter serial data output line—X_{OUT} remains inactive (high) when S9902 is not transmitting.
RIN	3	I	Receiver serial data input line—RCV—must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receiver circuitry.
CRU_{IN}	4	O	Serial data output pin from S9902 to CRU_{IN} input pin of the CPU.
$\overline{RTS}$	5	O	Request-to-send output from S9902 to modem. This output is enabled by the CPU and remains active (low) during transmission from the S9902.
$\overline{CTS}$	6	I	Clear-to-send input from modem to S9902. When active (low), it enables the transmitter section of S9902.
$\overline{DSR}$	7	I	Data set ready intput from modem to S9902. This input generates an interrupt when going On or Off.
CRU_{OUT}	8	I	Serial data input line to S9902 from CRU_{OUT} line of the CPU.
V_{SS}	9	I	Ground reference voltage.
S_4 (LSB)	10	I	
S_3	11	I	
S_2	12	I	
S_1	13	I	Address bus S_0-S_4 are the lines that are addressed by the CPU to select a particular S9902 function.
S_0	14	I	
CRU_{CLK}	15	I	CRU Clock. When active (high), S9902 from CRU_{OUT} line of the CPU.
ϕ	16	I	TTL Clock.
CE	17	I	Chip enable—when CE is inactive (high), the S9902 address decoding is inhibited which prevents execution of any S9902 command function. CRU_{IN} remains at high-impedance when $\overline{CE}$ is inactive (high).
V_{CC}	18	I	Supply voltage (+5V nominal).

Device Interface

The relationship of the ACC to other components in the system is shown in Figures 2 and 3. The ACC is connected to the asynchronous channel through level shifters which translate the TTL inputs and outputs to the appropriate levels (e.g., RS-232C, TTY current loop, etc.). The microprocessor transfers data to and from the ACC via the Communication Register Unit (CRU).

CPU Interface

The ACC interfaces to the CPU through the Communication Register Unit (CRU). The CRU interface consists of five address-select lines (S_0-S_4), chip enable (CE), and three CRU control lines (CRU_{IN}, CRU_{OUT}, and CRU_{CLK}). When $\overline{CE}$ becomes active (low), the five select lines address the CRU bit being accessed. When data is being transferred to the ACC from the CPU, CRU_{OUT} contains the valid datum which is strobed by CRU_{CLK}. When ACC data is being read, CRU_{IN} is the datum output by the ACC.

Figure 4. S9902 ACC in a S9900 System

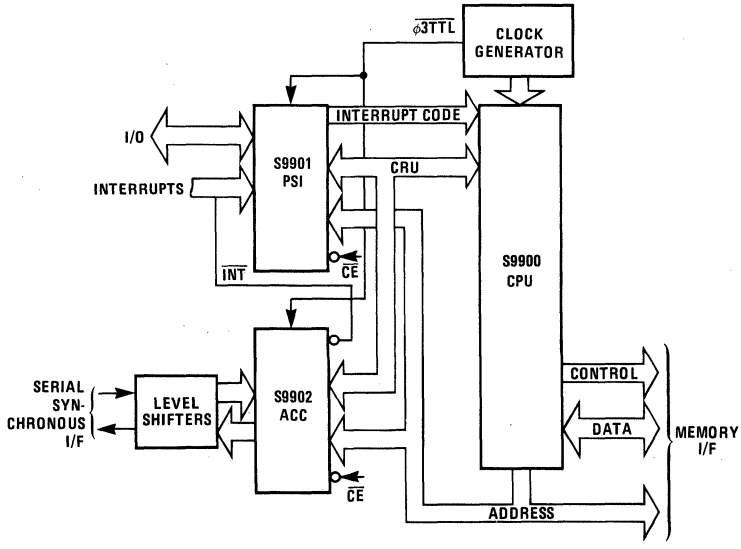
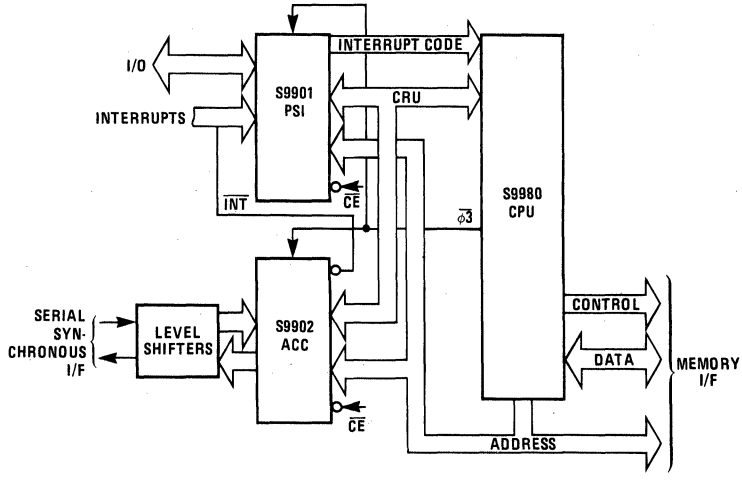


Figure 5. S9902 ACC in a S9980 System



Asynchronous Communication Channel Interface

The interface to the asynchronous communication channel consists of an output control line ($\overline{RTS}$), two input status lines ($\overline{DSR}$ and $\overline{CTS}$), and serial transmit (X_{OUT}) and receive (RIN) data lines. The request-to-send line ($\overline{RTS}$) is active (low) whenever the transmitter is activated. However, before data transmission begins, the clear-to-send ($\overline{CTS}$) input must be active. The data set ready ($\overline{DSR}$) input does not affect the receiver or transmitter. When $\overline{DSR}$ or $\overline{CTS}$ changes level, an interrupt is generated.

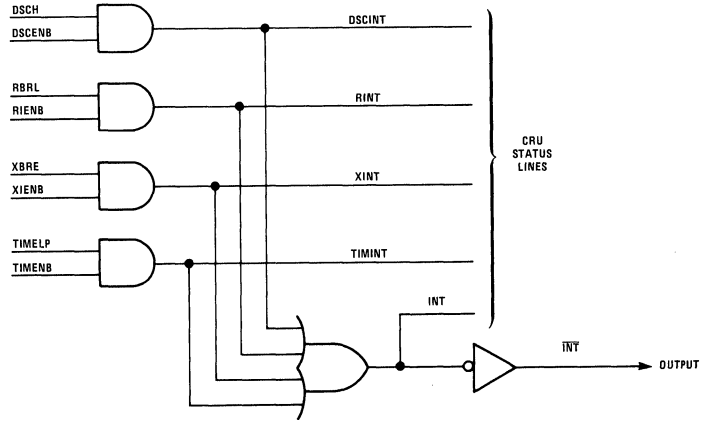
Interrupt Output

The interrupt output ($\overline{INT}$) is active (low) when any of the following conditions occurs and the corresponding interrupt has been enabled by the CPU:

(1) $\overline{DSR}$ or $\overline{CTS}$ changes levels (DSCH = 1);
(2) a character has been received and stored in the Receiver Buffer Register (RBRL = 1);
(3) the Transmit Buffer Register is empty (XBRE = 1); or
(4) the selected time interval has elapsed (TIMELP = 1).

The logical relationship of the interrupt output is shown below.

$\overline{INT}$ Output Generation



Clock Input

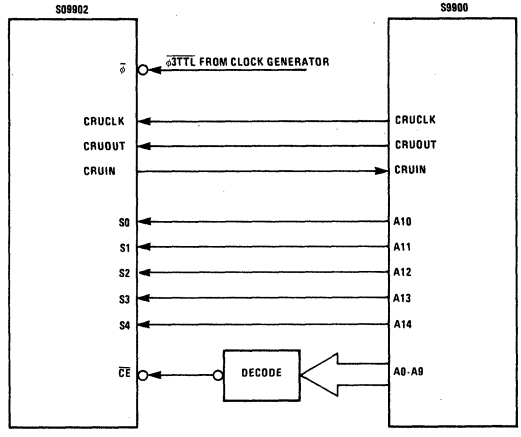
The clock input to the ACC ($\overline{\phi}$) is normally provided by the $\overline{\phi 3}$ output of the clock generator (9900 systems) or the S9980 (9980 systems). This clock input is used to generate the internal device clock, which provides the time base for the transmitter, receiver, and interval timer of the ACC.

Device Operation

Control and Data Output

Data and control information is transferred to the ACC using $\overline{CE}$, S_0-S_4, CRU_{OUT}, and CRU_{CLK}. The diagrams on page 7 show the connection of the ACC to the S9900 and S9980 CPUs. The high-order CPU address lines are used to decide the $\overline{CE}$ signal when the device is being selected. The low-order address lines are connected to the five address-select lines (S_0-S_4). Table 2 describes the output bit address assignments for the ACC.

Connection of the ACC to the S9900



Connection of the ACC to the S9980 CPU's

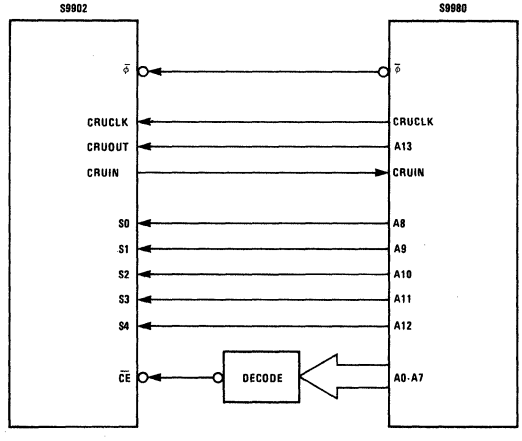


Table 2. S9902 ACC Output Bit Address Assignments

Address$_2$ S_0	S_1	S_2	S_3	S_4	Address$_{10}$	Name	Description
1	1	1	1	1	31	RESET	Reset Device
					30-22		Not used
1	0	1	0	1	21	DSCENB	Data Set Status Change Interrupt Enable
1	0	1	0	0	20	TIMENB	Timer Interrupt Enable
1	0	0	1	1	19	XBIENB	Transmitter Interrupt Enable
1	0	0	1	0	18	RIENB	Receiver Interrupt Enable
1	0	0	0	1	17	BRKON	Break On
1	0	0	0	0	16	RTSON	Request to Send On
0	1	1	1	1	15	TSTMD	Test Mode
0	1	1	1	0	14	LDCTRL	Load Control Register
0	1	1	0	1	13	LDIR	Load Interval Register
0	1	1	0	0	12	LRDR	Load Receiver Data Rate Register
0	1	0	1	1	11	LXDR	Load Transmit Data Rate Register
					10-0		Control, Interval, Receive Data Rate, Transmit Data Rate, and Transmit Buffer Registers

Bit 31 (RESET) — Writing a one or zero to Bit 31 causes the device to be reset, disabling all interrupts, initializing the transmitter and receiver, setting $\overline{RTS}$ inactive (high), setting all register load control flags (LDCTRL, LDIR, LRDR, and LXDR) to a logic one level, and resetting the BREAK flag. No other input or output operations should be performed for 11$\emptyset$ clock cycles after issuing the RESET command.

Bit 30-Bit 22 — Not used.

Bit 21 (DSCENB) — Data Set Change Interrupt Enable. Writing a one to Bit 21 causes the $\overline{INT}$ output to be active (low) whenever DSCH (Data Set Status Change) is a logic one. Writing a zero to Bit 21 causes DSCH interrupts to be disabled. Writing either a one or zero to Bit 21 causes DSCH to be reset.

Bit 20 (TIMENB) — Timer Interrupt Enable. Writing a one to Bit 20 causes the $\overline{INT}$ output to be active whenever TIMELP (Timer Elapsed) is a logic one. Writing a zero to Bit 20 causes TIMELP interrupts to be disabled. Writing either a one or zero to Bit 20 causes TIMELP and TIMERR (Timer Error) to be reset.

Bit 19 (XBIENB) — Transmit Buffer Interrupt Enable. Writing a one to Bit 19 causes the $\overline{INT}$ output to be active whenever XBRE (Transmit Buffer Register Empty) is a logic one. Writing a zero to Bit 19 causes XBRE interrupts to be disabled. The state of XBRE is not affected by writing to Bit 19.

Bit 18 (RIENB) — Receiver Interrupt Enable. Writing a one to Bit 18 causes the $\overline{INT}$ output to be active whenever RBRL (Receiver Buffer Register Loaded) is a logic one. Writing a zero to Bit 18 disables RBRL interrupts. Writing either a one or zero to Bit 18 causes RBRL to be reset.

Bit 17 (BRKON) — Break On. Writing a one to Bit 17 causes the XOUT (Transmitter Serial Data Output) to go to a logic zero whenever the transmitter is active and the Transmit Buffer Register (XBR) and the Transmit Shift Register (XSR) are empty. While BRKON is set, loading of characters into the XBR is inhibited. Writing a zero to Bit 17 causes BRKON to be reset and the transmitter to resume normal operation.

Bit 16 (RTSON) — Request-to-Send On. Writing a one to Bit 16 causes the $\overline{RTS}$ output to be active (low). Writing a zero to Bit 16 causes $\overline{RTS}$ to go to a logic one after the XSR and XBR are empty, and BRKON is reset. Thus, the $\overline{RTS}$ output does not become inactive (high) until after character transmission has been completed.

Bit 15 (TSTMD) — Test Mode. Writing a one to Bit 15 causes $\overline{RTS}$ to be internally connected to $\overline{CTS}$, XOUT to be internally connected to RIN, $\overline{DSR}$ to be internally held low, and the Interval Timer to operate at 32 times its normal rate. Writing a zero to Bit 15 re-enables normal device operation.

Bit 14-11 — Register Load Control Flags. Output Bits 14-11 control which of the five registers will be loaded by writing to Bits 10-0. The flags are prioritized as shown in Table 3.

Table 3. S9902 ACC Register Load Selection

Register Load Control Flag Status				Register Enabled
LDCTRL	LDIR	LDR	LXDR	
1	X	X	X	Control Register
0	1	X	X	Interval Register
0	0	1	X	Receive Data Rate Register
0	0	X	1	Transmit Data Rate Register
0	0	0	0	Transmit Buffer Register

Bit 14 (LDCTRL) — Load Control Register. Writing a one to Bit 1 causes LDCTRL to be set to a logic one. When LDCTRL = 1, any data written to bits 0-7 are directed to the Control Register. Note that LDCTRL is also set to a logic one when a one or zero is written to Bit 31 (RESET). Writing a zero to Bit 14 causes LDCTRL to be reset to a logic zero, disabling loading of the Control Register. LDCTRL is also automatically reset to a logic zero when a datum is written to Bit 7 of the Control Register which normally occurs as the last bit written when loading the Control Register with a LDCR instruction.

Bit 13 (LDIR) — Load Interval Register, Writing a one to Bit 13 causes LDIR to be set to a logic one. When LDIR = 1 and LDCTRL = 0, any data written to Bits 0-7 are directed to the Interval Register. Note that LDIR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Interval Register loading is not enabled until LDCTRL is set to a logic zero. Writing a zero to Bit 13 causes LDIR to be reset to logic zero, disabling loading of the Internal Register. LDIR is also automatically reset to logic zero when a datum is written to Bit 7 of the Interval Register, which normally occurs as the last bit written when loading the Interval Register with a LDCR instruction.

Bit 12 (LRDR) — Load Receive Data Rate Register. Writing a one to Bit 12 causes LRDR to be set to a logic one. When LRDR = 1, LDIR = 0, and LDCTRL = 0, any data written to Bits 0-10 are directed to the Receive Data Rate Register. Note that LRDR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Receive Data Rate Register loading is not enabled until LDCTRL and LDIR have been set to a logic zero. Writing a zero to Bit 12 causes LRDR to be reset to a logic zero, disabling loading of the Receive Data Rate Register. LRDR is also automatically reset to logic zero when a datum is written to Bit 10 of the Receive Data Rate Register, which normally occurs as the last bit written when loading the Receive Data Rate Register with a LDCR instruction.

Bit 11 (LXDR) — Load Transmit Data Rate Register. Writing a one to Bit 11 causes LXDR to be set to a logic one. When LXDR = 1, LDIR = 0, and LDCTRL = 0, any data written to Bits 0-10 are directed to the Transmit Data Rate Register. Note that loading of both the Receive and Transmit Data Rate Registers is enabled when LDCTRL = 0, LDIR = 0, LRDR = 1, and LXDR = 1; thus these two registers may be loaded simultaneously when data are received and transmitted at the same rate. LXDR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Transmit Data Rate Register loading is not enabled until LDCTRL and LDIR have been reset to logic zero. Writing a zero to Bit 11 causes LXDR to be reset to logic zero, disabling loading of the Transmit Data Rate Register. Since Bit 11 is the next bit addressed after loading the Transmit Data Rate Register, the register may be loaded and the LXDR flag reset with a single LDCR instruction where 12 bits (Bits 0-11) are written, with a zero written to Bit 11.

Control Register

The Control Register is loaded to select character length, device clock operation, parity, and the number of stop bits for the transmitter. Table 4 shows the bit address assignments for the Control Register.

Table 4. Control Register Bit Address Assignments

$Address_{10}$	Name	Description
7	SBS1	← Stop Bit Select
6	SBS2	
5	PENB	Parity Enable
4	PODD	Odd Parity Select
3	CLK4M	0 Input Divide Select
2	—	Not Used
1	RCL1	← Character Length Select
0	RCL0	

7	6	5	4	3	2	1	0
SBS1	SBS2	PENB	PODD	CLK4M	NOT USED	RCL1	RCL0
MSB							LSB

Bits 7 and 6 (SBS1 and SBS2) — Stop Bit Selection. The number of stop bits to be appended to each transmitter character is selected by Bits 7 and 6 of the Control Register as shown below. The receiver only tests for a single stop bit, regardless of the status of Bits 7 and 6.

Stop Bit Selection

SBS1 Bit 7	SBS2 Bit 6	Number of Transmitted Stop Bits
0	0	1½
0	1	2
1	0	1
1	1	1

Bits 5 and 4 (PENB and PODD) — Parity Selection. The type of parity to be generated for transmission and detected for reception is selected by Bits 5 and 4 of the Control Register as shown below. When parity is enabled (PENB = 1), the parity bit is transmitted and received in addition to the number of bits selected for the character length. Odd parity is such that the total number of ones in the character and parity bit, exclusive of stop bit(s), will be odd. For even parity, the total number of ones will be even.

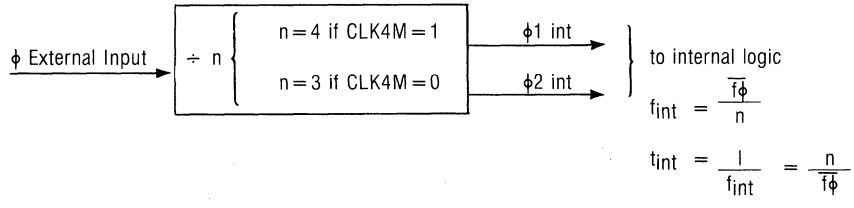
Parity Selection

PENB Bit 5	PODD Bit 4	PARITY
0	0	None
0	1	None
1	0	Even
1	1	Odd

Bit 3 (CLK4M) — ϕ Input Divide Select. The ϕ input to the S9902 ACC is used to generate internal dynamic logic clocking and to establish the time base for the Interval Timer, Transmitter and Receiver. The ϕ input is internally divided by either 3 or 4 to generate the two-phase internal clocks required for MOS logic, and to establish

the basic internal operating frequency (f_{int}) and internal clock period (t_{int}). When Bit 3 of the Control Register is set to a logic one (CLK4M = 1), ϕ is internally divided by 4, and when CLK4M = 0, ϕ is divided by 3. For example, when $f\phi = 3MHz$, as in a standard 3MHz S9900 system, and CLK4M = 0, ϕ is internally divided by 3 to generate an internal clock period t_{int} of 1μs. The figure below shows the operation of the internal clock divider circuitry. The internal clock frequency should be no greater than 1. 1MHz; thus, when $f\phi > 3.3MHz$, CLK4M should be set to a logic one.

Internal Clock Divider Circuitry



Bits 1 and 0 (RCL_1 and RCL_0) — Character Length Select. The number of data bits in each transmitted and received character is determined by Bits 1 and 0 of the Control Register as shown below.

Character Length Selection

RCL1 Bit 1	RCL0 Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Interval Register

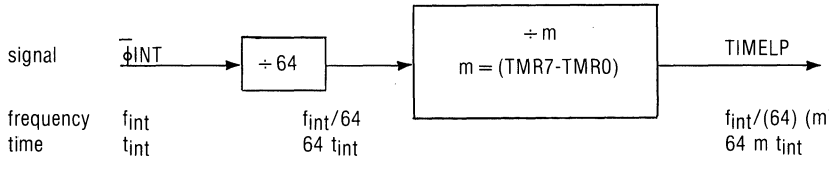
The Interval Register is enabled for loading whenever LDCTRL = 0 and LDIR = 1. The Interval Register is used for selecting the rate at which interrupts are generated by the Interval Timer of the ACC. The figure below shows the bit address assignments for the Interval Register when enabled for loading.

Interval Register Bit Address Assignments

7	6	5	4	3	2	1	0
TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
MSB							LSB

The figure below illustrates the establishment of the interval for the Interval Timer. As an example, if the Interval Register is loaded with a value of 80_{16} (128_{10}) the interval at which Timer Interrupts are generated is $t_{ITVL} = t_{int} \bullet 64 \circ M = (1\mu s) (\bullet 64) (\bullet 128) = 8.192$ ms. when $t_{int} = 1\mu s$.

Time Internal Selection



Receive Data Rate Register

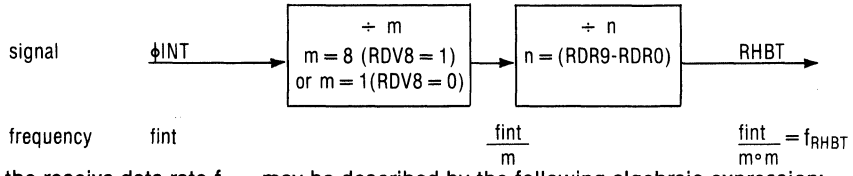
The Receive Data Rate Register is enabled for loading whenever LDCTRL = 0, LDIR = 0, and LRDR = 1. The Receive Data Rate Register is used for selecting the bit rate at which data is received. The diagram shows the bit address assignments for the Receive Data Rate Register when enabled for loading.

Receive Data Rate Register Bit Address Assignments

10	9	8	7	6	5	4	3	2	1	0
RDV8	RDR9	RDR8	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
MSB										LSB

The following diagram describes the manner in which the receive data rate is established. Basically, two programmable counters are used to determine the interval for one-half the bit period of receive data. The first counter either divides the internal system clock frequency (f_{int}) by either 8 (RDV8 = 1) or 1 (RDV8 = 0). The second counter has ten stages and may be programmed to divide its input signal by any value from 1 (RDR9-RDR0 = 0000000001) to 1023 (RDR8-RDR0 = 1111111111). The frequency of the output of the second counter (f_{RHBT}) is double the receive-data rate. Register is loaded with a value of 11000111000, RDV8 = 1, and RDR9-RDR0 = 1000111000 = 238_{16} = 568 10. Thus, for f_{int} = 1MHz, the receive-data rate = $1 \times 10^6 \div 8 \div 568 \div 2$ = 110.04 bits per second.

Receive Data Rate Selection



Quantitatively, the receive data rate f_{RCV} may be described by the following algebraic expression:

$$f_{RCV} = \frac{f_{RHBT}}{2} = \frac{f_{int}}{2mn} = \frac{f_{int}}{(2)\ (8^{RDV8})\ (RDR9\text{-}RDR0)}$$

Transmit Data Rate Register

The Transmit Data Rate Register is enabled for loading whenever LDCTRL = 0, LDIR = 0, and LXDR = 1. The Transmit Data Rate Register is used for selecting the data rate for the transmitter. The figure below shows the bit address assignments for the Transmit Data Rate Register.

10	9	8	7	6	5	4	3	2	1	0
XDV8	XDR9	XDR8	XDR7	XDR6	XDR5	XDR4	XDR3	XDR2	XDR1	XDR0
MSB										LSB

Selection of transmit data rate is accomplished with the Transmit Data Rate Register in the same way that the receive data rate is selected when the Receive Data Rate Register. The algebraic expression for the Transmit Data Rate f_{XMT} is:

$$f_{XMT} = \frac{f_{XHBT}}{2} = \frac{f_{int}}{(2)\ (8^{XDV8})\ (XDR9\text{-}XDR0)}$$

For example, if the Transmit Data Rate Register is loaded with a value of 00110100001, XDV8 = 0, and XDR9-XDR0 = $1A1_{16}$ = 417, the transmit data rate = $1 \times 10^6 \div 2 \div 1 \div 417$ = 1199.04 bits per second.

Transmit Buffer Register

The Transmit Buffer Register is enabled for loading when LDCTRL = 0, LDIR = 0, LRDR = 0, LXDR = 0, and BRKON = 0. The Transmit Buffer Register is used for storage of the next character to be transmitted. When the transmitter is active, the contents of the Transmit Buffer Register are transferred to the Transmit Shift Register each time the previous character has been completely transmitted. The bit address assignments for the Transmit Buffer Register are shown below:

Transmit Buffer Register Bit Address Assignments

7	6	5	4	3	2	1	0
XBR7	XBR6	XBR5	XBR4	XBR3	XBR2	XBR1	XBR0
MSB							LSB

All 8 bits should be transferred into the register, regardless of the selected character length. The extraneous high-order bits will be ignored for transmission purposes; however, loading of bit 7 is internally detected to cause the Transmit Buffer Register Empty (XBRE) status flag to be reset.

Status and Data Input

Status and data information is read from the ACC using $\overline{CE}$, S_0-S_4, and CRU_{IN}. The following figure illustrates the relationship of the signals used to access data from the ACC. Table 6 describes the input bit address assignments for the ACC.

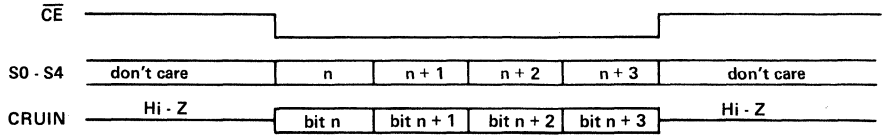


Table 5. CRU Output Bit Address Assignments

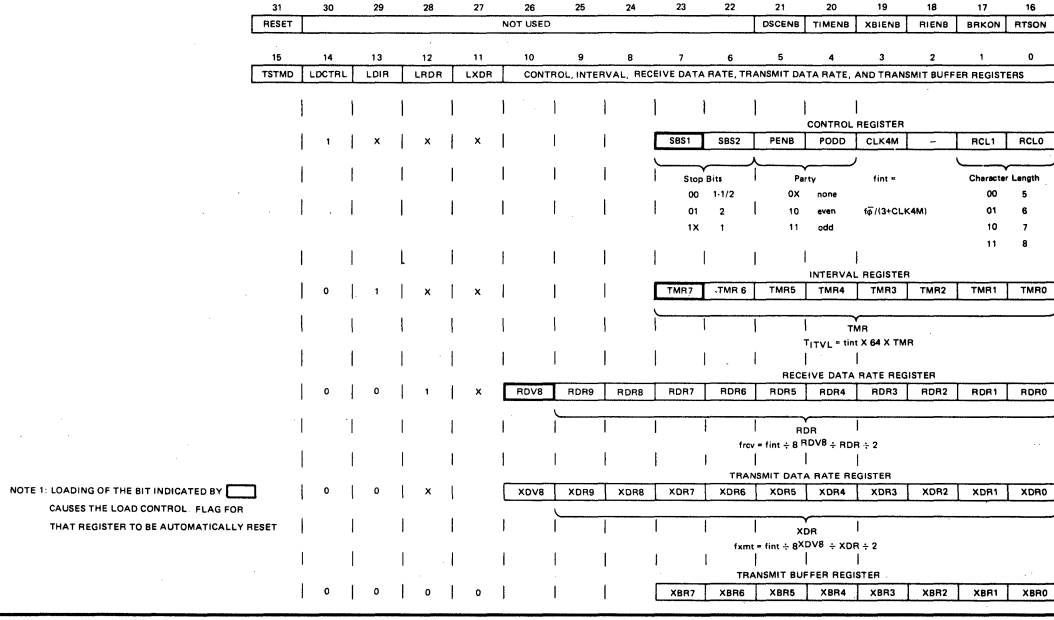


Table 6. S9902 ACC Input Bit Address Assignments

Address$_9$					Address$_{10}$	Name	Description
S_0	S_1	S_2	S_3	S_4			
1	1	1	1	1	31	INT	Interrupt
1	1	1	1	0	30	FLAG	Register Load Control Flag Set
1	1	1	0	1	29	DSCH	Data Set Status Change
1	1	1	0	0	28	CTS	Clear to Send
1	1	0	1	1	27	DSR	Data Set Ready
1	1	0	1	0	26	RTS	Request to Send
1	1	0	0	1	25	TIMELP	Timer Elapsed
1	1	0	0	0	24	TIMERR	Timer Error
1	0	1	1	1	23	XSRE	Transmit Shift Register Empty
1	0	1	1	0	22	XBRE	Transmit Buffer Register Empty
1	0	1	0	1	21	RBRL	Receive Buffer Register Loaded
1	0	1	0	0	20	DSCINT	Data Set Status Charge Interrupt (DSCH-DSCENB)
1	0	0	1	1	19	TIMINT	Timer Interrupt (TIMELP-TIMENB)
1	0	0	1	0	18	—	Not used (always = 0)
1	0	0	0	1	17	XBINT	Transmitter Interrupt (XBRE-XBIENB)
1	0	0	0	0	16	RBINT	Receiver Interrupt (RBRL-RIENB)
0	1	1	1	1	15	RIN	Receive Input
0	1	1	1	0	14	RSBD	Receive Start Bit Detect
0	1	1	0	1	13	RFBD	Receive Full Bit Detect
0	1	1	0	0	12	RFER	Receive Framing Error
0	1	0	1	1	11	ROVER	Receive Overrun Error
0	1	0	1	0	10	RPER	Receive Parity Error
0	1	0	0	1	9	RCVERR	Receive Error
0	1	0	0	0	8	—	Not used (always = 0)
					7-0	RBR7-RBR0	Receive Buffer Register (Received Data)

Bit 31 (INT) — INT = DSCINT + TIMINT + XBINT + RBINT. The interrupt output ($\overline{INT}$) is active when this status signal is a logic 1.

Bit 30 (FLAG) — FLAG = LDCTRL + LRDR + LXDR = BRKON. When any of the register load control flags or BRKON is set, FLAG = 1.

Bit 29 (DSCH) — Data Set Status Change Enable. DSCH is set when the $\overline{DSR}$ or $\overline{CTS}$ input changes state. To ensure recognition of the state change, $\overline{DSR}$ or $\overline{CTS}$ must remain stable in its new state for a minimum of two internal clock cycles. DSCH is reset by an output to bit 21 (DSCENB).

Bit 28 (CTS) — Clear to Send. The CTS signal indicates the inverted status of the $\overline{CTS}$ device input.

Bit 27 (DSR) — Data Set Ready. The DSR signal indicates the inverted status of the $\overline{DSR}$ device input.

Bit 26 (RTS) — Request to Send. The RTS signal indicates the inverted status of the $\overline{RTS}$ device output.

Bit 25 (TIMELP) — Timer Elapsed. TIMELP is set each time the Interval Timer decrements to 0. TIMELP is reset by an output to bit 20 (TIMENB).

Bit 24 (TIMERR)	—	Timer Error. TIMERR is set whenever the Interval timer decrements to 0 and TIMELP is already set, indicating that the occurrence of TIMELP was not recognized and cleared by the CPU before subsequent intervals elapsed. TIMERR is reset by an output to bit 20 (TIMENB).
Bit 23 (XSRE)	—	Transmit Shift Register Empty. When XSRE = 1, no data is currently being transmitted and the XOUT output is at logic 1 unless BRKON is set. When XSRE = 0, transmission of data is in progress.
Bit 22 (XBRE)	—	Transmit Buffer Register Empty. When XBRE = 1, the transmit buffer register does not contain the next character to be transmitted. XBRE is set each time the contents of the transmit buffer register are transferred to the transmit shift register. XBRE is reset by an output to bit 7 of the transmit buffer register (XBR7), indicating that a character has been loaded.
Bit 21 (RBRL)	—	Receive Buffer Register Loaded. RBRL is set when a complete character has been assembled in the receive shift register and the character is transferred to the receive buffer register. RBRL is reset by an output to bit 18 (RIENB).
Bit 20 (DSCINT)	—	Data Set Status Change Interrupt. DSCINT = DSCH (input bit 29) • DSCENB (output bit 21). DSCINT indicates the presence of an enabled interrupt caused by the changing of state of $\overline{\text{DRS}}$ or $\overline{\text{CTS}}$.
Bit 19 (TIMINT)	—	Timer Interrupt. TIMINT = TIMELP (input bit 25) • TIMENB (output bit 20). TIMINT indicates the presence of an enabled interrupt caused by the interval timer.
Bit 17 (XBINT)	—	Transmitter Interrupt. XBINT = XBRE (input bit 22) • XBIENB (output bit 19). XBINT indicates the presence of an enabled interrupt caused by the transmitter.
Bit 16 (RBINT)	—	Receiver Interrupt. RBINT = RBRL (input bit 21 • RIENB (output bit 18). RBINT indicates the presence of an enabled interrupt caused by the receiver.
Bit 15 (RIN)	—	Receive Input. RIN indicates the status of the RIN input to the device.
Bit 14 (RSBD)	—	Receive Start Bit Detect. RSBD is set one-half bit time after the 1-to-0 transition of RIN indicating the start bit of a character. If RIN is not still 0 at this point in time, RSBD is reset. Otherwise, RSBD remains true until the complete character has been received. This bit is normally used for testing purposes.
Bit 13 (RFBD)	—	Receive Full Bit Detect. RFBD is set one bit time after RSBD is set to indicate the sample point for the first data bit of the received character. RSBD is reset when the character has been completely received. This bit is normally used for testing purposes.
Bit 12 (RFER)	—	Receive Framing Error. RFER is set when a character is received in which the stop bit, which should be a logic 1, is a logic 0. RFER should only be read when RBRL (input bit 21) is a 1. RFER is reset when a character with a correct stop bit is received.
Bit 11 (ROVER)	—	Receive Overrun Error. ROVER is set when a new character is received before the RBRL flag (input bit 21) is reset, indicating that the CPU failed to read the previous character and reset RBRL before the present character is completely received. ROVER is reset when a character is received and RBRL is 0 when the character is transferred to the receive buffer register.
Bit 10 (RPER)	—	Receive Parity Error. RPER is set when a character is received in which the parity is incorrect. RPER is reset when a character with correct parity is received.
Bit 9 (RCVERR)	—	Receive Error. RCVERR = RFER + ROVER + RPER. RCVERR indicates the presence of an error in the most recently received character.
Bit 7-Bit 0 (RBR7-RBR0	—	Receive Buffer Register. The receive buffer register contains the most recently received character. For character lengths of fewer than 8 bits the character is right justified, with unused most significant bit(s) all zero(es). The presence of valid data in the receive buffer register is indicated when RBRL is a logic 1.

Transmitter Operation

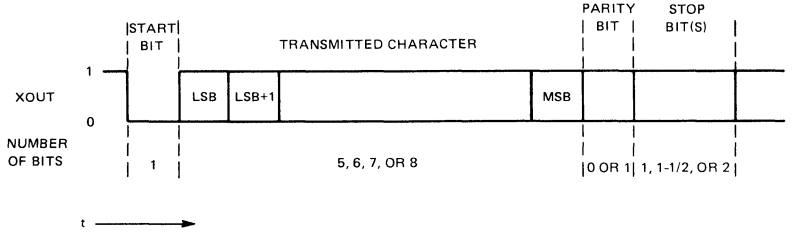
Transmitter Initialization

The operation of the transmitter is described in Figure 7. The transmitter is initialized by issuing the RESET command (output to bit 31), which causes the internal signals XSRE and XBRE to be set, and BRKON to be reset. Device outputs $\overline{RTS}$ and XOUT are set, placing the transmitter in its idle state. When RTSON is set by the CPU, the $\overline{RTS}$ output becomes active and the transmitter becomes active when $\overline{CTS}$ goes low.

Data Transmission

If the Transmit Buffer Register contains a character, transmission begins. The contents of the Transmit Buffer Register are transferred to the Transmit Shift Register, causing XSRE to be reset and XBRE to be set. The first bit transmitted (start bit) is always a logic 0. Subsequently, the character is shifted out, LSB first. Only the number of bits specified by RCL_1 and RCL_0 (character length select) of the Control Register are shifted. If parity is enabled, the correct parity bit is next transmitted. Finally the stop bit(s) selected by SBS_1 and SBS_0 of the Control Register are transmitted. Stop bits are always logic one. XSRE is set to indicate that no transmission is in progress, and the transmitter again tests XBRE to determine if the CPU has yet loaded the next character. The waveform for a transmitted character is shown below.

Transmitted Character Waveform



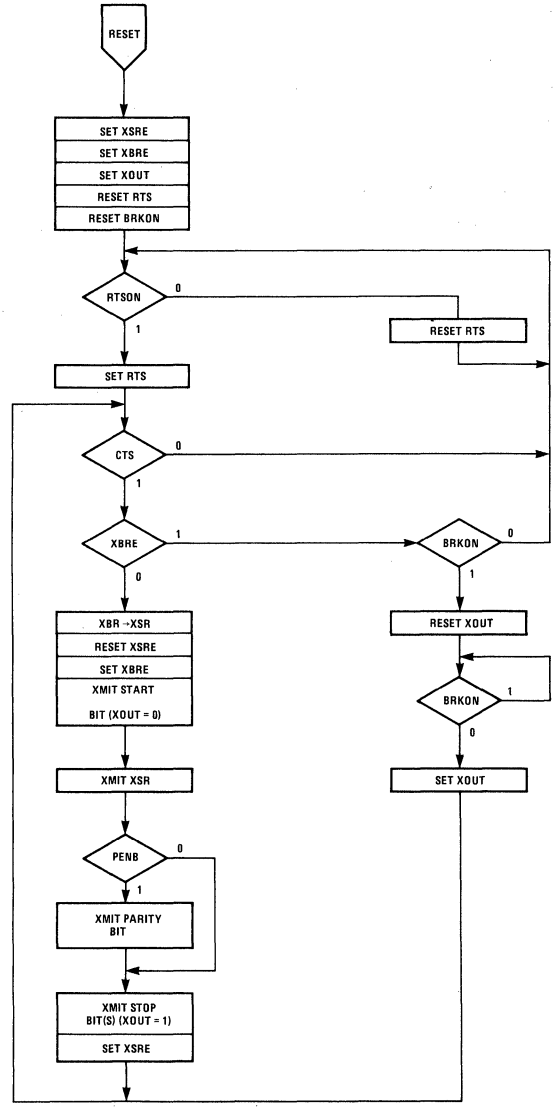
BREAK Transmission

The BREAK message is transmitted only if XBRE = 1, $\overline{CTS}$ = 9, and BRKON = 1. After transmission of the BREAK message begins, loading of the Transmit Buffer Register is inhibited and XOUT is reset. When BRKON is reset by the CPU, XOUT is set and normal operation continues. It is important to note that characters loaded into the Transmit Buffer Register are transmitted prior to the BREAK message regardless of whether the character has been loaded into the Transmit Shift Register before BRKON is set. Any character to be transmitted subsequent to transmission of the BREAK message may not be loaded into the Transmit Buffer Register until after BRKON is reset.

Transmission Termination

Whenever XSRE = 1 and BRKON = 0, the transmitter is idle, with XOUT set to one. If RTSON is reset at this time, the $\overline{RTS}$ device output will go inactive, disabling further data transmission until RTSON is again set. $\overline{RTS}$ will not go inactive, however, until any characters loaded into the Transmit Buffer Register prior to resetting RTSON are transmitted and BRKON = 0.

S9902 Transmitter Operation

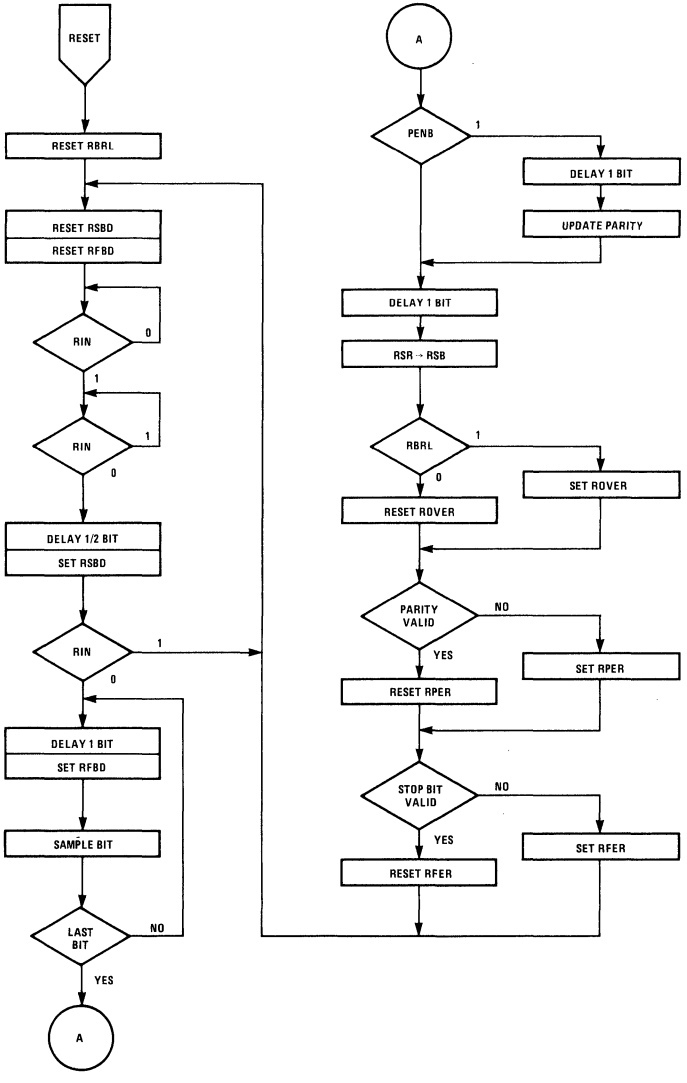


Receiver Operation

Receiver Initialization

Operation of the S9902 receiver is described in Figure 8. The receiver is initialized any time the CPU issues the RESET command. The RBRL flag is reset to indicate that no character is currently in the Receive Buffer Register, and the RSBD and RFBD flags are reset. The receiver remains in the inactive state until a 1 to 0 transition is detected on the RIN device input.

S9902 Receiver Operation



Start Bit Detection

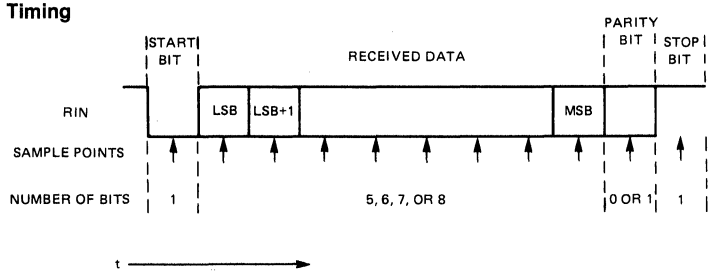
The receiver delays one-half bit time and again samples RIN to ensure that a valid start bit has been detected. If RIN = 0 after the half-bit delay, RSBD is set and data reception begins. If RIN = 1, no data reception occurs.

Data Reception

In addition to verifying the valid start bit, the half-bit delay after the 1-to-0 transition also establishes the sample point for all subsequent data bits in this character. Theoretically, the sample point is in the center of each bit cell, thus maximizing the limits of acceptable distortion of data cells. After the first full bit delay, the least significant data bit is received and RFBD is set. The receiver continues to delay one-bit intervals and sample RIN until the selected number of bits is received. If parity is enabled, one additional bit is read for parity. After an additional bit delay, the received character is transferred to the Receive Buffer Register, RBRL is set, ROVER and RPER are loaded with appropriate values, and RIN is tested for a valid stop bit. If RIN = 1, the stop bit is valid. RFER, RSBD, and RFBD are reset and the receiver waits for the next start bit to begin reception of the next character.

If RIN = 0 when the stop is sampled, RFER is set to indicate the occurrence of a framing error. RSBD and RFBD are reset but sampling for the start bit of the next character does not begin until RIN = 1.

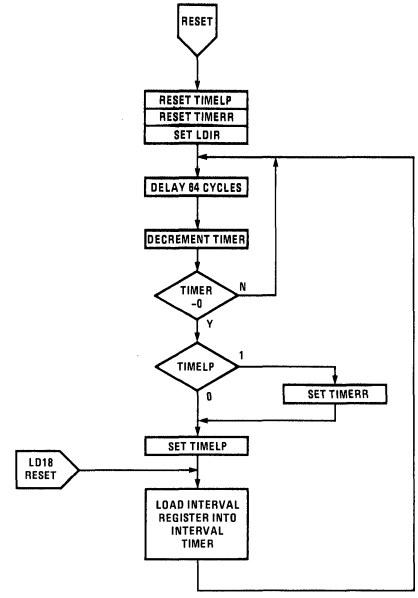
Character Reception Timing



Interval Timer Operation

A flowchart of the operation of the Interval Timer is shown in Figure 9. Execution of the RESET command by the CPU causes TIMELP and TIMERR to be reset and LDIR to be set. Resetting LDIR causes the contents of the Interval Register to be loaded into the Interval Timer, thus beginning the selected time interval. The timer is decremented every 64 internal clock cycles (every 2 internal clock cycles when in Test Mode) until it reaches zero, at which time the Interval Timer is reloaded by the Interval Register and TIMELP is set. If TIMELP was already set, TIMERR is set to indicate that TIMELP was not cleared by the CPU before the next time period elapsed. Each time LDIR is reset the contents of the Interval Register are loaded into the Interval Timer, thus restarting the time.

Interval Timer Operation



Device Application

This section describes the software interface between the CPU and the S9902 ACC and discusses some of the design considerations in the use of this device in asynchronous communications applications.

Device Initialization

The ACC is initialized by the CPU issuing the RESET command, followed by loading the Control, Interval, Receive Data Rate, and Transmit Data Rate registers. Assume that the value to be loaded into the CRU Base Register (register 12) in order to point to bit 0 is 0040_{16}. In this application, characters will have 7 bits of data plus even parity and one stop bit. The 0 input to the ACC is a 3MHz signal. The ACC will divide this signal frequency by 3 to generate an internal clock frequency of 1MHz. An interrupt will be generated by the Interval Timer every 1.6 milliseconds when timer interrupts are enabled. The transmitter will operate at a data rate of 300 bits per second and the receiver will operate at 1200 bits per second. Had it been desired that both the transmitter and receiver operate at 300 bits per second, the "LDCR @RDR,11" instruction would have been deleted, and the "LDCR @XDR,12" instruction would have caused both data rate registers to be loaded and LRDR and LXDR to have been reset.

Initialization Program

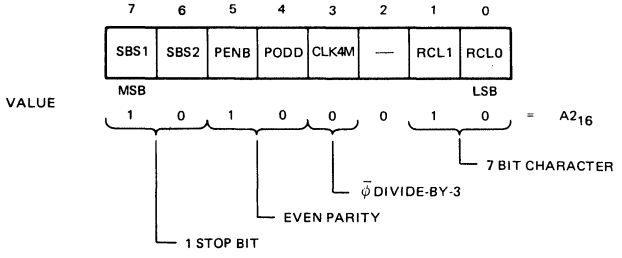
The initialization program for the configuration previously described is as shown below. The RESET command disables all interrupts, initializes all controllers, sets the four register load control flags (LDCTRL, LDIR, LRDR, and LXDR). Loading the last bits of each of the registers causes the load control flag to be automatically reset.

```
        LI      R12,>40     INITIALIZE CRU BASE
        SBO     31          RESET COMMAND
        LDCR    @CNTRL, 8   LOAD CONTROL AND RESET LDCTRL
        LDCR    @INTVL, 8   LOAD INTERVAL AND RESET LDIR
        LDCR    @RDR, 11    LOAD RDR AND RESET LRDR
        LDCR    @XDR, 12    LOAD XDR AND RESET LXDR
          •
          •
          •
CNTRL   BYTE    >A2
INTVL   BYTE    1600/64
RDR     DATA    >1A1
XDR     DATA    >4DO
```

The RESET command initializes all subcontrollers, disables interrupts, and sets LDCTRL, LDIR, LRDR, and LXDR, enabling loading of the control register.

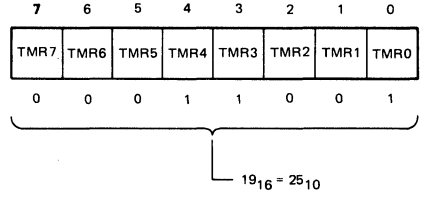
Control Register

The options described previously are selected by loading the value shown below.



Interval Register

The interval register is to be set up to generate an interrupt every 1.6 milliseconds. The value loaded into the interval register specifies the number of 64 microsecond increments in the total interval.



25 X 64 MICROSECONDS = 1.6 MILLISECONDS

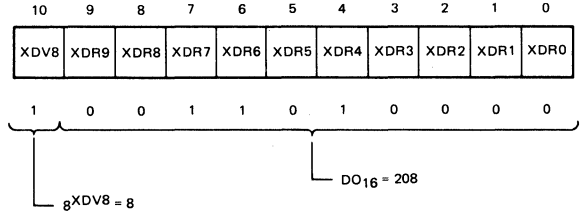
Receive Data Rate Register

The data rate for the receiver is to be 1200 bits per second. The value to be loaded into the Receive Data Rate Register is as shown:

$10^6 \div 1 \div 417 \div 2 = 1199.04$ BITS PER SECOND

Transmit Data Rate Register

The data rate for the transmitter is to be 300 bits per second. The value to be loaded into the Transmit Data Rate Register is:



$1 \times 10^6 \div 8 \div 208 \div 2 = 300.48$ BITS PER SECOND

Data Transmission

The subroutine shown below demonstrates a simple loop for the transmitting of a block of data.

```
        LI      R0, LISTAD      INITIALIZE LIST POINTER
        LI      R1, COUNT       INITIALIZE BLOCK COUNT
        LI      R12, CRUBAS     INITIALIZE CRU BASE
        SBO     16              TURN OFF TRANSMITTER
XMTLP   TB      22              WAIT FOR XBRE = 1
        JNE     XMTLP
        LDCR    *RO + ,8        LOAD CHARACTER INCREMENT POINTER RESET XBRE
        DEC     R1              DECREMENT COUNT
        JNE     XMTLP           LOOP IF NOT COMPLETE
        SBZ     16              TURN OFF TRANSMITTER
```

After initializing the list pointer, block count, and CRU base address, RTSON is set to cause the transmitter and the RTS output to become active. Data transmission does not begin, however, until the CTS input becomes active. After the final character is loaded into the transmit buffer register. RTSON is reset. The transmitter and the RTS output do not become inactive until the final character has been completely transmitted.

Data Reception

The software shown below will cause a block of data to be received and stored in memory.

```
CARRET  BYTE    >OD
RCVBLK  LI      R2, RCVLST      INITIALIZE LIST COUNT
        LI      R3, MXRCNT      INITIALIZE MAX COUNT
        LI      R4, CARRET      SET UP END OF BLOCK CHARACTER
RCVLP   TB      21              WAIT FOR RBRL = 1
        JNE     RCVLP
        STCR    *R2,8           STORE CHARACTER
        SBZ     18              RESET RBRL
        DEC     R3              DECREMENT COUNT
        JEQ     RCVEND          END IF COUNT = 0
        CB      *R2 + ,R4       COMPARE TO EOB CHARACTER, INCREMENT POINTER
        JNE     RCVLP           LOOP IF NOT COMPLETE
RCVEND  RT                      END OF SUBROUTINE
```

Register Loading After Initialization

The control, interval, and data rate registers may be reloaded after initialization. For example, it may be desirable to change the interval of the timer. Assume, for sample, that the interval is to be changed to 10.24 milliseconds. The instruction sequence is as follows:

```
        SBO     13              SET LOAD CONTROL FLAG
        LDCR    @INTVL2,8       LOAD REGISTER, RESET FLAG
          •
          •
          •
INTVL2  BYTE    10240/64
```

Caution should be exercised when transmitter interrupts are enabled to ensure that the transmitter interrupt does not occur while the load control flag is set. For example, if the transmitter interrupts between execution of the "SBO 13" and the next instruction, the transmit buffer is not enabled for loading when the transmitter interrupt service routine is entered because the LDIR flag is set. This situation may be avoided by the following sequence:

```
                BLWP    @INTVCHG        CALL SUBROUTINE
                  •
                  •
                  •
ITV CPC         LI MI   0               MASK ALL INTERRUPTS
                MOV     @24(R13), RIZ   LOAD CRU BASE ADDRESS
                SB0     13              SET FLAG
                LDCR    @INTVL2,8       LOAD REGISTER AND RESET FLAG
                RTWP                    RESTORE MASK AND RETURN
                  •
                  •
                  •
ITVCHG          DATA    ACCWP, ITVCPC
INTVL2          BYTE    10240/64
```

In this case all interrupts are masked, ensuring that all interrupts are disabled while the load control flag is set.

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S7500 Family

S7500 Family Selection Guide

S7500	CMOS 4-Bit Single Chip Microcomputer
S7501	CMOS 4-Bit Single Chip Microcomputer With LCD Controller/Driver
S7502/S7503	CMOS 4-Bit Single Chip Microcomputers With LCD Controller/Driver
S7506	CMOS 4-Bit Single Chip Microcomputer
S7507/S7508	CMOS 4-Bit Single Chip Microcomputers
S7519	CMOS 4-Bit Single Chip Microcomputer With Vacuum Fluorescent Display Controller/Driver

S7500 SERIES CMOS 4-BIT SINGLE CHIP MICROCOMPUTER FAMILY

Features

- ☐ Advanced 4th Generation Architecture
- ☐ Choice of 8-Bit Program Memory (ROM) Size:
  - 1K, 2K, 4K Bytes On-Board
- ☐ Choice of 4-Bit Data Memory (RAM) Size:
  - 64, 96, 128, 208, 224, or 256 Internal Nibbles
- ☐ RAM Stack
- ☐ Four General Purpose Registers: D, E, H, and L
  - Can Address Data Memory and I/O Ports
  - Can be Stored to or Retrieved From Stack
- ☐ Powerful Instruction Set
  - From 58 to 92 Instructions, Including:
    - Direct/Indirect Addressing
    - Table Look-Up
    - RAM Stack Push/Pop
    - Single Byte Subroutine Calls
    - RAM and I/O Port Single Bit Manipulation
    - Accumulator and I/O Port Logical Operations
    - 10μs Instruction Cycle Time, Typically
- ☐ Extensive General Purpose I/O Capability
  - One 4-Bit Input Port
  - Two 4-Bit Latched Tri-State Output Ports
  - Five 4-Bit Input/Latched Tri-State Output Ports
  - 8-Bit Parallel I/O Capability
- ☐ Hardware Logic Blocks—Reduce Software Requirements
  - Operation Completely Transparent to Instruction Execution
  - 8-Bit Timer/Event Counter
    - Binary-Up Counter Generates INT_T at Coincidence
  - Accurate Crystal Clock or External Event Operation Possible
  - Vectored, Prioritized Interrupt Controller
    - Three External Interrupts (INT_0, INT_1, INT_2)
    - Two Internal Interrupts (INT_T, INT_S)
  - Display Controller/Driver
    - Complete Direct Drive and Control of Multiplexed LCD or Vacuum Fluorescent Display
    - Display Data Automatically Multiplexed From RAM to Dedicated Segment/Backplane/Digit Driver lines
  - 8-Bit Serial Interface
    - 3-Line I/O Configuration Generates INT_S Upon Transmission of Eighth Bit
    - Ideal for Distributed Intelligence Systems or Communication With Peripheral Devices
  - Complete Operation Possible in HALT and STOP Power-Down Modes
- ☐ Built-in System Clock Generator
- ☐ Built-in Schmidt-Trigger RESET Circuitry
- ☐ Single Power Supply, Variable From 2.7V to 5.5V
- ☐ Low Power Consumption Silicon Gate 3-Micron CMOS Technology
  - 900μA Max. at 5V, 400μA Max. at 3V
  - HALT, STOP Power-Down Instructions Reduce Power Consumption to 20μA Max. at 5V, 10μA at 3V (Stop Mode)

Description

The AMI S7500 Series CMOS 4-bit Single Chip Microcomputer Family is a product line of 7 individual devices designed to fulfill a wide variety of applications. The advanced 4th generation architecture includes all of the functional blocks necessary for a single chip controller, including an ALU, Accumulator, Program Memory (ROM), Data Memory (RAM), four General Purpose Registers, Stack Pointer, Program Status Word (PSW), 8-Bit Timer/Event Counter, Interrupt Controller, Display Controller/Driver, and 8-Bit Serial Interface. The instruction set maximizes the efficient utilization of fixed Program Memory space, and includes a variety of addressing, Table-Look-up, Logical, Single Bit Manipulation, vectored jump, and Condition Skip instructions.

The S7500 Series includes three different devices, the S7501, S7502, and S7503, capable of directly driving Liquid Crystal Displays with up to 12 7-segment digits. The S7519 can directly drive up to 35V Vacuum Fluorescent Displays with up to 16 7-segment digits.

All seven devices are manufactured with a Silicon gate CMOS process, consuming only 900μA max. at 5V, and only 400μA max. at 3V. The HALT and STOP power-

Description (Continued)

down instructions can significantly reduce power consumption even further.

The flexibility and the wide variety of S7500 Series devices available make the S7500 series ideally suited for a wide range of battery-powered, solar-powered, and portable products, such as telecommunication devices, hand-held instruments and meters, automotive products, industrial controls, energy management systems, medical instruments, portable terminals, portable measuring devices, appliances, and consumer products.

S7500 Series

Features	7501	7502	7503	7506	7507	7508	7519
Internal ROM (8-bit words)	1K	2K	4K	1K	2K	4K	4K
RAM	96×4	128×4	224×4	64×4	128×4	224×4	256×4
I/O Lines	24	23	23	22	32	32	28
8-Bit Timer/Event Counter	•	•	•	•	•	•	•
8-Bit Serial Interface	•	•	•	•	•	•	•
Registers Outside RAM	2×4	4×4	4×4	2×4	4×4	4×4	4×4
Instructions	63	92	92	58	92	92	92
Min. Cycle Time (μs)	6.67	6.67	6.67	6.67	6.67	6.67	6.67
Interrupts	4	4	4	2	4	4	4
Stack Levels	RAM	RAM	RAM	RAM	RAM	RAM	RAM
Display Controller/Driver	LCD	LCD	LCD				VFD
Analog I/O							14-bit D/A
Current Consumption (max)							
Normal Operation	← 900A at 5V ± 100%; 400μA at 3V ± 10% →						
Stop Mode	← 20A at 5V ± 10%; 10μA at 3V ± 10% →						

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER WITH LCD CONTROLLER/DRIVER

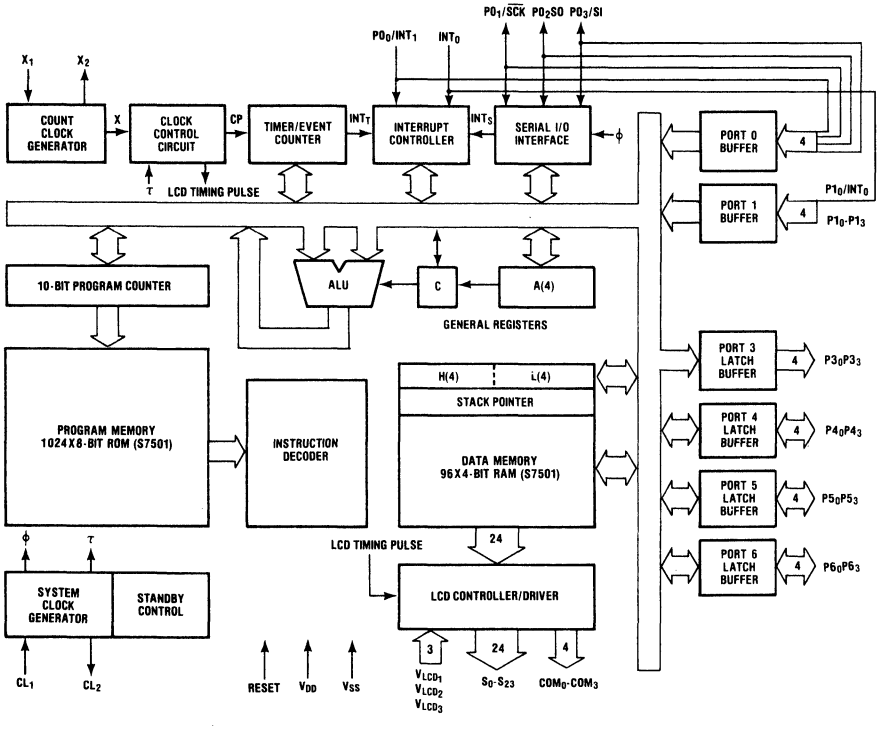
Functional Description

The S7501 is a CMOS 4-bit single chip microcomputer which has the 750x architecture.

The S7501 contains a 1024 x 8-bit ROM, and a 96 x 4-bit RAM.

The S7501 contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The S7501 typically executes 63 instructions of the S7500 series "B" instruction set with

Block Diagram



Functional Description (Continued)

a 10μs instruction cycle time.

The S7501 has two external and two internal edge-triggered testable interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements. The on-board LCD controller/driver supervises all of the timing required by the 24 Port S segment drivers and the 4 Port COM backplane drivers, for either a 12-digit 7-segment quadriplexed LCD, or an 8-digit 7-segment triplexed LCD.

The S7501 provides 24 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit input Port 1, the 4-bit output Port 3, and the 4-bit I/O Ports 4, 5, and 6. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes.

The S7501 is upward compatible with the S7502 and the S7503.

Absolute Maximum Ratings* ($T_A = 25°C$)

Power Supply Voltage, V_{DD}	$-0.3V$ to $+7.0V$
All Input and Output Voltages	$-0.3V$ to $V_{DD} + 0.3V$
Output-Current (Total, All Output Ports)	$I_{OH} = -20mA$; $I_{OL} = 30mA$

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (V_{DD} = 2.7V to 5.5V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
V_{IH} $V_{\phi H}$ V_{IHDR}	Input Voltage High	0.7 V_{DD} $V_{DD} - 0.5$ 0.9 V_{DDDR}		V_{DD} V_{DD} $V_{DDDR} + 0.2$	V	All Inputs Other than CL_1, X_1 CL_1, X_1 RESET, Data Retention Mode
V_{IL} $V_{\phi L}$	Input Voltage Low	0 0		0.3 V_{DD} 0.5	V	All Inputs Other than CL_1, X_1 CL_1, X_1
I_{LIH} $I_{L\phi H}$	Input Leakage Current High			3 10	μA	All Inputs Other than CL_1, X_1 CL_1, X_1 $V_I = V_{DD}$
I_{LIL} $I_{L\phi L}$	Input Leakage Current Low			−3 −10	μA	All Inputs Other than CL_1, X_1 CL_1, X_1 $V_I = 0V$
V_{OH}	Output Voltage High	$V_{DD} - 1.0$ $V_{DD} - 0.5$			V	$V_{DD} = 5V \pm 10\%$, $I_{OH} = -1.0mA$ $V_{DD} = 2.7V$ to 5.5V, $I_{OH} = -100\mu A$
V_{OL}	Output Voltage Low			0.4 0.5	V	$V_{DD} = 5V \pm 10\%$, $I_{OL} = 1.6mA$ $V_{DD} = 2.7V$ to 5.5V, $I_{OL} = 400\mu A$
I_{LOH}	Output Leakage Current High			3	μA	$V_O = V_{DD}$
I_{LOL}	Output Leakage Current Low			−3	μA	$V_O = 0V$
R_{COM}	Output Impedance		5	5	kΩ	COM_0 to COM_3, $2.7V \leqslant V_{LCD} \leqslant V_{DD}$ $V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V
R_S			20	20	kΩ	S_0 to S_{23}, $2.7V \leqslant V_{LCD} \leqslant V_{DD}$ $V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V
V_{DDDR}	Supply Voltage	2.0			V	Data Retention Mode

DC Characteristics (Continued)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions	
I_{DDO}	Supply Current		300 150	900 400	μA	Normal Operation	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 3V \pm 10\%$
I_{DDS}			2 0.5	20 10	μA	Stop Mode, $X_1 = 0V$	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 3V \pm 10\%$
I_{DDDR}			0.4	10	μA	Data Retention Mode $V_{DDDR} = 2.0V$	

AC Characteristics (V_{DD} = 2.7V to 5.5V)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions	
t_ϕ	System Clock Oscillation Frequency	120 60 60	200 100	280 130 180	kHz	R = 82kΩ ± 2% CL_1, CL_2 C = 33pF ± 5% R/C Clock R = 160kΩ ± 2% C = 33pF ± 5%	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 3V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V
$t_{\phi Ext}$		10 10	200	300 135	kHz	CL_1, External Clock	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V
$t_{r\phi}$, $t_{f\phi}$	System Clock Rise and Fall Times			0.2	μs	CL_1, External Clock	
$t_{\phi W_H}$, $t_{\phi W_L}$	System Clock Pulse Width	1.5 3.5		50 50	μs	CL_1, External Clock	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V
f_X	Counter Clock Oscillation Frequency	25	32	50	KHz	X_1, X_2 Crystal Oscillator	
f_{XExt}		0 0		300 135		X_1, External Pulse Input	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V
t_{rX}, t_{fX}	Counter Clock Rise and Fall Times			0.2	μs	X_1, External Pulse Input	
t_{XW_H}, t_{XW_L}	Counter Clock Pulse Width	1.5 3.5			μs	X_1, External Pulse Width	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V
t_{CYK}	$\overline{SCK}$ Cycle Time	4.0 7.0 6.7 14.0			μs	$\overline{SCK}$ is an input $\overline{SCK}$ is an output	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V $V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V
t_{KW_H}, T_{KW_L}	$\overline{SCK}$ Pulse Width	1.8 3.3 3.0 6.5			μs	$\overline{SCK}$ is an input $\overline{SCK}$ is an output	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V $V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V
t_{IS}	SI Setup Time to SCK↑	300			ns		
t_{IH}	SI Hold Time after SCK↑	450			ns		
t_{OD}	SO Delay Time after SCK↓			850 1200	ns	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to 5.5V	
t_{IOW_H} t_{IOW_L}	INT_0 Pulse Width	10			μs		

AC Characteristics (Continued)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{I1WH} t_{I1WL}	INT_1 Pulse Width	$2/f\phi$			μs	
t_{RWH} t_{RWL}	RESET Pulse Width	10			μs	
t_{RS}	RESET Setup Time	0			ns	
t_{RH}	RESET Hold Time	0			ns	

Capacitance ($T_A = 25°C$, $V_{DD} = 0V$)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
C_I	Input Capacitance			15	pF	f = 1MHz
C_O	Output Capacitance			15	pF	Unmeasured pins
$C_{I/O}$	Input/Output Capacitance			15		returned to V_{SS}

Pin Names

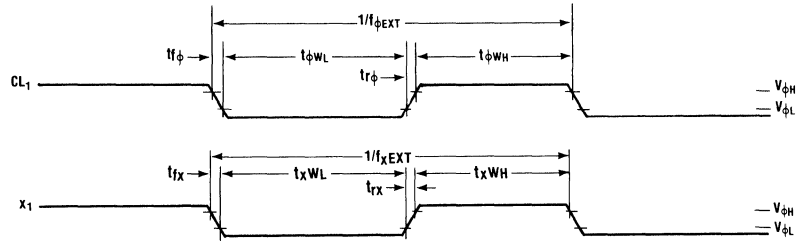
Symbol	Function
NC	No connection.
$P3_3$-$P3_0$	4-bit latched tri-state output Port 3 (active high).
$P0_3$/SI	4-bit input Port 0/serial I/O interface (active high).
$P0_2$/SO $P0_1/\overline{SCK}$ $P0_0/INT_1$	This port can be configured either as a parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer, comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_1.
$P6_3P6_0$	4-bit input/latched tri-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
$P5_3$-$P5_0$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
$P4_3$-$P4_0$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
X_2-X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
V_{SS}	Ground
V_{LCD3}, V_{LCD2}, V_{LCD1}	LCD bias voltage supply inputs to LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.

Pin Names (Continued)

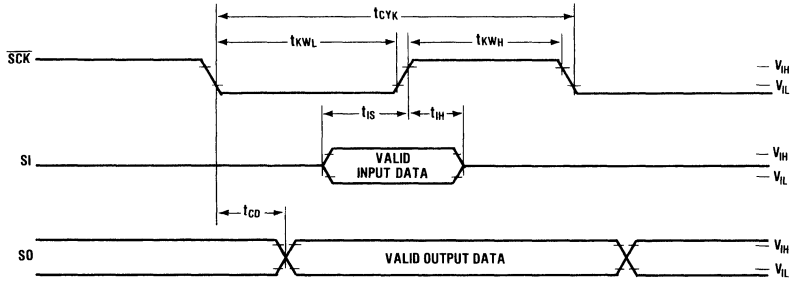
Symbol	Function
V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
COM_3-COM_0	LCD backplane driver outputs.
S_{23}-S_0	LCD segment driver outputs.
RESET	RESET input (active high). R/C circuit or pulse initializes S7501 after power-up.
CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
$P1_3$-$P1_0$ ($P1_0$/INT_0)	4-bit input Port 1 (active high). Line $P1_0$ is also shared with external interrupt INT_0.

Timing Waveforms

CLOCKS



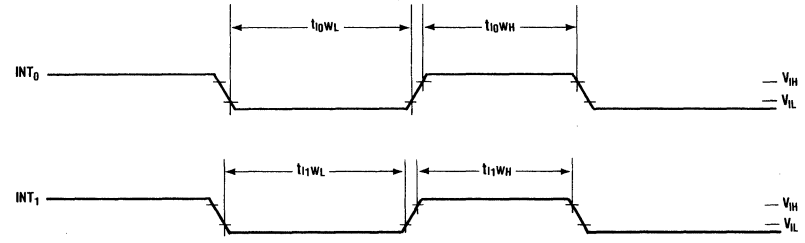
SERIAL INTERFACE



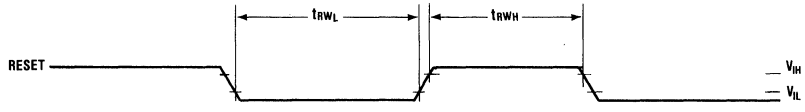
S7500 FAMILY

Timing Waveforms

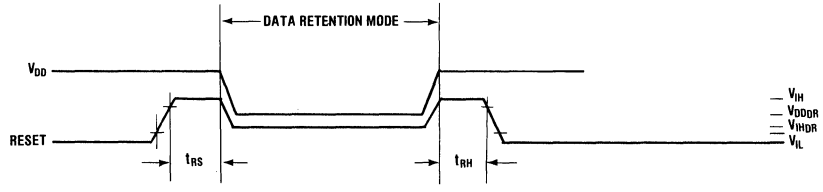
EXTERNAL INTERRUPTS



RESET



DATA RETENTION MODE



CMOS 4-BIT SINGLE CHIP MICROCOMPUTERS WITH LCD CONTROLLER/DRIVER

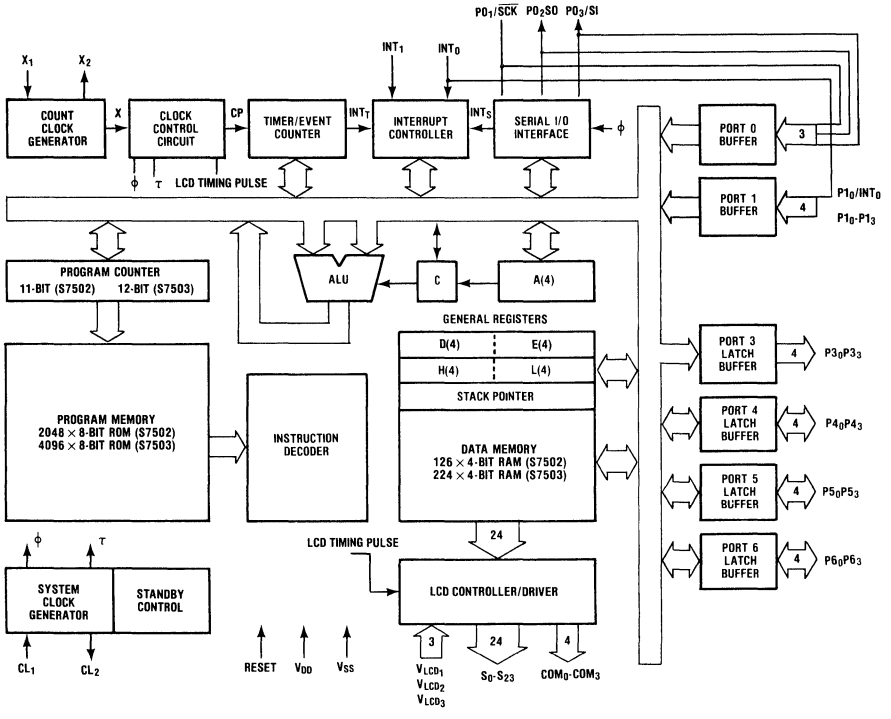
Functional Description

The S7502 and the S7503 are pin-compatible CMOS 4-bit single chip microcomputers which have the same S750X architecture.

The S7502 contains a 2048 x 8-bit ROM, and a 128 x 4-bit RAM. The S7503 contains a 4096 x 8-bit ROM, and a 224 x 4-bit RAM.

Both the S7502 and the S7503 contain four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values.

Block Diagram



Functional Description (Continued)

The S7502 and the S7503 typically execute 92 instructions of the S7500 series "A" instruction set with a 10μs instruction cycle time.

The S7502 and the S7503 have two external and two internal edge-triggered hardware vectored interrupts. They also contain an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements. The on-board LCD controller/driver supervises all of the timing required by the 24 Post S segment drivers and the 4 Port COM backplane drivers, for either a 12-digit 7-segment quadriplexed LCD, or an 8-digit 7-segment triplexed LCD.

Both the S7502 and the S7503 provide 23 I/O lines, organized into the 3-bit input/serial interface Port 0, the 4-bit input Port 1, the 4-bit output Port 3, and the 4-bit I/O Ports 4, 5, and 6. They are manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes.

The S7502 is downward compatible with the S7501.

Absolute Maximum Ratings* (T_A = 25°C)

All Input and Output Voltages	$-0.3V$ to $V_{DD} + 0.3V$
Output-Current (Total, All Output Ports)	$I_{OH} = -20mA$; $I_{OL} = 30mA$

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (V_{DD} = 2.7V to 5.5V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
V_{IH}	Input Voltage High	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1
$V_{\phi H}$		$V_{DD} - 0.5$		V_{DD}		CL_1, X_1
V_{IHDR}		0.9 V_{DDDR}		$V_{DDDR} + 0.2$		RESET, Data Retention Mode
V_{IL}	Input Voltage Low	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1
$V_{\phi L}$		0		0.5		CL_1, X_1
I_{LIH}	Input Leakage Current High			3	μA	All Inputs Other than CL_1, X_1 $V_I = V_{DD}$
$I_{L\phi H}$				10		CL_1, X_1
I_{LIL}	Input Leakage Current Low			−3	μA	All Inputs Other than CL_1, X_1 $V_I = 0V$
$I_{L\phi L}$				−10		CL_1, X_1
V_{OH}	Output Voltage High	$V_{DD} - 1.0$			V	$V_{DD} = 5V \pm 10\%$, $I_{OH} = -1.0mA$
		$V_{DD} - 0.5$				$V_{DD} = 2.7V$ to 5.5V, $I_{OH} = -100\mu A$
V_{OL}	Output Voltage Low			0.4	V	$V_{DD} = 5V \pm 10\%$, $I_{OL} = 1.6mA$
				0.5		$V_{DD} = 2.7V$ to 5.5V, $I_{OL} = 400\mu A$
I_{LOH}	Output Leakage Current High			3	μA	$V_O = V_{DD}$
I_{LOL}	Output Leakage Current Low			−3	μA	$V_O = 0V$
R_{COM}	Output Impedance		5	5	kΩ	COM_0 to COM_3, $2.7V \leq V_{LCD} \leq V_{DD}$ $V_{DD} = 5V \pm 10\%$ / $V_{DD} = 2.7V$ to 5.5V
R_S			20	20	kΩ	S_0 to S_{23}, $2.7V \leq V_{LCD} \leq V_{DD}$ $V_{DD} = 5V \pm 10\%$ / $V_{DD} = 2.7V$ to 5.5V
V_{DDDR}	Supply Voltage	2.0			V	Data Retention Mode

DC Characteristics (Continued)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions	
I_{DDO}	Supply Current		300 150	900 400	μA	Normal Operation	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 3V \pm 10\%$
I_{DDS}			2 0.5	20 10	μA	Stop Mode, $X_1 = 0V$	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 3V \pm 10\%$
I_{DDDR}			0.4	10	μA	Data Retention Mode $V_{DDDR} = 2.0V$	

AC Characteristics (V_{DD} = 2.7V to 5.5V)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions	
f_ϕ	System Clock Oscillation Frequency	120 60 60	200 100	280 130 180	kHz	CL_1, CL_2 $R = 82k\Omega \pm 2\%$, $C = 33pF \pm 5\%$ R/C Clock $R = 160k\Omega \pm 2\%$, $C = 33pF \pm 5\%$	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 3V \pm 10\%$ $V_{DD} = 2.7V$ to $5.5V$
$f_{\phi Ext}$		10 10	200	300 135	kHz	CL_1, External Clock	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to $5.5V$
$t_{r\phi}$, $t_{f\phi}$	System Clock Rise and Fall Times			0.2	μs	CL_1, External Clock	
$t_{\phi WH}$, $t_{\phi WL}$	System Clock Pulse Width	1.5 3.5		50 50	μs	CL_1, External Clock	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to $5.5V$
f_X	Counter Clock Oscillation Frequency	25	32	50	KHz	X_1, X_2 Crystal Oscillator	
f_{XExt}		0 0		300 135		X_1, External Pulse Input	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to $5.5V$
t_{rX}, t_{fX}	Counter Clock Rise and Fall Times			0.2	μs	X_1, External Pulse Input	
t_{XWH}, t_{XWL}	Counter Clock Pulse Width	1.5 3.5			μs	X_1, External Pulse Width	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to $5.5V$
t_{CYK}	$\overline{SCK}$ Cycle Time	4.0 7.0 6.7 14.0			μs	$\overline{SCK}$ is an input $\overline{SCK}$ is an output	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to $5.5V$ $V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to $5.5V$
t_{KWH}, t_{KWL}	$\overline{SCK}$ Pulse Width	1.8 3.3 3.0 6.5			μs	$\overline{SCK}$ is an input $\overline{SCK}$ is an output	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to $5.5V$ $V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to $5.5V$
t_{IS}	SI Setup Time to SCK↑	300			ns		
t_{IH}	SI Hold Time after SCK↑	450			ns		
t_{OD}	SO Delay Time after SCK↓			850 1200	ns	$V_{DD} = 5V \pm 10\%$ $V_{DD} = 2.7V$ to $5.5V$	
t_{IOWH} t_{IOWL}	INT_0 Pulse Width	10			μs		

AC Characteristics (Continued)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{I1WH} t_{I1WL}	INT_1 Pulse Width	$2/f\phi$			μs	
t_{RWH} t_{RWL}	RESET Pulse Width	10			μs	
t_{RS}	RESET Setup Time	0			ns	
t_{RH}	RESET Hold Time	0			ns	

Capacitance (T_A = 25°C, V_{DD} = 0V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
C_1	Input Capacitance			15	pF	f = 1MHz
C_0	Output Capacitance			15	pF	Unmeasured pins
$C_{I/O}$	Input/Output Capacitance			15		returned to V_{SS}

Pin Names

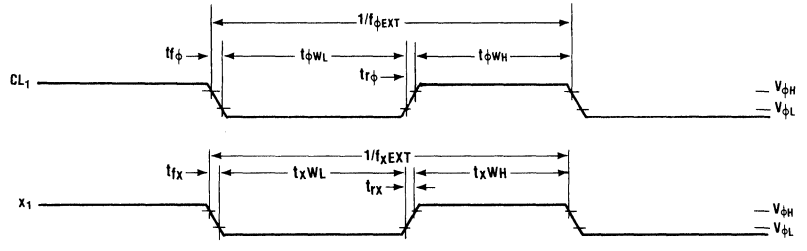
Symbol	Function
NC	No connection.
$P3_3$-$P3_0$	4-bit latched tri-state output Port 3 (active high).
$P0_3$/SI	3-bit input Port 0/serial I/O interface (active high).
$P0_2$/SO $P0_1/\overline{SCK}$	This port can be configured either as a parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active high), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer, comprise the 8-bit serial I/O interface.
$P6_3P6_0$	4-bit input/latched tri-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
$P5_3$-$P5_0$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
$P4_3$-$P4_0$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
X_2-X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
V_{SS}	Ground
V_{LCD3}, V_{LCD2}, V_{LCD1}	LCD bias voltage supply inputs to LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.

Pin Names (Continued)

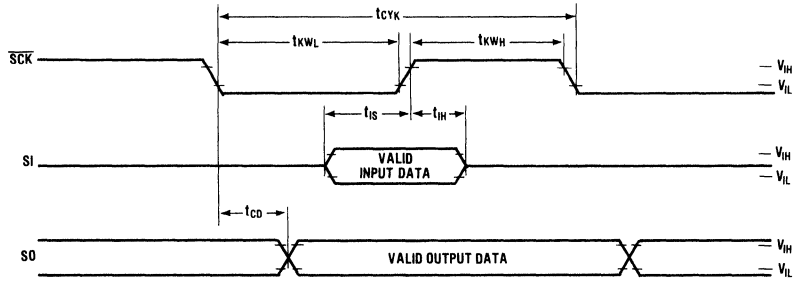
Symbol	Function
V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
COM_3-COM_0	LCD backplane driver outputs.
S_{23}-S_0	LCD segment driver outputs.
INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
RESET	RESET input (active high). R/C circuit or pulse initializes S7502 after power-up.
CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
$P1_3$-$P1_0$ ($P1_0$/INT_0)	4-bit input Port 1 (active high). Line $P1_0$ is also shared with external interrupt INT_0, which is a rising edge-triggered interrupt.

Timing Waveforms

CLOCKS



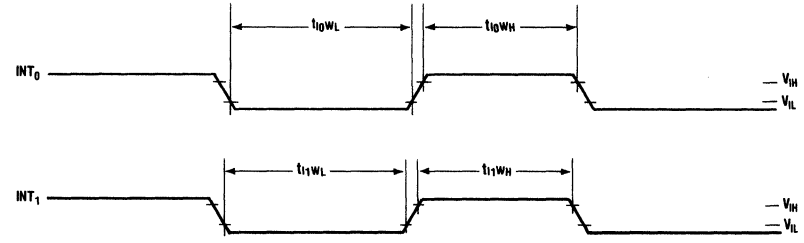
SERIAL INTERFACE



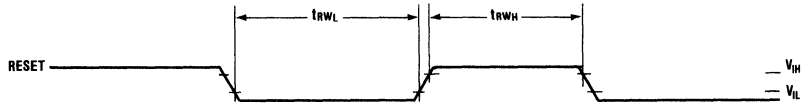
S7500 FAMILY

Timing Waveforms

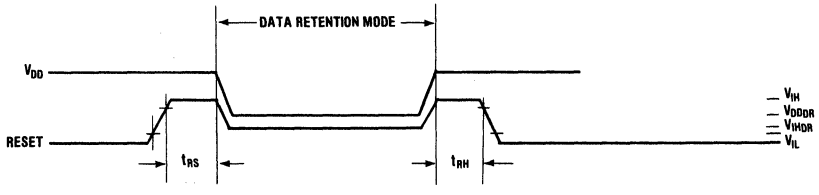
EXTERNAL INTERRUPTS



RESET



DATA RETENTION MODE



S7506

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

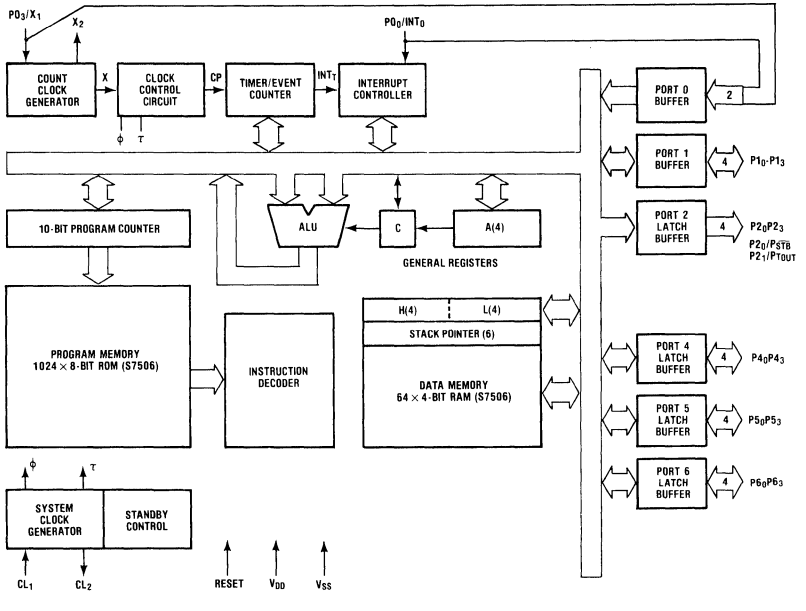
Functional Description

The S7506 is a CMOS 4-bit single chip microcomputer which has the 750x architecture.

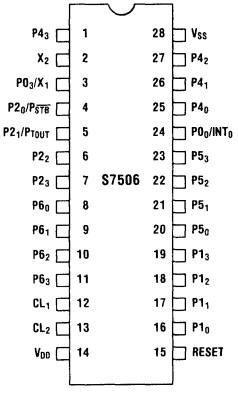
The S7506 contains a 1024 × 8-bit ROM, and a 64 × 4-bit RAM.

The S7506 contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The S7506 typically executes 58 instructions of the S7500 series "B" instruction set with

Block Diagram



Pin Configuration



(TOP VIEW)

S7500 FAMILY

Functional Description (Continued)

a 10μs instruction cycle time.

The S7506 has one external and one internal edge-triggered testable interrupts. It also contains an 8-bit timer/event counter to help reduce software requirements.

The S7506 provides 22 I/O lines organized into the 2-bit input Port 0, the 4-bit output Port 2, and the 4-bit I/O Ports 1, 4, and 5. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 600μA maximum, and can be lowered much further in the HALT and STOP power-down modes.

The S7506 is upward compatible with the S7507.

Absolute Maximum Ratings* ($T_A = 25°C$)

Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	$I_{OH} = -20mA$; $I_{OL} = 32mA$

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (V_{DD} = 2.7V to 5.5V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
V_{IH} $V_{\phi H}$ V_{IHDR}	Input Voltage High	0.7 V_{DD} V_{DD} − 0.5 0.9 V_{DDDR}		V_{DD} V_{DD} V_{DDDR} + 0.2	V	All Inputs Other than CL_1, X_1 CL_1, X_1 RESET, Data Retention Mode
V_{IL} $V_{\phi L}$	Input Voltage Low	0 0		0.3 V_{DD} 0.5	V	All Inputs Other than CL_1, X_1 CL_1, X_1
I_{LIH} $I_{L\phi H}$	Input Leakage Current High			3 10	μA	All Inputs Other than CL_1, X_1 $V_I = V_{DD}$ CL_1, X_1
I_{LIL} $I_{L\phi L}$	Input Leakage Current Low			−3 −10	μA	All Inputs Other than CL_1, X_1 $V_I = 0V$ CL_1, X_1
V_{OH}	Output Voltage High	V_{DD} − 1.0 V_{DD} − 0.5			V	$V_{DD} = 5V \pm 10\%$, $I_{OH} = -1.0mA$ V_{DD} = 2.7V to 5.5V, $I_{OH} = -100\mu A$
V_{OL}	Output Voltage Low			0.4 0.5	V	$V_{DD} = 5V \pm 10\%$, $I_{OL} = 1.6mA$ V_{DD} = 2.7V to 5.5V, $I_{OL} = 400\mu A$
I_{LOH}	Output Leakage Current High			3	μA	$V_O = V_{DD}$
I_{LOL}	Output Leakage Current Low			−3	μA	$V_O = 0V$
V_{DDDR}	Supply Voltage	2.0			V	Data Retention Mode
I_{DDO}	Supply Current		200 100	600 300	μA	Normal Operation $V_{DD} = 5V \pm 10\%$ $V_{DD} = 3V \pm 10\%$
I_{DDS}			1 0.3	10 5	μA	Stop Mode, $X_1 = 0V$ $V_{DD} = 5V \pm 10\%$ $V_{DD} = 3V \pm 10\%$
I_{DDDR}			0.4	10	μA	Data Retention Mode $V_{DDDR} = 2.0V$

AC Characteristics (V_{DD} = 2.7V to 5.5V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{ϕ}	System Clock Oscillation Frequency	120 60 60	200 100	260 130 180	kHz	R = 120kΩ ± 2% V_{DD} = 5V ± 10% CL_1, CL_2 R = 240kΩ ± 2% V_{DD} = 3V ± 10% V_{DD} = 2.7V to 5.5V
$t_{\phi Ext}$		10 10	200	300 135	kHz	CL_1, External Clock V_{DD} = 5V ± 10% V_{DD} = 2.7V to 5.5V
$t_{r\phi}$, $t_{f\phi}$	System Clock Rise and Fall Times			0.2	μs	CL_1, External Clock
$t_{\phi WH}$, $t_{\phi WL}$	System Clock Pulse Width	1.5 3.5		50 50	μs	CL_1, External Clock V_{DD} = 5V ± 10% V_{DD} = 2.7V to 5.5V
f_X	Counter Clock Oscillation Frequency	25	32	50	kHz	X_1, X_2 Crystal Oscillator
f_{XExt}		0 0		300 135		X_1, External Pulse Input V_{DD} = 5V ± 10% V_{DD} = 2.7V to 5.5V
t_{rX}, t_{fX}	Counter Clock Rise and Fall Times			0.2	μs	X_1, External Pulse Input
t_{XWH}, t_{XWL}	Counter Clock Pulse Width	1.5 3.5			μs	X_1, External Pulse Input V_{DD} = 5V ± 10% V_{DD} = 2.7V to 5.5V
t_{P1S}	Port 1 Output Setup Time to $P_{STB}\uparrow$	$1/(2f_{\phi}-800)$ $1/(2f_{\phi}-2000)$			ns	V_{DD} = 5V ± 10% V_{DD} = 2.7V to 5.5V
t_{P1H}	Port 1 Output Hold Time after $P_{\overline{STB}}\uparrow$	300 300	350	500 1500	ns	V_{DD} = 5V ± 10% V_{DD} = 2.7V to 5.5V
t_{SWL}	$P_{\overline{STB}}$ Pulse Width	$1/(2f_{\phi}-800)$ $1/(2f_{\phi}-2000)$			ns	V_{DD} = 5V ± 10% V_{DD} = 2.7V to 5.5V
t_{I0WH}, t_{I0WL}	INT_0 Pulse Width	10			μs	
t_{RWH}, t_{RWL}	RESET Pulse Width	10			μs	
t_{RS}	RESET Setup Time	0			ns	
t_{RH}	RESET Hold Time	0			ns	

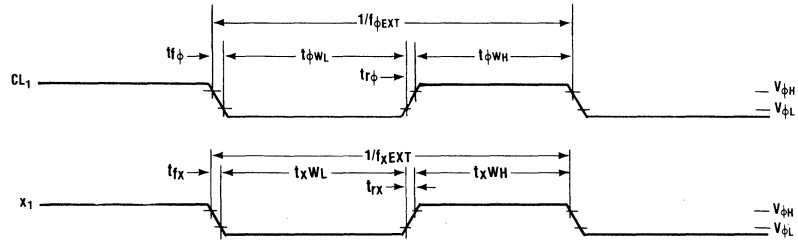
Capacitance (T_A = 25°C, V_{DD} = 0V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
C_I	Input Capacitance			15	pF	f = 1MHz
C_O	Output Capacitance			15		Unmeasured pins
$C_{I/O}$	Input/Output Capacitance			15		returned to V_{SS}

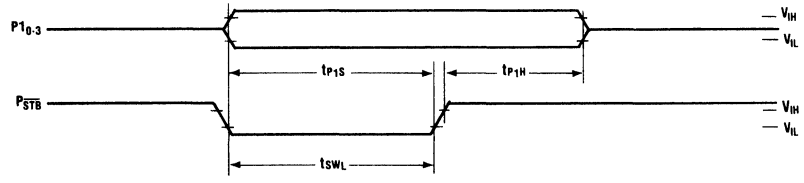
Pin Names

Symbol	Function
$P4_0$-$P4_3$	4-bit input/latched tristate output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
X_2-PO_3/X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting. Line X_1 is always shared with Port 0 input PO_3.
$P2_0$-$P2_3$ $P2_0/P_{\overline{STB}}$ $P2_1/P_{TOUT}$	4-bit latched tristate output Port 2 (active high). Line $P2_0$ is also shared with P_{STB}, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with P_{TOUT}, the timer-out F/F signal (active high).
$P6_0P6_3$	4-bit input/latched tristate output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
CL_1, CL_2	System clock input (active high). Connect 120kΩ resistor across CL_1 and CL_2. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
RESET	RESET input (active high). R/C circuit or pulse initializes S7507 or S7508 after power-up.
$P1_0P1_3$	4-bit input/tristate output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0/P_{STB}$ pulse.
$P5_0$-$P5_3$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
PO_0/INT_0 PO_3/X_1	2-bit input Port 0 (active high). Line PO_0 is always shared with external interrupt INT_0 (active high). Line PO_3 is always shared with crystal clock/external event input X_1 (active high).
V_{SS}	Ground

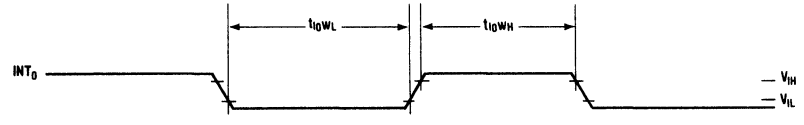
Timing Waveforms — Clocks



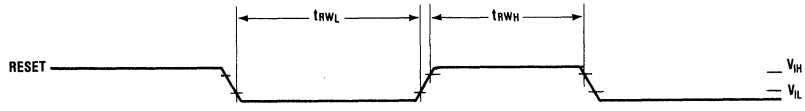
Timing Waveforms — Output Strobe



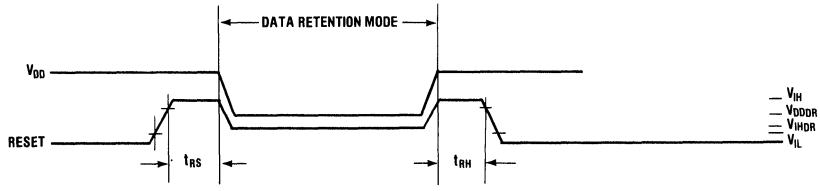
Timing Waveforms — External Interrupt



Timing Waveforms — Reset



Timing Waveforms — Data Retention Mode



CMOS 4-BIT SINGLE CHIP MICROCOMPUTERS

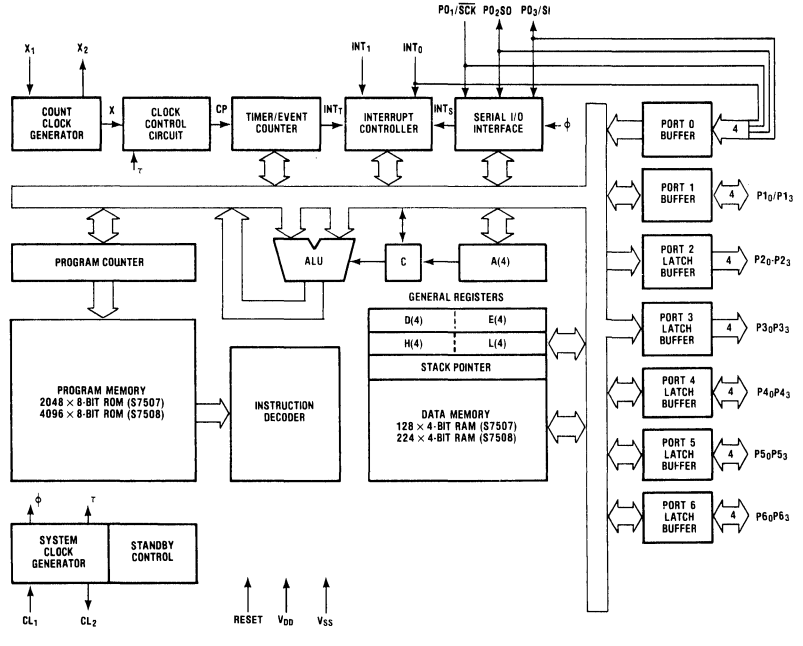
Functional Description

The S7507 and the S7508 are pin compatible CMOS 4-bit single chip microcomputers which have the 750x architecture.

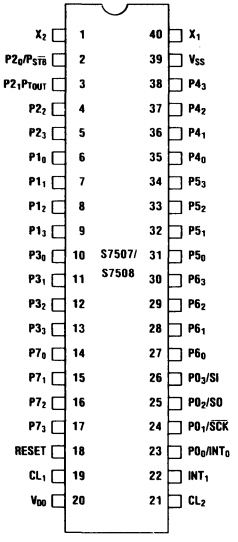
The S7507 contains a 2048 x 8-bit ROM, and a 128 x 4-bit RAM. The S7508 contains a 4096 x 8-bit ROM, and a 224 x 4-bit RAM.

Both the S7507 and the S7508 contain four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations

Block Diagram



Pin Configuration



S7500 FAMILY

Functional Description (Continued)

as the pushing and popping of register values. The S7507 and the S7508 typically execute 92 instructions of the S7500 series "A" instruction set with a 10μs instruction cycle time.

The S7507 and the S7508 have two external and two internal edge-triggered hardware vectored interrupts. They also contain an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

Both the S7507 and the S7508 provide 32 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit input Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, 6, and 7. They are manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes.

The S7507 is downward compatible with the S7506.

Absolute Maximum Ratings* ($T_A = 25°C$)

Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	$I_{OH} = -20mA$; $I_{OL} = 30mA$

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (V_{DD} = 2.7V to 5.5V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
V_{IH}	Input Voltage High	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1
$V_{\phi H}$		$V_{DD}-0.5$		V_{DD}		CL_1, X_1
V_{IHDR}		0.9 V_{DDDR}		$V_{DDDR}+0.2$		RESET, Data Retention Mode
V_{IL}	Input Voltage Low	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1
$V_{\phi L}$		0		0.5		CL_1, X_1
I_{LIH}	Input Leakage Current High			3	μA	All Inputs Other than CL_1, X_1 $V_I = V_{DD}$
$I_{L\phi H}$				10		CL_1, X_1
I_{LIL}	Input Leakage Current Low			−3	μA	All Inputs Other than CL_1, X_1 $V_I = 0V$
$I_{L\phi L}$				−10		CL_1, X_1
V_{OH}	Output Voltage High	$V_{DD}-1.0$			V	$V_{DD} = 5V \pm 10\%$, $I_{OH} = -1.0mA$
		$V_{DD}-0.5$				V_{DD} = 2.7V to 5.5V, $I_{OH} = -100\mu A$
V_{OL}	Output Voltage Low			0.4	V	$V_{DD} = 5V \pm 10\%$, $I_{OL} = 1.6mA$
				0.5		V_{DD} = 2.7V to 5.5V, $I_{OL} = 400\mu A$
I_{LOH}	Output Leakage Current High			3	μA	$V_O = V_{DD}$
I_{LOL}	Output Leakage Current Low			−3	μA	$V_O = 0V$
V_{DDDR}	Supply Voltage	2.0			V	Data Retention Mode
I_{DDO}	Supply Current		300	900	μA	Normal Operation $V_{DD} = 5V \pm 10\%$
			150	400		$V_{DD} = 3V \pm 10\%$
I_{DDS}			2	20	μA	Stop Mode, $X_1 = 0V$ $V_{DD} = 5V \pm 10\%$
			0.5	10		$V_{DD} = 3V \pm 10\%$
I_{DDDR}			0.4	10	μA	Data Retention Mode $V_{DDDR} = 2.0V$

AC Characteristics (V_{DD} = 2.7V to 5.5V)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
t_{ϕ}	System Clock Oscillation Frequency	120	200	280	kHz	CL_1, CL_2 R = 320kΩ ± 2% C = 33pF ± 5%	V_{DD} = 5V ± 10%
		60	100	130		R = 250kΩ ± 2% C = 33pF ± 5%	V_{DD} = 3V ± 10%
		60		180			V_{DD} = 2.7V to 5.5V
$t_{\phi Ext}$		10	200	300	kHz	CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
$t_{r\phi}$, $t_{f\phi}$	System Clock Rise and Fall Times			0.2	µs	CL_1, External Clock	
$t_{\phi WH}$, $t_{\phi WL}$	System Clock Pulse Width	1.5		50	µs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
f_X	Counter Clock Oscillation Frequency	25	32	50	KHz	X_1, X_2 Crystal Oscillator	
f_{XExt}		0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
t_{rX}, t_{fX}	Counter Clock Rise and Fall Times			0.2	µs	X_1, External Pulse Input	
t_{XWH}, t_{XWL}	Counter Clock Pulse Width	1.5			µs	X_1, External Pulse Width	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V
t_{CYK}	$\overline{SCK}$ Cycle Time	4.0			µs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		7.0					V_{DD} = 2.7V to 5.5V
		6.7				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		14.0					V_{DD} = 2.7V to 5.5V
t_{KWH}, T_{KWL}	$\overline{SCK}$ Pulse Width	1.8			µs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		3.3					V_{DD} = 2.7V to 5.5V
		3.0				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		6.5					V_{DD} = 2.7V to 5.5V
t_{IS}	SI Setup Time to $\overline{SCK}\uparrow$	300			ns		
t_{IH}	SI Hold Time after $\overline{SCK}\uparrow$	450			ns		
t_{OD}	SO Delay Time after $\overline{SCK}\downarrow$			850	ns	V_{DD} = 5V ± 10%	
				1200		V_{DD} = 2.7V to 5.5V	
t_{P1S}	Port 1 Output Setup Time to $P_{\overline{STB}}\uparrow$	$1/(2f_{\phi}-800)$			ns	V_{DD} = 5V ± 10%	
		$1/(2f_{\phi}-2000)$				V_{DD} = 2.7V to 5.5V	
t_{P1H}	Port 1 Output Hold Time after $P_{\overline{STB}}\uparrow$	300	350	500	ns	V_{DD} = 5V ± 10%	
		300		1500		V_{DD} = 2.7V to 5.5V	
t_{SWL}	P_{STB} Pulse Width	$1/(2f_{\phi}-800)$			ns	V_{DD} = 5V ± 10%	
		$1/(2f_{\phi}-2000)$				V_{DD} = 2.7V to 5.5V	
t_{I0WH} t_{I0WL}	INT_0 Pulse Width	10			µs		
t_{I1WH} t_{I1WL}	INT_1 Pulse Width	$2/f\phi$			µs		

AC Characteristics (Continued)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{RW_H} t_{RW_L}	RESET Pulse Width	10			μs	
t_{RS}	RESET Setup Time	0			ns	
t_{RH}	RESET Hold Time	0			ns	

Capacitance ($T_A = 25°C$, $V_{DD} = 0V$)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
C_I	Input Capacitance			15	pF	f = 1MHz
C_O	Output Capacitance			15	pF	Unmeasured pins
$C_{I/O}$	Input/Output Capacitance			15		returned to V_{SS}

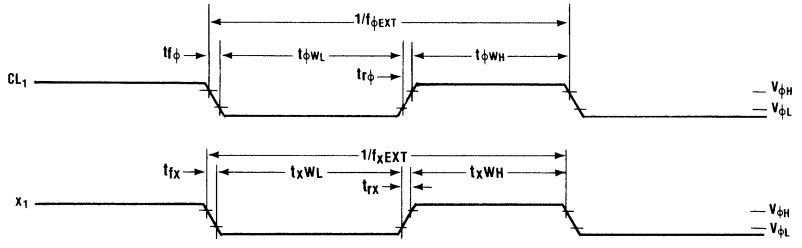
Pin Names

Symbol	Function
X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
$P2_0$-$P2_3$ $P2_0/P_{\overline{STB}}$ $P2_1P_{TOUT}$	4-bit latched tri-state output Port 2 (active high). Line $P2_0$ is also shared with P_{STB}, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with P_{TOUT}, the timer-out F/F signal (active high).
$P1_0$-$P1_3$	4-bit input/tri-state output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0/P_{STB}$ pulse.
$P3_0$-$P3_3$	4-bit input/latched tri-state output Port 3 (active high).
$P7_0$-$P7_3$	4-bit input/latched tri-state output Port 7 (active high).
RESET	RESET input (active high). R/C circuit or pulse initializes S7507 or S7508 after power-up.
CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
$P0_0/INT_0$ $P0_1/\overline{SCK}$ $P0_2/SO$ $P0_3/SI$	4-bit input Port 0/Serial I/O interface (active high). This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial input SI (active high), Serial Output SO (active low), and the Serial Clock SCK (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_0 (active high) which is a rising edge-triggered interrupt.

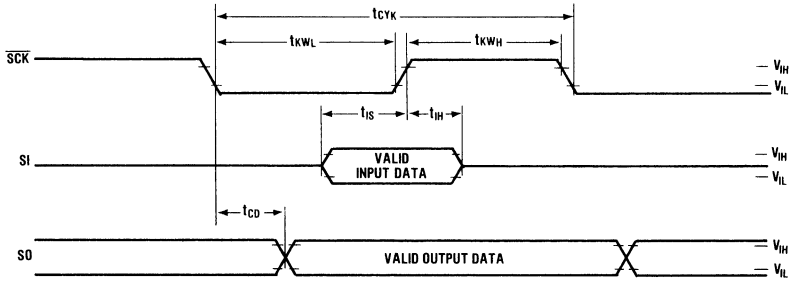
Pin Names (Continued)

Symbol	Function
$P6_0P6_3$	4-bit input/latched tri-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
$P5_0P5_3$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
$P4_0$-$P4_3$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
V_{SS}	Ground.

Timing Waveforms — Clocks

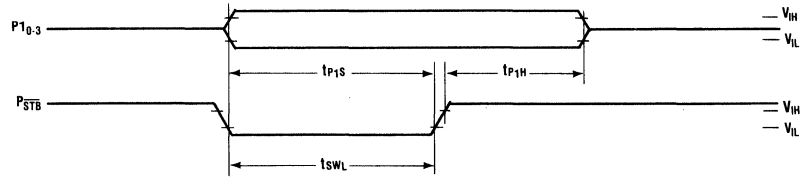


Timing Waveforms — Serial Interface

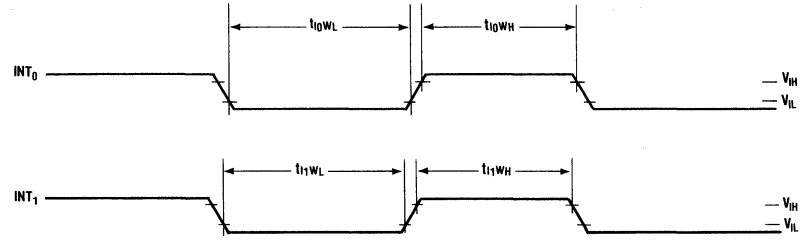


S7500 FAMILY

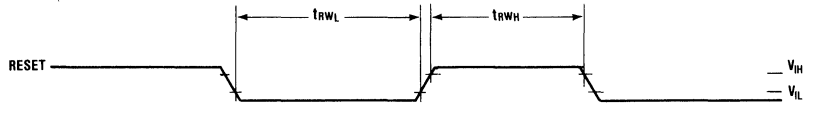
Timing Waveforms — Output Strobe



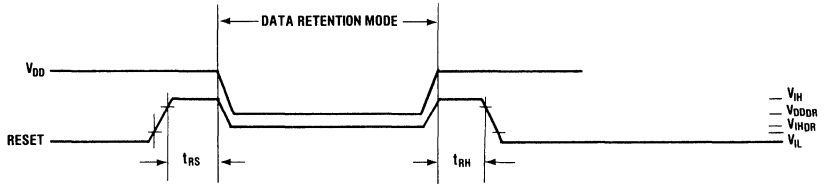
Timing Waveforms — External Interrupts



Timing Waveforms — Reset



Timing Waveforms — Data Retention Mode



CMOS 4-BIT SINGLE CHIP MICROCOMPUTER WITH VACUUM FLUORESCENT DISPLAY CONTROLLER/DRIVER

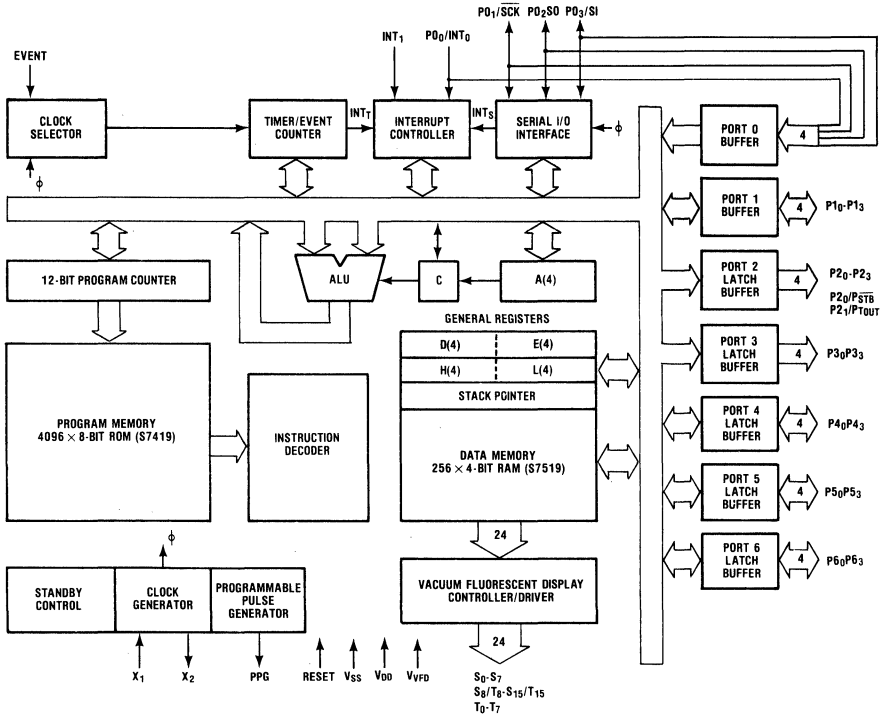
Functional Description

The S7519 is a CMOS 4-bit single chip microcomputer which has the 750x architecture.

The S7519 contains a 4096 x 8-bit ROM, and a 256 x 4-bit RAM.

The S7519 contains four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The S7519 typically executes 92 instructions of the S7500 series "A" instruction set with a 10μs instruction cycle time.

Block Diagram



Functional Description (Continued)

The S7519 has two external and two internal edge-triggered hardware vectored interrupts. It also contains an 8-bit timer/event counter, and an 8-bit serial interface, and a 9-bit D/A programmable pulse generator, to help reduce software requirements. The on-board vacuum fluorescent display controller/driver supervises all of the timing required by the 24 Port S segment drivers either for a 16-digit 7-segment vacuum fluorescent display, or for an 8-character 14-segment vacuum fluorescent display.

The S7519 provides 24 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit output Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, and 6. Additionally, Port 1 can be automatically expanded to 16 I/O lines through connection to a S82C43. The S7519 is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes.

Pin Names

Symbol	Function
NC	No connection.
$P3_3$-$P3_0$	4-bit latched tristate output Port 3 (active high).
$P3_3$/SI $P0_2$/SO $P0_1$/$\overline{SCK}$ $P0_0$/INT_0	4-bit input Port 0/serial I/O interface (active high). This port can be configured either as a parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active high), and the Serial Clock SCK (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_0, which is a rising edge-triggered interrupt.
$P6_3$-$P6_0$	4-bit input/latched tristate output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
$P5_3$-$P5_0$	4-bit input/latched tristate output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
$P4_3$-$P4_0$	4-bit input/latched tristate output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
X_2, X_1	Crystal clock input (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for system clock operation. Alternatively, an extrnal clock source may be connected to input X_1 while output X_2 is left open.
V_{SS}	Ground.
V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
RESET	RESET input (active high). R/C circuit or pulse initializes S7502 or S7503 after power-up.
$P1_3$-$P1_0$	4-bit input/latched tristate output Port 1 (active high).
$P2_3$-$P2_0$ $P2_0$/$P_{\overline{STB}}$ $P2_1$/P_{TOUT}	4-bit latched output Port 2 (active high). Line $P2_0$ is also shared with P_{STB}, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with P_{TOUT}, the timer-out F/F signal (active high).
PPG	1-bit programmable pulse generator output (active high).
Event	1-bit external event input for timer/event counter (active high).
V_{VFD}	Vacuum fluorescent display power supply negative. Apply single voltage between V_{DD} −35.0 and V_{DD} for proper display operation.
S_0-S_7 S_8/T_8-S_{15}/T_{15} T_0-T_7	Vacuum fluorescent display outputs (active high). S_0-S_7 are always segment driver outputs, and T_0-T_7 are always digit driver outputs. S_8/T_8-S_{15}/T_{15} can be configured as either segment driver outputs or as digit driver outputs under control of the display mode select register.

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S7800 Family

S7800 Family Selection Guide

S78C06	CMOS High-End 8-Bit Single Chip Microcomputer
S7811	High-End Single Chip 8-Bit Microcomputer With A/D Converter

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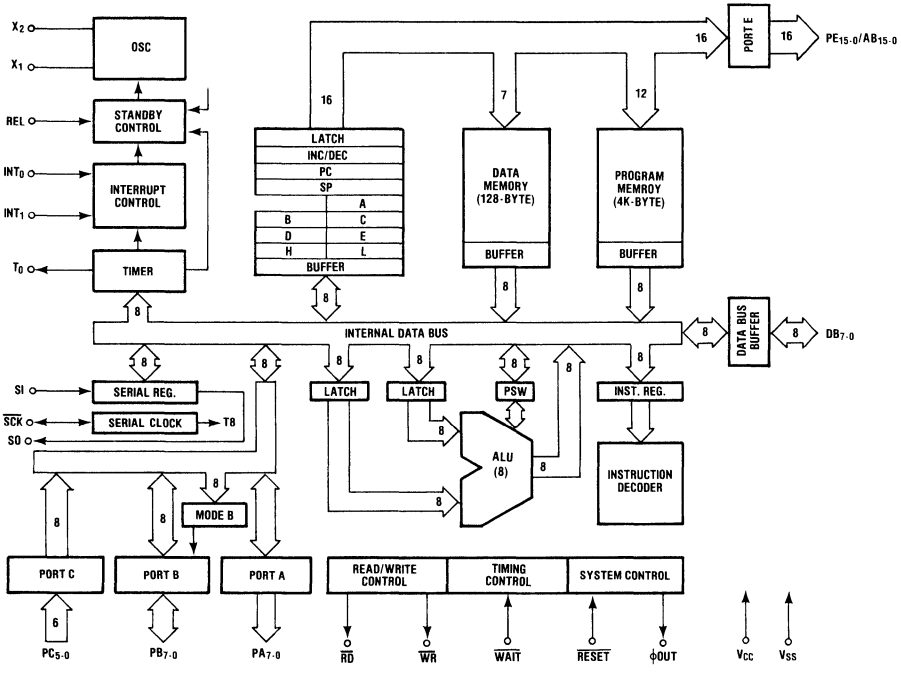
S78C06

CMOS HIGH END 8-BIT SINGLE CHIP MICROCOMPUTER

Features

- ☐ CMOS Silicon Gate Technology + 5V Supply
- ☐ Complete Single Chip Microcomputer
  - — 8-bit ALU
  - — 4K ROM
  - — 256 Bytes RAM
- ☐ Low Power Consumption
- ☐ 46 I/O Lines
- ☐ Expansion Capabilities
  - — 8080A Bus Compatible
  - — 60K Bytes External Memory Address Range
- ☐ Serial I/O Port
- ☐ 101 Instruction Set
  - — Multiple Address Modes
- ☐ Power Down Modes
  - — Halt Mode
  - — Stop Mode
- ☐ 8-Bit Timer
- ☐ Prioritized Interrupt Structure
  - — 2 External
  - — 1 Internal
- ☐ On Chip Clock Generator

Block Diagram



S7800 FAMILY

Functional Description

The AMI S78C06 is an advanced CMOS 8-bit general purpose single chip microcomputer intended for applications requiring 8-bit microprocessor control and extremely low power consumption; ideally suited for portable, battery-powered/backed-up products. The S78C06 integrates an 8-bit ALU, 4K ROM, 128 bytes RAM, 46 I/O lines, an 8-bit timer, and a serial I/O port on a single die. Fully compatible with the 8080A bus structure, expanded system operation can easily be implemented using industry standard peripheral and memory components. Total memory space can be increased to 64K bytes.

The S78C06 lends itself well to low power, portable applications by featuring two power down modes to further conserve power when the processor is not active.

Pin Names

Symbol	Function
PA_{7-0}, PB_{7-0}, PC_{5-0}, PE_{15-0}	I/O Ports
DB_{7-0}	Data Bus
WAIT	Wait Request
INT_0-INT_1	Interrupt Request
X_2-X_1	Xtal
SCK	Serial Clock Input/Output
SI	Serial Input
SO	Serial Output
RESET	Reset
RD	Read Strobe
WR	Write Strobe
ϕout	Clock Output

Table 4-1. HALT Mode and STOP Mode

Function	Halt Mode	Stop Mode
Oscillator	Run	Stop
Internal System Clock	Stop	
Timer	Run	
TIMER REG	Hold	Set
UPCOUNTER, PRESCALER 0, 1	Run	Cleared
Serial Interface		Run (1)
Serial Clock	Hold	Hold
Interrupt Control Circuit	Run	Stop
Interrupt Enable Flag	Hold	Reset
INT_0, INT_1 Input	Active	Inactive
INTT		—
T_8 (INTFS)		—
MASK Register	Hold	Set
Pending Interrupts (INTFX)		Reset
REL Input	Inactive	Active
RESET Input	Active	
On-Chip RAM	Hold	Hold
Output Latch in Port A, B, E		
Program Counter (PC)		Cleared
Stack Pointer (SP)		Unknown
General Registers (A, B, C, D, E, F, L)		
Program Status Word (PSW)		Reset
Mode B-Register		Hold
Standby Control Register(SC_0-SC_3)		
Standby Control Register (SC_4)		Set
Timer Mode Register (TMM_{0-1})		Hold
Timer Mode Register (TMM_1)		Set
Serial Mode Register (SM)		Hold
Data Bus (DB_{0-7})	High-Z	High-Z
RD, WR Output	High	High

Note: Serial clock counter is running and T_8 is generated; however, there are no effects by it.

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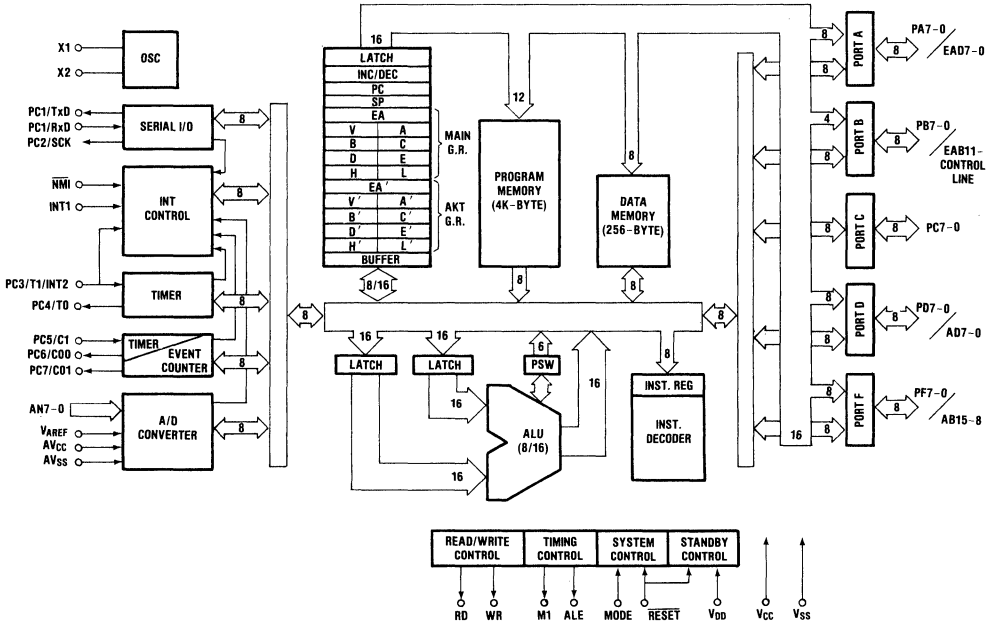
S7811

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH A/D CONVERTER

Features

- ☐ NMOS Silicon Gate Technology Requiring +5V Supply
- ☐ Complete Single Chip Microcomputer
  - 16-Bit ALU
  - 4K ROM
  - 256 Bytes RAM
- ☐ 44 I/O Lines
- ☐ Two Zero-Cross Detect Inputs
- ☐ Expansion Capabilities
  - 8085A Bus Compatible
  - 60K Bytes External Memory Address Range
- ☐ 8-Channel, 8-Bit A/D Converter
  - Auto Scan
  - Channel Select
- ☐ Full Duplex USART
  - Synchronous and Asynchronous
- ☐ 153 Instruction Set
  - 16-Bit Arithmetic, Multiply and Divide
- ☐ 1μs Instruction Cycle Time
- ☐ Prioritized Interrupt Structure
  - 2 External
  - 4 Internal
- ☐ Standby Function
- ☐ On-Chip Clock Generator

Block Diagram



S7800 FAMILY

Description

The AMI S7811 is a high performance single chip microcomputer integrating sophisticated on-chip peripheral functionality normally provided by external components. The device's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing make the S7811 appropriate in data processing as well as control applications. The device integrates a 16-bit ALU, 4K ROM, 256 Bytes RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART and two zero-cross detect inputs on a single die, to direct the device into fast, high-end processing applications involving analog signal interface and processing.

The S7811 is the mask-ROM high volume production device embedded with custom customer program. The S7810 is a ROM-less version for prototyping and small volume production.

Input/Output

8 Analog Input Lines

44 Digital I/O Lines — Five 8-Bit Ports (Port A, Port B, Port C, Port D, Port F) and 4 Input Lines (AN_{4-7})

1. Analog Input Lines — AN_{0-7} are configured as analog input lines for on-chip A/D converter.
2. Port Operation
   — Port A, Port B, Port C, Port F — Each line of these ports can be individually programmed as an input or as an output.
   — Port D — Port D can be programmed as a byte input or a byte output.
   — AN_{4-7} — In addition to the analog input lines, AN_{4-7} can be used as digital input lines for falling edge detection.
3. Control Lines — Under software control, each line of Port C can be configured individually to provide control lines for serial interface, Timer and Timer/Counter.
4. Memory Expansion — In addition to the single-chip operation mode the S7811 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

Table 1.

Memory Expansion	Port Configuration
Non	Port D — I/O Port Port F — I/O Port
256 Bytes	Port D — Multiplexed Address/Data Bus Port F — I/O Port
4K Bytes	Port D — Multiplexed Address/Data Bus Port F0-3 — Address Bus Port F4-7 — I/O Port
16K Bytes	Port D — Multiplexed Address/Data Bus Port F0-5 — Address Bus Port F6, 7 — I/O Port
60K Bytes	Port D — Multiplexed Address/Data Bus Port F — Address Bus

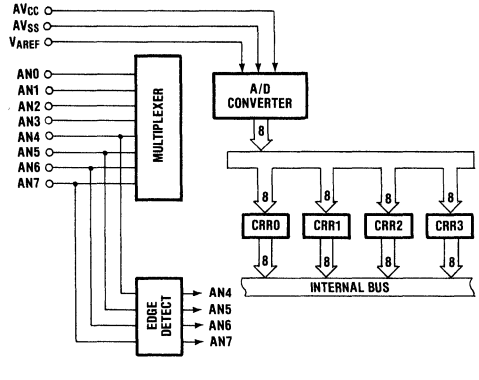
8-Bit A/D Converter

8 Input Channels
4 Conversion Result Registers
2 Powerful Operation Modes
  Auto Scan Mode
  Channel Select Mode
Successive Approximation Technique

Absolute Accuracy	± 1.5 LSB (± 0.6%)
Conversion Range	0 ∼ 5V
Conversion Time	50μs

Interrupt Generation

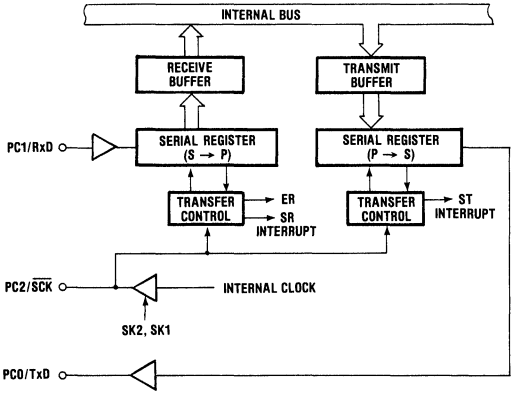
A/D Converter Block Diagram



Universal Serial Interface

- —Full-Duplex, Double Buffering
- — Synchronous Operation Mode
  - Search Mode
  - Receive Mode
- — Asynchronous Operation Mode
  - 7, 8-Bits/Character
  - Start/Stop Bit
  - Even/Odd Parity
  - Programmable Clock Rate x1, x16, x64
- — I/O Expansion Mode (S7801 Serial Mode)
- — Programmable Communication Rate
  - 2μs, 32μs, Timer 1 and External
- — Interrupt Generation

Universal Serial Interface Block Diagram



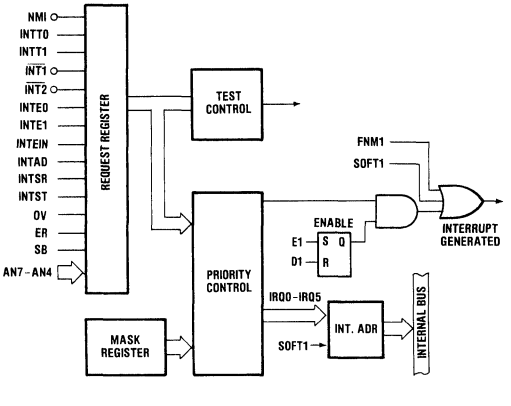
Interrupt Structure

- — 11 Interrupt Sources
- — 6 Priority Levels
- — Non-maskable Interrupt Capability — NMI
- — Individual Request Mask Capability — Except NMI

Table 2.

Interrupt Request	Interrupt	Type of Interrupt	In/Ext
IRQ0	4	NMI (Non-maskable interrupt)	External
IRQ1	8	INTT0 (Coincidence signal from timer 0) INT1 (Coincidence signal from timer 1)	Internal
IRQ2	16	INT1 (Maskable interrupt) INT2 (Maskable interrupt)	External
IRQ3	24	INTE0 (Coincidence signal from timer/event counter) INTE1 (Coincidence signal from timer/event counter)	Internal
IRQ4	32	INTEIN (Falling signal of C1 and T0 counter) INTAD (A/D converter interrupt)	In/External
IRQ5	40	INTSR (Serial receive interrupt) INST (Serial send interrupt)	Internal

Interrupt Structure Block Diagram



S7800 FAMILY

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Future Products

Communication Products

S2579	BCD Input DTMF Generator
S3527	16 Tap Analog Transversal Filter With 9-Bit Tap Control. Designed for Equalizing Band Signals.
S3529	Programmable High Pass Filter
S35213	212A Modulator-Demodulator

Consumer Products

S4520	30-Volt Dichroic LCD Driver

ROMs

680XX	High Speed Family of NMOS ROMs Including 32K, 64K Bi-Polar PROM Pin-Outs

Semi-Custom Products

	Two Micron Family of Gate Arrays and Standard Cells
	1.25 Micron Family of Gate Arrays and Standard Cells

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Application Note Summary

Communications Products

S2559 DTMF Tone Generator

Describes design considerations, test methods, and results obtained using the S2559 Tone Generator family in DTMF pushbutton telephones. Interface with type 500 and 2500 networks are discussed. Use in ancillary equipment is also covered.

Consumer Products

MOS Music

MOS Music is a primer on the application of standard MOS/LSI circuits in creating electronic music. This note discusses the key elements of music production in an electronic organ.

S6800 Family

A Minimal S6802/S6846 Systems Design

Details how to make an S6802/S6846 version of the EVK in a minimal systems application.

S68045 Compared with Motorola MC 6845

Describes the fundamental differences between the two devices.

S9900 Family

S9900 Minimum System Design with the S9900 16-Bit Microprocessor

This design uses just the CPU, a 1K ROM, a 2K RAM, a clock and six smaller IC's.

S9900 Controlled Dot Matrix Printer

S9900 shows how to control a 7040 series dot matrix printer in a minimal systems application.

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General Information

Guide to MOS Handling

At AMI we are continually searching for more effective methods of providing protection for MOS devices. Present configurations of protective devices are the result of years of research and review of field problems.

Although the oxide breakdown voltage may be far beyond the voltage levels encountered in normal operation, excessive voltages may cause permanent damage. Even though AMI has evolved the best designed protective device possible, we recognize that it is not 100% effective.

A large number of failed returns have been due to misapplication of biases. In particular, forward bias conditions cause excessive current through the protective devices, which in turn will vaporize metal lines to the inputs. **Careful inspection of the device data sheets and proper pin designation should help reduce this failure mode.**

Gate ruptures caused by static discharge also account for a large percentage of device failures in customers' manufacturing areas. **Precautions should be taken to minimize the possibility of static charges occurring during handling and assembly of MOS circuits.**

To assist our customers in reducing the hazards which may be detrimental to MOS circuits, the following guidelines for handling MOS are offered. **The precautions listed here are used at AMI.**

1. All benches used for assembly or test of MOS circuits are covered with conductive sheets. WARNING: Never expose an operator directly to a hard electrical ground. For safety reasons, the operator must have a resistance of at least 100K Ohms between himself and hard electrical ground.
2. All entrances to work areas have grounding plates on door and/or floor, which must be contacted by people entering the area.
3. Conductive straps are worn inside and outside of employees' shoes so that body charges are grounded when entering work area.
4. Anti-static neutralized smocks are worn to eliminate the possibility of static charges being generated by friction of normal wear. Two types are available; Dupont anti-static nylon and Dupont neutralized 65% polyester/ 35% cotton.
5. Cotton gloves are worn while handling parts. Nylon gloves and rubber finger cots are not allowed.
6. Humidity is controlled at a minimum of 35% to help reduce generation of static voltages.
7. All parts are transported in conductive trays. Use of plastic containers is forbidden. Axial leaded parts are stored in conductive foam, such as Velofoam#7611.
8. All equipment used in the assembly area must be thoroughly grounded. Attention should be given to equipment that may be inductively coupled and generate stray voltages. Soldering irons must have grounded tips. Grounding must also be provided for solder posts, reflow soldering equipment, etc.
9. During assembly of ICs to printed circuit boards, it is advisable to place a grounding clip across the fingers of the board to ground all leads and lines on the board.
10. Use of carpets should be discouraged in work areas, but in other areas may be treated with anti-static solution to reduce static generation.
11. MOS parts should be handled on conductive surfaces and the handler must touch the conductive surface **before** touching the parts.
12. In addition, no power should be applied to the socket or board while the MOS device is being inserted. This permits any static charge accumulated on the MOS device to be safely removed before power is applied.
13. MOS devices should not be handled by their leads unless absolutely necessary. If possible, MOS devices should be handled by their packages as opposed to their leads.
14. In general, materials prone to static charge accumulation should not come in contact with MOS devices.

These precautions should be observed even when an MOS device is suspected of being defective. The true cause of failure cannot be accurately determined if the device is damaged due to static charge build-up.

It should be remembered that even the most elaborate physical prevention techniques will not eliminate device failure if personnel are not fully trained in the proper handling of MOS.

This is a most important point and should not be overlooked.

More information can be obtained by contacting the Product Assurance Department.

American Microsystems, Inc.
3800 Homestead Road
Santa Clara, California 95051
Telephone (408) 246-0330
TWX 910-338-0024 or 910-338-0018

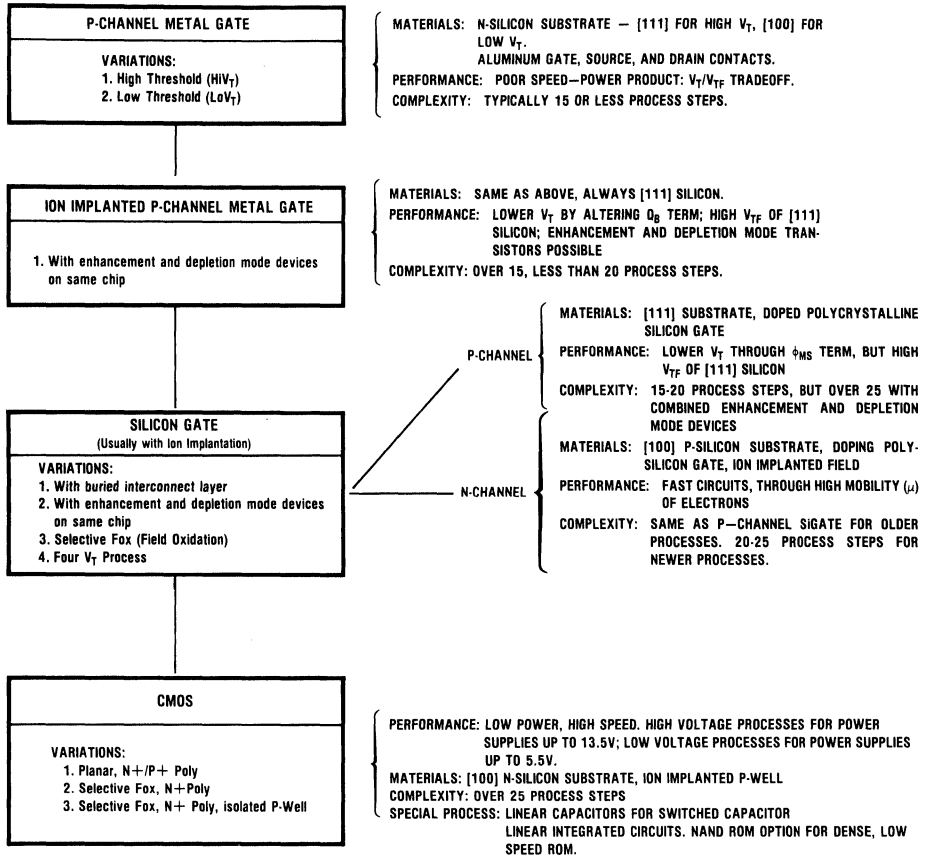
Process Descriptions

Each of the major MOS processes is described on the following pages. First, the established production proven processes are described, followed by those advanced processes, which are starting to go into volume production now. In each case, the basic processes is described first, followed by an explanation of its advantages, applications, etc.

P-Channel Metal Gate Process

Of all the basic MOS processes, P-Channel Metal Gate is the oldest and the most completely developed. It has served as the foundation for the MOS/LSI industry and still finds use today in some devices. Several versions of this process have evolved since its earliest days. A thin slice (8 to 10 mils) of lightly doped N-type silicon wafer serves as the substrate or body of the MOS transistor. Two closely spaced, heavily doped P-type regions, the source and drain, are formed within the substrate by selective diffusion of an impurity that provides holes as majority electrical carriers. A thin deposited layer of aluminum metal, the gate, covers the area between the source and drain regions, but is electrically insulated from the substrate by a thin layer (1000-15000A) of silicon dioxide. The P-Channel transistor is turned on by a negative gate voltage and conducts current between the source and the drain by means of holes as the majority carriers.

Figure B.1. Summary of MOS Process Characteristics



The basic P-Channel metal gate process can be subdivided into two general categories: **High-threshold and low-threshold.** Various manufacturers use different techniques (particularly so with the low threshold process) to achieve similar results, but the difference between them always rests in the threshold voltage V_T required to turn a transistor on. The high threshold V_T is typically -3 to -5 volts and the low threshold V_T is typically -1.5 to -2.5 volts.

The original technique used to achieve the difference in threshold voltages was by the use of substrates with different crystalline structures. The high V_T process used [111] silicon whereas, the low V_T process used [100] silicon. The difference in the silicon structure causes the surface charge between the substrate and the silicon dioxide to change in such a manner that it lowers the threshold voltages.

One of the main advantages of lowering V_T is the ability to interface the device with TTL circuitry. However, the use of [100] silicon carries with it a distinct disadvantage also. Just as the surface layer of the [100] silicon can be inverted by a lower V_T, so it also can be inverted at other random locations—through the thick oxide layers—by large voltages that may appear in the metal interconnections between circuit components. This is undesirable because it creates parasitic transistors, which interfere with circuit operation. The maximum voltage that can be carried in the interconnections is called the parasitic field oxide threshold voltage V_{TF}, and generally limits the overall voltage at which a circuit can operate. This, then, is the main factor that limits the use of the [100] low V_T process. A drop in V_{TF} between a high V_T and low V_T process may, for example, be from -28V to -17V.

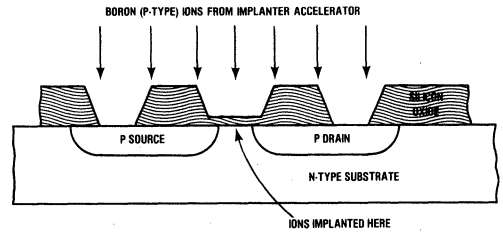
The low V_T process, because of its lower operating voltages, usually produces circuits with a lower operating speed than the high V_T process, but is easier to interface with other circuits, consumes less power, and therefore is more suitable for clocked circuits. Both P-Channel metal gate processes yield devices slower in speed than those made by other MOS processes, and have a relatively poor speed/power product. Both processes require two power supplies in most circuit designs, but the high V_T process, because it operates at a high threshold voltage, has excellent noise immunity.

Ion Implanted P-Channel Metal Gate Process

The P-Channel Ion Implanted process uses essentially the same geometrical structure and the same materials as the high V_T P-Channel process, but includes the ion implantation step. The purpose of ion implantation is to introduce P-type impurity ions into the substrate in the limited area under the gate electrode. By changing the characteristics of the substrate in the gate area, it is possible to lower the threshold voltage V_T of the transistor, without influencing any other of its properties.

Figure B.2. shows the ion implantation step in a diagrammatic manner. It is performed after the gate oxide is grown, but before the source, gate, and drain metallization deposition. The wafer is exposed to an ion beam which penetrates through the thin gate oxide layer and implants ions into the silicon substrate. Other areas of the substrate are protected both by the thicker oxide layer and sometimes also by other masking means. Ion implantation can be used with any process and, therefore could, except for the custom of the industry, be considered a special technique, rather than a process in itself.

Figure B.2. Diagram of Ion Implantation Step



The implantation of P-type ions into the substrate, in effect, reduces the effective concentration of N-type ions in the channel area and thus lowers the V_T required to turn the transistor on. At the same time, it does not alter the N-type ion concentration elsewhere in the substrate and therefore, does not reduce the parasitic field oxide threshold voltage V_{TF} (a problem with the low V_T P-Channel Metal Gate process, described above). The [111] silicon usually is used in ion-implanted transistors.

In fact, if the channel area is exposed to the ion beam long enough, the substrate in the area can be turned into P-type silicon (while the body of the substrate still remains N-type) and the transistor becomes a depletion mode device. In any circuit some transistors can be made enhancement type, while others are depletion type, and the combination is a very useful circuit design tool.

The Ion-Implanted P-Channel Metal Gate process is very much in use today. Among all the processes, it represents a good optimization between cost and performance and thus is the logical choice for many common circuits, such as memory devices, data handling (communication) circuits, and others.

Because of its low V_T, it offers the designer a choice of using low power supply voltages to conserve power or increase supply voltages to get more driving power and thus increase speed. At low power levels it is more feasible to implement clock generating and gating circuits on the chip. In most circuit designs only a single power supply voltage is required.

N-Channel Process

Historically, N-Channel process and its advantages were known well at the time when the first P-Channel devices were successfully manufactured; however, it was much more difficult to produce N-Channel. One of the main reasons was that the polarity of intrinsic charges in the materials combined in such a way that a transistor was on at 0V and had a V_T of only a few tenths of a volt (**positive**). Thus, the transistor operated as a marginal depletion mode device without a well-defined **on/off** biasing range. Attempts to raise V_T by varying gate oxide thickness, increasing the substrate doping, and back biasing the substrate, created other objectionable results and it was not until research into materials, along with ion implantation, silicon gates, and other improvements came about that N-Channel became practical for high density circuits.

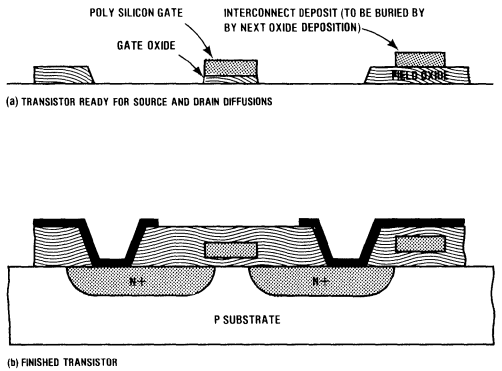
The N-Channel process gained its strength only after the P-Channel process, ion implantation, and silicon gate all were already well developed. N-Channel went into volume productions with advent of the 4K dynamic RAM and the microprocessor, both of which required speed and high density. Because P-Channel processes were nearing their limits in both of these respects, N-Channel became the logical answer.

The N-Channel process is structurally different from any of the processes described so far, in that the source, drain, and channel all are N-type silicon, whereas the body of the substrate is P-type. Conduction in the N-Channel is by means of electrons, rather than holes.

The main advantage of the N-Channel process is that the mobility of electrons is about three times greater than that of holes and, therefore, N-Channel transistors are faster than P-Channel. In addition, the increased mobility allows more current flow in a channel of any given size, and therefore N-Channel transistors can be made smaller. The positive gate voltage allows an N-Channel transistor to be completely compatible with TTL.

Although metal gate N-Channel processes have been used, the predominant N-Channel process is a silicon gate process. Among the advantages of silicon gate is the possibility of a buried layer of interconnect lines, in addition to the normal aluminum interconnnections deposited on the surface of the chip. This gives the circuit designer more latitude in layout and often allows the reduction of the total chip size. Because the polysilicon gate electrode is deposited in a separate step, after the thick oxide layer is in place, the simultaneous deposition of additional polysilicon interconnect lines is only a matter of masking. These interconnect lines are buried by later steps, as shown in Figure B.3.

Figure B.3. Crossection of an N-Channel Silicon Gate MOS Transistor



One minor limitation associated with the buried interconnect lines is their location. Because the source and drain diffusions are done after the polysilicon is deposited [see (a) of Figure B.3] the interconnect lines cannot be located over these diffusion regions.

A second advantage of a silicon gate is associated with the reduction of overlap between the gate and both the source and drain. This reduces the parasitic capacitance at each location and improves speed, as well as power consumption characteristics. Whereas in the metal gate process, the P region source and drain diffusion must be done prior to deposition of the gate electrode, in silicon gate process, the electrode is in place during diffusion, see (a) of Figure B.3. Therefore, no planned overlap for manufacturing tolerance purposes need exist and the gate is said to be **self-aligned**. The only overlap that occurs is due to the normal lateral extension of the source and drain regions during the diffusion process.

The silicon-gate process produces devices that are more compact than metal gate, and are slightly faster because of the reduced gate overlap capacitance. Because the basic silicon gate process is relatively simple, it is also economical. It is a versatile process that is used in memory devices and most any other circuit.

N-Channel development continues at a vigorous pace, resulting in all kinds of process variations, production tech-

niques and applications. The combination of high speed, TTL compatibility, low power requirements, and compactness have already made N-Channel the most widely used process. The cost of N-Channel has been coming down also.

In addition to its use in large memory chips and microprocessors, N-Channel has become a good general purpose process for circuits in which compactness and high speed are important.

CMOS

The basic CMOS circuit is an inverter, which consists of two adjacent transistors—one an N-Channel, the other a P-Channel, as shown in Figure B.4. The two are fabricated on the same substrate, which can be either N or P type.

The CMOS inverter in Figure B.4 is fabricated on an N-type silicon substrate in which a P "tub" is diffused to form the body for the N-Channel transistor. All other steps, including the use of silicon gates and ion implantation, are much the same as for other processes.

The main advantage of CMOS is extremely low power consumption. When the common input to both gate electrodes is at a logic 1 (a positive voltage) the N-Channel transistor is biased on, the P-Channel is off, and the output is near ground potential. Conversely, when the input is at a logic 0 level, its negative voltage biases only the P-Channel transistor on and the output is near the drain voltage $+V_{DD}$. In either case, only one of the two transistors is on at a time and thus, there is virtually no current flow and no power consumption. Only during the transition from one logic level to the other are both transistors on and current flow increases momentarily.

Silicon Gate CMOS is also fast approaching speeds of bipolar TTL circuits. On the other hand, the use of two transistors in every gate makes CMOS slightly more complex and costly, and requires more chip size. For these reasons, the original popularity of CMOS was in SSI logic elements and MSI circuits—logic gates, inverters, small shift registers, counters, etc. These CMOS devices constitute a logic family in the same way as TTL, ECL, and other bipolar circuits do; and in the areas of very low power consumption, high noise immunity, and simplicity of operation, are still widely accepted by discrete logic circuit designers.

Low power CMOS circuits made the watch circuit possible and also have been used in space exploration, battery operated consumer products, and automotive control devices. As experience was gained with CMOS, tighter design rules and reduced device sizes have been implemented and now LSI circuits, such as 1K RAM memories and microprocessors, are being manufactured in volume.

CMOS circuits can be operated on a single power supply voltage, which can be varied from +2.5 to about +13.5 volts with the high voltage processes, with a higher voltage giving more speed and higher noise immunity. Low voltage processes allow single power supply voltages from +1.5 to +5.5 volts.

The first implementation of an inverting gate is a process that uses both n+ to p+ polysilicon. The basic structure is a first-generation approach to which a selective field-oxidation process has been added.

Figure B.5 shows the plan and section views of the three-device gate portion. Because the P-Well in the top view spans both N-Channel devices, it is referred to as ubiquitous, and the process is called Ubiquitous P-Well.

In this planar process, p+ guard rings are used to reduce surface leakage. Polysilicon cannot cross the rings, however, so that bridges must be built. Note the use of p+ polysilicon in the P-Channel areas. The plan view shows the construction of the bridges linking p+ to metal to n+. (Were the process to be used for a low-voltage, first-generation application like a watch circuit, the guard rings would not be necessary and polysilicon could directly connect N-Channel and P-Channel devices; however, to ensure good ohmic contact from one type of polysilicon to another, polysilicon-diode contacts must be capped with metal.)

This process provides a buried contact (n+ polysilicon to n+ diffusion) that can yield a circuit-density advantage. However, neither of the other two second-generation approaches provides buried contacts. Therefore, if a layout in this process is to be compatible with the others, the buried contact must be eliminated. Though there will be a penalty in real estate, the gain for custom applications is a great increase in the number of available CMOS vendors.

The n+-Only Polysilicon Approach

Both of the second-generation CMOS processes that follow are variants of the n+-only, selective-field-oxide approach. One closely resembles the p+ n+ Ubiquitous-P-Well process, since it, too, has a Ubiquitous P-Well that is implanted before the field oxidation and thus runs under the field oxide. The other, called isolated P-Well, has separate wells for each N-Channel device that are implanted after field oxidation.

Figure B.6 shows the section and plan views of the n+-only Ubiquitous-P-Well approach used to build the gate of Figure B.4. This is the 5μm process recommended by AMI and others for new, high-performance CMOS designs. The layout is simpler than with the n+/p+ polysilicon Ubiquitous-Well approach (there are no buried contacts and no polysilicon-diode contacts), and it occupies less area for the same line widths. Also, since the process permits implanting in the field region, no guard rings are required.

Polysilicon can thus cross directly from P- to N-Channel device areas without the need for bridges or polysilicon-dioxide contacts.

A variant of the all n+ (See Figure B.7) polysilicon process just discussed uses basically the selective field-oxide approach except that the P-Wells are not continuous under the field-oxide areas; they are instead bounded by field-oxide edges. Since the P-Wells are naturally isolated from one another, the process is called n+ poly-isolated P-Well. The isolated wells must all be connected to ground; if they are left floating, circuit malfunctions are bound to occur. The grounding is done either with p+ diffusions or with top-side metalization that covers a p+-to-P-Well contact diffusion.

Figure B.4. Crossection and Schematic Diagram of a CMOS Inverter

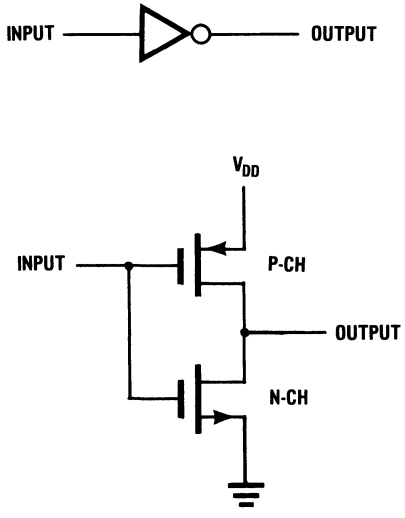
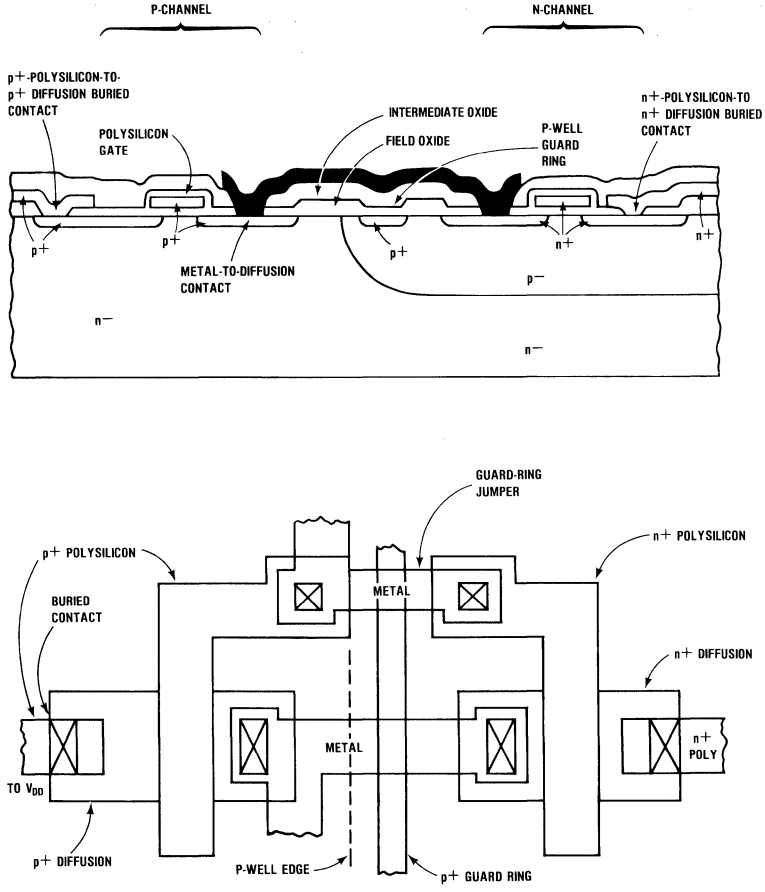
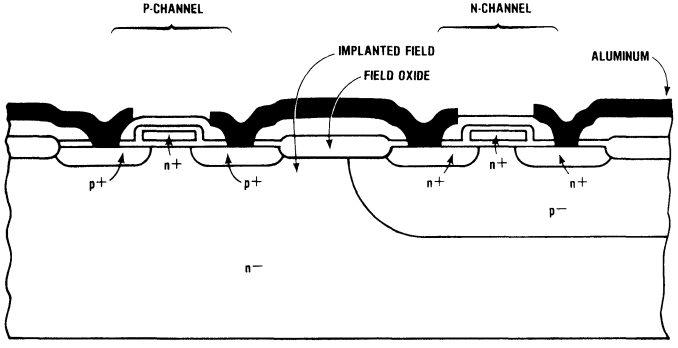


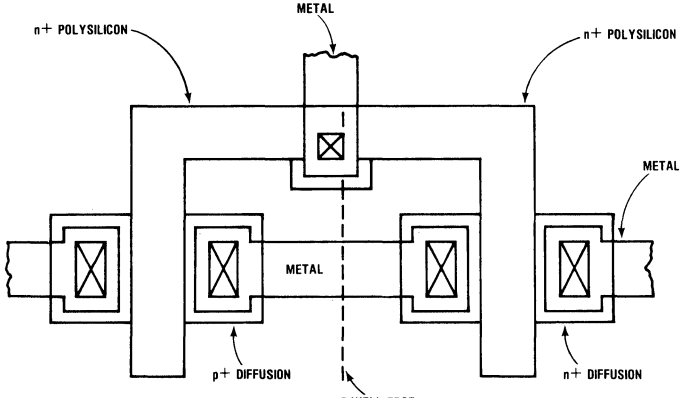
Figure B.5. n + /p + Polysilicon Approach



THE FIRST HIGH-PERFORMANCE COMPLEMENTARY-MOS PLANAR PROCESS. ITS DRAWBACKS: TWO TYPES OF POLYSILICON ARE USED, AND THE UNAVAILABILITY OF FIELD IMPLANT DOPING TIES FIELD THRESHOLD TO DEVICE THRESHOLDS.

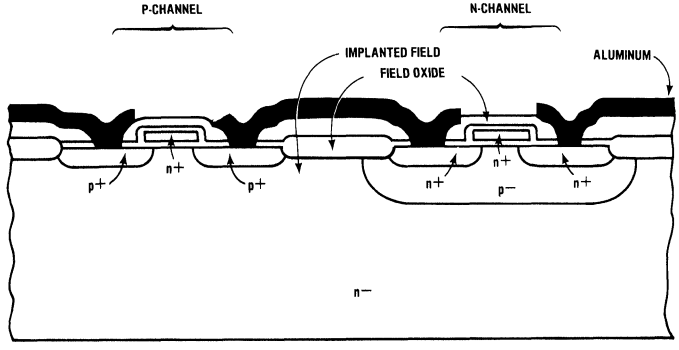
Figure B.6. n + – Only Polysilicon Approach

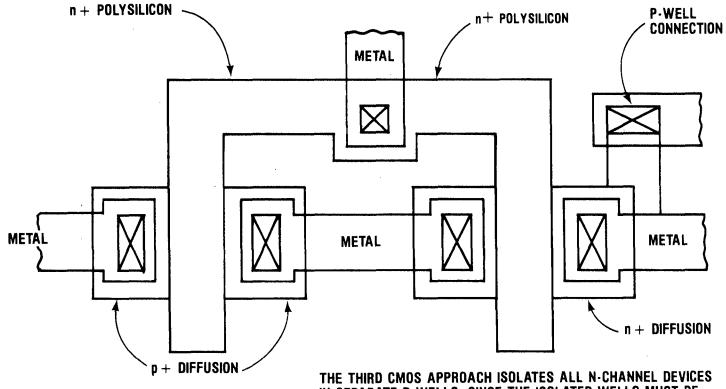




ALL NEW HIGH-PERFORMANCE CMOS CIRCUITS WILL USE ONE TYPE OF POLYSILICON. THIS VERSION HAS A UBIQUITOUS P-WELL: THAT IS, SERIES N-CHANNEL DEVICES SIT IN A COMMON P-WELL, WHICH, IMPLANTED BEFORE FIELD OXIDATION, RUNS UNDER THE FIELD OXIDE. THIS IS AMI'S PREFERRED CMOS PROCESS FORMAT FOR ALL NEW DESIGNS.

Figure B.7. Isolated Wells





THE THIRD CMOS APPROACH ISOLATES ALL N-CHANNEL DEVICES IN SEPARATE P-WELLS, SINCE THE ISOLATED WELLS MUST BE DOPED MUCH MORE HEAVILY THAN THOSE OF THE UBIQUITOUS-WELL APPROACH, n+ -TO P-WELL CAPACITANCE IS GREATER AND SWITCHING SPEEDS LOWER. THIS IS AN n+ -ONLY POLYSILICON PROCESS.

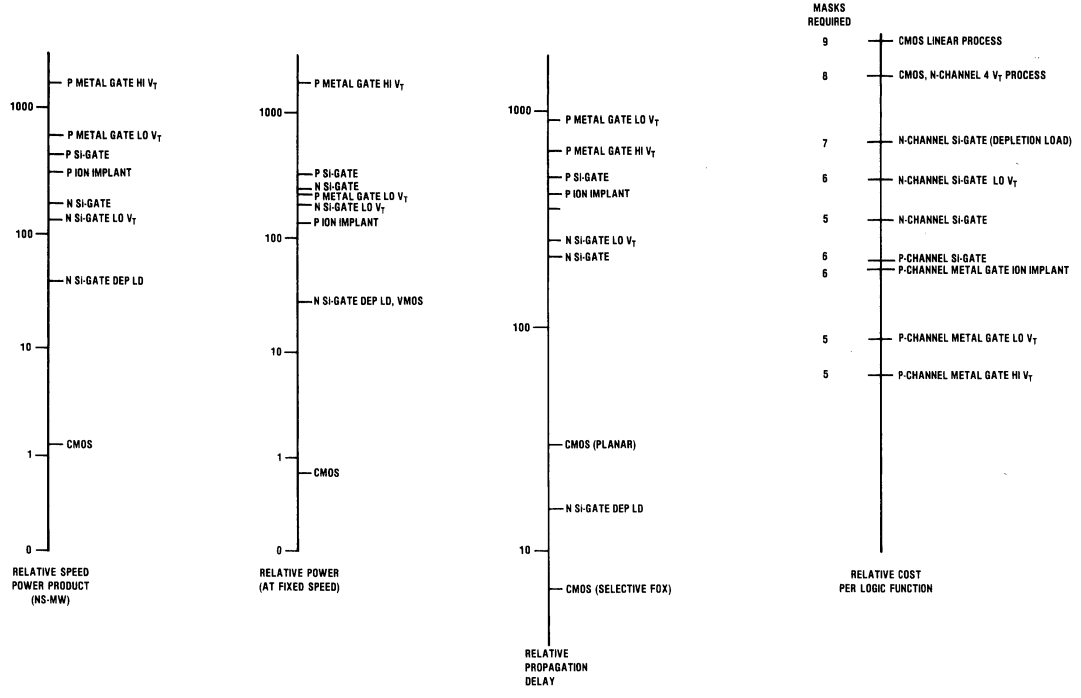
In the Isolated-Well process, the P-Wells must be doped much more heavily than in the Ubiquitous-Well process. One result is a higher junction capacitance between the n+ areas and the wells that both slows switching speeds and raises the power dissipation of a device. Even though the speed loss could be compensated for by slightly shorter channel lengths, the operating power still remains high.

Although currently available from AMI and other manufacturers, the Isolated-Well process is in fact not recommended for new designs by AMI. Its layout takes up more area than does one using the Ubiquitous-Well approach, even though its P-Well to p+-area spacing is slightly less.

Table 1. Layout Compatibility Concerns for CMOS Processes

Layout Feature	n+/p+ Polysilicon Ubiquitous P-Well	n+ – Only Polysilicon Ubiquitous P-Well	n+ – Only Polysilicon Isolated P-Well
Buried Contact	X	No	No
Polysilicon Diode Contact	Yes	X	X
P-Well Isolation With Diffusion Mask	No	No	Yes
Tight P-Well-To-p+ Spacing	No	No	Yes
Layout Care Required For P-Well Electrical Contacts	No	No	Yes

Figure B.8. Comparative Data on Major MOS Processes



7.5 Micron CMOS Process Parameters

	Low V_T		High V_T		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	.55	.85	1.0	1.5	N-Channel Threshold at 1μA 50 x 7.5μ Device (Volts)
V_{TP}	−.4	−.95	−.8	−1.4	P-Channel Threshold at 1μA 50 x 7.5μ Device (Volts)
V_{TF}	8		15		Poly Field Threshold at 1μA 50 x 10μ Device (Volts)
B_{VDSS}	24	—	28	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	30	39	28	33	Diffusion Resistivity Ω/□
N+	9	15	9.1	12.6	Diffusion Resistivity Ω/□
R_{POLY} P+	118	172	80	140	Poly Resistivity Ω/□
N+	30	60	29	39	Poly Resistivity Ω/□
T_{OX}	1300		1200		Gate Oxide Thickness, In Angstroms
X_j P+	1.8*		1.8*		Junction Depth, In μ
N+	2.0*		2.0*		Junction Depth, In μ
Operating Voltage	—	5	5	12	In Volts
Max Rating	—	5.5	—	13.2	In Volts
Process Designator	CTA	CTA	CTE	CTE	

(*Typical)

CMOS I Process Parameters

	General Purpose				Double Poly				NAND ROM				
	High V		Low V		High V		Low V		High V		Low V		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	0.7	1.3	0.5	1.1	0.7	1.3	0.5	1.1	0.7	1.3	0.5	1.1	N-Channel Threshold 50 x 5μ Device (Volts)
V_{TP}	−0.7	−1.3	−0.5	−1.1	−0.7	−1.3	−0.5	−1.1	−0.7	−1.3	−0.5	−1.1	P-Channel Threshold 50 x 5μ Device (Volts)
V_{TF}	17	—	7	—	17	—	7	—	17	—	7	—	Poly Field Threshold (Volts)
B_{VDSS}	17	—	7	—	17	—	7	—	17	—	7	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	15	35	15	35	15	35	15	35	15	35	15	35	Diffusion Resistivity Ω/□
N+	35	80	35	80	35	80	35	80	35	80	35	80	Diffusion Resistivity Ω/□
R_{POLY}	15	45	15	45	15	45	15	45	15	45	15	45	Poly Resistivity Ω/□ (All poly is N+)
T_{OX}	750	850	750	850	750	850	750	850	750	850	750	850	Gate Oxide Thickness, In Angstroms
X_j P+	1.2*		1.2*		1.2*		1.2*		1.2*		1.2*		Junction Depth, In μ
N+	1.5*		1.5*		1.5*		1.5*		1.5*		1.5*		Junction Depth, In μ
Operating Voltage	2.2	13.2	1.5	5.5	2.2	13.2	1.5	5.5	2.2	13.2	1.5	5.5	In Volts
Max Rating	—	13.2	—	5.5	—	13.2	—	5.5	—	13.2	—	5.5	In Volts
Process Designator	CVA	CVA	CVH	CVH	CVB	CVB	CVE	CVE	CVD	CVD	CVC	CVC	

(*Typical)

CMOS II Process Parameters

	Single Metal		Double Metal		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	0.6	1.0	0.6	1.0	N-Channel Threshold (Volts)
V_{TP}	−0.6	−1.0	−0.6	−1.0	P-Channel Threshold (Volts)
V_{TF}	10.0	—	10.0	—	Poly Field Threshold (Volts)
B_{VDSS}	10.0	—	10.0	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	35	80	35	80	Diffusion Resistivity Ω/□
N+	15	40	15	40	Diffusion Resistivity Ω/□
R_{POLY}	15	30	15	30	Poly Resistivity, Ω/□ (All Poly is N+)
T_{OX}	450	550	450	550	Gate Oxide Thickness, In Angstroms
X_j P+	0.3	0.5	0.3	0.5	Junction Depth, In μ
N+	0.3	0.5	0.3	0.5	Junction Depth, In μ
Operating Voltage	5.0	5.0	5.0	5.0	In Volts
Max Rating	—	5.5	—	5.5	In Volts
Process Designator	CCA	CCA	CCD	CCD	

6 & 5 Micron SiGate NMOS Process Parameters

	6 Micron						5 Micron		
	Low V_T		High V_T		16.67/ Process Shrink				
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TE}	0.6	1.0	0.8	1.2	.75	1.25	0.6	1.0	Extrapolated Enhancement Threshold on a 50 x 6μ Transistor (Volts)
V_{TD}	−3.0	−4.0	−2.5	−3.5	−2.5	−3.5	−2.5	−3.5	Extrapolated Depletion Threshold on a 50 x 50μ Transistor (Volts)
V_{TN}	—	—	—	—	—	—	−.2	−.2	Intrinsic Device Threshold 50 x 6μ Transistor (Volts)
V_{TDD}	—	—	—	—	—	—	−4.35	−3.65	Deep Depletion Threshold (Volts)
V_{TF}	13	40	13	40	12	30	10	—	Poly Field Threshold (Volts)
B_{VDSS}	14	—	14	—	12	—	10	—	Drain-Source Breakdown on 50 x 50μ Transistor
R_{DIFF}	8	14	8	14	8	14	8	25	N+ Region Resistivity Ω/□
R_{POLY}	20	40	20	40	20	40	20	40	N+ Doped Poly Resistivity Ω/□
T_{OX}	1000	1150	1000	1150	750	850	750	850	Gate Oxide Thickness, In Angstroms
X_j	1.2	1.6	1.2	1.6	0.8	1.2	0.8	1.2	Junction Depth, In μ
Operating Voltage	5	12	5	12	5	12	5	12	In Volts
Max Rating		13.2		13.2		13.2		13.2	In Volts
Process Designator	NVC	NVC	NVD	NVD	NVS	NVS	NEA/NEC		

NMOS I & NMOS II Process Parameters

	NMOS I				NMOS II				
	$4V_T$		Std.		$4V_T$		Std.		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TE}	0.6	1.0	0.6	1.0	0.6	1.0	0.6	1.0	Extrapolated Enhancement Threshold Voltage on a 50 x 4μ Transistor (4μ Processes) or 50 x 3μ Transistor (3μ Processes) (Volts)
V_{TD}	−3.5	−2.5	−3.5	−2.5	−3.5	−2.5	−3.5	−2.5	Extrapolated Threshold 50 x 50μ Device (Volts)
V_{TN}	−0.15	+0.15	N/A	N/A	−0.15	+0.15	N/A	N/A	Extrapolated Threshold 50 x 6μ Device (Volts)
V_{TDD}	−4.35	−3.65	N/A	N/A	−4.85	−4.15	N/A	N/A	Extrapolated Threshold 50 x 50μ Device (Volts)
V_{TF}	7.5	—	7.5	—	7.5	—	7.5	—	Poly Field Threshold (Volts)
B_{VDSS}	7.5	—	7.5	—	7.5	—	7.5	—	Punch Through Voltage 50 x 4μ Device (4μ Processes) or 50 x 3μ Device (3μ Processes) (Volts)
R_{DIFF}	15	30	15	30	15	30	15	30	Diffusion Resistivity Ω/□
R_{POLY}	20	50	20	50	20	40	20	40	Poly Resistivity Ω/□
T_{OX}	650	750	650	750	450	550	450	550	Gate Oxide Thickness, In Angstroms
X_j	0.3	0.5	0.3	0.5	0.3	0.5	0.3	0.5	N+ Junction Depth, In μ
Operating Voltage	—	5/12	—	5/12	—	5	—	5	In Volts
Max Rating	—	5.5/13.2	—	5.5/13.2	—	5.5	—	5.5	In Volts
Process Designator	NDD	NDD	NDE	NDE	NCC	NCC	NCA	NCA	

7.5 Micron Metal Gate PMOS Process Parameters

	0 Implant						1 Implant		2 Implant		
	High V_T		Med V_T		Low V_T						
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TE}	−3.25	−4.95	−2.8	−4.2	−1.8	−2.5	−1.0	−1.8	−1.2	−2.0	$I_{DS} = 1\mu A$
V_{TD}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	4.0	5.0	Depletion Measurement on a 50μ Transistor (Volts)
V_{TF}	30	—	25	—	17	—	25	—	25	—	Field Threshold (Volts)
B_{VDSS}	30	—	30	—	30	—	22	—	22	—	Drain-Source Breakdown (Volts)
R_{DIFF}	30	60	30	60	30	60	30	60	30	60	Sheet Resistivity Ω/□
I_{DS}/mA	1.25	2.55	0.8	2.2	0.8	2.0	2.8	4.0	2	4	Drain-Source Current (mA)
B_{VOXG}	120	—	80	—	100	—	90	—	90	—	Gate Oxide Breakdown (Volts)
X_jU	1.7	1.9	1.7	1.9	1.7	1.9	1.7	1.9	1.7	1.9	Junction Depth, In μ
Process Designator	PMC	PMC	PMT	PMT	PMD	PMD	PNR	PNR	POG	POG	

Product Assurance Program

Introduction

Quality is one of the most used, least understood, and variously defined assets of the semiconductor industry. At AMI we have always known just how important effective quality assurance, quality control, and reliability monitoring are in the ability to deliver a repeatably reliable product. Particularly, through the manufacture of custom MOS/LSI, experience has proved that one of the most important tasks of quality assurance is the effective control and monitoring of manufacturing processes. Such control and monitoring has a twofold purpose: to assure a consistently good product, and to assure that the product can be manufactured at a later date with the same degree of reliability.

To effectively achieve these objectives, AMI has developed a Product Assurance Program consisting of three major functions:

- Quality Control
- Quality Assurance
- Reliability

Each function has a different area of concern, but all share the responsibility for a reliable product.

The AMI Product Assurance Program

The program is based on MIL-STD-883, MIL-M-38510, and MIL-Q-9858A methods. Under this program, AMI manufactures highest quality MOS devices for all segments of the commercial and industrial market and, under special adaptations of the basic program, also manufactures high reliability devices to full military specifications for specific customers.

The three aspects of the AMI Product Assurance Program—Quality Control, Quality Assurance, and Reliability—have been developed as a result of many years of experience in MOS device design and manufacture.

Quality Control establishes that every method meets or fails to meet, processing or production standards—**QC checks methods.**

Quality Assurance establishes that every method meets, or fails to meet, product parameters—**QA checks results.**

Reliability establishes that QA and QC are effective—**Reliability checks device performance.**

One indication that the AMI Product Assurance Program has been effective is that NASA has endorsed AMI products for flight quality hardware since 1967. The Lunar Landers and Mars Landers all have incorporated AMI circuits, and AMI circuits have also been utilized in the Viking and Vinson programs, as well as many other military airborne and reconnaissance hardware programs.

Quality Control

The Quality Control function in AMI's Product Assurance Program involves constant monitoring of all aspects of materials and production, starting with the raw materials purchased, through all processing steps, to device shipment. There are three major areas of Quality Control:

- Incoming Materials Control
- Microlithography Control
- Process/Assembly Control

Incoming Materials Control

All purchased materials, including raw silicon, are checked carefully to various test and sampling plans. The purpose of incoming materials inspection is to ensure that all items required for the production of AMI MOS circuits meet such standards as are required for the production of high quality, high reliability devices.

Incoming inspection is performed to specifications agreed to by suppliers of all materials. The Quality Control group continuously analyzes supplier performance, performs comparative analysis of different suppliers, and qualifies the suppliers.

Tests are performed on all direct material, including packages, wire, lids, eutectics, and lead frames. These tests are performed using a basic sampling plan in accordance with MIL-S-19500, generally to a Lot Tolerance Percent Defective (LTPD) level of 10%. The AQL must be below 1% overall.

Two incoming material inspection sequences illustrate the thoroughness of AMI Quality Control:

- Purchased packages are first inspected visually. Then, dimensional inspections are performed, followed by a full functional inspection, which subjects the packages to an entire production run simulation. Finally, a full electrical evaluation is made, including checks of the insulation, resistance, and lead-to-lead isolation. A package lot which passes these tests to an acceptable LTPD level is accepted.
- Raw silicon must also pass visual and dimensional checks. In addition, a preferential etch quality inspection is performed. For this inspection, the underlayers of bulk silicon are examined for potential anomalies such as dislocation, slippage or etch pits. Resistivity of the silicon is also tested.

Microlithography Control

Microlithography involves the processes which result in finished working plates, used for the fabrication of wafers. These processes are pattern or artwork generation, photoreduction, and the actual printing of the working plates.

Pattern generation now is the most common practice at AMI. The circuit layout is digitized and stored on a tape, which then is read into an automated pattern generator which prints a highly accurate 10x reticle directly.

In cases where the more traditional method of artwork generation is used whether Rubylith, Gerber Plots, AMI generated or customer generated—the artwork is thoroughly inspected. It is checked for level-to-level registration and dimensional tolerances. Also, a close visual inspection of the workmanship is made. AMI artwork is usually produced at 200x magnification and must con-

form to stringent design rules, which have been developed over a period of years as part of the process control requirements.

Acceptable artwork is photographically reduced to a 20x magnification, and then further to a 10x magnification. The resulting 10x reticles are then used for producing 1x masters. The masters undergo severe registration comparisons to a registration master and all dimensions are checked to insure that reductions have been precise. During this step, image and geometry are scrutinized for missing or faded portions and other possible photographic omissions.

For a typical N-Channel silicon gate device, master sets are checked at all six geometry levels in various combinations against each other and against a proven master set. Allowable deviations within the die are limited to 0.5 micron, deviations within a plate are limited to 1 micron, and all plate deviations are considered cumulatively.

Upon successful completion of a device master set, it is released to manufacturing where the 1x plates are printed. A sample inspection is performed by manufacturing on each 30-plate lot and the entire lot is returned to Quality Control for final acceptance. Quality Control performs audits on each manufacturing inspector daily, by sample inspection techniques.

The plates can be rejected first by manufacturing when the 30-plate lots are inspected, or by Quality Control when the lots are submitted for final acceptance. If either group rejects the plates, they are rescreened and then undergo the same inspection sequence. In the rescreening process, the plates undergo registration checks; visual checks for pin holes, protrusions, and faded or missing images, as well as all critical dimension checks.

Process Control

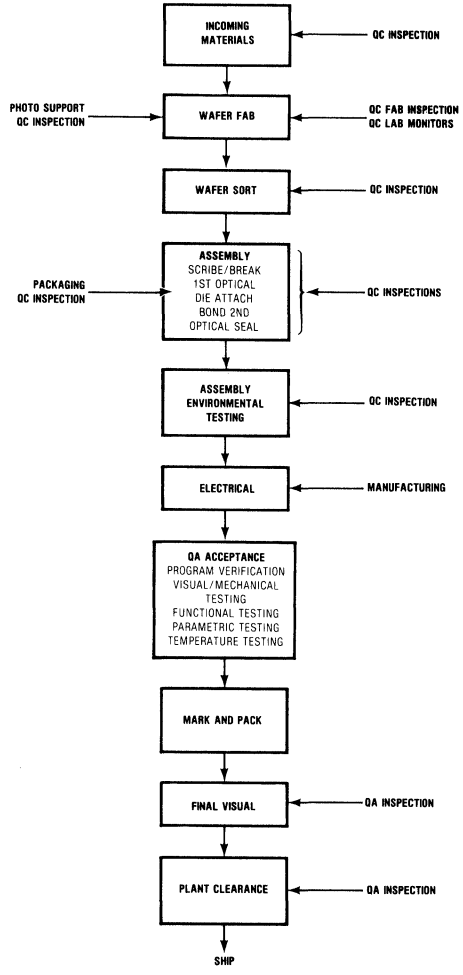
Once device production has started in manufacturing, AMI Quality Control becomes involved in one of the most important aspects of the Product Assurance Program—the analysis and monitoring of virtually all production processes, equipment, and devices.

Process controls are performed in the fabrication area, by the Quality Control Fabrication Group, to assure adherence to specifications. This involves checks on operators, equipment and environment. Operators are tested for familiarity with equipment and adherence to procedure. Equipment is closely checked both through calibration and maintenance audits. Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possibility of contamination or adverse effects due to temperature or humidity excesses.

Experience has proven that such close control of the operators, equipment, and environment is highly effective towards improved quality and increased yields.

In addition to the specification adherence activities of the

Figure 1. Flowchart of Product Assurance Program Implementation



QC Fabrication Group, A QC Laboratory performs constant process monitoring of virtually every step of all processes. Specimens are taken from all production steps and critically evaluated. Sampling frequency varies, depending on the process, but generally, oxidation, diffusion, masking and evaporization are the most closely monitored steps.

Results are supplied both to manufacturing and engineering. When evidence of a problem occurs, QC provides recommendations for corrections and follows up the corrective action taken.

Optical Inspections are performed at several steps; quality control limits are based on a 10% LTPD. The chart in Figure 1 shows process steps and process control points.

Quality Assurance

The Quality Assurance function in the Product Assurance Program involves checking the ability of manufactured parts to meet specifications. In addition, the QA group also is responsible for calibration of all equipment, and for the maintenance of AMI internal product specifications, to assure that they are always in conformance with customer specifications or other AMI specifications.

After devices undergo 100% testing in manufacturing, they are sent to Quality Assurance for acceptance. Lots are defined, and using the product specifications, sample sizes are determined, along with the types of tests to be performed and the test equipment to be used. Lots must pass QA testing to a 0.1% AQL.

Three types of tests are performed on the samples: visual/mechanical, parametric, and functional. All tests are performed both at room temperature and at elevated temperature. In addition, a number of other special temperature tests may be performed if required by the specification.

To perform the tests, QA uses AMI PAFT test systems, ROM test systems, Macrodata testers, Fairchild **Sentry**, LTX **Sentinel, XINCOM** systems, Teradyne test systems, and various bench test units. In special instances a part may also be tested in a real life environment in the equipment which is to finally utilize it.

If a lot is rejected during QA testing, it is returned to the production source for an electrical rescreening. It is then returned to QA for acceptance but is identified as a resubmitted lot. If it fails again, corrective action in engineering is initiated. As evidence of the problem is detected, the parts may also be traced all the way back to the wafer run to analyze the cause.

When a lot is acceptable, it is sent to packaging and then to finished goods. When parts leave finished goods, they are again checked by the QA group to a 10% LTPD with visual/mechanical tests. Also, all supporting documentation for the parts is verified, including QA acceptance, special customer specifications, certificates of compliance, etc. Only after this last check are devices considered ready for plant clearance.

If there are customer returns, they are first sample tested by QA to determine the cause of the return. (Many times an invalid customer test will incorrectly cause returns.) Selected return samples are sent to Reliability for failure analysis.

Reliability

The Reliability function in the Product Assurance Program involves process qualification, device qualification, package qualification, reliability program qualification and failure analysis. To perform these functions AMI Reliability group is organized into two major areas:

- Reliability Laboratory
- Failure Analysis

Reliability Laboratory

AMI Reliability Laboratory is responsible for the following functions.

- New Process Qualification
- Process Change Qualification
- Process Monitoring
- New Device Qualification
- Device Change Qualification
- New Package Qualification
- Device Monitoring
- Package Change Qualification
- Package Monitoring
- High Reliability Programs

There are various closely interrelated and interactive phases involved in the development of a new process, device, package or reliability program. A process change may affect device performance, a device change may affect process repeatability, and a package change may affect both device performance and process repeatability. To be effective, the Reliability Laboratory must monitor and analyze all aspects of new or changed processes, devices, and packages. It must be determined what the final effect is on product reliability, and then evaluate the merits of the innovation or change.

Process Qualification

For example, AMI Research and Development group recommends a new process or process alteration when it feels that the change can result in product improvement. The Reliability Laboratory then performs appropriate environmental and electrical evaluations of a new process. Typically, a special test vehicle, or "rel chip", generated by R&D during process development, is used to qualify the recommended new process or process change.

The rel chip is composed of circuit elements similar to those that may be required under worst-case circuit design conditions. The rel chip elements are standard for any given process, and thus allow precise comparisons between diffusion runs. The following is an example of what is included on a typical rel chip:

- A discrete inverter and an MOS capacitor

- A large P-N junction covered by an MOS capacitor.
- A large P-N junction area (identical to the junction area above, but without the MOS capacitor)
- A large area MOS capacitor over substrate
- Several long contact strings with different contact geometries
- Several long conductor geometries, which cross a series of eight deeply etched areas

Each circuit element of a rel chip allows a specific test to be performed. As an example, the discrete inverter and MOS load device accommodate power life tests. As a consequence, any type of parameter drift can be observed. The MOS capacitor, covering the large P-N junction, can serve to indicate the presence of contamination in the oxide, under the oxide, or in the bulk silicon. If unusual drift is evidenced, the location of contamination can be determined through analysis of the additional MOS capacitor and the large P-N junction area. The metal conductor interconnecting contacts is useful for life testing under relatively high current conditions. It facilitates the detection of metal separation when moisture or other contaminants are present.

The conductors crossing deeply etched areas allow the checking of process control. Rather than depending upon optical inspection of metal quality, burned out areas caused by high currents are readily identified and provide a quantitative measure of metal quality.

If the Reliability Laboratory determines that a recommended new process or process change is viable for manufacturing purposes, further analysis is necessary to determine that production devices can be manufactured in high volume, in a repeatable and reliable manner.

Process Monitoring

In addition to process qualification, the Reliability group also conducts ongoing process monitoring programs. Once every 90 days each major production process is evaluated using rel chips as test vehicles. The resulting test data is analyzed for parameter limits and process stability. In this manner AMI can help assure repeatability and high product quality.

Package Qualifications

New packages are also qualified before they are adopted. To analyze packages, a qualification matrix is designed, according to which the new package and an established package (used for control) are tested concurrently. The test matrix consists of a full spectrum of electrical and environmental stress tests, in accordance with MIL-STD-883.

Failure Analysis

Another important function of the Reliability group is failure analysis. Scanning electron microscopes, high power optical microscopes, diagnostic probe stations, and other equipment is used in failure analysis of devices submitted from various sources. It is the function of the Reliability group to determine the cause of failure and recommend corrective action.

The Reliability group provides a failure analysis service for the previously mentioned in-house programs and for the evaluation of customer returns. All AMI customers are provided a failure analysis service for any part that fails within one year from date of purchase and the results of the analysis are returned in the form of a written report.

Summary

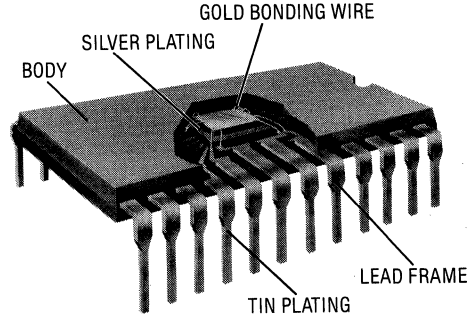
The Product Assurance Program at AMI is oriented towards process control and monitoring, and the evaluation of devices. The Program consists of three major functions: Quality Control, Quality Assurance, and Reliability. Constant monitoring of all phases of production, with information feedback at all levels, allows fast and efficient detection of problems, evaluation and analysis, correction, and verification of the correction. The overall result is a line of products which are highly repeatable and reliable, with a very low reject level.

PLASTIC PACKAGE

The AMI plastic dual-in-line package is the equivalent of the widely accepted industry standard, refined by AMI for MOS/VLSI applications. The package consists of a plastic body, transfer-molded directly onto the assembled lead frame and die. The lead frame is Kovar or Alloy 42, with external pins tin plated. Internally, there is a 150μin. silver spot on the die attach pad and on each bonding fingertip. Gold bonding wire is attached with the thermosonic gold ball bonding technique.

Materials of the lead frame, the package body, and the die attach are all closely matched in thermal expansion coefficients, to provide optimum response to various thermal conditions. During manufacture every step of the process is rigorously monitored to assure maximum quality of the AMI plastic package.

Available in: 8, 14, 16, 18, 22, 24, 28, 40, 48 and 64 pin configurations.

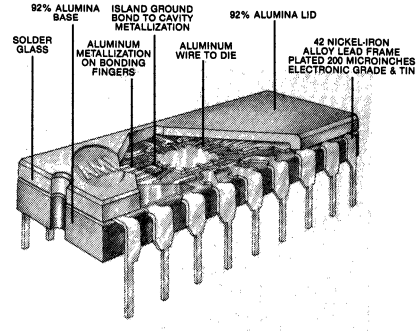


CERDIP PACKAGE

The Cerdip dual-in-line package has the same high performance characteristics as the standard three-layer ceramic package yet is a cost-effective alternative. It is a military approved type package with excellent reliability characteristics.

The package consists of an Alumina (Al_2O_3 base and the same material lid, hermetically fused onto the base with low temperature solder glass.

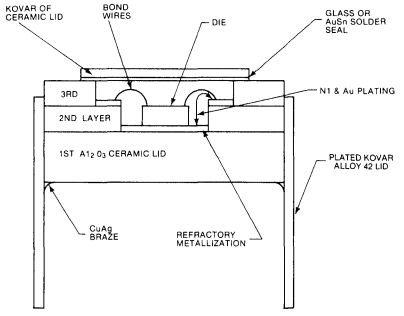
Available in 14, 16, 18, 20, 22, 24, 28 and 40 pin configurations.



CERAMIC PACKAGE

Industry standard high performance, high reliability package, made of three layers of AL_2O_3 ceramic and nickel-plated refractory metal. Either a low temperature glass sealed ceramic lid or a gold tin **eutectic** sealed Kovar lid is used to form the hermetic cavity of this package. Package leads are available with gold or tin plating for socket insertion or soldering.

Available in 14, 16, 18, 22, 24, 28, 40, 48 and 64 pin configurations.

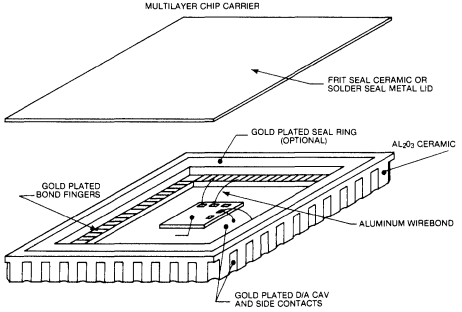


CHIP CARRIER PACKAGE

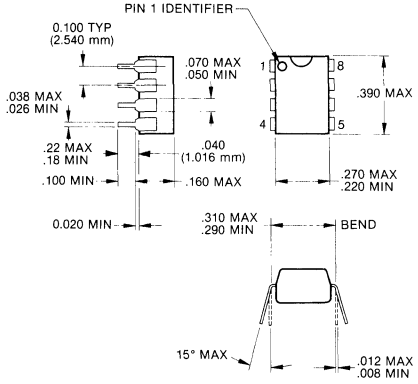
Chip carriers are the new industry standard in reducing package size. Built on the same concept as the highly reliable side-braze ceramic package, it is made of three layers of AL_2O_3 ceramic, refractory metallization and gold plating. The chip carrier also offers contact pads equally spaced on all four sides of the carrier resulting in increased package density, better electrical characteristics, and a more cost effective way of packaging IC devices.

The package comes with a gold tin **eutectic** sealed metal lid or the low cost glass sealed ceramic lid creating a standard hermetic cavity.

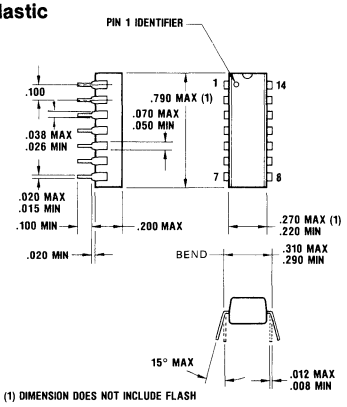
Available in 20, 24, 28, 40, 44, 48, 68 and 84 LD standard 3-layer versions and 24, 28, 44 LD slam style on 50 mil center lines to the JEDEC standards.



8-Pin Plastic



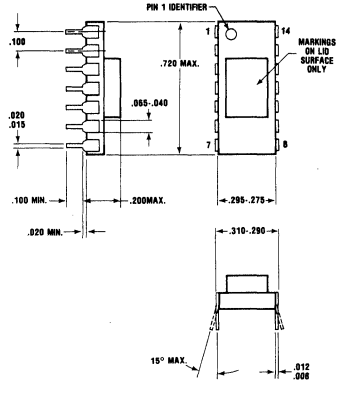
14-Pin Plastic



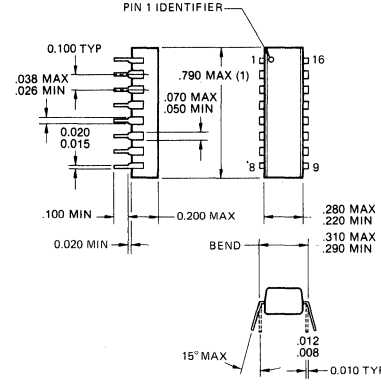
NOTE: (1) DIMENSION DOES NOT INCLUDE FLASH

Packaging

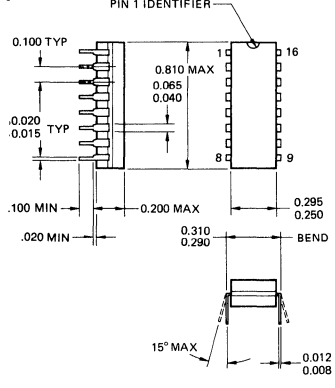
14-Pin Ceramic



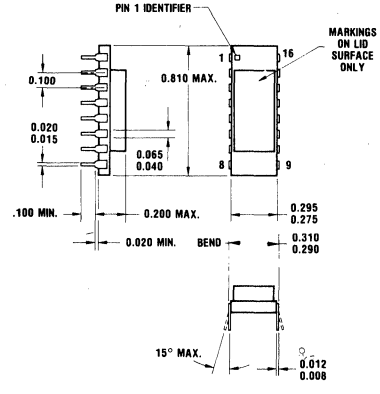
16-Pin Plastic



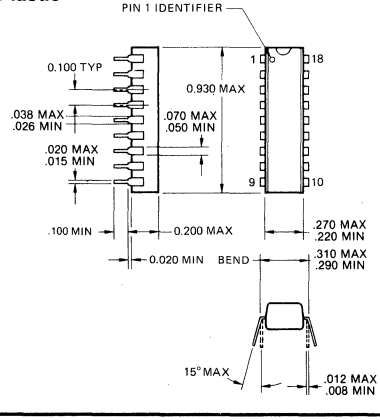
16-Pin Cerdip



16-Pin Ceramic



18-Pin Plastic



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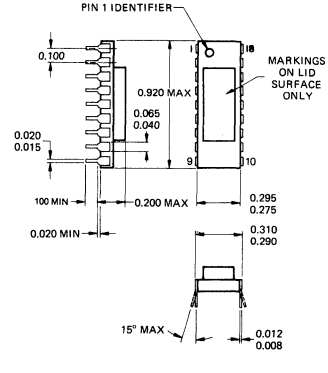
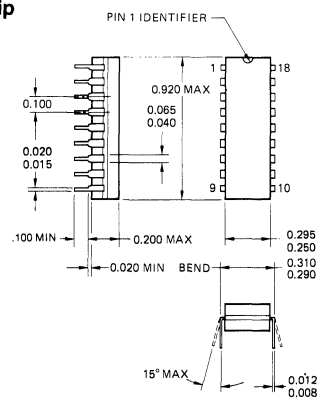
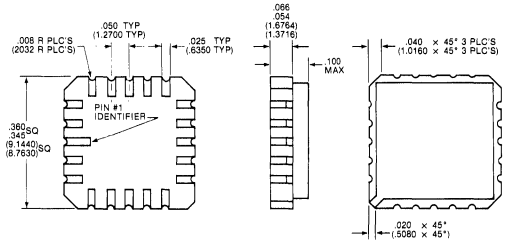


Packaging

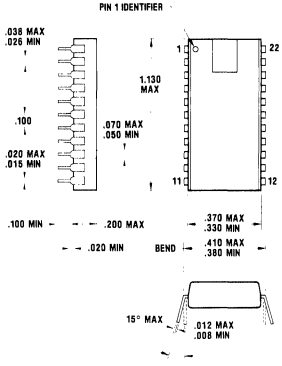
18-Pin Cerdip



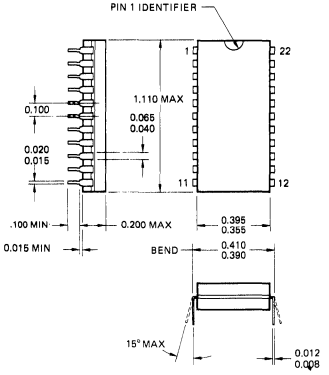
20-Lead Chip Carrier



22-Pin Plastic



22-Pin Cerdip



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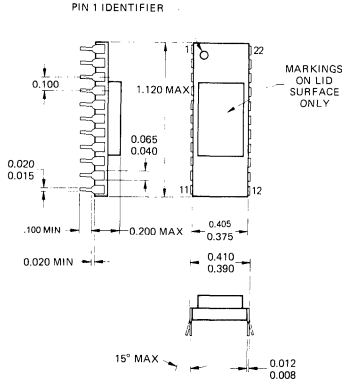
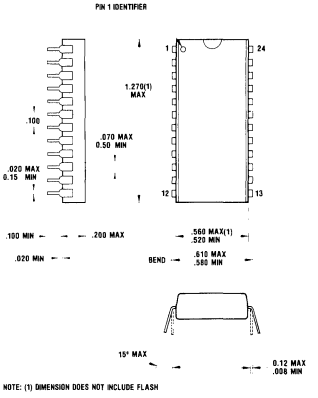
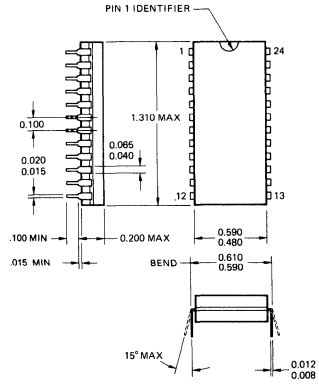


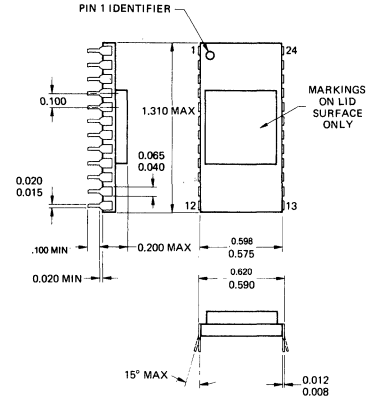
24-Pin Plastic



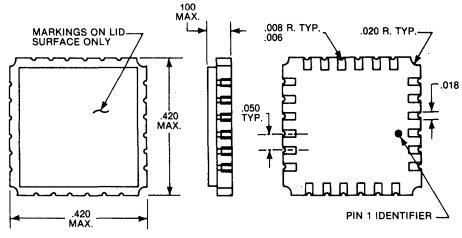
24-Pin Cerdip



24-Pin Ceramic

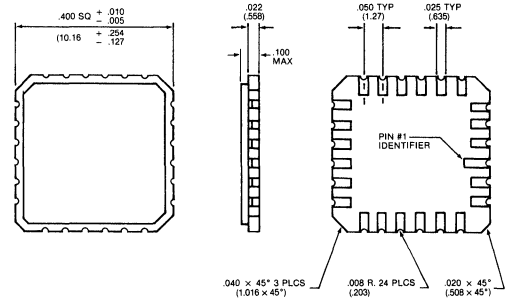


24-Lead Chip Carrier



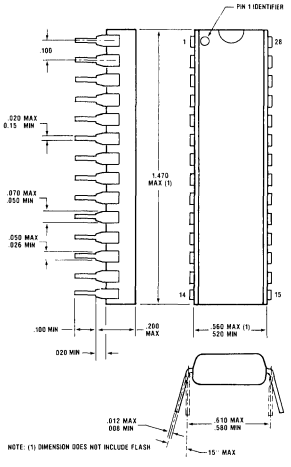
24-Lead Slam Chip Carrier

NOTE: This package is presently in development

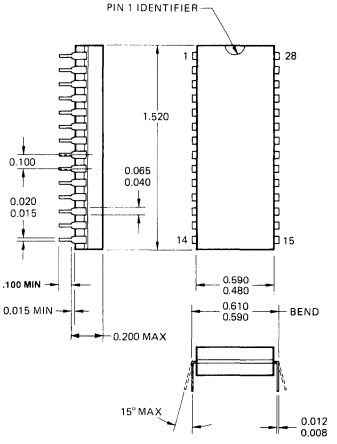


Packaging

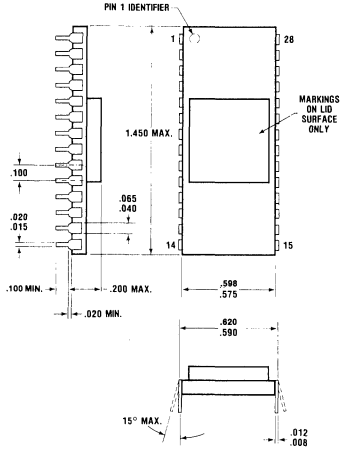
28-Pin Plastic



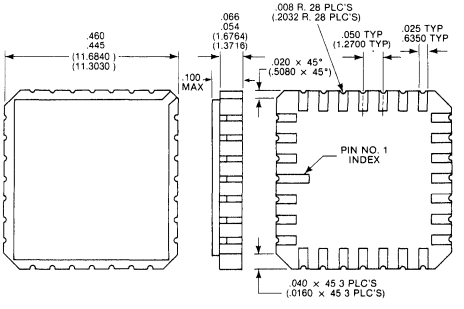
28-Pin Cerdip



28-Pin Ceramic



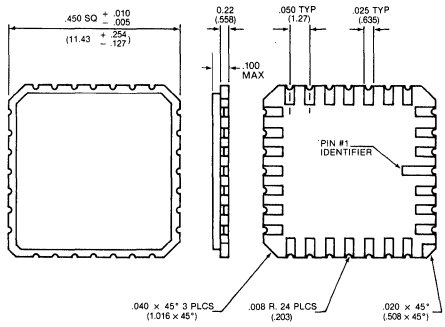
28-Lead Chip Carrier



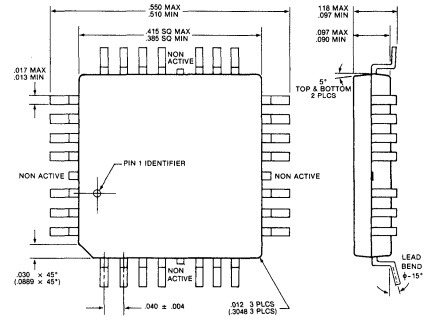
Packaging

28-Lead Slam Chip Carrier

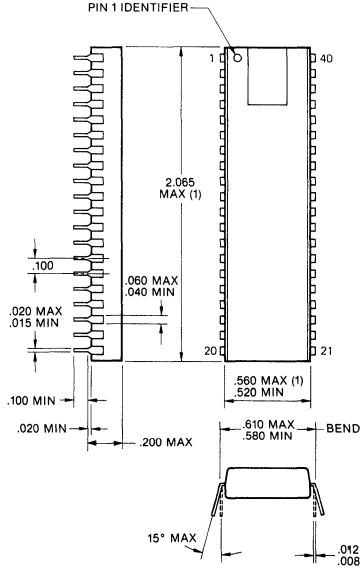
NOTE: This package is presently in development



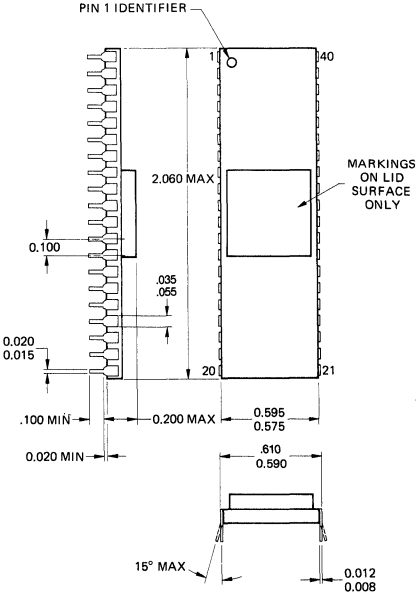
28-Lead Plastic Mini-Flat Package



40-Pin Plastic

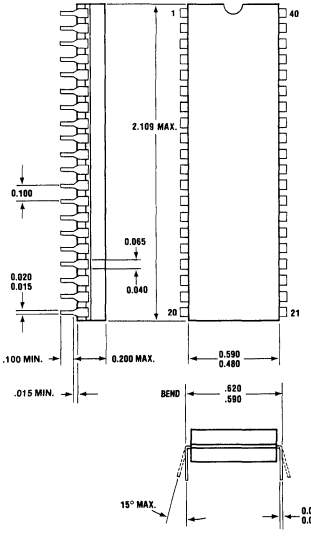


40-Pin Ceramic

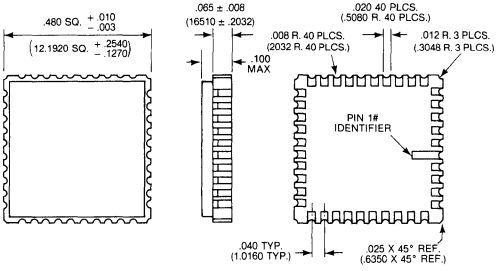


Packaging

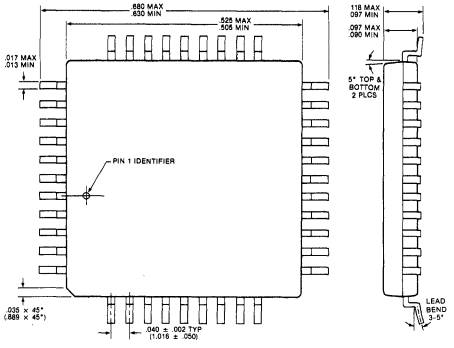
40-Pin Cerdip



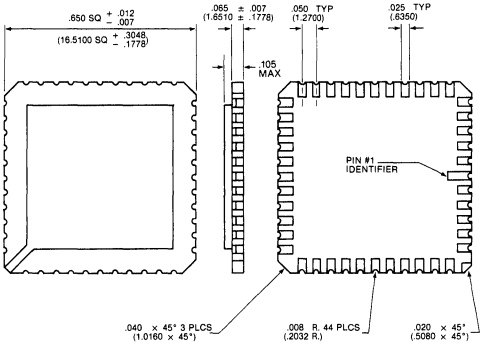
40-Lead Chip Carrier



40 Lead Plastic Mini-Flat Package

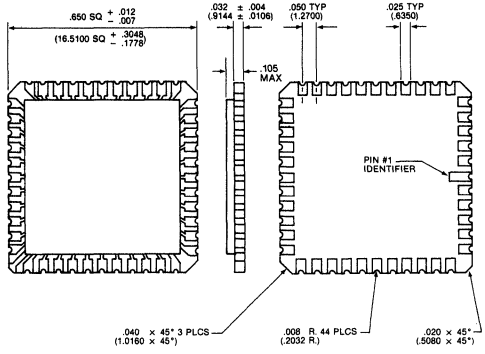


44-Lead Chip Carrier

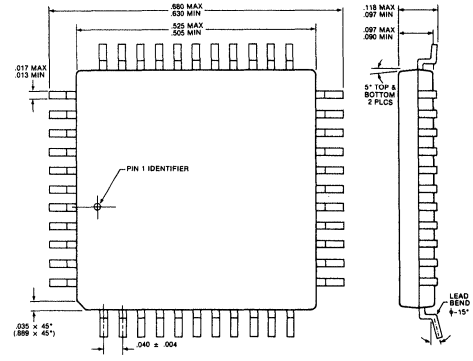


44-Lead Slam Chip Carrier

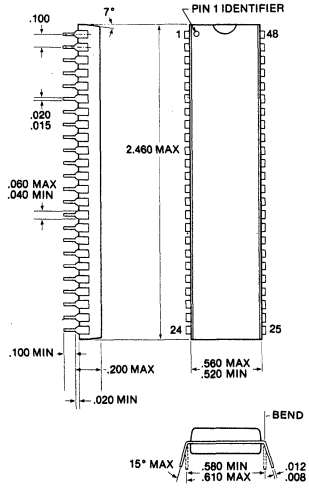
NOTE: This package is presently in development



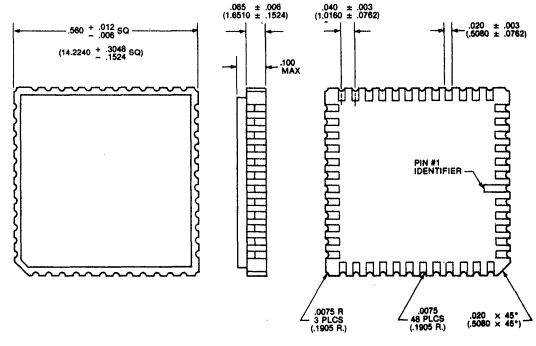
44-Lead Plastic Mini-Flat Package



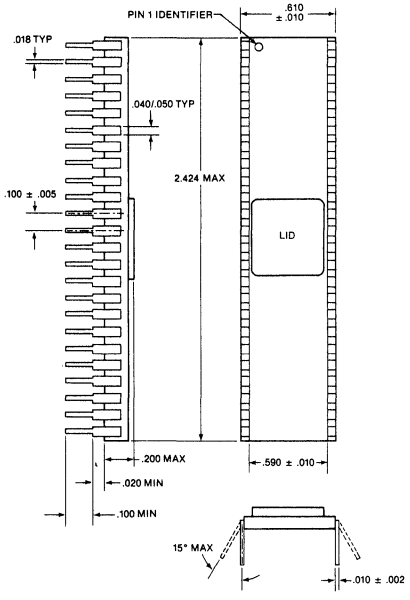
48-Pin Plastic



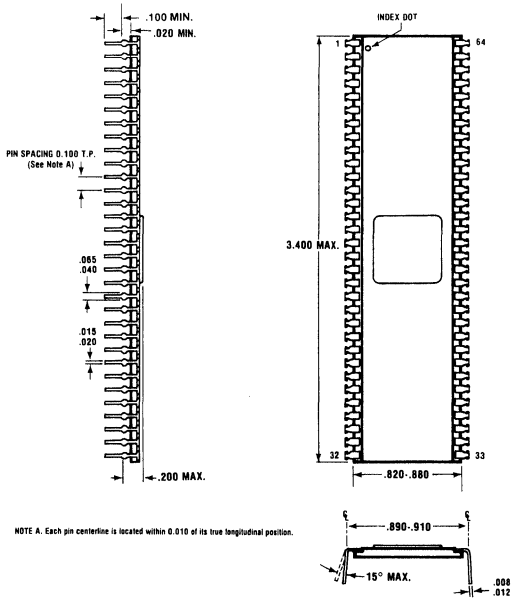
48-Lead Chip Carrier



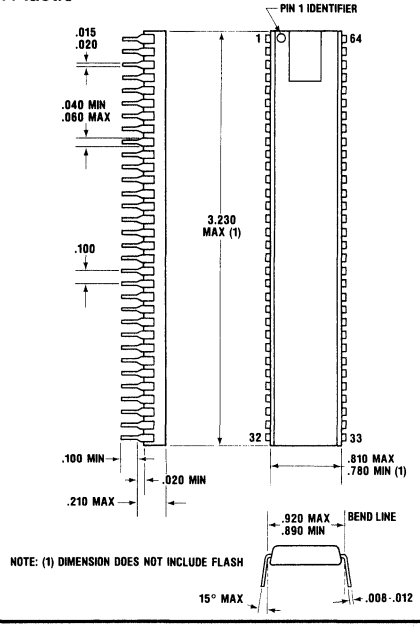
48-Pin Side Brazed



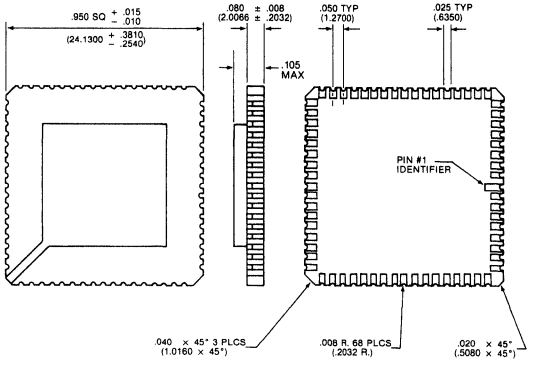
64-Pin Ceramic



64-Pin Plastic

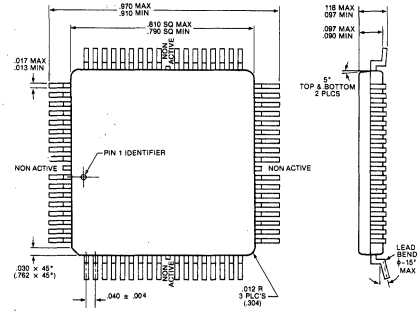


68-Lead Chip Carrier

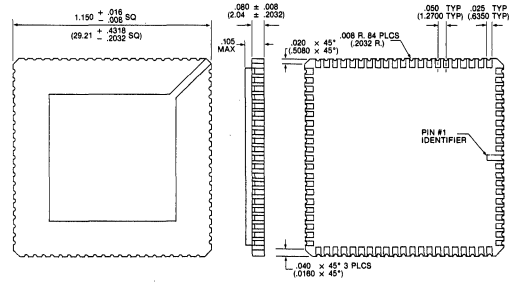


Packaging

68 Lead Plastic Mini-Flat Package



84-Lead Chip Carrier



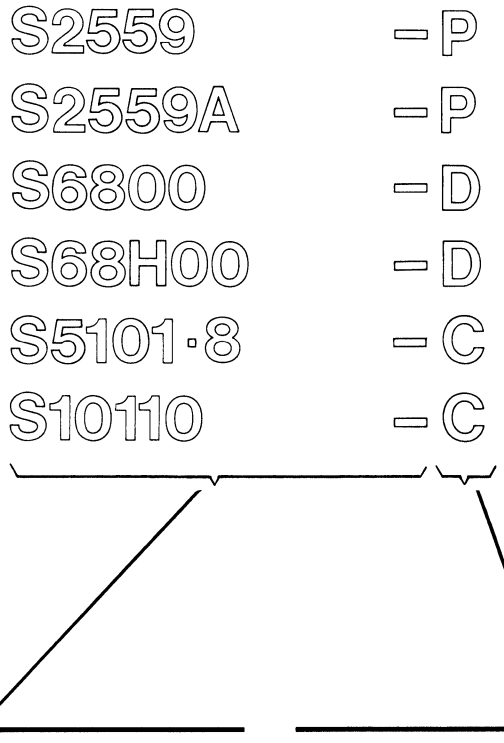
Ordering Information

Standard Products

Any product in this MOS Products Catalog can be ordered using the simple system described below. With this system it is possible to completely specify any standard device in this catalog in a manner that is compatible with AMI's order processing methods. The example below shows how this ordering system works and will help you to order your parts in a manner that can be expedited rapidly and accurately.

All orders (except those in sample quantities) are normally shipped in plastic containers or aluminum tube containers, which protect the devices from static electricity damage under all normal handling conditions. Either container is compatible with standard automatic IC handling equipment.

Any device described in this catalog is an AMI Standard Product. However, ROM devices that require mask preparation or programming to the requirements of a particular user, devices that must be tested to other than AMI Quality Assurance standard procedures, or other devices requiring special masks are sold on a negotiated price basis.



Device Number—prefix S, followed by four (or five*) numeric digits that define the basic device type. Versions to the basic device are indicated by an additional alpha or numeric digit as shown in the above examples.

*Organ Circuits

Package Type—a single letter designation which identifies the basic package type. The letters are coded as follows:

P — Plastic package

D — Cerdip package

C — Ceramic (three-layer) package

Terms of Sale

TERMS OF SALE

JANUARY 1983

1. ACCEPTANCE: THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. PAYMENT:

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefor shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. TAXES: Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority, (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. F.O.B. POINT: All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, United Parcel Service (UPS), Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. DELIVERY: Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. PATENTS: The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. INSPECTION: Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY: The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. PRODUCTS NOT WARRANTED BY SELLER: The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES EXPRESSED, STATUTORY OR IMPLIED INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INFRINGEMENT AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products contact Seller.

10. PRICE ADJUSTMENTS: Seller's unit prices are based on certain material costs. These materials include, among other things, gold packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. VARIATION IN QUANTITY: If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. CONSEQUENTIAL DAMAGES: In no event shall Seller be liable for special, incidental or consequential damages.

13. GENERAL:

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities domestic or foreign.

(g) Unless otherwise agreed in a writing signed by both Buyer and Seller, Seller shall retain title to and possession of all tooling of any kind (including but not limited to masks and pattern generator tapes) used in the production of products furnished hereunder"

(h) Buyer, by accepting these products, certifies that he will not export or re-export the products furnished hereunder unless he complies fully with all laws and regulations of the United States relating to such export or re-export, including but not limited to the Export Administration Act of 1979 and the Export Administration Regulations of the U.S. Department of Commerce.

14. GOVERNMENT CONTRACT PROVISIONS: If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Defense Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be - i.e., "Contracting Officer" shall mean "Buyer" "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Rhodesia and Certain Communist Areas; 7-103.16, Contract Work Hours and Safety Standards Act - Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity Clause; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government (only to the extent that Buyer's contract is terminated for the convenience of the government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-103.24, Responsibility for Inspection; 7-103.25, Commercial Bills of Lading Covering Shipments Under FOB Origin Contracts; 7-103.27, Listing of Employment Openings; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.15, Examination of Records by Comptroller General; 7-104.20, Utilization of Labor Surplus Area Concerns.

Worldwide Sales Offices

UNITED STATES

Northwest Region

HEADQUARTERS—3800 Homestead Road, Santa Clara, California 95051 ..... (408) 246-0330
TWX: 910-338-0018
or 910-338-0024

CALIFORNIA, 2960 Gordon Avenue, Santa Clara 95051 ..... (408) 738-4151
WASHINGTON, 20709 N.E. 232nd Avenue, Battle Ground 98604 ..... (206) 687-3101

Southwest Region

CALIFORNIA, 1451 Quail Street, Suite 208, Newport Beach 92660 ..... (714) 851-5931
CALIFORNIA, San Diego 92008 ..... (619) 729-3512
ARIZONA, Scottsdale 85254 ..... (602) 996-5638

Central Region

ILLINOIS, 500 Higgins Road, Suite 210, Elk Grove Village 60007 ..... (312) 437-6496
MICHIGAN, 29200 Vassar Avenue, Suite 221, Livonia 48152 ..... (313) 478-4220
COLORADO, 7346A So. Alton Way, Englewood 80112 ..... (303) 694-0629

Southeastern Region

FLORIDA, 139 Whooping Loop, Altamonte Springs 32701 ..... (305) 830-8889
NORTH CAROLINA, 5711 Six Forks Road, Suite 210, Raleigh 27609 ..... (919) 847-9468
ALABAMA, 500 Wynn Drive #304-C, Huntsville 35085 ..... (205) 830-1435
TEXAS, 725 South Central Expressway, Suite A-9, Richardson 75080 ..... (214) 231-5721
(214) 231-5285
TEXAS, Austin 78746 ..... (512) 327-5286

Mid-Atlantic Area

PENNSYLVANIA, Axewood East, Butler & Skippack Pikes, Suite 230, Ambler 19002 ..... (215) 643-0217
VIRGINIA, Northway Building, 500 Westfield Road, Suite 211, Charlottesville 22906 ..... (804) 973-1213
INDIANA, 408 South 9th Street, Suite 201, Noblesville 46060 ..... (317) 773-6330
OHIO, 100 East Wilson Bridge Road, Suite 225, Worthington 43085 ..... (614) 436-0330

Northeastern Region

NEW YORK, 20F Robert Pitt Drive, Suite 208, Monsey 10952 ..... (914) 352-5333
MASSACHUSETTS, 24 Muzzey Street, Lexington 02173 ..... (617) 861-6530

INTERNATIONAL

ENGLAND, AMI Microsystems, Ltd., Princes House, Princes St., Swindon SN1 2HU ..... (0793) 37852
FRANCE, AMI Microsystems, S.A.R.L., 124 Avenue de Paris, 94300 Vincennes ..... (01) 374 00 90
WEST GERMANY, AMI Microsystems GmbH, Suite 237, Rosenheimer Strasse 30/32, 8000 Munich 80 ..... (089) 483081
AUSTRIA, Austria Microsystems International GmbH, Schloss Premstätten
8141 Unterpremstätten, Austria ..... (3136) 3666-0
ITALY, AMI Microsystems, S.p.A., Piazza Gobetti 12, Milano 20131 ..... (02) 293745
JAPAN, AMI Japan Ltd., 502 Nikko Sanno Building 2-5-3, Akasaka, Minato-ku, Tokyo 107 ..... (3) 586-8131

Domestic Representatives & Distributors

Domestic Representatives

CANADA, Burnaby B.C.	Woodbery Elect. Sales Ltd.	(604) 430-3302
CANADA, Mississauga, Ontario	Vitel Electronics	(416) 676-9720
CANADA, Ottowa, Ontario	Vitel Electronics	(613) 592-0090
CANADA, Quebec, Quebec	Vitel Electronics	(514) 331-7393
IOWA, Cedar Rapids	Comstrand, Inc.	(319) 377-1575
KANSAS, Overland Park	Kebco, Inc.	(913) 541-8431
KANSAS, Wichita	Kebco, Inc.	(316) 733-1301
MARYLAND, Rockville	Mechtronics Sales	(301) 340-2130
MASSACHUSETTS, Tyngsboro	Comptech	(617) 649-3030
MINNESOTA, Minneapolis	Comstrand, Inc.	(612) 788-9234
MISSOURI, Maryland Heights	Kebco, Inc.	(314) 576-4111
NEW YORK, Clinton	Advanced Components	(315) 853-6438
NEW YORK, Endicott	Advanced Components	(607) 785-3191
NEW YORK, North Syracuse	Advanced Components	(315) 699-2671
NEW YORK, Rochester	Advanced Components	(716) 544-7017
NEW YORK, Scottsville	Advanced Components	(716) 889-1429
PUERTO RICO, San Juan	Electronic Tech. Sales, Inc.	(809) 780-8259

Domestic Distributors

ALABAMA, Huntsville	Schweber Electronics	(205) 882-2200
ARIZONA, Phoenix	Kierulff Electronics	(602) 243-4101
ARIZONA, Scottsdale	Western Microtechnology	(602) 948-4240
ARIZONA, Tempe	Anthem Electronics	(602) 244-0900
ARIZONA, Tucson	Kierulff Electronics	(602) 624-9986
CALIFORNIA, Canoga Park	Schweber Electronics	(213) 999-4702
CALIFORNIA, Chatsworth	Anthem Electronics	(213) 700-1000
CALIFORNIA, Cupertino	Western Microtechnology	(408) 725-1660
CALIFORNIA, Irvine	Schweber Electronics	(714) 556-3880
CALIFORNIA, Los Angeles	Kierulff Electronics	(213) 725-0325
CALIFORNIA, Palo Alto	Kierulff Electronics	(415) 968-6292
CALIFORNIA, Sacramento	Schweber Electronics	(916) 929-9732
CALIFORNIA, San Diego	Anthem Electronics	(619) 453-4871
CALIFORNIA, San Diego	Kierulff Electronics	(619) 278-2112
CALIFORNIA, San Jose	Anthem Electronics	(408) 946-8000
CALIFORNIA, Santa Clara	Schweber Electronics	(408) 748-4700
CALIFORNIA, Tustin	Anthem Electronics	(714) 730-8000
CALIFORNIA, Tustin	Kierulff Electronics	(714) 731-5711
CANADA, Alberta, Calgary	Future Electronics	(403) 259-6408
CANADA, British Columbia, Vancouver	Future Electronics, Inc.	(604) 438-5545
CANADA, Ontario, Downsview	Cesco Electronics, Ltd.	(416) 661-0220
CANADA, Ontario, Downsview	Future Electronics, Inc.	(416) 663-5563
CANADA, Ottawa	Future Electronics, Inc.	(613) 820-8313
CANADA, Quebec, Montreal	Cesco Electronics, Ltd.	(514) 735-5511
CANADA, Quebec, Point Claire	Future Electronics, Inc.	(514) 694-7710
CANADA, Quebec	Cesco Electronics, Ltd.	(418) 687-4231
COLORADO, Denver	Kierulff Electronics	(303) 371-6500
COLORADO, Englewood	Anthem Electronics	(303) 790-4500
COLORADO, Englewood	Kierulff Electronics	(303) 790-4444
CONNECTICUT, Danbury	Schweber Electronics	(203) 792-3742
CONNECTICUT, Wallingford	Kierulff Electronics	(203) 265-1115
FLORIDA, Altamonte Springs	Schweber Electronics	(305) 331-7555
FLORIDA, Ft. Lauderdale	Kierulff Electronics	(305) 486-4004
FLORIDA, Hollywood	Schweber Electronics	(305) 927-0511
FLORIDA, St. Petersburg	Kierulff Electronics	(813) 576-1966
GEORGIA, Norcross	Kierulff Electronics	(404) 447-5252

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IOWA, Cedar Rapids	Schweber Electronics	(319) 373-1417
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MASSACHUSETTS, Bedford	Schweber Electronics	(617) 275-5100
MASSACHUSETTS, Billerica	Kierulff Electronics	(617) 935-5134
MICHIGAN, Livonia	Schweber Electronics	(313) 525-8100
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MINNESOTA, Edina	Kierulff Electronics	(612) 941-7500
MISSOURI, Earth City	Scheweber	(314) 739-0526
MISSOURI, Maryland Heights	Kierulff Electronics	(314) 739-0855
NEW HAMPSHIRE, Manchester	Schweber Electronics	(603) 625-2250
NEW JERSEY, Fairfield	Kierulff Electronics	(201) 575-6750
NEW JERSEY, Fairfield	Schweber Electronics	(201) 227-7880
NEW YORK, Rochester	Schweber Electronics	(716) 424-2222
NEW YORK, Westbury L.I.	Schweber Electronics	(516) 334-7474
NORTH CAROLINA, Greensboro	Kierulff Electronics	(919) 852-9440
NORTH CAROLINA, Raleigh	Schweber Electronics	
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OHIO, Cleveland	Kierulff Electronics	(216) 587-6558
OHIO, Dayton	Schweber Electronics	(513) 439-1800
OKLAHOMA, Tulsa	Kierulff Electronics	(918) 252-7537
OKLAHOMA, Tulsa	Schweber Electronics	(918) 622-8000
OREGON, Portland	Kierulff Electronics	(503) 641-9150
PENNSYLVANIA, Horsham	Schweber Electronics	(215) 441-0600
PENNSYLVANIA, Pittsburgh	Schweber Electronics	(412) 782-1600
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TEXAS, Austin	Schweber Electronics	(512) 458-8253
TEXAS, Dallas	Kierulff Electronics	(214) 343-2400
TEXAS, Dallas	Schweber Electronics	(214) 661-5010
TEXAS, Houston	Kierulff Electronics	(713) 530-7030
TEXAS, Houston	Schweber Electronics	(713) 784-3600
UTAH, Salt Lake City	Kierulff Electronics	(801) 973-6913
WASHINGTON, Bellevue	Anthem Electronics	(206) 881-0850
WASHINGTON, Tukwila	Kierulff Electronics	(206) 575-4420
WISCONSIN, Brookfield	Schweber Electronics	(414) 784-9020
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BRAZIL, Sao Paulo	Datatronix Electronica Ltda.	11-826-0111
CHILE	Victronics Ltda.	36440
DENMARK,	Semicap A/S	(01) 22150
ENGLAND, Derby	Quarndon Electronics Ltd.	(0332) 32651
ENGLAND, Harlow, Essex	VSI Electronics (UK) Ltd.	(0279) 2935477
FINLAND, Espoo	OY Atomica AB	(80) 423533
FRANCE, Sevres	Tekelec Airtronic	(01) 534-75-35
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ISRAEL, Tel Aviv	Eldis Electronics, Ltd.	410656
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MEXICO	Dicopel S.A.	(905) 561-3211
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SOUTH AFRICA, Transvaal	Radiokom Pty, Ltd.	(011) 485712
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SWITZERLAND, Zurich	W. Moor AG	(01) 8406644
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WEST GERMANY, Berlin	Aktiv Elektronik GmbH	(030) 6845088
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WEST GERMANY, Viersen	Mostron Halbleitervertriebs	(0216) 17024
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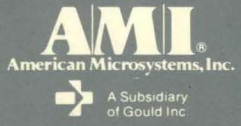

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