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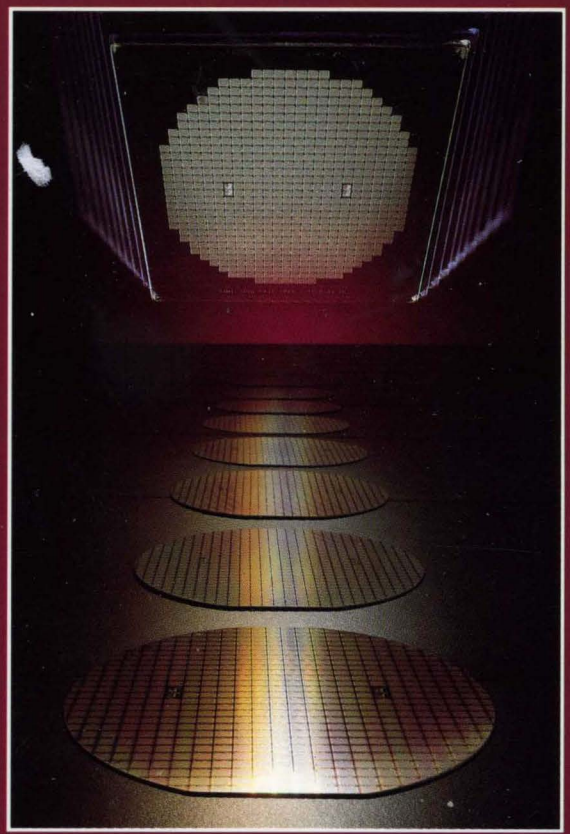

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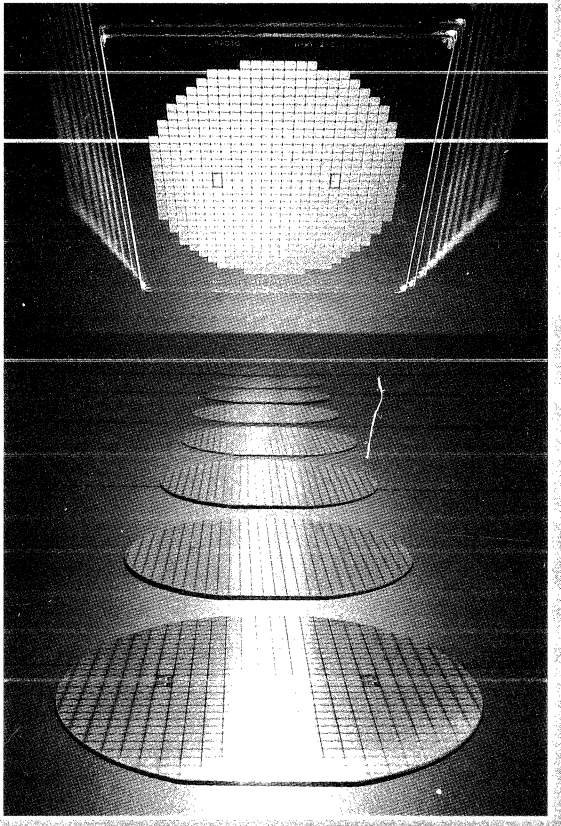

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1985 3μ HCMOS Gate Array Databook

Introduction

Since its founding in 1966, Gould AMI Semiconductors, headquartered in Santa Clara, California, has been a leader in the design and manufacture of custom metal-oxide-silicon/very-large-scale integrated (MOS/VLSI) circuits. Today, the company supports an entire continuum of application specific solutions—gate arrays, standard cell designs, interactive full custom circuits, and circuits fabricated from a customer's own tooling—with a goal of continually reducing the risk, development span, and cost of application specific circuits.

In addition, Gould AMI is also a supplier of catalog MOS/VLSI devices that are synergistic with our custom capabilities. These devices include read-only memories (ROMs) and random-access memories (RAMs), and data communications and telecommunications circuits, including modems and digital signal processors. By developing catalog parts that are synergistic with our custom products, Gould AMI can provide the broadest range of chips needed to implement a specific system solution.

With more than 3000 different customized ICs produced, Gould AMI ranks as the leading supplier of application specific integrated circuits (ASICs). The company's success in this area of semiconductor manufacture is the result of technical expertise that is characterized by commitment to service. Gould AMI will work with a company at any stage of a product's design: from system concept to IC fabrication based on a customer's own tooling.

Gould AMI has design centers in Cupertino, California; Jericho, New York; and Altamonte Springs, Florida, which will provide assistance to customers. Wafer fabrication is done at a new state-of-the art facility in Pocatello, Idaho. Circuit packaging and assembly operations are conducted in Manila, the Philippines. A joint venture company, Austria Microsystems International, located in Graz, Austria, serves the European common market with complete design and fabrication facilities. Another joint venture company in Tokyo, Japan, Asahi Microsystems Inc., also designs and will produce integrated circuits for Japan and countries of the Pacific Basin.

This databook is intended for your information only, and is not necessarily the most current version of the data. For actual gate array circuit design, we recommend that you subscribe to our Gate Array Design Manual update service by filling out the card in the back of this databook.

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OR02	Pre-Routed Two Input OR Gate	1.5	2.67
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3μ Double-Metal HCMOS Gate Array

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AN01	Pre-Routed AND-NOR Gate	2.0	3.10
AN02	Pre-Routed AND-NOR Gate	2.0	3.11
AN03	Pre-Routed AND-NOR Gate	2.0	3.12
AN04	Pre-Routed AND-NOR-NOR Gate	3.0	3.13
AN05	Pre-Routed Four 3-In AND's Into A 4-In NOR	6.0	3.14
AN06	Pre-Routed Three 3-In AND's Into A 3-In NOR	5.0	3.15
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DF01	Pre-Routed D Flip-Flop	4.0	3.17
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3μ Double-Metal HCMOS Gate Array (Continued)

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DL19	Pre-Routed Latch With Set	3.0	3.42
DL1A	Pre-Routed Latch With Reset	3.0	3.44
DL1B	Pre-Routed Latch With Active Low Set	3.0	3.46
DL1C	Pre-Routed Latch With Active Low Reset	3.0	3.48
DL1D	Pre-Routed Latch With Active Low Set and Reset	3.0	3.50
EN01	Pre-Routed Exclusive NOR Gate	3.0	3.52
EO01	Pre-Routed Exclusive OR Gate	3.0	3.53
IB01	Pre-Routed CMOS Non-Inverting Input Buffer	1.0	3.54
IB02	Pre-Routed CMOS Inverting Input Buffer	0.0	3.55
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3μ Double-Metal HCMOS Gate Array (Continued)

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IT01	Non-Inverting Internal Tri-State Buffer	2.0	3.78
IT02	Pre-Routed Inverter Driving A Transmission Gate	2.0	3.79
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NA04	Pre-Routed Four Input NAND Gate	2.0	3.84
NA05	Pre-Routed Five Input NAND Gate	3.0	3.85
NA06	Pre-Routed Six Input NAND Gate	3.0	3.86
NO02	Pre-Routed Two Input NOR Gate	1.0	3.87
NO03	Pre-Routed Three Input NOR Gate	2.0	3.88
NO04	Pre-Routed Four Input NOR Gate	2.0	3.89
NO05	Pre-Routed Five Input NOR Gate	3.0	3.90
NO06	Pre-Routed Six Input NOR Gate	3.0	3.91
OB03	CMOS Output Buffer	n/a	3.92
OB04	CMOS Inverting Output Buffer	2.0	3.93
OB05	Open Drain Output Buffer	n/a	3.94
OB06	Inverting Open Drain Output Buffer	2.0	3.95
OB07	Open Drain Output Buffer	n/a	3.96
OB08	Inverting Open Drain Output Buffer	2.0	3.97
OB09	CMOS Tri-State Non-Inverting Output Buffer	7.0	3.98

3μ Double-Metal HCMOS Gate Array (Continued)

Cell	Description	Gate Equiv.	Page
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ON02	Pre-Routed OR-NAND Gate	2.0	3.101
ON03	Pre-Routed OR-NAND Gate	2.0	3.102
ON04	Pre-Routed OR-NAND-NAND Gate	3.0	3.103
OR02	Pre-Routed Two Input OR Gate	2.0	3.104
OR03	Pre-Routed Three Input OR Gate	2.0	3.105
OR04	Pre-Routed Four Input OR Gate	3.0	3.106
OR05	Pre-Routed Five Input OR Gate	3.0	3.107
PP01	V_{SS} Ground Pin	n/a	3.108
PP02	V_{DD} Power Pin	n/a	3.109
SR00	Pre-Routed Set-Reset NAND Gate Latch	2.0	3.110
SR01	Pre-Routed Set-Reset OR Gate Latch	2.0	3.111

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Count2	4-Bit Binary Counter Presetable	53	5.4
Count3	4-Bit Binary Counter Expandable	45	5.6
Count4	4-Bit Binary Counter Presetable, Expandable	58	5.8
DEC1	4-Bit Decade Counter	43	5.10
DEC2	4-Bit Decade Counter With DIRECT LOAD	57	5.12
DEC3	4-Bit Decade Counter With CARRYIN And CARRYOUT	49	5.14
DEC4	4-Bit Decade Counter With DIRECT LOAD, CARRYIN, And CARRYOUT	62	5.16
UDB1	4-Bit Binary Up/Down Counter	50	5.18
UDB2	4-Bit Binary Up/Down Counter With DIRECT LOAD	63	5.20
UDB3	4-Bit Binary Up/Down Counter With CARRYIN And CARRYOUT	70	5.22
UDB4	4-Bit Binary Up/Down Counter With DIRECT LOAD, CARRYIN, and CARRYOUT	73	5.24
UDD1	4-Bit Up/Down Decade Counter	65	5.26
UDD2	4-Bit Up/Down Decade Counter With DIRECT LOAD	75	5.28
UDD3	4-Bit Up/Down Decade Counter With CARRYIN and CARRYOUT	71	5.30
UDD4	4-Bit Up/Down Decade Counter With DIRECT LOAD, CARRYIN and CARRYOUT	85	5.32
10G138	3 to 8 Decoder	24	5.34
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10G148	8 to 3 Priority Encoder	46	5.38
10G154	4 to 16 Decoder	56	5.40
10G164	8-Bit Serial in Parallel Out Shift Register	55	5.42
10G165	8-Bit Parallel/Serial In Serial Out Shift Register	78	5.44
10G166	8-Bit Parallel/Serial Serial Out Shift Register	80	5.46
10G182	Carry Lookahead Generator	38	5.48
10G194	4-Bit Bi-Directional Universal Shift Register	65	5.50
10G195	4-Bit Synchronous Universal Shift Register	44	5.52
10G199	8-Bit Universal Shift Register	83	5.54
10G91	8-Bit Serial Shift Register	40	5.56
10G280	9-Bit Odd/Even Parity Generator/Check	51	5.58

Gate Array Design Guide

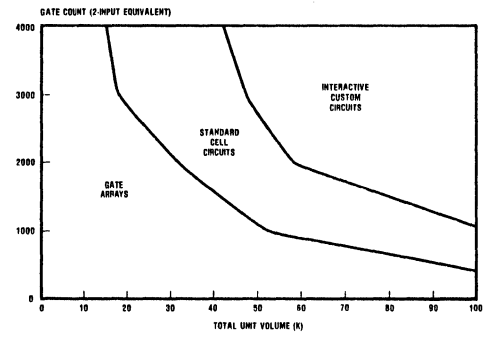
1. Semicustom VLSI

1.1 Introduction

Gould AMI Semiconductors, headquartered in Santa Clara, California is the semiconductor industry leader in the design and manufacture of custom and semicustom gate array and standard cell MOS/VLSI (metal-oxide-silicon/very-large-scale-integrated) circuits. Gould AMI fabricates integrated circuits for the leading computer manufacturers, telecommunications companies, automobile manufacturers and consumer product companies world-wide. Gould AMI is a wholly owned subsidiary of Gould Inc.

With wafer fabrication and test facilities in Santa Clara (California), Pocatello (Idaho), and Graz (Austria) and assembly and test facilities in Manila (the Philippines) that include the latest semiconductor manufacturing equipment, Gould AMI can support a wide spectrum of customer applications in a cost effective way, independent of volume requirements. Figure 1.1 shows the economic tradeoffs of Gould AMI's custom and semicustom solutions.

Figure 1.1. Cost vs Volume Alternatives



Gould AMI Technology is the most advanced integrated software system for MOS/VLSI design available in the industry. It uses a common database for logic simulation, mask layout and test program generation, thereby, simplifying the conversion of a gate array design to a standard cell or full custom circuit, resulting in lower unit costs when the volume requirements warrant it.

1.2 Gate Arrays

Also known as "uncommitted logic arrays" or "master slices", gate arrays are late-mask-programmable devices that contain a predefined number of transistors used to form combinatorial and sequential logic functions, by defining a specific interconnect pattern. Thus, wafers can be fabricated in large scale and placed in inventory for future customization.

From the fabrication point of view, there is little difference between gate arrays and late-mask-programmable ROMs, although these two types of integrated circuits are quite different architecturally. While a ROM's architecture is based on a fixed AND and a mask-programmable OR array configuration only useful in combinatorial networks, gate arrays contain totally uncommitted devices and can be programmed to implement random logic functions as well as storage elements that can be controlled by common or independent clock signals, depending on the user's requirements.

Gould AMI gate arrays are fabricated with advanced CMOS process technologies, thus offering all of the conventional advantages of CMOS, such as very low power dissipation, broad power supply voltage range, and high noise immunity. Furthermore, state-of-the-art 3- and 2-micron array families offer circuit complexities of up to 10,000 2-input equivalent gates with performance characteristics superior to STL (Skottky-Transistor-Logic) devices, and approaching ECL (Emitter-Coupled-Logic) speeds.

Gould AMI's family of 5-micron gate arrays operate over the widest power supply range (2.5 to 13.2 volts) available in the industry for Silicon-Gate CMOS arrays. There are six different members in this family, as shown in Table 1.1, with gate densities ranging from 300 up to 1260 2-input equivalent gates. Specific details on device characteristics can be found in this semi-custom Design Manual. Table 1.2 shows the electrical characteristics of the 5-micron arrays.

High performance and gate densities can be achieved with 3-micron gate arrays, which are fabricated with a state-of-the-art CMOS process that includes single and double metal interconnect options, and allows operation from 2.5 to 5.5 volts over the full military range.

As shown in Table 1.3, the single metal 3-micron array family consists of five members with gate densities ranging from 500 to 2500 2-input equivalent gates, and offer the most cost effective solution for applications requiring 5 Volt operation. The overall performance of these arrays is, however, degraded by the use of polysilicon "crossunders", which are needed to route signals under metal interconnect tracks or power buses, and can be a limiting factor in gate arrays with high component utilization, high gate counts or stringent performance requirements.

In the double metal set of 3-micron arrays two layers of aluminum are used for interconnect purposes, and the switching characteristics of the circuit can be improved anywhere from 10% to 30% with respect to the single metal family, depending on the specific application. Moveover, the double metal arrays allow higher utilization of the uncommitted transitors, and gate densities of up to 4000 gates (See Table 1.4).

Table 1.1. 5-Micron Gate Array Family

Device Type	Equivalent Two-Input	Bonding Pads	Low Power Drivers	High Power Drivers
UA-1	300	40	17	20
UA-2	400	46	23	20
UA-3	540	52	25	24
UA-4	770	62	31	28
UA-5	1000	70	35	32
UA-6	1260	78	39	36

Table 1.2

Absolute Maximum Ratings, 5-Micron Gate Arrays

Supply Voltage, V_{DD} ..... −.5V to +15V
Input Voltage, V_{IN} ..... −.5V to V +.5V
D.C. Input Current, I_{IN} ..... +10mA
Storage Temperature, T_{STG} ..... −65° to +150°C

D.C. Electrical Characteristics, 5-Micron Gate Arrays:
Specified at V_{DD} = 5V ±10% or 10V ±10%, V_{SS} = 0V, T_A = −55° to +125°C

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit	Conditions
V_{OL}	Low Level Output Voltage				0.05	V	I_{OL} = 1.0μA
	High Power Output	5			0.4	V	I_{OL} = 2.4mA
	High Power Output	10			0.5	V	I_{OL} = 4.8mA
	Low Power Output	5			0.4	V	I_{OL} = 0.8mA
	Low Power Output	10			0.5	V	I_{OL} = 1.6mA
V_{OH}	High Level Output Voltage		V_{DD}−.05			V	I_{OH} = 1.0μA
	High Power Output	5	2.4			V	I_{OH} = 1.6mA
	High Power Output	10	9.5			V	I_{OH} = 1mA
	Low Power Output	5	2.4			V	I_{OH} = .8mA
	Low Power Output	10	9.5			V	I_{OH} = .4mA
V_{IL}	Input Low Voltage	5	0.0		0.8	V	TTL Input
		5	0.0		1.5	V	CMOS Input
		10	0.0		3.0	V	CMOS Input
V_{IH}	Input High Voltage	5	2.0		V_{DD}	V	TTL Input
		5	2.0		V_{DD}	V	TTL Input
		10	7.0		V_{DD}	V	CMOS Input
I_{IN}	Input Leakage Current	5	−1		1	μA	V_{IN} = V_{DD} or V_{SS}
I_{OZ}	High Impedance Output Leakage Current	5	−10	0.001	10	μA	V_{OH} = V_{DD} or V_{SS}
C_{IN}	Input Capacitance			5		pF	Any Input

Table 1.3. 3-Micron Single Metal Arrays

Device Type	No. Of Gates	I/O Cells	Bonding Pads
GA500	540	40	40
GA1000	1072	54	54
GA1500	1500	64	64
GA2000	2025	74	74
GA2500	2500	84	84

Table 1.4. 3-Micron Double Metal Arrays

Device Type	No. Of Gates	I/O Cells	Bonding Pads
GA500D	520	40	44
GA1000D	1152	64	68
GA2000D	2070	84	88
GA3000D	3080	102	110
GA4000D	4080	120	124

Both families of 3-micron arrays offer total I/O flexibility since every pin can be programmed to be any of the following interface functions:

- TTL/LSTTL Output Driver
- CMOS Output Driver
- Open Drain Output
- Tri-State Buffer
- Bi-Directional Buffer
- Analog Switch
- TTL Input Buffer
- CMOS Input Buffer
- V_{DD} Supply
- V_{SS} Supply

In addition, the D.C. electrical characteristics of 3-micron arrays (See Table 1.5) have been tailored to provide current sinking and sourcing capabilities commensurable with TTL systems requirements.

Table 1.5

Absolute Maximum Ratings, 3-Micron Gate Arrays

Supply Voltage, V_{DD} ..... −.5V to +7V
Input Voltage, V_{IN} ..... −.5V to V +.5V
D.C. Input Current, I_{IN} ..... +10mA
Storage Temperature, T_{STG} ..... −65° to +150°C

D.C. Electrical Characteristics, 3-Micron Gate Arrays:
Specified at V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = −55° to +125°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OL}	Low Level Output Voltage			0.05	V	I_{OL} = 1.0μA
V_{OH}	High Level Output Voltage	4.95 2.40			V V	I_{OH} = 1.0μA I_{OH} = 5mA
V_{IL}	Low Level Input Voltage	0.0 0.0		0.8 1.5	V V	TTL Interface CMOS Interface
V_{IH}	High Level Input Voltage	2.0 2.0		V_{DD} V_{DD}	V V	TTL Interface CMOS Interface
I_{IN}	Input Leakage Current			1	μA	V_{IN} = V_{DD}
I_{OZ}	High Impedance Output Leakage Current	−10	0.001	10	μA	V_{OH} = V_{DD} or V_{SS}
C_{IN}	Input Capacitance		5		pF	Any Input

A new family of gate arrays with drawn transistor channel lengths of 2 μm ($L_{EFF} \approx 1.5$ m) is already in the development stages and expected to be released for prototyping in the second half of 1985. This new set of arrays will allow integration of logic designs of up to 10,000 2-input-equivalent gates, with typical propagation delays approaching ECL specifications. Table 1.6 lists all the members in the 2-micron family.

Table 1.6. 2-Micron Array Family

Eq. Gates	I/O Cells	Bonding Pads
1.0K	60	68
2.0K	76	84
3.0K	96	104
4.0K	108	120
6.0K	132	144
8.0K	168	184
10.0K	192	208

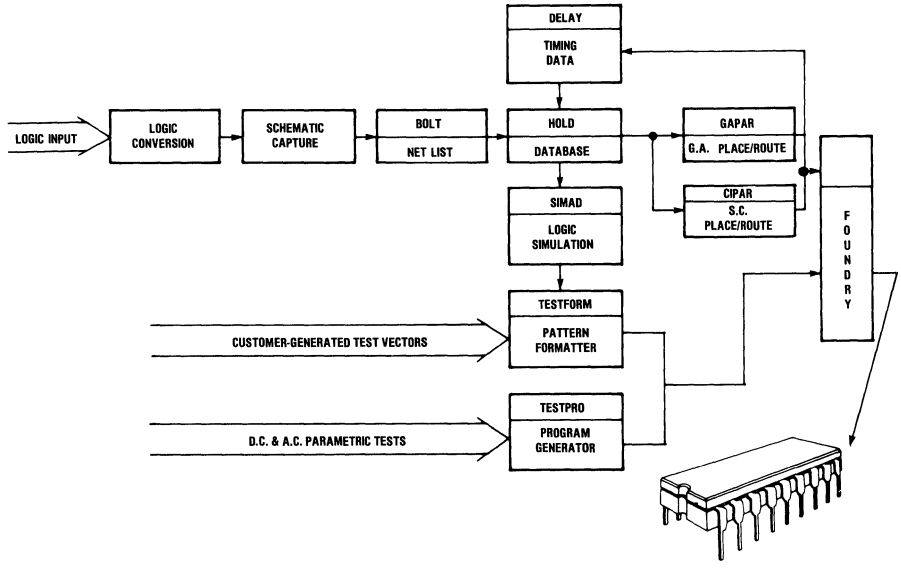
1.3 Semicustom Circuit Development

Recent advances in computer aided design (CAD) tools have greatly simplified the development of integrated circuits, particularly gate arrays and standard cells, allowing turn-around times of four to six weeks from circuit schematic to final tested prototypes. Moreover, tasks that used to require extensive background in integrated circuit design can now be under the control of system designers with little or no previous experience in semiconductor physics.

Gould AMI has developed a totally integrated CAD system that allows the user to perform schematic data capture, logic simulation and timing verification, automated placement and routing of functional macros, followed by timing validation of circuit requirements, including parasitic resistance and capacitance associated with interconnect tracts.

Figure 1.2 depicts the steps involved in developing a semicustom circuit using Gould AMI software capabilities.

Figure 1.2. Semicustom Development Flow



The first task in the semicustom development phase is to format the circuit schematic or logic diagram in terms of precharacterized functional macros. This information is then entered into the system using any of the commercially available CAE workstations that support Gould AMI semicustom libraries.

BOLT™ (Block Oriented Logic Translator) is a hardware description language and a compiler that allows unlimited macro nesting capabilities when describing the logic network in a hierarchical fashion. The BOLT logic description is compiled and the resulting HOLD (Hierarchically Organized Logic Database) file becomes the database common to all the design tools in the system.

SIMAD™ is an event and table driven, MOS logic simulator that creates a logic model of the circuit to be validated from the HOLD database. Nodes may assume any one of six logic states 0, 1, X, L, H, and Z, thus allowing accurate simulation of transmission gates.

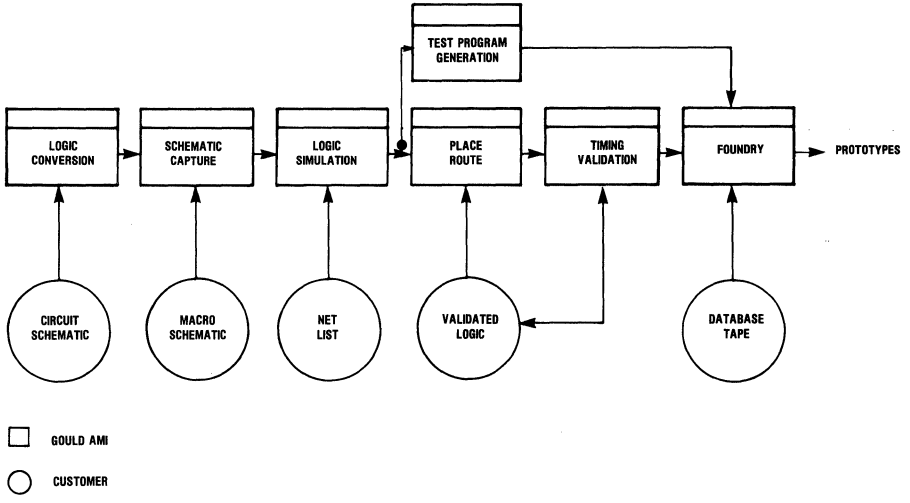
Since each logic device in the model can be assigned propagation delays, SIMAD also allows timing verification, including race detection.

GAPAR™ is the software package that does automatic placement and routing of gate arrays to produce mask data. This software allows completion of at least 98% of the wiring connections on a 100% utilized double metal gate array.

CIPAR™ is the counterpart of GAPAR for creating an error-free standard cell circuit mask layout. CIPAR (Custom Interactive Placement and Routing) is fully automatic though it allows correct-by-construct interactive operation for optimization for placement and routing of critical paths. This feature is also available in GAPAR.

DELAY™ extracts from the layout database all the interconnect resistance and capacitance, which it feeds back to the HOLD file to allow circuit timing validation before the mask tooling is created.

Figure 1.3. 3-Micron Gate Array Customer Interfaces and Development Spans



TESTFORM™ generates compressed functional test patterns from the applied input vectors and the simulated output vectors generated by SIMAD.

TESTPRO™ allows off-line generation of D.C. parametric tests in the FACTOR test language used by Fairchild test systems.

The test program generated by TESTPRO and the test pattern produced by TESTFORM are used to test semicustom circuits on Fairchild Sentry™ test systems.

All Gould AMI semicustom circuits are first screened for functionality at the wafer level, and then fully tested after assembly, according to customer specifications.

Though Gould AMI's CAD Software System is highly portable and compatible with the medium and low priced minicomputers, the system designer is not restricted to use the tools when developing a Gould AMI gate array or standard cell circuit. Instead, he can use any of the commercially available CAE workstations that support Gould AMI semicustom libraries. Furthermore, with Gould AMI the designer is given total interface flexibility, since no restrictions are placed on the type of input data to be supplied by the customer, as shown in Figure 1.3.

2. Semicustom Architectures

2.1 Gate Array Configurations

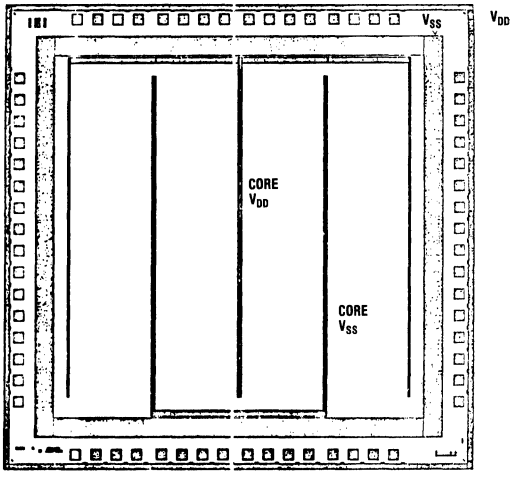
A gate array die can be subdivided into two separate areas called the core and the periphery.

The core contains the basic logic cells and the interconnect channels used to customize the device. It occupies the majority of the die area, and provides most of the signal processing capabilities on the chip.

The outermost area of gate array is filled with the peripheral cells, used to interface with external components, and the power buses which distribute the supply voltages, V_{DD} and V_{SS}, throughout the circuit.

Figure 2.1 shows the typical configuration of a 3-micron double metal gate array. The core is formed by stepping across the die, in the horizontal and vertical direction, a predetermined number of core cells which are bounded by the peripheral cells on all four sides of the chip. The corners of the die are occupied by test devices, alignment and reduction marks, as well as Gould AMI's logo.

Figure 2.1. 3-Micron Double Metal Gate Array Architecture



2.1.1. Gate Array Core Cells

A gate array core cell contains a predetermined number of uncommitted transistor pairs, which are used to build logic gates and flip-flops by selecting the metal interconnect pattern for the required function.

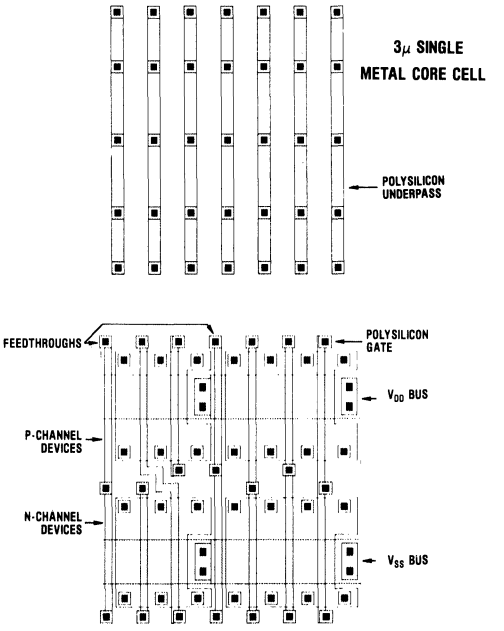
Figure 2.2 illustrates the basic organization of a 3-micron single metal core cell, which consists of five transistor pairs subdivided into two blocks containing two and three pairs, respectively. This configuration allows highly efficient component usage when building sequential logic structures, since a data latch requires a fully utilized single cell. Yet this structure is also very efficient in building combinatorial gates with up to five inputs per cell.

The P-channel devices are located at the top of the cell with the V_{DD} bus running horizontally across the cell between the double set of drain/source contacts to the P-type diffusions. Contact from the V_{DD} bus to the N-type substrate is made within each cell, thus, down bonding from the V_{DD} pad to the die substrate is not required.

The N-channel transistors occupy the bottom half of the cell, sitting in a P-well which is common to all cells within a row. The V_{SS} bus is connected to the P-well within each core cell to minimize substrate drops, thus offering high latch-up protection.

Note that all but one of the transistor pairs in the core cell share a common gate that can be used as a feed-through to cross cell rows. The reason for splitting the gates of one transistor pair is to facilitate the connection of the 4 transistors, within the smallest cell block, as two transmission gates with a common drain/source terminal, widely used in building latches and flip-flops.

Figure 2.2. 3-Micron Single Metal Core Cell

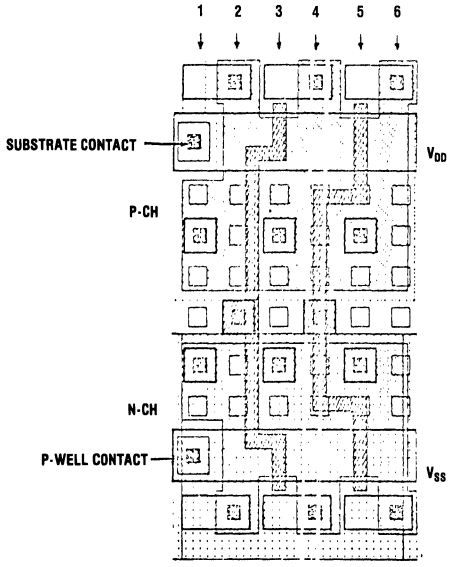


In addition to the device gates, there are two completely uncommitted polysilicon underpasses in each cell, one on the left side of the active area, and the other between the 3 and 2 transistor pair blocks, that can be used to cross the cell without contacting any logic elements.

Outside the active area there are 7 polysilicon underpasses oriented in the vertical or Y direction with five contacts for each underpass. This structure allows routing of ten metal tracks in the horizontal or X direction without contacting any of the cross-unders.

Figure 2.3 shows the configuration of a 3-micron double metal core cell which contains only 2 transistor pairs, and has been designed to allow high component usage as well as highly efficient automated placement and routing of the macros. For this purpose the number of total interconnect channels associated with a given core cell varies, depending on the location of the cell with respect to the center of the die.

Figure 2.3. 3-Micron Double Metal Core Cell



Statistically, cells in the center of the core will require more interconnect channels than those located near the periphery. Therefore, in 3-micron double metal arrays the cell rows in the center of the die have twice as many horizontal tracks as the ones on top and bottom of the core. The number of vertical tracks per cell, however, remains fixed independent of the cell coordinates. The interconnect channels in the horizontal or X direction are routed on the first metal layer, while vertical tracks run on the top layer of aluminum. Contact between the two layers is made through programmable via openings at each intersection of the vertical and horizontal channels.

2.1.2 Gate Array Peripheral Cells

The criteria used in designing the interface cells for gate arrays was to offer maximum flexibility for pin assignment within constraints imposed by the use of prefabrication components. Thus, each peripheral cell can be used as a receiving or a transmitting port, or both. Moveover, any bonding pad within a gate array can be connected to the external V_{DD} or V_{SS} power supplies, and as mentioned before, internal and external power buses can be isolated from each other.

Figure 2.4. Peripheral Cell for 3-Micron Single Metal Arrays

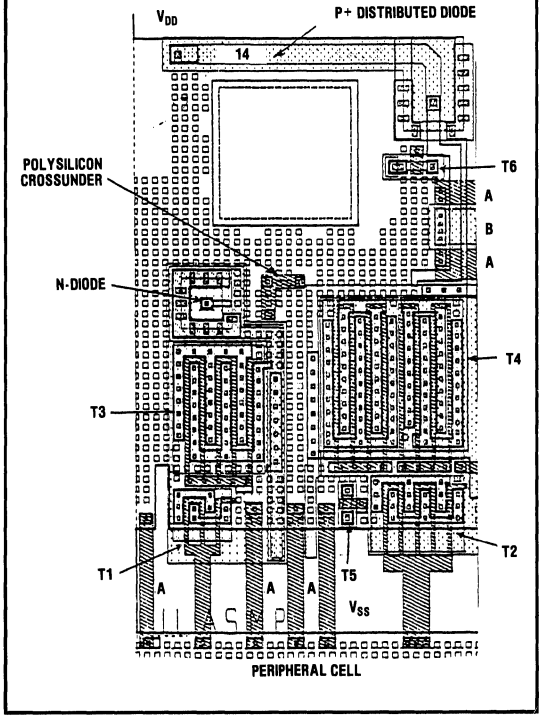


Figure 2.4 shows the component layout for a 3-micron single metal peripheral cell, which in terms of functions and sourcing and driving capabilities is no different from the interface cell for double metal arrays.

There are, however, minor differences between the two families with respect to the physical layout of the components and the material used to connect the internal logic to the peripheral components. In single metal this is accomplished by using polysilicon to cross under the power buses, and the switching characteristics of input and output buffers are not as good as double metal arrays where only aluminum is used for interconnect purposes.

In reference to Figure 2.4, transistors T1 and T2 are the N-type and P-type transistors, respectively, which are used to form a pre-driver when using the cell as an output. T3 and T4 are the N-channel and P-channel drivers.

T5 and T6 are small transistors with relatively high "on" impedance that can be used as on-chip pull-down or pull-up, respectively.

The N – and P + diodes are used to protect the chip against electrostatic discharges when the cell is used as an input.

The peripheral cells are delimited on each side by the V_{DD} and V_{SS} power supply buses which are distributed over the entire chip forming concentric loops, and by proper interconnection of the available components any one of the following functions can be formed:

- TTL/LSTTL Output Driver
- CMOS Output Driver
- Open-Drain Buffer
- Tri-State Buffer
- Analog Switch
- TTL Input Translator
- CMOS Receiver
- V_{DD} Supply
- V_{SS} Supply

3. Semicustom Logic Design

The design of a semicustom gate array or standard cell circuit is very similar to that of a printed circuit board using SSI/MSI components. After the functional behavior for the circuit is specified, the system designer selects from a library of standard functions those which best fit the application, and a logic diagram is then generated.

Functional verification of the logic and timing analysis of critical paths are, in many cases, performed at the breadboard levels. As circuit complexities increase, breadboarding can extend development cycles beyond reasonable limits, and logic simulation is used instead as a vehicle to validate the integrity of the logic design.

The last step in the design phase is to determine the final layout configuration of the logic components. A variety of software packages are available to perform this task, and system designers do not usually get involved in this phase of the development cycle.

The three basic steps described above are essentially the same for printed circuit boards and semicustom devices alike, although the tools used in accomplishing these tasks differ.

This section describes the basic logic functions that are the foundation of complex combinatorial and sequential structures, and outlines the main factors to be taken into consideration when converting an existing design, based on discrete components, to a CMOS semicustom circuit. The user is also introduced in this section to a hardware description language (BOLT) used at Gould AMI to create the logic database, and the main features of a proprietary logic simulator with assignable delays (SIMAD) are also outlined.

3.1 Basic Logic Gates

3.1.1 The CMOS Inverter

The INVERTER is the most elementary logic gate in CMOS technology, and its implementation requires one P-channel and one N-channel transistor connected in series, as shown in Figure 3.1 (b). As long as the input voltage to the common gate of the devices is V_{DD} or V_{SS}, only one of the transistors will be "on" while the other will be turned "off". Under these conditions the power dissipation is a function of leakage currents through reversed biased junctions on the device, and it is negligible for most practical purposes since these currents are typically in the femtoamp range.

On the other hand, as the input voltage is switched from V_{SS} to V_{DD}, or vice-versa, there is a range of values for which both transistors will be "on". During this time there is a low impedance path from the positive to the negative supply "rails", and power will be dissipated.

The transfer characteristics of Figure 3.1 (c) show that when both transistors are "on" there is a current spike which is a function of transistor geometries, supply voltage, and rise and fall times of the input signal.

In addition to the power dissipation associated with current spikes during switching transitions, CMOS gates dissipate power when the output voltage switches states, since the node capacitances need to be charged or discharged. Section 4.6 treats this topic in more detail.

Figure 3.1. CMOS Inverter

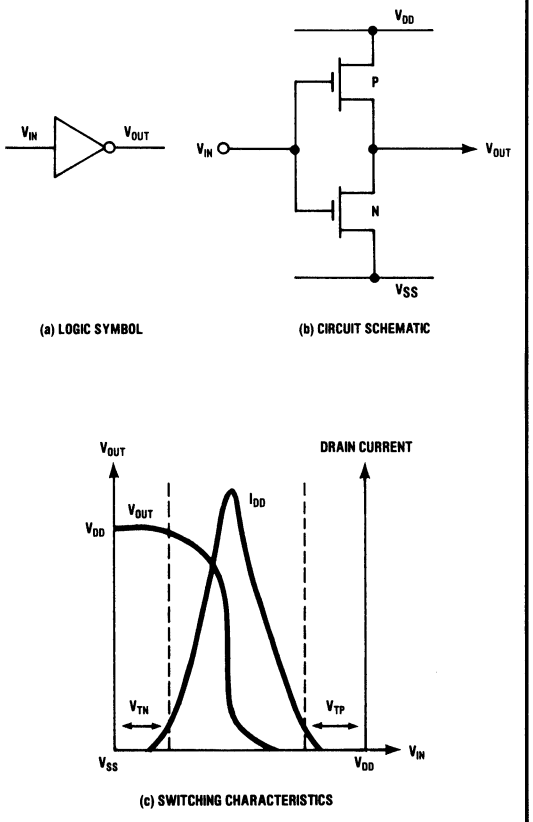
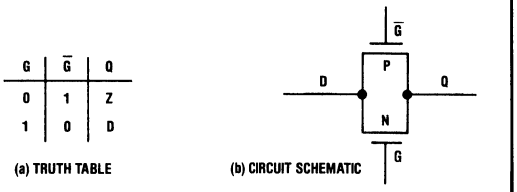


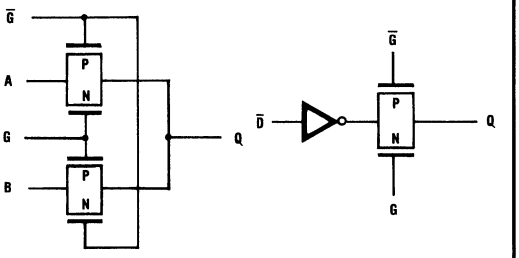
Figure 3.2. CMOS Transmission Gate



G	$\overline{G}$	Q
0	1	Z
1	0	D

(a) TRUTH TABLE

Figure 3.3. Transmission Gate Configurations



3.1.2 Transmission Gate

Unique to MOS technology, this logic element acts as a bidirectional switch widely used in multiplexing/demultiplexing applications. As with the CMOS inverter, only two transistors are required to implement this function, but in this case the transistors are connected in parallel and the gates of the devices are controlled by signals of opposite polarities. Figure 3.2 shows the logic symbol, circuit schematic, and truth table for a CMOS transmission gate.

When the control signals at the gates of the N-channel and P-channel transistors have the right polarity (i.e. G = 1, $\overline{G}$ = 0), both devices are "on" and signals can propagate in both directions through a relatively low impedance path which depends on the size of the transistors, and the voltage levels at the common drain/source terminals of the gate. If G = 0 and $\overline{G}$ = 1, the transistors will be "off" and the gate will be in a high impedance state.

Because of the high impedance characteristics of transmission gates in the "off" state, they can be used very efficiently in building multiplexers, or internal tri-state configurations, although the latter does normally require the use of drivers, as depicted in Figure 3.3.

Transmission gates, also known as transfer gates or bidirectional switches, are widely used in CMOS technologies to build latches and flip-flops, as will be seen later in this section.

3.1.3 NAND Gates

In general, to build a CMOS gate requires two complementary transistors for every input to the gate. Except for transmission gates, these transistor pairs have a common polysilicon gate which is connected to the input signals.

In the case of NAND gates the P-channel transistors are connected in parallel, and the N-channel devices in series. Thus, the output of a NAND gate is low only if all the inputs are high.

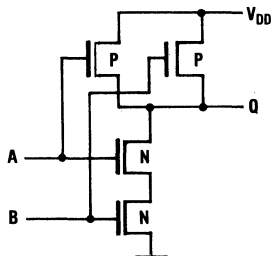
In gate arrays the P- and N-channel transistors in the core have typically the same geometries; however, their driving capabilities are quite different due to inherent properties of CMOS processes. The "on" impedance of P-channel transistors is approximately two to three times higher than that of N-channel devices. As shown in Figure 3.4, NAND gates have the weaker transistors connected in parallel, while the stronger ones are in series. The end result is that these logic elements tend to have more symmetrical propagation delays than other CMOS gates, and their use is recommended whenever close matching of rise and fall times or minimization of propagation delays are desired.

Figure 3.4. 2-Input NAND Gate

(a) LOGIC SYMBOL

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

(b) TRUTH TABLE

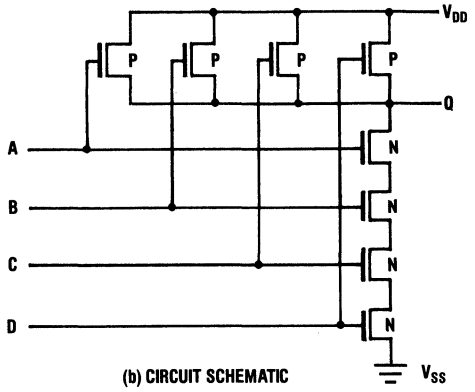


(c) CIRCUIT SCHEMATIC

The number of inputs to the gate can be expanded by simply adding more N-channel devices in series, and an equal number of P-channel transistors in parallel. An example of a 4-input NAND is given in Figure 3.5.

Figure 3.5. 4-Input NAND Gate

(a) LOGIC SYMBOL

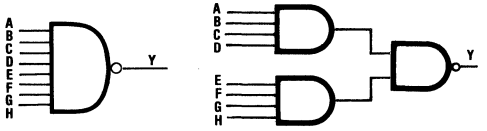


(b) CIRCUIT SCHEMATIC

As the fan-in of a gate is increased, however, the parasitic capacitances and the "on" resistance of the devices connected in series will also increase, and the propagation delay of the gate will be affected. For NAND gates with more than 5 inputs the suggested implementation is the AND-NAND configuration shown in Figure 3.6 for an 8-input gate.

The AND function, in CMOS, is obtained by using NAND gates followed by inverters, although this is transparent to the user since a fully characterized hardware macro for this function already exists in the gate arrays and standard cells libraries.

Figure 3.6. 8-Input NAND Gate



(a) 74LS30

(b) CMOS IMPLEMENTATION

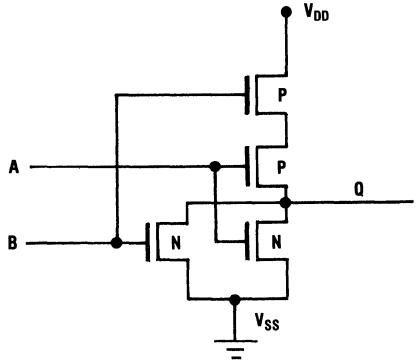
3.1.4 NOR Gates

The NOR gate realizes the same function for negative logic as the NAND gate does for positive logic. This is, the output of a NOR gate is high if all the inputs are low.

Implementing a NOR gate in CMOS technology requires, once again, a pair of complementary transistors for every input. In this case, however, the P-channel transistors are connected in series and the N-channel in parallel. This configuration leads to asymmetrical waveforms, particularly in gate arrays, where the transistor geometries are similar for P- and N-type due to a mismatch between the "on" impedances of the pull-up and pull-down devices.

Figure 3.7. 2-Input NOR Gate

(a) LOGIC SYMBOL



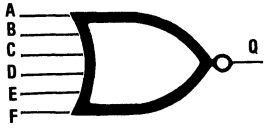
(b) CIRCUIT SCHEMATIC

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

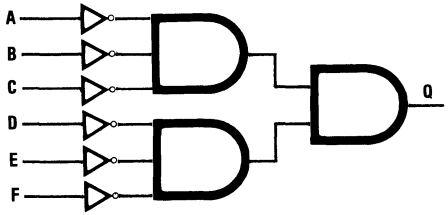
(c) TRUTH TABLE

The asymmetrical characteristics of NOR gates are accentuated as the fan-in of the gate is increased, and critical paths should not be designed with NOR logic. Instead, one can use De Morgan's theorem to obtain a functional equivalence requiring inverters and AND gates as shown in Figure 3.8. If the true and complemented outputs of the signals driving the inverters are available, as would be the case in latches and flip-flops, the inverters of Figure 3.8 would not be required, and the component utilization would be minimized.

Figure 3.8. 6-Input NOR Gate Implementation



(a) 6-INPUT NOR GATE



(b) FUNCTIONAL EQUIVALENCE

An alternate implementation of a six-input NOR gate, using OR-NOR logic is shown in Figure 3.9. This logic structure yields average propagation delays similar to the INVERTER-AND configuration previously discussed, and uses fewer components, particularly for NOR functions with large fan-in.

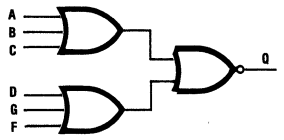
The output waveform produced by the OR-NOR logic structure is not as symmetrical as the one generated with the INVERTER-AND scheme, but it is considerably more symmetrical than that of a standard NOR implementation, where all the P-channel transistors are connected in series.

The OR function is implemented in hardware with a NOR gate followed by an inverter; thus, signals transmitted through will undergo a double inversion, and the overall propagation delays are obtained by adding

Figure 3.9. 6-Input NOR Gate

$$Q = \overline{A+B+C+D+E+F} = \overline{(A+B+C)+(D+E+F)}$$

(a) LOGIC EQUATION



(b) OR-NOR LOGIC

the rising time of the first gate to the falling time of the second and vice versa. Since the mismatch between rising and falling signals of a NOR gate and an INVERTER are in the same direction, when used in series they produce waveforms with better symmetry than that of the individual gates.

3.2 Complex Gates

Series-parallel and parallel-series connection of transistors having the same polarities, in CMOS technology, result in logic structures with two logic levels being highly efficient in terms of component utilization.

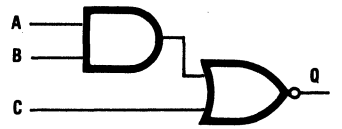
3.2.1 AND-NOR Gates

The AND-NOR function can be obtained by connecting P-channel transistors in a parallel-series combination, while N-channel devices are connected in the opposite manner.

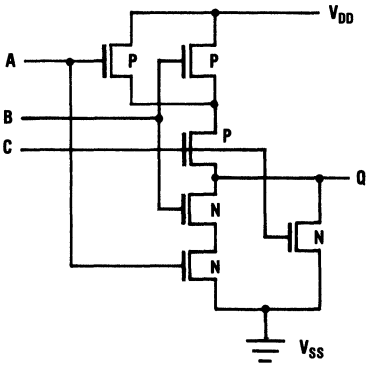
Figure 3.10 shows the internal logic of the AND2NOR2 function, where the pull-up portion of the complex gate is implemented by first connecting the P-channel transistors for A and B in parallel, and these in turn are connected in series with the P-type device whose input is driven by C. The corresponding pull-down devices for A and B are, on the other hand, connected in series with respect to each other, but in parallel with respect to the N-channel device associated with B.

A 4-input wide AND-NOR function requires an additional transistor pair, and its implementation is illustrated in Figure 3.11.

Figure 3.10. AND2NOR2 Function



(a) LOGIC DIAGRAM



(b) CIRCUIT SCHEMATIC

3.2.2 OR-NAND Gates

A dual of the AND-NOR function is realized by reversing the connection of p and n transistors described in the preceding paragraph.

Figure 3.12 depicts the implementation of the OR2NAND2 functional macro. In this case, the P-channel transistors associated with inputs A and B are in series with each other, and in parallel with the PMOS transistor whose gate is connected to input C. This configuration is then reversed for the corresponding N-channel transistors to form the pull-down structure of this complex gate.

An expansion of the OR-NAND function described above is shown in Figure 3.13. In general, expanding the number of inputs to the OR gates requires series connection of additional P-type devices, and parallel connection of the corresponding N-channel transistors, whereas increasing the fan-in of the NAND function is obtained by parallel and series connection to additional PMOS and NMOS devices.

Figure 3.11. AND4NOR2 Implementation

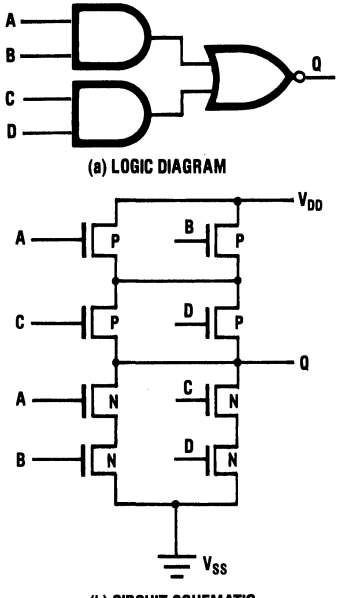


Figure 3.12. OR2NAND2 Complex Gate

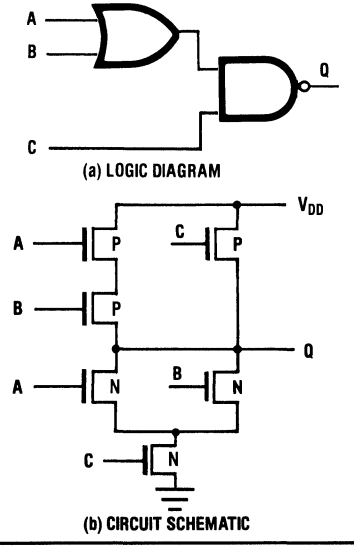


Figure 3.13. OR4NAND2 Function

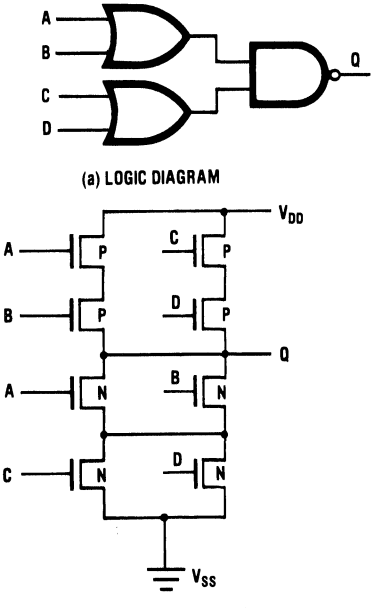


Figure 3.14. EXCLUSIVE OR Function

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

(a) TRUTH TABLE

$Q = \overline{A} * B + A * \overline{B}$

3.2.3 EXCLUSIVE OR and EXCLUSIVE NOR Gates

The output of an EXCLUSIVE OR gate is high only if either one of the inputs is high, but not both. For this reason, it is also known as the non-coincidence gate, since it detects inputs with complementary states, and it is widely used in building full adders, parity generators/checkers and ALUs.

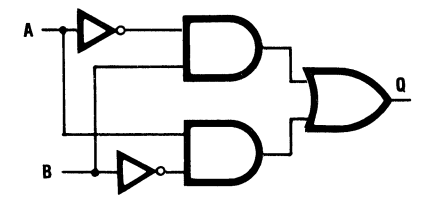
A straight-forward implementation of the EXCLUSIVE OR function, as suggested by the logic equation above, requires AND-OR logic involving the true and complemented states of the input signals. This con-

figuration is particularly useful in building synchronous counters, where the EXCLUSIVE OR function is used in conjuction with the outputs of flip-flops.

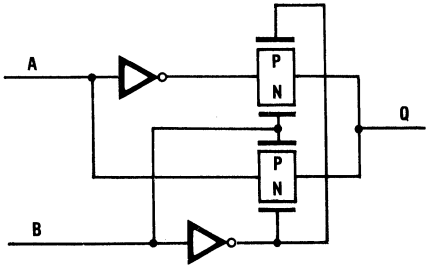
Figure 3.15 illustrates an EXCLUSIVE OR function implemented with AND-OR functional macros, and an equivalent configuration using transmission gates. The first logic structure requires eleven transistor pairs, or 5½ equivalent 2-input gates, versus only four pairs of complementary transistors (2 gates) when transmission gates are used.

The high gate count associated with the logic circuit of Figure 3.15 (a) makes this structure highly inefficient and its use is not recommended. Instead, manipulation of the logic equation leads to an implementation that does not require both polarities of the input signals and can be implemented with 5 transistor pairs, or 2½ gates, as shown in Figure 3.16.

Figure 3.15. EXCLUSIVE OR Implementations



(a) AND-OR LOGIC

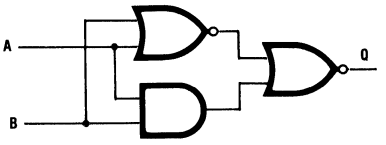


(b) EQUIVALENT LOGIC

Figure 3.16. EXCLUSIVE OR Function

$$F = A*\overline{B} + \overline{A}*B = \overline{(\overline{A}+B)*(\overline{A}+\overline{B})} = \overline{\overline{A*\overline{B}} + \overline{A*B}} = \overline{\overline{(A+\overline{B})} + A*B}$$

(a) LOGIC EQUATION



(b) LOGIC DIAGRAM

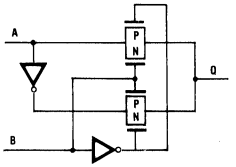
The EXCLUSIVE NOR function is sometimes referred to as the equivalence gate, since its output is high only when both inputs have the same polarity. This function could be realized by simply inverting the EXCLUSIVE OR gates described above, but this configuration would not yield the minimum number of components. Instead, one can take advantage of the fact that when either one, but not both, of the inputs to an EXCLUSIVE OR is complemented, the resulting function is the EXCLUSIVE NOR. Thus, a simple rearrangement of the internal connections of the true and the complement of one of the input signals leads to the EXCLUSIVE NOR configurations shown in Figure 3.17.

Figure 3.17. EXCLUSIVE NOR Gate

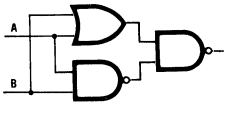
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

(a) TRUTH TABLE

(b) LOGIC SYMBOL



(c) TRANSMISSION GATE STRUCTURE



(d) OR-NAND EQUIVALENT

3.3 Storage Elements

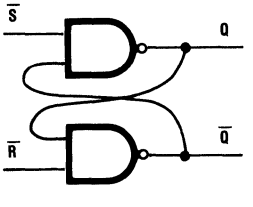
The outputs of a sequential network depend not only on the present state of the input signals, but also on their past values. Therefore, sequential logic design requires memory elements which are used to store information regarding the previous states of the circuit.

This seciton describes the basic elements commonly used in CMOS design for data storage.

3.3.1 Latches

The simplest memory element can be constructed with two cross-coupled NAND gates, as shown in Figure 3.18. The outputs of this circuit can assume one of two stable states, and for that reason it is sometimes called a bistable multivibrator. This circuit, however, is more commonly known as SET-RESET latch.

Figure 3.18. SET-RESET Latch



(a) LOGIC DIAGRAM

$\overline{S}$	$\overline{R}$	Q+
0	0	X
0	1	1
1	0	1
1	1	Q

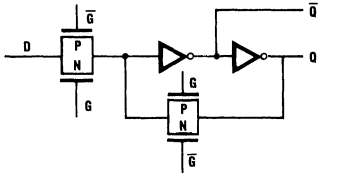
X = INDETERMINATE

(b) STATE TABLE

In this logic element, the condition of the outputs at any given time, other than during transitions, indicates which of the inputs was low just before the output was switched. Note that if S and R are both low, the state of the outputs is indeterminate; consequently, the input signals are not normally allowed to be low at the same time.

Another type of storage element is the clocked latch, whose logic diagram and state table are given in Figure 3.19. In its most elementary form this latch requires one pair of transmission gates, with complementary controls, plus two inverters. This memory cell is the basic building block of CMOS flip-flops, which will be described next.

Figure 3.19. Clocked Data Latch



(a) LOGIC DIAGRAM

D	G	Q+
0	0	Q−
0	1	0
1	0	Q−
1	1	1

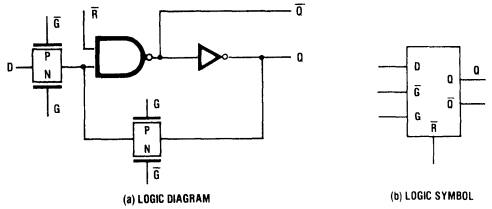
(b) STATE TABLE

When the control signals G and $\overline{G}$ are such that the transmission gate driven by the input data is "on", the latch becomes transparent and signals arriving at the input port will be transmitted to the output node. During this time, the transmission gate on the feedback path is "off".

As the control signals change states, the input transmission gate will be turned "off" while the one in the feedback path will turn "on", latching the data at the output of the inverter driving it.

Preset and clear functions can be added to this memory element by simply using either a 2-input NOR or a NAND gate depending on whether active high or active low signals are required. Because of the inherent speed advantages of NAND gates, the macros in the library have active low preset and clear functions. Shown below are the logic configurations for two clocked latches, one with reset only and the other with reset and set inputs.

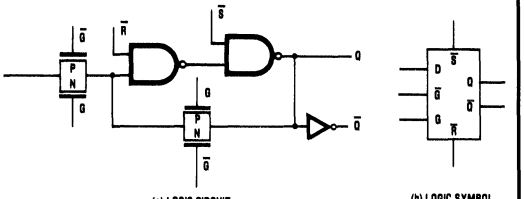
Figure 3.20. Clocked Latch With Asynchronous Clear



(a) LOGIC DIAGRAM

(b) LOGIC SYMBOL

Figure 3.21. D-Latch With Asynchronous Preset and Clear



3.3.2 Flip-Flops

As long as the control signals G = 1 and $\overline{G}$ = 0, the data latches of Figures 3.19 and 3.21 will change state in response to any changes at the input port. In synchronous circuits, this feature might be particularly undesirable. This conflict can be resolved by using a master-slave configuration, instead.

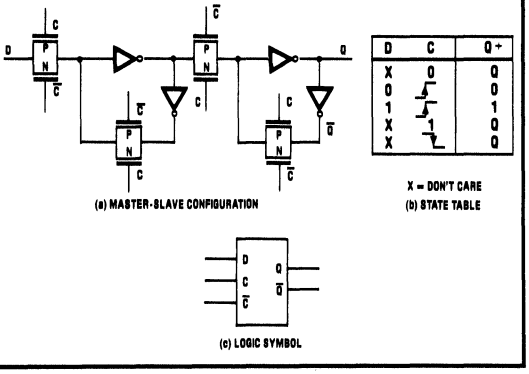
The D flip-flop is the most commonly used storage element in CMOS technology, because its implementation requires the least number of components. In fact, all other types of flip-flops are usually built with this memory element and external gates. Figure 3.22 shows the basic structure of a master-slave flip-flop built out of two data latches triggered on opposite edges of the clock, thus isolating the slave stage from any changes occurring at the output of the master latch as a result of a change in the input data while the C signal is low.

On the low to high transition of the clock, the contents of the master stage are transferred to the slave. At the same time the input transmission gate is turned "off" thus, changes in the input data cannot propagate to the output of the flip-flop.

Data is setup on the negative going edge of the clock, and the time required is calculated by adding the propagation delays through the input transmission gate plus the two inverters in the master latch. The clock to output delay of the flip-flop is, on the other hand, obtained by adding the delays associated with one transmission gate and an inverter in the slave section.

Asynchronous set and reset functions can easily be added to the flip-flop, by simply changing the inverters in the master and slave stages to NOR or NAND gates, depending on whether active high or low signals are desired.

Figure 3.22. D-Type Flip-Flop



D	C	Q+
X	0	Q
0	↓	0
1	↓	1
X	1	Q
X	↑	Q

Figure 3.23. Flip-Flop With Set And Reset

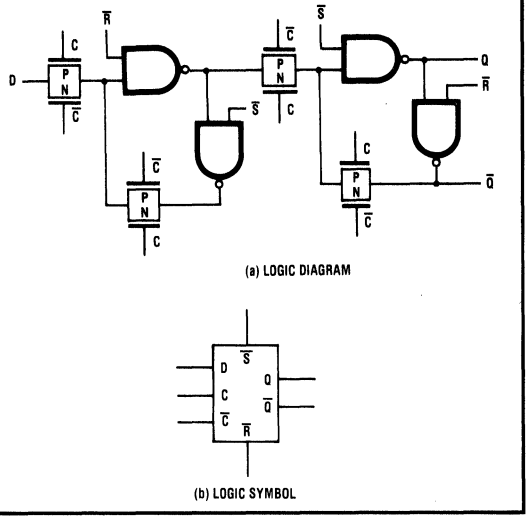
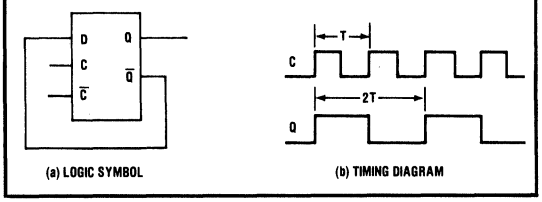


Figure 3.24. Toggle Flip-Flop



If the $\overline{Q}$ output of the D flip-flop is fed back to the input, as shown in Figure 3.24, the resulting configuration is called a "toggle flip-flop", since its output changes state with every incoming clock pulse.

Note that the period of the output waveform, in the toggle flip-flop, is twice as long as the clock period; therefore, the output frequency is one half that of the clock signal. For this reason, this element is sometimes referred to as a "modulo 2 counter" widely used in frequency synthesizers.

Another type of flip-flop, particularly useful in building synchronous counters, is the JK. The state table of Figure 3.25 shows that, depending on the input signal conditions, this flip-flop can inhibit the data from changes at the clock input, or it can behave as either SET-RESET or toggle flip-flop.

A straight-forward manipulation of the logic equation for the JK flip-flop leads to the configuration illustrated in Figure 3.25 (c). Here, a D-type flip-flop and complex gate, identical to the one used to implement the EXCLUSIVE OR function, emulate the behavior of a JK flip-flop, while minimizing the number or required components.

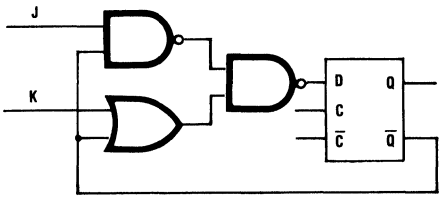
Figure 3.25. JK Flip-Flop

J	K	Q+
0	0	Q
0	1	1
1	0	0
1	1	$\overline{Q}$

(a) TRUTH TABLE

$$Q+ = J*\overline{Q} + \overline{K}*Q = \overline{J*\overline{Q}*(K+\overline{Q})}$$

(b) LOGIC EQUATION



(c) LOGIC DIAGRAM

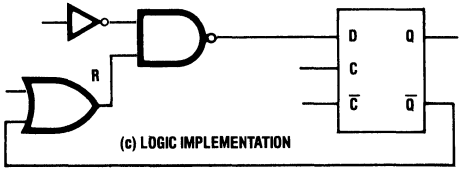
Since the next state of a D flip-flop is always the same as the input data before the clock pulse, its characteristic equation is Q+ = D. Thus, converting another flip-flop to a D-type plus some additional logic gates can easily be accomplished by equating the characteristic equations of both flip-flops, as illustrated in Figure 3.26 for a SET-RESET flip-flop.

Figure 3.26. S-R To D Flip-Flop Conversion

D-TYPE $Q^+ = D$

SR-TYPE: $Q^+ = S + \overline{R}*Q$ $\qquad D = S + \overline{R}*Q = \overline{\overline{S}*(R+\overline{Q})}$

(a) CHARACTERISTIC EQUATIONS (b) LOGIC TRANSFORMATION



(c) LOGIC IMPLEMENTATION

3.4 Logic Reconfiguration

For many years, logic designers have been accustomed to use standard, off-the-shelf components designed to cover a wide range of applications. Because of the general nature of these devices, some the functions provided in the package end up not being utilized, with a consequent waste of P.C. board area associated with the unused pins.

Moreover, the level of integration encountered on discrete devices is relatively low, and several packages per logic function would be needed to meet today's system requirements where it is common to find 32-bit wide logic structures. Since the number of packages on a board has a direct effect on system reliability, designers had to compromise between performance and dependability.

State-of-the-art semicustom devices combine the logic flexibility achievable with gates and flip flops, with a level of integration equivalent to several thousand gates and upwards. Furthermore, present on-chip delays attainable with CMOS are already comparable to Schottky-Transistor-Logic speeds, and are expected to be in the subnanosecond range in the very near future.

In semicustom design, the most efficient silicon usage is typically achieved by converting large functional

blocks into their more primitive components, namely gates and flip-flops. Although standard cell libraries tend to offer more complex functional macros than gate arrays, as the complexity of the function is increased it becomes uneconomical to develop dedicated macros for all the possible variations of the basic function. Instead, user requirements are met by using "software macros" built from more basic elements for mask layout purposes.

Hence, the first step in a typical semicustom development is to prepare the schematic diagram in a form directly compatible with the library of macros for the selected technology. In doing so, the logic designer needs to take into consideration several factors which will influence the complexity as well as the performance of the circuit.

Figure 3.27. Equivalent Gate Networks

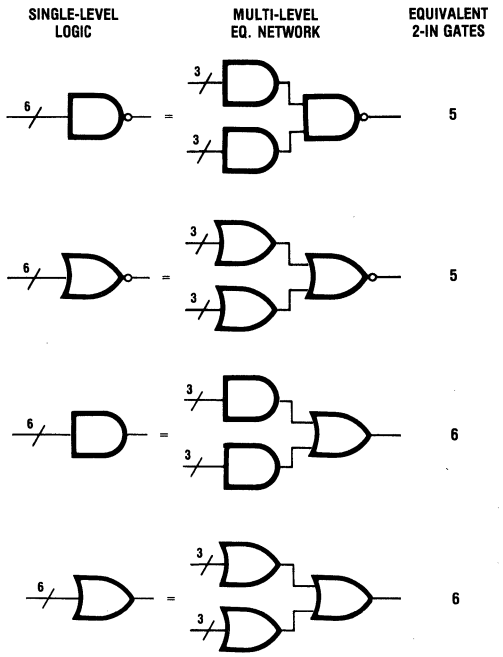
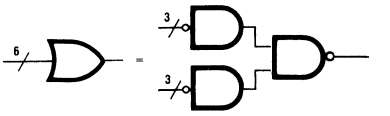


Figure 3.28. OR Gate Equivalence



3.4.1 Fan-In Considerations

In describing the basic CMOS gates, it was mentioned that the performance of a gate is degraded as the number of inputs to the gate is increased. As a rule, logic gates requiring more than 5 inputs should be implemented in two or more levels of logic by using simple transformation techniques derived from the basic theorems of Boolean algebra.

Figure 3.27 shows how to convert 6-input CMOS gates into a 2-level network by straight application of the distributive law.

If the complement of the input signals in an OR gate is available, one could use De Morgan's theorem to obtain an alternate 2-level network with better performance characteristics than the one shown on Figure 3.28.

3.4.2 Fan-Out Considerations

Since the rise and fall times of a CMOS gate increase almost linearly with increasing load capacitance, certain restrictions need to be imposed regarding the maximum number of unit loads that can be driven from a single gate.

In describing the CMOS INVERTER, it was mentioned that as the input signal to the gate changes states, power is dissipated during the finite time where both transistors are "on", thereby creating a low impedance path between V_{DD} and V_{SS}. The longer it takes to switch the input signal, the longer the transistors will be "on", and the more power the gate will dissipate.

On the other hand, if the rise and fall times of all the internal nodes in the circuit are optimized, the power dissipation due to current spikes during input transitions can be minimized and, in most cases, neglected.

In general, the speed degradation of a gate, rather than power dissipation, is the limiting factor when determining the maximum allowable capacitive load at the output node. Therefore, it might be necessary to add redundant logic to the circuit to meet the speed requirements, depending on the particular application.

The propagation delay of a CMOS gate can be approximated by:

$$t_d = t_{dx} + k_{t_{dx}} C \text{ where}$$

t_d = Propagation delay of the gate in nanoseconds.
t_{dx} = No-load (Intrinsic) delay.
$k_{t_{dx}}$ = Fan-Out dependent time delay (Ns/pF).
C = Total output node capacitance in picofarads.

In semicustom devices with only one layer of metallization, polysilicon underpasses are needed to route signals under metal tracks. When this happens, the designer must take into consideration the additional delay introduced by the underpass resistance, which is two orders of magnitude higher than that of aluminum, and consequently cannot be neglected.

The equation above implies that every underpass will cause the total delay to increase by approximately .3 Ns/pF. Therefore, in order to optimize circuit performance critical paths should only be routed with metal interconnect, whenever possible. Statistically, however, as the circuit complexity increases it becomes infeasible to entirely eliminate the use of underpasses when routing signals in single metal gate arrays and standard cells.

The number of underpasses in a given path is dependent both on the placement of the functional macros that generate and propagate the signal under consideration, and the fan-out of each gate in the signal path. Statistically, a critical path in a 3-micron single metal gate array is expected to contain no more than ½ of an underpass per fan-out of each gate in the path, whereas non-critical paths can be routed with no more than 1½ underpasses per fan-out per gate. Thus, if a critical signal propagates through three logic gates with fan-outs of 3, 4, and 2 respectively, the maximum number of underpasses in the path will be 1.5 for the first gate and 2 and 1 for the other gates, respectively. Moreover, the total delay of the first gate will increase by .45 Ns/pF, while the second and third gate delays will increase by .6 and .3 Ns/pF, respectively.

These statistical figures of merit are normally used at the onset of a semicustom development for the purpose of determining if the circuit requirements are within the capabilities of 3-micron single metal CMOS technology.

Nonetheless, one of the required steps in the development of every semicustom device is to perform post-layout timing validation of the logic to include all the parasitic resistance and capacitance due to interconnect tracks, which is extracted from the geometrical database.

In double metal technology there are no polysilicon underpasses. The propagation delay equation is also:

$$t_d = t_{dx} + k_{t_{dx}} C$$

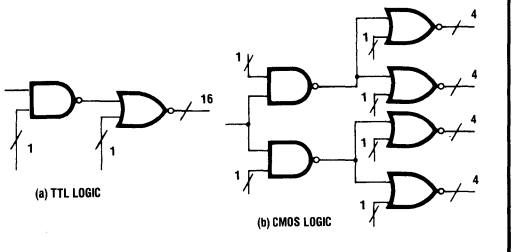
Where C is the total output node capacitance of the gate, which is the sum of the individual contributions of the gate pairs connected to the node plus the interconnect capacitance due to metal tracks.

Again, the parasitic interconnect capacitance is not actually known until the mask layout is completed, and statistical values are instead used in the initial stages of the design phase. The propagation delay vs. fan-out tables on the data sheets of Section 7 already include interconnect capacitance equivalent to 500μm of metal loading per fan-out. Hence, when using these tables a fan-out of 2, for instance, is equivalent to the capacitance associated with 2 gate-pairs plus 1000μm of metal interconnect.

If the fan-out exceeds the values given on the tables, the output node capacitance per fan-out should be .25pF including metal interconnect. Thus, if the gate fan-out is 10 the total node capacitance should be 2.5pF.

As a rule of thumb, if a CMOS gate with heavy fan-out is part of critical paths on the chip, redundant circuitry should be added to minimize the propagation delay of the required signals. For example, assume that a 2 input NAND gate driving a 2-input NOR with a fan-out of 15 is part of three critical paths in a CMOS semicustom circuit. Figure 3.29 shows a possible implementation where the NOR gate has been replicated three times, whereas the NAND gate has only been duplicated.

Figure 3.29. Fan-Out Distribution



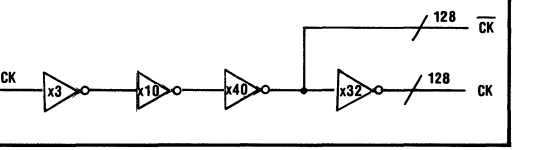
The amount of redundancy introduced in the circuit because of fan-out versus speed trade-offs is entirely dependent on the individual application requirements, and the user is advised to study each case carefully. Note that every time a gate is duplicated the fan-out of the previous gate is increased; therefore, in some cases redundant gates might need to be added all the way back to the input pins.

When long counters or shift registers are used in CMOS circuits, special care must be taken in minimizing the skew between the opposite phases of the clock signal. As we saw in preceding paragraphs, both polarities of the clock are needed in CMOS registers to control the transmission gates in the latches. Typically, one of the phases is derived from the other by using an INVERTER, and there will be a finite time when all the transmission gates in the flip-flop will be "on" simultaneously. If this time is long enough, due to excessive skew in the clock drivers, master-slave flip-flops could become transparent latches, and the circuit could malfunction.

In some cases, flip-flop macros only require one edge of the clock, since the opposite edge is generated internally. In the most general case, however, both polarities of the clock need to be generated outside the flip-flop. These clock drivers are standard functions in the cell libraries, but in gate arrays they are constructed by paralleling inverters in a tree configuration, where the maximum load allowed on any given inverter is 2 flip-flops, which is equivalent to 4 gate-pairs. Also, as a rule, the clock signals are distributed through the chip without polysilicon crossunders, thus minimizing propagation delays.

Keep in mind that one of the clock edges is derived from the other; hence, one of the clock drivers will have a heavier load than the other, since in addition to the flip-flops, it has to drive the inverters that generate the opposite clock signal. Thus, in building a clock tree one begins by figuring out the number of inverters needed to drive just the flip-flops, based on the rule outlined above of 2 flip-flops maximum per single inverter, and then proceeds backwards in building the rest of the tree using the same rule of 4 gate-pairs per inverter, until the load of the final driver is less than 4 gates. Figure 3.30 illustrates this technique, applied to a 64-bit shift register. The number inside the drivers indicates the number of paralleled inverters in a gate array.

Figure 3.30. Clock Tree for a 64-Bit Shift Register



3.4.3 Gate Count

Over the years, the complexity of an integrated circuit was measured in terms of total number of transistors on the chip. For CMOS semicustom devices, however, it is common practice to use 2-input gates to describe the level of integration on the chip.

To facilitate the task of determining the 2-input gate equivalence of a logic structure, conversion tables are provided for all Gould AMI macrocells, as well as for TTL and CMOS standard SSI/MSI functions. Table 3.1 shows the gate equivalence of basic logic functions.

Table 3.1. Gate Count for Basic CMOS Functions

Basic Function	Gate Equivalence
Inverter	.5 or 1
Transmission Gate	.5 or 1
1 To 5-In NAND	.5 Per Input
6 To 10-In NAND	.5 Per Input + 2
1 To 5-In NOR	.5 Per Input
6 To 10-In NOR	.5 Per Input + 2
1 To 4-In AND	.5 Per Input + .5
5 To 8-In AND	.5 Per Input + 2.5
1 To 4-In OR	.5 Per Input + .5
5 To 8-In OR	.5 Per Input + 2.5
Exclusive OR/NOR	2.5
AND-OR-INVERT	.5 Per Input
OR-AND-INVERT	.5 Per Input
2 TO 1 MUX	2
Set-Reset Latch	2
Data Latch With Set OR Reset	2.5
Data Latch With Set AND Reset	3
D Flip-Flop With Set OR Reset	5
D Flip-Flop With Set AND Reset	6 or 7
J-K Flip-Flop	8

Inverters used to build drivers, as discussed in the preceding paragraph, can be counted as .5 gates per inverter; otherwise, their equivalent count should be 1 gate, because of layout constraints.

Similarly, transmission gates with complementary control signals, as in multiplexers, can be counted as .5 gates, but if the control signals are independent they are counted as a full gate.

The equivalent gate count for CMOS and TTL standard devices, given on Table 3.2 and Table 3.3, respectively, is based on the assumption that all the device functions are used. Furthermore, for counters and registers the given gate count already takes into consideration the fan-in and fan-out limitations inherent in CMOS semicustom devices, covered in the preceding paragraphs.

In most applications implemented with discrete components some of the package pins are not normally exercised; therefore, the internal logic could be reduced accordingly, leading to a more efficient use of silicon. The easiest way to accomplish this task is to refer to the logic diagrams for the specific devices, which are normally supplied on the data sheets.

High voltage or current drivers have been deleted from the list of standard components, as well as memory devices, and Schmitt trigger buffers. If any of these components needs to be integrated, consult Gould AMI for feasibility.

Table 3.2. Gate Equivalence for CMOS Standard Components

Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.
4000	4	4022	40	4069	3	40163	54
4001	4	4024	40	4070	10	40174	35
4002	4	4026	60	4071	6	40175	23
4006	103	4027	23	4072	5	40192	65
4007	2	4028	26	4073	6	40193	62
4008	32	4029	80	4075	6	4510	82
4009	3	4030	10	4076	49	4511	52
4010	3	4032	63	4077	10	4512	23
4011	4	4034	110	4078	6	4514	78
4012	4	4035	39	4081	6	4515	78
4013	12	4038	64	4082	5	4516	79
4014	51	4040	66	4089	80	4518	44
4015	58	4041	6	4094	86	4519	36
4017	48	4042	13	4099	82	4520	42
4018	41	4043	24	40106	30	4532	39
4019	10	4044	24	40107	18	4555	15
4020	77	4051	15	40160	59	4556	11
4021	55	4068	6	40162	59		

Table 3.3. Gate Count for TTL Discretes

Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.
7400	4	7470	14	74150	61	74248	62
7401	4	7471	18	74151	28	74249	62
7402	4	7472	14	74152	28	74251	32
7403	4	7473	16	74153	24	74253	26
7404	3	7474	12	74154	50	74257	18
7405	3	7475	10	74155	20	74258	16
7406	3	7476	16	74156	20	74259	68
7407	6	7477	10	74157	15	74260	6
7408	6	7478	18	74158	17	74261	72
7409	6	7480	16	74159	50	74265	5
7410	5	7482	26	74160	65	74266	12
7411	6	7483	55	74161	60	74273	44
7412	5	7485	50	74162	65	74276	38
7415	6	7486	10	74163	60	74278	38
7416	3	7487	17	74164	50	74279	10
7417	6	7490	40	74165	70	74280	56
7420	4	7491	50	74166	65	74281	163
7421	5	7492	35	74167	60	74283	62
7422	4	7493	21	74168	70	74290	41
7423	7	7494	35	74169	70	74293	37
7425	6	7495	40	74170	120	74295	41
7426	4	7496	40	74173	40	74298	36
7427	5	7497	110	74174	35	74299	132
7428	4	7498	35	74175	25	74323	132
7430	6	7499	45	74176	40	74348	49
7432	6	74100	25	74177	38	74351	64
7433	4	74102	26	74178	55	74352	26
7437	4	74103	16	74179	55	74353	28
7438	4	74106	18	74180	27	74363	25
7440	4	74107	16	74181	104	74364	47
7442	30	74108	18	74182	34	74373	33
7443	30	74109	18	74183	15	74374	55
7444	30	74110	12	74190	70	74375	10
7445	30	74111	18	74191	66	74376	40
7448	60	74112	18	74192	73	74377	72
7449	50	74113	18	74193	67	74378	54
7451	8	74114	18	74194	59	74379	40
7452	7	74116	25	74195	38	74381	160
7453	10	74120	15	74196	40	74386	12
7454	9	74135	20	74197	38	74390	52
7455	6	74136	10	74198	88	74393	42
7460	5	74138	25	74199	86	74395	40
7461	6	74139	22	74226	70	74398	36
7462	9	74145	24	74245	52	74399	36
7464	10	74147	35	74246	58	74670	125
7465	10	74148	35	74247	58		

Fuse or field programmable devices can be subdivided into three different groups: PROMs, PALs, and FPLAs.

All three types have the same basic architecture consisting of AND-OR arrays, where either or both of the arrays are user programmable, and they allow a level of integration approximately an order of magnitude higher than that achievable with SSI/MSI discretes.

Typically, fuse programmable devices are customized by defining the Boolean expressions for the output functions, and the component utilization varies depending on the particular application. Therefore, to determine the equivalent number of 2-input gates for one of these devices, the Boolean expressions used in generating the fuse pattern need to be known.

In general, the component utilization of field programmable devices is somewhere between two and three hundred gates, although higher density components are being designed using CMOS technology.

After all the internal circuitry in a semicustom device has been accounted for in terms of 2-input gates, an additonal gate per output driver should be added to the gate count, because of circuit design considerations. Likewise, input buffers should be counted as 1 gate for CMOS and 2 gates for TTL receivers.

3.5 Net List Generation

Gould AMI provides the most advanced computer aided design (CAD) tools available for MOS/VLSI design in an integrated system which supports gate arrays, standard cells, and full custom circuits. This system provides programs for logic simulation, automatic placement and routing, post-layout timing verification, and test program development.

All the software programs operate from a Hierarchically Organized Logic Database (HOLD) that contains a complete logical, electrical, and structural description of the circuit being developed. To generate this database the user first creates a textual description of the circuit using a hardware description language called BOLT (Block Oriented Logic Translator).

Although the BOLT language supports a hierarchical circuit description approach with unlimited macro nesting capabilities, the logic simulation and timing verification packages require that the circuit be described at the logic level using existing logic macros, for the corresponding product family.

The BOLT file can be created using an ordinary text editor by first labeling each logic component in the circuit with the BOLT syntax given on the data sheet for the associated macro. Even though the BOLT language is very flexible and allows the module name to be anywhere in the node list, it is recommended to follow the format used on the data sheets with output nodes first, followed by the name and input nodes, in that order. A semicolon character is used to terminate the BOLT statement. Figure 3.31 shows the coding of an EXCLUSIVE OR module.

Figure 3.31. BOLT Syntax of an EXCLUSIVE OR


```
Y .E02 A B; GATE ARRAYS
Y .E02X A B; STANDARD CELLS
```

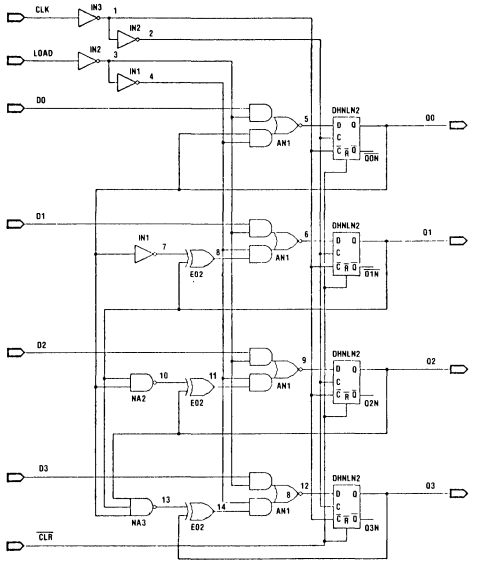
The next step is to assign a number or a name to each node in the circuit connected to other components. It is also recommended to label unused nodes, to facilitate reading and checking the net list file. If a node is left unnamed, a question mark should be entered in the corresponding field of the BOLT statement for that component or module.

Coding and checking the circuit are facilitated by subdividing the logic diagram into functional blocks chosen in such a way as to minimize the number of interconnections between blocks. By doing so, major portions of the circuit can be coded separately, and later combined to form the entire circuit. For very large circuits, this may be the only way to proceed because of the limitations on file size with some text editors.

Figure 3.32 shows a circuit coding example of a 4-bit synchronous counter with asychronous clear, assumed to be part of a larger logic structure. The signals interfacing with other portions of the circuitry were assigned names, whereas the internal nodes were numbered following a left-to-right, top-to-bottom sequence. This is only a suggested procedure which makes the BOLT code easier to implement and check.

The macro names used in this example indicate that 3-micron technology had been chosen to implement the logic.

Figure 3.32. 4-Bit Synchronous Counter



The BOLT language is a free format language. This means that single statements may be written on multiple lines, while multiple statements can be written on the same line. These features allow insertion of blank lines anywhere in the file to delimit sections for easy identification purposes.

Comments are preceded and terminated by the % symbol, and are allowed to be inserted on any and all of the lines, mixed with the BOLT source code.

Shown below is the BOLT net list for the 4-bit counter example of Figure 3.32.

```
% 4-BIT SYNCHRONOUS COUNTER NET LIST %
    BEGIN
      Q0 Q0N .DHNLN2 5 2 1 CLR;
      Q1 Q1N .DHNLN2 6 2 1 CLR;
      Q2 Q2N .DHNLN2 9 2 1 CLR;
      Q3 Q3N .DHNLN2 12 2 1 CLR;
      5 .AN1 D0 3 Q0 4;
      6 .AN1 D1 3 4 8;
      9 .AN1 D2 3 4 11;
      12 .AN1 D3 3 4 14;
      8 .E02 7 Q1;
      11 .E02 10 Q2;
      14 . E02 13 Q3;
      7 .IN Q0;
      10 .NA2 Q0 Q1;
      13 .NA3 Q0 Q1 Q2;
      1 .IN3 CLK:
      2 .IN2 1;
      3 .IN2 LOAD;
      4 .IN1 3;
    END;
```

3.6 Logic Simulation

Validation of logic networks, and development of test patterns are performed at Gould AMI with a proprietary software program called SIMAD (SIMulator with Assignable Delays) developed for MOS networks.

SIMAD creates a logic model of a circuit from the user supplied BOLT file which is compiled and stored in a HOLD database. The logic model of the circuit is extracted from this central database with no invervention from the user. Customer-generated input patterns are interactively entered into the system, and used to validate the functionality of the circuit. The user must specify simulation control and output formatting information, and the results are saved on the computer disk pack, for later use by the TESTFORM test pattern formatter.

Each logic device in the model can be assigned propagation delays, thus allowing for timing verification, including limited race detection. All SIMAD timing is understood in terms of integer-multiples of a user specified "Elementary Time Unit" (ETU).

In SIMAD a node may assume any one of six logic states: 0, 1 X, L, H, and Z. The first three states represent the normal driven states, with X being the result of a "clash" between 0 and 1. L, H, and Z represent floating logic states preserved by load capacitance at outputs of transmission gates which are in the high impedance state. SIMAD assumes that a floating logic state will not decay as a result of leakage currents.

The subject of logic simulation using SIMAD is treated in more detail in regularly scheduled training courses offered at Gould AMI.

4. Circuit Design

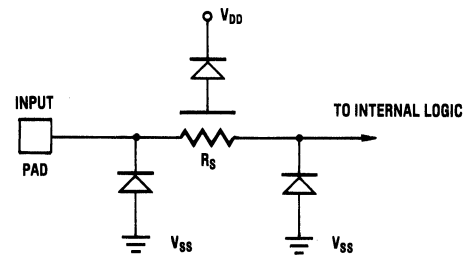
4.1 CMOS Input Protection

Because of the insulating layer of oxide between the gate and the body of a CMOS transistor, the equivalent input network can be approximated by a low-leakage capacitor in parallel with a very high impedance resistor. As a consequence, a typical CMOS gate input is susceptible to electrostatic charge build-up that can develop damaging voltage levels across the high impedance input.

If the breakdown voltage of the gate oxide is exceeded, the gate can be permanently shorted to the substrate, and the circuit will stop functioning.

To avoid this problem, all semicustom devices are protected against electrostatic discharge, with an input network consisting of a series resistor and shunt diodes, as illustrated in Figure 4.1. The resistor-diode combination clamps the input voltage to within a diode drop from the power rails, thus preventing gate oxide ruptures due to electrostatic discharges in excess of 2000 volts.

Figure 4.1. Input Protection Network



The series resistor is obtained by diffusing p+ material into the n-type substrate, thus creating a distributed diode whose cathode is connected to V_{DD} when the power supply is turned on. The presence of this diode imposes certain limitations on the power-on sequence. That is, V_{DD} should always be turned on before signals, particularly from low impedance sources, are applied to the device inputs. Conversely, input signals should be removed before turning V_{DD} off. Failure to do so could trigger a latch-up mechanism due to a parasitic SCR inherent in all CMOS devices, which could be destructive.

Furthermore, to avoid excessive current through the shunt diodes, the maximum allowable input current in a semicustom device is 10 milliamperes, and the quiescent input voltage should not exceed V_{DD} or fall below V_{SS} by more than .5 volts.

4.2 Input Thresholds

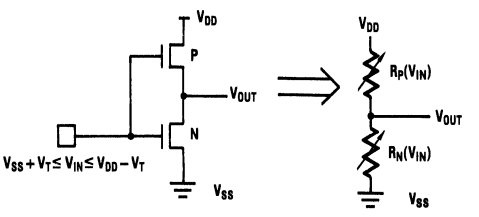
The threshold voltage of a CMOS transistor is defined as the minimum gate voltage required to create a conductive channel between drain and source. This is a process dependent parameter, and cannot be controlled by the circuit designer.

The input threshold of a CMOS logic gate is, on the other hand, dependent on device geometries and, to a certain extent a controllable parameter for design purposes, since different types of gates have different thresholds. Typically, CMOS logic thresholds are specified as 30% and 70% of the supply voltage for maximum V_{IL} and minimum V_{IH}, respectively. That is, for a device operating at 5 volts, a maximum "0" level would be 1.5 volts, whereas the minimum "1" level would be 3.5 volts.

The specified input levels for TTL logic families are .8 volts and 2.0 volts for maximum and minimum "0" and "1" levels, respectively. Since the minimum TTL "high" input level is lower than the minimum level recognized by a CMOS gate, level translation buffers are used when interfacing CMOS semicustom devices with TTL or LSTTL components.

As long as the input voltage to a CMOS logic gate is within $V_{SS} + V_T$ and $V_{DD} - V_T$, where V_T is the transistor threshold defined above, the pull-up and pull-down devices will be both turned "on", and the equivalent network for the gate is a voltage controlled resistor divider as shown in Figure 4.2.

Figure 4.2. CMOS Network Equivalence

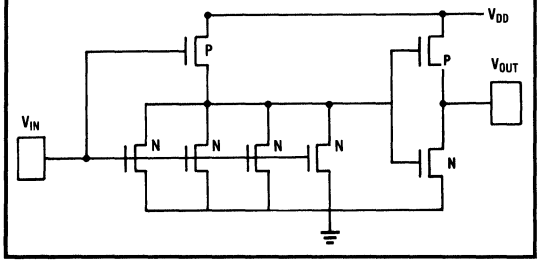


To recognize the TTL "1" level, the pull-down transistor of Figure 4.2 is made larger than the pull-up device, and the output voltage of the gate is thus shifted to a level that can be recognized by a CMOS gate. In standard cell level translators, the device channel length is the same for P and N-channel types, and impedance ratios are controlled by varying the channel width.

In gate arrays, the device geometries are the same for both transistor types, and ratioing is accomplished by series-parallel combination of pull-up and pull-down devices.

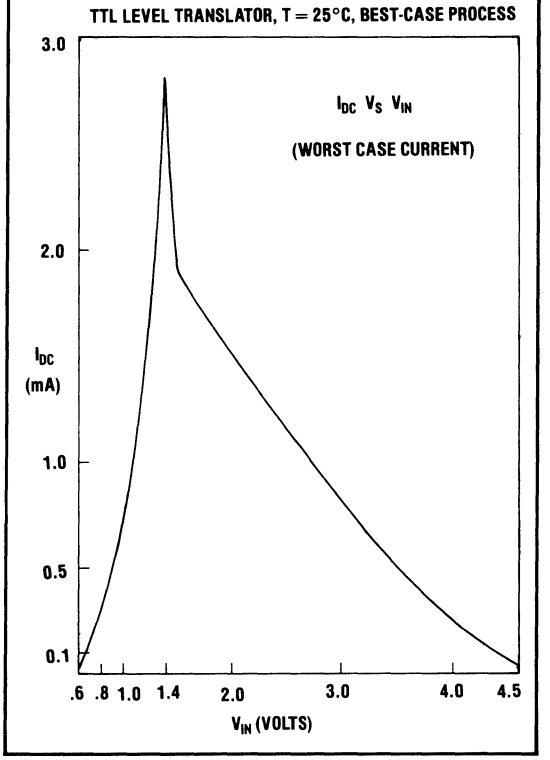
A typical gate array TTL level translator is shown in Figure 4.3, where the gate pull-up consists of a single P-channel device, whereas the pull-down is formed by paralleling four N-channel transistors.

Figure 4.3. Gate Array Level Translator



Level translators will dissipate power unless the input signals are switched all the way to the rails, and for a given V_{DD} the gate current is dependent on the input voltage, as shown in Figure 4.4. Therefore, if power dissipation is an important consideration, it is recommended that a pull-up be connected to the gate input to fully switch off the P-channel device.

Figure 4.4. I_{DD} vs. V_{IN} for TTL Level Translator



4.3 Schmitt-Trigger Input Buffers

Schmitt-trigger action takes place when a gate switches at different voltage levels for positive- and negative-going signals. This feature is typically required when the device is to be operated in a noisy environment, or when the input signals have long rise and fall times.

Schmitt-trigger buffers are said to have hysteresis, which is defined as the voltage difference between the positive- and the negative-going thresholds. A Schmitt-trigger buffer, widely used in 3-micron single metal arrays, is shown in Figure 4.5, along with its transfer characteristics.

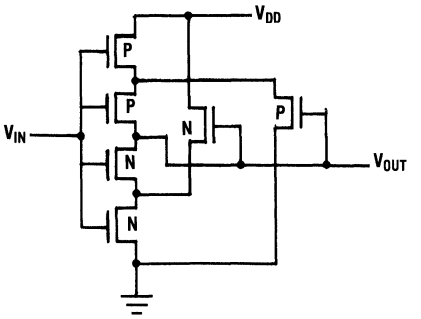
4.4 Floating Inputs

The high input impedance characteristics of CMOS gates, along with leakage currents inherent in any semiconductor junction, will cause logic gates with floating inputs to be biased in the linear region where the pull-up and pull-down devices are both on.

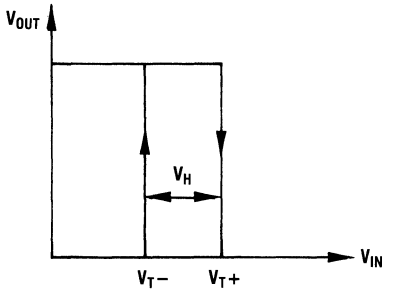
Besides increasing the overall power dissipation in the circuit, floating gates will have indeterminate output levels, and it is strongly recommended to use on-chip or off-chip components to terminate either to V_{DD} or V_{SS} those gate inputs that could be temporarily left open or unconnected.

On-chip resistors for semicustom devices are obtained by biasing high impedance transistors into saturation. These resistors, however, are highly susceptible to threshold variations, and the equivalent impedance can vary by as much as 300% over the entire range of process variations.

Figure 4.5. Schmitt-Trigger Input Buffer



(a) Schematic Diagram



(b) Transfer Characterisitics

Figure 4.6 shows the maximum and minimum values of pull-up devices for the 3-micron family of gate arrays versus varying input voltage. The temperature effects on the equivalent impedance of these devices are also depicted in Figure 4.6.

Standard cell libraries include input buffers with built-in pull-ups and pull-downs with similar characteristics as those for gate arrays. In both families, the equivalent impedance of these devices, when biased into saturation, is relatively large to minimize power consumption on the chip.

Figure 4.7 illustrates the characteristics of pull-down devices for 3-micron single metal arrays over temperature. The two sets of curves shown correspond to the maximum and minimum values of the equivalent impedance of the saturated transistors, covering the entire spectrum of allowable process parameter deviations.

Figure 4.6. Gate Array Pull-Up Characteristics

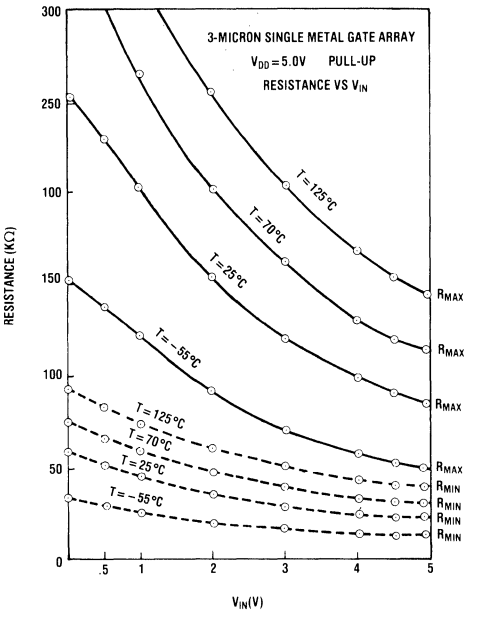
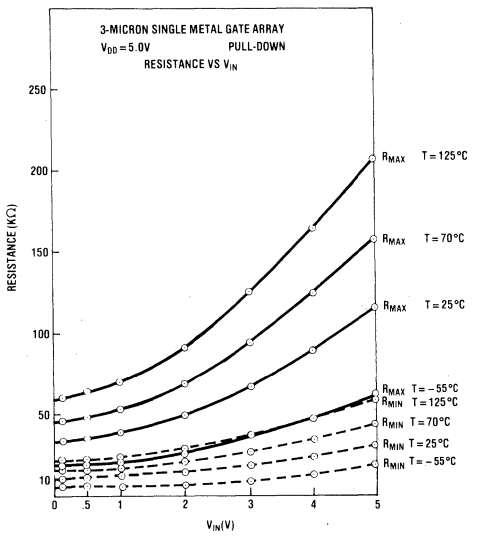


Figure 4.7. Gate Array Pull-Down Characteristics



4.5 Output Drivers

The basic CMOS output driver is, from the structural point of view, no different from the inverter discussed in the logic design section. However, in order to provide enough driving capability to interface with bipolar families, the "push-pull" devices used to build the output drivers are several times bigger than the internal transistors.

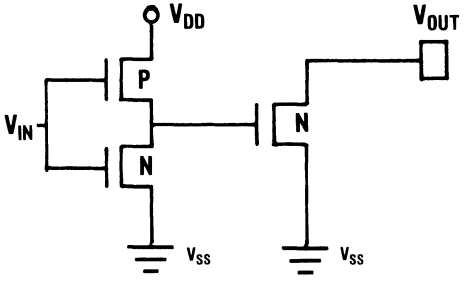
In most cases, the functional macros for semicustom output buffers already include pre-drivers used to scale down the load on internal gates, and the overall function ends up being non-inverting.

Variations of the basic type include:

- Open-Drain Drivers
- Tri-State Drivers

The open-drain output buffer consists of a single N-channel transistor whose drain terminal, as its name indicates, is left floating while the source is connected to V_{SS}.

Figure 4.8. Open Drain Output Buffer



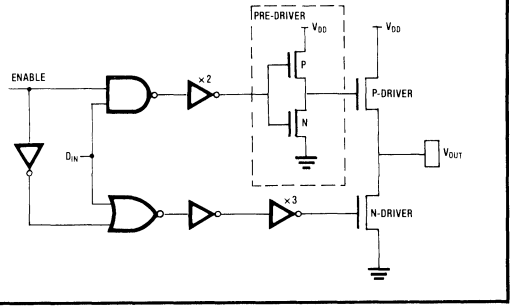
Open-drain and emitter-follower drivers are widely used in asynchronous structures, where a common use for these buffers is the construction of wired-or logic.

A tri-state buffer is constructed from the basic inverting driver by incorporating additional circuitry that allows turning off the pull-up and pull-down transistors, simultaneously, thus leaving the output node floating. Three-state drivers are typically used when several circuits access a common signal line synchronously, for example, a memory data bus.
The D.C. characteristics of semicustom drivers are specified in the corresponding data sheets, and to a first-order approximation the drive capability of a given transistor is a function of its size, input level, and drain to source voltage. Normally, the input levels are either V_{DD} or V_{SS} since leakage currents are to small to cause a significant voltage drop across the internal devices. Thus, the output drive becomes a function of geometries and output levels only.

Since usually the device sizes for pull-up and pull-down drivers are different, their driving capabilities are also different and need to be considered separately. In any case, for a fixed device driven by internal logic, the sinking or sourcing currents depend on the output voltage level.

Figures 4.9 and 4.10 illustrate the characteristics of the pull-up and pull-down drivers used in the 3-micron family of gate arrays. The curves shown take into consideration worst case process parameters, and the devices are assumed to be operated at 4.5 volts.

Figure 4.9. CMOS Tri-State Output Buffer



Although output drivers can be paralleled to increase sinking or sourcing currents, as these currents are increased, the voltage drop across the power rails can become significant, particularly in gate arrays where there are certain constraints imposed on the width of the power buses, and additional power pins might be required in order to preserve the noise margin of the device.

Important consideration must also be given to the maximum current density through the power supply lines. In this respect, the thickness of the metal line in semicustom devices is fixed, and the allowable current density for any given line is one milliampere per micron of width. Violation of this basic rule can lead to reliability hazards, caused by aluminum electromigration.

Figure 4.10. 3-Micron Arrays Current Sinking Characteristics

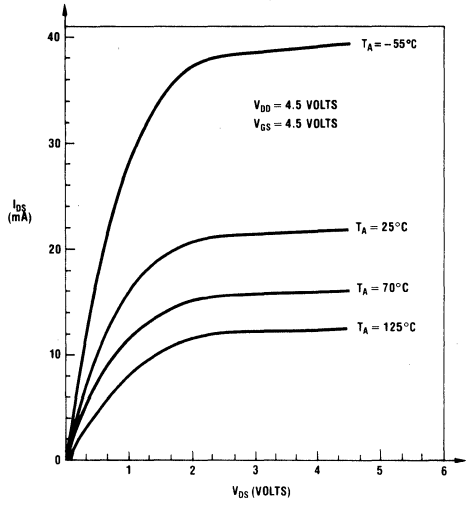
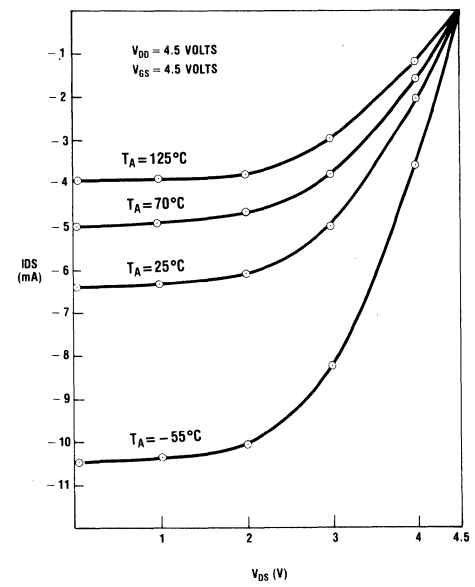


Figure 4.11. 3-Micron Arrays Current Sourcing Characteristics



4.6 Switching Current

In describing a basic CMOS inverter, it was noted that when the output node changes states a current spike is generated. The duration of this current pulse is a function of the device geometries and the capacitive load for a fixed power supply.

Semicustom devices are quite often used in bus oriented logic structures, where the total capacitive load associated with an output driver can sometimes exceed 200 picofarads. Since the transistors used to interface with external components have relatively large geometries, the current spikes generated by the output drivers are typically in the order of 20 to 40 milliamperes.

If several outputs with high capacitive load are switched simultaneously, the RMS value of the A.C. current can be large enough to cause significant voltage drops along the power supply lines, and in some cases it might exceed the recommended current density in the aluminum. In any case, when a situation like this is encountered, the internal logic should be isolated from these A.C. currents by providing a different pair of power supply pins than the one used to operate the output drivers.

Furthermore, to avoid reliability problems in some applications, the drivers themselves might require several V_{DD} and V_{SS} pins depending on the number of outputs switching at once and the associated node capacitance.

Figures 4.12 and 4.13 illustrate the duration of the current spikes on the 3-micron single metal gate array drivers as a function of the capacitive load.

4.7 Power Dissipation

a) Leakage Currents
b) Transient Currents
c) A.C. Currents

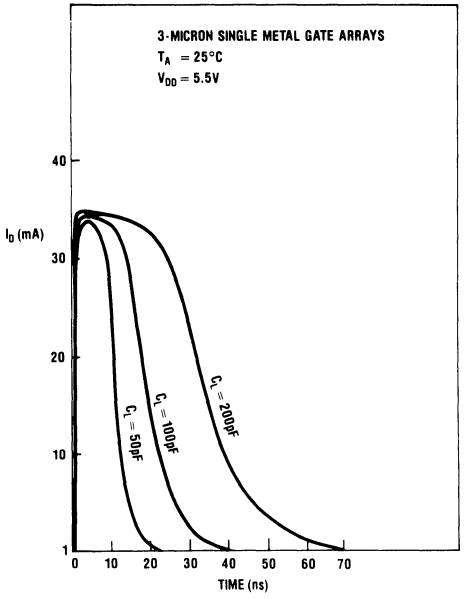
The first component is the quiescent power dissipation, which in CMOS devices is typically in the order of a few microwatts.

Transient currents are those associated with input switching transitions, where the pull-up and pull-down transistors are both on simultaneously for a short period of time, depending on device geometries as well as on frequency and rise and fall times of the input signal, and can be approximated by the following expression:

$$P(V_{IN}) = \frac{(V_{DD} - 2V_T) \times I_{PEAK} (T_{RISE} + T_{FALL} \times F)}{2}$$

where:

Figure 4.12. N-Driver Current Pulse vs. Output Capacitance



V_{DD} = Operating Supply Voltage
V_T = Transistor Threshold Voltage
I_{PEAK} = Maximum Non-Capacitive Transient Current
F = Frequency of the Input Signal

Typically, if the fan-out rules given in Section 3 are followed, the power dissipation due to transient spikes can in most cases, be neglected.

The major contribution to power consumption in a CMOS circuit is, however, the transfer of energy stored at the output node capacitance. This energy is 1/2 C V, but since the capacitor is both charged and discharged every cycle, the amount of energy provided by the CMOS device per unit time is:

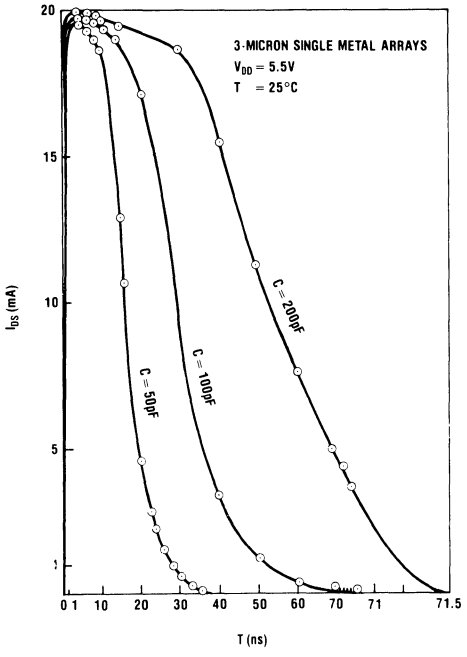
$$Pd = C \times V^2 \times F$$

where C is the capacitive load, V the supply voltage, and F the frequency.

To estimate the total power dissipation in a semi-custom device is definitely not a trivial effort, since all gates are not operating at the same frequency, and an individual calculation needs to be made for every single gate in the circuit. When dealing with several thousand gates, this task can only be handled by a computer.

In many cases, however, an approximate figure for the power consumption is good enough, in which case the circuit can be broken down into different sections where the gates operate more or less at the same frequency. The total power can then be calculated based on the percentage consumed in the individual sections.

Figure 4.13. Current Pulse Duration for P-Channel Driver



5. Testing

5.1 Gould AMI Testing Procedures

The generation of a test program which will guarantee that a customer receives quality parts once his production begins actually starts in the initial stages of spec negotiation. It is important, at this point, for test engineering to get involved to insure that specifications which can be designed can also be tested. The cognizant test engineer at Gould AMI will review each specification individually to ascertain whether or not the available test systems have the capability to fully

test the part to spec. Once he has an approved, mutally agreed apon set of test parameters, the pin assignments are made to the tester channels and a performance board is designed which will interface the device to the tester.

There are basically two types of tests which must be performed on each device — DC parametric tests and an AC functional test. The DC section of the test program ordinarily contains the following tests:

1. Continuity/Shorts — This test insures that all device pins have been correctly bonded and no short circuits exist.

2. Input Leakage — Insures that no inputs have a leakage current greater than the specified value (usually 1μA).

3. Tri-State Leakage — For those pins which have bus sharing or act as both input and output pins (I/Os), a test is performed with both the p and n output transistors off to guarantee that the leakage is less than 10μA.

4. Power Test — A static test is performed with the chip powered up and the inputs held high, low or floating, depending upon the specified conditions and the current flow measured.

5. Output Level Tests — Tests performed on all output pins to insure that all output drivers are capable of sinking or sourcing the required amounts of current at the specified voltage levels.

The AC functional tests are performed to guarantee that the logic which is implemented on the chip performs as it is supposed to, and will operate at the necessary speed. The quality of this check depends heavily on the quality of the test inputs received from the customer at the outset of the program. The customer supplied test inputs (vectors) are called a functional test pattern. This test pattern must be capable of detecting a high percentage of the possible logic faults to guarantee high quality functional testing.

Once the performance board is built, the parametric tests written, and the timing values programmed, the functional pattern, which is generated from the logic simulation results, is inserted into the test program. The Gould AMI logic simulator (SIMAD) is run with the BOLT netlist and the input stimuli (vectors) generated by the person who knows the chip best — the logic designer. The input vectors are applied to the network simulation model and output states generated. From this point a formatting and compression program called TESTFORM is run to produce a Sentry compatible test pattern which is output on a magnetic tape and given to the test engineer. The engineer then incorporates this pattern into his "shell" test program and begins to debug the result. Part of his responsibility is to insure that the program meets the published guidelines of the Gould AMI manufacturing organization. One such guideline is that the program has 3 different "switch" options, each representing a test performed at a different point in the production cycle. These are summarized below:

Switch 1 (WAFER SORT) — This is the option selected for wafer level ("SORT") testing. The parameter value limits used in the wafer sort test may or may not equal the specification depending upon the speed and marginality of the part. The distance between the bonding pads on the die and the tester channel increases at wafer sort due to the use of long interface cables. The extra capacitance and noise introduced by the long cables can degrade the performance enough to cause a good part to fail. For this reason, a careful correlation study is done to determine the best parameter limits for testing. Wafer sort testing is the most economical way to catch bad die, so the costs of assembly and final testing are limited to good die.

Switch 2 (FINAL TEST) — Once the tested wafers have been diced and assembled into individual packages, a "final test" must be performed. This is the last step before Quality Assurance checks the product; thus it must be a complete test which totally checks all parameters included in the spec. Actually, the final test is more stringent that the specification because of "guardbanding". Guardbanding is a procedure by which certain parametric and timing values are tightened to compensate for the possibility of marginal parts passing at final test and then failing the QA test (Switch 3) because of differences which may exist between test systems. The Gould AMI sample plan for Quality Assurance requires that there be 0 failures at the QA checkpoint, which explains the necessity for guardbanding.

Switch 3 (QA TEST) — This switch option is normally the only option which tests the part exactly to the customer specification. Customers can rely on Gould AMI to normally test 100% of production parts at limits more stringent that the customer spec.

5.2 Test Capabilities

Gould AMI performs all of their Semicustom testing on the Fairchild Sentry line of testers. Systems at the Gould AMI Santa Clara facility include 5 Sentry VIIs and 3 Series 21s. All systems can test up to 60 pin devices, except one Series 21 which has 120 pin capability. A table summarizing the capabilities of the test system is shown below. Pin counts in excess of 120 pins are accomodated by multiplexing channels on the performance board.

Feature	Sentry VII	Series 21
Maximum Test Rate	10MHz	20MHz
Max Test Rate (Multiplexed)	20MHz	40MHz
Test Rate Resolution	10ns	5ns
I/O Switching Specs	±10ns	±3ns
Timing Sets	1	16
I/O Registers (DA/DB)	2	16
Masking Registers	2	16
Maximum Clock Rate	30MHz	60MHz
D.C. Measurement Ranges	4	6
Maximum Pin Count	60	120
Max Pin Count (Multiplexed)	−84	−156

Also available for device testing requiring higher speeds is the Genrad GR-16 tester at the Gould AMI wafer fabrication plant in Pocatello, Idaho. This tester can provide test rates of 30MHz and presently has 96 pin capability with expansion to 144 pins available.

5.2.1 Test Limitations

The limitations of today's VLSI test systems are seldom reached. Rather, the limiting factor in testing is the development time required to write and debug the test as well as the test time required to execute the test. Apart from the "Design for Testability" techniques, which facilitate efficient testing (discussed in the next section), several recommendations for defining test conditions to minimize testing problems are summarized below:

1. V_{OL} and V_{OH} (Output CMOS high and low levels) — Conventional specifications call for both of these to be guaranteed to within .05 volts from the respective voltage rail. While in reality this is not a problem for unloaded outputs, it can cause problems in a test environment because of test system resolution. The Sentry has voltage supply resolution in the range of 40mV. So the supply voltage can range from 4.96 to 5.04 volts, if programmed at 5V. In addition, the PMU (Precision Measurement Unit) on the Sentry which measures voltage also has a measurement tolerance. Adding to these tolerances, the effects of noise can result in a test which will fail parts that have in-spec V_{OL} and V_{OH} levels. It is best for testing purposes to put at least 100mV between the supply value and the expected output level. Gould AMI will usually perform a functional test with the device unloaded and then verify sink and source current capability by using the test system to force a current into or out of the outputs, thus simulating the static loaded conditions. However, any dynamic circuitry must still have loads on the performance board.

2. Load Specifications — The Sentry has an inherent 50pF capacitive load built into the test head. Many products, however, require speed paths to be checked with load capacitances as low as 5pF. This presents a testing problem because speed goes down as capacitive loading goes up; therefore, parts which actually meet the speed requirements can fail. For this reason, all test conditions related to output pin speeds should be derated to 50pF for test purposes.

3. Avoid specifying a requirement for measurement of output pulse widths. While this test can be done, it requires a very time-consuming binary search routine on the Sentry to find the rising and falling edges of a pulse.

4. Input frequencies must be integer multiples of each other to be incorporated into a functional pattern. It is impossible to have a 10MHz clock running at the same time a 3MHz clock is required.

The above recommendations cover the most frequently encountered types of test problems.

5.3 Designing For Testability

Design for Testability involves three main concepts:

Initialization — The ability to set the state of the device under test (DUT) at the beginning of the test cycle.

Controllability — The ability to set internal nodes of the DUT in a given state by external stimulus.

Observability — The ability to observe at a DUT output, the state of an internal node.

Here are some suggestions/solutions to overcome the implementation problem for each testability concept.

1. Initialization — It is essential to set the state of the DUT at the beginning of a test cycle. This reduces both testing time and the risk of invalid failures of good devices. If the DUT cannot be initialized, then a routine known as "match mode" must be used on the Sentry to apply a pattern to the DUT until it "matches" a pattern supplied by the test engineer. When a match occurs, the DUT is in a known state. There are two types of resets used in the implementation of Semicustom products. These are the reset pin and a reset by a combination of stimuli on one or several other pins.

a. Reset pin — Designing a reset pin into the circuitry is the recommended way to guarantee initialization. This pin is connected internally to all of the storage elements and provides an immediate initialization of the DUT. The reset signal is sent by the test system to initialize the DUT and start the test sequence. A disadvantage of the use of a reset pin is that it requires an additional pin and reset; it adds a substantial amount of circuitry to the device. The reset pin becomes especially costly when the designer has to go into the next larger pin count package to provide the reset pin. However, these disadvantages are often outweighed by the advantages of the fastest possible reset sequence and the easiest initialization method. The tester only needs to send one pulse to the DUT rather than a whole sequence of reset commands.

b. Reset by a Combination (Sequential reset) — The variety of combinational reset techniques is limited only by the imagination and creativity of the designer. Two widely used techniques are discussed here. The first uses a reset pin, but in order to save some internal circuitry, the internal reset pin goes only to a limited number of devices. A complete reset of the DUT requires a certain number of clock cycles during which known signals are propagated through the entire circuit. The implementation of this technique starts by the identification of serial synchronous delay lines and the study of the signals required to initialize them in the chosen state. The length of the reset sequence is the length of the longest such line. The second example avoids using an additional reset pin, generally for package considerations. Here the reset sequence must be initialized by a combination of the input signals that cannot occur during the normal operation of the circuit. The advantages of the above techniques are that they:

a) use standard circuitry
b) allow the designer the flexibility of deciding how to implement the reset function
c) allow the test engineer to precondition the DUT into a known state at a known time

2. Controllability — The first element of controllability is the ability to unconditionally reset the DUT. Another important controllability technique is the ability to externally place the DUT in any state required to simplify testing. Several approaches can be used. One of the most popular methods of increasing controllability is the implementation of a "test mode". This can be achieved externally and requires a number of exclusive combinations of the inputs at least equal to the number of states in the test mode. This can also be achieved by internally storing the test mode sequence of events and starting it by the reset pin.

3. Observability — Observability of the outputs defines how easily the internal behavior of the device can be observed on the external pins. Numerous techniques exist that improve the observability of a given circuit, and almost all of them are based on the transferring of the internal states to an external pin. The main limitation is the pin count or the extra circuitry required. However, the access to normally inaccessible internal nodes can greatly increase the test coverage while at the same time, reduce the overall test time.

5.4 Test Pattern Formatting

Once logic simulation has been completed, the designer must devise a set of input stimuli (test pattern) which will test enough of the internal nodes to insure that a part which passes the test pattern will work in the system. Once this test pattern has been written, it is submitted to Gould AMI for use by the test engineering department in writing the test program. To get the test program debugged as quickly as possible, the test pattern must be properly formatted. Patterns which were not produced with Gould AMI's logic simulator (SIMAD), thus allowing the use of Gould AMI's test formatting program (TESTFORM), must be supplied to Gould AMI in a Sentry compatible format on a magnetic tape. Complete instructions for the formatting to be used and the acceptable tape formats can be found by referencing Gould AMI document number 4150073 entitled "Generation of Sentry/Sentinel Functional

Test Patterns". This document is available from any salesman or Semicustom marketing engineer.

If the circuit has been described in BOLT format and can therefore be run on SIMAD, the process is simpler. The input stimuli are coded into Gen-blocks, which are strings of binary data for each input. The format for a pin might read 40-0, 6-1, 2-0, which would mean that that input pin should receive 40 low pulses followed by 6 high pulses and then 2 low pulses. Given this input stimuli, the SIMAD program will generate output states based on the logic description. In order to insure that the logic simulation results are correct, it is best to supply the expected output so a comparison can be made. If Gould AMI performs the logic simulation, then the test pattern inputs can be submitted in one of three ways:

1. Timing Diagrams — Diagrams showing all input pins referenced to some test "period".

2. Truth Table — Patterns of "1's" and "0's" which reflect the operation of the chip. Normally, the highest frequency DUT input signal determines the test period. Each line of the truth table must specify one DUT clock pulse, along with other input data, and SIMAD will provide the expected outputs. If the propagation delay of any output is longer than the basic test period, the expected output state will be pushed into the next test cycle.

3. Gen-blocks — This is the input format for SIMAD. Information on this type of formatting can be obtained by consulting the Gould AMI SIMAD User's Manual.

6. Packaging

Gould AMI offers a broad range of standard and non-standard packages for semicustom devices. Table 6.1 shows the various types of standard packages with their respective lead count. This table also illustrates the smallest package that can be used with a particular gate array.

Dual-in-line packages are available in plastic, cerdip and ceramic, ranging in lead count from 8 to 64 for plastic, 14 to 40 for cerdip and 14 to 64 for ceramic DIP. Mini flat packs are Gould AMI's proprietary post molded, surface mounted packages and are available in plastic with 40 mil centers and lead counts ranging from 18 to 68 pins. Ceramic leadless chip carriers, pre- and post-molded, will be available in 68 and 84 leads in the near future. Leaded ceramic chip carriers are also available upon customer request. Ceramic pin grid array packages are offered starting at 68 pins and going up to 256 pins. Plastic pin grid array packages are expected to be in production by Q1 '86. Cavity down pin grid array options are also available at Gould AMI.

To determine if a particular gate array can fit in a certain package, all one needs to know is the die size of the gate array and the cavity size of the package. However, the maximum cavity size varies depending on whether or not the down bonding option (see Section 6.2) is required.

In standard circuits, the die size for every design has to be calculated and is based on the number of gates, number of pads, level of interconnect and process technology. The calculated die size of the standard cell circuit is then compared with the cavity size of the desired package type.

Semicustom products can also be ordered in wafer or die form if required. Gould AMI also develops non-standard package options for customers with very high volume requirements.

Gate arrays operate over a broad range of voltages and temperatures. Supply voltages specified for the GA Series range from 2.5 to 5 V (± 10%). Temperatures can meet standard commercial requirements (0°C to 70°C), industrial environmental needs (−40°C to 85°C), or full military specifications (−55°C to 125°C).

Burn-in, high reliablity screening, and full MIL-STD-883 Class B Military screening are also offered.

6.1 Package Families

PLASTIC PACKAGE:

Gould AMI's custom and standard MOS/VLSI products are available in economical, reliable silicon epoxy transfer-molded packages. Consistent with Gould AMI's policy of improving quality and reliability while staying on the historic semiconductor learning curve, Gould AMI now provides spot silver leadframes, conductive adhesive die attach, automated die attach and automatic wire bonding. In developing these capabilities, exhaustive evaluations have been made of numerous materials, processing technologies and device performance after encapsulation. In addition, equally extensive production and reliability tests have been conducted, which include life and environmental tests in accordance with MIL-STD-883B to insure package integrity.

Table 6.1. Gate Array Package Options

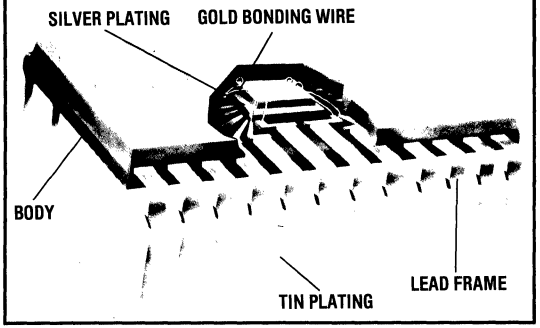
Package Type	Lead Count	Spacing (mils)	Gate Array Matrix									Maximum Chip Without Down Bond (MILS × MILS)	Thermal Characteristics	
			3μ Single Metal					3μ Double Metal						
			GA-500	GA-1000	GA-1500	GA-2000	GA-2500	GA-1000D	GA-2000D	GA-3000D	GA-4000D		Θ_{JA} (°C/W)	Θ_{JC} (°C/W)
Plastic	14	100	•									140×170	121.8	47.0
	16	100	•									140×210	114.8	39.5
	18	100	•									140×210	125.1	57.5
	22	100	0	0	•			•				220×240	83.0	36.7
	24	100	0	0	0	0	•	0	0			290×280	102.1	42.5
	28	100	0	0	0	0	•	0	0			250×240	82.1	31.2
	40	100	0	0	0	0	0	0	0	0		340×330	79.9	31.9
	48	100	X	0	0	•		0				250×260	•	•
	64	100	X	X	0	0	0	0	0	•		315×305	64.1	39.5
Cerdip	22	100	•	•	•							200×280	65.0	18.6
	24	100	0	0	0	0	•	•	•			250×390	51.6	15.8
	28	100	0	0	0	0	•	•	•			250×390	50.0	15.8
	40	100	0	0	0	0	•	•	•			260×345	38.3	10.1
Ceramic Side-Brazed	22	100	0	•	•	•						220×260	56.5	11.1
	24	100	0	0	0	0	•	•	•			270×280	42.5	9.0
	28	100	0	0	0	0	•	•	•			280×290	40.9	6.9
	40	100	0	0	0	0	•	•	•			320×360	37.1	8.2
	48	100	X	0	0	0	0	0	0	•		310×320	37.8	8.6
	64	100	X	X	0	0	0	0	0			295×305	37.7	5.7
Mini Flatpack	18	40	0									200×190	96.2	37.1
	22	40	0									200×190	96.2	37.1
	24	40	0									200×190	96.2	37.1
	28	40	0									200×190	96.2	37.1
	40	40	0	0	0	0	0	0	0	0	•	240×230	116.9	35.3
	44	40	X	0	0	0	0	0	0	0	0	240×230	116.9	35.3
	68	40	X	X	X	0	0	X	0	0	•	240×230	92.1	36.8
Leadless Chip Carrier	24	50	0	•				•				205×215	75.3	38.4
	28	50	0	0	0	•	•	0	•			220×230	•	•
	40	40	0	0	0	•	•	0	•			270×280	40.5	•
	44	50	X	0	0	•	•	0	•			270×280	•	•
	48	40	X	0	0	0	0	0	0	•		320×330	•	•
	68	50	X	X	X	0	0	X	0	0	0	370×380	25.4	•
	84	50	X	X	X	X	0	X	0	0	0	360×370	•	•
Pin Grid Array	68	100	X	X	X	0	0	X	0	0	•	271×261	24	•
	84	100	X	X	X	X	0	X	0	0	0	380×370	21	•
	100	100	X	X	X	X	X	X	X	•	•	330×320	•	•
	120	100	X	X	X	X	X	X	X	X	0	413×403	•	•
	144	100	X	X	X	X	X	X	X	X	X	442×452	•	•
Ceramic Flatpack	42	50	X	•								196×206	53.9	14.7
Plastic Molded Leaded Chip-Carriers	44	50	X									•	•	•
	68	50	X	X	X	0	0	X	0			•	•	•
	84	50	X	X	X	X	0	X	0			•	•	•

Legend: 0 = No Restrictions X = Less Pads than Pins • = Consult Gould AMI

PLASTIC FEATURES:

- Materials
  Epoxy compound
  — High temperature stability, low in ionics
  Gold Wire
  — 1.3 mil
  Kovar or alloy 42 leadframes (copper leadframe)
  — 150 microinches min. spot silver on die attach pad and bonding fingers
  — 200 microinches min. semi-matte tin plate on external package leads

Figure 6.1. Plastic Package



CERAMIC (LAMINATED) PACKAGE:

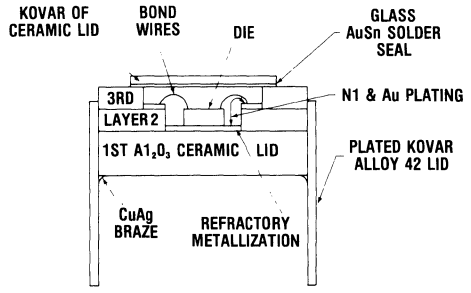
- Sidebrazed — multilayer package

The ceramic layers are punched in the green (unfired) state from a long ribbon or "tape". This tape is formed from a paste of approximately 90% alumina Al_2O_3. Conductor metallization to provide electrical connections between the lead tips at the cavity and the package exterior is then screened onto the appropriate green ceramic layer in a defined pattern. The layers are then stacked or laminated. The refractory metal brazing contracts are applied, and then the laminate is co-fired at approximately 1500°C. The leads are attached by brazing in high temperature ovens. Gold is spot plated on the die cavity and bonding fingers.

LAMINATED CERAMIC FEATURES:

- Laminated ceramic packages are generally used for high reliability functions and for prototype assemblies. They are relatively easy to obtain and assemble.
- Chip carriers were developed as a space saving package alternative. SLAMS are a less expensive socketable type of chip carrier. Additionally, pin grid arrays are beginning to see wider use, especially for VLSIC, VHSIC and ULST applications which require high lead counts.
- Additional features of these packages are hermetic seal with metal or ceramic lid and aluminum ultrasonic bonding.

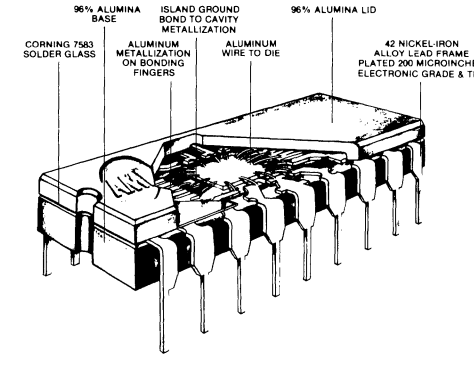
Figure 6.2. Ceramic Package



CERDIP (PRESSED CERAMIC) PACKAGE:

The two ceramic components of the cerdip package, the cap and base, are pressed from 90-94% pure Al_2O_3 powder and fired. Whereas the laminated package has the gold plated on, the cerdip has a gold paste fired to the die attach cavity. Glass is then glazed onto the land areas of the cerdip package, i.e., the top surface of the base and the bottom surface of the cap. This glass is the package sealant.

Figure 6.3. Cerdip Package



The combined cerdip base and lead frame serve the same purpose as the laminated ceramic package.

The cerdip lead frame is first embedded in the glass on the cerdip base by heating in a furnace. This assembly is then die attached and lead bonded. The cap is then attached by heating in a furnace again. In each heat treatment, the glass on the ceramic parts softens and flows, creating a hermetic seal. Sealing temperatures are generally higher for cerdip packages than for laminated packages.

CERDIP FEATURES:

Cerdip packages, in general, are the least expensive hermetic package, and are especially cost efficient in high volumes. Cerdip packages at Gould AMI utilize the latest glass and moisture control technology, and can be used where requirements include high reliability, low moisture, and improved thermal dissipation.

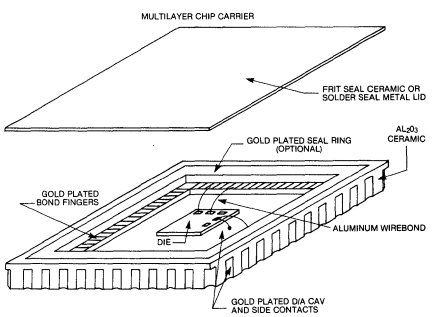
CHIP CARRIER PACAKAGE:

Chip carriers are the new industry standard in reducing package size. Built on the same concept as the highly reliable sidebraze ceramic package, the chip carrier is made of three layers of Al_2O_3 ceramic, refractory metallization and gold plating. The chip carrier also offers contact pads equally spaced on all four sides of the carrier resulting in increased package density, better electrical characteristics, and a more cost effective way of packaging IC devices.

The package comes with a gold tin eutectic sealed metal lid or the low cost glass sealed ceramic lid creating a standard hermetic cavity.

It is available in 20, 24, 28, 40, 44, 68 and 84 lead standard 3-layer versions, and 24, 28, 44 lead slam style on 50 mil center lines to the JEDEC standards.

Figure 6.4. Chip Carrier



6.2 Assembly Considerations

A. DOWN BONDING:

Down bonding is required in cases where the chip substrate is not connnected to V_{DD} through diffusion "plugs" properly distributed across the entire die. A floating substrate could lead to potential latch-up due to the parasitic SCRs inherent in CMOS devices. To prevent this condition, down bonding is provided by means of connecting the substrate of the die to the V_{DD} pin on the package. Depending on the package type, down bonding requires 20 to 60 mils of the cavity space, thus reducing the usable cavity area for die attach, accordingly. State-of-the-art gate arrays and standard cells provide adequate substrate contacts through diffusion "plugs" and do not require down bonding. Table 6.1 shows the maximum cavity size without down bond. If, however, down bonding is required on a die, consult the factory to determine the maximum usable cavity area.

B. THERMAL RESISTANCE:

Thermal resistance data for Θ_{JA} and Θ_{JC} (resistance from junction to ambient and from junction to case respectively) is given in degrees centigrade per watt. Data is obtained in the following manner:

Blocks of dice containing simple transistors are sliced out of wafers to cover an appropriate portion of the die attach area for each package type tested. A few of the transistors are bonded up and package assembly completed. One transistor, located near the center of the die attach area, is selected as sensor. It is biased as a diode with constant current. With the package placed in a controlled and monitored temperature environment, a calibration curve of diode voltage versus temperature is obtained. When this stage of calibration is completed, the package is then placed in a stabilized, monitored, still air environment. Remaining transistors, connected in parallel as diodes, are then powered up in incremental steps of power. As power is increased, the temperature of the package interior rises above the external ambient temperature and is monitored by means of the previously calibrated diode. This differential temperature between package interior and external ambient divided by the power applied is the definition of thermal resistance Θ_{JA} (resistance from junction to ambient) expressed in degrees centigrade per watt of power dissipated internally. Θ_{JC} (resistance from junction to case) is measured in a similar manner. In this case, however, the package is physically connected to a heat sink which is large enough to be considered infinite in size. In reality,

when the heat sink surface is sufficiently large, the thermal resistance between it and the surrounding air is insignificantly small compared to the device connected to it.

An example for utilizing Θ_{JA} follows:

$$\Theta_{JA} = 40°C/watt$$

Maximum power expected to be dissipated = 1 watt
Die temperature rise above external ambient =

$$\frac{40°C}{watt} \times 1 \text{ watt} = 40°C$$

If the ambient temperature is not expected to be greater than 70°C, an often assumed commercial temperature, then the internal die will rise to a maximum of 40 + 70 or 110 degrees centigrade.

C. POWER DISSIPATION

The maximum power dissipation of a circuit is limited by the thermal resistance of the package in which it is used, and the maximum allowable junction temperature:

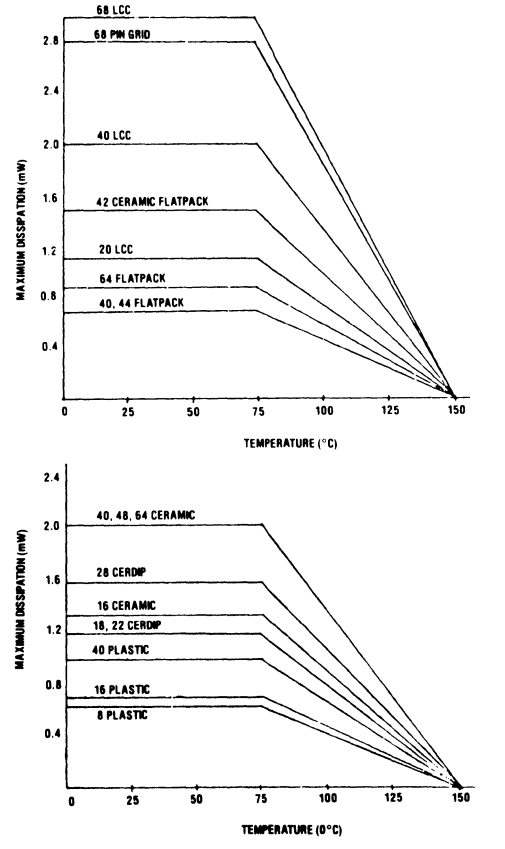
$$P_{MAX} = \frac{T_{JMAX} - T_A}{\Theta_{JA}}$$

Where P_{MAX} = maximum power dissipation (watts)
T_{JMAX} = maximum allowable junction temperature (°C)
T_A = ambient temperature (°C)
Θ_{JA} = thermal resistance of the chip (°C/W)

Under normal conditions, junction temperatures of up to 150°C do not affect the reliability of the circuits. However, a lower limit may be specified for various reasons.

Power derating curves for different package types are shown in Figure 6.5

Figure 6.5. Power Derating Curves



6.3 Package Reliability

A. QUALITY ASSURANCE/RELIABILITY

Gould AMI's Product Assurance Program is based on MIL-STD-883B, MIL-M-38510, and MIL-Q-9858A methods. Under this program, Gould AMI manufactures the highest quality MOS devices for all segments of the commercial and industrial market. Under special adaptations of the basic program, Gould AMI also manufactures high reliability devices to full military specifications, if requested.

This program has a twofold purpose: to assure a consistently high quality, reliable product; and to assure that the product can be manufactured at a later date with the same degree of reliability. To effectively achieve these objectives, Gould AMI has developed a product assurance program consisting of three major functions:

- Quality Control establishes that every method meets, or fails to meet, processing or production standards; **Quality Control checks methods.**
- Quality Assurance establishes that every product meets, or fails to meet, product parameters; **Quality Assurance checks results.**

- Reliability establishes that Quality Control and Quality Assurance are effective; **Reliability checks device performance.**

Each function has a different area of concern, but all share the responsibility for a reliable product. Constant monitoring of all phases of production, with information feedback at all levels, allows fast and efficient detection of problems, evaluation and analysis, correction, and verification of the corrections. The overall result is a line of products which is highly repeatable and reliable, with a very low reject level.

To insure that this high level of reliability is maintained, Gould AMI has an on-going program of monitors that evaluates device performance through stress testing.

B. A SPECTRUM OF TEST METHODS:

Operating Life Test:

In order to predict the expected life of a device at a nominal stress, it is necessary to perform an operating life test. Time dependent random failure mechanisms are accelerated through the application of higher than normal temperatures while devices are under power. Because failures of semiconductors occur as a result of some chemical or physical reaction, we can describe the temperature dependence of these mechanisms by applying the Arrhenius reaction rate equation. Using the thermal activation energy for a failure mechanism, we can determine the acceleration factor of the operating life test with the following equation:

Equation:

$$F = \exp \frac{E}{K} \left(\frac{1}{T_1} - \frac{1}{T_2} \right)$$

F = Acceleration Factor
E = Activation Energy in eV
K = Boltzmans constant: 8.63×10^{-5} eV/°K
T_1 = Higher test temperature in °K
T_2 = Lower nominal temperature in °K

Thus with the Arrhenius model we can predict the reliability of a device in terms of a failure rate expressed in percent per 1000 hours (typically with 60% confidence level).

Furthermore, the on-going identification of prevalent failure modes allows the Reliability Department to make recommendations for improving the intrinsic reliability of circuit designs, layout and processes used to manufacture devices. This allows Gould AMI to further improve reliability through design in all its products.

Temperature and Humidity (85°C/85% RH) Test:

The considerable cost savings achieved by encapsulating an integrated circuit in molded plastic instead of a hermetically sealed package brings with it a trade-off of exposure of the passivated die surface to water vapor or other contaminates.

Thus, temperature and humidity stressing under bias is used to evaluate design factors such as plastic molding compounds, integrity of the passivation layers, and the interface between plastic and the lead frame.

Major moisture related failure mechanisms include:

- Corrosion of metallization. When ionic species, moisture and bias are present, eletrochemical cells can be established which cause corrosion of metallization. Corrosion rates can be accelerated by increases in temperature and moisture.
- Charge separation on the surface of MOS structures can cause leakage from parasitic devices.

Temperature Cycle Test:

This test repeatedly exposes devices to large variations in temperature during a specified period of time. Due to differences in thermal expansion coefficents between lead frames, silicon chip, molding compounds, die attach material, and bonding wires, the repeated thermal stresses may eventually lead to fatigue cracking in any of the above components. Therefore, this test evaluates thermal compatibility of materials throughout the life of the circuit. The test is also used to detect package defects as well as micro-cracks in metal deposition.

Thermal Shock Test:

The Thermal Shock test is similar to temperature cycling except that liquid media are employed resulting in a rapid heat transfer, shorter cycle time and greater thermal gradient. This test is used primarily to determine the compatibility of materials. Problems in workmanship at assembly steps such as die attach and wire bonding are also identified by this test.

Autoclave Test:

Autoclave is an unbiased accelerated moisture resistance test performed in an environment of saturated steam under about 15psi. It provides rapid saturation of the plastic by moisture. If there are reactants available, the device metal may corrode or mobile ionic contamination may cause malfunction in devices inadequately passivated.

Gate Array Datasheets

3μ Single-Metal HCMOS Gate Array

Selection Guide

3μ Single-Metal HCMOS Gate Array

Cell	Description
AA02	Pre-Routed Two Input AND Gate
AA03	Pre-Routed Three Input AND Gate
AA04	Pre-Routed Four Input AND Gate
AN01	Pre-Routed AND-NOR Gate
AN02	Pre-Routed AND-NOR Gate
DF01	Pre-Routed D Flip-Flop
DF02	Pre-Routed D Flip-Flop With Asynchronous Active Low Set
DF03	Pre-Routed D Flip-Flop With Asynchronous Active Low Reset
DF04	Pre-Routed D Flip-Flop With Asynchronous Active Low Set And Active Low Reset
DL01	Pre-Routed Latch With Q And QN
DL18	Pre-Routed Latch With Set And Reset
DL19	Pre-Routed Latch With Set
DL1A	Pre-Routed Latch With Reset
DL1B	Pre-Routed Latch With Active Low Set
DL1C	Pre-Routed Latch With Active Low Reset
DL1D	Pre-Routed Latch With Active Low Set and Reset
EN01	Pre-Routed Exclusive NOR Gate
EO01	Pre-Routed Exclusive OR Gate
IB13	Input Pad With Protection Diode
IB14	Input Pad With Protection Diode With P-Channel
IB15	Input Pad With Protection Diode With N-Channel
IIF0	Pre-Routed Inverting Schmitt Trigger
IIF3	Pre-Routed TTL Lever Translator
IN01	Single Pre-Routed Inverter
IN02	Two Pre-Routed Inverters in Parallel
IN03	Three Pre-Routed Inverters in Parallel
IN04	Four Pre-Routed Inverters in Parallel
IN05	Five Pre-Routed Inverters in Parallel
IO05	Tri-State Input-Output Buffer
IT02	Pre-Routed Inverter Driving A Transmission Gate
MU20	Pre-Routed Two To One Multiplexer

Cell	Description
NA02	Pre-Routed Two Input NAND Gate
NA03	Pre-Routed Three Input NAND Gate
NA04	Pre-Routed Four Input NAND Gate
NA05	Pre-Routed Five Input NAND Gate
NO02	Pre-Routed Two Input NOR Gate
NO03	Pre-Routed Three Input NOR Gate
NO04	Pre-Routed Four Input NOR Gate
NO05	Pre-Routed Five Input NOR Gate
OB03	CMOS Output Buffer
OB07	Open Drain Output Buffer
OB0D	Tri-State Output Buffer
ON01	Pre-Routed OR-NAND Gate
ON02	Pre-Routed OR-NAND Gate
OR02	Pre-Routed Two Input OR Gate
OR03	Pre-Routed Three Input OR Gate
OR04	Pre-Routed Four Input OR Gate
PP01	V_{SS} Ground Pin
PP02	V_{DD} Power Pin
RS00	Pre-Routed Set-Reset NAND Gate Latch
RS01	Pre-Routed NOR S R Latch
TG01	Pre-Routed Transmission Gate

Data Sheets

3μ HCMOS Single-Metal Gate Array

The Gould AMI 3μ Single Metal Gate Array Macro Library is a collection of high performance digital integrated circuit building blocks. It is intended for use by logic, circuit, and MOS IC designers. Thus, anyone familiar with standard logic design methods can successfully design a gate array using these macros.

The 3μ Single Metal Macro Cells are implemented with a P-well, CMOS process. They are intended primarly for 5 volt (+ 10%) operation but will operate at voltages as low as 2.5 volts with reduced performance. Below is a description of the data and terms used in the data sheets.

- **PRE-ROUTED MACROS** are the simpler functional blocks such as the basic gates, latches, and flip-flops. Since these macros have a pre-defined layout they can be accurately characterized for propagation delays.

- **SOFTWARE MACROS** are macros which incorporate several pre-routed macros to form more complicated functional blocks such as counters or shift registers. These macros are not pre-defined with respect to layout, so the automatic placement and routing software maintains optimum layout flexibility. Since layout is not pre-defined, estimates of propagation delays through these macros are arrived at by adding the delays of the individual pre-routed macros used in the software macros.

- **THE CELL NAME** for each functional macro is displayed in the upper right hand corner of each data sheet. This is the same name that appears in the Bolt invocation.

- **THE LOGIC SYMBOL** for each macro is displayed as it appears in the gate array library.

- **A TRUTH TABLE** description of the logical functions for the cells is provided.

- **THE TABLE OF INPUT LOADING** gives the number of equivalent unit loads for each logical input of the pre-routed macros.

- **THE EQUIVALENT GATE COUNT** is the number of equivalent two input NAND gates in each cell.

- **BOLT SYNTAX** is the invocation syntax of each macro cell. Notice these statements always end with a semi-colon, and the order of these inputs and outputs must be maintained.

- **THE SWITCHING CHARACTERISTICS** give the propagation delay as a function of unit load. The unit load is the capacitance associated with a gate pair (i.e., the gate capacitance of an N-channel and a P-channel core transistor), plus an associated metal interconnection capacitance. All data is given for typical process, temperature, and power supply conditions. Both low-to-high transitions are shown. To find delays under other operating conditions derating curves must be used.

- **THE PROPAGATION DELAY EQUATION** is used for calculating propagation delays when the load is different from those explicitly given in the table. The intrinsic propagation delay, t_{dx}, is used when there is no output loading, and $k_{t_{dx}}$, is a capacitive multiplication factor. As an example consider the two input NAND Gate with a fan-out of 5. To calculate the propagation delay for the high-to-low transition use $t_{dx} = 0.1$ and $k_{t_{dx}} = 1.8$ so,

  $$t_{PHL} = 0.1 + (1.8)(.25)(5) = 2.35\text{ns}.$$

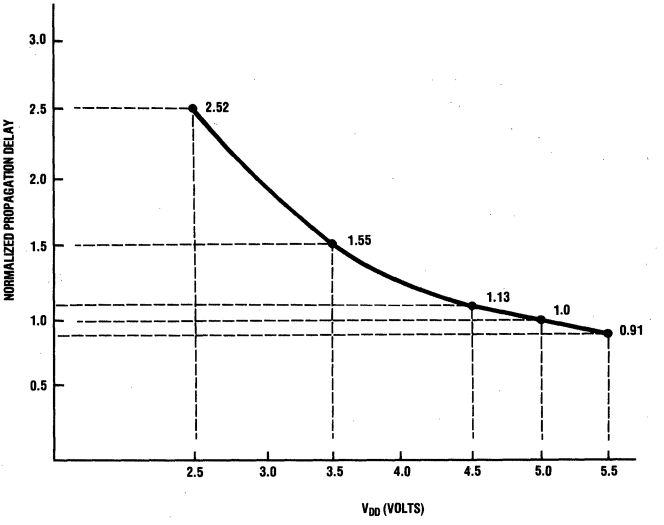
- **A LOGIC SCHEMATIC** is shown for the more complicated prerouted macros and the software macros not shown.

- **POWER SUPPLY MACROS** (PP01, PP02) must be shown on each circuit. While no connections to these macros are necessary, one macro must be shown per power or ground pin.

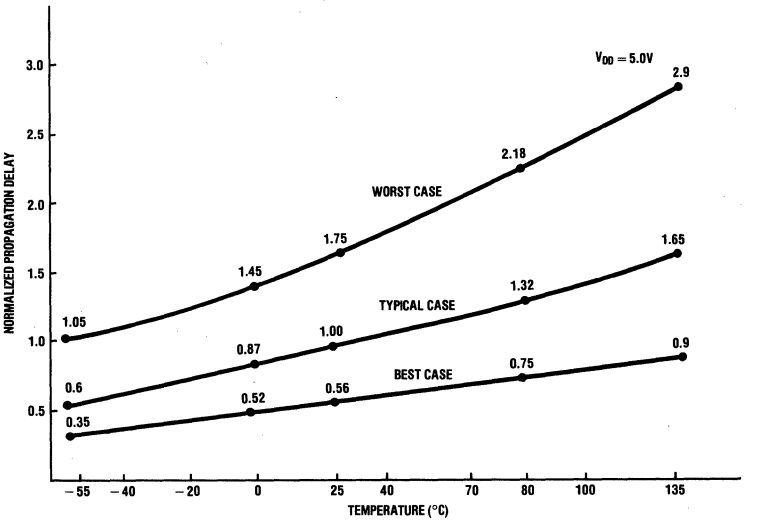
- **DERATING CURVES** are provided to account for changes in propagation delay as process, temperature and power supply vary.

Derating Curves

Normalized Delays vs. Power Supply Voltage



Normalized Delays vs. Process Model and Temperature



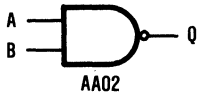
AA02

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Two Input AND Gate

Logic Symbol



Truth Table

A	B	Q
L	X	L
X	L	L
H	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 1.5
Bolt Syntax: Q .AA02 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	1.8	2.5	3.2	3.9	6.7
		t_{PHL}	2.2	2.5	2.8	3.1	4.4

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
1.0	2.85
1.9	1.20

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

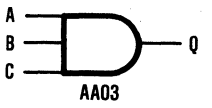
Unit Load = .25 pF including statistical wiring capacitance

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Three Input AND Gate

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .AA03 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.5	3.2	4.0	4.7	7.6
		t_{PHL}	2.9	3.2	3.5	3.8	5.1

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
1.8	2.92
2.5	1.30

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

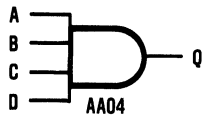
AA04

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Four Input AND Gate

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .AA04 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.4	4.1	4.9	5.6	8.6
		t_{PHL}	3.2	3.6	3.9	4.2	5.6

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
2.7	2.97
2.9	1.33

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

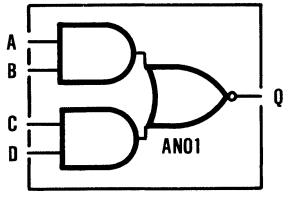
AN01

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed AND-NOR Gates

Logic Symbol



Truth Table

A	B	C	D	Q
H	H	H	H	L
H	H	X	X	L
X	X	H	H	L
All Other				H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .AN01 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	6.6	8.1	9.5	11.0	16.8
		t_{PHL}	1.3	1.8	2.3	2.7	4.6

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
5.2	5.80
0.9	1.84

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

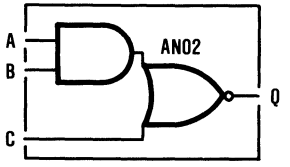
AN02

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed AND-NOR Gates

Logic Symbol



Truth Table

A	B	C	Q
H	H	H	L
H	H	X	L
X	X	H	L
All Other			H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 1.5
Bolt Syntax: Q .AN02 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	4.6	6.0	7.5	8.9	14.7
		t_{PHL}	0.8	1.3	1.7	2.2	4.1

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
3.1	5.80
0.3	1.86

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

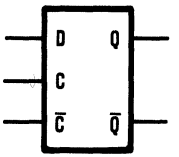
DF01

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop

Logic Symbol



DF01

Truth Table

C	CN	D	Q	QN
L	H	X	No Change	
↑	↓	L	L	H
↑	↓	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	2

Equivalent Gate Count: 5
Bolt Syntax: Q QN .DF01 D C CN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	3.0	3.4	3.9	4.3	6.0
		t_{PHL}	2.4	2.6	2.9	3.1	4.1
C	QN	t_{PLH}	4.1	4.8	5.6	6.3	9.2
		t_{PHL}	3.2	3.5	3.8	4.1	5.3

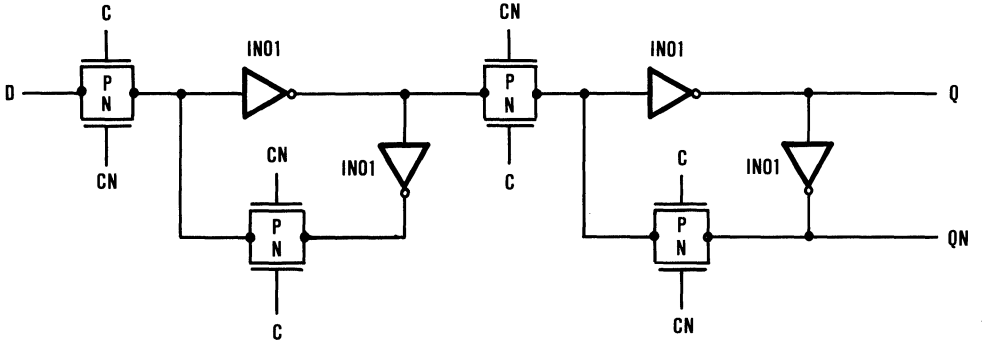
Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
2.6	1.70
2.2	1.00
3.4	2.90
2.9	1.20

Set-Up	To H	1.8
Set-Up	To L	2.2

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

DF01 :



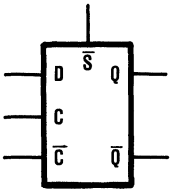
DF02

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Active Low Set

Logic Symbol



DF02

Truth Table

SN	C	CN	D	Q	QN
H	L	H	X	No Change	
H	↑	↓	L	L	H
H	↑	↓	H	H	L
L	X	X	X	H	L

Input Loading

Logic Input	Equivalent Unit Loads
D	2.5
All Other	2

Equivalent Gate Count: 5
Bolt Syntax: Q QN .DF02 D C CN SN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	3.4	4.2	4.9	5.7	8.6
		t_{PHL}	3.1	3.5	4.0	4.5	6.5
C	QN	t_{PLH}	4.6	5.4	6.1	6.8	9.6
		t_{PHL}	3.6	3.9	4.2	4.5	5.7
SN	Q	t_{PLH}	2.6	3.3	4.0	4.8	7.6
SN	Q	t_{PHL}	3.0	3.3	3.6	3.8	5.0

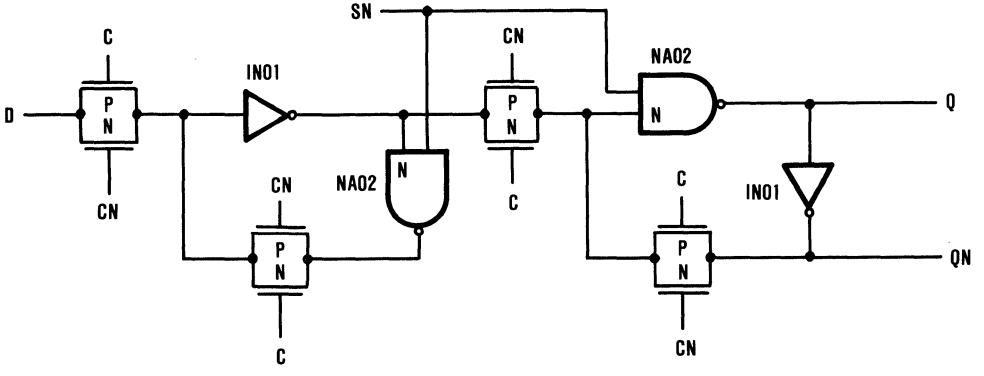
Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
2.7	2.99
2.6	1.97
3.9	2.85
3.3	1.17
1.9	2.85
2.7	1.11

Set-Up	To H	2.8
Set-Up	To L	3.0

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

DF02:



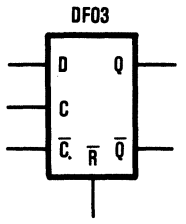
DF03

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Active Low Set

Logic Symbol



Truth Table

RN	C	CN	D	Q	QN
H	L	H	X	No Change	
H	↑	↓	L	L	H
H	↑	↓	H	H	L
L	X	X	X	L	H

Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	2

Equivalent Gate Count: 5
Bolt Syntax: Q QN .DF03 D C CN RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	3.8	4.6	5.4	6.1	9.2
		t_{PHL}	2.7	3.1	3.5	3.8	5.3
C	QN	t_{PLH}	4.7	5.4	6.2	6.9	9.8
		t_{PHL}	4.1	4.5	5.0	5.4	7.1
RN	QN	t_{PLH}	3.5	4.2	4.9	5.5	8.2
RN	Q	t_{PHL}	3.8	4.2	4.6	4.9	6.4

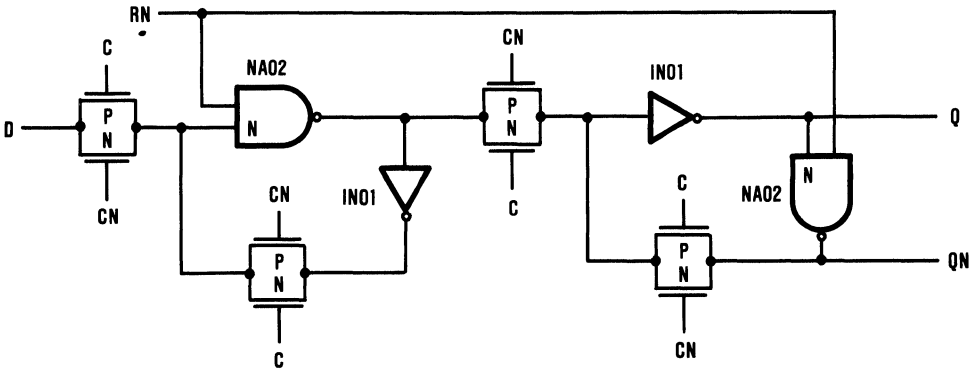
Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
3.0	3.10
2.3	1.50
4.0	2.90
3.7	1.70
2.8	2.70
3.4	1.50

Set-Up	To H	2.7
Set-Up	To L	3.1

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

DF03:

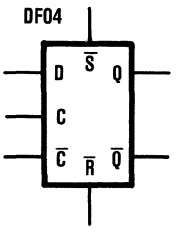


3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Active Low Set And Active Low Reset

Logic Symbol



Truth Table

SN	RN	C	CN	D	Q	QN
H	H	L	H	X	No Change	
H	H	↑	↓	L	L	H
H	H	↑	↓	H	H	L
H	L	X	X	X	L	H
L	H	X	X	X	H	L
L	L	X	X	X	Illegal	

Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	2

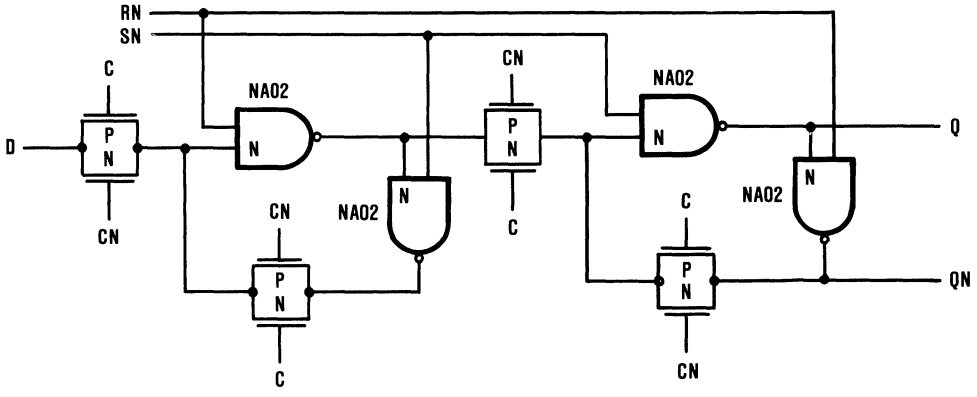
Equivalent Gate Count: 7
Bolt Syntax: Q QN .DF04 D C CN SN RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	4.5	5.2	6.0	6.7	9.8
		t_{PHL}	3.1	3.5	4.0	4.5	6.5
C	QQ	t_{PLH}	5.3	6.1	6.8	7.5	10.4
		t_{PHL}	4.8	5.3	5.7	6.2	7.9
SN	Q	t_{PLH}	2.2	2.9	3.6	4.4	7.3
SN	Q	t_{PHL}	4.6	5.1	5.7	6.2	8.3
RN	QN	t_{PLH}	3.6	4.3	5.0	5.7	8.4
RN	Q	t_{PHL}	4.9	5.4	6.0	6.5	8.6
Set-Up		To H		3.4			
Set-Up		To L		3.6			

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
3.7	3.05
2.6	1.95
4.6	2.89
4.4	1.74
1.4	2.95
4.1	2.10
3.0	2.71
4.4	2.10

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance


RN
SN
C
D
P
N
CN
NA02
N
CN
NA02
N
P
N
C
CN
NA02
N
C
P
N
CN
NA02
N
Q
QN

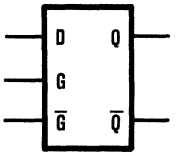
DL01

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Q and QN

Logic Symbol



DL01

Truth Table

G	GN	D	Q	QN
L	H	X	No Change	
H	L	D	D	DN

Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q QN .DL01 D G GN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

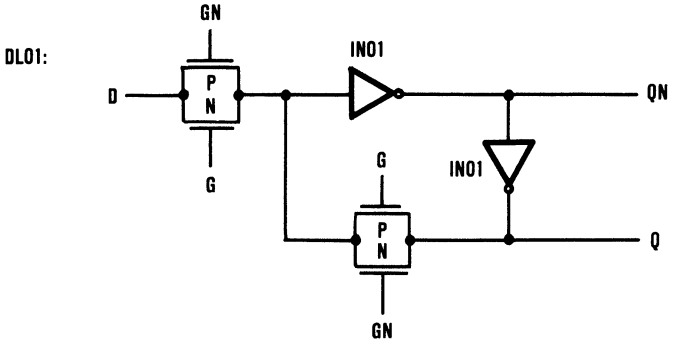
Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
G	Q	t_{LH}	4.3	5.0	5.7	6.4	9.3
		t_{HL}	3.1	3.4	3.7	3.9	5.1
G	QN	t_{LH}	2.8	3.2	3.6	4.0	5.7
		t_{HL}	2.5	2.8	3.0	3.3	4.4
D	Q	t_{PLH}	2.1	2.9	3.6	4.3	7.2
D	Q	t_{PHL}	2.2	2.5	2.8	3.0	4.1
D	QN	t_{PLH}	1.9	2.3	2.7	3.2	4.8
D	QN	t_{PHL}	0.5	0.8	1.0	1.3	2.4

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
3.6	2.85
2.8	1.12
2.4	1.65
2.2	1.06
1.4	2.90
1.9	1.10
1.5	1.67
0.2	1.11

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

DL01:



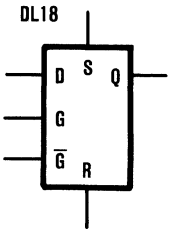
DL18

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Asynchronous Set And Reset

Logic Symbol



Truth Table

S	R	G	GN	D	Q
L	L	L	H	X	No Change
L	L	H	L	D	D
L	H	X	X	X	L
H	L	X	X	X	H
H	H	X	X	X	L

Input Loading

Logic Input	Equivalent Unit Loads
D	2.5
All Other	1

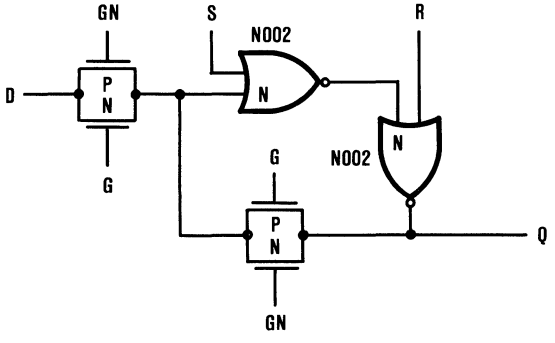
Equivalent Gate Count: 3.5
Bolt Syntax: Q .DL18 D G GN S R;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8	Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
G	Q	t_{PLH}	5.7	6.9	8.1	9.4	14.3	4.5	4.90
		t_{PHL}	4.0	4.3	4.7	5.0	6.3	3.7	1.30
D	Q	t_{PLH}	4.0	5.2	6.5	7.7	12.6	2.8	4.90
		t_{PHL}	3.3	3.6	4.0	4.3	5.6	3.0	1.30
S	Q	t_{PLH}	6.0	7.2	8.5	9.7	14.6	4.8	4.90
R	Q	t_{PHL}	1.2	1.5	1.9	2.2	3.5	0.9	1.30

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

DL18:



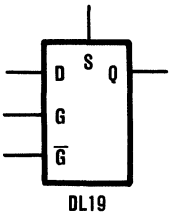
DL19

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Set

Logic Symbol



DL19

Truth Table

S	G	GN	D	Q
L	L	H	X	No Change
L	H	L	D	D
H	X	X	X	H

Input Loading

Logic Input	Equivalent Unit Loads
D	2.5
All Other	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .DL19 D G GN S;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

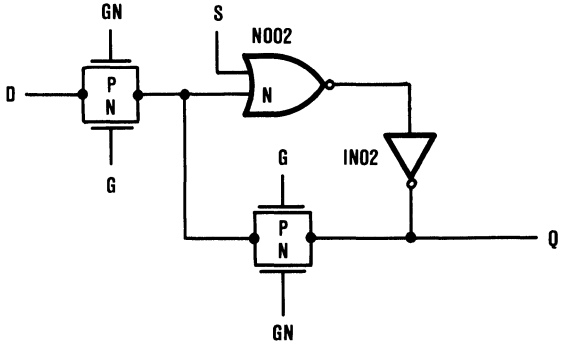
Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
G	Q	t_{PLH}	4.3	5.0	5.7	6.5	9.4
		t_{PHL}	3.9	4.2	4.6	4.9	6.2
D	Q	t_{PLH}	2.5	3.2	3.9	4.7	7.6
		t_{PHL}	3.2	3.5	3.9	4.2	5.5
S	Q	t_{PLH}	3.4	4.1	4.9	5.6	8.5

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
3.6	2.90
3.6	1.30
1.8	2.90
2.9	1.30
2.7	2.90

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

DL19:



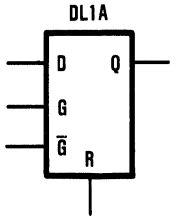
DL1A

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Reset

Logic Symbol



Truth Table

R	G	GN	D	Q
L	L	H	X	No Change
L	H	L	D	D
H	X	X	X	L

Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .DL1A D G GN R;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

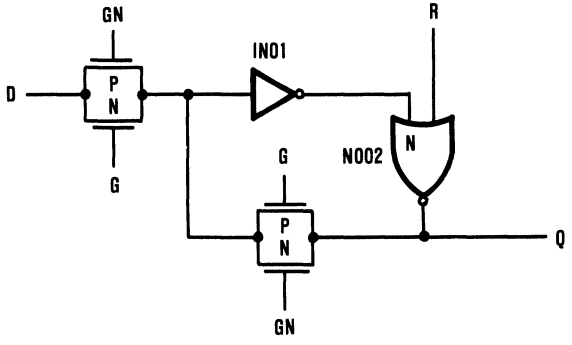
Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
G	Q	t_{PLH}	5.6	6.9	8.1	9.3	14.2
		t_{PHL}	3.3	3.5	3.8	4.1	5.2
D	Q	t_{PLH}	4.0	5.2	6.4	7.7	12.5
		t_{PHL}	2.5	2.8	3.1	3.4	4.6
R	Q	t_{PLH}	1.2	1.5	1.8	2.2	3.4

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
4.4	4.88
3.0	1.11
2.8	4.87
2.2	1.20
0.9	1.27

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

DL1A:



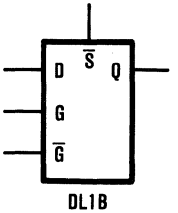
DL1B

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Active Low Set

Logic Symbol



DL1B

Truth Table

SN	G	GN	D	Q
H	L	H	X	No Change
H	H	L	D	D
L	X	X	X	H

Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	1

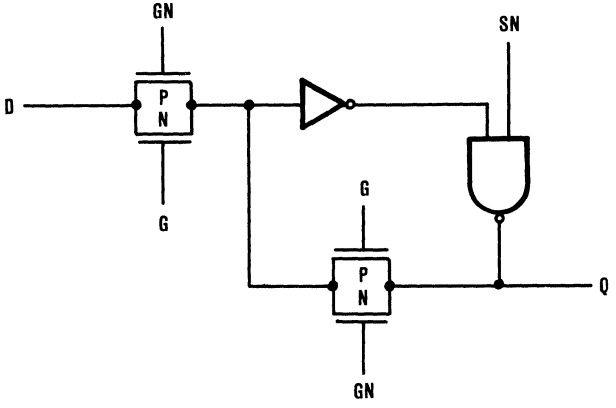
Equivalent Gate Count: 2.5
Bolt Syntax: Q .DL1B D G GN SN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8	Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
G	Q	t_{PLH}	4.3	5.0	5.7	6.4	9.2	3.6	2.80
		t_{PHL}	3.7	4.1	4.6	5.0	6.7	3.3	1.70
D	Q	t_{PLH}	2.6	3.3	4.0	4.8	7.7	1.9	2.90
		t_{PHL}	3.0	3.5	3.9	4.3	6.1	2.6	1.80
SN	Q	t_{PLH}	3.9	4.5	5.2	5.8	8.5	3.2	2.60

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

DL1B:



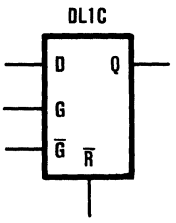
DL1C

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Active Low Reset

Logic Symbol



Truth Table

RN	G	GN	D	Q
H	L	H	X	No Change
H	H	L	D	D
L	X	X	X	L

Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .DL1C D G GN RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

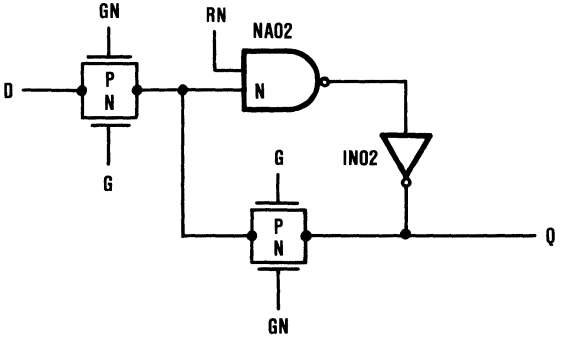
Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
G	Q	t_{PLH}	4.5	5.3	6.0	6.7	9.6
		t_{PHL}	3.4	3.6	3.9	4.2	5.3
D	Q	t_{PLH}	3.0	3.7	4.4	5.1	8.0
		t_{PHL}	2.6	2.9	3.2	3.5	4.6
RN	Q	t_{PHL}	3.0	3.3	3.6	3.9	5.0

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
3.8	2.87
3.1	1.12
2.2	2.88
2.3	1.15
2.8	1.13

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

DL1C:



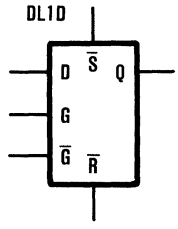
DL1D

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Active Low Set And Reset

Logic Symbol



Truth Table

SN	RN	G	GN	D	Q
H	H	L	H	X	No Change
H	H	H	L	D	D
H	L	X	X	X	L
L	H	X	X	X	H
L	L	X	X	X	H

Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	1

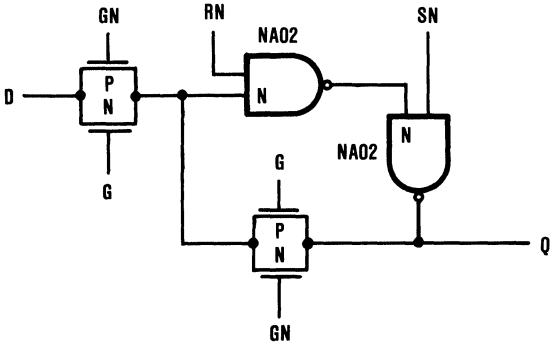
Equivalent Gate Count: 3.5
Bolt Syntax: Q .DL1D D G GN SN RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8	Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
D	Q	t_{PLH}	4.8	5.5	6.3	7.0	9.9	4.1	2.90
		t_{PHL}	4.1	4.6	5.2	5.7	7.9	3.5	2.20
D	QQ	t_{PLH}	3.2	3.9	4.7	5.4	8.3	2.5	2.90
		t_{PHL}	3.5	4.0	4.6	5.1	7.2	3.0	2.10
SN	Q	t_{PLH}	4.1	4.8	5.5	6.1	8.8	3.4	2.70
RN	Q	t_{PHL}	4.6	5.1	5.7	6.2	8.3	4.1	2.10

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

DL1D:



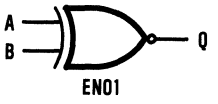
EN01

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Two Input Exclusive—NOR Gate

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	L	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	2

Equivalent Gate Count: 2.5
Bolt Syntax: Q .EN01 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.0	2.7	3.4	4.2	7.1
		t_{PHL}	2.6	3.1	3.5	4.0	5.8

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
1.3	2.90
2.2	1.84

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

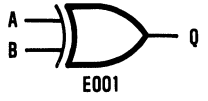
EO01

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Two Input Exclusive—OR Gate

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	2

Equivalent Gate Count: 2.5
Bolt Syntax: Q .EO01 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	4.0	5.4	6.9	8.3	14.1
		t_{PHL}	2.7	3.0	3.4	3.7	5.1

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
2.6	5.75
2.4	1.35

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

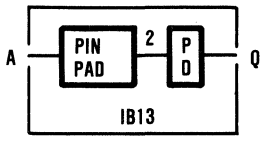
IB13

3μ Single-Metal HCMOS Gate Arrays

Description

Input Pad With Protection Diode.

Logic Symbol



Truth Table

A	Q
H	H
L	L

Input Loading

Logic Input	Equivalent Unit Loads
N.A.	

Equivalent Gate Count: Contained within peripheral cells, no core devices used.
Bolt Syntax: Q .IB13 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH} t_{PHL}					

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

NOTE: Delay not applicable because of external drive.

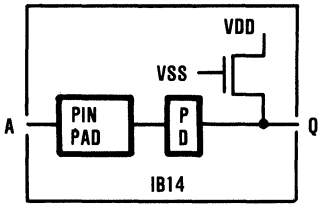
IB14

3μ Single-Metal HCMOS Gate Arrays

Description

Input Pad With Protection Diode And P-Channel Transistor

Logic Symbol



Truth Table

A	Q
H	H
L	L

Input Loading

Logic Input	Equivalent Unit Loads
N.A.	

Equivalent Gate Count: Contained within peripheral cells, no core devices used.
Bolt Syntax: Q .IB14 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH} t_{PHL}					

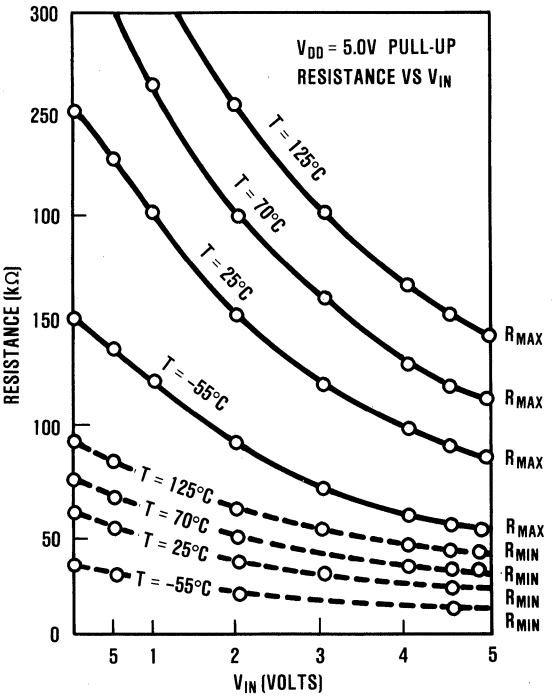
Intrinsic Parameters t_{dx}	$k_{t_{dx}}$

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

NOTE: Delay not applicable because of external drive.

3-MICRON SINGLE METAL GATE ARRAY



Gate Array Pull-Up Characteristics

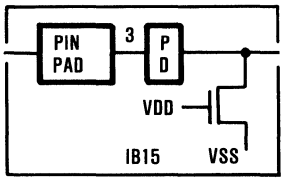
IB15

3μ Single-Metal HCMOS Gate Arrays

Description

Input Pad With Protection Diode And N-Channel Transistor

Logic Symbol



Truth Table

A	Q
H	H
L	L

Input Loading

Logic Input	Equivalent Unit Loads
N.A.	

Equivalent Gate Count: Contained within peripheral cells, no core devices used.
Bolt Syntax: Q .IB15 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

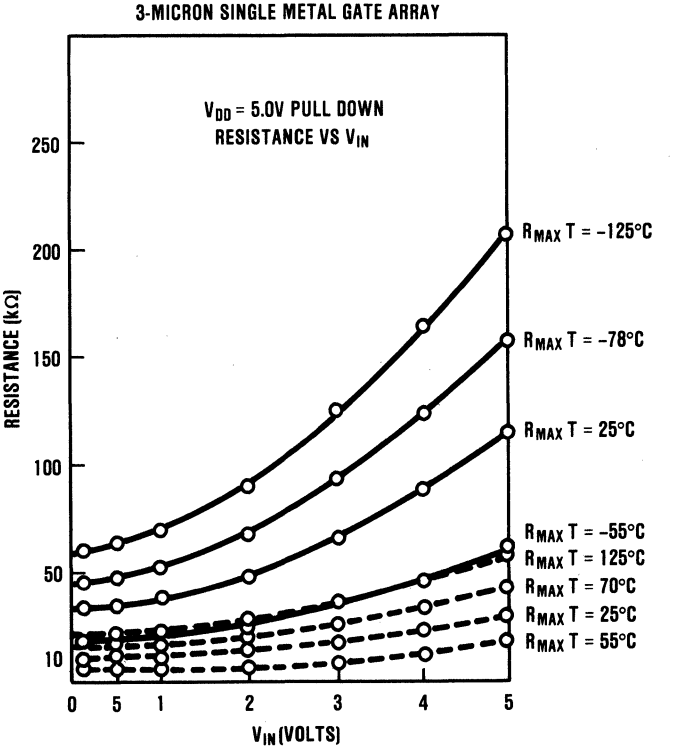
Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH} t_{PHL}					

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

NOTE: Delay not applicable because of external drive.



Gate Array Pull-Down Characteristics

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Inverting Schmitt Trigger

Logic Symbol

IIF0

Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	2

Equivalent Gate Count: 1.5
Bolt Syntax: Q .IIF0 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	4.6	5.9	7.3	8.6	12.4
		t_{PHL}	2.2	2.7	3.3	3.8	4.6

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
3.3	5.40
1.7	2.10

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

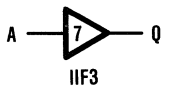
	V_{IH}	V_{IL}	HYSTERISIS
Trip Points	3.0V	1.6V	1.4V

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed TTL Lever Translator

Logic Symbol



IIF3

Truth Table

A	Q
H	H
L	L

Input Loading

Logic Input	Equivalent Unit Loads
A	4

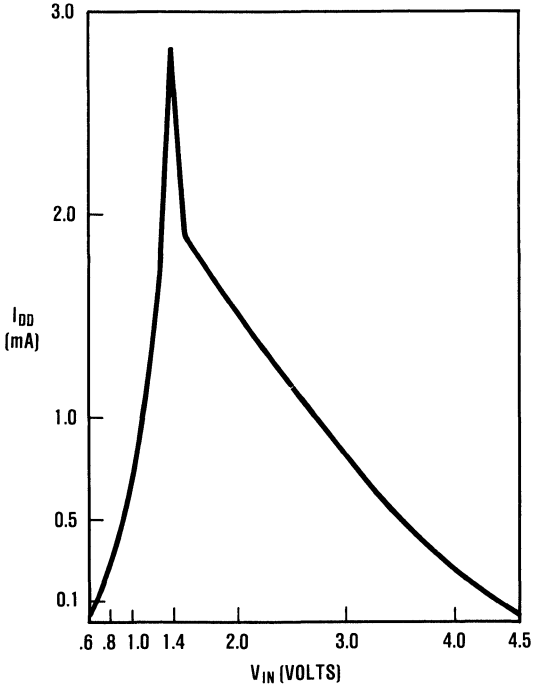
Equivalent Gate Count: 2.5
Bolt Syntax: Q .IIF3 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	5.3	6.0	6.7	7.5	10.4
		t_{PHL}	3.9	4.2	4.6	4.9	6.3

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
4.6	2.90
3.5	1.40

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance



I_{DD} VS. V_{IN} FOR TTL Level Translators

3μ Single-Metal HCMOS Gate Arrays

Description

Single Pre-Routed Inverter

Logic Symbol

IN01

Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	1

Equivalent Gate Count: 1
Bolt Syntax: Q .IN01 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	1.6	2.4	3.1	3.8	6.7
		t_{PHL}	0.1	0.5	0.9	1.2	2.6

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
0.9	2.92
0.0	1.43

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

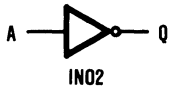
IN02

3μ Single-Metal HCMOS Gate Arrays

Description

Two Pre-Routed Inverters In Parallel

Logic Symbol



Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	2

Equivalent Gate Count: 1
Bolt Syntax: Q .IN02 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	1.0	1.4	1.8	2.2	3.7
		t_{PHL}	0.1	0.3	0.6	0.8	1.7

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
0.6	1.55
0.0	0.90

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

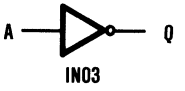
IN03

3μ Single-Metal HCMOS Gate Arrays

Description

Three Pre-Routed Inverters In Parallel

Logic Symbol



IN03

Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	3

Equivalent Gate Count: 1.5
Bolt Syntax: Q .IN03 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 4	8	12	16	20
Any Input	Q	t_{PLH}	2.0	3.1	4.3	5.5	6.7
		t_{PHL}	0.2	0.9	1.7	2.4	3.1

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
0.8	1.20
0.0	0.72

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

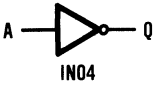
Unit Load = .25 pF including statistical wiring capacitance

3μ Single-Metal HCMOS Gate Arrays

Description

Four Pre-Routed Inverters in Parallel

Logic Symbol



Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	4

Equivalent Gate Count: 2.5
Bolt Syntax: Q .IN04 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 4	8	12	16	20
Any Input	Q	t_{PLH}	1.4	2.3	3.2	4.1	5.0
		t_{PHL}	0.2	0.8	1.4	2.0	2.7

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
0.5	0.90
0.0	0.62

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

IN05

3μ Single-Metal HCMOS Gate Arrays

Description

Five Pre-Routed Inverters in Parallel

Logic Symbol

IN05

Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	5

Equivalent Gate Count: 2.5
Bolt Syntax: Q .IN05 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 4	8	12	16	20
Any Input	Q	t_{PLH}	1.5	2.2	3.0	3.8	4.6
		t_{PHL}	0.1	0.6	1.2	1.7	2.3

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
0.7	0.80
0.0	0.54

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

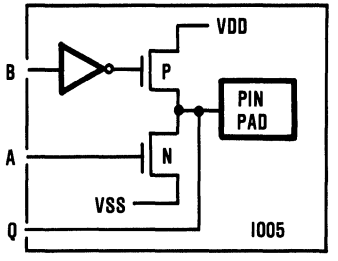
IO05

3μ Single-Metal HCMOS Gate Arrays

Description

Tri-State Input-Output Buffer

Logic Symbol



Truth Table

A	B	Q
L	H	L
L	L	Z
H	L	L
H	H	Illegal

Input Loading

Logic Input	Equivalent Unit Loads
B	3
A	4

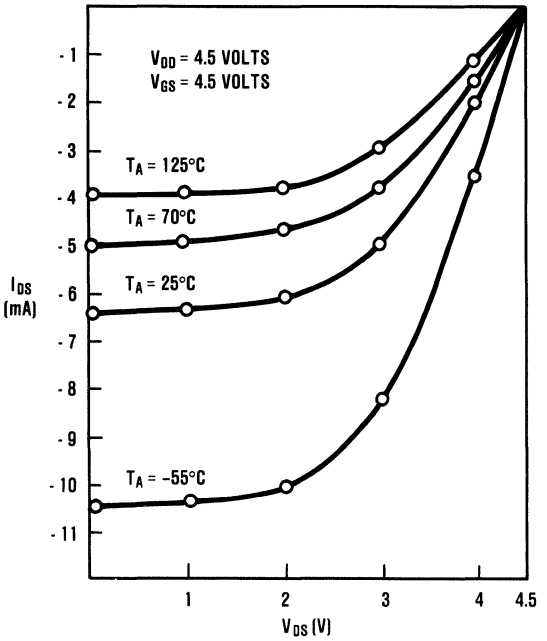
Equivalent Gate Count: Contained within peripheral cells, no core devices used.
Bolt Syntax: Q .IO05 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF	Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
A	Q	t_{PLH}	9.3	16.2	23.1	2.5	0.14
		t_{PHL}	5.6	10.4	15.2	0.8	0.10
ENABLE	Q	t_{PZH}	8.4	15.2	22.1	1.5	0.14
		t_{PZL}	5.7	11.4	17.0	0.1	0.11
DISABLE	Q	t_{PLZ}		0.6		0.6	0.00
		t_{PHZ}		1.8		1.8	0.00

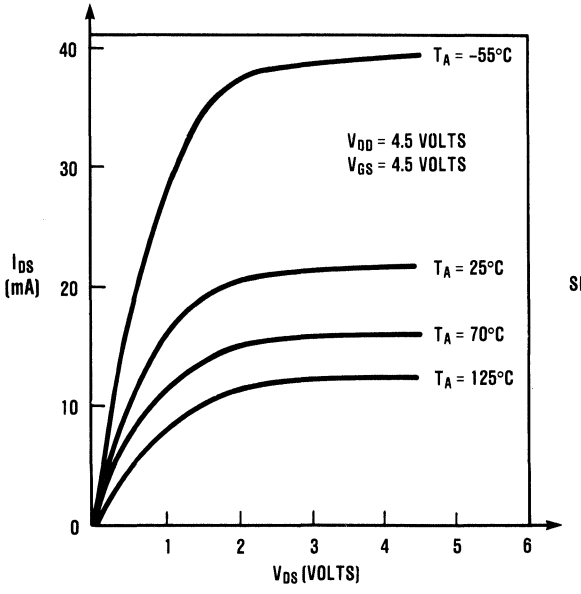
Symbol	Parameters	Conditions	Min.	Typ.	Max.
I_{DSS}	Output Leakage Current		−10 μA		+10μA
V_{OL}	Low Level Output Voltage	$I_{OL} = 4.0$ mA			.4V
V_{OH}	High Level Output Voltage	$I_{OH} = 5.0$ mA	2.4V		

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance



P-CHANNEL DRIVER
SOURCING CHARACTERISTICS



N-CHANNEL DRIVER
SINKING CHARACTERISTICS

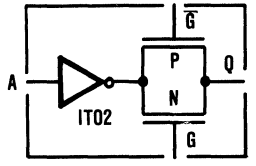
IT02

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Inverter Driving a Transmission Gate.

Logic Symbol



Truth Table

A	G	GN	Q
A	L	H	Z
A	H	L	AN

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .IT02 A G GN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
G	Q	t_{PLH}	2.3	3.3	4.4	5.4	9.5
		t_{PHL}	1.2	1.7	2.3	2.8	5.0
A	Q	t_{PLH}	3.4	4.4	5.5	6.5	10.6
		t_{PHL}	1.1	1.6	2.1	2.6	4.6

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
1.3	4.10
0.6	2.20
2.4	4.10
0.6	2.00

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

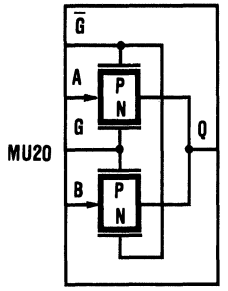
MU20

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Two To One Multiplexer

Logic Symbol



Truth Table

A	B	G	GN	Q
A	B	L	H	B
A	B	H	L	A

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	2

Equivalent Gate Count: 1
Bolt Syntax: Q .MU20 A B G GN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A,B	Q	t_{PLH}	1.6	2.2	2.8	3.4	5.8
		t_{PHL}	1.1	1.6	2.1	2.5	4.4
G	Q	t_{PLH}	3.2	4.4	5.5	6.6	11.2
		t_{PHL}	1.1	1.6	2.2	2.8	5.1
GN	Q	t_{PLH}	3.5	4.7	5.9	7.1	11.9
		t_{PHL}	2.5	3.0	3.4	3.9	5.7

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
0.9	2.43
0.6	1.91
2.1	4.56
0.5	2.28
2.3	4.78
2.0	1.84

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

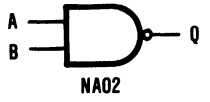
NA02

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Two Input NAND Gate

Logic Symbol



NA02

Truth Table

A	B	Q
L	X	H
X	L	H
H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 1
Bolt Syntax: Q .NA02 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.2	2.9	3.6	4.4	7.3
		t_{PHL}	0.5	1.0	1.5	1.9	3.8

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
1.4	2.95
0.1	1.84

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

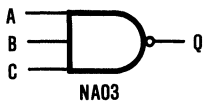
NA03

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Three Input NAND Gate

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 1.5
Bolt Syntax: Q .NA03 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.8	3.5	4.3	5.0	8.0
		t_{PHL}	1.2	1.8	2.4	3.0	5.4

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
2.0	2.97
0.6	2.43

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

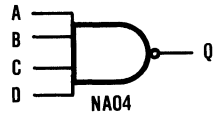
NA04

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Four Input NAND Gate

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .NA04 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.4	4.2	5.0	5.7	8.8
		t_{PHL}	2.2	3.0	3.8	4.6	7.9

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
2.6	3.08
1.3	3.30

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

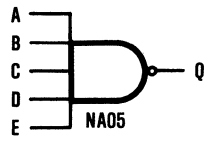
NA05

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Five Input NAND Gate

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .NA05 A B C D E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.9	4.7	5.5	6.3	9.4
		t_{PHL}	3.3	4.3	5.3	6.3	10.2

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
3.1	3.15
2.3	3.99

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

NO02

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Two Input NOR Gate

Logic Symbol

NO02

Truth Table

A	B	Q
L	L	H
X	H	L
H	X	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 1
Bolt Syntax: Q .NO02 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.8	4.0	5.2	6.4	11.3
		t_{PHL}	0.4	0.7	1.1	1.4	2.8

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
1.6	4.84
0.1	1.37

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

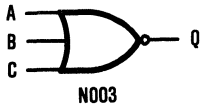
NO03

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Three Input NOR Gate

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 1.5
Bolt Syntax: Q .NO03 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	5.2	6.9	8.7	10.4	17.2
		t_{PHL}	0.6	1.0	1.3	1.7	3.1

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
3.5	6.82
0.2	1.44

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

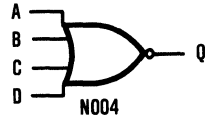
NO04

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Four Input NOR Gate

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
X	X	X	H	L
X	X	H	X	L
X	H	X	X	L
H	X	X	X	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .NO04 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	8.3	10.7	13.2	15.6	25.4
		t_{PHL}	0.7	1.0	1.4	1.8	3.3

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
5.8	9.80
0.3	1.50

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

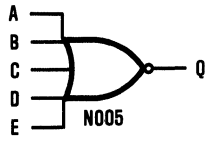
NO05

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Five Input NOR Gate

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
X	X	X	X	H	L
X	X	X	H	X	L
X	X	H	X	X	L
X	H	X	X	X	L
H	X	X	X	X	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .NO05 A B C D E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	12.4	15.3	18.2	21.1	32.9
		t_{PHL}	0.9	1.2	1.5	1.9	3.2

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
9.4	11.72
0.5	1.36

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

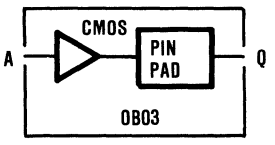
OB03

3μ Single-Metal HCMOS Gate Arrays

Description

CMOS Output Buffer

Logic Symbol



Truth Table

A	Q
L	L
H	H

Input Loading

Logic Input	Equivalent Unit Loads
A	3

Equivalent Gate Count: Contained within peripheral cells, no core devices used.
Bolt Syntax: Q .OB03 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

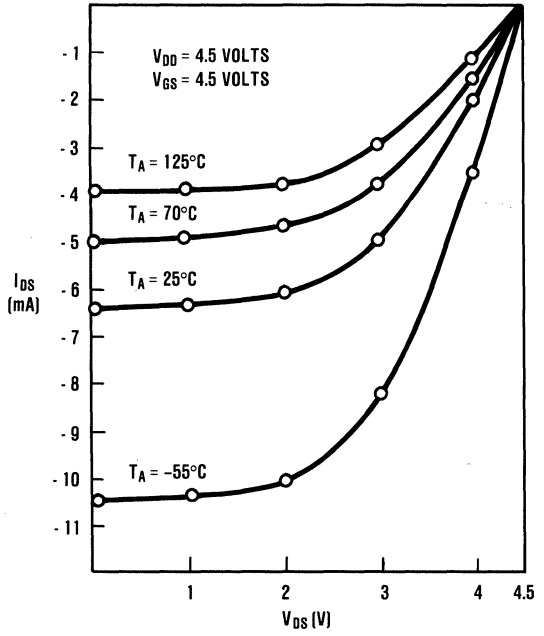
Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	Q	t_{PLH}	9.0	15.6	22.2
		t_{PHL}	6.8	11.2	15.7
A	Q	t_{PLH}	5.9	9.8	13.8
(I TTL LOAD)		t_{PHL}	10.0	17.3	24.6

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
2.3	0.13
2.3	0.09
1.9	0.08
2.7	0.15

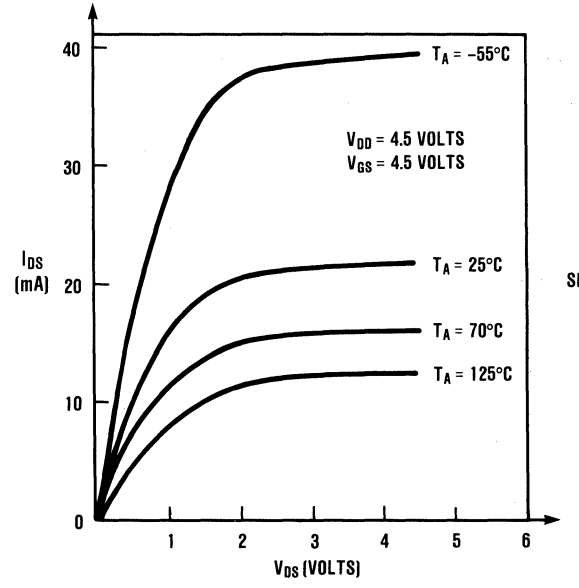
Symbol	Parameters	Conditions	Min.	Typ.	Max.
I_{DSS}	Output Leakage Current		−10 μA		+10μA
V_{OL}	Low Level Output Voltage	$I_{OL} = 1$ μA			.05V
V_{OH}	High Level Output Voltage	$I_{OH} = 1$ μA	4.95V		

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance



P-CHANNEL DRIVER
SOURCING CHARACTERISTICS



N-CHANNEL DRIVER
SINKING CHARACTERISTICS

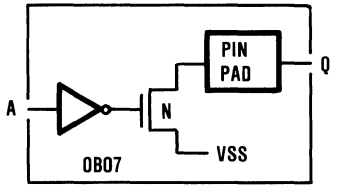
OB07

3μ Single-Metal HCMOS Gate Arrays

Description

Open Drain N-Channel Output Buffer

Logic Symbol



Truth Table

A	Q
H	Z
L	L

Input Loading

Logic Input	Equivalent Unit Loads
A	3

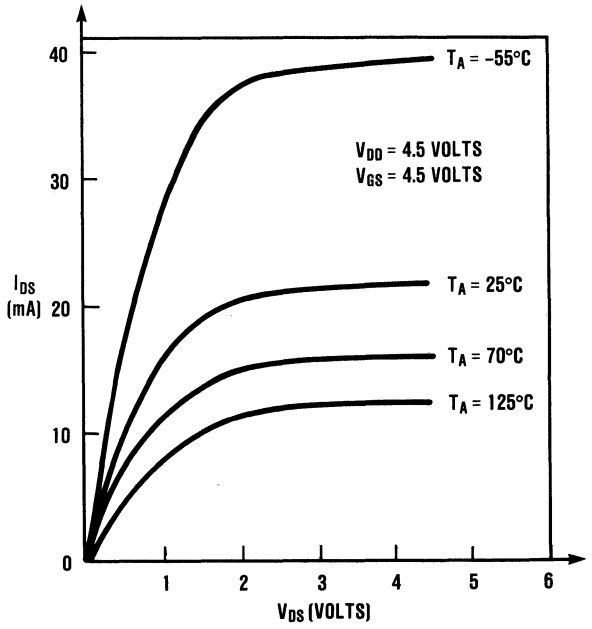
Equivalent Gate Count: Contained within peripheral cells, no core devices used.
Bolt Syntax: Q .OB07 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF	Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
A	Q (1K Resistor)	t_{PHL}	5.8	10.4	15.0	1.3	0.09
A	Q (10K Resistor)	t_{PHL}	5.6	10.0	14.4	1.2	0.09
A	Q	t_{PLZ}		0.6		0.6	

Symbol	Parameters	Conditions	Min.	Typ.	Max.
I_{DSS}	Output Leakage Current		−10 μA		+10μA
V_{OL}	Low Level Output Voltage	$I_{OL} = 4.0$ μA			.4V
V_{OH}	High Level Output Voltage	$I_{OH} = 5.0$ μA	2.4V		

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance



N-CHANNEL DRIVER
SINKING CHARACTERISTICS

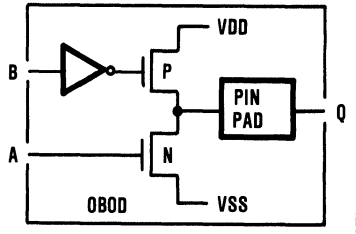
OB0D

3μ Single-Metal HCMOS Gate Arrays

Description

Tri-State Output Buffers

Logic Symbol



Truth Table

A	B	Q
L	H	H
L	L	Z
H	L	L
H	H	Illegal

Input Loading

Logic Input	Equivalent Unit Loads
B	3
A	4

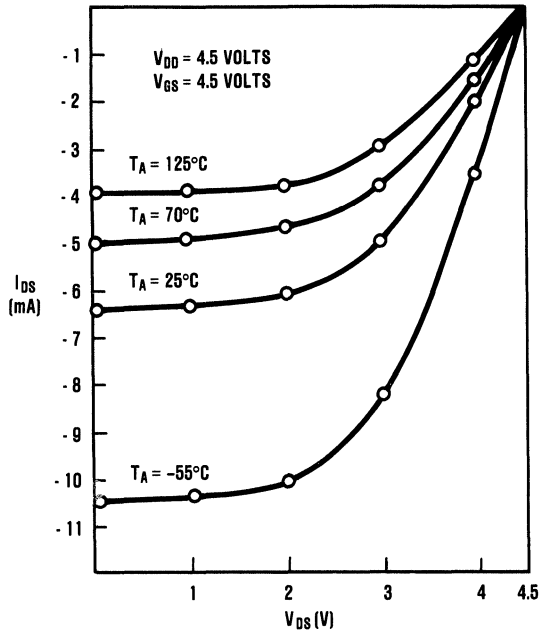
Equivalent Gate Count: Contained within peripheral cells, no core devices used.
Bolt Syntax: Q .OB0D A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF	Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
A	Q	t_{PLH}	9.3	16.2	23.1	2.5	0.14
		t_{PHL}	5.6	10.4	15.2	0.8	0.10
ENABLE	Q	t_{PZL}	8.4	15.2	22.1	1.5	0.14
		t_{PZL}	5.7	11.4	17.0	0.1	0.11
DISABLE	Q	t_{PLZ}		0.6		0.6	0.00
		t_{PHZ}		1.8		1.8	0.00

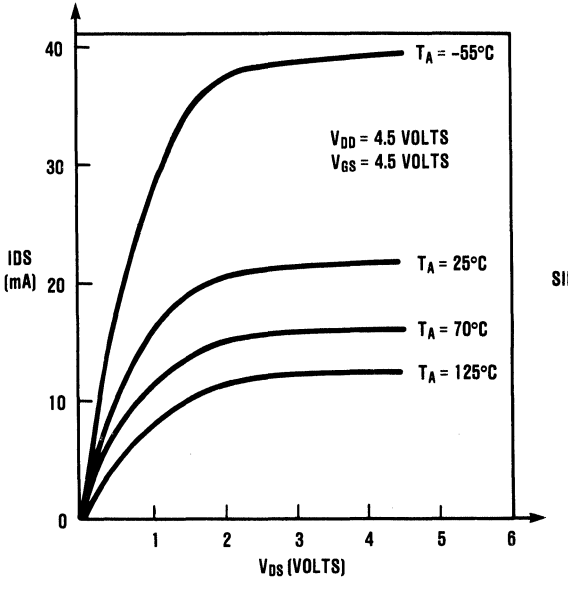
Symbol	Parameters	Conditions	Min.	Typ.	Max.
I_{DSS}	Output Leakage Current		−10 μA		+10μA
V_{OL}	Low Level Output Voltage	$I_{OL} = 4.0$ μA			.4V
V_{OH}	High Level Output Voltage	$I_{OH} = 5.0$ μA	2.4V		

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance



P-CHANNEL DRIVER
SOURCING CHARACTERISTICS



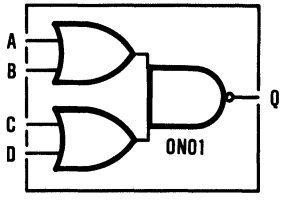
N-CHANNEL DRIVER
SINKING CHARACTERISTICS

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed OR-OR-NAND Gate

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
L	L	L	L	H
All Other				L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .ON01 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	5.5	6.7	7.9	9.1	14.0
		t_{PHL}	1.9	2.5	3.0	3.6	5.9

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
4.3	4.82
1.3	2.28

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

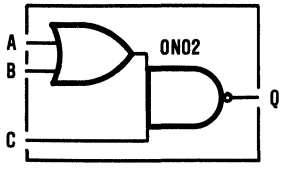
ON02

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed OR-NAND Gate

Logic Symbol



Truth Table

A	B	C	Q
X	X	L	H
H	X	H	L
X	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 1.5
Bolt Syntax: Q .ON02 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	4.0	5.2	6.4	7.7	12.6
		t_{PHL}	0.8	1.3	1.8	2.3	4.2

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
2.8	4.91
0.3	1.93

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

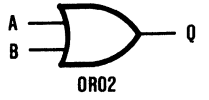
Unit Load = .25 pF including statistical wiring capacitance

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Two Input OR Gate

Logic Symbol



Truth Table

A	B	Q
L	L	L
H	X	H
X	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 1.5
Bolt Syntax: Q .OR02 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	1.5	2.3	3.0	3.7	6.5
		t_{PHL}	2.7	3.0	3.3	3.6	4.9

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
0.8	2.85
2.3	1.30

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

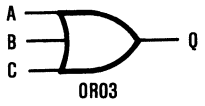
OR03

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Three Input OR Gate

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .OR03 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	1.7	2.4	3.1	3.8	6.7
		t_{PHL}	3.8	4.2	4.6	5.0	6.6

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
0.9	2.88
3.4	1.62

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

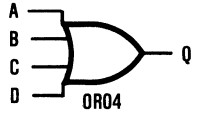
OR04

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Four Input OR Gate

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q .OR04 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.1	2.8	3.6	4.3	7.4
		t_{PHL}	7.5	8.0	8.6	9.1	11.2

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
1.4	2.88
7.0	2.10

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

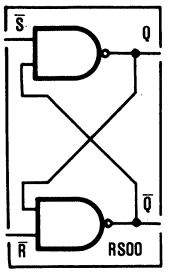
RS00

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Set-Reset NAND Gate Latch

Logic Symbol



Truth Table

SN	RN	Q	QN
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q QN .RS00 RN SN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.6	3.3	4.0	4.7	7.4
		t_{PHL}	2.8	3.0	3.2	3.4	4.3

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
2.0	2.72
2.6	0.82

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

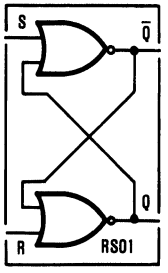
RS01

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Set-Reset NOR Gate Latch

Logic Symbol



Truth Table

S	R	Q	QN
H	H	L	L
H	L	H	L
L	H	L	H
L	L	No Change	

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2.5
Bolt Syntax: Q QN .RS01 R S;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

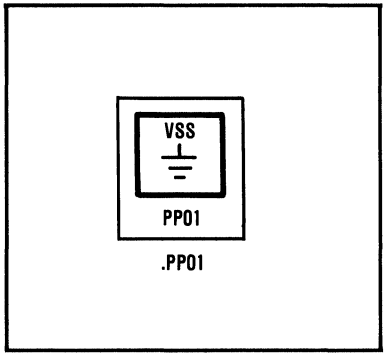
Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.4	4.6	5.8	7.1	12.0
		t_{PHL}	0.6	0.9	1.2	1.5	2.8

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
2.1	4.92
0.2	1.26

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

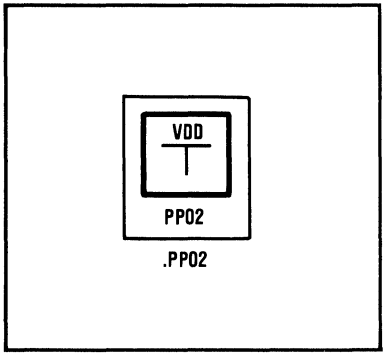
Unit Load = .25 pF including statistical wiring capacitance

3μ Single-Metal HCMOS Gate Arrays



NOTE: ONE PP01 MUST BE USED PER GROUND (V_{SS}) PIN.

3μ Single-Metal HCMOS Gate Arrays



NOTE: ONE PP02 MUST BE USED PER POWER (V_{DD}) PIN.

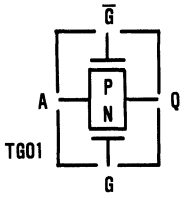
TG01

3μ Single-Metal HCMOS Gate Arrays

Description

Pre-Routed Transmission Gate

Logic Symbol



Truth Table

A	G	GN	Q
A	L	H	Z
A	H	L	A

Input Loading

Logic Input	Equivalent Unit Loads
A	2
G,GN	1

Equivalent Gate Count: 0.5
Bolt Syntax: Q .TG01 A G GN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	1.4	1.9	2.4	3.0	4.56
		t_{PHL}	0.9	1.3	1.7	2.1	3.74
G,GN	Q	t_{PLH}	3.8	5.2	6.6	8.1	13.78
		t_{PHL}	2.4	2.8	3.3	3.7	5.38

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
0.3	2.13
0.5	1.62
2.3	5.74
2.0	1.69

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

Unit Load = .25 pF including statistical wiring capacitance

Gate Array Datasheets

3μ Double-Metal HCMOS Gate Array

Selection Guide

3μ Double-Metal HCMOS Gate Array

Cell	Description
AA02	Pre-Routed Two Input AND Gate
AA03	Pre-Routed Three Input AND Gate
AA04	Pre-Routed Four Input AND Gate
AA05	Pre-Routed Five Input AND Gate
AN01	Pre-Routed AND-NOR Gate
AN02	Pre-Routed AND-NOR Gate
AN03	Pre-Routed AND-NOR Gate
AN04	Pre-Routed AND-NOR-NOR Gate
AN05	Pre-Routed Four 3-In AND's Into A 4-In NOR
AN06	Pre-Routed Three 3-In AND's Into A 3-In NOR
AO01	Pre-Routed AND-OR Gate
DF01	Pre-Routed D Flip-Flop
DF02	Pre-Routed D Flip-Flop With Asynchronous Active Low Set
DF03	Pre-Routed D Flip-Flop With Asynchronous Active Low Reset
DF04	Pre-Routed D Flip-Flop With Asynchronous Active Low Set And Active Low Reset
DF05	Pre-Routed D Flip-Flop With Asynchronous Set
DF06	Pre-Routed D Flip-Flop With Asynchronous Reset
DF07	Pre-Routed D Flip-Flop With Asynchronous Set And Reset
DF08	Pre-Routed D Flip-Flop With Single Clock
DF09	Pre-Routed D Flip-Flop With Asynchronous Active Low Set And Single Clock
DF0A	Pre-Routed D Flip-Flop With Asynchronous Active Low Reset And Single Clock
DF0B	Pre-Routed D Flip-Flop With Asynchronous Active Low Set, Active Low Reset, And Single Clock
DF0C	Pre-Routed D Flip-Flop With Asynchronous Set And Single Clock
DF0D	Pre-Routed D Flip-Flop With Asynchronous Reset and Single Clock
DF0E	Pre-Routed D Flip-Flop With Asynchronous Set, Reset, And Single Clock
DL01	Pre-Routed Latch With Q And QN
DL18	Pre-Routed Latch With Set And Reset
DL19	Pre-Routed Latch With Set
DL1A	Pre-Routed Latch With Reset
DL1B	Pre-Routed Latch With Active Low Set
DL1C	Pre-Routed Latch With Active Low Reset
DL1D	Pre-Routed Latch With Active Low Set and Reset
EN01	Pre-Routed Exclusive NOR Gate
EO01	Pre-Routed Exclusive OR Gate
IB01	Pre-Routed CMOS Non-Inverting Input Buffer
IB02	Pre-Routed CMOS Inverting Input Buffer
IB04	Pre-Routed CMOS Inverting Input Buffer
IB06	Pre-Routed CMOS Inverting Input Buffer With Pull Down
IB07	Pre-Routed TTL Non-Inverting Input Buffer
IB08	Pre-Routed TTL Inverting Input Buffer
IB0A	Pre-Routed TTL Inverting Input Buffer With Pull Up
IB0C	Pre-Routed TTL Inverting Input Buffer With Pull Down
II11	Pre-Routed Clock Driver With A Single Inverter Followed By A Single Inverter
II12	Pre-Routed Clock Driver With A Single Inverter Followed By A Single Inverter
II13	Pre-Routed Clock Driver With A Single Inverter Followed By Three Inverters In Parallel
II21	Pre-Routed Clock Driver With Two Inverters In Parallel Followed By A Single Inverter
II22	Pre-Routed Clock Driver With Two Inverters In Parallel Followed By Two Inverters In Parallel
II31	Pre-Routed Clock Driver With Three Inverters In Parallel Followed By A Single Inverter

3μ Double-Metal HCMOS Gate Array (Continued)

Cell	Description
IN01	Single Pre-Routed Inverter
IN02	Two Pre-Routed Inverters In Parallel
IN03	Three Pre-Routed Inverters In Parallel
IN04	Four Pre-Routed Inverters In Parallel
IN05	Five Pre-Routed Inverters In Parallel
IN06	Six Pre-Routed Inverters In Parallel
IO01	TTL Non-Inverting Bi-Directional Input/ Output Buffer With Positive Enable
IO03	CMOS Non-Inverting Bi-Directional Input/Output Buffer With Positive Enable
IO04	CMOS Inverting Bi-Directional Input/Output Buffer With Positive Enable
IT01	Non-Inverting Internal Tri-State Buffer
IT02	Pre-Routed Inverter Driving A Transmission Gate
ITOF	Inverting Internal Tri-State Buffer
MU23	Pre-Routed Two-To-One Multiplexer
NA02	Pre-Routed Two Input NAND Gate
NA03	Pre-Routed Three Input NAND Gate
NA04	Pre-Routed Four Input NAND Gate
NA05	Pre-Routed Five Input NAND Gate
NA06	Pre-Routed Six Input NAND Gate
NO02	Pre-Routed Two Input NOR Gate
NO03	Pre-Routed Three Input NOR Gate
NO04	Pre-Routed Four Input NOR Gate
NO05	Pre-Routed Five Input NOR Gate
NO06	Pre-Routed Six Input NOR Gate
OB01	TTL Output Buffer
OB02	TTL Inverting Output Buffer
OB03	CMOS Output Buffer
OB04	CMOS Inverting Output Buffer
OB05	Open Drain Output Buffer
OB06	Inverting Open Drain Output Buffer
OB07	Open Drain Output Buffer
OB08	Inverting Open Drain Output Buffer
OB09	CMOS Tri-State Non-Inverting Output Buffer With Negative Enable
OB0A	CMOS Tri-State Inverting Output Buffer With Positive Enable
ON01	Pre-Routed OR-NAND Gate
ON02	Pre-Routed OR-NAND Gate
ON03	Pre-Routed OR-NAND Gate
ON04	Pre-Routed OR-NAND-NAND Gate
OR02	Pre-Routed Two Input OR Gate
OR03	Pre-Routed Three Input OR Gate
OR04	Pre-Routed Four Input OR Gate
OR05	Pre-Routed Five Input OR Gate
PP01	V_{SS} Ground Pin
PP02	V_{DD} Power Pin
SR00	Pre-Routed Set-Reset NAND Gate Latch
SR01	Pre-Routed Set-Reset OR Gate Latch

3μ HCMOS Double-Metal Gate Array

The Gould AMI 3μ Double Metal Gate Array Macro Library is a collection of high performance digital integrated circuit building blocks. It is intended for use by logic, circuit, and MOS IC designers. Thus, anyone familiar with standard logic design methods can successfully design a gate array using these macros.

The 3μ Double Metal Macro Cells are implemented with a P-well, CMOS process. They are intended primarly for 5 volt (+ 10%) operation but will operate at voltages as low as 2.5 volts with reduced performance. Below is a description of the data and terms used in the data sheets.

- **PRE-ROUTED MACROS** are the simpler functional blocks such as the basic gates, latches, and flip-flops. Since these macros have a pre-defined layout they can be accurately characterized for propagation delays.

- **SOFTWARE MACROS** are macros which incorporate several pre-routed macros to form more complicated functional blocks such as counters or shift registers. These macros are not pre-defined with respect to layout, so the automatic placement and routing software maintains optimum layout flexibility. Since layout is not pre-defined, estimates of propagation delays through these macros are arrived at by adding the delays of the individual pre-routed macros used in the software macros.

- **THE CELL NAME** for each functional macro is displayed in the upper right hand corner of each data sheet. This is the same name that appears in the Bolt invocation.

- **THE LOGIC SYMBOL** for each macro is displayed as it appears in the gate array library.

- **A TRUTH TABLE** description of the logical functions for the cells is provided.

- **THE TABLE OF INPUT LOADING** gives the number of equivalent unit loads for each logical input of the pre-routed macros.

- **THE EQUIVALENT GATE COUNT** is the number of equivalent two input NAND gates in each cell.

- **BOLT SYNTAX** is the invocation syntax of each macro cell. Notice these statements always end with a semi-colon, and the order of these inputs and outputs must be maintained.

- **THE SWITCHING CHARACTERISTICS** give the propagation delay as a function of unit load. The unit load is the capacitance associated with a gate pair (i.e., the gate capacitance of an N-channel and a P-channel core transistor), plus an associated metal interconnection capacitance. All data is given for typical process, temperature, and power supply conditions. Both low-to-high transitions are shown. To find delays under other operating conditions derating curves must be used.

- **THE PROPAGATION DELAY EQUATION** is used for calculating propagation delays when the load is different from those explicitly given in the table. The intrinsic propagation delay, t_{dx}, is used when there is no output loading, and K, is a capacitive multiplication factor. As an example consider the two input NAND Gate with a fan-out of 5. To calculate the propagation delay for the high-to-low transition use t_{dx} = 0.6 and K = .44 so,

$$t_{PHL} = 0.6 + (.44)(5) = 2.8\text{ns}.$$

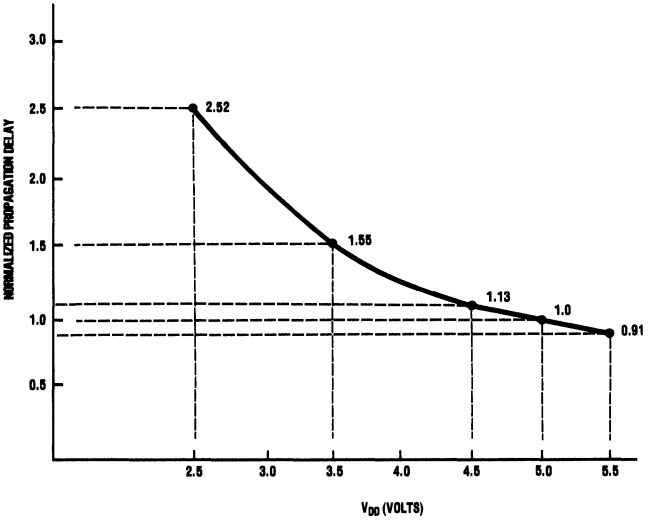
- **A LOGIC SCHEMATIC** is shown for the more complicated prerouted macros and the software macros not shown.

- **POWER SUPPLY MACROS** (PP01, PP02) must be shown on each circuit. While no connections to these macros are necessary, one macro must be shown per power or ground pin.

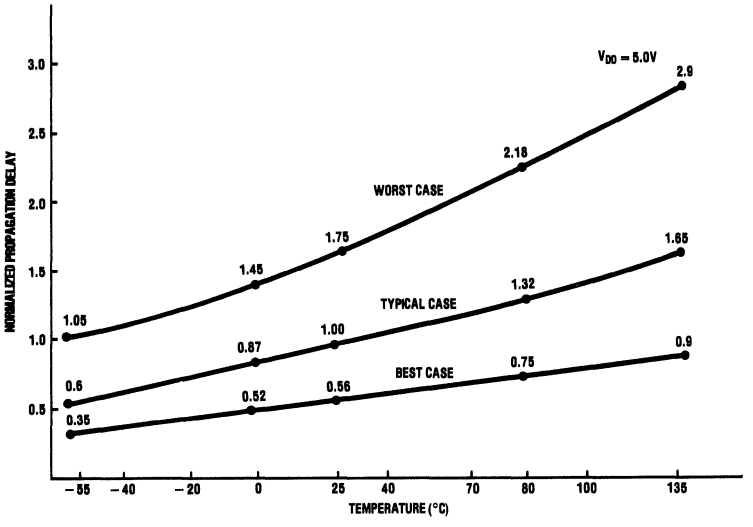
- **DERATING CURVES** are provided to account for changes in propagation delay as process, temperature and power supply vary.

Derating Curves

Normalized Delays vs. Power Supply Voltage



Normalized Delays vs. Process Model and Temperature



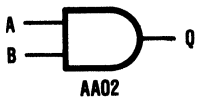
AA02

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Two Input AND Gate

Logic Symbol



Truth Table

A	B	Q
L	X	L
X	L	L
H	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .AA02 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.2	2.7	3.2	3.7	5.8
		t_{PHL}	2.2	2.5	2.8	3.1	4.3

Intrinsic Parameters t_{dx}	K
1.70	0.52
1.90	0.30

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

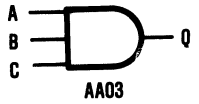
AA03

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Three Input AND Gate

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .AA03 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.3	3.8	4.4	4.9	7.1
		t_{PHL}	2.8	3.1	3.5	3.8	5.1

Intrinsic Parameters t_{dx}	K
2.80	0.55
2.50	0.31

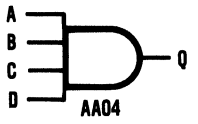
Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Four Input AND Gate

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 3
Bolt Syntax: Q .AA04 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	4.2	4.8	5.3	5.9	8.2
		t_{PHL}	3.1	3.4	3.7	4.1	5.4

Intrinsic Parameters t_{dx}	K
3.60	0.57
2.70	0.34

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

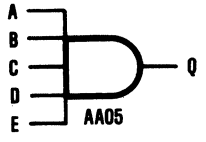
AA05

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Five Input AND Gate

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	L
X	L	X	X	X	L
X	X	L	X	X	L
X	X	X	L	X	L
X	X	X	X	L	L
H	H	H	H	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 3
Bolt Syntax: Q .AA05 A B C D E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	5.8	6.4	7.0	7.7	10.1
		t_{PHL}	3.4	3.8	4.1	4.5	6.0

Intrinsic Parameters t_{dx}	K
5.20	0.62
3.00	0.38

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

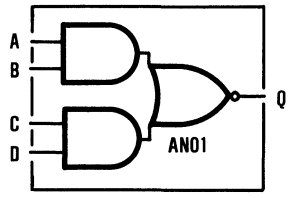
AN01

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed AND-NOR Gate

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .AN01 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	5.3	6.3	7.3	8.2	12.2
		t_{PHL}	2.1	2.5	2.9	3.4	5.1

Intrinsic Parameters t_{dx}	K
4.30	0.98
1.60	0.42

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

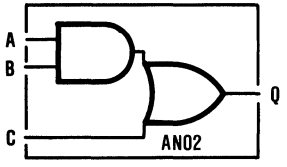
AN02

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed AND-NOR Gate

Logic Symbol



Truth Table

A	B	C	Q
L	X	L	H
X	L	L	H
H	H	X	L
X	X	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .AN02 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.9	4.8	5.7	6.7	10.5
		t_{PHL}	1.6	2.1	2.5	3.0	4.8

Intrinsic Parameters t_{dx}	K
2.90	0.95
1.10	0.46

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

Unit Load = .21 pF including statistical wiring capacitance

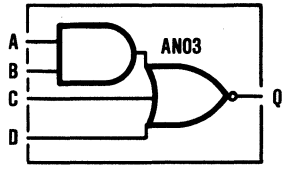
AN03

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed AND-NOR Gate

Logic Symbol



Truth Table

A	B	C	D	Q
X	X	X	H	L
X	X	H	X	L
H	H	X	X	L
X	L	L	L	H
L	X	L	L	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .AN03 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	6.4	7.8	9.2	10.6	16.3
		t_{PHL}	1.8	2.3	2.7	3.1	4.9

Intrinsic Parameters t_{dx}	K
5.00	1.41
1.40	0.43

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

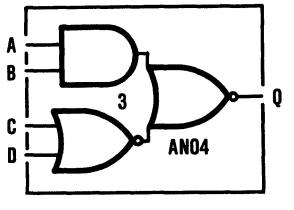
AN04

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed 2 in AND, 2 in NOR into 2 in NOR

Logic Symbol



Truth Table

A	B	C	D	Q
X	X	L	L	L
L	L	X	H	H
L	L	H	X	H
L	H	X	H	H
L	H	H	X	H
H	L	X	H	H
H	L	H	X	H
H	H	X	H	L
H	H	H	X	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 3
Bolt Syntax: Q .AN04 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.6	4.6	5.6	6.7	10.8
		t_{PHL}	3.0	3.3	3.6	3.9	5.2

Intrinsic Parameters t_{dx}	K
2.60	1.02
2.60	0.33

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

GOULD

AMI Semiconductors

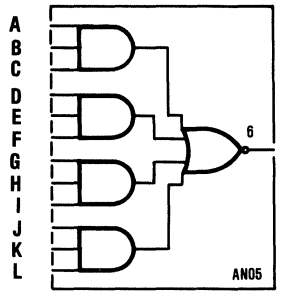
AN05

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Four 3-in ANDs, Into a 4-in NOR

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	J	K	L	Q
L	X	X	L	X	X	L	X	X	L	X	X	H
X	L	X	X	L	X	X	L	X	X	L	X	H
X	X	L	X	X	L	X	X	L	X	X	L	H
H	H	H	X	X	X	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	X	X	X	H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 6
Bolt Syntax: Q .AN05 A B C D E F G H I J K L;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	26.6	28.7	30.8	32.9	41.2
		t_{PHL}	6.6	7.3	7.9	8.6	11.3

Intrinsic Parameters t_{dx}	K
24.5	2.09
5.9	0.67

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

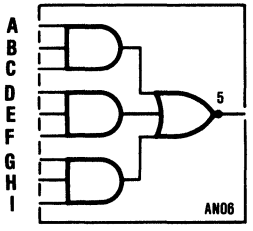
AN06

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Three 3-in ANDs, Into a 3-in NOR

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
L	X	X	L	X	X	L	X	X	H
X	L	X	X	L	X	X	L	X	H
X	X	L	X	X	L	X	X	L	H
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 5
Bolt Syntax: Q .AN06 A B C D E F G H I;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	16.0	17.5	19.1	20.7	27.1
		t_{PHL}	5.3	6.0	6.7	7.4	10.1

Intrinsic Parameters t_{dx}	K
14.4	1.59
4.7	0.68

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

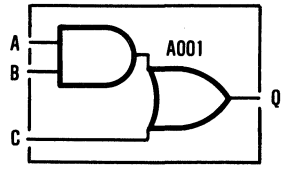
AO01

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed AND-OR Gate

Logic Symbol



Truth Table

A	B	C	Q
X	X	H	H
L	X	L	L
X	L	L	L
H	H	X	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .AO01 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.7	3.3	3.8	4.3	6.5
		t_{PHL}	4.1	4.5	4.9	5.3	6.9

Intrinsic Parameters t_{dx}	K
2.20	0.55
3.70	0.40

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

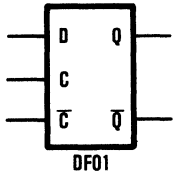
DF01

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop

Logic Symbol



Truth Table

C	CN	D	Q	QN
L	H	X	No Change	
↑	↓	L	L	H
↑	↓	H	H	L

Input Loading

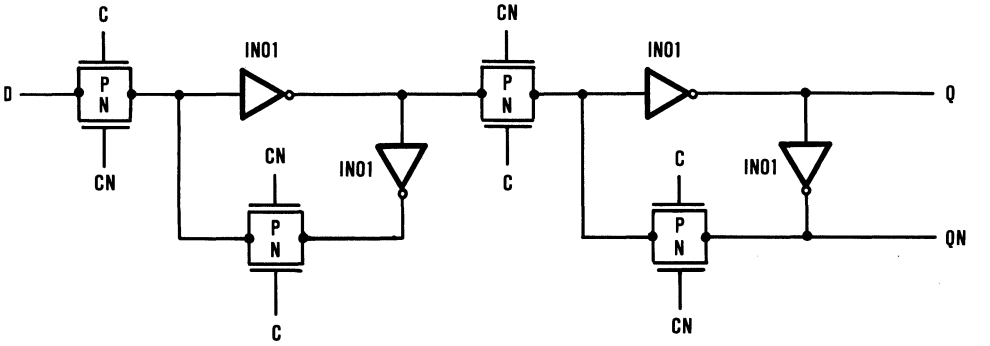
Logic Input	Equivalent Unit Loads
D	3
All Other	2

Equivalent Gate Count: 4
Bolt Syntax: Q QN .DF01 D C CN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	2.8	3.3	3.9	4.4	6.6
		t_{PHL}	2.3	2.7	3.0	3.4	4.9
C	QN	t_{PLH}	3.7	4.3	4.8	5.3	7.5
		t_{PHL}	3.0	3.3	3.6	3.8	4.9
Set-Up		t_{SU}	2.7				

Intrinsic Parameters t_{dx}	K
2.20	0.55
1.90	0.38
3.20	0.55
2.80	0.27

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


C
D
P
N
CN
IN01
CN
P
N
C
IN01
CN
P
N
C
IN01
C
P
N
CN
IN01
Q
QN

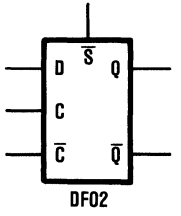
DF02

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Active Low Set

Logic Symbol



DF02

Truth Table

SN	C	CN	D	Q	QN
H	L	H	X	No Change	
H	↑	↓	L	L	H
H	↑	↓	H	H	L
L	X	X	X	H	L

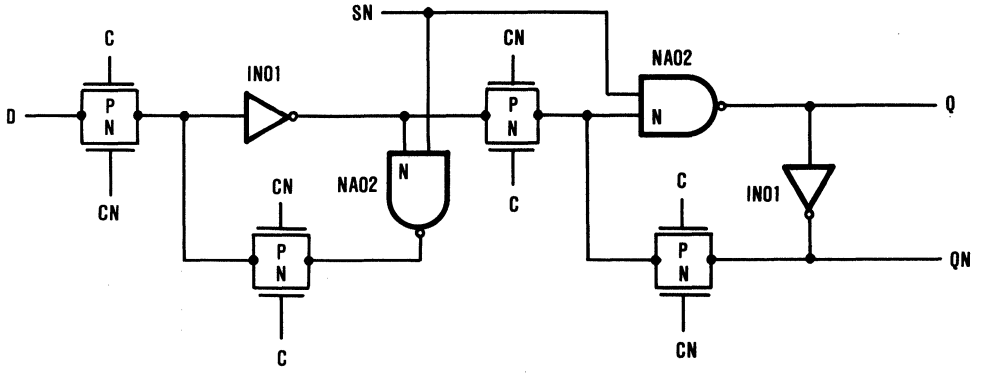
Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	2

Equivalent Gate Count: 5
Bolt Syntax: Q QN .DF02 D C CN SN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8	Intrinsic Parameters t_{dx}	K
C	Q	t_{PLH}	2.9	3.5	4.1	4.6	6.9	2.30	0.58
		t_{PHL}	3.0	3.5	4.1	4.6	6.6	2.50	0.51
C	QN	t_{PLH}	4.4	5.0	5.5	6.1	8.3	3.90	0.56
		t_{PHL}	3.2	3.5	3.8	4.1	5.2	2.90	0.29
SN	Q	t_{PLH}	2.3	2.9	3.4	4.0	6.3	1.70	0.57
SN	QN	t_{PHL}	2.6	2.9	3.2	3.5	4.7	2.30	0.30
Set-Up		t_{SU}			3.3				

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

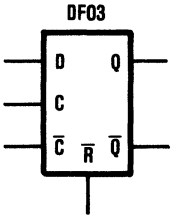

SN
C
CN
NA02
INO1
D
P
N
Q
CN
NA02
N
C
INO1
CN
C
QN
C
CN

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Active Low Reset

Logic Symbol



Truth Table

RN	C	CN	D	Q	QN
H	L	H	X	No Change	
H	↑	↓	L	L	H
H	↑	↓	H	H	L
L	X	X	X	L	H

Input Loading

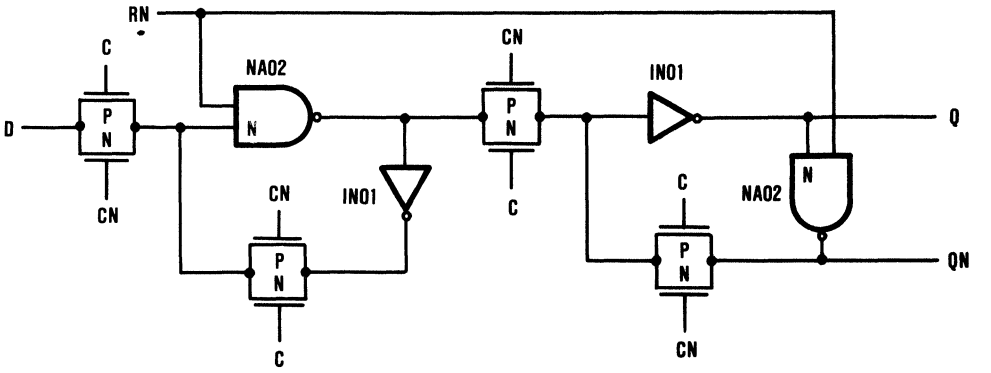
Logic Input	Equivalent Unit Loads
D	3
All Other	2

Equivalent Gate Count: 5
Bolt Syntax: Q QN .DF03 D C CN RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	3.0	3.6	4.2	4.8	7.1
		t_{PHL}	2.4	2.7	3.1	3.4	4.8
C	QN	t_{PLH}	3.8	4.4	5.0	5.5	7.8
		t_{PHL}	3.9	4.3	4.8	5.2	7.1
RN	QN	t_{PLH}	3.4	4.0	4.5	5.0	7.2
RN	Q	t_{PHL}	4.1	4.4	4.8	5.2	6.7
Set-Up		t_{SU}			3.1		

Intrinsic Parameters t_{dx}	K
2.40	0.60
2.00	0.35
3.20	0.57
3.40	0.46
2.90	0.55
3.70	0.38

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


RN
C
D
P
N
CN
NA02
N
CN
P
N
C
IN01
CN
P
N
C
IN01
C
P
N
CN
NA02
N
Q
QN

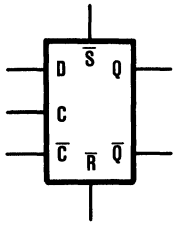
3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Active Low Set And Active Low Reset

Logic Symbol

DF04



Truth Table

SN	RN	C	CN	D	Q	QN
H	H	L	H	X	No Change	
H	H	↑	↓	L	L	H
H	H	↑	↓	H	H	L
H	L	X	X	X	L	H
L	H	X	X	X	H	L
L	L	X	X	X	Illegal	

Input Loading

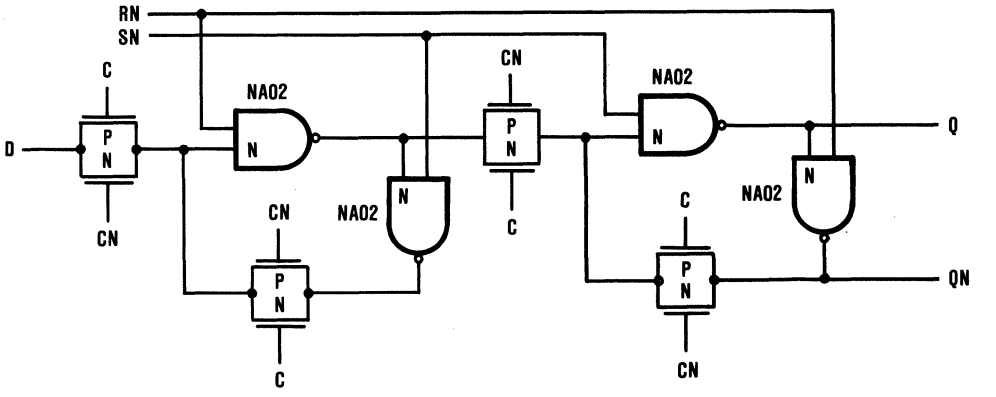
Logic Input	Equivalent Unit Loads
D	3
All Other	2

Equivalent Gate Count: 6
Bolt Syntax: Q QN .DF04 D C CN SN RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	3.1	3.7	4.3	4.9	7.3
		t_{PHL}	3.0	3.5	4.0	4.6	6.7
C	QN	t_{PLH}	4.4	5.0	5.5	6.1	8.2
		t_{PHL}	4.0	4.5	4.9	5.4	7.3
SN	Q	t_{PLH}	2.3	2.8	3.4	4.0	6.3
SN	QN	t_{PHL}	3.2	3.7	4.1	4.6	6.4
RN	QN	t_{PLH}	2.4	3.0	3.5	4.1	6.2
RN	Q	t_{PHL}	5.1	5.6	6.2	6.7	8.9
Set-Up		t_{SU}			3.3		

Intrinsic Parameters t_{dx}	K
2.50	0.60
2.50	0.52
3.90	0.55
3.50	0.46
1.70	0.57
2.70	0.46
1.90	0.55
4.50	0.78

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

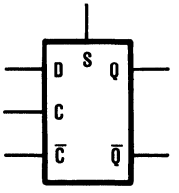

RN
SN
C
D
P
N
CN
NA02
N
CN
NA02
N
P
N
C
CN
NA02
N
C
P
N
CN
Q
QN

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Set

Logic Symbol



DF05

Truth Table

S	C	CN	D	Q	QN
L	L	H	X	No Change	
L	↑	↓	L	L	H
L	↑	↓	H	H	L
H	X	X	X	H	L

Input Loading

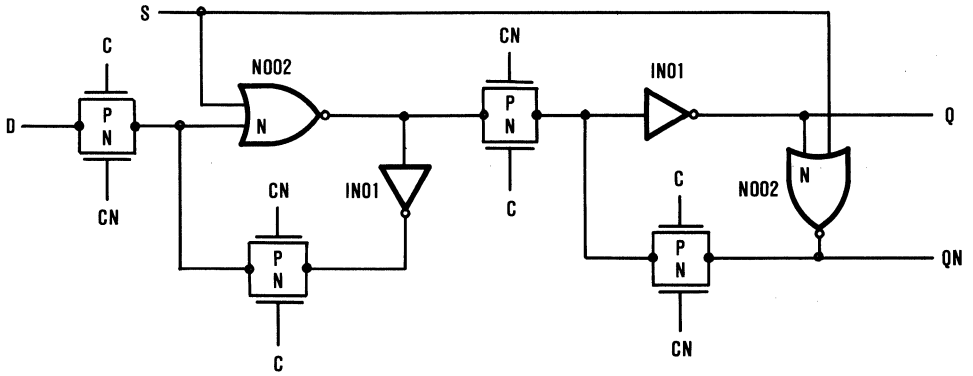
Logic Input	Equivalent Unit Loads
D	3
All Other	2

Equivalent Gate Count: 5
Bolt Syntax: Q QN .DF05 D C CN S;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	2.9	3.5	4.0	4.6	6.8
		t_{PHL}	2.7	3.1	3.5	4.0	5.7
C	QN	t_{PLH}	5.6	6.6	7.6	8.6	12.6
		t_{PHL}	3.2	3.5	3.8	4.1	5.2
S	Q	t_{PLH}	3.7	4.3	4.9	5.5	7.9
S	QN	t_{PHL}	1.1	1.4	1.7	2.0	3.3
Set-Up		t_{SU}			4.0		

Intrinsic Parameters t_{dx}	K
2.40	0.56
2.30	0.42
4.60	1.01
2.90	0.28
3.10	0.60
0.80	0.31

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


S
C
D
P
N
CN
NOO2
N
CN
P
N
C
INO1
CN
P
N
C
INO1
Q
C
P
N
CN
NOO2
N
QN

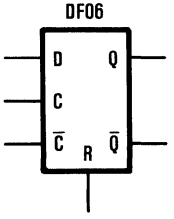
DF06

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Reset

Logic Symbol



Truth Table

R	C	CN	D	Q	QN
L	L	H	X	No Change	
L	↑	↓	L	L	H
L	↑	↓	H	H	L
H	X	X	X	L	H

Input Loading

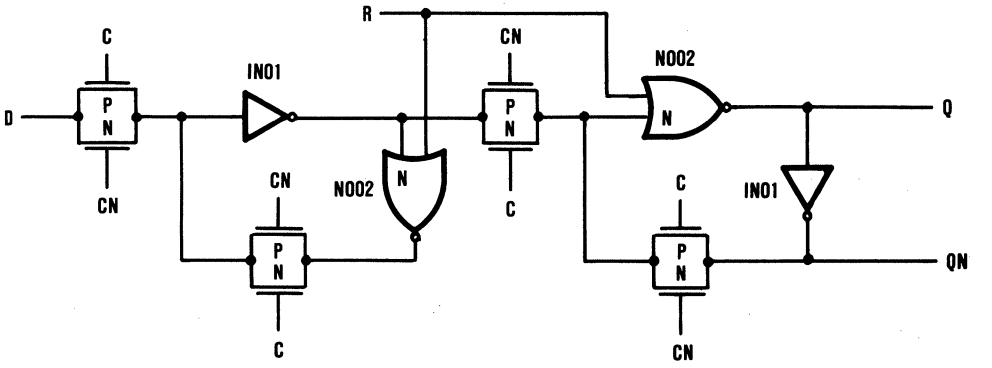
Logic Input	Equivalent Unit Loads
D	3
All Other	2

Equivalent Gate Count: 5
Bolt Syntax: Q QN .DF06 D C CN R;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	4.2	5.2	6.2	7.3	11.4
		t_{PHL}	2.4	2.7	3.1	3.4	4.8
C	QN	t_{PLH}	3.8	4.4	5.0	5.5	7.8
		t_{PHL}	3.9	4.2	4.5	4.9	6.2
R	QN	t_{PLH}	3.6	4.2	4.7	5.3	7.6
R	Q	t_{PHL}	0.9	1.2	1.6	1.9	3.4
Set-Up		t_{SU}			3.5		

Intrinsic Parameters t_{dx}	K
3.10	1.03
2.00	0.34
3.20	0.57
3.60	0.32
3.00	0.34
0.50	0.57

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


R
C
CN
NO02
IN01
D
P
N
Q
CN
NO02
N
C
IN01
CN
C
QN
C
CN

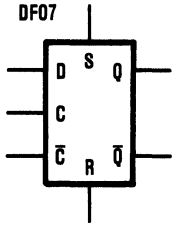
DF07

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Set And Reset

Logic Symbol



Truth Table

S	R	C	CN	D	Q	QN
L	L	L	H	X	No Change	
L	L	↑	↓	L	L	H
L	L	↑	↓	H	H	L
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	X	X	X	Illegal	

Input Loading

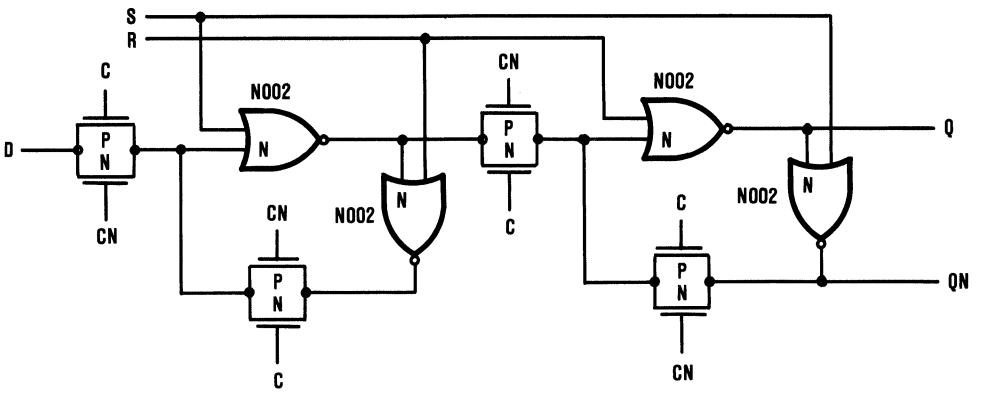
Logic Input	Equivalent Unit Loads
D	3
All Other	2

Equivalent Gate Count: 6
Bolt Syntax: Q QN .DF07 D C CN S R;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	4.2	5.3	6.3	7.3	11.5
		t_{PHL}	2.6	3.1	3.5	3.9	5.7
C	QN	t_{PLH}	5.6	6.6	7.6	8.6	12.6
		t_{PHL}	4.0	4.3	4.6	4.9	6.2
R	QN	t_{PLH}	4.0	5.0	6.0	7.0	11.0
R	Q	t_{PHL}	0.9	1.3	1.6	1.9	3.2
S	Q	t_{PLH}	4.8	5.8	6.8	7.8	11.8
S	QN	t_{PHL}	1.1	1.4	1.7	2.0	3.3
Set-Up		t_{SU}			4.0		

Intrinsic Parameters t_{dx}	K
3.20	1.04
2.20	0.42
4.60	1.01
3.70	0.32
3.00	1.01
0.60	0.31
3.80	0.99
0.80	0.31

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


S
R
C
D
P
N
CN
NOO2
N
CN
NOO2
N
P
N
C
CN
NOO2
N
C
P
N
CN
NOO2
N
Q
QN

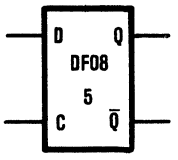
DF08

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Single Clock

Logic Symbol



Truth Table

C	D	Q	QN
L	X	No Change	
↑	L	L	H
↑	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
D	3
C	1

Equivalent Gate Count: 5
Bolt Syntax: Q QN .DF08 D C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	6.5	7.0	7.6	8.1	10.3
		t_{PHL}	6.0	6.4	6.7	7.1	8.6
C	QN	t_{PLH}	7.5	8.0	8.6	9.1	11.3
		t_{PHL}	5.8	6.0	6.3	6.6	7.7
Set-Up		t_{SU}			2.7		

Intrinsic Parameters t_{dx}	K
5.90	0.55
5.60	0.38
6.90	0.55
5.50	0.27

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

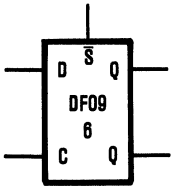
DF09

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Active Low Set And Single Clock

Logic Symbol



Truth Table

SN	C	D	Q	QN
H	L	X	No Change	
H	↑	L	L	H
H	↑	H	H	L
L	X	X	H	L

Input Loading

Logic Input	Equivalent Unit Loads
D	3
SN	2
C	1

Equivalent Gate Count: 6
Bolt Syntax: Q QN .DF09 D C SN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	5.6	6.2	6.7	7.3	9.6
		t_{PHL}	6.7	7.2	7.7	8.2	10.3
C	QN	t_{PLH}	8.2	8.7	9.3	9.8	12.1
		t_{PHL}	6.9	7.2	7.5	7.8	8.9
SN	Q	t_{PLH}	2.3	2.9	3.4	4.0	6.3
SN	QN	t_{PHL}	2.6	2.9	3.2	3.5	4.7
Set-Up		t_{SU}			3.3		

Intrinsic Parameters t_{dx}	K
5.00	0.58
6.20	0.51
7.60	0.56
6.60	0.29
1.70	0.57
2.30	0.30

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

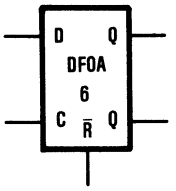
DF0A

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Active Low Reset And Single Clock

Logic Symbol



Truth Table

RN	C	D	Q	QN
H	L	X	No Change	
H	↑	L	L	H
H	↑	H	H	L
L	X	X	L	H

Input Loading

Logic Input	Equivalent Unit Loads
D	3
RN	2
C	1

Equivalent Gate Count: 6
Bolt Syntax: Q QN .DF0A D C RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	6.7	7.3	7.9	8.5	10.9
		t_{PHL}	6.1	6.4	6.8	7.1	8.5
C	QN	t_{PLH}	7.5	8.0	8.6	9.2	11.5
		t_{PHL}	7.6	8.0	8.5	8.9	10.8
RN	QN	t_{PLH}	3.4	4.0	4.5	5.0	7.2
RN	Q	t_{PHL}	4.1	4.4	4.8	5.2	6.7
Set-Up		t_{SU}	3.1				

Intrinsic Parameters t_{dx}	K
6.10	0.60
5.70	0.35
6.90	0.57
7.10	0.46
2.90	0.55
3.70	0.38

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

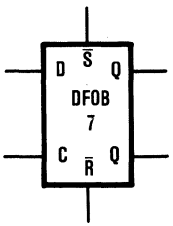
DF0B

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Active Low Set, Active Low Reset, And Single Clock

Logic Symbol



Truth Table

SN	RN	C	D	Q	QN
H	H	L	X	No Change	
H	H	↑	L	L	H
H	H	↑	H	H	L
H	L	X	X	L	H
L	H	X	X	H	L
L	L	X	X	Illegal	

Input Loading

Logic Input	Equivalent Unit Loads
D	3
SN, RN	2
C	1

Equivalent Gate Count: 7
Bolt Syntax: Q QN .DF0B D C SN RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	6.8	7.4	8.0	8.6	11.0
		t_{PHL}	6.7	7.2	7.8	8.3	10.4
C	QN	t_{PLH}	8.2	8.7	9.3	9.8	12.0
		t_{PHL}	7.7	8.1	8.6	9.0	10.9
SN	Q	t_{PLH}	2.3	2.8	3.4	4.0	6.3
SN	QN	t_{PHL}	3.2	3.7	4.1	4.6	6.4
RN	QN	t_{PLH}	2.4	3.0	3.5	4.1	6.2
RN	Q	t_{PHL}	5.1	5.6	6.2	6.7	8.8
Set-Up		t_{SU}			3.3		

Intrinsic Parameters t_{dx}	K
6.20	0.60
6.20	0.52
7.60	0.55
7.20	0.46
1.70	0.57
2.70	0.46
1.90	0.55
4.50	0.78

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

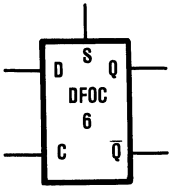
DF0C

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Set And Single Clock

Logic Symbol



Truth Table

S	C	D	Q	QN
L	L	X	No Change	
L	↑	L	L	H
L	↑	H	H	L
H	X	X	H	L

Input Loading

Logic Input	Equivalent Unit Loads
D	3
S	2
C	1

Equivalent Gate Count: 6
Bolt Syntax: Q QN .DF0C D C S;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	6.7	7.2	7.8	8.3	10.6
		t_{PHL}	6.4	6.8	7.3	7.7	9.4
C	QN	t_{PLH}	9.3	10.3	11.3	12.3	16.4
		t_{PHL}	6.9	7.2	7.4	7.7	8.8
S	Q	t_{PLH}	3.7	4.3	4.9	5.5	7.9
S	QN	t_{PHL}	1.1	1.4	1.7	2.0	3.3
Set-Up		t_{SU}			4.0		

Intrinsic Parameters t_{dx}	K
6.10	0.56
6.00	0.42
8.30	1.01
6.60	0.28
3.10	0.60
0.80	0.31

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

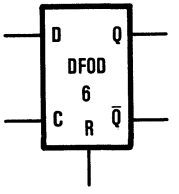
DF0D

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Reset And Single Clock

Logic Symbol



Truth Table

R	C	D	Q	QN
L	L	X	No Change	
L	↑	L	L	H
L	↑	H	H	L
H	X	X	L	H

Input Loading

Logic Input	Equivalent Unit Loads
D	3
R	2
C	1

Equivalent Gate Count: 6
Bolt Syntax: Q QN .DF0D D C R;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	7.8	8.9	9.9	10.9	15.0
		t_{PHL}	6.1	6.4	6.8	7.1	8.5
C	QN	t_{PLH}	7.5	8.0	8.6	9.2	11.5
		t_{PHL}	7.6	8.0	8.3	8.6	9.9
R	QN	t_{PLH}	3.6	4.2	4.7	5.3	7.6
R	Q	t_{PHL}	0.9	1.2	1.6	1.9	3.3
Set-Up		t_{SU}			3.5		

Intrinsic Parameters t_{dx}	K
6.80	1.03
5.70	0.35
6.90	0.57
7.30	0.33
3.00	0.57
0.50	0.35

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

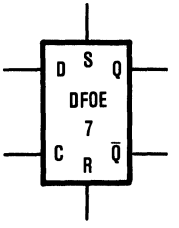
DF0E

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed D Flip Flop With Asynchronous Set, Reset and Single Clock

Logic Symbol



Truth Table

S	R	C	D	Q	QN
L	L	L	X	No Change	
L	L	↑	L	L	H
L	L	↑	H	H	L
L	H	X	X	L	H
H	L	X	X	H	L
H	H	X	X	Illegal	

Input Loading

Logic Input	Equivalent Unit Loads
D	3
S, R	2
C	1

Equivalent Gate Count: 7
Bolt Syntax: Q QN .DF0E D C S R;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
C	Q	t_{PLH}	7.9	9.0	10.0	11.1	15.2
		t_{PHL}	6.3	6.8	7.2	7.6	9.3
C	QN	t_{PLH}	9.3	10.3	11.3	12.3	16.3
		t_{PHL}	7.7	8.0	8.4	8.7	10.0
R	QN	t_{PLH}	4.0	5.0	6.0	7.0	11.0
R	Q	t_{PHL}	0.9	1.3	1.6	1.9	3.2
S	Q	t_{PLH}	4.8	5.8	6.8	7.8	11.8
S	QN	t_{PHL}	1.1	1.4	1.7	2.0	3.3
Set-Up		t_{SU}			4.0		

Intrinsic Parameters t_{dx}	K
6.90	1.04
5.90	0.43
8.30	1.00
7.40	0.32
3.00	1.00
0.60	0.32
3.80	1.00
0.80	0.[illegible]

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

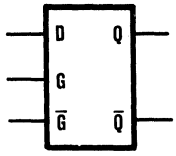
DL01

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Q and QN

Logic Symbol



DL01

Truth Table

G	GN	D	Q	QN
L	H	X	No Change	
H	L	D	D	DN

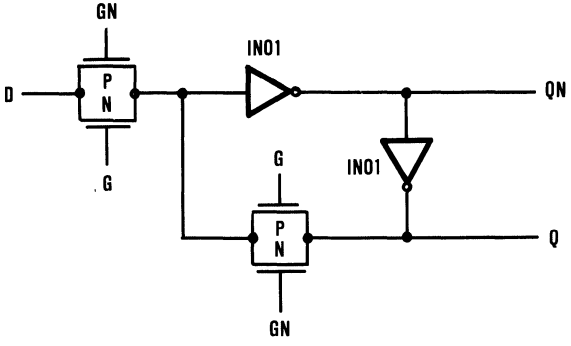
Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	1

Equivalent Gate Count: 2
Bolt Syntax: Q QN .DL01 D G GN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8	Intrinsic Parameters t_{dx}	K
G	Q	t_{PLH}	3.9	4.4	5.0	5.5	7.8	3.30	0.56
		t_{PHL}	3.2	3.5	3.8	4.0	5.2	2.90	0.28
G	QN	t_{PLH}	2.9	3.4	4.0	4.6	6.9	2.30	0.57
		t_{PHL}	2.4	2.8	3.1	3.5	4.9	2.10	0.35
D	Q	t_{PLH}	2.7	3.1	3.8	4.3	6.5	2.10	0.55
		t_{PHL}	2.6	2.9	3.2	3.4	4.6	2.30	0.28
D	QN	t_{PLH}	2.3	2.9	3.4	4.0	6.4	1.70	0.59
		t_{PHL}	1.2	1.6	2.0	2.3	3.8	0.90	0.36

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


GN
D
P
N
G
IN01
QN
G
IN01
P
N
Q
GN

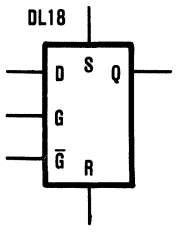
DL18

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Set And Reset

Logic Symbol



Truth Table

S	R	G	GN	D	Q
L	L	L	H	X	No Change
L	L	H	L	D	D
L	H	X	X	X	L
H	L	X	X	X	H
H	H	X	X	X	L

Input Loading

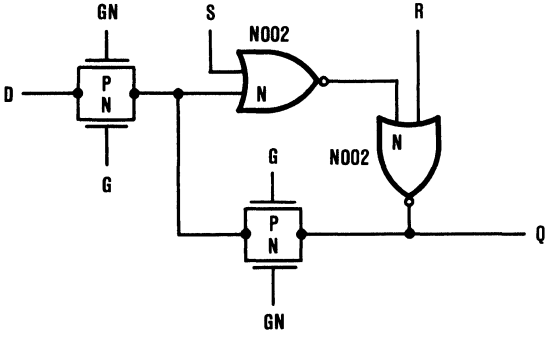
Logic Input	Equivalent Unit Loads
D	3
All Other	1

Equivalent Gate Count: 3
Bolt Syntax: Q .DL18 D G GN S R;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
G	Q	t_{PLH}	5.0	6.0	7.0	8.0	12.0
		t_{PHL}	3.8	4.1	4.5	4.8	6.1
D	Q	t_{PLH}	4.1	5.1	6.1	7.1	11.1
		t_{PHL}	3.3	3.6	3.9	4.2	5.9
S	Q	t_{PLH}	6.2	7.2	8.3	9.3	13.3
R	Q	t_{PHL}	1.5	1.8	2.1	2.4	3.6

Intrinsic Parameters t_{dx}	K
4.00	1.01
3.50	0.32
3.10	1.01
3.00	0.30
5.20	1.01
1.20	0.30

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

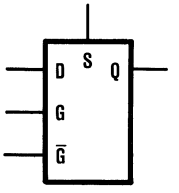

GN
S
NOO2
R
D
P
N
N
G
NOO2
N
G
P
N
Q
GN

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Set

Logic Symbol



DL19

Truth Table

S	G	GN	D	Q
L	L	H	X	No Change
L	H	L	D	D
H	X	X	X	H

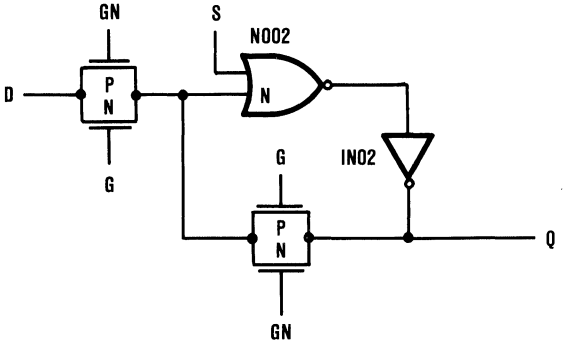
Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	1

Equivalent Gate Count: 3
Bolt Syntax: Q .DL19 D G GN S;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8	Intrinsic Parameters t_{dx}	K
G	Q	t_{PLH}	4.0	4.6	5.2	5.7	8.0	3.50	0.57
		t_{PHL}	4.1	4.4	4.8	5.1	6.4	3.80	0.32
D	Q	t_{PLH}	2.6	3.2	3.7	4.3	6.4	2.10	0.55
		t_{PHL}	3.4	3.7	4.0	4.3	5.5	3.10	0.30
S	Q	t_{PLH}	3.7	4.2	4.8	5.4	7.7	3.10	0.57

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


GN
S
NOO2
D
P
N
N
G
G
INO2
P
N
Q
GN

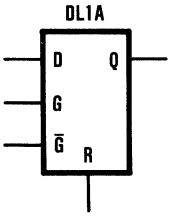
DL1A

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Reset

Logic Symbol



Truth Table

R	G	GN	D	Q
L	L	H	X	No Change
L	H	L	D	D
H	X	X	X	L

Input Loading

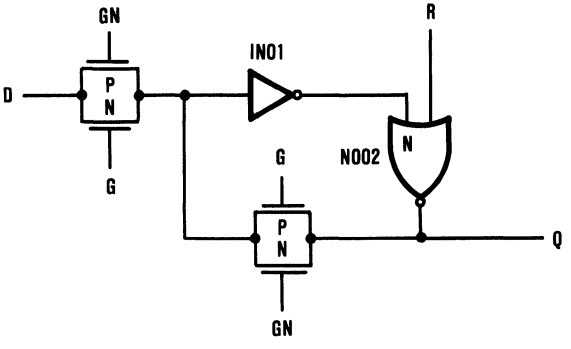
Logic Input	Equivalent Unit Loads
D	3
All Other	1

Equivalent Gate Count: 3
Bolt Syntax: Q .DL1A D G GN R;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
G	Q	t_{PLH}	5.5	6.5	7.5	8.4	12.4
		t_{PHL}	3.2	3.5	3.8	4.1	5.3
D	Q	t_{PLH}	4.2	5.2	6.2	7.3	11.3
		t_{PHL}	2.6	2.9	3.2	3.4	4.5
R	Q	t_{PLH}	1.7	2.0	2.3	2.6	3.8

Intrinsic Parameters t_{dx}	K
4.50	0.99
2.90	1.30
3.20	1.02
2.40	0.26
1.40	0.30

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


GN
D
P
N
G
IN01
R
N002
N
G
P
N
Q
GN

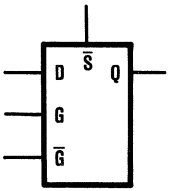
DL1B

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Active Low Set

Logic Symbol



Truth Table

SN	G	GN	D	Q
H	L	H	X	No Change
H	H	L	D	D
L	X	X	X	H

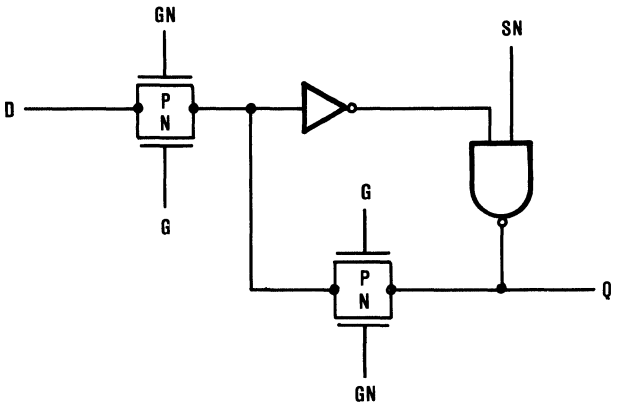
Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	1

Equivalent Gate Count: 3
Bolt Syntax: Q .DL1B D G GN SN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8	Intrinsic Parameters t_{dx}	K
G	Q	t_{PLH}	4.1	4.7	5.2	5.7	7.9	3.60	0.55
		t_{PHL}	3.9	4.4	4.9	5.4	7.4	3.40	0.49
D	Q	t_{PLH}	2.7	3.3	3.8	4.3	6.5	2.20	0.55
		t_{PHL}	3.2	3.7	4.2	4.6	6.5	2.80	0.47
SN	Q	t_{PLH}	3.6	4.2	4.7	5.2	7.3	3.10	0.52

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


GN
SN
D
P
N
G
G
P
N
Q
GN

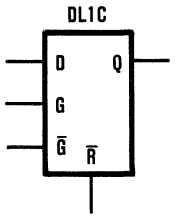
DL1C

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Active Low Reset

Logic Symbol



Truth Table

RN	G	GN	D	Q
H	L	H	X	No Change
H	H	L	D	D
L	X	X	X	L

Input Loading

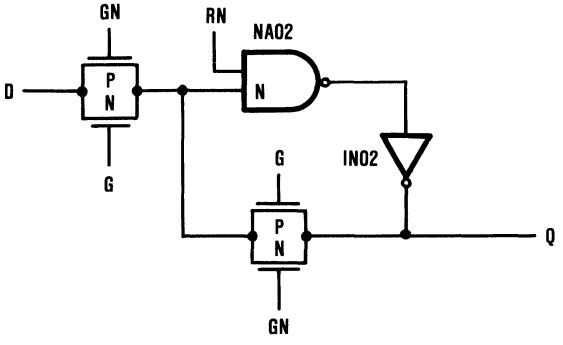
Logic Input	Equivalent Unit Loads
D	3
All Other	1

Equivalent Gate Count: 3
Bolt Syntax: Q .DL1C D G GN RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
G	Q	t_{PLH}	4.4	5.0	5.5	6.1	8.3
		t_{PHL}	3.3	3.5	3.8	4.1	5.2
D	Q	t_{PLH}	3.2	3.8	4.3	4.9	7.1
		t_{PHL}	2.6	2.9	3.2	3.5	4.6
RN	Q	t_{PHL}	3.1	3.4	3.7	4.0	5.1

Intrinsic Parameters t_{dx}	K
3.90	0.56
3.00	0.27
2.70	0.56
2.30	0.27
2.80	0.21

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


GN
RN
NA02
D
P
N
N
G
G
IN02
P
N
Q
GN

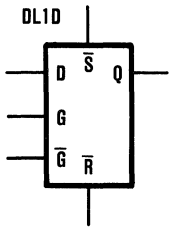
DL1D

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Latch With Active Low Set And Reset

Logic Symbol



Truth Table

SN	RN	G	GN	D	Q
H	H	L	H	X	No Change
H	H	H	L	D	D
H	L	X	X	X	L
L	H	X	X	X	H
L	L	X	X	X	H

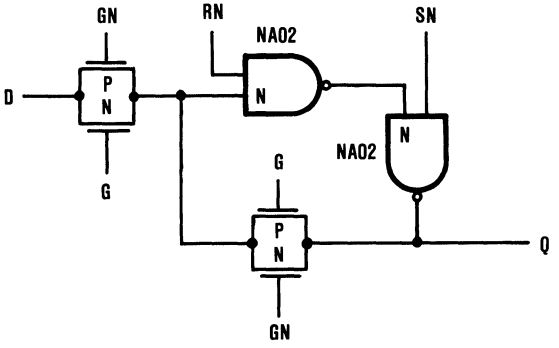
Input Loading

Logic Input	Equivalent Unit Loads
D	3
All Other	1

Equivalent Gate Count: 3
Bolt Syntax: Q .DL1D D G GN SN RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8	Intrinsic Parameters t_{dx}	K
G	Q	t_{PLH}	5.0	5.5	6.0	6.6	8.8	4.40	0.55
		t_{PHL}	4.1	4.6	5.0	5.5	7.3	3.60	0.46
D	Q	t_{PLH}	3.6	4.1	4.7	5.2	7.4	3.00	0.55
		t_{PHL}	3.5	3.9	4.3	4.8	6.5	3.00	0.42
SN	Q	t_{PLH}	3.7	4.3	4.8	5.3	7.5	3.20	0.55
RN	Q	t_{PHL}	4.5	4.9	5.4	5.8	7.7	4.00	0.46

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$


GN
RN
NA02
SN
D
P
N
N
N
NA02
G
G
P
N
Q
GN

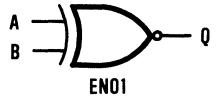
EN01

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Exclusive NOR Gate

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 3
Bolt Syntax: Q .EN01 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.4	4.0	4.5	5.1	7.4
		t_{PHL}	3.2	3.7	4.1	4.6	6.6

Intrinsic Parameters t_{dx}	K
2.90	0.56
2.70	0.48

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

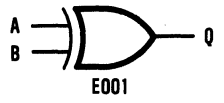
EO01

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Exclusive OR Gate

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	2

Equivalent Gate Count: 3
Bolt Syntax: Q .EO01 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.6	4.7	5.7	6.7	10.0
		t_{PHL}	2.9	3.3	3.6	4.0	5.3

Intrinsic Parameters t_{dx}	K
2.60	1.06
2.60	0.34

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

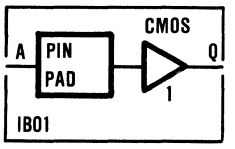
IB01

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed CMOS Non-Inverting Input Buffer

Logic Symbol



Truth Table

A	Q
H	H
L	L

Input Loading

Logic Input	Equivalent Unit Loads
NA	

Equivalent Gate Count: 1
Bolt Syntax: Q .IB01 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	1.1	1.4	1.6	1.9	3.0
		t_{PHL}	0.8	1.0	1.2	1.4	2.2

Intrinsic Parameters t_{dx}	K
0.80	0.28
0.60	0.20

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

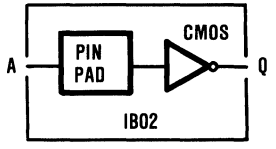
IB02

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed CMOS Inverting Input Buffer

Logic Symbol



Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
NA	

Equivalent Gate Count: 0
Bolt Syntax: Q .IB02 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	0.5	0.6	0.7	0.8	1.3
		t_{PHL}	0.2	0.3	0.4	0.5	0.8

Intrinsic Parameters t_{dx}	K
0.40	0.11
0.20	0.08

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

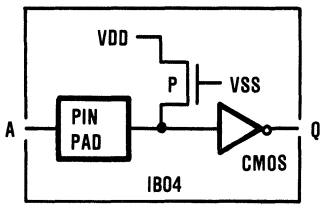
IB04

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed CMOS Inverting Input Buffer With Pull-Up

Logic Symbol



Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
NA	

Equivalent Gate Count: 0
Bolt Syntax: Q .IB04 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	0.5	0.6	0.7	0.8	1.3
		t_{PHL}	0.2	0.3	0.4	0.5	0.8

Intrinsic Parameters t_{dx}	K
0.40	0.11
0.20	0.08

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

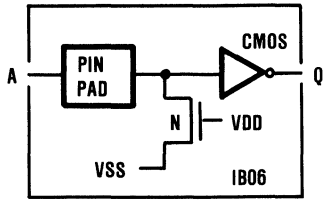
IB06

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed CMOS Inverting Input Buffer With Pull Down

Logic Symbol



Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
NA	

Equivalent Gate Count: 0
Bolt Syntax: Q .IB06 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	0.5	0.6	0.7	0.8	1.3
		t_{PHL}	0.2	0.3	0.4	0.5	0.8

Intrinsic Parameters t_{dx}	K
0.40	0.11
0.20	0.08

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

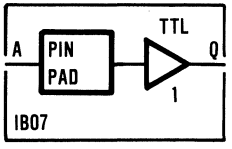
IB07

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed TTL Non-Inverting Input Buffer

Logic Symbol



Truth Table

A	Q
H	H
L	L

Input Loading

Logic Input	Equivalent Unit Loads
NA	

Equivalent Gate Count: 1
Bolt Syntax: Q .IB07 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.6	3.9	4.1	4.4	5.5
		t_{PHL}	3.8	4.0	4.2	4.4	5.2

Intrinsic Parameters t_{dx}	K
3.30	0.28
3.60	0.20

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

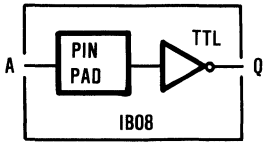
IB08

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed TTL Inverting Input Buffer

Logic Symbol



Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
NA	

Equivalent Gate Count: 0
Bolt Syntax: Q .IB08 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.3	3.6	3.9	4.2	5.6
		t_{PHL}	2.5	2.8	3.0	3.2	4.1

Intrinsic Parameters t_{dx}	K
2.90	0.32
2.30	0.21

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

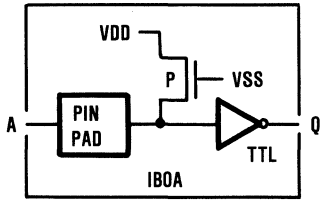
IB0A

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed TTL Inverting Input Buffer With Pull-Up

Logic Symbol



Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
NA	

Equivalent Gate Count: 0
Bolt Syntax: Q .IB0A A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.3	3.6	3.9	4.2	5.6
		t_{PHL}	2.5	2.8	3.0	3.2	4.1

Intrinsic Parameters t_{dx}	K
2.90	0.32
2.30	0.21

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

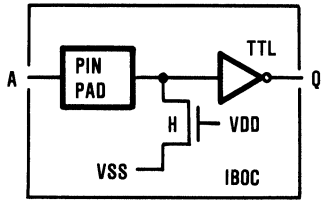
IB0C

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed TTL Inverting Input Buffer With Pull Down

Logic Symbol



Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
NA	

Equivalent Gate Count: 0
Bolt Syntax: Q .IB0C A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.3	3.6	3.9	4.2	5.6
		t_{PHL}	2.5	2.8	3.0	3.2	4.1

Intrinsic Parameters t_{dx}	K
2.90	0.32
2.30	0.21

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

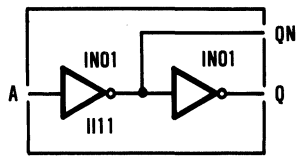
II11

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Clock Driver With a Single Inverter Followed By a Single Inverter

Logic Symbol



Truth Table

A	QN	Q
H	L	H
L	H	L

Input Loading

Logic Input	Equivalent Unit Loads
A	1

Equivalent Gate Count: 1
Bolt Syntax: Q QN .II11 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	2.6	3.7	4.9	6.0	10.6
		t_{PHL}	2.9	4.0	5.0	6.1	10.3
A	QN	t_{PLH}	2.2	3.0	3.7	4.4	7.4
		t_{PHL}	0.9	1.3	1.7	2.1	3.8

Intrinsic Parameters t_{dx}	K
1.40	1.14
1.90	1.06
1.50	0.73
0.50	0.41

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

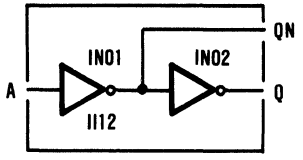
II12

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Clock Driver With Single Inverter Followed By Two Inverters In Parallel

Logic Symbol



Truth Table

A	QN	Q
H	L	H
L	H	L

Input Loading

Logic Input	Equivalent Unit Loads
A	1

Equivalent Gate Count: 2
Bolt Syntax: Q QN .II12 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	2.2	3.0	3.8	4.6	7.7
		t_{PHL}	2.9	3.8	4.6	5.5	9.0
A	QN	t_{PLH}	2.9	3.6	4.3	4.9	7.6
		t_{PHL}	1.2	1.6	2.0	2.3	3.9

Intrinsic Parameters t_{dx}	K
1.40	0.78
2.00	0.86
2.20	0.68
0.80	0.38

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

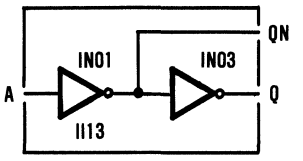
II13

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Clock Driver With Single Inverter Followed By a Three Inverters In Parallel

Logic Symbol



Truth Table

A	QN	Q
H	L	H
L	H	L

Input Loading

Logic Input	Equivalent Unit Loads
A	1

Equivalent Gate Count: 2
Bolt Syntax: Q QN .II13 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8	Intrinsic Parameters t_{dx}	K
A	Q	t_{PLH}	2.1	2.6	3.1	3.6	5.7	1.60	0.51
		t_{PHL}	2.7	3.2	3.8	4.4	6.8	2.10	0.58
A	QN	t_{PLH}	2.7	3.3	3.8	4.3	6.5	2.20	0.54
		t_{PHL}	1.1	1.4	1.7	2.1	3.3	0.70	0.33

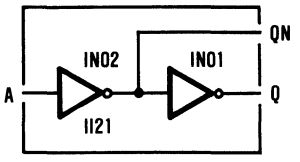
Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Clock Driver With Two Inverters In Parallel Followed By A Single Inverter

Logic Symbol



Truth Table

A	QN	Q
H	L	H
L	H	L

Input Loading

Logic Input	Equivalent Unit Loads
A	2

Equivalent Gate Count: 2
Bolt Syntax: Q QN .II21 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	1.4	2.0	2.7	3.3	5.8
		t_{PHL}	1.9	2.5	3.1	3.6	5.9
A	QN	t_{PLH}	1.6	1.9	2.3	2.6	4.1
		t_{PHL}	0.4	0.6	0.9	1.1	2.1

Intrinsic Parameters t_{dx}	K
0.80	0.62
1.40	0.57
1.20	0.35
0.10	0.24

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

GOULD

AMI Semiconductors

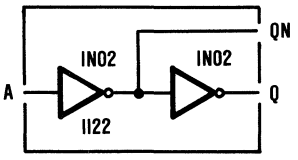
II22

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Clock Driver With By Two Inverters In Parallel Followed By Two Inverters In Parallel

Logic Symbol



Truth Table

A	QN	Q
H	L	H
L	H	L

Input Loading

Logic Input	Equivalent Unit Loads
A	2

Equivalent Gate Count: 2
Bolt Syntax: Q QN .II22 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	2.5	3.2	3.8	4.5	7.1
		t_{PHL}	3.2	4.0	4.8	5.5	8.6
A	QN	t_{PLH}	3.5	4.2	4.9	5.5	8.3
		t_{PHL}	1.4	1.9	2.3	2.7	4.3

Intrinsic Parameters t_{dx}	K
1.90	0.65
2.50	0.76
2.80	0.68
1.00	0.41

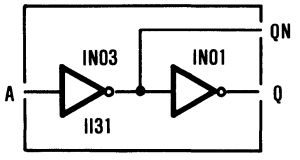
Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Clock Driver With Three Inverters In Parallel Followed By A Single Inverter

Logic Symbol



Truth Table

A	QN	Q
H	L	H
L	H	L

Input Loading

Logic Input	Equivalent Unit Loads
A	3

Equivalent Gate Count: 2
Bolt Syntax: Q QN .II31 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	1.7	2.7	3.6	4.5	8.2
		t_{PHL}	2.0	2.6	3.2	3.8	6.3
A	QN	t_{PLH}	1.2	1.4	1.7	1.9	2.9
		t_{PHL}	0.1	0.3	0.5	0.7	1.5

Intrinsic Parameters t_{dx}	K
0.80	0.92
1.40	0.62
0.90	0.24
0.00	0.19

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

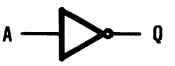
IN01

3μ Double-Metal HCMOS Gate Arrays

Description

Single Pre-Routed Inverter

Logic Symbol



IN01

Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	1

Equivalent Gate Count: 1
Bolt Syntax: Q .IN01 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	1.3	1.9	2.4	2.9	4.7
		t_{PHL}	0.6	0.9	1.3	1.6	3.0

Intrinsic Parameters t_{dx}	K
0.80	0.53
0.30	0.33

Propagation Delay Equation: $t_{px} = t_{dx}(F)$

IN02

3μ Double-Metal HCMOS Gate Arrays

Description

Two Pre-Routed Inverters In Parallel

Logic Symbol

IN02

Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	2

Equivalent Gate Count: 1
Bolt Syntax: Q .IN02 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	0.8	1.1	1.4	1.6	2.7
		t_{PHL}	0.2	0.4	0.6	0.8	1.6

Intrinsic Parameters t_{dx}	K
0.50	0.28
0.00	0.18

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

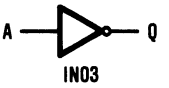
IN03

3μ Double-Metal HCMOS Gate Arrays

Description

Three Pre-Routed Inverters In Parallel

Logic Symbol



IN03

Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	3

Equivalent Gate Count: 2
Bolt Syntax: Q .IN03 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 4	8	12	16	20
A	Q	t_{PLH}	1.4	2.1	2.8	3.5	4.3
		t_{PHL}	0.6	1.1	1.6	2.2	2.7

Intrinsic Parameters t_{dx}	K
0.60	0.18
0.00	0.13

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

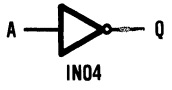
IN04

3μ Double-Metal HCMOS Gate Arrays

Description

Four Pre-Routed Inverters in Parallel

Logic Symbol



Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	4

Equivalent Gate Count: 2
Bolt Syntax: Q .IN04 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 4	8	12	16	20
Any Input	Q	t_{PLH}	1.1	1.7	2.3	2.9	3.5
		t_{PHL}	0.4	0.9	1.4	1.9	2.4

Intrinsic Parameters t_{dx}	K
0.50	0.15
0.00	0.13

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

IN05

3μ Double-Metal HCMOS Gate Arrays

Description

Five Pre-Routed Inverters In Parallel

Logic Symbol

IN05

Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	5

Equivalent Gate Count: 3
Bolt Syntax: Q .IN05 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 4	8	12	16	20
Any Input	Q	t_{PLH}	1.0	1.54	2.06	2.58	3.1
		t_{PHL}	0.4	0.8	1.2	1.6	2.0

Intrinsic Parameters t_{dx}	K
0.50	0.13
0.00	0.10

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times K(F)$

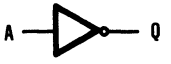
IN06

3μ Double-Metal HCMOS Gate Arrays

Description

Six Pre-Routed Inverters in Parallel

Logic Symbol



IN06

Truth Table

A	Q
H	L
L	H

Input Loading

Logic Input	Equivalent Unit Loads
A	6

Equivalent Gate Count: 3
Bolt Syntax: Q .IN06 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 4	8	12	16	20
A	Q	t_{PLH}	0.9	1.4	1.8	2.2	2.7
		t_{PHL}	0.2	0.5	0.8	1.1	1.5

Intrinsic Parameters t_{dx}	K
0.50	0.11
0.00	0.08

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

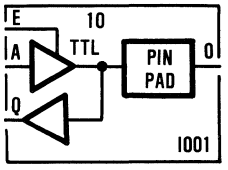
IO01

3μ Double-Metal HCMOS Gate Arrays

Description

TTL Non-Inverting Bi-Directional Input/Output Buffer With Positive Enable

Logic Symbol



Truth Table

Output		Input		
A	E	O	O	Q
X	L	Z		
H	H	H	H	H
L	H	L	L	L

Input Loading

Logic Input	Equivalent Unit Loads
A, E	2
O	4

Equivalent Gate Count: 10
Bolt Syntax: Q O .IO01 A E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	O	t_{PLH}	16.8	26.3	35.8
		t_{PHL}	10.8	14.3	17.8
E	O	t_{PZH}	16.2	25.7	35.2
		t_{PZL}	9.6	13.1	16.6
			Number of Unit Loads (F) 1	2	3	4	8
O	Q	t_{PLH}	3.9	4.5	5.0	5.5	7.7
		t_{PHL}	3.2	3.5	3.9	5.5	5.5

Delay Coefficients t_{dx}	$k_{t_{dx}}$
7.30	0.19
7.30	0.07
6.70	0.19
6.10	0.07
Intrinsic Parameters t_{dx}	K
3.40	0.54
2.90	0.32

Propagation Delay Equation Out: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$
Propagation Delay Equation In: $t_{px} = t_{dx} + K(F)$

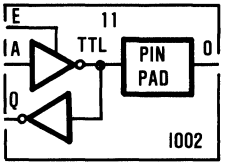
IO02

3μ Double-Metal HCMOS Gate Arrays

Description

TTL Non-Inverting Bi-Directional Input/Output Buffer With Positive Enable

Logic Symbol



Truth Table

Output		Input		
A	E	O	O	Q
X	L	Z		
H	H	L	L	H
L	H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
A	1
E	2
O	4

Equivalent Gate Count: 11
Bolt Syntax: Q O .IO02 A E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	O	t_{PLH}	17.7	27.2	36.7
		t_{PHL}	12.7	16.2	19.7
E	O	t_{PZH}	16.2	25.7	35.2
		t_{PZL}	9.6	13.1	16.6
			Number of Unit Loads (F) 1	2	3	4	8
O	Q	t_{PLH}	4.3	4.6	4.8	5.1	6.2
		t_{PHL}	4.7	4.9	5.1	5.3	6.1

Delay Coefficients t_{dx}	$k_{t_{dx}}$
8.20	0.19
9.20	0.07
6.70	0.19
6.10	0.07
Intrinsic Parameters t_{dx}	K
4.00	0.28
4.50	0.20

Propagation Delay Equation Out: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$
Propagation Delay Equation In: $t_{px} = t_{dx} + K(F)$

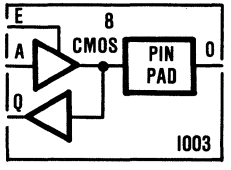
IO03

3μ Double-Metal HCMOS Gate Arrays

Description

CMOS Non-Inverting Bi-Directional Input/Output Buffer With Positive Enable

Logic Symbol



Truth Table

Output		Input	
A	E	O	Q
X	L	Z	
H	H	H	H
L	H	L	L

Input Loading

Logic Input	Equivalent Unit Loads
A, E	2
O	2

Equivalent Gate Count: 8
Bolt Syntax: Q O .IO03 A E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	O	t_{PLH}	11.1	16.6	22.1
		t_{PHL}	7.1	10.1	13.1
E	O	t_{PZH}	10.0	15.5	21.0
		t_{PZL}	7.3	10.8	14.3

			Number of Unit Loads (F) 1	2	3	4	8
O	Q	t_{PLH}	2.6	3.2	3.9	4.5	7.1
		t_{PHL}	3.3	4.0	4.8	5.5	8.6

Delay Coefficients t_{dx}	$k_{t_{dx}}$
5.60	0.11
4.10	0.06
4.50	0.11
3.80	0.07
Intrinsic Parameters t_{dx}	**K**
1.90	0.65
2.50	0.76

Propagation Delay Equation Out: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$
Propagation Delay Equation In: $t_{px} = t_{dx} + K(F)$

GOULD
AMI Semiconductors

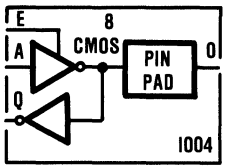
IO04

3μ Double-Metal HCMOS Gate Arrays

Description

CMOS Non-Inverting Bi-Directional Input/Output Buffer With Positive Enable

Logic Symbol



Truth Table

Output		Input		
A	E	O	O	Q
X	L	Z		
H	H		L	H
L	H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
A	1
E, O	2

Equivalent Gate Count: 8
Bolt Syntax: Q O .IO04 A E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	O	t_{PLH}	12.0	17.5	23.0
		t_{PHL}	9.0	12.0	15.0
E	O	t_{PZH}	10.0	15.5	21.0
		t_{PZL}	7.3	10.8	14.3
			Number of Unit Loads (F) 1	2	3	4	8
O	Q	t_{PLH}	0.8	1.1	1.4	1.6	2.7
		t_{PHL}	0.2	0.4	0.6	0.8	1.6

Delay Coefficients t_{dx}	$k_{t_{dx}}$
5.50	0.11
6.00	0.06
4.50	0.11
3.80	0.07
Intrinsic Parameters t_{dx}	K
0.50	0.28
0.00	0.20

Propagation Delay Equation Out: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$
Propagation Delay Equation In: $t_{px} = t_{dx} + K(F)$

IT01

3μ Double-Metal HCMOS Gate Arrays

Description

Non-Inverter Internal Tri-State Buffer

Logic Symbol

Truth Table

A	E	Q
X	L	Z
X	H	A

Input Loading

Logic Input	Equivalent Unit Loads
A	1
E	2

Equivalent Gate Count: 2
Bolt Syntax: Q .IT01 A E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	2.0	2.6	3.1	3.7	6.0
		t_{PHL}	2.0	2.5	3.0	3.4	5.4
E	Q	Z-1	1.9	2.5	3.1	3.6	5.9
		Z-0	0.5	1.0	1.5	2.0	4.1

Intrinsic Parameters t_{dx}	K
1.50	0.56
1.60	0.47
1.40	0.56
0.00	0.51

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

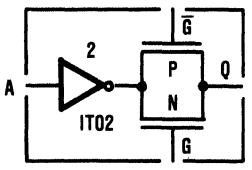
IT02

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Inverter Driving a Transmission Gate

Logic Symbol



Truth Table

A	G	GN	Q
A	L	H	Z
A	H	L	AN

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .IT02 A G GN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
G	Q	t_{PLH}	1.8	2.4	3.1	3.8	6.5
		t_{PHL}	1.0	1.4	1.8	2.3	4.0
A	Q	t_{PLH}	2.5	3.2	3.8	4.5	7.1
		t_{PHL}	1.2	1.6	2.0	2.4	4.1

Intrinsic Parameters t_{dx}	K
1.10	0.68
0.50	0.43
1.90	0.65
0.80	0.41

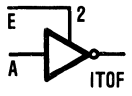
Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

3μ Double-Metal HCMOS Gate Arrays

Description

Inverting Internal Tri-State Buffer

Logic Symbol



Truth Table

A	E	Q
X	L	Z
X	H	AN

Input Loading

Logic Input	Equivalent Unit Loads
A	1
E	2

Equivalent Gate Count: 2
Bolt Syntax: Q .ITOF A E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	4.8	5.9	6.9	8.0	12.2
		t_{PHL}	1.9	2.4	2.8	3.3	5.2
E	Q	Z-1	4.4	5.5	6.5	7.5	11.8
		Z-0	1.4	1.9	2.4	2.9	5.0

Intrinsic Parameters t_{dx}	K
3.80	1.05
1.40	0.47
3.40	1.05
0.90	0.51

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

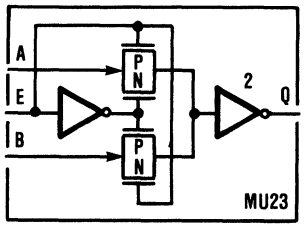
MU23

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Two To One Multiplexer

Logic Symbol



Truth Table

A	B	E	Q
A	B	H	BN
A	B	L	AN

Input Loading

Logic Input	Equivalent Unit Loads
A, B	4
E	2

Equivalent Gate Count: 2
Bolt Syntax: Q .MU23 A B E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
A	Q	t_{PLH}	1.7	2.3	2.8	3.4	5.7
		t_{PHL}	0.6	1.0	1.3	1.7	3.2
E	Q	t_{PLH}	2.8	3.4	4.0	4.5	6.8
		t_{PHL}	2.1	2.5	2.8	3.1	4.4

Intrinsic Parameters t_{dx}	K
1.10	0.57
0.20	0.38
2.30	0.56
1.80	0.33

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

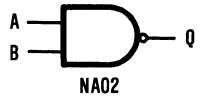
NA02

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Two Input NAND Gate

Logic Symbol



NA02

Truth Table

A	B	Q
L	X	H
X	L	H
H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 1
Bolt Syntax: Q .NA02 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	1.8	2.3	2.8	3.4	5.4
		t_{PHL}	1.0	1.5	1.9	2.4	4.2

Intrinsic Parameters t_{dx}	K
1.30	0.52
0.60	0.44

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

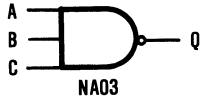
NA03

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Three Input NAND Gate

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .NA03 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.5	3.0	3.6	4.1	6.3
		t_{PHL}	2.1	2.8	3.4	4.1	6.7

Intrinsic Parameters t_{dx}	K
1.90	0.55
1.50	0.65

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

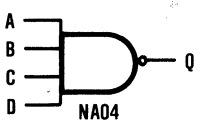
NA04

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Four Input NAND Gate

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .NA04 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.7	3.3	3.9	4.4	6.7
		t_{PHL}	3.0	3.9	4.7	5.5	8.8

Intrinsic Parameters t_{dx}	K
2.20	0.56
2.20	0.82

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

GOULD

AMI Semiconductors

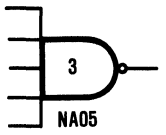
NA05

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Five Input NAND Gate

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 3
Bolt Syntax: Q .NA05 A B C D E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.1	3.7	4.3	5.0	7.5
		t_{PHL}	4.1	5.2	6.2	7.3	11.5

Intrinsic Parameters t_{dx}	K
2.50	0.62
3.00	1.06

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

GOULD

AMI Semiconductors

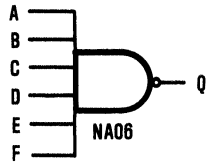
NA06

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Six Input NAND Gate

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 3
Bolt Syntax: Q .NA06 A B C D E F;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	3.3	4.0	4.6	5.2	7.7
		t_{PHL}	5.9	7.2	8.4	9.6	14.5

Intrinsic Parameters t_{dx}	K
2.70	0.62
4.70	1.22

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

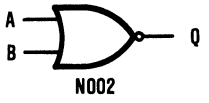
NO02

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Two Input NOR Gate

Logic Symbol



Truth Table

A	B	Q
L	L	H
X	H	H
H	X	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 1
Bolt Syntax: Q .NO02 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.4	3.4	4.3	5.2	8.9
		t_{PHL}	0.8	1.1	1.4	1.8	3.1

Intrinsic Parameters t_{dx}	K
1.50	0.92
0.50	0.31

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

GOULD

AMI Semiconductors

NO03

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Three Input NOR Gate

Logic Symbol

NO03

Truth Table

A	B	C	Q
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .NO03 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	6.7	6.1	7.5	8.9	14.5
		t_{PHL}	1.0	1.3	1.6	1.9	3.1

Intrinsic Parameters t_{dx}	K
3.30	1.41
0.70	0.30

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

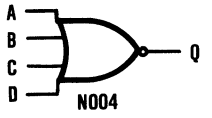
NO04

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Four Input NOR Gate

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
X	X	X	H	L
X	X	H	X	L
X	H	X	X	L
H	X	X	X	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .NO04 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	7.5	9.3	11.1	12.8	20.0
		t_{PHL}	1.1	1.6	1.8	2.1	3.3

Intrinsic Parameters t_{dx}	K
5.70	1.79
0.80	0.30

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

GOULD

AMI Semiconductors

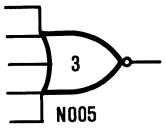
NO05

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Five Input NOR Gate

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
X	X	X	X	H	L
X	X	X	H	X	L
X	X	H	X	X	L
X	H	X	X	X	L
H	X	X	X	X	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 3
Bolt Syntax: Q .NO05 A B C D E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	10.8	13.2	15.7	18.7	27.9
		t_{PHL}	1.1	1.4	1.7	2.0	3.2

Intrinsic Parameters t_{dx}	K
8.30	2.45
0.80	0.30

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

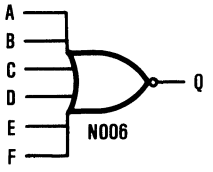
NO06

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Six Input NOR Gate

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	L	L	L	H
X	X	X	X	X	H	L
X	X	X	X	H	X	L
X	X	X	H	X	X	L
X	X	H	X	X	X	L
X	H	X	X	X	X	L
H	X	X	X	X	X	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 3
Bolt Syntax: Q .NO06 A B C D E F;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	14.6	17.3	20.0	22.7	33.6
		t_{PHL}	1.3	1.6	1.9	2.2	3.4

Intrinsic Parameters t_{dx}	K
11.90	2.72
1.00	0.30

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

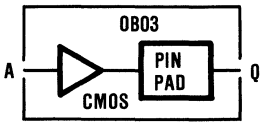
OB03

3μ Double-Metal HCMOS Gate Arrays

Description

CMOS Output Buffer

Logic Symbol



Truth Table

A	Q
L	L
H	H

Input Loading

Logic Input	Equivalent Unit Loads
A	5

Equivalent Gate Count: Contained within peripheral cell, no core devices used.
Bolt Syntax: Q .OB03 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	Q	t_{PLH}	6.9	11.6	16.5
		t_{PHL}	5.3	8.4	11.6
ITTL LOAD		t_{PLH}	4.9	8.0	11.2
A	Q	t_{PHL}	8.1	13.6	19.1

Delay Coefficients t_{dx}	$k_{t_{dx}}$
2.00	0.10
2.20	0.10
1.70	0.10
2.60	0.10

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

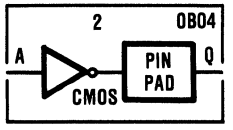
OB04

3μ Double-Metal HCMOS Gate Arrays

Description

CMOS Inverting Output Buffer

Logic Symbol



Truth Table

A	Q
L	H
H	L

Input Loading

Logic Input	Equivalent Unit Loads
A	4

Equivalent Gate Count: 2
Bolt Syntax: Q .OB04 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	Q	t_{PLH}	8.3	13.3	18.3
		t_{PHL}	5.7	8.7	11.7
ITTL LOAD		t_{PLH}	6.0	9.0	12.0
A	Q	t_{PHL}	8.1	13.1	18.1

Delay Coefficients t_{dx}	$k_{t_{dx}}$
3.30	0.10
2.70	0.06
3.00	0.06
3.10	0.10

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

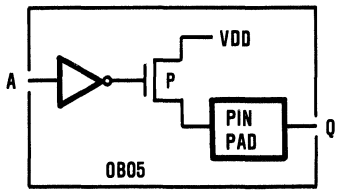
OB05

3μ Double-Metal HCMOS Gate Arrays

Description

Open Drain Output Buffer

Logic Symbol



Truth Table

A	Q
H	H
L	Z

Input Loading

Logic Input	Equivalent Unit Loads
A	1

Equivalent Gate Count: Contained within peripheral cell, no core devices used.
Bolt Syntax: Q .OB05 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	Q	t_{PLH}	6.5	11.7	17.0

Intrinsic Parameters t_{dx}	$k_{t_{dx}}$
1.30	0.10

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

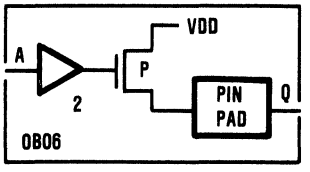
OB06

3μ Double-Metal HCMOS Gate Arrays

Description

Inverting Open Drain Output Buffer

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Input Loading

Logic Input	Equivalent Unit Loads
A	4

Equivalent Gate Count: 2
Bolt Syntax: Q .OB06 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	Q	t_{PLH}	7.6	12.8	18.0

Delay Coefficients t_{dx}	$k_{t_{dx}}$
2.40	.104

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

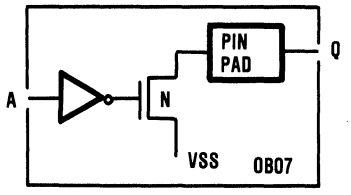
OB07

3μ Double-Metal HCMOS Gate Arrays

Description

Open Drain Output Buffer

Logic Symbol



Truth Table

A	Q
H	Z
L	L

Input Loading

Logic Input	Equivalent Unit Loads
A	5

Equivalent Gate Count: Contained within peripheral cell, no core devices used.
Bolt Syntax: Q .OB07 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	Q 1K RESISTOR	t_{PHL}	4.8	8.3	11.8
A	Q 10K RESISTOR	t_{PHL}	4.7	8.0	11.4

Delay Coefficients t_{dx}	$k_{t_{dx}}$
1.30	0.10
1.30	0.10

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

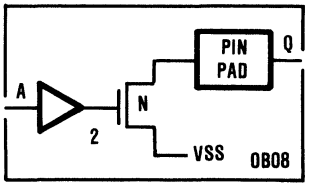
OB08

3μ Double-Metal HCMOS Gate Arrays

Description

Inverting Open Drain Output Buffer

Logic Symbol



Truth Table

A	Q
L	Z
H	L

Input Loading

Logic Input	Equivalent Unit Loads
A	4

Equivalent Gate Count: 2
Bolt Syntax: Q .OB08 A;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	Q 1K RESISTOR	t_{PLH}	5.3	8.8	12.3
A	Q 10K RESISTOR	t_{PHL}	5.2	8.5	11.7

Delay Coefficients t_{dx}	$k_{t_{dx}}$
1.80	0.07
1.80	0.067

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

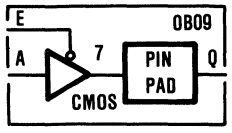
OB09

3μ Double-Metal HCMOS Gate Arrays

Description

CMOS Tri-State Non-Inverting Output Buffer With Negative Enable

Logic Symbol



Truth Table

A	EN	Q
X	H	Z
H	L	H
L	L	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	2

Equivalent Gate Count: 7
Bolt Syntax: Q .OB09 A EN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	Q	t_{PLH}	11.1	16.6	22.1
		t_{PHL}	7.1	10.1	13.1
EN	Q	t_{PZH}	11.0	16.5	22.0
		t_{PZL}	7.7	11.2	14.7

Delay Coefficients t_{dx}	$k_{t_{dx}}$
5.60	0.11
4.10	0.06
5.50	0.11
4.20	0.07

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

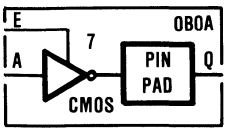
OB0A

3μ Double-Metal HCMOS Gate Arrays

Description

CMOS Tri-State Non-Inverting Output Buffer With Positive Enable

Logic Symbol



Truth Table

A	E	Q
X	L	Z
L	H	H
H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	2

Equivalent Gate Count: 7
Bolt Syntax: Q .OB0A A E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Capacitive Load 50pF	100pF	150pF
A	Q	t_{PLH}	15.3	20.8	26.3
		t_{PHL}	10.2	13.2	16.2
E	Q	t_{PZH}	14.5	20.0	25.5
		t_{PZL}	11.1	14.6	18.1

Delay Coefficients t_{dx}	$k_{t_{dx}}$
9.80	0.11
7.20	0.06
9.00	0.11
7.60	0.07

Propagation Delay Equation: $t_{px} = t_{dx} + k_{t_{dx}} \times C_L$

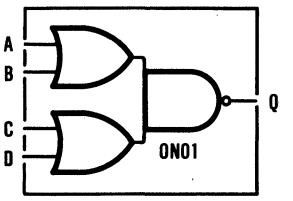
ON01

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed OR-NAND Gate

Logic Symbol



Truth Table

A	B	C	D	Q
H	X	H	X	L
H	X	X	H	L
X	H	H	X	L
L	L	X	X	H
X	X	L	L	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .ON01 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	5.1	6.0	7.0	7.9	11.7
		t_{PHL}	2.1	2.6	3.0	3.4	5.2

Intrinsic Parameters t_{dx}	K
4.10	0.95
1.70	0.42

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

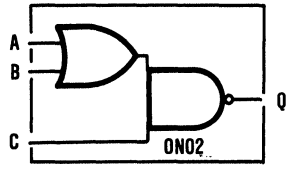
ON02

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed OR-NAND Gate

Logic Symbol



Truth Table

A	B	C	Q
X	X	L	H
X	H	H	L
H	X	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .ON02 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	4.1	5.1	6.1	7.1	11.0
		t_{PHL}	1.6	2.1	2.6	3.0	4.9

Intrinsic Parameters t_{dx}	K
3.10	0.98
1.10	0.46

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

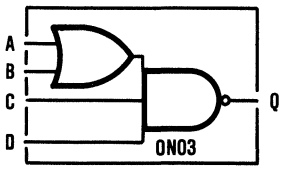
ON03

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed OR-NAND Gate

Logic Symbol



Truth Table

A	B	C	D	Q
X	X	X	L	H
X	X	L	X	H
L	L	X	X	H
X	H	H	H	L
H	X	H	H	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .ON03 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.8	3.7	4.7	5.6	9.4
		t_{PHL}	1.9	2.6	3.3	3.9	6.5

Intrinsic Parameters t_{dx}	K
1.90	0.94
1.30	0.65

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

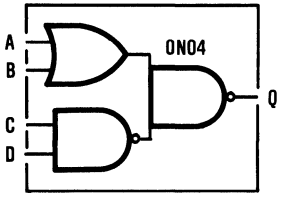
ON04

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed OR-NAND-NAND Gate

Logic Symbol



Truth Table

A	B	C	D	Q
X	H	X	L	L
H	X	X	L	L
X	H	L	X	L
H	X	L	X	L
L	L	X	X	H
X	X	H	H	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 3
Bolt Syntax: Q .ON04 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.3	2.8	3.3	3.8	5.9
		t_{PHL}	2.6	3.1	3.6	4.1	6.0

Intrinsic Parameters t_{dx}	K
1.70	0.56
2.10	0.49

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

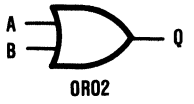
OR02

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Two Input OR Gate

Logic Symbol



Truth Table

A	B	Q
L	L	L
X	H	H
H	X	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .OR02 A B;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	1.9	2.4	2.9	3.5	5.5
		t_{PHL}	2.7	3.1	3.5	3.8	5.2

Intrinsic Parameters t_{dx}	K
1.40	0.52
2.40	0.34

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

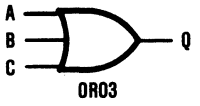
OR03

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Three Input OR Gate

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
X	X	H	H
X	H	X	H
H	X	X	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q .OR03 A B C;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.2	2.7	3.3	3.8	5.8
		t_{PHL}	4.9	5.3	5.7	6.2	7.8

Intrinsic Parameters t_{dx}	K
1.70	0.52
4.50	0.40

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

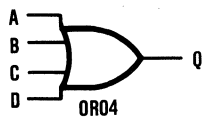
OR04

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Four Input OR Gate

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
X	X	X	H	H
X	X	H	X	H
X	H	X	X	H
H	X	X	X	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 3
Bolt Syntax: Q .OR04 A B C D;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.3	2.8	3.4	3.9	5.9
		t_{PHL}	6.6	7.1	7.6	8.2	10.3

Intrinsic Parameters t_{dx}	K
1.80	0.52
6.10	0.52

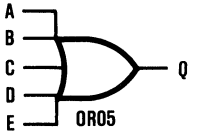
Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Five Input OR Gate

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	L
X	X	X	X	H	H
X	X	X	H	X	H
X	X	H	X	X	H
X	H	X	X	X	H
H	X	X	X	X	H

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

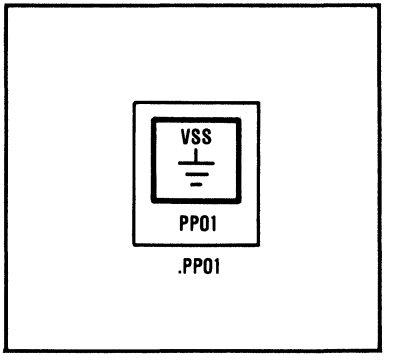
Equivalent Gate Count: 3
Bolt Syntax: Q .OR05 A B C D E;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
Any Input	Q	t_{PLH}	2.4	2.9	3.5	4.0	6.2
		t_{PHL}	9.3	9.9	10.5	11.0	13.3

Intrinsic Parameters t_{dx}	K
1.90	0.55
8.80	0.56

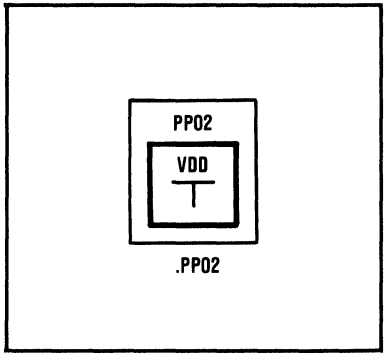
Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

3μ Double-Metal HCMOS Gate Arrays



NOTE: ONE PP01 MUST BE USED PER GROUND (V_{SS}) PIN.

3μ Double-Metal HCMOS Gate Arrays



NOTE: ONE PP02 MUST BE USED PER POWER (V_{DD}) PIN.

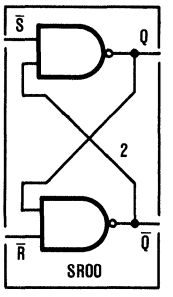
SR00

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed Set-Reset NAND Gate Latch

Logic Symbol



Truth Table

SN	RN	Q	QN
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q QN .SR00 SN RN;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
SN	Q	t_{PLH}	2.2	2.7	3.2	3.8	5.9
RN	Q	t_{PHL}	3.0	3.4	3.9	4.3	6.1

Intrinsic Parameters t_{dx}	K
1.60	0.53
2.60	0.45

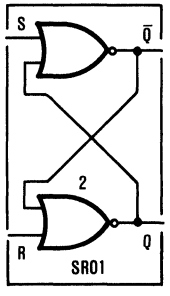
Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

3μ Double-Metal HCMOS Gate Arrays

Description

Pre-Routed NOR S R Latch

Logic Symbol



Truth Table

S	R	Q	QN
L	L	No change	
L	H	L	H
H	L	H	L
H	H	L	L

Input Loading

Logic Input	Equivalent Unit Loads
Any Input	1

Equivalent Gate Count: 2
Bolt Syntax: Q QN .SR01 R S;
Switching Characteristics:
Conditions: $V_{DD} = 5V$, $T_J = 25°C$, Typical Process

Max. Delay (ns) FROM	TO	Parameter	Number of Unit Loads (F) 1	2	3	4	8
S	Q	t_{PLH}	3.5	4.4	5.4	6.3	10.0
R	Q	t_{PHL}	1.0	1.3	1.6	1.9	3.2

Intrinsic Parameters t_{dx}	K
2.60	0.93
0.70	0.31

Propagation Delay Equation: $t_{px} = t_{dx} + K(F)$

Schematic Capture Aids

Schematic Capture Aids

SCA	Description
Count1	4-Bit Binary Counter
Count2	4-Bit Binary Counter Presetable
Count3	4-Bit Binary Counter Expandable
Count4	4-Bit Binary Counter Presetable, Expandable
DEC1	4-Bit Decade Counter
DEC2	4-Bit Decade Counter With DIRECT LOAD
DEC3	4-Bit Decade Counter With CARRYIN And CARRYOUT
DEC4	4-Bit Decade Counter With DIRECT LOAD, CARRYIN, And CARRYOUT
UDB1	4-Bit Binary Up/Down Counter
UDB2	4-Bit Binary Up/Down Counter With DIRECT LOAD
UDB3	4-Bit Binary Up/Down Counter With CARRYIN And CARRYOUT
UDB4	4-Bit Binary Up/Down Counter With DIRECT LOAD, CARRYIN, and CARRYOUT
UDD1	4-Bit Up/Down Decade Counter
UDD2	4-Bit Up/Down Decade Counter With DIRECT LOAD
UDD3	4-Bit Up/Down Decade Counter With CARRYIN and CARRYOUT
UDD4	4-Bit Up/Down Decade Counter With DIRECT LOAD, CARRYIN and CARRYOUT
10G138	3 to 8 Decoder
10G139	2 to 4 Decoder
10G148	8 to 3 Priority Encoder
10G154	4 to 16 Decoder
10G164	8-Bit Serial in Parallel Out Shift Register
10G165	8-Bit Parallel/Serial In Serial Out Shift Register
10G166	8-Bit Parallel/Serial Serial Out Shift Register
10G182	Carry Lookahead Generator
10G194	4-Bit Bi-Directional Universal Shift Register
10G195	4-Bit Synchronous Universal Shift Register
10G199	8-Bit Universal Shift Register
10G91	8-Bit Serial Shift Register
10G280	9-Bit Odd/Even Parity Generator/Check

Schematic Capture Aids

I. Introduction

Schematic capture aids (SCA) are pre-captured and pre-simulated functional blocks. They are intended to reduce the time required for logic conversion, schematic capture, and logic simulation. Since they have not been characterized with respect to timing, propagation delays for the individual SCA's have not been supplied. In order to calculate propagation delays a user must use data from the pre-characterized macros which make up an SCA.

Since Gould AMI requires that each wire name in a circuit be unique, TEC files have been created to facilitate the changing of wire names. THE WIRE NAMES ON THE ORIGINAL DRAWINGS SHOULD NOT CHANGE AS THIS WILL RENDER THE ASSOCIATED TEC FILE OBSOLETE.

The data sheets for each SCA contain all the necessary information for successful usage. This includes:

- Description
- Equivalent Gate Count
- Functional Description
- Truth Table
- Drawing of the SCA

In addition, a table of contents is provided for the user's convenience.

Schematic Capture Aids Datasheets

SCA COUNT1

Description

Count1 Four Bit Binary Counter

Equivalent Gate Count: 39

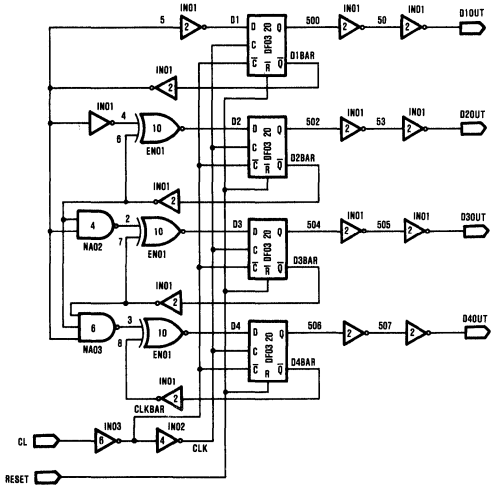
Functional Description

Count1 is a four bit synchronous binary counter with asynchronous RESET. This counter consists of 4 D flip-flops with appropriate gate networks feeding the D inputs. When RESET is high, all output changes occur as a result of a low to high clock transition. When RESET is low, it overrides all other inputs and sets the outputs low.

Truth Table

CLOCK	RESET	D4 OUT	D3 OUT	D2 OUT	D1 OUT
X	L	L	L	L	L
↑	H	L	L	L	H
↑	H	L	L	H	L
↑	H	L	L	H	H
•	•		•		
•	•		•		
•	•		•		
↑	H	H	H	H	H
↑	H	L	L	L	L

SCA COUNT1


INO1
D1
DFF03 20
D1BAR
D1OUT
D2
D2BAR
D2OUT
D3
D3BAR
D3OUT
D4
D4BAR
D4OUT
ENO1
NAO2
NAO3
CLKBAR
IN03
IN02
CL
CLK
RESET

Description

Count2 Four Bit Binary Counter with DIRECT LOAD

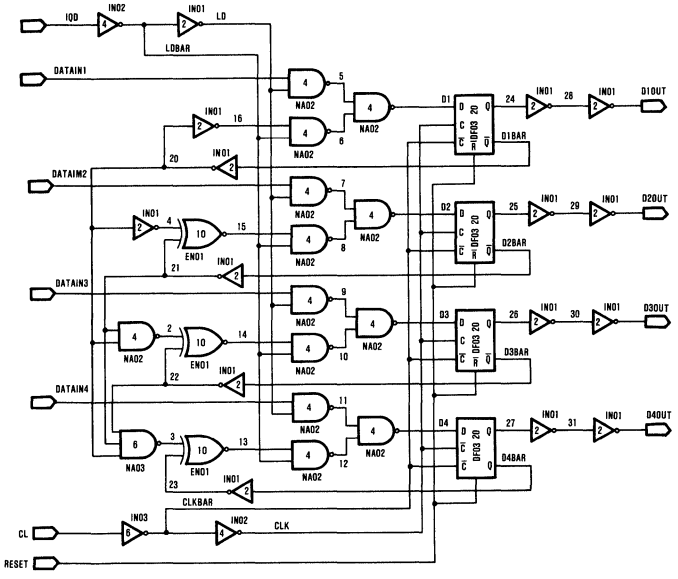
Equivalent Gate Count: 53

Functional Description

Count2 is a four bit synchronous binary counter with asynchronous RESET and direct load (LOD). This counter consists of 4 D flip-flops with appropriate gate networks feeding the D inputs. When RESET is high and LOD is low the output changes with the rising edge of the clock. When RESET is low, it overrides all other inputs and the outputs are set low. When RESET and LOD are high, data at inputs DATAIN1-DATAIN4 is loaded, with the rising clock edge, to the outputs D1OUT-D4OUT. If LOD is made low before the next clock cycle, the output will start counting from the number which was loaded.

Truth Table

CLOCK	RESET	LOD	DATAIN1	DATAIN2	DATAIN3	DATAIN4	D4OUT	D3OUT	D2OUT	D1OUT
X	L	X	X	X	X	X	L	L	L	L
↑	H	L	X	X	X	X	L	L	L	H
↑	H	L	X	X	X	X	L	L	H	L
↑	H	L	X	X	X	X	L	L	H	H
•	•	•		•				•		
•	•	•		•				•		
•	•	•		•				•		
↑	H	L	X	X	X	X	H	H	H	H
↑	H	H	X	X	X	X	L	L	L	L
↑	H	H	D1	D2	D3	D4	D4	D3	D2	D1


IQD
INO2
INO1
LD
LDBAR
DATAIN1
DATAIM2
DATAIN3
DATAIN4
CL
RESET
INO3
CLK
CLKBAR
NAO2
NAO3
END1
D1
D2
D3
D4
DFG3
D1BAR
D2BAR
D3BAR
D4BAR
D1OUT
D2OUT
D3OUT
D4OUT

Description

Count3 Four Bit Binary Counter With CARRYIN and CARRYOUT

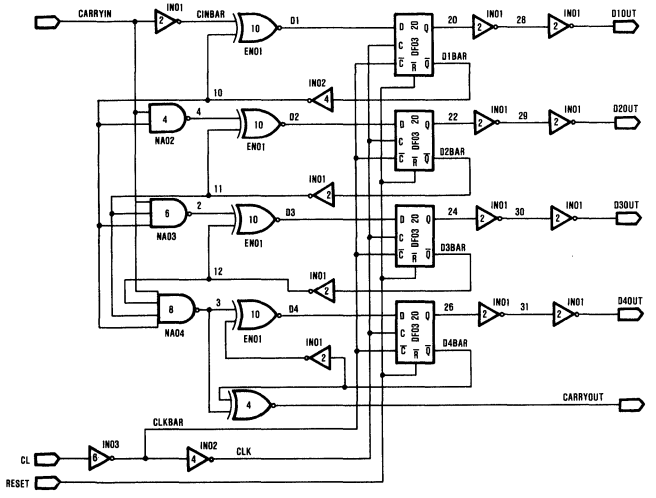
Equivalent Gate Count: 45

Functional Description

Count3 is a four bit synchronous counter with asynchronous RESET, CARRYIN, and CARRYOUT. This counter consists of 4 D flip-flops with appropriate gate networks feeding the D inputs. When RESET and CARRYIN are high, the output changes with the leading clock edge. On the 16th count, CARRYOUT becomes high for one cycle. When RESET is low it overrides all other inputs and outputs are set low. When RESET is high and CARRYIN is low, the output remains in its previous state.

Truth Table

CLOCK	RESET	CARRYIN	CARRYOUT	D4OUT	D3OUT	D2OUT	D1OUT
X	L	X	L	L	L	L	L
↑	H	H	L	L	L	L	H
↑	H	H	L	L	L	H	L
↑	H	H	L	L	L	H	H
•	•	•		•			
•	•	•		•			
•	•	•		•			
↑	H	H	L	H	H	H	L
↑	H	H	H	H	H	H	H
↑	H	L	L	H	H	H	H
↑	H	H	L	L	L	L	L
↑	H	L	H	Holds Previous State			


CARRYIN
IN01
CINBAR
10
ENO1
D1
DFF3
D1BAR
D1OUT
NA02
D2
D2BAR
D2OUT
NA03
D3
D3BAR
D3OUT
NA04
D4
D4BAR
D4OUT
CARRYOUT
CLKBAR
IN03
IN02
CLK
CL
RESET

SCA COUNT4

Description

Count4 Four Bit Binary Counter with DIRECT LOAD, CARRYIN and CARRYOUT

Equivalent Gate Count: 58

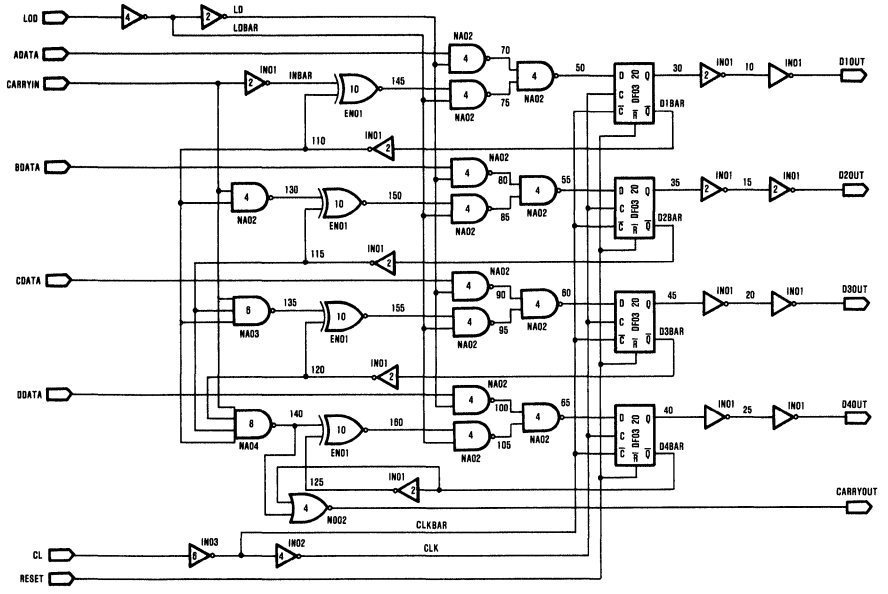
Functional Description

Count4 is a four bit binary synchronous counter with asynchronous RESET, DIRECT LOAD (LOD), CARRYIN, and CARRYOUT. When RESET and CARRYIN are high and LOD is low, the output changes with the leading clock edge. On the 16th count CARRYOUT becomes high for one cycle. When RESET is low, it overrides all other inputs and outputs are set low. When RESET is high, CARRYIN and LOD are low, the output remains in its past state. When RESET and LOD are high, data at inputs DATAIN1-DATAIN4 are loaded, with the leading clock edge, to the outputs D1OUT-D4OUT. If LOD is made low before the next cycle, the output will start counting from the number which was loaded.

Truth Table

CLOCK	RESET	LOD	CARRYIN	DATAIN1	DATAIN2	DATAIN3	DATAIN4	CARRYOUT	D4OUT	D3OUT	D2OUT	D1OUT
X	L	X	X	X	X	X	X	L	L	L	L	L
↑	H	L	H	X	X	X	X	L	L	L	L	H
↑	H	L	H	X	X	X	X	L	L	L	H	L
↑	H	L	H	X	X	X	X	L	L	L	H	H
•	•	•	•	•	•	•	•			•		
•	•	•	•	•	•	•	•			•		
•	•	•	•	•	•	•	•			•		
↑	H	L	H	X	X	X	X	L	H	H	H	L
↑	H	L	H	X	X	X	X	H	H	H	H	H
↑	H	L	L	X	X	X	X	L	H	H	H	H
↑	H	L	H	X	X	X	X	L	L	L	L	L
↑	H	L	L	X	X	X	X	L	Hold Previous State			
↑	H	H	H	D1	D2	D3	D4	—	D4	D3	D2	D1

SCA COUNT4


LOD
LD
LDBAR
ADATA
CARRYIN
INBAR
BDATA
CDATA
DDATA
CL
RESET
CLKBAR
CLK
CARRYOUT
D1OUT
D2OUT
D3OUT
D4OUT
D1BAR
D2BAR
D3BAR
D4BAR
NAO2
NAO3
NAO4
ENO1
NO02
INO1
INO2
INO3
DFR3

Description

DEC1 Four Bit Decade Counter

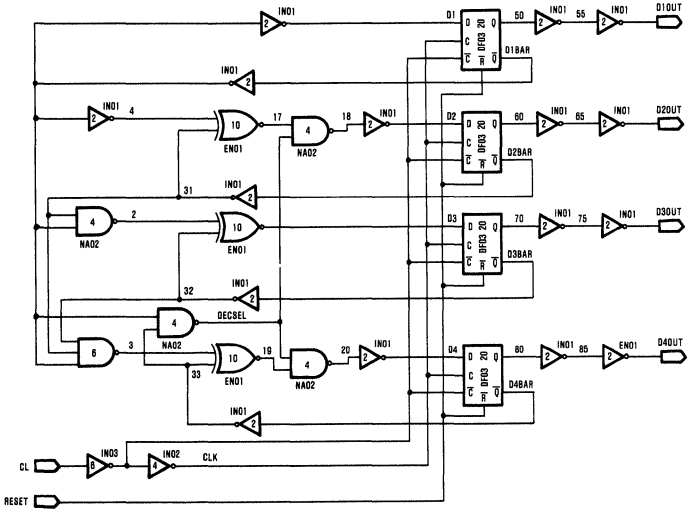
Equivalent Gate Count: 43

Functional Description

DEC1 is a four bit synchronous decade counter with asynchronous RESET. This counter consists of 4 D flip-flops with appropriate gate networks feeding the D inputs. When RESET is high the output changes with the rising clock edge. This modulo 10 counter counts from 0-9 then resets to zero. When RESET is low, it overrides all other inputs and the outputs are set low.

Truth Table

CLK	RESET	D40UT	D30UT	D20UT	D10UT
X	L	L	L	L	L
↑	H	L	L	L	L
↑	H	L	L	H	L
•	•			•	
•	•			•	
•	•			•	
↑	H	H	L	L	L
↑	H	H	L	L	H
↑	H	L	L	L	L


IND1
D1
DFD3
D1BAR
D1OUT
D2
D2BAR
D2OUT
D3
D3BAR
D3OUT
D4
D4BAR
D4OUT
ENO1
NAO2
DECSEL
CL
IND3
IND2
CLK
RESET

Description

DEC2 Four Bit Decade Counter with DIRECT LOAD

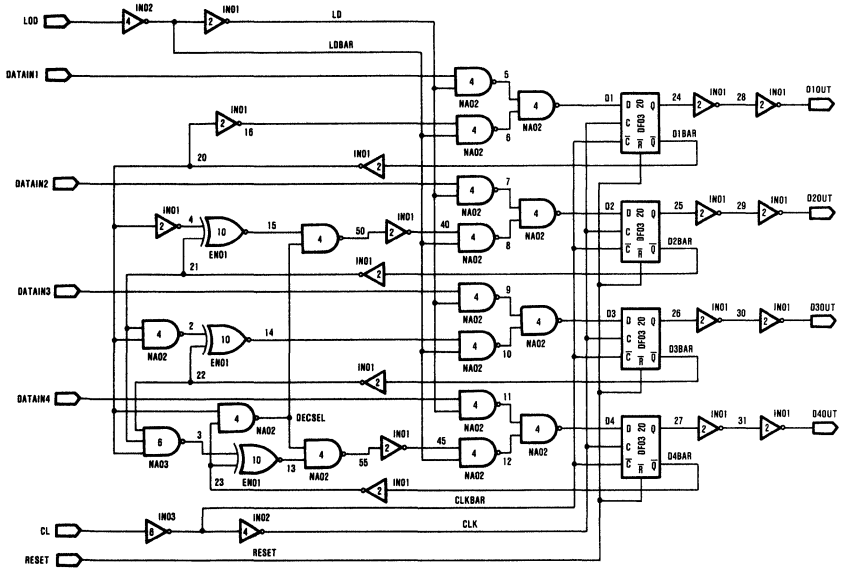
Equivalent Gate Count: 57

Functional Description

DEC2 is a four bit synchronous decade counter with asynchronous RESET and DIRECT LOAD (LOD). This counter consists of D flip-flops with appropriate gate networks feeding into the D inputs. When RESET is high and LOD is low, the output changes with the rising clock edge. This modulo 10 counter counts from 0-9 then resets to zero. When RESET is low, it overrides all other inputs and the outputs are set low. When RESET and LOD are high, data at the inputs DATAIN1-DATAIN4 are loaded with the rising clock edge, to the outputs D1OUT-D4OUT. If LOD is made low before the next clock cycle, the output will start counting from the number which was loaded.

Truth Table

CLK	RESET	LOD	DATAIN1	DATAIN2	DATAIN3	DATAIN4	D4OUT	D3OUT	D2OUT	D1OUT
X	L	X	X	X	X	X	L	L	L	L
↑	H	L	X	X	X	X	L	L	L	H
↑	H	L	X	X	X	X	L	L	H	L
↑	H	L	X	X	X	X	L	L	H	H
•	•	•		•				•		
•	•	•		•				•		
•	•	•		•				•		
↑	H	L	X	X	X	X	H	L	L	H
↑	H	L	X	X	X	X	L	L	L	L
↑	H	L	D1	D2	D3	D4	D4	D3	D2	D1


LOD
DATAIN1
DATAIN2
DATAIN3
DATAIN4
CL
RESET
LD
LDBAR
DECSEL
CLKBAR
CLK
RESET
D1OUT
D2OUT
D3OUT
D4OUT
D1BAR
D2BAR
D3BAR
D4BAR
IND1
IND2
IND3
NAO2
NAO3
END1
DFR3

Description

DEC3 Four Bit Decade Counter With CARRYIN and CARRYOUT

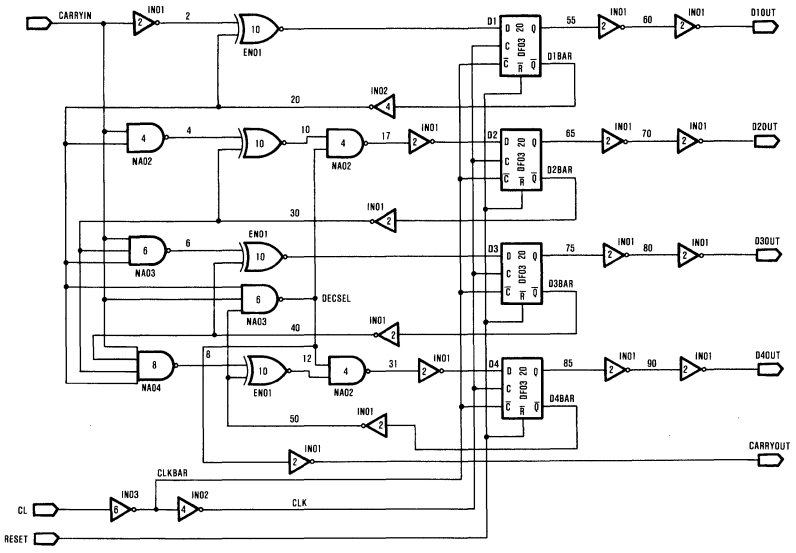
Equivalent Gate Count: 49

Functional Description

DEC3 is a four bit synchronous counter with asynchronous RESET, CARRYIN, and CARRYOUT. The counter consists of 4 D flip-flops with appropriate gate networks feeding the D inputs. When RESET and CARRYIN are high the output changes with the rising clock edge. This modulo 10 counter counts from 0-9 then resets to zero. On the 10th count, CARRYOUT becomes high for one cycle. When RESET is low, it overrides all other inputs, and outputs are set low. When RESET is high and CARRYIN is low, the output remains in its past state.

Truth Table

CLK	RESET	CARRYIN	CARRYOUT	D4OUT	D3OUT	D2OUT	D1OUT
X	L	X	L	L	L	L	L
↑	H	H	L	L	L	L	H
↑	H	H	L	L	L	H	L
↑	H	H	L	L	L	H	H
•	•	•			•		
•	•	•			•		
•	•	•			•		
↑	H	H	H	H	L	L	H
↑	H	L	L	H	L	L	H
↑	H	H	L	L	L	L	L
↑	H	L	L	Holds Previous State			


CARRYIN
IN01
2
10
EN01
D1
DFF03
55
IN01
60
IN01
D1OUT
D1BAR
20
IN02
4
4
NA02
10
10
4
NA02
17
IN01
D2
65
IN01
70
IN01
D2OUT
D2BAR
30
IN01
6
6
NA03
EN01
10
D3
75
IN01
80
IN01
D3OUT
D3BAR
6
NA03
DECSEL
40
IN01
8
8
NA04
10
EN01
12
4
NA02
31
IN01
D4
85
IN01
90
IN01
D4OUT
D4BAR
50
IN01
IN01
CARRYOUT
CLKBAR
CL
IN03
6
IN02
4
CLK
RESET

Description

DEC4 Four Bit Decade Counter with DIRECT LOAD, CARRYIN and CARRYOUT

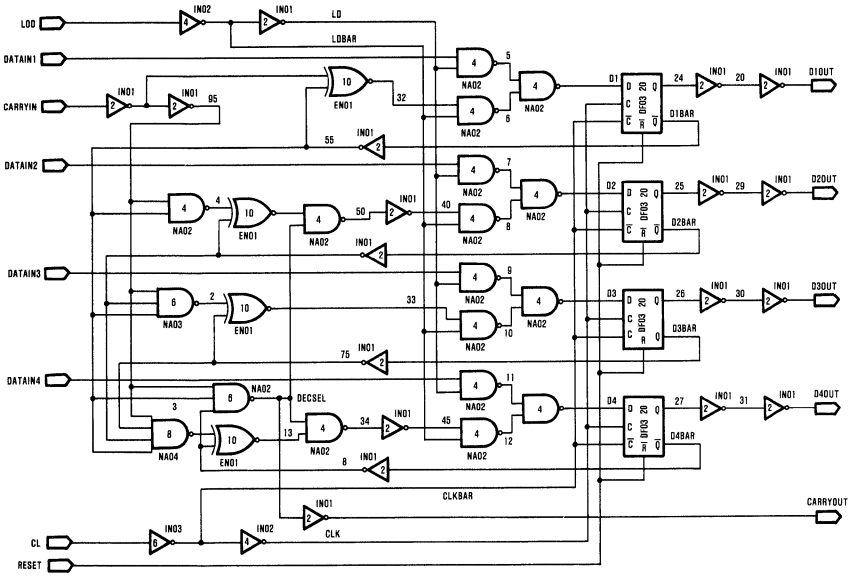
Equivalent Gate Count: 62

Functional Description

DEC4 is a four bit synchronous decade counter with asynchronous RESET, DIRECT LOAD (LOD), CARRYIN, and CARRYOUT. The counter consists of 4 D flip-flops with appropriate gate networks feeding into the D inputs. When RESET and CARRYIN are high and LOD is low, the output changes with the rising clock edge. The modulo 10 counter counts from 0-9 then resets to zero. On the 10th count CARRYOUT becomes high for one cycle. When RESET is low, it overrides all other inputs and outputs are set low. When RESET and LOD are high, data at inputs DATAIN1-DATAIN4 are loaded, with the rising clock edge, to the outputs D1OUT-D4OUT. When RESET is high, and CARRYIN and LOD are low, the output remains in its past state.

Truth Table

CLK	RESET	CARRYIN	LOD	DATAIN1	DATAIN2	DATAIN3	DATAIN4	CARRYOUT	D4OUT	D3OUT	D2OUT	D1OUT
X	L	X	X	X	X	X	X	L	L	L	L	L
↑	H	H	H	X	X	X	X	L	L	L	L	H
↑	H	H	H	X	X	X	X	L	L	L	H	L
↑	H	H	H	X	X	X	X	L	L	L	H	H
•	•	•	•		•					•		
•	•	•	•		•					•		
•	•	•	•		•					•		
↑	H	H	H	X	X	X	X	H	H	L	L	H
↑	H	L	H	X	X	X	X	L	H	L	L	H
↑	H	H	H	X	X	X	X	L	L	L	L	L
↑	H	L	H	X	X	X	X	L	Hold Previous State			
↑	H	H	L	D1	D2	D3	D4	—	D4	D3	D2	D1


LDD
DATAIN1
CARRYIN
DATAIN2
DATAIN3
DATAIN4
CL
RESET
LD
LDBAR
DECSEL
CLKBAR
CLK
CARRYOUT
D1BAR
D2BAR
D3BAR
D4BAR
D1OUT
D2OUT
D3OUT
D4OUT
INO1
INO2
INO3
NAO2
NAO3
NAO4
END1
DFG3

Description

UDB1 Four Bit Binary Up/Down Counter

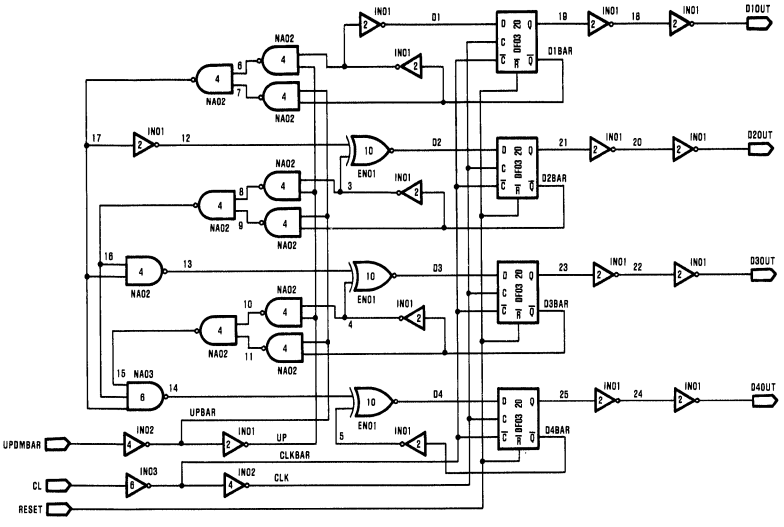
Equivalent Gate Count: 50

Functional Description

UDB1 is a four bit synchronous binary up/down counter with asynchronous RESET. This counter consists of 4 D flip-flops with appropriate gate networks feeding into the D inputs. When RESET is high the output changes with the rising clock edge. If UPDNBAR is high the output with will count forward and if UPDNBAR is low, the output will count backward. When RESET is low, it overrides all other inputs and outputs are set low.

Truth Table

CL	RESET	UPDNBAR	D40UT	D30UT	D20UT	D10UT
X	L	X	L	L	L	L
↑	H	L	H	H	H	H
↑	H	L	H	H	H	L
↑	H	L	H	H	L	H
↑	H	L	H	H	L	L
•	•	•		•		
•	•	•		•		
•	•	•		•		
↑	H	L	L	L	L	L
↑	H	L	H	H	H	H
↑	H	H	L	L	L	L
↑	H	H	L	L	L	H
↑	H	H	L	L	H	L
•	•	•		•		
•	•	•		•		
•	•	•		•		
↑	H	H	H	H	H	H
↑	H	H	L	L	L	L


INO1
D1
DFF03
D1BAR
D1OUT
NAO2
D2
D2BAR
D2OUT
D3
D3BAR
D3OUT
NAO3
D4
D4BAR
D4OUT
UPBAR
UPDMBAR
IN02
UP
CLKBAR
CL
IN03
CLK
RESET

Description

UDB2 Four Bit Binary Up/Down Counter With DIRECT LOAD

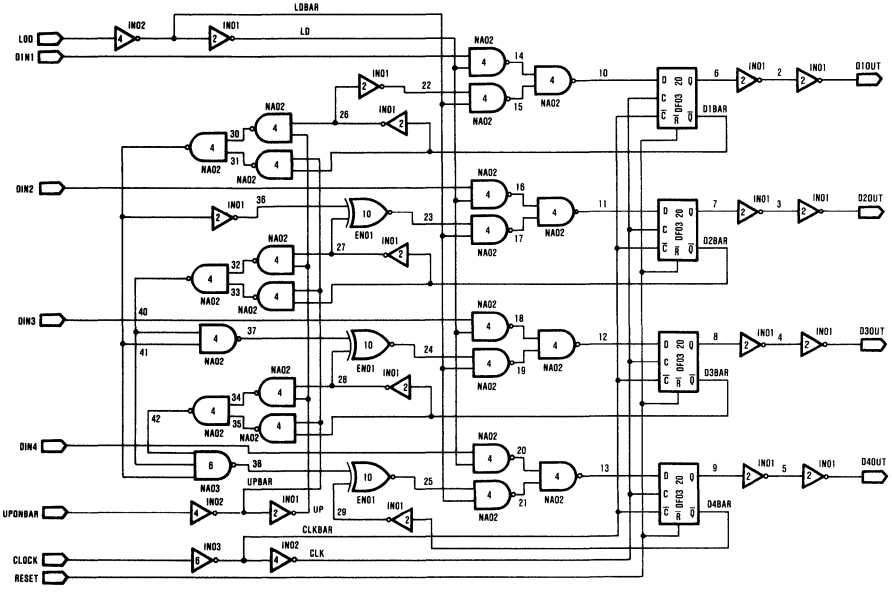
Equivalent Gate Count: 63

Functional Description

UDB2 is a four bit synchronous binary up/down counter with asynchronous RESET and DIRECT LOAD (LOD). This counter consists of 4 D flip-flops with appropriate gate networks feeding into the D inputs. When RESET is high and LOD is low, the output will count backwards. When RESET is low, it overrides all other inputs and outputs are set low. When RESET and LOD are high, data at inputs DIN1-DIN4 are loaded to the outputs D1OUT-D4OUT. If LOD is made low before the next clock cycle, the output will start counting forward or backward (depending on the state of UPDNBAR) from the number which was loaded.

Truth Table

CL	RESET	LOD	UPDNBAR	DIN4	DIN3	DIN2	DIN1	D4OUT	D3OUT	D2OUT	D1OUT
X	L	X	X	X	X	X	X	L	L	L	L
↑	H	L	L	X	X	X	X	H	H	H	H
↑	H	L	L	X	X	X	X	H	H	H	L
↑	H	L	L	X	X	X	X	H	H	L	H
↑	H	L	L	X	X	X	X	H	H	L	L
•	•	•			•					•	
•	•	•			•					•	
•	•	•			•					•	
↑	H	L	L	X	X	X	X	L	L	L	L
↑	H	L	L	X	X	X	X	H	H	H	H
↑	H	L	H	X	X	X	X	L	L	L	L
↑	H	L	H	X	X	X	X	L	L	L	H
↑	H	L	H	X	X	X	X	L	L	H	L
•	•	•	•		•					•	
•	•	•	•		•					•	
•	•	•	•		•					•	
↑	H	L	H	X	X	X	X	H	H	H	H
↑	H	L	H	X	X	X	X	L	L	L	L
↑	H	H	H	D4	D2	D2	D1	D4	D3	D2	D1


LDBAR
LOD
DIN1
DIN2
DIN3
DIN4
UPDNBAR
CLOCK
RESET
LD
UPBAR
UP
CLKBAR
CLK
D1BAR
D2BAR
D3BAR
D4BAR
D1OUT
D2OUT
D3OUT
D4OUT
INO1
INO2
INO3
NAO2
NAO3
END1
DFF3

Description

UDB3 Four Bit Binary Up/Down Counter With CARRYIN and CARRYOUT

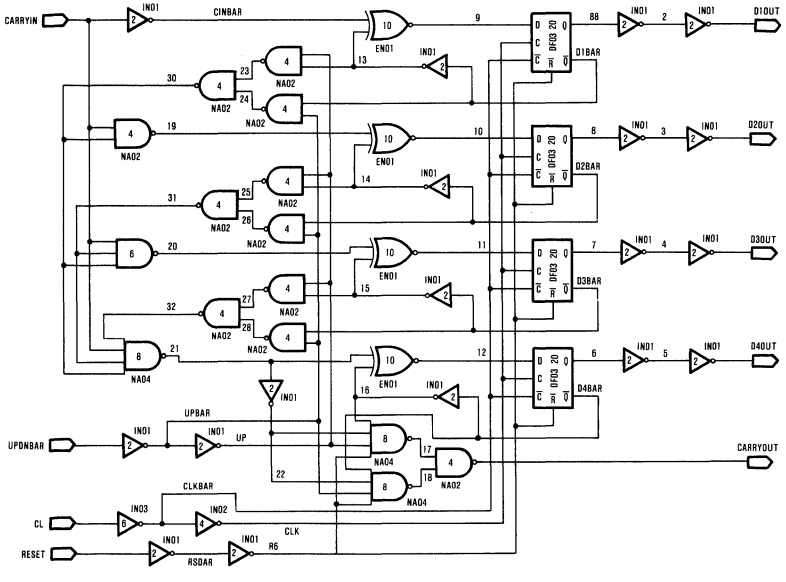
Equivalent Gate Count: 70

Functional Description

UDB3 is a four bit synchronous binary up/down counter with asynchronous RESET, CARRYIN, and CARRYOUT. This counter consists of 4 D flip-flops with appropriate gate networks feeding into the D inputs. When RESET and CARRYIN are high, the outputs change with the rising clock edge. If UPDNBAR is high, the output will count forward and if UPDNBAR is low, the output will count backward. When RESET is low, it overrides all other inputs and the outputs are set low. When RESET is high and CARRYIN is low, the output remains in past state.

Truth Table

CL	RESET	CARRYIN	UPDNBAR	CARRYOUT	D40UT	D30UT	D20UT	D10UT
X	L	X	X	L	L	L	L	L
↑	H	H	L	L	H	H	H	H
↑	H	H	L	L	H	H	L	H
↑	H	H	L	L	H	H	L	L
•	•	•	•		•			
•	•	•	•		•			
•	•	•	•		•			
↑	H	H	L	H	L	L	L	L
↑	H	L	L	L	L	L	L	L
↑	H	H	L	L	H	H	H	H
↑	H	H	L	L	H	H	H	L
↑	H	H	H	H	H	H	H	H
↑	H	L	H	L	H	H	H	H
↑	H	H	H	L	L	L	L	L
↑	H	H	H	L	L	L	L	H
↑	H	H	H	L	L	L	H	L


CARRYIN
CINBAR
UPDNBAR
UPBAR
UP
CLKBAR
CL
CLK
RESET
RSDAR
R6
CARRYOUT
D1OUT
D2OUT
D3OUT
D4OUT
D1BAR
D2BAR
D3BAR
D4BAR
IND1
IND2
IND3
NAO2
NAO4
NAD4
ENO1
DF03
DF02
DF01
DF00

Description

UDB4 Four Bit Binary Up/Down Counter with DIRECT LOAD, CARRYIN and CARRYOUT

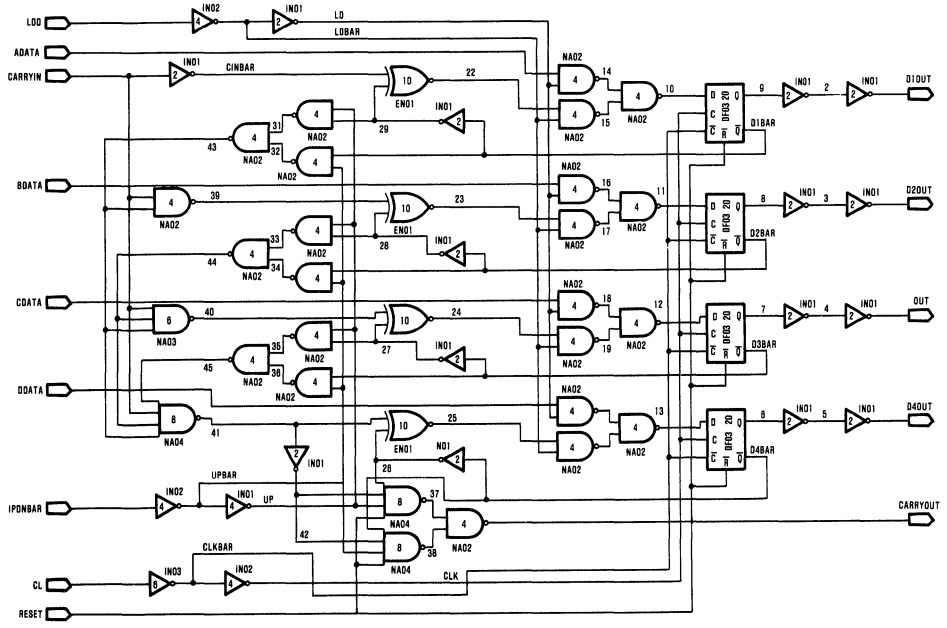
Equivalent Gate Count: 73

Functional Description

UDB4 is a four bit synchronous binary up/down counter with asynchronous RESET, DIRECT LOAD (LOD), CARRY-IN, and CARRYOUT. This counter consists of 4 D flip-flops with appropriate gate networks feeding into the D inputs. When RESET and CARRYIN are high and LOD is low, the output changes with the rising edge of the clock. If UPDNBAR is high, the output counts forward, and if UPDNBAR is low, the output counts backward. CARRYOUT becomes high for one cycle when all outputs are high (16th forward count). When RESET is low it overrides all other inputs, and the outputs are set low. When RESET and LOD are high, data at inputs ADATA-DDATA are loaded, with the rising clock edge, to the outputs D1OUT-D4OUT. If LOD is made low before the next clock cycle, the output will start counting forward or backward (depending on the state of UPDNBAR) from the number which was loaded. When CARRYIN and LOD are low, and RESET is high, the output remains in its past state.

Truth Table

CLK	RESET	CARRYIN	LOD	UPDNBAR	DDATA	CDATA	BDATA	ADATA	CARRYOUT	D4OUT	D3OUT	D2OUT	D1OUT
X	L	X	X	X	X	X	X	X	L	L	L	L	L
↑	H	H	L	L	X	X	X	X	L	H	H	H	H
↑	H	H	L	L	X	X	X	X	L	H	H	H	L
↑	H	H	L	L	X	X	X	X	L	H	H	L	H
↑	H	H	L	L	X	X	X	X	L	H	H	L	L
•	•	•	•	•							•		
•	•	•	•	•							•		
•	•	•	•	•							•		
↑	H	H	L	L	X	X	X	X	H	L	L	L	L
↑	H	L	L	L	X	X	X	X	L	L	L	L	L
↑	H	H	L	L	X	X	X	X	L	H	H	H	H
↑	H	H	L	L	X	X	X	X	L	H	H	H	L
↑	H	H	L	H	X	X	X	X	H	H	H	H	H
↑	H	L	L	H	X	X	X	X	L	H	H	H	H
↑	H	H	L	H	X	X	X	X	L	L	L	L	L
↑	H	H	L	H	X	X	X	X	L	L	L	L	H
↑	H	H	L	H	X	X	X	X	L	L	L	H	L
↑	H	H	H	H	D4	D3	D2	D1	—	D4	D3	D2	D1


LOD
ADATA
CARRYIN
BDATA
CDATA
DDATA
IPDNBAR
CL
RESET
CLKBAR
UPBAR
CINBAR
LD
LDBAR
UP
CLK
CARRYOUT
D1OUT
D2OUT
OUT
D4OUT
D1BAR
D2BAR
D3BAR
D4BAR
INO1
INO2
INO3
NAO2
NAO3
NAO4
ENO1
NO1
DFD3

Description

UDD1 Four Bit Up/Down Decade Counter

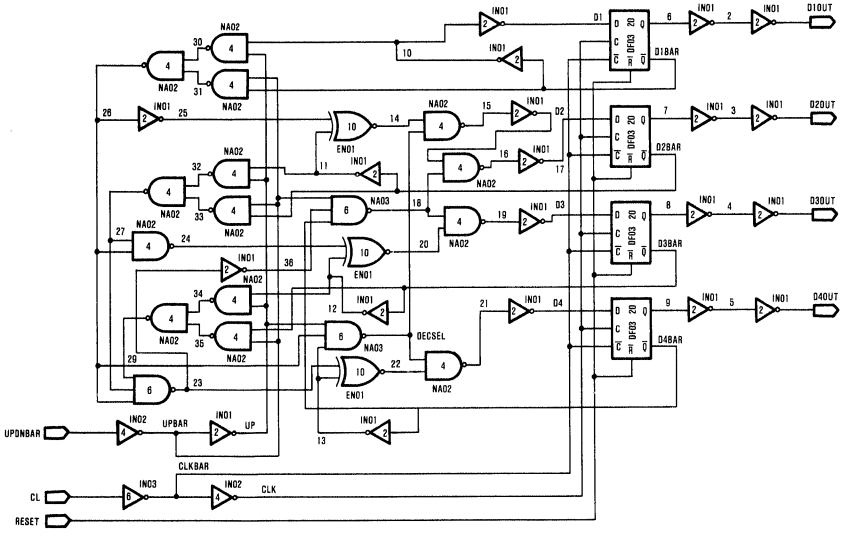
Equivalent Gate Count: 65

Functional Description

UDD1 is a four bit synchronous binary up/down decade counter with asynchronous RESET. This counter consists of 4 D flip-flops with appropriate gate networks feeding into the D inputs. When RESET is high, the output changes with the rising clock edge. If UPDNBAR is high, the output with will count forward and if UPDNBAR is low, the output will count backward. This modulo 10 counter counts from 0-9 (or 9-0) then resets to zero. When RESET is low, it overrides all other inputs and the outputs are set low.

Truth Table

CLK	RESET	UPDNBAR	D40UT	D30UT	D20UT	D10UT
X	L	X	L	L	L	L
↑	H	H	L	L	L	H
↑	H	H	L	L	H	L
↑	H	H	L	L	H	H
	•			•		
	•			•		
	•			•		
↑	H	H	H	L	L	H
↑	H	H	L	L	L	L
↑	H	L	H	L	L	H
↑	H	L	H	L	L	L
	•			•		
	•			•		
	•			•		
↑	H	L	L	L	L	L


INO1
NAO2
NAO3
ENO1
DFE3
D1
D2
D3
D4
D1BAR
D2BAR
D3BAR
D4BAR
D1OUT
D2OUT
D3OUT
D4OUT
DECSEL
UPDNBAR
UPBAR
UP
CLKBAR
CL
RESET
INO2
INO3
CLK

Description

UDD2 Four Bit Up/Down Decade Counter With DIRECT LOAD

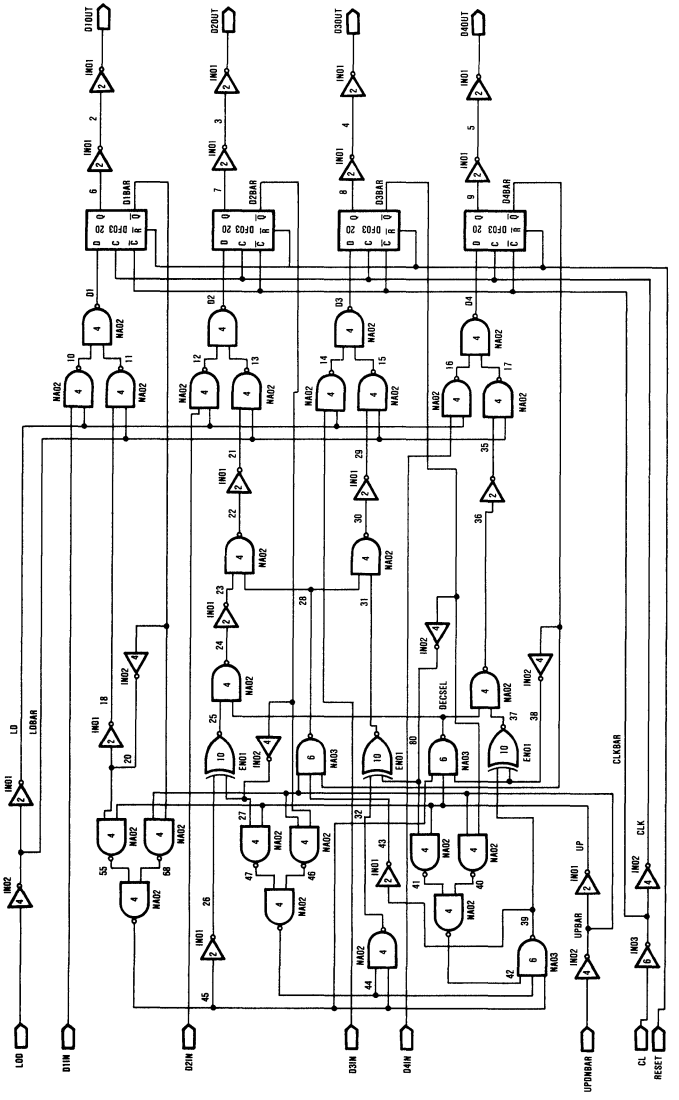
Equivalent Gate Count: 75

Functional Description

UDD2 is a four bit synchronous up/down counter with asynchronous RESET and DIRECT LOAD (LOD). This counter consists of 4 D flip-flops with appropriate gate networks feeding into the D inputs. When RESET is high and LOD is low, the output changes with the rising clock edge. If UPDNBAR is high, the output counts forward and if UPDNBAR is low, the output counts backward. This modulo 10 counter counts from 0-9 (or 9-0) then resets to zero. When RESET is low, it overrides all other inputs and outputs are set low. When RESET and LOD are high, data at inputs D1IN-D4IN is loaded to the outputs D1OUT-D4OUT. If LOD is made low before the next cycle, the counter will start counting forward or backward (depending on the state of UPDNBAR) from the loaded number.

Truth Table

CL	RESET	LOD	UPDNBAR	D4IN	D3IN	D2IN	D1IN	D4OUT	D3OUT	D2OUT	D1OUT
X	L	X	X	X	X	X	X	L	L	L	L
↑	H	L	H	X	X	X	X	L	L	L	H
↑	H	L	H	X	X	X	X	L	L	H	L
↑	H	L	H	X	X	X	X	L	L	H	H
	•								•		
	•								•		
	•								•		
↑	H	L	H	X	X	X	X	H	L	L	H
↑	H	L	L	X	X	X	X	L	L	L	L
↑	H	L	L	X	X	X	X	H	L	L	H
↑	H	L	L	X	X	X	X	H	L	L	L
	•								•		
	•								•		
	•								•		
↑	H	L	L	X	X	X	X	L	L	L	L
↑	H	H	X	D4	D3	D2	D1	D4	D3	D2	D1


D1OUT
D2OUT
D3OUT
D4OUT
D1BAR
D2BAR
D3BAR
D4BAR
DFD3 20
LD
LDBAR
RECSEL
CLKBAR
UP
UPBAR
CLK
LOD
D1IN
D2IN
D3IN
D4IN
UPDNBAR
CL
RESET

Description

UDD3 Four Bit Up/Down Decade Counter With CARRYIN and CARRYOUT

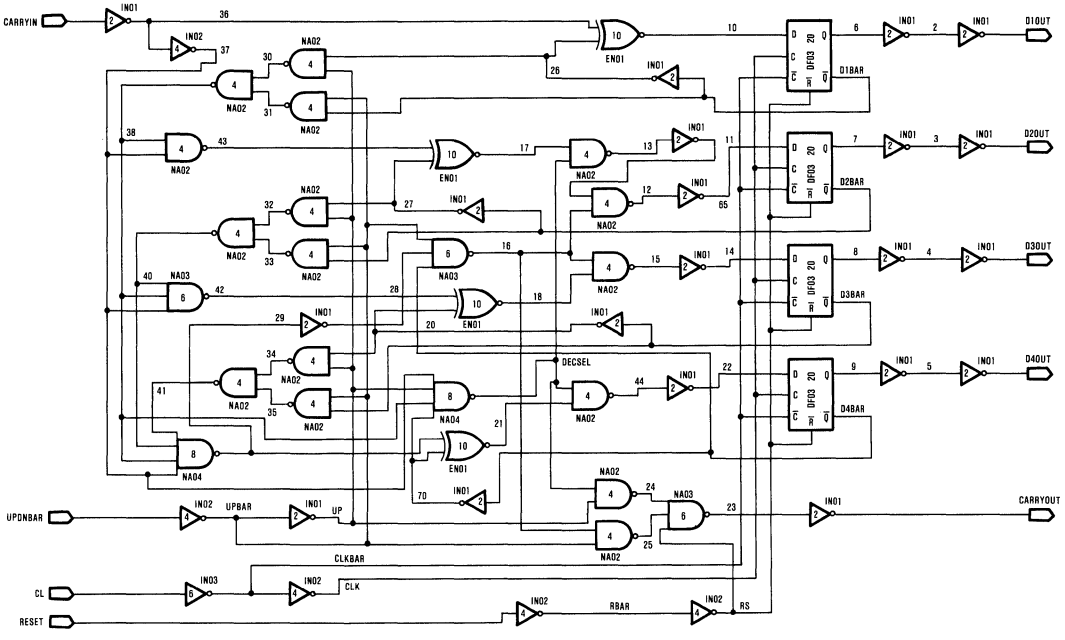
Equivalent Gate Count: 71

Functional Description

UDD3 is a four bit synchronous up/down decade counter with asynchronous RESET, CARRYIN, and CARRYOUT. This counter consists of 4 D flip-flops with appropriate gate networks feeding the D inputs. When RESET and CARRYIN are high, outputs change with the rising clock edge. If UPDNBAR is high the output counts forward and if UPDNBAR is low, the output counts backward. This modulo 10 counter counts from 0-9 (or 9-0) then resets to zero. CARRYOUT becomes high for one clock cycle when the output reads 9 (10th count). When RESET is low, it overrides all other inputs and the outputs are set low. When RESET is high and CARRYIN is low, the output remains in its past state.

Truth Table

CL	RESET	UPDNBAR	CARRYIN	CARRYOUT	D40UT	D30UT	D20UT	D10UT
X	L	X	X	L	L	L	L	L
↑	H	H	H	L	L	L	L	H
↑	H	H	H	L	L	L	H	L
↑	H	H	H	L	L	L	H	H
•	•	•	•			•		
•	•	•	•			•		
•	•	•	•			•		
↑	H	H	H	H	H	L	L	H
↑	H	H	L	L	H	L	L	H
↑	H	H	H	L	L	L	L	L
↑	H	H	H	L	L	L	L	H
↑	H	L	H	H	L	L	L	L
↑	H	L	L	L	L	L	L	L
↑	H	L	H	L	H	L	L	H
↑	H	L	H	L	H	L	L	L


CARRYIN
UPDNBAR
CL
RESET
CLKBAR
UPBAR
UP
CLK
RBAR
RS
DECSEL
CARRYOUT
D1OUT
D2OUT
D3OUT
D4OUT
D1BAR
D2BAR
D3BAR
D4BAR
INO1
INO2
INO3
NAO2
NAO3
NAO4
ENO1
UFD3

Description

UDD4 Four Bit Up/Down Decade Counter with DIRECT LOAD, CARRYIN and CARRYOUT

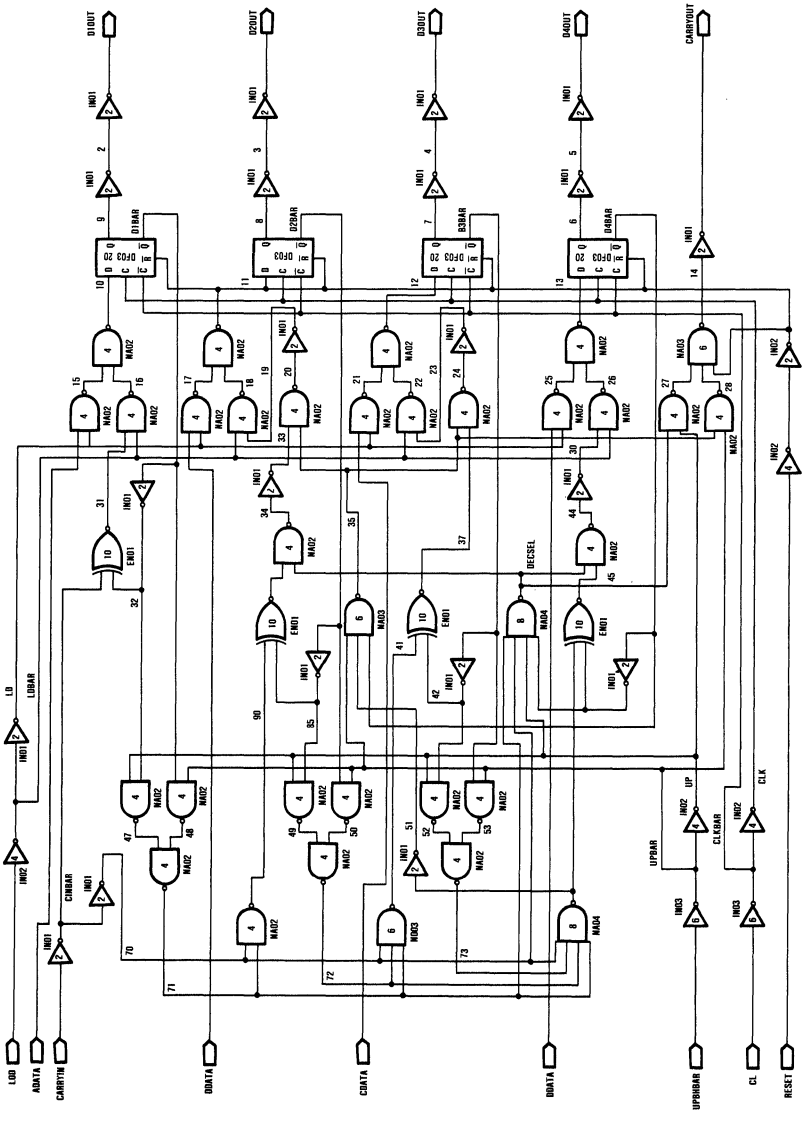
Equivalent Gate Count: 85

Functional Description

UDD4 is a four bit synchronous up/down decade counter with asynchronous RESET, DIRECT LOAD (LOD), CARRY-IN, and CARRYOUT. This counter consists of 4 D flip-flops with appropriate gate networks feeding into the D inputs. When RESET and CARRYIN are high and LOD is low, the output changes with the rising clock edge. If UPDNBAR is high, the output will count forward, and if UPDNBAR is low, the output will count backward. This modulo 10 counter counts 0-9 (or 9-0) then resets to zero. CARRYOUT become high for one cycle when the output reads 9 (10th count). When RESET is low it overrides all other inputs and the outputs are set low. When RESET is high and CARRYIN is low, the output remains in its past state. When RESET and LOD are high, data at inputs ADATA-DDATA are loaded to outputs D1OUT-D4OUT. If LOD is made low before the next cycle, the output will start counting forward or backward (depending on the state of UPDNBAR) from the number loaded.

Truth Table

CLK	RESET	UPDNBAR	LOD	CARRYIN	DDATA	CDATA	BDATA	ADATA	CARRYOUT	D4OUT	D3OUT	D2OUT	D1OUT
X	L	X	X	X	X	X	X	X	L	L	L	L	L
↑	H	H	L	H	X	X	X	X	L	L	L	L	H
↑	H	H	L	H	X	X	X	X	L	L	L	H	L
↑	H	H	L	H	X	X	X	X	L	L	L	H	H
•	•	•	•	•		•					•		
•	•	•	•	•		•					•		
•	•	•	•	•		•					•		
↑	H	H	L	H	X	X	X	X	H	H	L	L	H
↑	H	H	L	L	X	X	X	X	L	H	L	L	H
↑	H	H	L	H	X	X	X	X	L	L	L	L	L
↑	H	H	L	H	X	X	X	X	L	L	L	L	H
↑	H	L	L	H	X	X	X	X	H	L	L	L	L
↑	H	L	L	L	X	X	X	X	L	L	L	L	L
↑	H	L	L	H	X	X	X	X	L	H	L	L	H
↑	H	L	L	H	X	X	X	X	L	H	L	L	L
↑	H	X	H	X	D4	D3	D2	D1	L	D4	D3	D2	D1


D1OUT
D2OUT
D3OUT
D4OUT
CARRYOUT
D1BAR
D2BAR
D3BAR
D4BAR
DECSEL
LD
LDBAR
CINBAR
UP
UPBAR
CLKBAR
CLK
LOD
ADATA
CARRYIN
BDATA
CDATA
DDATA
UPBNBAR
CL
RESET

SCA 10G138

Description

3 to 8 Decoder

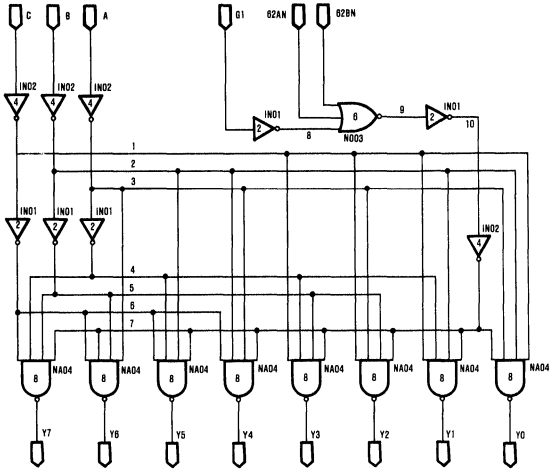
Equivalent Gate Count: 24

Functional Description

The 10G138 is a 3 to 8 Decoder/Demultiplexer with three enable inputs. When G1 is high, GZAN and G2BN are low; one of the outputs (Y0-Y7) will be low, depending on the states of A, B, and C. If GZAN or G2BN are high, or if G1 is low, all outputs will be high.

Truth Table

G A Z N	G 2 B N	G 1	A	B	C	Y 0	Y 1	Y 2	Y 3	Y 4	Y 5	Y 6	Y 7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L


C
B
A
G1
G2AN
G2BN
IN02
IN01
NO03
NA04
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0

SCA 10G139

Description

2 to 4 Decoder

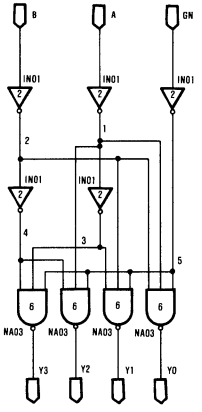
Equivalent Gate Count: 8

Functional Description

The 10G139 is a 2 to 4 Decoder with active low enable. When GN is low, one of the outputs (Y0-Y3) will be low, depending on the state of A and B. When GN is high, all outputs are high.

Truth Table

GN	A	B	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L


B
A
GN
IN01
IN01
IN01
2
1
2
IN01
IN01
4
3
5
6
6
6
6
NA03
NA03
NA03
NA03
Y3
Y2
Y1
Y0

Description

8 to 3 Priority Encoder

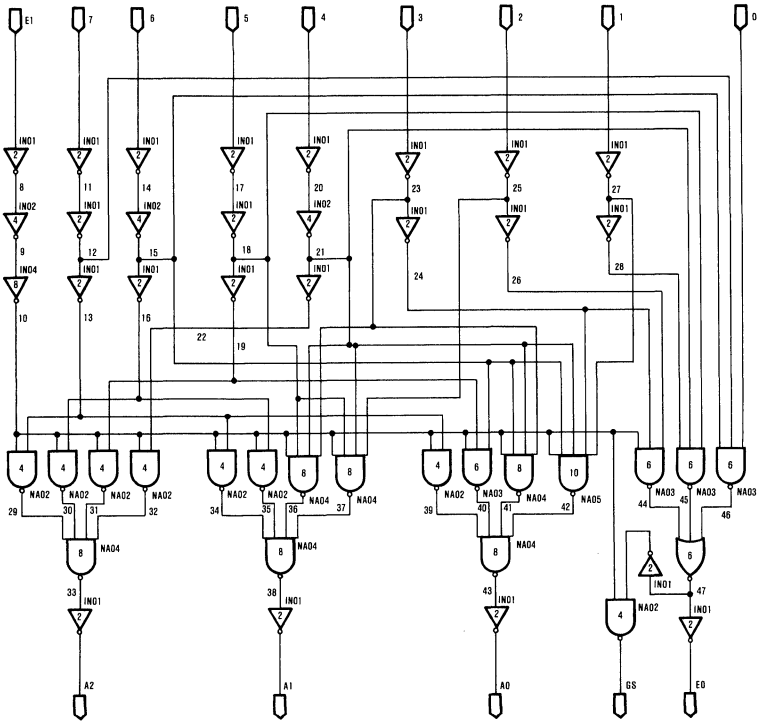
Equivalent Gate Count: 46

Functional Description

The 10G148 is an 8 to 3 Priority Encoder with Enable input and Enable output for cascading purposes. The GS (Group Signal) is active low when any of the inputs are low. It serves to indicate when any of the inputs are active. When EI is high, all outputs are high and when EI is low, the outputs depend on the states of inputs 0-7, as indicated in the table.

Truth Table

E									A	A	A	G	E
I	0	1	2	3	4	5	6	7	2	1	0	S	0
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H


E1
7
6
5
4
3
2
1
0
IND1
IND2
IND4
NAO2
NAO3
NAO4
NAO5
A2
A1
A0
GS
EO

Description

4 to 16 Decoder

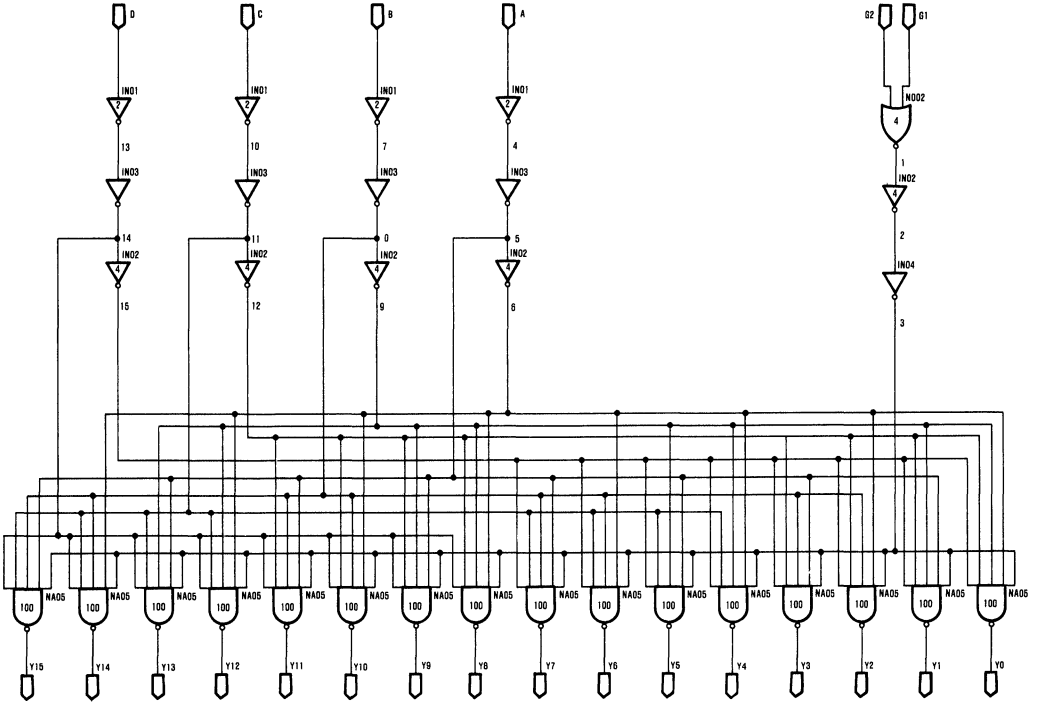
Equivalent Gate Count: 56

Functional Description

The 10G154 is a 4 to 16 Decoder with two active low enable inputs. When G1 and G2 are low, one of the outputs (Y1-Y16) will be low, depending on the state of A, B, C, and D. When G1 and/or G2 are high, all outputs are high.

Truth Table

G1	G2	A	B	C	D	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H


D
C
B
A
G2
G1
IN01
IN02
IN03
IN04
NO02
NA05
100
Y15
Y14
Y13
Y12
Y11
Y10
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0

Description

8 Bit Serial-in Parallel-out Shift Register

Equivalent Gate Count: 55

Functional Description

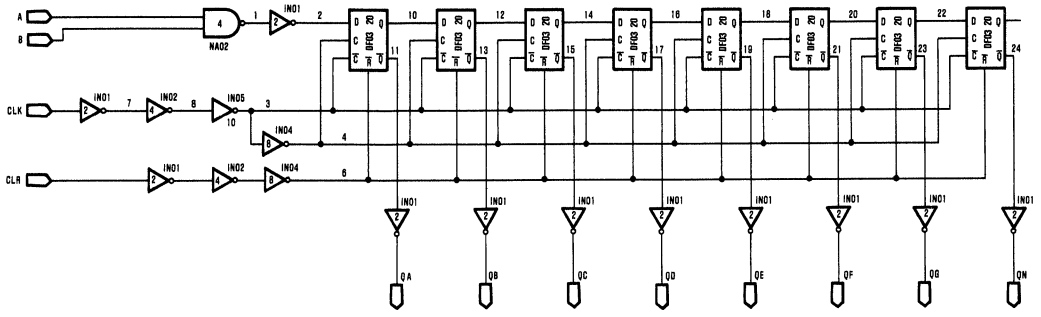
The 10G164 is a Serial-in Parallel-out 8 Bit Synchronous Shift Register with Asynchronous CLR. Data can be entered through A or B, and outputs can be taken at all 8 stages. When CLR is high, each rising clock edge shifts data right, and enters the logical AND of A + B into QA. When CLR is low, it overrides all other inputs and outputs are set low.

Truth Table

CLR	CLK	A	B	QA	QB	QH
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	↑	H	H	H	QAN	QGN
H	↑	L	X	L	QAN	QGN
H	↑	X	L	L	QAN	QGN

QA0, QB0, QH0 = Level of QA, QB, QH before the indicated steady-state input conditions were established

QAN, QGN = Level of QA or QG before the most recent transition of the clock; indicates a one-bit shift


A
B
NA02
IN01
CLK
IN02
IN05
IN04
CLR
DFR3
QA
QB
QC
QD
QE
QF
QG
QH

Description

8 Bit Parallel/Serial-in Serial-out Shift Register

Equivalent Gate Count: 78

Functional Description

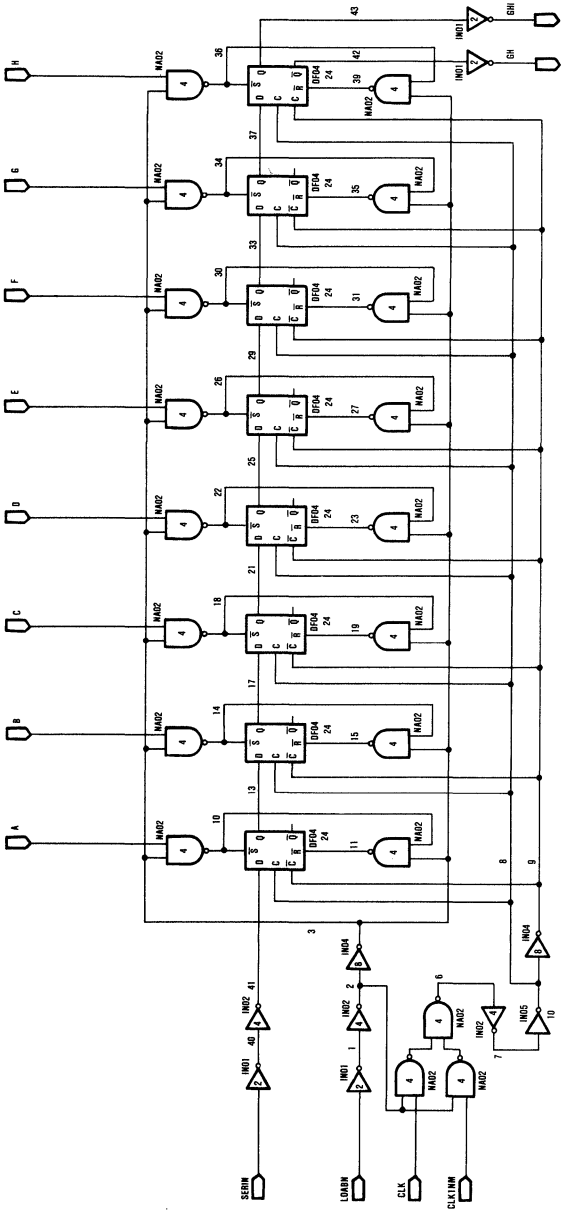
The 10G165 is an 8 Bit Synchronous Parallel or Serial-in/Serial-out Shift Register. Parallel inputing occurs asynchronously when LOADN is low. When LOADN is high, serial shifting to output QH occurs on the rising edge of the clock, and new data enters serially via SERIN. The 2 input OR clock can be used to combine two clock sources or one input can act as a single clock.

Truth Table

LOADN	CLKINH	CLK	SERIN	A . . . H	INTERNAL OUTPUTS QA	QB	OUTPUT QH
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	QA0	QB0	QH0
H	L	↑	H	X	H	QAN	QGN
H	L	↑	L	X	L	QAN	QGN
H	H	X	X	X	QA0	QB0	QH0

QA0, QB0, QH0 = Level of QA, QB, QH before the indicated steady-state input conditions were established

QAN, QGN = Level of QA or QG before the most recent transition of the clock; indicates a one-bit shift


H
G
F
E
D
C
B
A
NAD2
DFD4
INV1
INV2
INV4
INV5
GHH
GH
SERIN
LOADN
CLK
CLKINN

Description

8 Bit Parallel/Serial-in Serial-out Shift Register

Equivalent Gate Count: 80

Functional Description

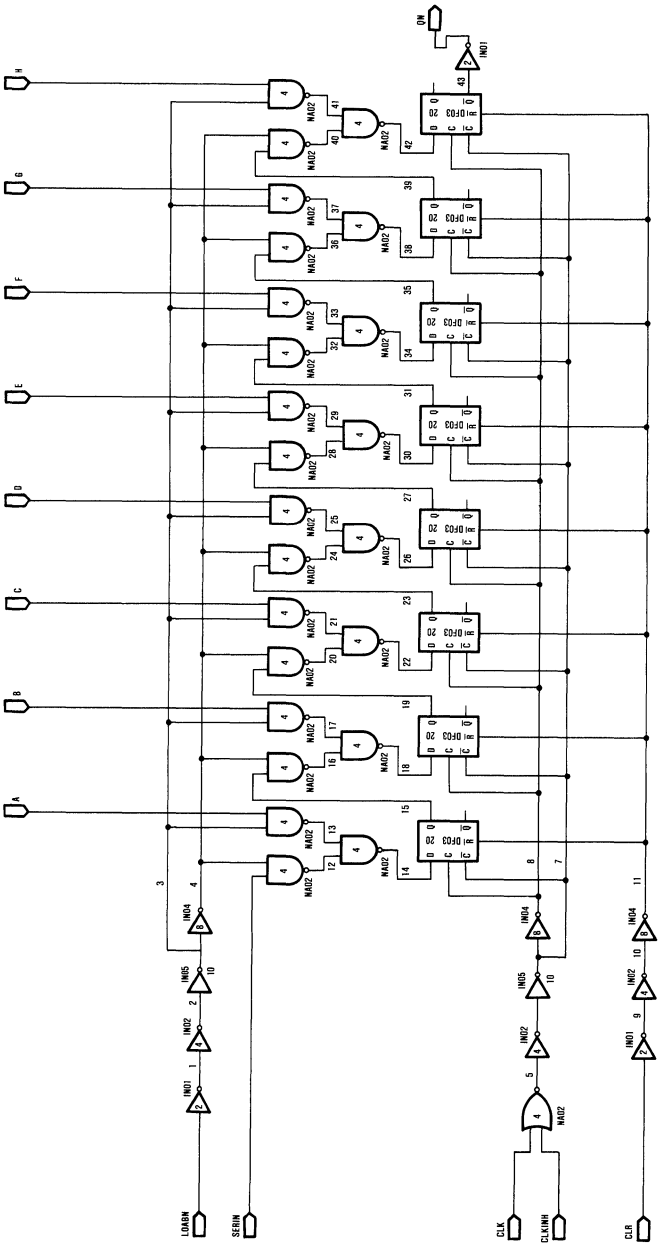
The 10G166 is an 8 Bit Synchronous Parallel/Serial-input Serial-output Shift Register with reset. Parallel inputing at inputs A-H occurs asynchronously when LOADN is low. When LOADN is high, serial shifting to output QH occurs on the rising edge of the clock, and new data enters serially via SERIN. The 2 input OR clock can be used to combine two clock sources, or by holding one input low, can be used as a single clock source. When CLR is high, all outputs are set low.

Truth Table

CLR	LOADN	CLKINH	CLK	SERIN	PARALLEL A...H	INTERNAL OUTPUTS QA	INTERNAL OUTPUTS QB	OUTPUT QH
H	X	X	X	X	X	L	L	L
L	X	L	L	X	X	QA0	QB0	QH0
L	L	L	↑	X	a...h	a	b	h
L	H	L	↑	H	X	H	QAN	QGN
L	H	L	↑	L	X	L	QAN	QGN
L	X	H	↑	X	X	QA0	QB0	QH0

QA0, QB0, QH0 = Level of QA, QB, QH before the indicated steady-state input conditions were established

QAN, QGN = Level of QA or QG before the most recent transition of the clock; indicates a one-bit shift


QW
INV1
H
G
F
E
D
C
B
A
NAN2
OFD3
INV4
INV5
INV2
INV1
NAN2
LOADN
SERIN
CLK
CLKINH
CLR

SCA 10G182

Description

Carry Lookahead Generator

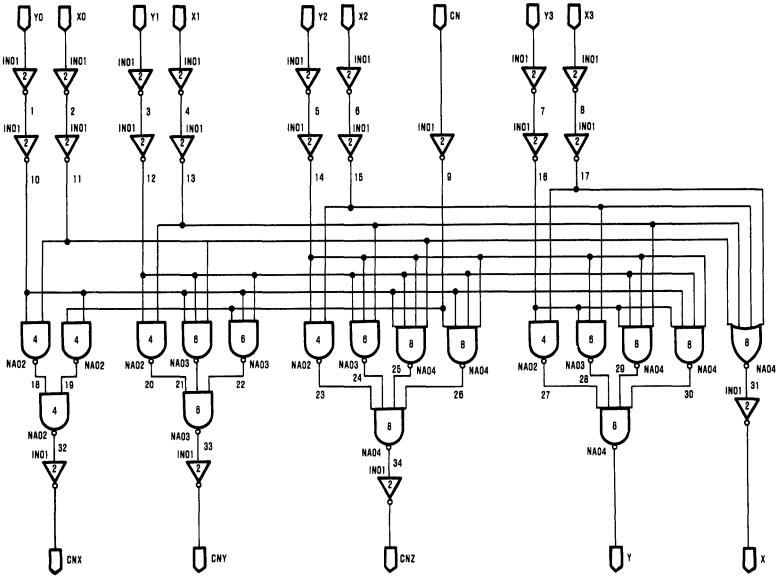
Equivalent Gate Count: 38

Functional Description

The 10G182 is a Carry Lookahead Generator. It is generally used with the 10G181 4-bit ALU to provide high speed lookahead over word length of more than four bits. It accepts up to four pairs of Carry Propagate (X0-X3) and Carry Generate (Y0-Y3) signals, with active high Carryin (CN). It provides anticipated active high carries (CNX-CNZ) and has Carry Propagate (X) and Generate (Y) outputs. The logic operations provided at outputs are:

Truth Table

CN	Y0	X0	Y1	X1	Y2	X2	Y3	X3	CNX	CNY	CNZ	X	Y
X	L	X							H				
H	X	L							H				
			All Other Combinations						L				
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
			All Other Combinations							L			
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
			All Other Combinations								L		
	L		L		L		L					L	
			All Other Combinations									H	
	X		X	X	X	X	L	X					L
	X		X	X	L	X	X	L					L
	X		L	X	X	L	X	L					L
	L		X	L	X	L	X	L					L
			All Other Combinations										H


Y0
X0
Y1
X1
Y2
X2
CN
Y3
X3
IND1
NAO2
NAO3
NAO4
CNX
CNY
CNZ
Y
X

Description

4 Bit Bidirectional Universal Shift Register

Equivalent Gate Count: 65

Functional Description

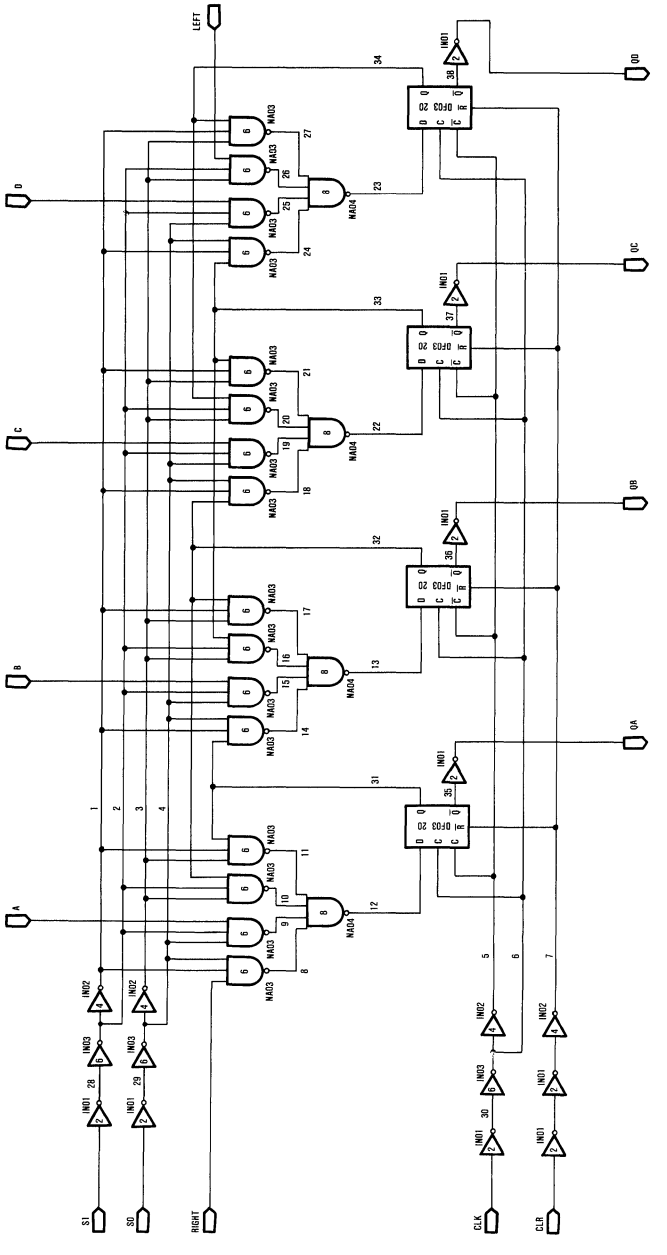
The 10G194 is a 4 Bit Synchronous Bidirectional Universal Shift Register with clear. This shift register consists of 4 D flip-flops and appropriate gate networks feeding into the D inputs. It may be used in Serial-Serial, Shift Left, Shift Right, Serial-Parallel, Parallel-Serial, and Parallel-Parallel shift register applications. When S1 and S0 are both low, the outputs remain in their past states, and when S0 and S1 are both high, inputs A-D are parallel loaded asynchronously. When S0 is low and S1 is high, data is shifted left and data at input LEFT are shifted into Q3 with the rising clock edge. Similarly, when S0 is high and S1 is low, data are shifted right, and data at input RIGHT are shifted into Q1. When CLR is low, it overrides all other inputs and outputs are set low.

Truth Table

CLR	S1	S0	CLK	LEFT	RIGHT	A	B	C	D	QA	QB	QC	QC
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAN	QBN	QCN
H	L	H	↑	X	L	X	X	X	X	L	QAN	QBN	QCN
H	H	L	↑	H	X	X	X	X	X	QBN	QCN	QDN	H
H	H	L	↑	L	X	X	X	X	X	QBN	QCN	QDN	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

QA0, QB0, QH0 = Level of QA, QB, QH before the indicated steady-state input conditions were established

QAN, QGN = Level of QA or QG before the most recent transition of the clock; indicates a one-bit shift


LEFT
RIGHT
A
B
C
D
S1
S0
CLK
CLR
QA
QB
QC
QD
NAD3
NAD4
IND1
IND2
IND3
OFD3 20

Description

4 Bit Synchronous Universal Shift Register

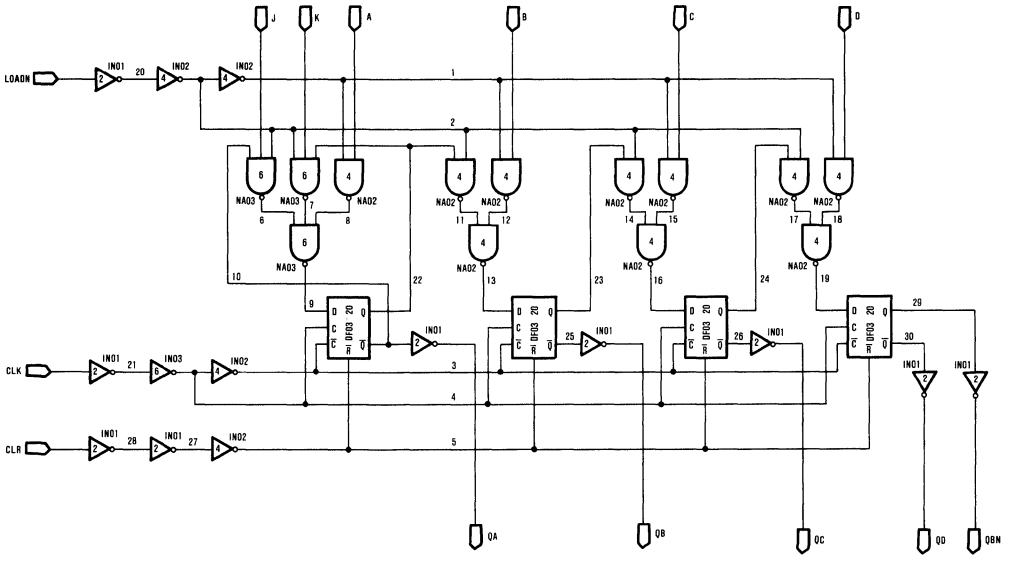
Equivalent Gate Count: 44

Functional Description

The 10G195 is a 4 Bit Synchronous Universal Shift Register with reset. It consists of 4 D flip-flops with appropriate gate networks feeding the D inputs. It may be used in Serial-Serial, Serial-Parallel, Parallel-Serial, and Parallel-Parallel shift register applications. When LOADN is low, data at inputs A-D are loaded into the D Flip-Flops. When LOADN is high, data enters the first flip-flop QA via the JK inputs, and is shifted RIGHT with the rising clock edge. The JK inputs may be tied together for D-type inputs. When CLR is low, it overrides all other inputs and outputs are set low.

Truth Table

CLR	LOADN	CLK	J	K	A	B	C	D	QA	QB	QC	QD	QDN
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0	$\overline{Q}$D0
H	H	↑	L	H	X	X	X	X	QA0	QA0	QBN	QCN	$\overline{Q}$CN
H	H	↑	L	L	X	X	X	X	L	QAN	QBN	QCN	$\overline{Q}$CN
H	H	↑	H	H	X	X	X	X	H	QAN	QBN	QCN	$\overline{Q}$CN
H	H	↑	H	L	X	X	X	X	$\overline{Q}$AN	QAN	QBN	QCN	$\overline{Q}$CN


J
K
A
B
C
D
LOADN
CLK
CLR
INO1
INO2
INO3
NAO3
NAO2
DF03
QA
QB
QC
QD
QBN

Description

8 Bit Universal Shift Register

Equivalent Gate Count: 83

Functional Description

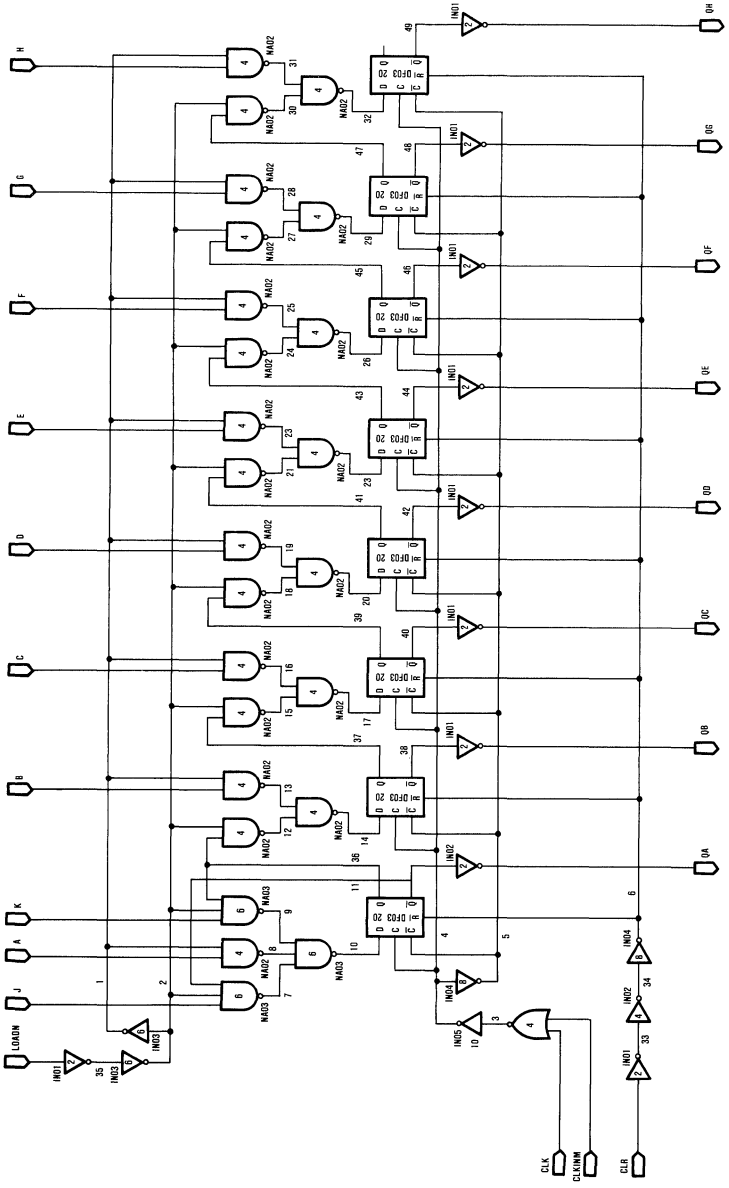
The 10G199 is an 8 Bit Synchronous Universal Shift Register with active high reset. This register consists of 4 D flip-flops with appropriate gates feeding into the D inputs. It may be used in Serial-Serial, Parallel-Serial, Serial-Parallel, and Parallel-Parallel shift register applications. When LOADN is low, data at inputs A-H are parallel loaded into the D flip-flops. When LOADN is high, data enter the first flip-flop QA via the JK inputs, and is shifted right with the rising clock edge. The JK inputs may be tied together for D-type flip-flops. The 2 input OR clock can be used to combine two clock sources, or by holding one input low, can be used as a single clock source. When CLR is high, all outputs are set low.

Truth Table

CLR	LOADN	CLKINH	CLK	J	K	A...H	QA	QB	QC	QH
H	X	X	X	X	X	X	L	L	L	L
L	X	L	L	X	X	X	QA0	QB0	QC0	QH0
L	L	L	↑	X	X	a...h	a	b	c	h
L	H	L	↑	L	H	X	QAN	QA0	QBN	QGN
L	H	L	↑	L	L	X	L	QAN	QBN	QGN
L	H	L	↑	H	H	X	H	QAN	QBN	QHN
L	H	L	↑	H	L	X	QAN	QAN	QBN	QGN
L	X	H	↑	X	X	X	QA0	QB0	QC0	QH0

QA0, QB0, QH0 = Level of QA, QB, QH before the indicated steady-state input conditions were established

QAN, QGN = Level of QA or QG before the most recent transition of the clock; indicates a one-bit shift


H
G
F
E
D
C
B
K
A
J
LOADN
CLK
CLKNNM
CLR
QH
QG
QF
QE
QD
QC
QB
QA
NAD2
NAD3
IND1
IND2
IND3
IND4
IND5
DFD3 2D

SCA 10G91

Description

8 Bit Serial Shift Register

Equivalent Gate Count: 40

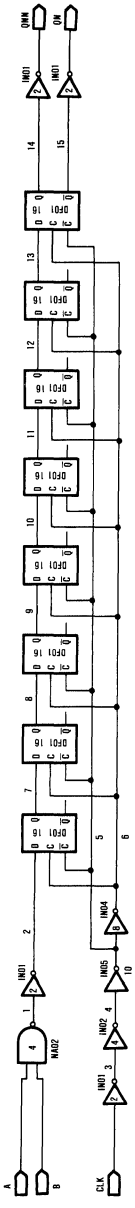
Functional Description

The 10G91 is an 8 Bit Synchronous Serial Shift Register. This shift register consists of 8 D flip-flops connected in series. Data can be entered at A or B and output can be taken at QH or QHN. Each rising clock edge shifts data right, and enters the logical AND of A + B into the first D flip-flop.

Truth Table

A at Tn	B at Tn	Q H (at Tn + 8 counts)	Q H N (at Tn + 8 counts)
H	H	H	L
L	X	L	H
X	L	L	H

Note: Tn = reference bit time, clock low;
Tn+8 = bit time after 8 low-to-high clock transitions


QNN
QN
IND1
IND1
14
15
DFD1 16
13
12
11
10
9
8
7
5
6
IND4
2
IND1
IND5
10
1
NAD2
4
IND2
4
IND1
3
A
B
CLK

SCA 10G280

Description

9 Bit Odd/Even Parity Generator/Check

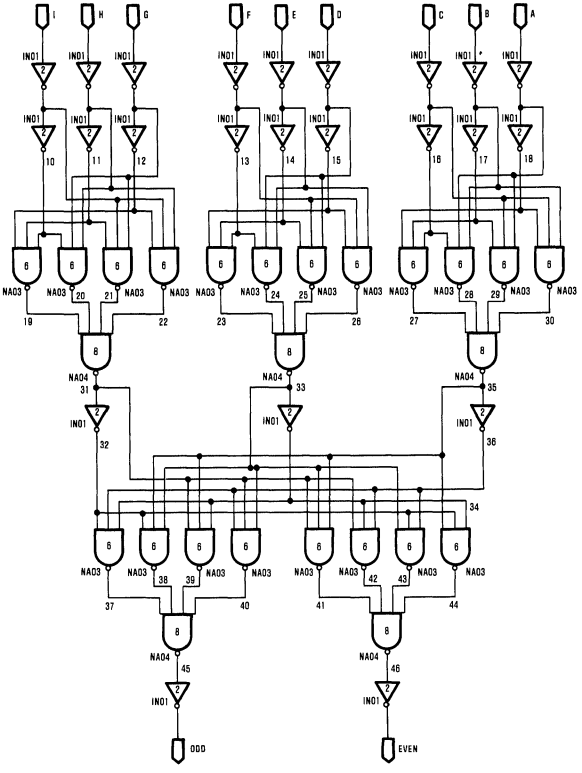
Equivalent Gate Count: 51

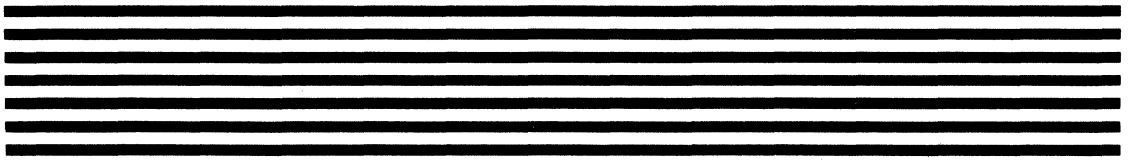
Functional Description

The 10G280 is an 9-Bit Odd/Even Parity Generator/Check. If the number of high inputs at A-I is even, EVEN will be high and if the number of high inputs is odd, ODD will be high.

Truth Table

Number of Inputs A-1 That Are High	ODD	EVEN
0, 2, 4, 6, 8	L	H
1, 3, 5, 7, 9	H	L


I
H
G
F
E
D
C
B
A
INO1
NAO3
NAO4
ODD
EVEN



Notes

Notes

Notes

General Information

Guide to MOS Handling

At Gould AMI we are continually searching for more effective methods of providing protection for MOS devices. Present configurations of protective devices are the result of years of research and review of field problems.

Although the oxide breakdown voltage may be far beyond the voltage levels encountered in normal operation, excessive voltages may cause permanent damage. Even though Gould AMI has evolved the best designed protective device possible, we recognize that it is not 100% effective.

A large number of failed returns have been due to misapplication of biases. In particular, forward bias conditions cause excessive current through the protective devices, which in turn will vaporize metal lines to the inputs. **Careful inspection of the device data sheets and proper pin designation should help reduce this failure mode.**

Gate ruptures caused by static discharge also account for a large percentage of device failures in customers' manufacturing areas. **Precautions should be taken to minimize the possibility of static charges occurring during handling and assembly of MOS circuits.**

To assist our customers in reducing the hazards which may be detrimental to MOS circuits, the following guidelines for handling MOS are offered. **The precautions listed here are used at Gould AMI.**

1. All benches used for assembly or test of MOS circuits are covered with conductive sheets. WARNING: Never expose an operator directly to a hard electrical ground. For safety reasons, the operator must have a resistance of at least 100K Ohms between himself and hard electrical ground.
2. All entrances to work areas have grounding plates on door and/or floor, which must be contacted by people entering the area.
3. Conductive straps are worn inside and outside of employees' shoes so that body charges are grounded when entering work area.
4. Anti-static neutralized smocks are worn to eliminate the possibility of static charges being generated by friction of normal wear. Two types are available; Dupont anti-static nylon and Dupont neutralized 65% polyester/35% cotton.
5. Cotton gloves are worn while handling parts. Nylon gloves and rubber finger cots are not allowed.
6. Humidity is controlled at a minimum of 35% to help reduce generation of static voltages.
7. All parts are transported in conductive trays. Use of plastic containers is forbidden. Axial leaded parts are stored in conductive foam, such as Velofoam#7611.
8. All equipment used in the assembly area must be thoroughly grounded. Attention should be given to equipment that may be inductively coupled and generate stray voltages. Soldering irons must have grounded tips. Grounding must also be provided for solder posts, reflow soldering equipment, etc.
9. During assembly of ICs to printed circuit boards, it is advisable to place a grounding clip across the fingers of the board to ground all leads and lines on the board.
10. Use of carpets should be discouraged in work areas, but in other areas may be treated with anti-static solution to reduce static generation.
11. MOS parts should be handled on conductive surfaces and the handler must touch the conductive surface **before** touching the parts.
12. In addition, no power should be applied to the socket or board while the MOS device is being inserted. This permits any static charge accumulated on the MOS device to be safely removed before power is applied.
13. MOS devices should not be handled by their leads unless absolutely necessary. If possible, MOS devices should be handled by their packages as opposed to their leads.
14. In general, materials prone to static charge accumulation should not come in contact with MOS devices.

These precautions should be observed even when an MOS device is suspected of being defective. The true cause of failure cannot be accurately determined if the device is damaged due to static charge build-up.

It should be remembered that even the most elaborate physical prevention techniques will not eliminate device failure if personnel are not fully trained in the proper handling of MOS.

This is a most important point and should not be overlooked.

More information can be obtained by contacting the Product Assurance Department.

Gould AMI Semiconductors
3800 Homestead Road
Santa Clara, California 95051
Telephone (408) 246-0330
TWX 910-338-0024 or 910-338-0018

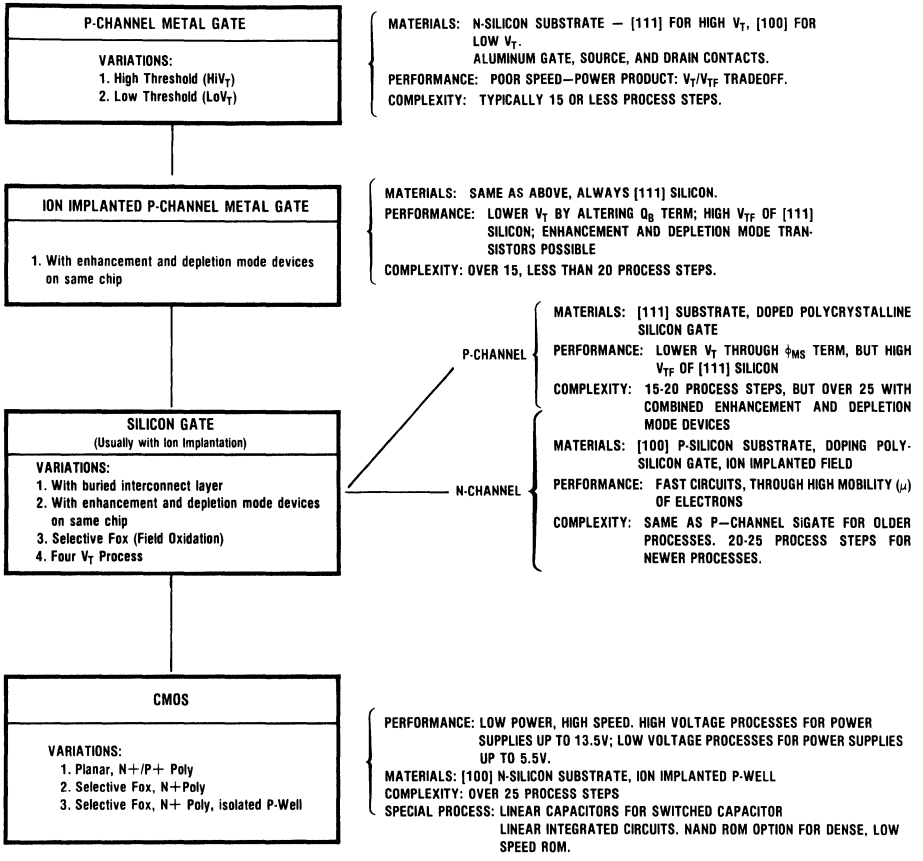
Process Descriptions

Each of the major MOS processes is described on the following pages. First, the established production proven processes are described, followed by those advanced processes, which are starting to go into volume production now. In each case, the basic processes is described first, followed by an explanation of its advantages, applications, etc.

P-Channel Metal Gate Process

Of all the basic MOS processes, P-Channel Metal Gate is the oldest and the most completely developed. It has served as the foundation for the MOS/LSI industry and still finds use today in some devices. Several versions of this process have evolved since its earliest days. A thin slice (8 to 10 mils) of lightly doped N-type silicon wafer serves as the substrate or body of the MOS transistor. Two closely spaced, heavily doped P-type regions, the source and drain, are formed within the substrate by selective diffusion of an impurity that provides holes as majority electrical carriers. A thin deposited layer of aluminum metal, the gate, covers the area between the source and drain regions, but is electrically insulated from the substrate by a thin layer (1000-15000A) of silicon dioxide. The P-Channel transistor is turned on by a negative gate voltage and conducts current between the source and the drain by means of holes as the majority carriers.

Figure B.1. Summary of MOS Process Characteristics



The basic P-Channel metal gate process can be subdivided into two general categories: **High-threshold and low-threshold.** Various manufacturers use different techniques (particularly so with the low threshold process) to achieve similar results, but the difference between them always rests in the threshold voltage V_T required to turn a transistor on. The high threshold V_T is typically -3 to -5 volts and the low threshold V_T is typically -1.5 to -2.5 volts.

The original technique used to achieve the difference in threshold voltages was by the use of substrates with different crystalline structures. The high V_T process used [111] silicon whereas, the low V_T process used [100] silicon. The difference in the silicon structure causes the surface charge between the substrate and the silicon dioxide to change in such a manner that it lowers the threshold voltages.

One of the main advantages of lowering V_T is the ability to interface the device with TTL circuitry. However, the use of [100] silicon carries with it a distinct disadvantage also. Just as the surface layer of the [100] silicon can be inverted by a lower V_T, so it also can be inverted at other random locations—through the thick oxide layers—by large voltages that may appear in the metal interconnections between circuit components. This is undesirable because it creates parasitic transistors, which interfere with circuit operation. The maximum voltage that can be carried in the interconnections is called the parasitic field oxide threshold voltage V_{TF}, and generally limits the overall voltage at which a circuit can operate. This, then, is the main factor that limits the use of the [100] low V_T process. A drop in V_{TF} between a high V_T and low V_T process may, for example, be from -28V to -17V.

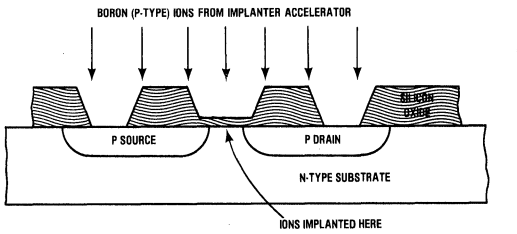
The low V_T process, because of its lower operating voltages, usually produces circuits with a lower operating speed than the high V_T process, but is easier to interface with other circuits, consumes less power, and therefore is more suitable for clocked circuits. Both P-Channel metal gate processes yield devices slower in speed than those made by other MOS processes, and have a relatively poor speed/power product. Both processes require two power supplies in most circuit designs, but the high V_T process, because it operates at a high threshold voltage, has excellent noise immunity.

Ion Implanted P-Channel Metal Gate Process

The P-Channel Ion Implanted process uses essentially the same geometrical structure and the same materials as the high V_T P-Channel process, but includes the ion implantation step. The purpose of ion implantation is to introduce P-type impurity ions into the substrate in the limited area under the gate electrode. By changing the characteristics of the substrate in the gate area, it is possible to lower the threshold voltage V_T of the transistor, without influencing any other of its properties.

Figure B.2. shows the ion implantation step in a diagrammatic manner. It is performed after the gate oxide is grown, but before the source, gate, and drain metallization deposition. The wafer is exposed to an ion beam which penetrates through the thin gate oxide layer and implants ions into the silicon substrate. Other areas of the substrate are protected both by the thicker oxide layer and sometimes also by other masking means. Ion implantation can be used with any process and, therefore could, except for the custom of the industry, be considered a special technique, rather than a process in itself.

Figure B.2. Diagram of Ion Implantation Step



The implantation of P-type ions into the substrate, in effect, reduces the effective concentration of N-type ions in the channel area and thus lowers the V_T required to turn the transistor on. At the same time, it does not alter the N-type ion concentration elsewhere in the substrate and therefore, does not reduce the parasitic field oxide threshold voltage V_{TF} (a problem with the low V_T P-Channel Metal Gate process, described above). The [111] silicon usually is used in ion-implanted transistors.

In fact, if the channel area is exposed to the ion beam long enough, the substrate in the area can be turned into P-type silicon (while the body of the substrate still remains N-type) and the transistor becomes a depletion mode device. In any circuit some transistors can be made enhancement type, while others are depletion type, and the combination is a very useful circuit design tool.

The Ion-implanted P-Channel Metal Gate process is very much in use today. Among all the processes, it represents a good optimization between cost and performance and thus is the logical choice for many common circuits, such as memory devices, data handling (communication) circuits, and others.

Because of its low V_T, it offers the designer a choice of using low power supply voltages to conserve power or increase supply voltages to get more driving power and thus increase speed. At low power levels it is more feasible to implement clock generating and gating circuits on the chip. In most circuit designs only a single power supply voltage is required.

N-Channel Process

Historically, N-Channel process and its advantages were known well at the time when the first P-Channel devices were successfully manufactured; however, it was much more difficult to produce N-Channel. One of the main reasons was that the polarity of intrinsic charges in the materials combined in such a way that a transistor was on at 0V and had a V_T of only a few tenths of a volt (**positive**). Thus, the transistor operated as a marginal depletion mode device without a well-defined **on/off** biasing range. Attempts to raise V_T by varying gate oxide thickness, increasing the substrate doping, and back biasing the substrate, created other objectionable results and it was not until research into materials, along with ion implantation, silicon gates, and other improvements came about that N-Channel became practical for high density circuits.

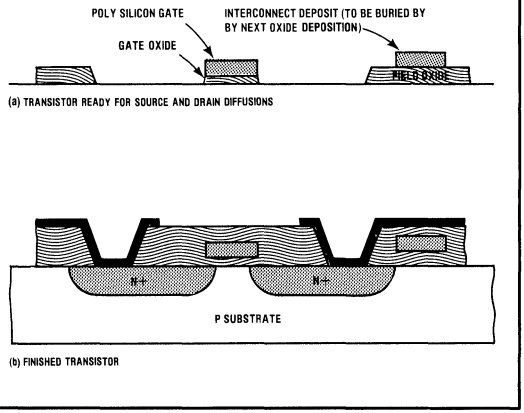
The N-Channel process gained its strength only after the P-Channel process, ion implantation, and silicon gate all were already well developed. N-Channel went into volume productions with advent of the 4K dynamic RAM and the microprocessor, both of which required speed and high density. Because P-Channel processes were nearing their limits in both of these respects, N-Channel became the logical answer.

The N-Channel process is structurally different from any of the processes described so far, in that the source, drain, and channel all are N-type silicon, whereas the body of the substrate is P-type. Conduction in the N-Channel is by means of electrons, rather than holes.

The main advantage of the N-Channel process is that the mobility of electrons is about three times greater than that of holes and, therefore, N-Channel transistors are faster than P-Channel. In addition, the increased mobility allows more current flow in a channel of any given size, and therefore N-Channel transistors can be made smaller. The positive gate voltage allows an N-Channel transistor to be completely compatible with TTL.

Although metal gate N-Channel processes have been used, the predominant N-Channel process is a silicon gate process. Among the advantages of silicon gate is the possibility of a buried layer of interconnect lines, in addition to the normal aluminum interconnnections deposited on the surface of the chip. This gives the circuit designer more latitude in layout and often allows the reduction of the total chip size. Because the polysilicon gate electrode is deposited in a separate step, after the thick oxide layer is in place, the simultaneous deposition of additional polysilicon interconnect lines is only a matter of masking. These interconnect lines are buried by later steps, as shown in Figure B.3.

Figure B.3. Crossection of an N-Channel Silicon Gate MOS Transistor



One minor limitation associated with the buried interconnect lines is their location. Because the source and drain diffusions are done after the polysilicon is deposited [see (a) of Figure B.3] the interconnect lines cannot be located over these diffusion regions.

A second advantage of a silicon gate is associated with the reduction of overlap between the gate and both the source and drain. This reduces the parasitic capacitance at each location and improves speed, as well as power consumption characteristics. Whereas in the metal gate process, the P region source and drain diffusion must be done prior to deposition of the gate electrode, in silicon gate process, the electrode is in place during diffusion, see (a) of Figure B.3. Therefore, no planned overlap for manufacturing tolerance purposes need exist and the gate is said to be **self-aligned**. The only overlap that occurs is due to the normal lateral extension of the source and drain regions during the diffusion process.

The silicon-gate process produces devices that are more compact than metal gate, and are slightly faster because of the reduced gate overlap capacitance. Because the basic silicon gate process is relatively simple, it is also economical. It is a versatile process that is used in memory devices and most any other circuit.

In addition to its use in large memory chips and microprocessors, N-Channel has become a good general purpose process for circuits in which compactness and high speed are important.

CMOS

The basic CMOS circuit is an inverter, which consists of two adjacent transistors—one an N-Channel, the other a P-Channel, as shown in Figure B.4. The two are fabricated on the same substrate, which can be either N or P type.

The CMOS inverter in Figure B.4 is fabricated on an N-type silicon substrate in which a P "tub" is diffused to form the body for the N-Channel transistor. All other steps, including the use of silicon gates and ion implantation, are much the same as for other processes.

The main advantage of CMOS is extremely low power consumption. When the common input to both gate electrodes is at a logic 1 (a positive voltage) the N-Channel transistor is biased on, the P-Channel is off, and the output is near ground potential. Conversely, when the input is at a logic 0 level, its negative voltage biases only the P-Channel transistor on and the output is near the drain voltage + V_{DD}. In either case, only one of the two transistors is on at a time and thus, there is virtually no current flow and no power consumption. Only during the transition from one logic level to the other are both transistors on and current flow increases momentarily.

Silicon Gate CMOS is also fast approaching speeds of bipolar TTL circuits. On the other hand, the use of two transistors in every gate makes CMOS slightly more complex and costly, and requires more chip size. For these reasons, the original popularity of CMOS was in SSI logic elements and MSI circuits—logic gates, inverters, small shift registers, counters, etc. These CMOS devices constitute a logic family in the same way as TTL, ECL, and other bipolar circuits do; and in the areas of very low power consumption, high noise immunity, and simplicity of operation, are still widely accepted by discrete logic circuit designers.

Low power CMOS circuits made the watch circuit possible and also have been used in space exploration, battery operated consumer products, and automotive control devices. As experience was gained with CMOS, tighter design rules and reduced device sizes have been implemented and now VLSI circuits, such as 16K RAM memories and microprocessors, are being manufactured in volume.

CMOS circuits can be operated on a single power supply voltage, which can be varied from +2.5 to about +13.5 volts with the high voltage processes, with a higher voltage giving more speed and higher noise immunity. Low voltage processes allow single power supply voltages from +1.5 to +5.5 volts.

The first implementation of an inverting gate is a process that uses both n+ to p+ polysilicon. The basic structure is a first-generation approach to which a selective field-oxidation process has been added.

Figure B.5 shows the plan and section views of the three-device gate portion. Because the P-Well in the top view spans both N-Channel devices, it is referred to as ubiquitous, and the process is called Ubiquitous P-Well.

In this planar process, p+ guard rings are used to reduce surface leakage. Polysilicon cannot cross the rings, however, so that bridges must be built. Note the use of p+ polysilicon in the P-Channel areas. The plan view shows the construction of the bridges linking p+ to metal to n+. (Were the process to be used for a low-voltage, first-generation application like a watch circuit, the guard rings would not be necessary and polysilicon could directly connect N-Channel and P-Channel devices; however, to ensure good ohmic contact from one type of polysilicon to another, polysilicon-diode contacts must be capped with metal.)

This process provides a buried contact (n+ polysilicon to n+ diffusion) that can yield a circuit-density advantage. However, neither of the other two second-generation approaches provides buried contacts. Therefore, if a layout in this process is to be compatible with the others, the buried contact must be eliminated. Though there will be a penalty in real estate, the gain for custom applications is a great increase in the number of available CMOS vendors.

The n+-Only Polysilicon Approach

Both of the second-generation CMOS processes that follow are variants of the n+-only, selective-field-oxide approach. One closely resembles the p+ n+ Ubiquitous-P-Well process, since it, too, has a Ubiquitous P-Well that is implanted before the field oxidation and thus runs under the field oxide. The other, called isolated P-Well, has separate wells for each N-Channel device that are implanted after field oxidation.

Figure B.6 shows the section and plan views of the n+-only Ubiquitous-P-Well approach used to build the gate of Figure B.4. This is the 5μm process recommended by AMI and others for new, high-performance CMOS designs. The layout is simpler than with the n+/p+ polysilicon Ubiquitous-Well approach (there are no buried contacts and no polysilicon-diode contacts), and it occupies less area for the same line widths. Also, since the process permits implanting in the field region, no guard rings are required.

Polysilicon can thus cross directly from P- to N-Channel device areas without the need for bridges or polysilicon-dioxide contacts.

A variant of the all n+ (See Figure B.7) polysilicon process just discussed uses basically the selective field-oxide approach except that the P-Wells are not continuous under the field-oxide areas; they are instead bounded by field-oxide edges. Since the P-Wells are naturally isolated from one another, the process is called n+ poly-isolated P-Well. The isolated wells must all be connected to ground; if they are left floating, circuit malfunctions are bound to occur. The grounding is done either with p+ diffusions or with top-side metalization that covers a p+-to-P-Well contact diffusion.

Figure B.4. Crossection and Schematic Diagram of a CMOS Inverter

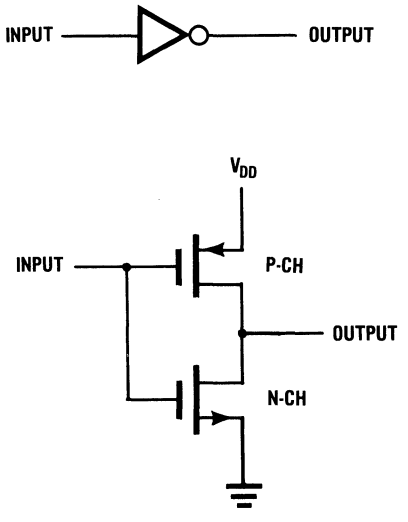
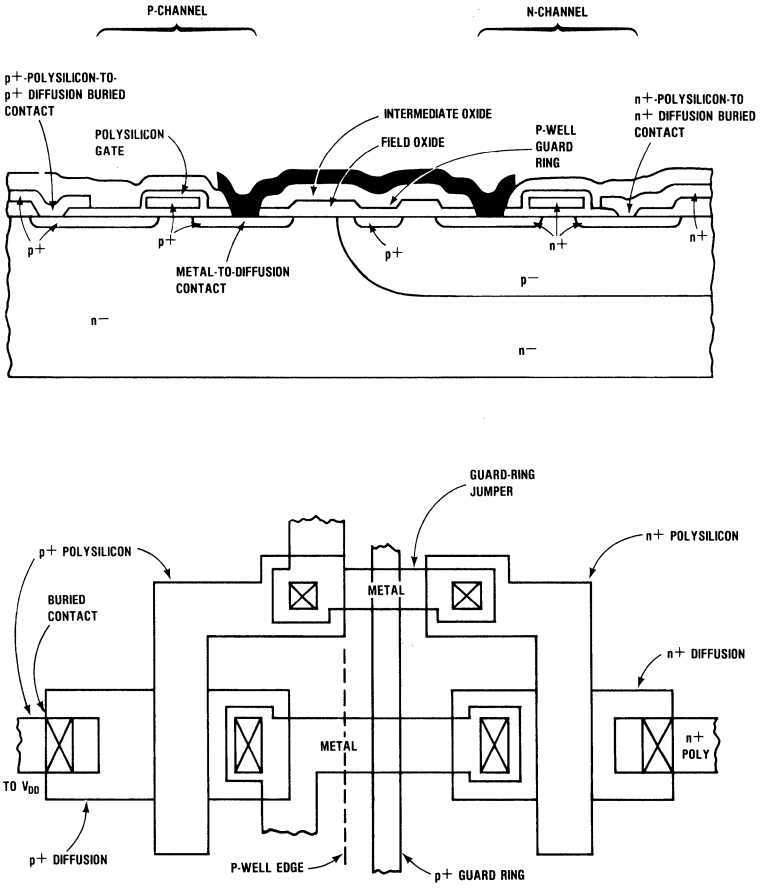
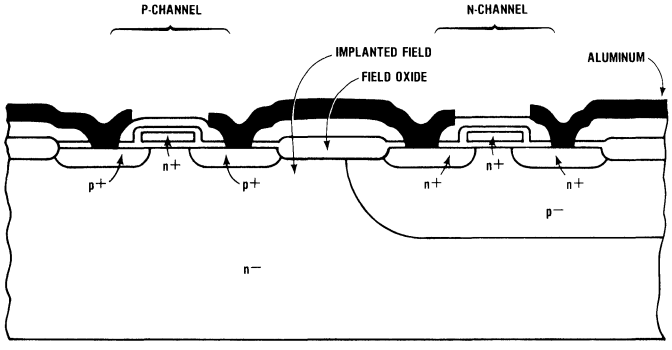


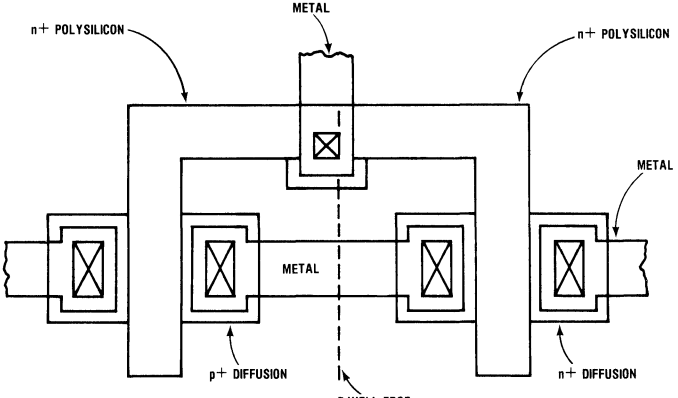
Figure B.5. n + /p + Polysilicon Approach



THE FIRST HIGH-PERFORMANCE COMPLEMENTARY-MOS PLANAR PROCESS. ITS DRAWBACKS: TWO TYPES OF POLYSILICON ARE USED, AND THE UNAVAILABILITY OF FIELD IMPLANT DOPING TIES FIELD THRESHOLD TO DEVICE THRESHOLDS.

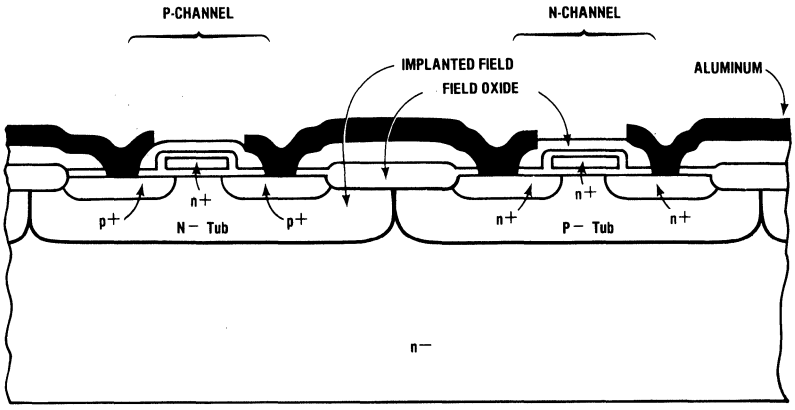
Figure B.6. n + – Only Polysilicon Approach

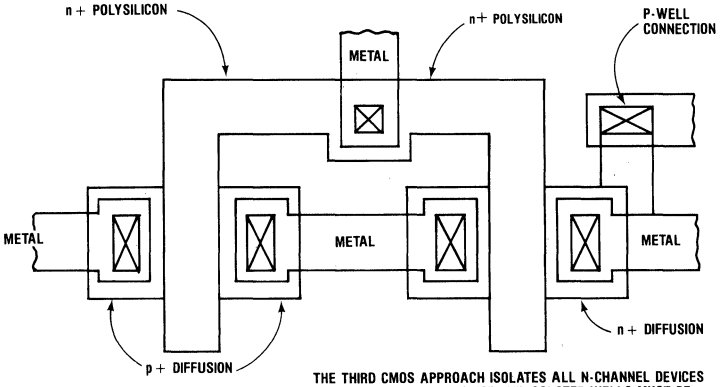




ALL NEW HIGH-PERFORMANCE CMOS CIRCUITS WILL USE ONE TYPE OF POLYSILICON. THIS VERSION HAS A UBIQUITOUS P-WELL: THAT IS, SERIES N-CHANNEL DEVICES SIT IN A COMMON P-WELL, WHICH, IMPLANTED BEFORE FIELD OXIDATION, RUNS UNDER THE FIELD OXIDE. THIS IS AMI'S PREFERRED CMOS PROCESS FORMAT FOR ALL NEW DESIGNS.

Figure B.7. Isolated Wells





THE THIRD CMOS APPROACH ISOLATES ALL N-CHANNEL DEVICES IN SEPARATE P-WELLS, SINCE THE ISOLATED WELLS MUST BE DOPED MUCH MORE HEAVILY THAN THOSE OF THE UBIQUITOUS-WELL APPROACH, n+ -TO P-WELL CAPACITANCE IS GREATER AND SWITCHING SPEEDS LOWER. THIS IS AN n+ -ONLY POLYSILICON PROCESS.

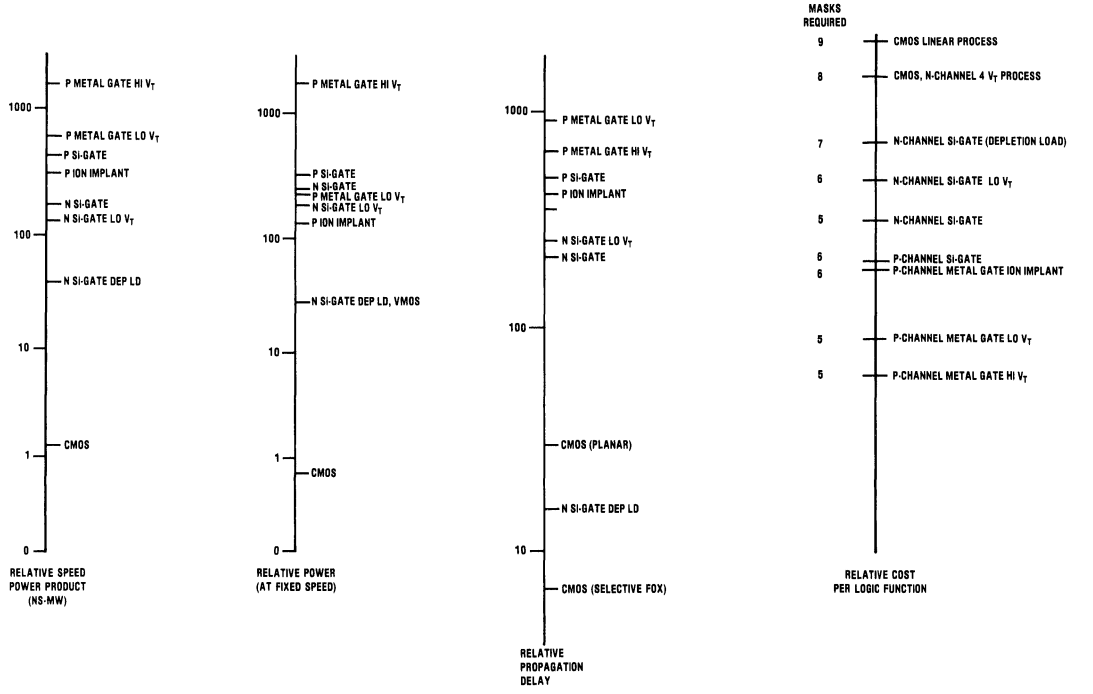
In the Isolated-Well process, the P-Wells must be doped much more heavily than in the Ubiquitous-Well process. One result is a higher junction capacitance between the n+ areas and the wells that both slows switching speeds and raises the power dissipation of a device. Even though the speed loss could be compensated for by slightly shorter channel lengths, the operating power still remains high.

Although currently available from Gould AMI and other manufacturers, the Isolated-Well process is in fact not recommended for new designs by Gould AMI. Its layout takes up more area than does one using the Ubiquitous-Well approach, even though its P-Well to p+-area spacing is slightly less.

Table 1. Layout Compatibility Concerns for CMOS Processes

Layout Feature	n+/p+ Polysilicon Ubiquitous P-Well	n+ – Only Polysilicon Ubiquitous P-Well	n+ – Only Polysilicon Isolated P-Well
Buried Contact	X	No	No
Polysilicon Diode Contact	Yes	X	X
P-Well Isolation With Diffusion Mask	No	No	Yes
Tight P-Well-To-p+ Spacing	No	No	Yes
Layout Care Required For P-Well Electrical Contacts	No	No	Yes

Figure B.8. Comparative Data on Major MOS Processes



7.5 Micron CMOS Process Parameters

	Low V_T		High V_T		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	.55	.85	1.0	1.5	N-Channel Threshold at 1μA 50 x 7.5μ Device (Volts)
V_{TP}	−.4	−.95	−.8	−1.4	P-Channel Threshold at 1μA 50 x 7.5μ Device (Volts)
V_{TF}	8		15		Poly Field Threshold at 1μA 50 x 10μ Device (Volts)
B_{VDSS}	24	—	28	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	30	39	28	33	Diffusion Resistivity Ω/□
N+	9	15	9.1	12.6	Diffusion Resistivity Ω/□
R_{POLY} P+	118	172	80	140	Poly Resistivity Ω/□
N+	30	60	29	39	Poly Resistivity Ω/□
T_{OX}	1300		1200		Gate Oxide Thickness, In Angstroms
X_j P+	1.8*		1.8*		Junction Depth, In μ
N+	2.0*		2.0*		Junction Depth, In μ
Operating Voltage	—	5	5	12	In Volts
Max Rating	—	5.5	—	13.2	In Volts
Process Designator	CTA	CTA	CTE	CTE	

(*Typical)

CMOS I Process Parameters

	General Purpose				Double Poly				NAND ROM				
	High V		Low V		High V		Low V		High V		Low V		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	0.7	1.3	0.5	1.1	0.7	1.3	0.5	1.1	0.7	1.3	0.5	1.1	N-Channel Threshold 50 x 5μ Device (Volts)
V_{TP}	−0.7	−1.3	−0.5	−1.1	−0.7	−1.3	−0.5	−1.1	−0.7	−1.3	−0.5	−1.1	P-Channel Threshold 50 x 5μ Device (Volts)
V_{TF}	17	—	7	—	17	—	7	—	17	—	7	—	Poly Field Threshold (Volts)
B_{VDSS}	17	—	7	—	17	—	7	—	17	—	7	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	15	35	15	35	15	35	15	35	15	35	15	35	Diffusion Resistivity Ω/□
N+	35	80	35	80	35	80	35	80	35	80	35	80	Diffusion Resistivity Ω/□
R_{POLY}	15	45	15	45	15	45	15	45	15	45	15	45	Poly Resistivity Ω/□ (All poly is N+)
T_{OX}	750	850	750	850	750	850	750	850	750	850	750	850	Gate Oxide Thickness, In Angstroms
X_j P+	1.2*		1.2*		1.2*		1.2*		1.2*		1.2*		Junction Depth, In μ
N+	1.5*		1.5*		1.5*		1.5*		1.5*		1.5*		Junction Depth, In μ
Operating Voltage	2.2	13.2	1.5	5.5	2.2	13.2	1.5	5.5	2.2	13.2	1.5	5.5	In Volts
Max Rating	—	13.2	—	5.5	—	13.2	—	5.5	—	13.2	—	5.5	In Volts
Process Designator	CVA	CVA	CVH	CVH	CVB	CVB	CVE	CVE	CVD	CVD	CVC	CVC	

(*Typical)

CMOS II Process Parameters (P-Well)

	Single Metal		Double Metal		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	0.6	1.0	0.6	1.0	N-Channel Threshold (Volts)
V_{TP}	−0.6	−1.0	−0.6	−1.0	P-Channel Threshold (Volts)
V_{TF}	14.0	—	12.0	—	Poly Field Threshold (Volts)
BV_{DSS}	12.0	—	10.0	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	50	100	50	100	Diffusion Resistivity Ω/□
N+	15	40	15	40	Diffusion Resistivity Ω/□
R_{POLY}	15	30	15	30	Poly Resistivity, Ω/□ (All Poly is N+)
T_{OX}	450	550	450	550	Gate Oxide Thickness, In Angstroms
X_j P+	0.3	0.5	0.3	0.5	Junction Depth, In Microns
N+	0.3	0.5	0.3	0.5	Junction Depth, In Microns
Operating Voltage	2.25	11.0	2.25	5.5	In Volts
Max Rating	—	11.0	—	7.5	In Volts
Process Designator	CCB, CCF, CCG		CCD		CCF Has Double Poly Capacitor CCG Has Poly Capacitor and Depletion N-Channel

6 & 5 Micron SiGate NMOS Process Parameters

			6 Micron				5 Micron		
	Low V_T		HighV_T		16.67/ Process Shrink				
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TE}	0.6	1.0	0.8	1.2	.75	1.25	0.6	1.0	Extrapolated Enhancement Threshold on a 50 x 6μ Transistor (Volts)
V_{TD}	−3.0	−4.0	−2.5	−3.5	−2.5	−3.5	−2.5	−3.5	Extrapolated Depletion Threshold on a 50 x 50μ Transistor (Volts)
V_{TN}	—	—	—	—	—	—	−.2	−.2	Intrinsic Device Threshold 50 x 6μ Transistor (Volts)
V_{TDD}	—	—	—	—	—	—	−4.35	−3.65	Deep Depletion Threshold (Volts)
V_{TF}	13	40	13	40	12	30	10	—	Poly Field Threshold (Volts)
B_{VDSS}	14	—	14	—	12	—	10	—	Drain-Source Breakdown on 50 x 50μ Transistor
R_{DIFF}	8	14	8	14	8	14	8	25	N+ Region Resistivity Ω/□
R_{POLY}	20	40	20	40	20	40	20	40	N+ Doped Poly Resistivity Ω/□
T_{OX}	1000	1150	1000	1150	750	850	750	850	Gate Oxide Thickness, In Angstroms
X_j	1.2	1.6	1.2	1.6	0.8	1.2	0.8	1.2	Junction Depth, In μ
Operating Voltage	5	12	5	12	5	12	5	12	In Volts
Max Rating		13.2		13.2		13.2		13.2	In Volts
Process Designator	NVC	NVC	NVD	NVD	NVS	NVS	NEA/NEC		

NMOS I & NMOS II Process Parameters

	NMOS I				NMOS II				
	$4V_T$		Std.		$4V_T$		Std.		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TE}	0.6	1.0	0.6	1.0	0.6	1.0	0.6	1.0	Extrapolated Enhancement Threshold Voltage on a 50 x 4μ Transistor (4μ Processes) or 50 x 3μ Transistor (3μ Processes) (Volts)
V_{TD}	−3.5	−2.5	−3.5	−2.5	−3.5	−2.5	−3.5	−2.5	Extrapolated Threshold 50 x 50μ Device (Volts)
V_{TN}	−0.15	+0.15	N/A	N/A	−0.15	+0.15	N/A	N/A	Extrapolated Threshold 50 x 6μ Device (Volts)
V_{TDD}	−4.35	−3.65	N/A	N/A	−4.85	−4.15	N/A	N/A	Extrapolated Threshold 50 x 50μ Device (Volts)
V_{TF}	7.5	—	7.5	—	7.5	—	7.5	—	Poly Field Threshold (Volts)
B_{VDSS}	7.5	—	7.5	—	7.5	—	7.5	—	Punch Through Voltage 50 x 4μ Device (4μ Processes) or 50 x 3μ Device (3μ Processes) (Volts)
R_{DIFF}	15	30	15	30	15	30	15	30	Diffusion Resistivity Ω/□
R_{POLY}	20	50	20	50	20	40	20	40	Poly Resistivity Ω/□
T_{OX}	650	750	650	750	450	550	450	550	Gate Oxide Thickness, In Angstroms
X_j	0.3	0.5	0.3	0.5	0.3	0.5	0.3	0.5	N+ Junction Depth, In μ
Operating Voltage	—	5/12	—	5/12	—	5	—	5	In Volts
Max Rating	—	5.5/13.2	—	5.5/13.2	—	5.5	—	5.5	In Volts
Process Designator	NDD	NDD	NDE	NDE	NCC	NCC	NCA	NCA	

7.5 Micron Metal Gate PMOS Process Parameters

			0 Implant				1 Implant		2 Implant		
	High V_T		Med V_T		Low V_T						
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TE}	−3.25	−4.95	−2.8	−4.2	−1.8	−2.5	−1.0	−1.8	−1.2	−2.0	I_{DS} = 1μA
V_{TD}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	4.0	5.0	Depletion Measurement on a 50μ Transistor (Volts)
V_{TF}	30	—	25	—	17	—	25	—	25	—	Field Threshold (Volts)
B_{VDSS}	30	—	30	—	30	—	22	—	22	—	Drain-Source Breakdown (Volts)
R_{DIFF}	30	60	30	60	30	60	30	60	30	60	Sheet Resistivity Ω/□
I_{DS}/mA	1.25	2.55	0.8	2.2	0.8	2.0	2.8	4.0	2	4	Drain-Source Current (mA)
B_{VOXG}	120	—	80	—	100	—	90	—	90	—	Gate Oxide Breakdown (Volts)
X_jJ	1.7	1.9	1.7	1.9	1.7	1.9	1.7	1.9	1.7	1.9	Junction Depth, In μ
Process Designator	PMC	PMC	PMT	PMT	PMD	PMD	PNR	PNR	POG	POG	

CMOS II Process Parameters (N-Well)

	Single Metal		Double Metal		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	0.6	1.0	0.6	1.0	N-Channel Threshold (Volts)
V_{TP}	−0.6	−1.0	−0.6	−1.0	P-Channel Threshold (Volts)
V_{TF}	14.0	—	12.0	—	Poly Field Threshold (Volts)
BV_{DSS}	12.0	—	10.0	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+ N+	50 15	100 40	50 15	100 40	Diffusion Resistivity Ω/□ Diffusion Resistivity Ω/□
R_{POLY}	15	30	15	30	Poly Resistivity, Ω/□ (All Poly is N+)
T_{OX}	390	460	390	460	Gate Oxide Thickness, In Angstroms
X_j P+ N+	0.3 0.3	0.5 0.5	0.3 0.3	0.5 0.5	Junction Depth, In Microns Junction Depth, In Microns
Operating Voltage	2.25	11.0	2.25	5.5	In Volts
Max Rating	—	11.0	—	7.5	In Volts
Process Designator	CCN/CCO		CCP		CCO Has Double Poly Capacitor

CMOS III Process Parameters (Twin-Tub)

	Single Metal		Double Metal		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	0.5	1.0	0.5	1.0	N-Channel Threshold (Volts)
V_{TP}	−0.5	−1.0	−0.5	−1.0	P-Channel Threshold (Volts)
V_{TF}	10.0	—	10.0	—	Poly Field Threshold (Volts)
BV_{DSS}	8.0	—	8.0	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+ N+	60 40	100 60	60 40	100 60	Diffusion Resistivity Ω/□ Diffusion Resistivity Ω/□
R_{POLY}	20	30	20	30	N+ Poly Silicon Resistivity Ω/□ (All Poly is N+)
T_{OX}	270	330	270	330	Gate Oxide Thickness, In Angstroms
X_j P+ N+	0.25 0.25	0.35 0.40	0.25 0.35	0.35 0.40	Junction Depth, In Microns Junction Depth, In Microns
Operating Voltage	2.25	5.5	2.25	5.5	In Volts
Max Rating	—	7.0	—	7.0	In Volts
Process Designator	CBA, CBC		CBB, CBD		CBA & CBB Use P-type Substrate CBC & CBD Use N-type Substrate

Technology Comparision

	NMOS		CMOS		
Feature	**NMOS I**	**NMOS II**	**CMOS I**	**CMOS II**	**CMOS III**
Channel Length (Effect) (Drawn)	2.4 3.5	1.9 3.0	3.0 5.0	2.1 3.0	1.5 2.0
Field OX Pitch (μm)	7.5	6.0	10.0	6.0	4.5
Poly Pitch (μm)	7.5	6.0	10.0	6.0	4.0
Metal Pitch (μm)	8.5	7.0 8.0	10.0	7.0 9.0	5.0 5.0
Channel Width (Drawn) (μm)	4.0	3.0	5.0	3.0	2.5
Contact Size (μm)	4×4	3×3	5×5	3×3	2×2
Inverter Delay (ns) ($t_0=1$)	2.5	1.5	2.9	1.7	1.2
Power Supply (V)	5-12	5	5-12	5-10	5
Gate OX Thickness (Å)	700	500	800	500	300

GOULD

AMI Semiconductors

Product Assurance Program

Introduction

Quality is one of the most used, least understood, and variously defined assets of the semiconductor industry. At Gould AMI we have always known just how important effective quality assurance, quality control, and reliability monitoring are in the ability to deliver a repeatably reliable product. Particularly, through the manufacture of custom MOS/LSI, experience has proved that one of the most important tasks of quality assurance is the effective control and monitoring of manufacturing processes. Such control and monitoring has a twofold purpose: to assure a consistently good product, and to assure that the product can be manufactured at a later date with the same degree of reliability.

To effectively achieve these objectives, Gould AMI has developed a Product Assurance Program consisting of three major functions:

- Quality Control
- Quality Assurance
- Reliability

Each function has a different area of concern, but all share the responsibility for a reliable product.

The Gould AMI Product Assurance Program

The program is based on MIL-STD-883, MIL-M-38510, and MIL-Q-9858A methods. Under this program, Gould AMI manufactures highest quality MOS devices for all segments of the commercial and industrial market and, under special adaptations of the basic program, also manufactures high reliability devices to full military specifications for specific customers.

The three aspects of the Gould AMI Product Assurance Program—Quality Control, Quality Assurance, and Reliability—have been developed as a result of many years of experience in MOS device design and manufacture.

Quality Control establishes that every method meets or fails to meet, processing or production standards—**QC checks methods.**

Quality Assurance establishes that every method meets, or fails to meet, product parameters—**QA checks results.**

Reliability establishes that QA and QC are effective—**Reliability checks device performance.**

One indication that the Gould AMI Product Assurance Program has been effective is that NASA has endorsed Gould AMI products for flight quality hardware since 1967. The Lunar Landers and Mars Landers all have incorporated Gould AMI circuits, and Gould AMI circuits have also been utilized in the Viking and Vinson programs, as well as many other military airborne and reconnaissance hardware programs.

Quality Control

The Quality Control function in Gould AMI's Product Assurance Program involves constant monitoring of all aspects of materials and production, starting with the raw materials purchased, through all processing steps, to device shipment. There are three major areas of Quality Control:

- Incoming Materials Control
- Microlithography Control
- Process/Assembly Control

Incoming Materials Control

All purchased materials, including raw silicon, are checked carefully to various test and sampling plans. The purpose of incoming materials inspection is to ensure that all items required for the production of Gould AMI MOS circuits meet such standards as are required for the production of high quality, high reliability devices.

Incoming inspection is performed to specifications agreed to by suppliers of all materials. The Quality Control group continuously analyzes supplier performance, performs comparative analysis of different suppliers, and qualifies the suppliers.

Tests are performed on all direct material, including packages, wire, lids, eutectics, and lead frames. These tests are performed using a basic sampling plan in accordance with MIL-S-19500, generally to a Lot Tolerance Percent Defective (LTPD) level of 10%. The AQL must be below 1% overall.

Two incoming material inspection sequences illustrate the thoroughness of Gould AMI Quality Control:

- Purchased packages are first inspected visually. Then, dimensional inspections are performed, followed by a full functional inspection, which subjects the packages to an entire production run simulation. Finally, a full electrical evaluation is made, including checks of the insulation, resistance, and lead-to-lead isolation. A package lot which passes these tests to an acceptable LTPD level is accepted.
- Raw silicon must also pass visual and dimensional checks. In addition, a preferential etch quality inspection is performed. For this inspection, the underlayers of bulk silicon are examined for potential anomalies such as dislocation, slippage or etch pits. Resistivity of the silicon is also tested.

Microlithography Control

Microlithography involves the processes which result in finished working plates, used for the fabrication of wafers. These processes are pattern or artwork generation, photoreduction, and the actual printing of the working plates.

Pattern generation now is the most common practice at Gould AMI. The circuit layout is digitized and stored on a tape, which then is read into an automated pattern generator which prints a highly accurate 10x reticle directly.

In cases where the more traditional method of artwork generation is used whether Rubylith, Gerber Plots, Gould AMI generated or customer generated—the artwork is thoroughly inspected. It is checked for level-to-level registration and dimensional tolerances. Also, a close visual inspection of the workmanship is made. Gould AMI artwork is usually produced at 200x magnification and

must conform to stringent design rules, which have been developed over a period of years as part of the process control requirements.

Acceptable artwork is photographically reduced to a 20x magnification, and then further to a 10x magnification. The resulting 10x reticles are then used for producing 1x masters. The masters undergo severe registration comparisons to a registration master and all dimensions are checked to insure that reductions have been precise. During this step, image and geometry are scrutinized for missing or faded portions and other possible photographic omissions.

For a typical N-Channel silicon gate device, master sets are checked at all six geometry levels in various combinations against each other and against a proven master set. Allowable deviations within the die are limited to 0.5 micron, deviations within a plate are limited to 1 micron, and all plate deviations are considered cumulatively.

Upon successful completion of a device master set, it is released to manufacturing where the 1x plates are printed. A sample inspection is performed by manufacturing on each 30-plate lot and the entire lot is returned to Quality Control for final acceptance. Quality Control performs audits on each manufacturing inspector daily, by sample inspection techniques.

The plates can be rejected first by manufacturing when the 30-plate lots are inspected, or by Quality Control when the lots are submitted for final acceptance. If either group rejects the plates, they are rescreened and then undergo the same inspection sequence. In the rescreening process, the plates undergo registration checks; visual checks for pin holes, protrusions, and faded or missing images, as well as all critical dimension checks.

Process Control

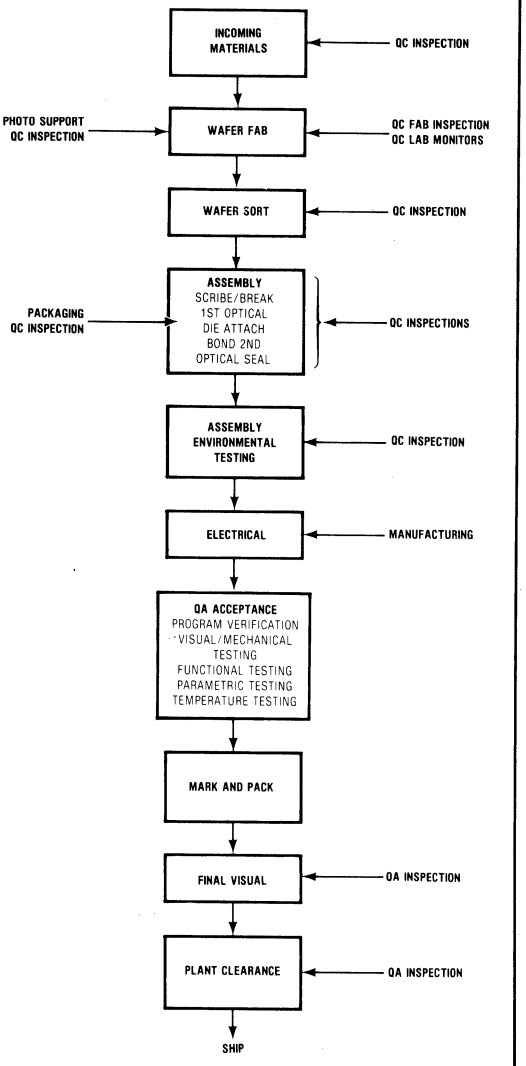
Once device production has started in manufacturing, Gould AMI Quality Control becomes involved in one of the most important aspects of the Product Assurance Program—the analysis and monitoring of virtually all production processes, equipment, and devices.

Process controls are performed in the fabrication area, by the Quality Control Fabrication Group, to assure adherence to specifications. This involves checks on operators, equipment and environment. Operators are tested for familiarity with equipment and adherence to procedure. Equipment is closely checked both through calibration and maintenance audits. Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possibility of contamination or adverse effects due to temperature or humidity excesses.

Experience has proven that such close control of the operators, equipment, and environment is highly effective towards improved quality and increased yields.

In addition to the specification adherence activities of the

Figure 1. Flowchart of Product Assurance Program Implementation



QC Fabrication Group, A QC Laboratory performs constant process monitoring of virtually every step of all processes. Specimens are taken from all production steps and critically evaluated. Sampling frequency varies, depending on the process, but generally, oxidation, diffusion, masking and evaporization are the most closely monitored steps.

Results are supplied both to manufacturing and engineering. When evidence of a problem occurs, QC provides recommendations for corrections and follows up the corrective action taken.

Optical Inspections are performed at several steps; quality control limits are based on a 10% LTPD. The chart in Figure 1 shows process steps and process control points.

Quality Assurance

The Quality Assurance function in the Product Assurance Program involves checking the ability of manufactured parts to meet specifications. In addition, the QA group also is responsible for calibration of all equipment, and for the maintenance of Gould AMI internal product specifications, to assure that they are always in conformance with customer specifications or other Gould AMI specifications.

After devices undergo 100% testing in manufacturing, they are sent to Quality Assurance for acceptance. Lots are defined, and using the product specifications, sample sizes are determined, along with the types of tests to be performed and the test equipment to be used. Lots must pass QA testing to a 0.04% AQL.

Three types of tests are performed on the samples: visual/mechanical, parametric, and functional. All tests are performed both at room temperature and at elevated temperature. In addition, a number of other special temperature tests may be performed if required by the specification.

To perform the tests, QA uses Gould AMI PAFT test systems, ROM test systems, Macrodata testers, Fairchild **Sentry**, LTX **Sentinel**, **XINCOM** systems, Teradyne test systems, and various bench test units. In special instances a part may also be tested in a real life environment in the equipment which is to finally utilize it.

If a lot is rejected during QA testing, it is returned to the production source for an electrical rescreening. It is then returned to QA for acceptance but is identified as a resubmitted lot. If it fails again, corrective action in engineering is initiated. As evidence of the problem is detected, the parts may also be traced all the way back to the wafer run to analyze the cause.

When a lot is acceptable, it is sent to packaging and then to finished goods. When parts leave finished goods, they are again checked by the QA group to a 10% LTPD with visual/mechanical tests. Also, all supporting documentation for the parts is verified, including QA acceptance, special customer specifications, certificates of compliance, etc. Only after this last check are devices considered ready for plant clearance.

If there are customer returns, they are first sample tested by QA to determine the cause of the return. (Many times an invalid customer test will incorrectly cause returns.) Selected return samples are sent to Reliability for failure analysis.

Reliability

The Reliability function in the Product Assurance Program involves process qualification, device qualification, package qualification, reliability program qualification and failure analysis. To perform these functions Gould AMI Reliability group is organized into two major areas:

- Reliability Laboratory
- Failure Analysis

Reliability Laboratory

Gould AMI Reliability Laboratory is responsible for the following functions.

- New Process Qualification
- Process Change Qualification
- Process Monitoring
- New Device Qualification
- Device Change Qualification
- New Package Qualification
- Device Monitoring
- Package Change Qualification
- Package Monitoring
- High Reliability Programs

There are various closely interrelated and interactive phases involved in the development of a new process, device, package or reliability program. A process change may affect device performance, a device change may affect process repeatability, and a package change may affect both device performance and process repeatability. To be effective, the Reliability Laboratory must monitor and analyze all aspects of new or changed processes, devices, and packages. It must be determined what the final effect is on product reliability, and then evaluate the merits of the innovation or change.

Process Qualification

For example, Gould AMI Research and Development group recommends a new process or process alteration when it feels that the change can result in product improvement. The Reliability Laboratory then performs appropriate environmental and electrical evaluations of a new process. Typically, a special test vehicle, or "rel chip", generated by R&D during process development, is used to qualify the recommended new process or process change.

The rel chip is composed of circuit elements similar to those that may be required under worst-case circuit design conditions. The rel chip elements are standard for any given process, and thus allow precise comparisons between diffusion runs. The following is an example of what is included on a typical rel chip:

- A discrete inverter and an MOS capacitor

- A large P-N junction covered by an MOS capacitor.
- A large P-N junction area (identical to the junction area above, but without the MOS capacitor)
- A large area MOS capacitor over substrate
- Several long contact strings with different contact geometries
- Several long conductor geometries, which cross a series of eight deeply etched areas

Each circuit element of a rel chip allows a specific test to be performed. As an example, the discrete inverter and MOS load device accommodate power life tests. As a consequence, any type of parameter drift can be observed. The MOS capacitor, covering the large P-N junction, can serve to indicate the presence of contamination in the oxide, under the oxide, or in the bulk silicon. If unusual drift is evidenced, the location of contamination can be determined through analysis of the additional MOS capacitor and the large P-N junction area. The metal conductor interconnecting contacts is useful for life testing under relatively high current conditions. It facilitates the detection of metal separation when moisture or other contaminants are present.

The conductors crossing deeply etched areas allow the checking of process control. Rather than depending upon optical inspection of metal quality, burned out areas caused by high currents are readily identified and provide a quantitative measure of metal quality.

If the Reliability Laboratory determines that a recommended new process or process change is viable for manufacturing purposes, further analysis is necessary to determine that production devices can be manufactured in high volume, in a repeatable and reliable manner.

Process Monitoring

In addition to process qualification, the Reliability group also conducts ongoing process monitoring programs. Once every 90 days each major production process is evaluated using rel chips as test vehicles. The resulting test data is analyzed for parameter limits and process stability. In this manner Gould AMI can help assure repeatability and high product quality.

Package Qualifications

New packages are also qualified before they are adopted. To analyze packages, a qualification matrix is designed, according to which the new package and an established package (used for control) are tested concurrently. The test matrix consists of a full spectrum of electrical and environmental stress tests, in accordance with MIL-STD-883.

Failure Analysis

Another important function of the Reliability group is failure analysis. Scanning electron microscopes, high power optical microscopes, diagnostic probe stations, and other equipment is used in failure analysis of devices submitted from various sources. It is the function of the Reliability group to determine the cause of failure and recommend corrective action.

The Reliability group provides a failure analysis service for the previously mentioned in-house programs and for the evaluation of customer returns. All Gould AMI customers are provided a failure analysis service for any part that fails within one year from date of purchase and the results of the analysis are returned in the form of a written report.

Summary

The Product Assurance Program at Gould AMI is oriented towards process control and monitoring, and the evaluation of devices. The Program consists of three major functions: Quality Control, Quality Assurance, and Reliability. Constant monitoring of all phases of production, with information feedback at all levels, allows fast and efficient detection of problems, evaluation and analysis, correction, and verification of the correction. The overall result is a line of products which are highly repeatable and reliable, with a very low reject level.

Packaging

Introduction

Plastic Packages

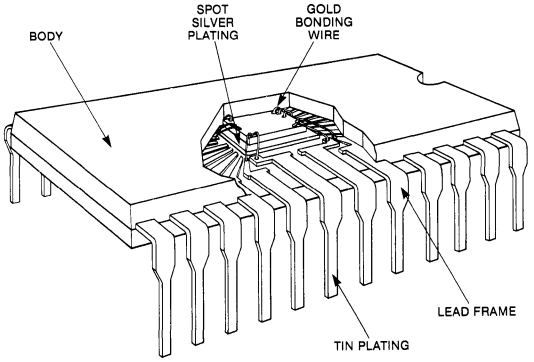
Gould AMI's plastic packages utilize transfer molded epoxy novalacs to provide the highest quality and most reliable plastic encapsulated custom and standard ICs available. Features include copper leadframes with sopot silver on P-DIPs, PCCs and SOICs utilizing a conductive adhesive with automated die bonding. This variety gives you the flexibility you desire, and assures you the best thermal and electrical performance available for your application.

Plastic Dual-In-Line Package

The Gould AMI plastic dual-in-line package is the equivalent of the widely accepted industry standard, refined by Gould AMI for MOS/VLSI applications. The package consists of a plastic body, transfer-molded directly onto the assembled leadframe and die. The leadframe is copper alloy, with external pins tin plated. Internally, there is a 150μIn. silver spot on the die attach pad and on each bonding fingertip. Gold bonding wire is attached with the thermosonic gold ball bonding technique.

Materials of the leadframe, the package body, and the die attach are all closely matched in thermal expansion coefficients to provide optimum response to various thermal conditions. During manufacture every step of the process is rigorously monitored to assure maximum quality of the Gould AMI plastic package.

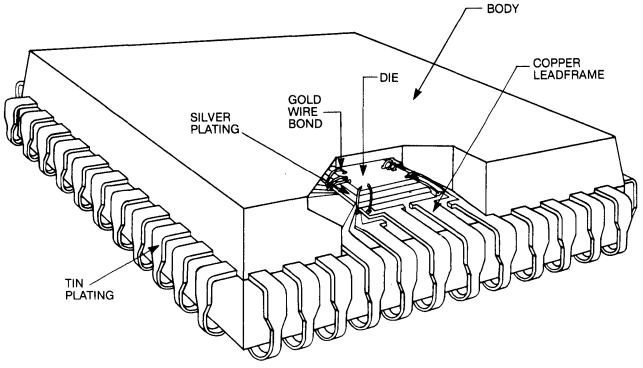
Available in 8, 14, 16, 18, 20, 22, 24, 28, 40, 48 and 64 pin configurations, our JEDEC standard P-DIPS are on 100 mil centers.



Plastic Chip Carrier

For gate arrays, standard cell designs and custom ICs, our new Plastic Chip Carrier (PCC) meets you need for a quality surface-mount quad package to support complex integrated circuits requiring high lead counts. An added benefit is the PCC's J-form leads which make it ideal for easy handling and shipping. The PCC is transfer molded and thermosonically wire bonded. Die is mounted on a copper leadframe and external leads are tin plated.

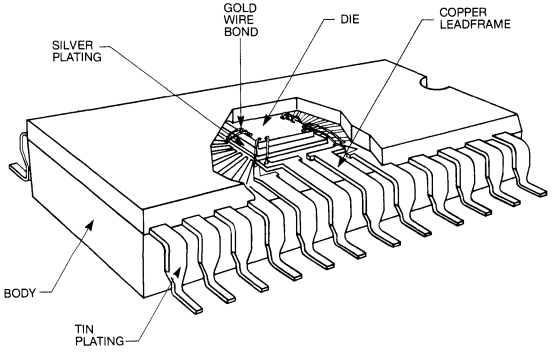
Available in 44, 68 and 84 pin configurations, our JEDEC standard PCCs are on 50 mil centers.



Small Outline IC Package

Our small-outline integrated circuit (SOIC) package is the smallest dual-in-line package available, and is an excellent choice for maximum board density. It can be automatically surface mounted on your printed circuit board and is ideal for the automotive, telecommunications and computer industries, or any industry that requires dense placement of chips on boards to fulfill heavy electronic capability requirements. The SOIC uses the standard gull wing lead form.

Available in 16 and 28 pin configurations, our JEDEC standard SOICs are on 50 mil centers.

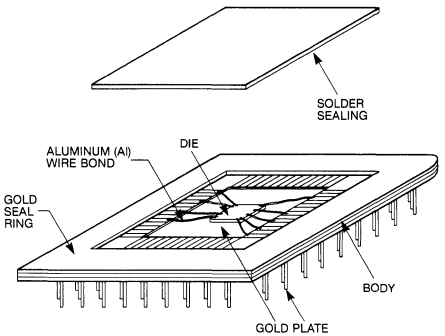


Pin Grid Array

Built on the same concept as the ceramic side brazed package, the Pin Grid Array is also suitable for high reliability applications but provides the opportunity for high density packaging with very high pin counts. The unique lead design makes it compatible with socket insertion mounting.

Most commonly supplied with an Al_2O_3 ceramic body, gold plating on the lead and die cavity, and sealed with a gold-tin eutectic solder on a Kovar/alloy 42 lid.

Available in 68, 84, 100, 120 and 144 pin configurations.



Packaging

Introduction

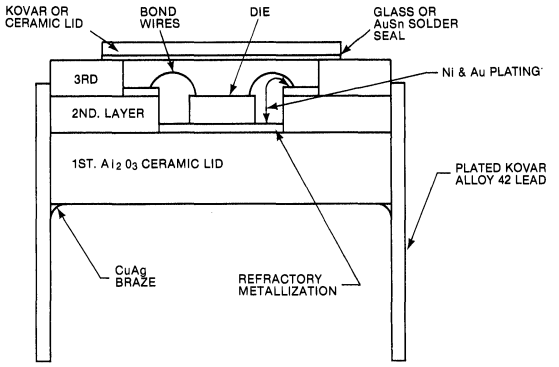
Ceramic Packages

The ceramic and cerdip packages provided by Gould AMI are commonly used for high reliability applications. Glass or solder eutectic sealing and ceramic body yields excellent hermeticity characteristics, thereby insuring against device failure from moisture penetration..Gould AMI supplied a full range of ceramic packages to meet many applications.

Ceramic Package

Industry standard high performance, high reliability package, made of three layers of Al_2O_3 ceramic and nickel-plated refractory metal. Either a low temperature glass sealed ceramic lid or a gold tin eutectic sealed Kovar lid is used to form the hermetic cavity of this package. Package leads are available with gold or tin plating for socket insertions or soldering.

Available in 14, 16, 18, 22, 24, 28, 40, 48 and 64 pin configurations.

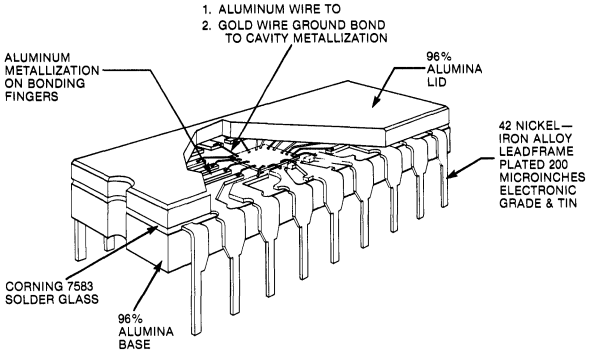


Cerdip Package

The Cerdip dual-in-line package has the same high performance characteristics as the standard three-layer ceramic package yet is a cost-effective alternative. It is a military approved type package with excellent reliability characteristics.

The package consists of an Alumina (Al_2O_3) base and the same material lid, hermetically fused onto the base with low temperature solder glass.

Available in 14, 16, 18, 22, 24, 28 and 40 pin configurations.



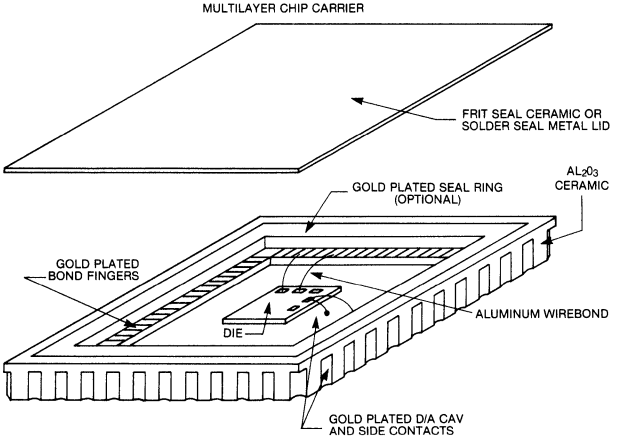
Packaging

Chip Carrier Package

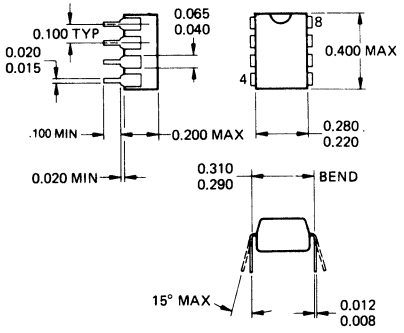
Chip carriers are the new industry standard in reducing package size. Built on the same concept as the highly reliable side-braze ceramic package, it is made of three layers of AL_2O_3 ceramic, refractory metalization and gold plating. The chip carier also offers contact pads equally spaced on all four sides of the carrier resulting in increased package density, better electrical characteristics, and a more cost effective way of packaging IC devices.

The package comes with a gold tin eutectic sealed metal lid or the low cost glass sealed ceramic lid creating a standard hermetic cavity.

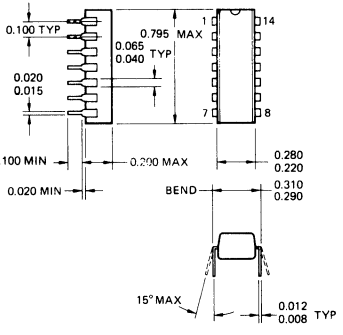
Available in 20, 24, 28, 40, 44, 48, 52, 68 and 84 LD standard 3-layer versions on 50 mil center lines to JEDEC standards.



8-Pin Plastic

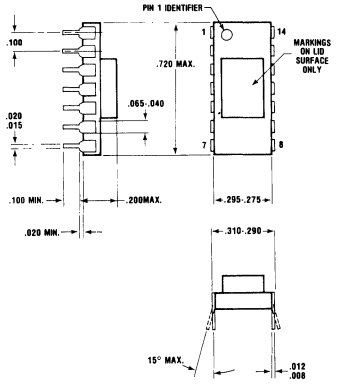


14-Pin Plastic

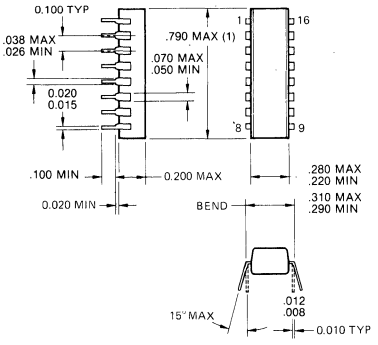


Packaging

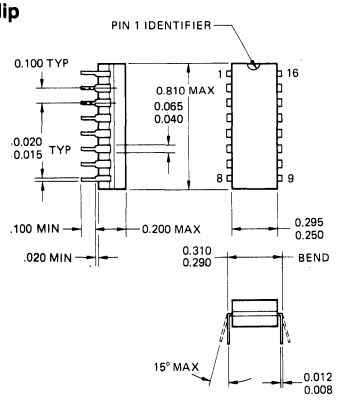
14-Pin Ceramic



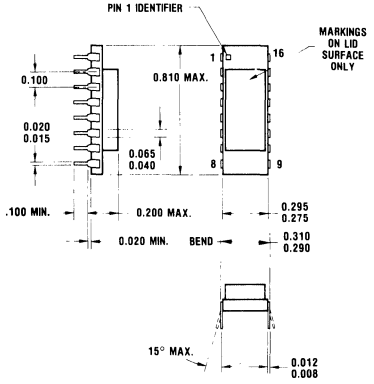
16-Pin Plastic



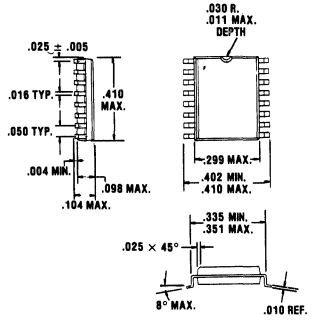
16-Pin Cerdip



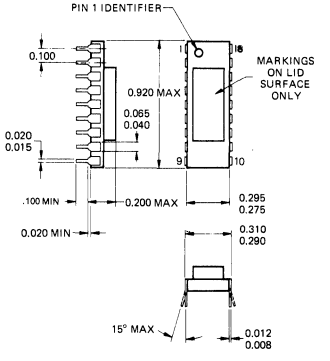
16-Pin Ceramic



16-Lead Plastic S.O.I.C.

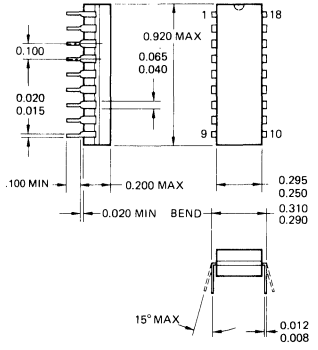


18-Pin Ceramic

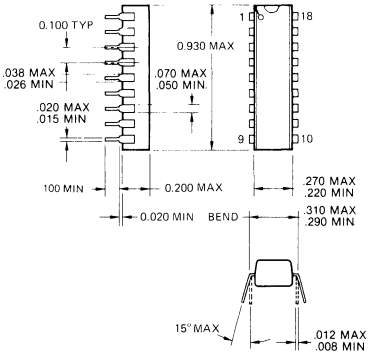


Packaging

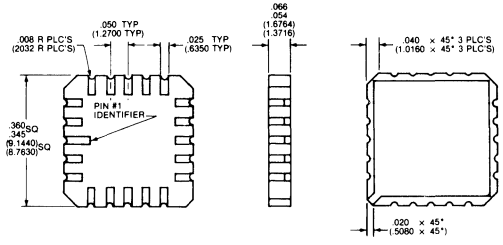
18-Pin Cerdip



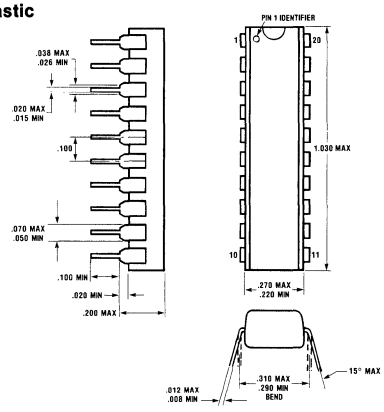
18-Pin Plastic



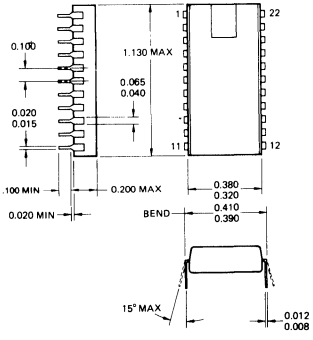
20-Lead Chip Carrier



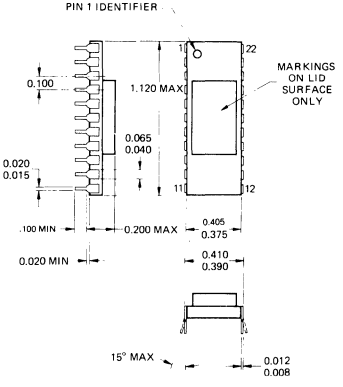
20-Pin Plastic



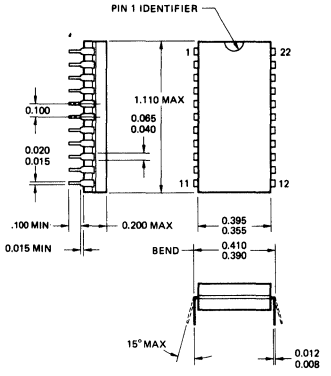
22-Pin Plastic



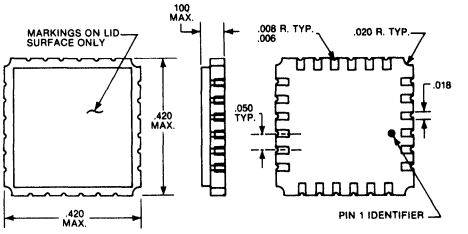
22-Pin Ceramic



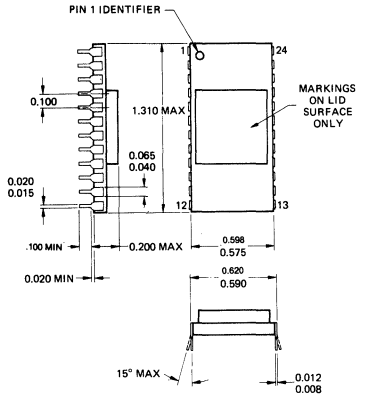
22-Pin Cerdip



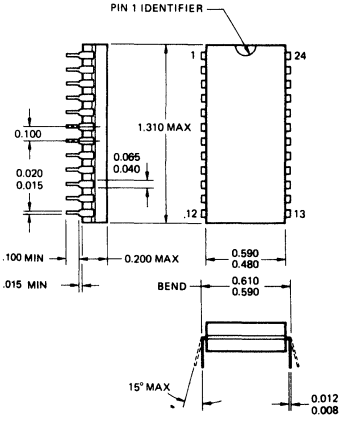
24-Lead Chip Carrier



24-Pin Ceramic

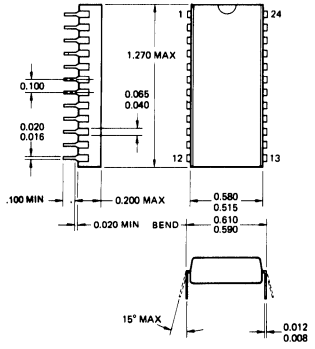


24-Pin Cerdip

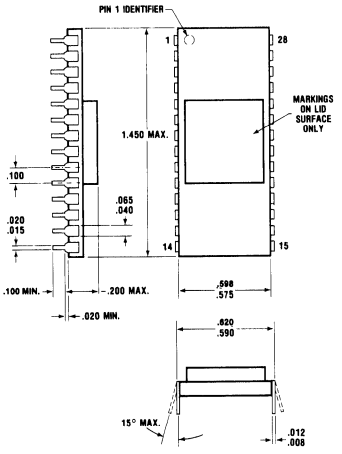


Packaging

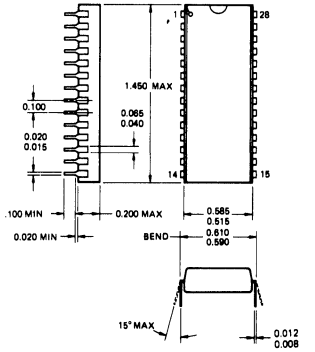
24-Pin Plastic



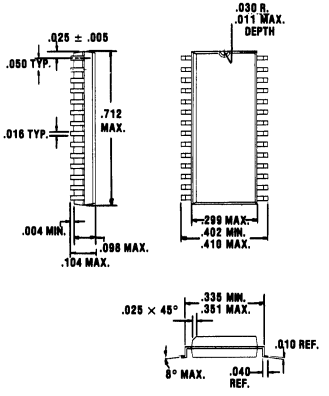
28-Pin Ceramic



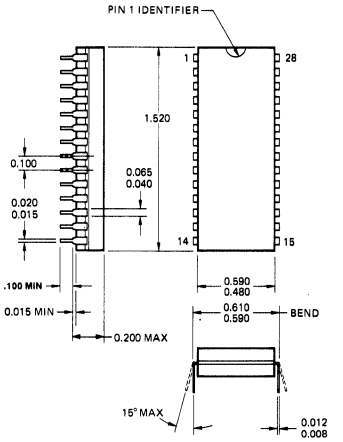
28-Pin Plastic



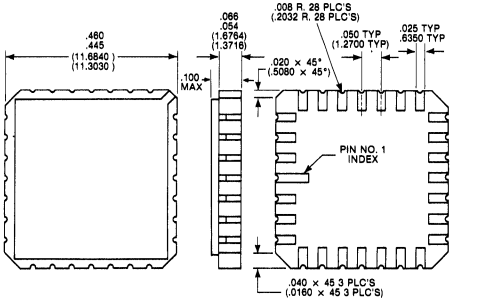
28-Lead Plastic S.O.I.C.



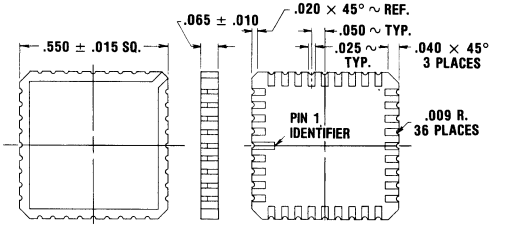
28-Pin Cerdip



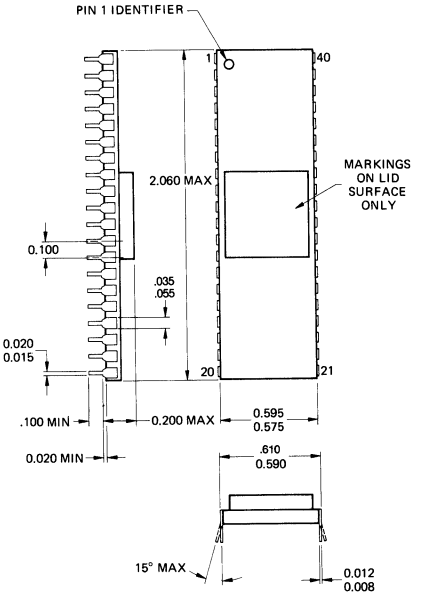
28-Lead Chip Carrier



36-Lead Ceramic Chip Carrier

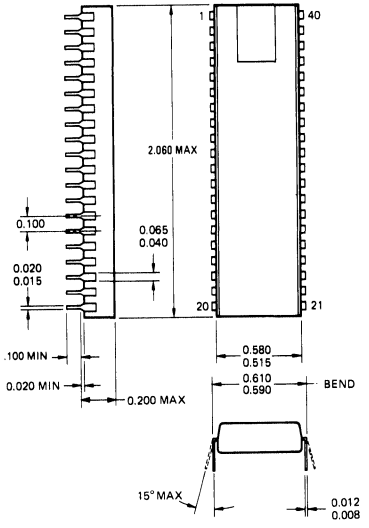


40-Pin Ceramic

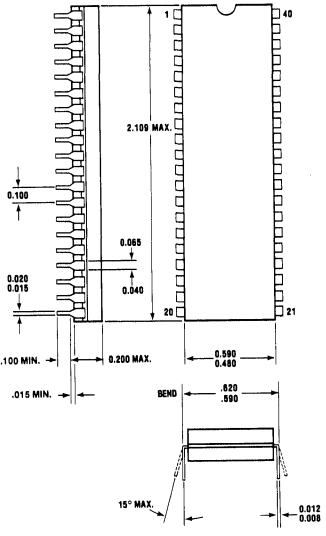


Packaging

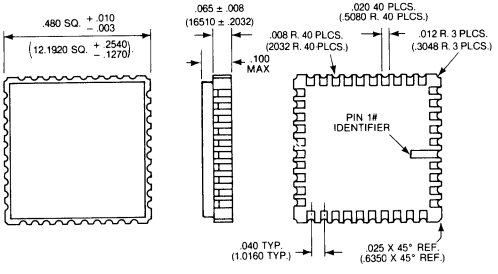
40-Pin Plastic



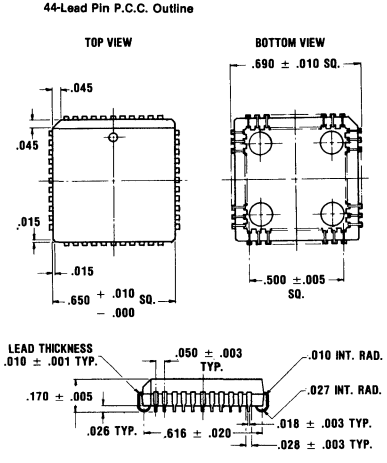
40-Pin Cerdip



40-Lead Chip Carrier

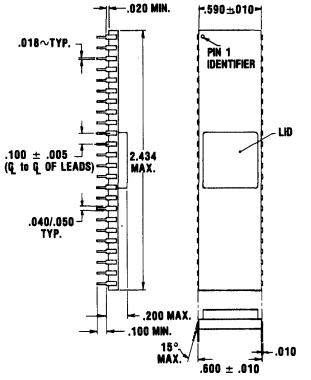


44-Lead Plastic Chip Carrier

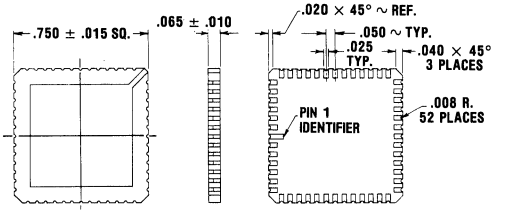


Packaging

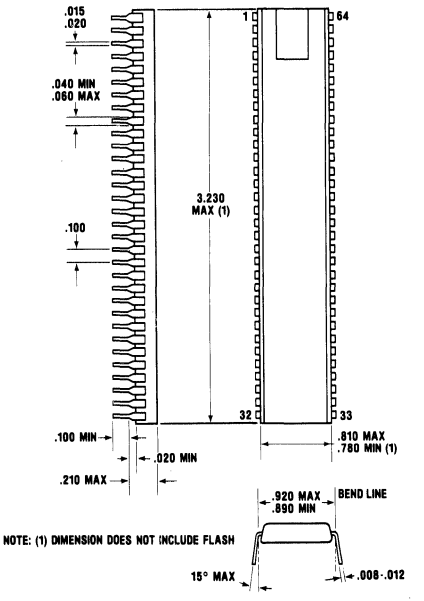
48-Lead Ceramic



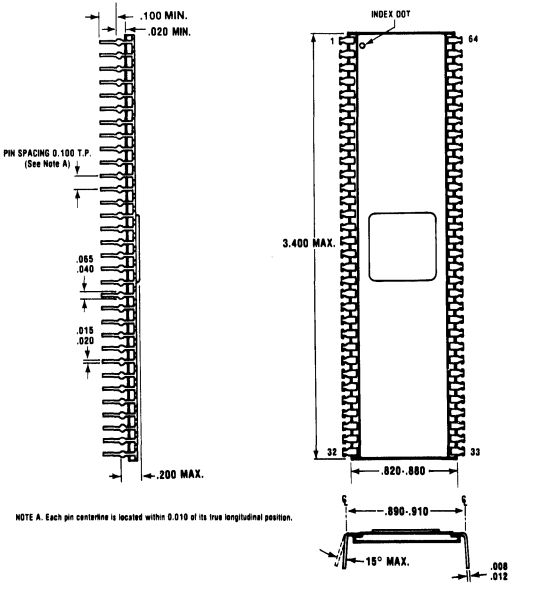
52-Lead Chip Carrier



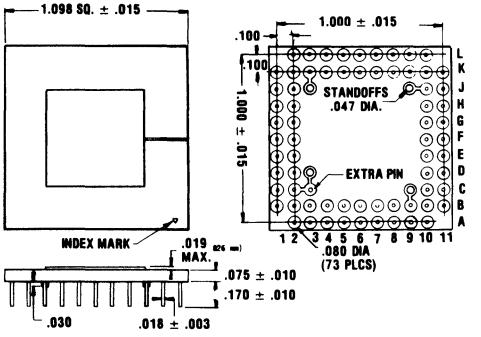
64-Pin Plastic



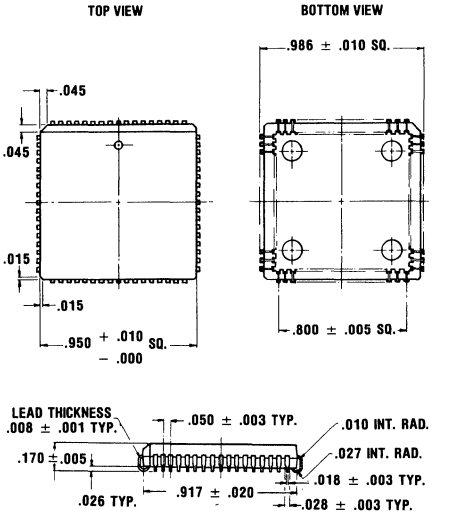
64-Pin Ceramic



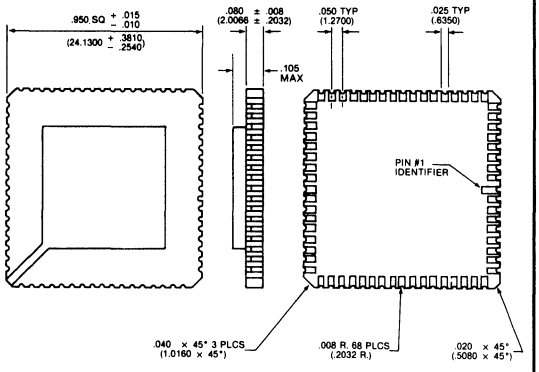
68-Pin Grid Array



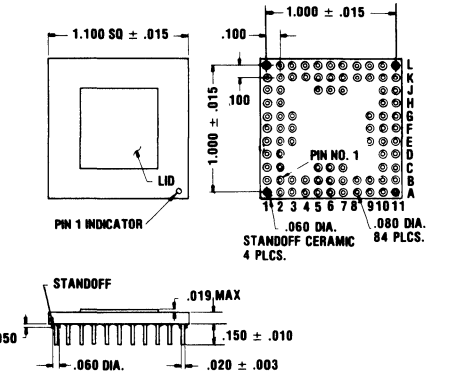
68-Lead Plastic Chip Carrier



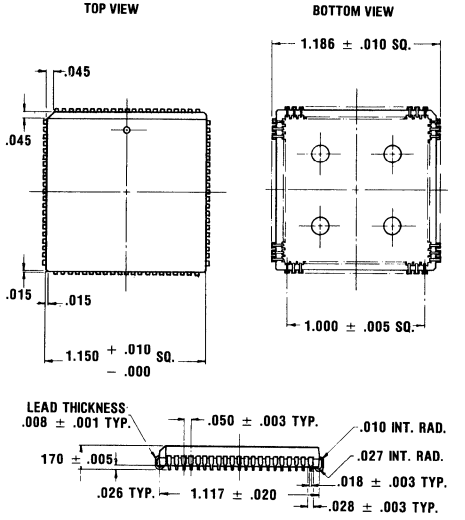
68-Lead Chip Carrier



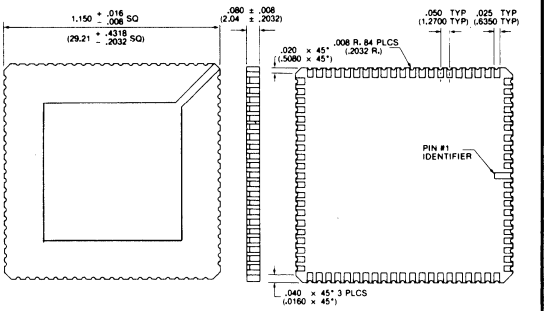
84-Pin Grid Array Outline



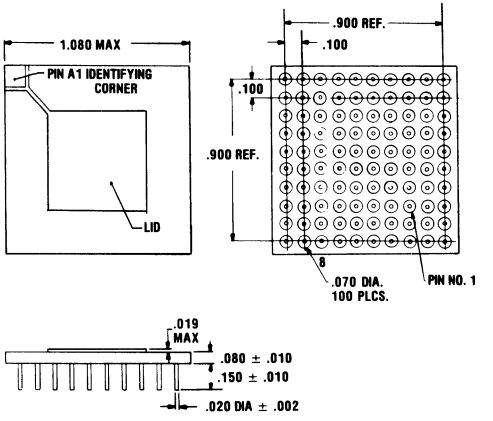
84-Lead Plastic Chip Carrier



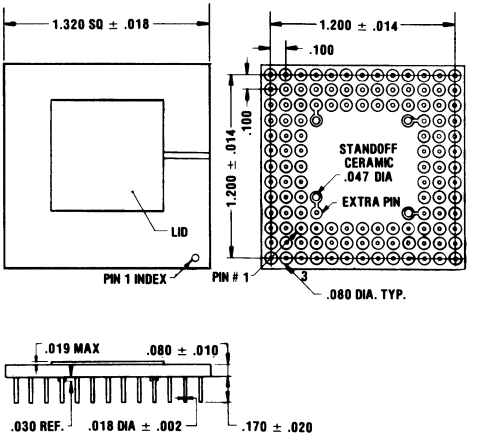
84-Lead Chip Carrier



100-Pin Array Outline

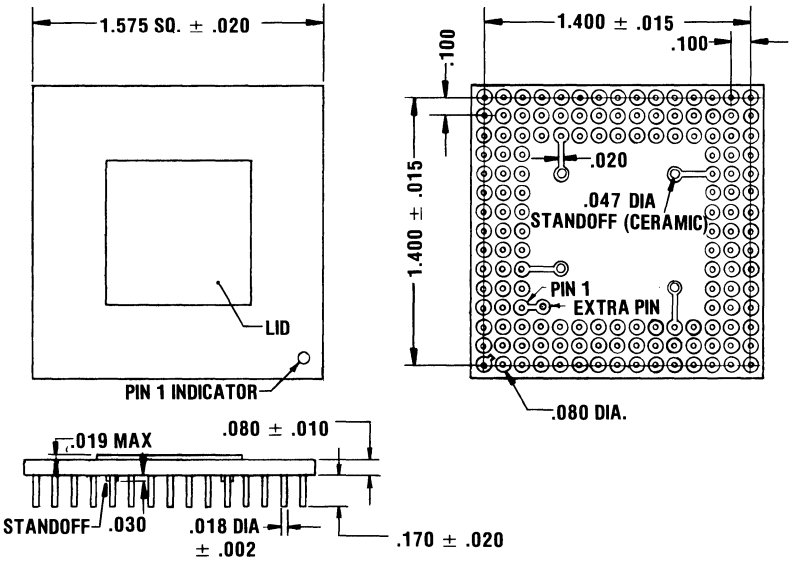


120-Pin Grid Array Outline



Packaging

144-Pin Grid Array Outline



Terms of Sale

TERMS OF SALE

JANUARY 1984

1. ACCEPTANCE: THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. PAYMENT:

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefore shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. TAXES: Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority, (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. F.O.B. POINT: All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, United Parcel Service (UPS), Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. DELIVERY: Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. PATENTS: The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. INSPECTION: Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY: The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. PRODUCTS NOT WARRANTED BY SELLER: The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES EXPRESSED, STATUTORY OR IMPLIED INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INFRINGEMENT AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products contact Seller.

10. PRICE ADJUSTMENTS: Seller's unit prices are based on certain material costs. These materials include, among other things, gold packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. VARIATION IN QUANTITY: If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. CONSEQUENTIAL DAMAGES: In no event shall Seller be liable for special, incidental or consequential damages.

13. GENERAL:

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities domestic or foreign.

(g) Unless otherwise agreed in a writing signed by both Buyer and Seller, Seller shall retain title to and possession of all tooling of any kind (including but not limited to masks and pattern generator tapes) used in the production of products furnished hereunder.

(h) Buyer, by accepting these products, certifies that he will not export or re-export the products furnished hereunder unless he complies fully with all laws and regulations of the United States relating to such export or re-export, including but not limited to the Export Administration Act of 1979 and the Export Administration Regulations of the U.S. Department of Commerce.

(i) Seller shall own all copyrights in or relating to each product developed by Seller whether or not such product is developed under contract with a third party.

14. GOVERNMENT CONTRACT PROVISIONS: If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Defense Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be - i.e., "Contracting Officer" shall mean "Buyer", "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Rhodesia and Certain Communist Areas; 7-103.16, Contract Work Hours and Safety Standards Act - Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity Clause; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government (only to the extent that Buyer's contract is terminated for the convenience of the government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-103.24, Responsibility for Inspection; 7-103.25, Commercial Bills of Lading Covering Shipments Under FOB Origin Contracts; 7-103.27, Listing of Employment Openings; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.15, Examination of Records by Comptroller General; 7-104.20, Utilization of Labor Surplus Area Concerns.

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