American Microsystems, Inc.

1.0 µm CMOS Gate Array Data Book

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AMI Semiconductors

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PREFACE

Since its founding in 1966, American Microsystems, Inc., headquartered in Pocatello, Idaho, has been the architect of the custom MOS/VLSI industry. Today, the company supports a continuum of Application Specific IC (ASIC) solutions including E^2 programmable logic, gate array, standard cell, and cell-based custom integrated circuits, with a goal of providing users with the design approach which best meets specific requirements of their application.

AMI believes that getting the optimum ASIC solution requires more than just an ASIC vendor--it requires a partner with a full range of ASIC alternatives, focused yet flexible design approaches and an eye toward innovation in a rapidly evolving field. Since the best design for your system may require a combination of programmable logic devices, gate arrays, standard cell designs or cell-based custom circuits, your success rests in selecting a vendor with a full spectrum of ASIC design alternatives as well as design methods that are both flexible and customer-controlled.

With its continuum of ASIC products and design options, AMI Semiconductors can offer you tailored, low-cost solutions to your ASIC needs--no matter how sophisticated or varied. And, we do it without sacrificing quality, reliability or innovation. Company-wide implementation of *Statistical Process Control (SPC)* to build quality into AMI's semiconductor products is just one example of how our products, design expertise and systems have evolved as your ASIC needs have changed and matured.

At AMI Semiconductors we are firmly committed to the philosophy that one- or two-product ASIC vendors with rigid design rules cannot provide the optimum solution. They offer a product, a design process--to which customers must adapt. At AMI, it's the other way around. We offer a variety of ASIC products and design interface flexibility. AMI offers solutions.

This data book provides you with the important information you need to design with AMI GDX series gate arrays. The GDX series is fabricated in a 1.0-micron, oxide-isolated, isoplaner silicon-gate CMOS technology. Members of the GDX series can be used to implement logic circuits as large as 120,000 usable gates.

Included in this data book are Design Information, ASIC Standard functions, our basic MSI and 7400 functions, and megacell functions.

For design software, complete technical data,or for application assistance or training, contact your local AMI sales office (see listing at back of data book).

SELECTION GUIDES

April, 1992

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Simple Gates

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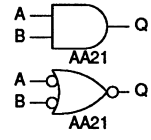
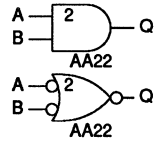
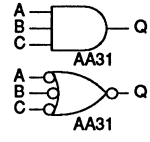
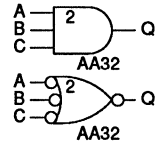
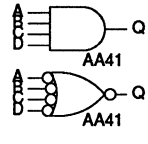
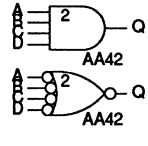
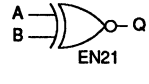
AA21	2	2-input AND gate		3-1
AA22	2	2-input AND gate		3-2
AA31	2	3-input AND gate		3-3
AA32	3	3-input AND gate		3-4
AA41	3	4-input AND gate		3-5
AA42	3	4-input AND gate		3-6
EN21	3	Exclusive NOR.		3-71

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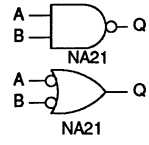
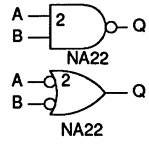
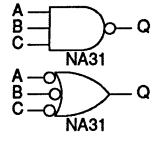
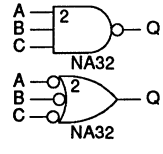
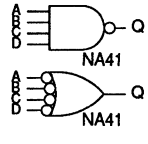
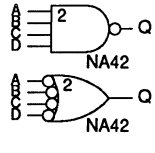
NA21	1	2-input NAND gate		3-157
NA22	2	2-input NAND gate		3-158
NA31	2	3-input NAND gate		3-159
NA32	3	3-input NAND gate		3-160
NA41	2	4-input NAND gate		3-161
NA42	4	4-input NAND gate		3-162

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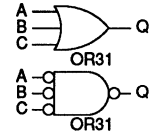
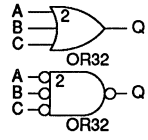
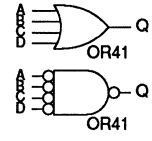
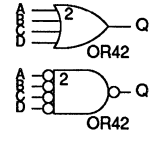
OR31	2	3-Input OR buffer.		3-205
OR32	3	3-Input OR buffer.		3-206
OR41	3	4-Input OR buffer.		3-207
OR42	3	4-Input OR buffer.		3-208

Complex Gates

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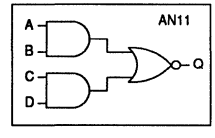
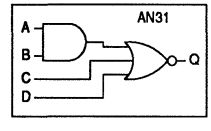
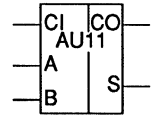
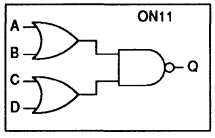
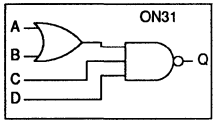
AN11	2	2x2-input AND into 2-input NOR.		3-7
AN31	2	2-input AND into 3-input NOR.		3-8
AU11	7	One bit full adder.		3-9

ON11	2	2x2-input OR into 2-input NAND.		3-201
ON31	2	2-input OR into 3-input NAND.		3-202

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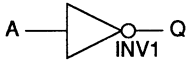
INV1	1	inverter		3-87
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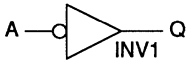
INV5	3	"		3-91
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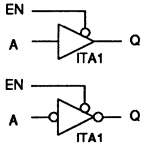
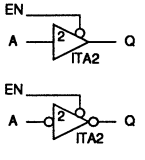
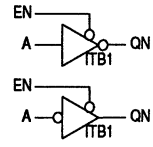
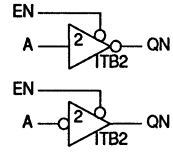
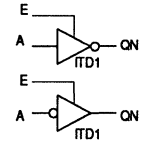
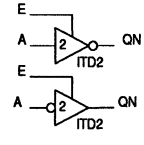
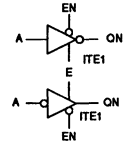
ITA1	2	Internal TS buffer, non-inverting.		3-126
ITA2	4	Internal TS buffer, non-inverting.		3-128

ITB1	2	Internal TS buffer, inverting.		3-129
ITB2	4	Internal TS buffer, inverting.		3-131
ITD1	2	Internal TS buffer, inverting.		3-132
ITD2	4	Internal TS buffer, inverting.		3-133
ITE1	1	Internal TS buffer, inverting.		3-134

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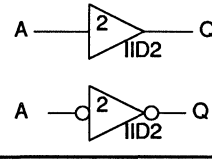
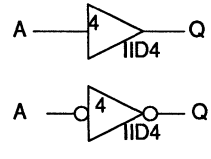
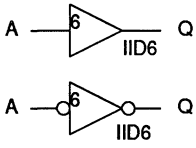
IID2	2	Non-inverting clock driver.		3-84
IID4	3	Non-inverting clock driver.		3-85

IID6	4	Non-inverting clock driver.		3-86

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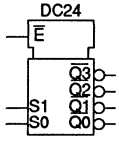
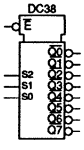
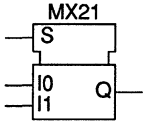
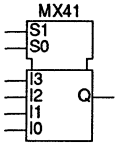
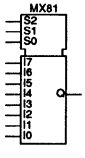
DC24	8	2:4 Line Decoder.		3-14
DC38	18	3:8 Line Decoder.		3-16
MX21	3	2:1 Digital Multiplexer.		3-151
MX41	8	4:1 Digital Multiplexer.		3-153
MX81	16	8:1 Digital Multiplexer.		3-155

Sequential Logic

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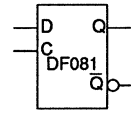
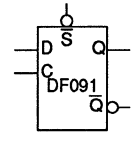
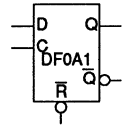
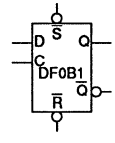
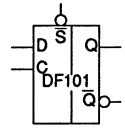
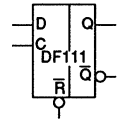
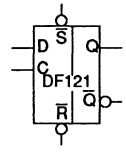
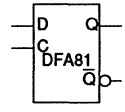
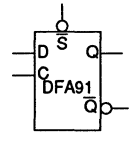
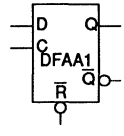
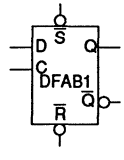
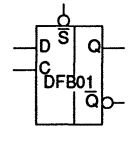
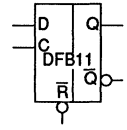
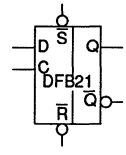
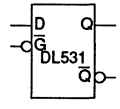
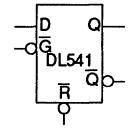
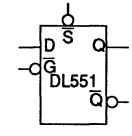
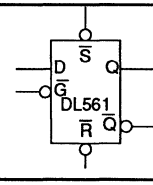
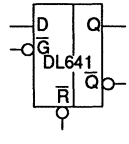
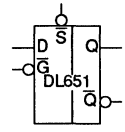
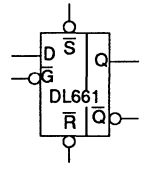
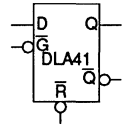
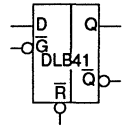
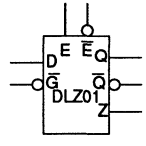
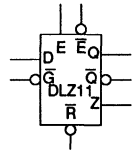
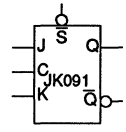
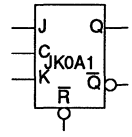
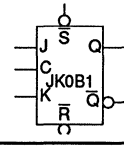
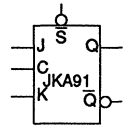
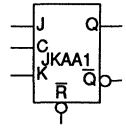
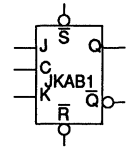
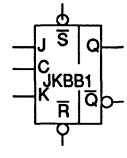
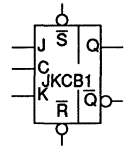
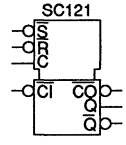
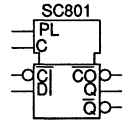
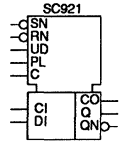
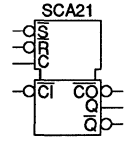
DF081	6	D-type F/F without set and reset.		3-18
DF091	7	D-type F/F with active low set.		3-20
DF0A1	7	D-type F/F with active low reset.		3-22
DF0B1	8	D-type F/F with active low set and reset.		3-24
DF101	8	D-type F/F with active low set. Buffered.		3-26
DF111	8	D-type F/F with active low reset, Buffered.		3-28

DF121	10	D-type F/F with active low set and reset. Buffered.		3-30
DFA81	5	D-type F/F without set and reset. Equivalent to DF081 with lower gate count.		3-32
DFA91	6	D-type F/F with active low set. Equivalent to DF091 with lower gate count.		3-34
DFAA1	6	D-type F/F with active low reset. Equivalent to DF0A1 with lower gate count.		3-36
DFAB1	7	D-type F/F with active low set and reset. Equivalent to DF0B1 with lower gate count.		3-38
DFB01	7	D-type F/F with active low set. Buffered. Equivalent to DF101 with lower gate count.		3-41

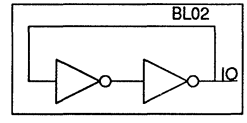
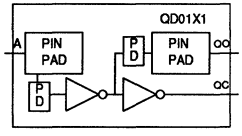
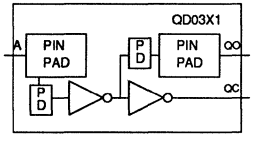
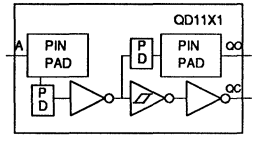
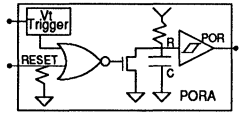
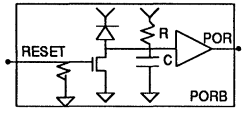
DFB11	7	D-type F/F with active low reset. Buffered. Equivalent to DF111 with lower gate count.		3-42
DFB21	8	D-type F/F with active low set and reset. Buffered. Equivalent to DF121 with lower gate count.		3-44
DL531	3	D-type latch without set or reset.		3-46
DL541	5	D-type latch with active low reset.		3-48
DL551	4	D-type latch with active low set.		3-50
DL561	5	D-type latch with active low set and reset.		3-52
DL641	6	D-type latch with active low reset. Buffered.		3-55

DL651	5	D-type latch with active low set. Buffered.		3-57
DL661	6	D-type latch with active low set and reset. Buffered		3-59
DLA41	4	D-type latch with active low reset. Equivalent to DL541 with lower gate count.		3-62
DLB41	5	D-type latch with active low reset. Buffered. Equivalent to DL641 with lower gate count.		3-63
DLZ01	4	D-type latch without set or reset and a dual-enable tri-state output.		3-65
DLZ11	5	D-type latch with active low reset, and a dual-enable tri-state output.		3-68

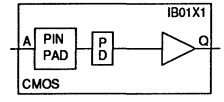
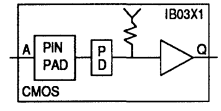
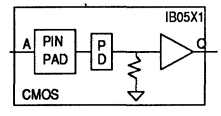
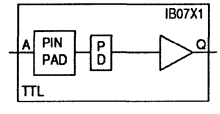
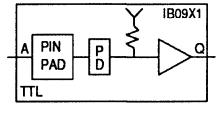
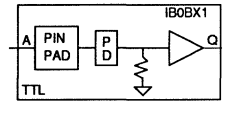
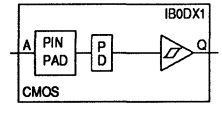
JK091	10	JK-type F/F with active low set. 	3-135
JK0A1	10	JK-type F/F with active low reset. 	3-137
JK0B1	13	JK-type F/F with active low set and reset. 	3-139
JKA91	9	JK-type F/F with active low set. Equivalent to JK091 with lower gate count. 	3-141
JKAA1	9	JK-type F/F with active low reset. Equivalent to JK0A1 with lower gate count. 	3-143
JKAB1	10	JK-type F/F with active low set and reset. Equivalent to JK0B1 with lower gate count. 	3-145
JKBB1	13	JK-type F/F with active low set and reset, and buffered output. 	3-147

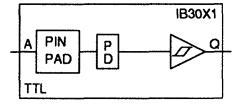
JKCB1	11	JK-type F/F with active low set and reset, and buffered output. Equivalent to JKBB1 with lower gate count.		3-149
SC121	16	Sync. counter, ripple carry with active low set and reset.		3-218
SC801	15	Sync. counter, async. load, ripple carry.		3-221
SC921	19	Sync. counter, async. load, ripple carry, with active low set and reset.		3-224
SCA21	12	Sync. counter, ripple carry with active low set and reset. Equivalent to SC121 with lower gate count.		3-227

Special Cells

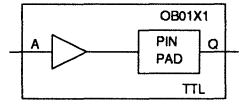
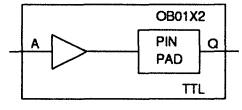
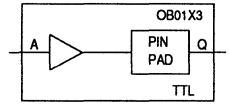
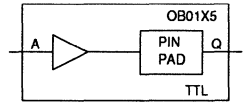
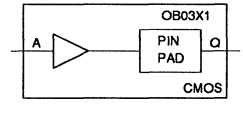
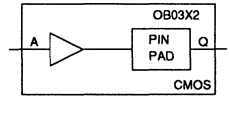
Name	Size	Description	Symbol	Page
BL02	7	Tri-state bus latch.		3-11
QD01X1	0	3.58 MHz (1 MHz - 10 MHz) crystal oscillator.		3-215
QD03X1	0	20 MHz (10 MHz -32 MHz) crystal oscillator.		3-216
QD11X1	0	32 KHz (1 KHz - 1 MHz) crystal oscillator, with Schmitt-trigger.		3-217
PORA	0	Power-on-reset circuit for 5 volt operation.		3-209
PORB	0	Power-on-reset circuit for 3 volt operation.		3-210

Input Pad Cells

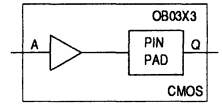
Name	Size	Description	Symbol	Page
IB01X1	0	CMOS input buffer.		3-75
IB03X1	0	CMOS input buffer with Pull-Up.		3-76
IB05X1	0	CMOS input buffer with Pull-Down.		3-77
IB07X1	0	TTL input buffer.		3-78
IB09X1	0	TTL input buffer with Pull-Up.		3-79
IB0BX1	0	TTL input buffer with Pull-down.		3-80
IB0DX1	0	CMOS Schmitt Trigger input buffer.		3-81

IB30X1	0	TTL Schmitt Trigger input buffer.		3-83

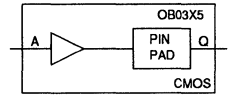
Output Pad Cells

Name	Size	Description	Symbol	Page
OB01X1	0	TTL output buffer, 1ma.		3-175
OB01X2	0	TTL output buffer, 2ma.		3-176
OB01X3	0	TTL output buffer, 4ma.		3-177
OB01X5	0	TTL ouput buffer, 8ma.		3-178
OB03X1	0	CMOS output buffer, 1ma.		3-179
OB03X2	0	CMOS output buffer, 2ma.		3-180

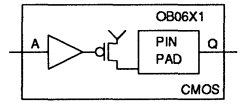
OB03X3	0	CMOS output buffer, 4ma.	3-181



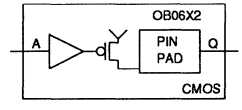
OB03X5	0	CMOS output buffer,8ma.	3-182



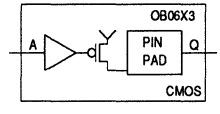
OB06X1	0	CMOS p-channel, open drain, inverting output buffer, 1ma.	3-183



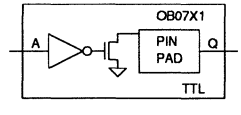
OB06X2	0	CMOS p-channel, open drain, inverting output buffer, 2ma.	3-184



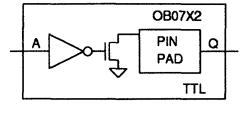
OB06X3	0	CMOS p-channel, open drain, inverting output buffer, 4ma.	3-185



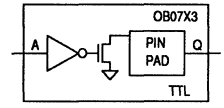
OB07X1	0	TTL n-channel open drain output buffer, 1ma.	3-186

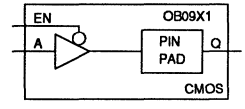


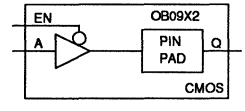
OB07X2	0	TTL n-channel open drain output buffer, 2ma.	3-187

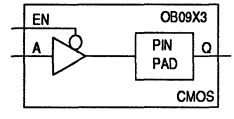


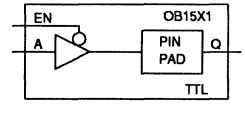
OB07X3	0	TTL n-channel open drain output buffer, 4ma.	3-188
OB09X1	0	CMOS 3-state output buffer, 1ma.	3-189
OB09X2	0	CMOS 3-state output buffer, 2ma.	3-190
OB09X3	0	CMOS 3-state output buffer, 4ma.	3-191
OB15X1	0	TTL 3-state output buffer, 1ma.	3-192
OB15X2	0	TTL 3-state output buffer, 2ma.	3-193
OB15X3	0	TTL 3-state output buffer, 4ma.	3-194

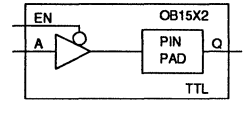


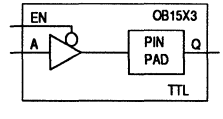




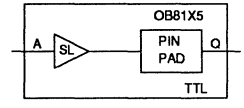


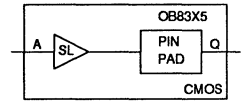


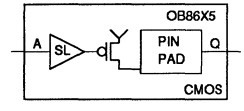


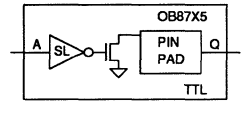


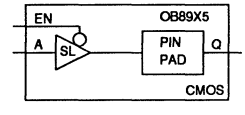
OB81X5	0	TTL output buffer, 8ma, with controlled slew rate output.	3-195
OB83X5	0	CMOS output buffer, 8ma, with controlled slew rate output.	3-196
OB86X5	0	CMOS inverting open drain p-channel output buffer, 8ma, with controlled slew rate output.	3-197
OB87X5	0	TTL open drain n-channel output buffer, 8ma, with controlled slew rate output.	3-198
OB89X5	0	CMOS Tri-state output buffer, 8ma, with controlled slew rate output.	3-199
OB95X5	0	TTL Tri-state output buffer, 8ma, with controlled slew rate output.	3-200

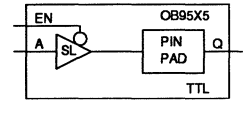




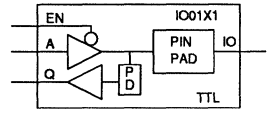
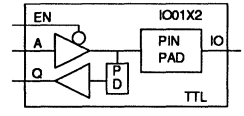
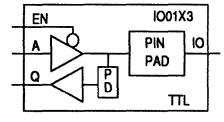
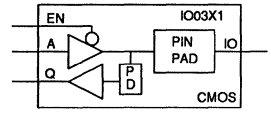
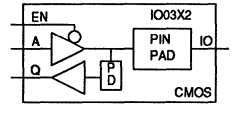
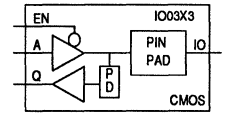
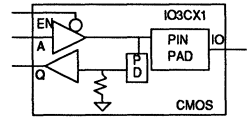




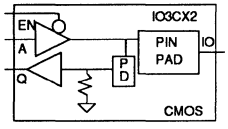




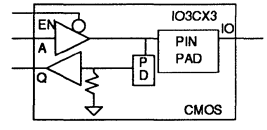
Input/Output Pad Cells

Name	Size	Description	Symbol	Page
IO01X1	0	TTL I/O buffer, 1ma.		3-93
IO01X2	0	TTL I/O buffer, 2ma.		3-94
IO01X3	0	TTL I/O buffer, 4ma.		3-95
IO03X1	0	CMOS I/O buffer, 1ma.		3-97
IO03X2	0	CMOS I/O buffer, 2ma.		3-98
IO03X3	0	CMOS I/O buffer, 4ma.		3-99
IO3CX1	0	CMOS I/O buffer with Pull-down, 1ma.		3-101

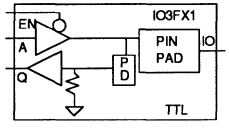
IO3CX2	0	CMOS I/O buffer with Pull-down, 2ma.	3-102



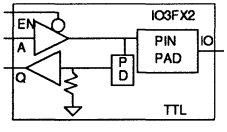
IO3CX3	0	CMOS I/O buffer with Pull-down, 4ma.	3-103



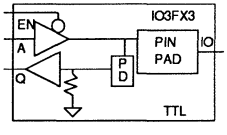
IO3FX1	0	TTL I/O buffer with Pull-down, 1ma.	3-104



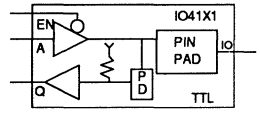
IO3FX2	0	TTL I/O buffer with Pull-down, 2ma.	3-105



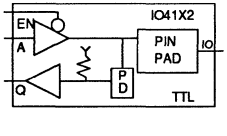
IO3FX3	0	TTL I/O buffer with Pull-down, 4ma.	3-106

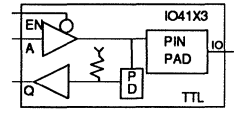
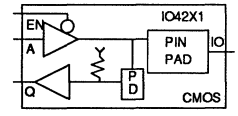
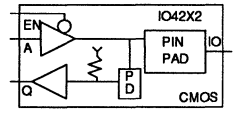
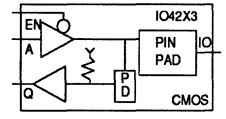
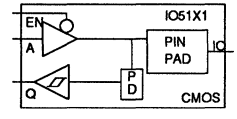
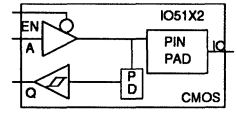
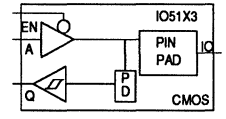


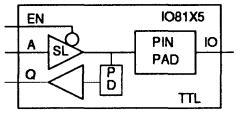
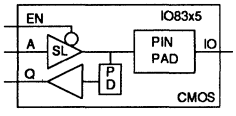
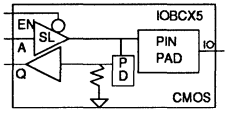
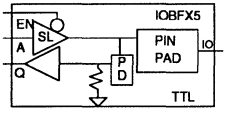
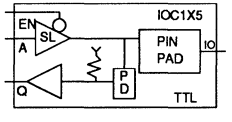
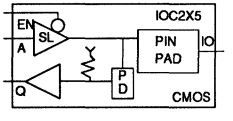
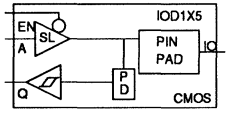
IO41X1	0	TTL I/O buffer w/ pull-up, 1ma.	3-107



IO41X2	0	TTL I/O buffer w/ pull-up, 2ma.	3-108



IO41X3	0	TTL I/O buffer w/ pull-up, 4ma. 	3-109
IO42X1	0	CMOS I/O buffer w/ pull-up, 1ma. 	3-111
IO42X2	0	CMOS I/O buffer w/ pull-up, 2ma. 	3-112
IO42X3	0	CMOS I/O buffer w/ pull-up, 4ma. 	3-113
IO51X1	0	CMOS I/O buffer w/ Schmitt Trigger input, 1ma. 	3-115
IO51X2	0	CMOS I/O buffer w/ Schmitt Trigger input, 2ma. 	3-116
IO51X3	0	CMOS I/O buffer w/ Schmitt Trigger input, 4ma. 	3-117

IO81X5	0	TTL I/O Tri-state buffer, 8ma, with controlled slew rate output.		3-119
IO83X5	0	CMOS I/O Tri-state buffer, 8ma, with controlled slew rate output.		3-120
IOBCX5	0	CMOS I/O Tri-state buffer with Pull-down, and controlled slew rate output, 8ma.		3-121
IOBFX5	0	TTL I/O Tri-state buffer with Pull-down, and controlled slew rate output, 8ma.		3-122
IOC1X5	0	TTL I/O Tri-state buffer with Pull-up, and controlled slew rate output, 8ma.		3-123
IOC2X5	0	CMOS I/O Tri-state buffer with Pull-up, and controlled slew rate output, 8ma.		3-124
IOD1X5	0	CMOS I/O Tri-state buffer with Schmitt-trigger, and controlled slew rate output, 8ma.		3-125

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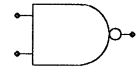
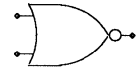
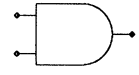
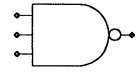
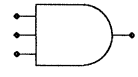
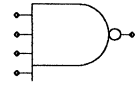
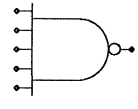
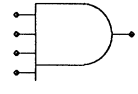
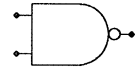
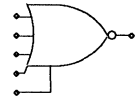
Simple Gates

Name	Size	Description	Symbol
74LS00	1	2 Input NAND	
74LS02	1	2 Input NOR	
74LS08	2	2 Input AND	
74LS10	2	3 Input NAND	
74LS11	2	3 Input AND	
74LS13	2	4 Input NAND	
74LS20	2	5 Input NAND	
74LS21	3	4 Input AND	
74LS24	1	2 Input NAND	
74LS25	4	4 Input NOR with Strobe	

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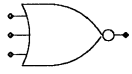
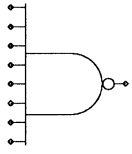
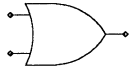
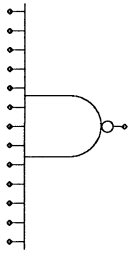
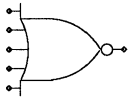
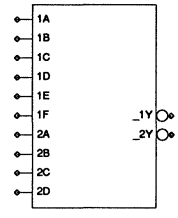
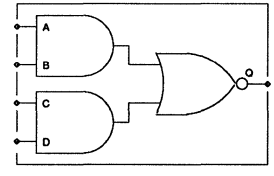
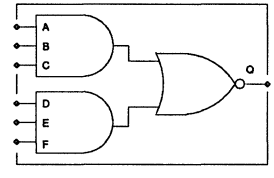
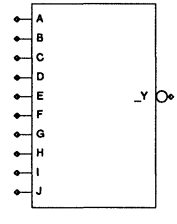
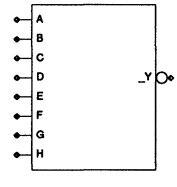
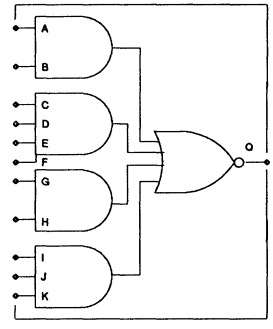
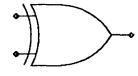
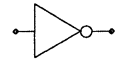
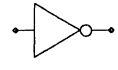
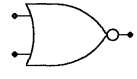
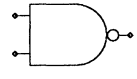
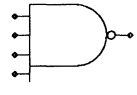
Name	Size	Description	Symbol
74LS27	2	3 Input NOR	
74LS30	6	8 Input NAND	
74LS32	2	2 Input OR	
74LS133	10	13 Input NAND	
74LS260	3	5-input NOR gate	

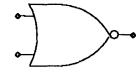
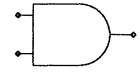
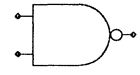
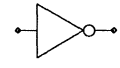
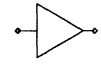
Complex Gates

Name	Size	Description	Symbol
74LS51	10	And-or-invert gates	
74LS51A	2	And-Or-Invert gate	
74LS51B	5	2 Wide 3 Input And-Or-Invert Gate	
74LS54	10	4 Wide And-Or-Invert Gate	
74LS55	7	2 Wide 4 Input And-Or-Invert Gate	

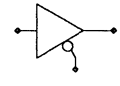
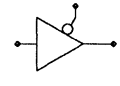
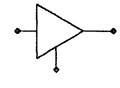
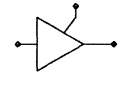
Name	Size	Description	Symbol
74LS64	11	4-2-3-2 Input And-Or-Invert Gate	
74LS86	3	2 Input Exclusive OR	

Non-Inverting And Inverting Drivers

Name	Size	Description	Symbol
74LS04	1	Inverter	
74LS14	1	Inverter	
74LS28	1	2 Input NOR Buffer	
74LS37	1	2 Input NAND Buffer	
74LS40	2	4 Input NAND Buffer	

Name	Size	Description	Symbol
74LS805	5	2 Input NOR Driver	
74LS808	4	2 Input AND Driver	
74LS1000	5	2 Input NAND Driver	
74LS1004	3	Inverting Driver	
74LS1034	4	Driver	

Internal Tri-State Drivers

Name	Size	Description	Symbol
74LS125	4	Bus Buffer w/3-state Output	
74LS125A	4	Bus Buffers With 3-State Outputs	
74LS126	3	Bus Buffer w/3-state Output	
74LS126A	3	Bus Buffers With 3-State Outputs	

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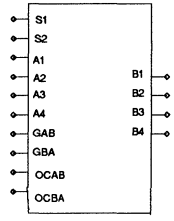
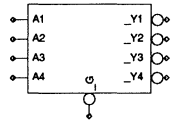
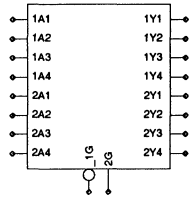
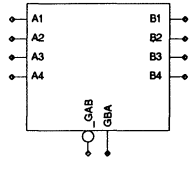
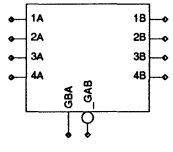
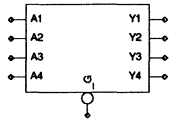
Name	Size	Description	Symbol
74LS226	94	4 Bit Parallel Latched Bus Transceiver w/3-State Outputs	
74LS240	18	Octal Buffers and Line Drivers w/inverted 3-State Outputs	
74LS241	26	Octal Buffers and Line Drivers w/3-State Outputs and Complementary Gates	
74LS242	18	Quadruple Bus Transceiver w/Inverted Outputs	
74LS243	26	Quadruple Bus Transceiver	
74LS244	26	Octal Buffers and Line Drivers w/3-State Outputs	

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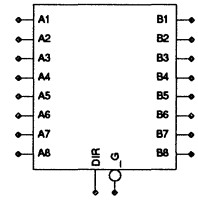
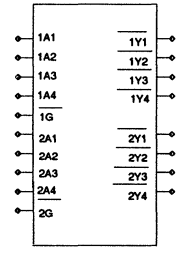
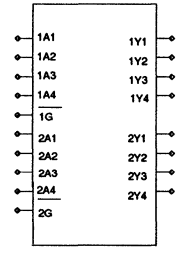
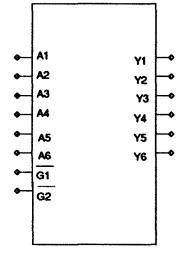
Name	Size	Description	Symbol
74LS245	54	Octal Bus Transceiver w/3-State Outputs	
74LS340	18	Octal Buffers and Line Drivers w/Inverted 3-State Outputs	
74LS344	26	Octal Buffers and Line Drivers w/3-State Outputs	
74LS365	21	Hex Bus Drivers w/3-State Outputs	

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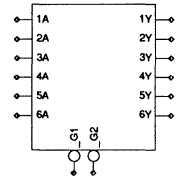
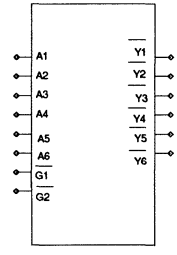
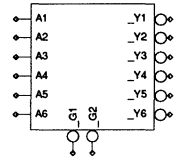
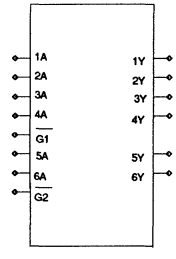
Name	Size	Description	Symbol
74LS365A	34	Hex bus drivers w/3-state outputs	
74LS366	15	Hex Bus Drivers w/3-State Inverted Outputs	
74LS366A	28	Hex bus drivers w/3-state outputs	
74LS367	20	Hex Bus Drivers w/3-State Outputs	

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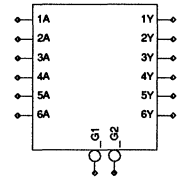
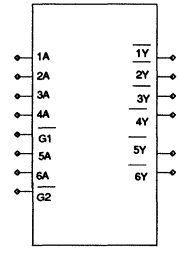
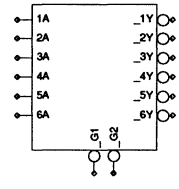
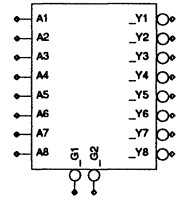
Name	Size	Description	Symbol
74LS367A	22	Hex bus drivers w/3-state outputs	
74LS368	14	Hex Bus Drivers w/3-State inverted Outputs	
74LS368A	16	Hex bus drivers w/3-state outputs	
74LS540	19	Octal Buffers and Line Drivers w/3-State Inverted Outputs	

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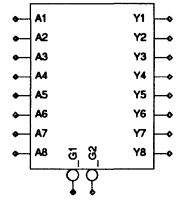
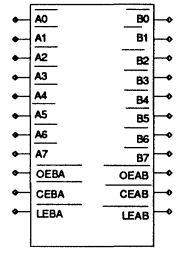
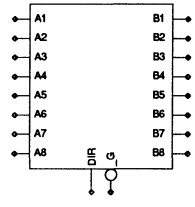
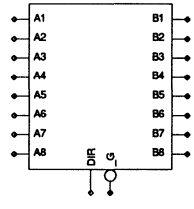
Name	Size	Description	Symbol
74LS541	27	Octal Buffers and Line Drivers w/3-State Outputs	
74LS544	92	Octal Registered Bus Transceiver w/3-State Inverted Outputs	
74LS640	38	Octal Bus Transceiver w/3-State Inverting Outputs	
74LS643	52	Octal bus transceivers	

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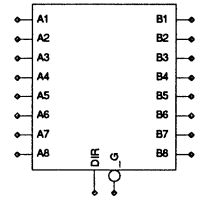
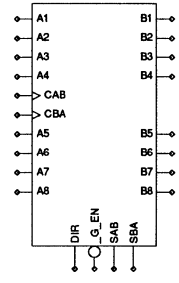
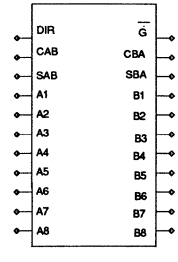
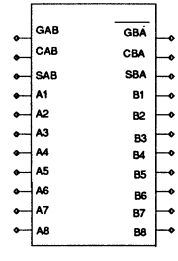
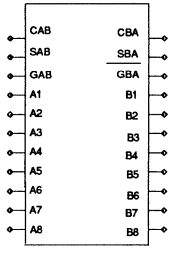
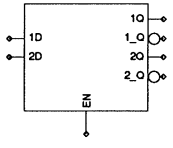
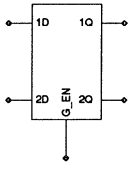
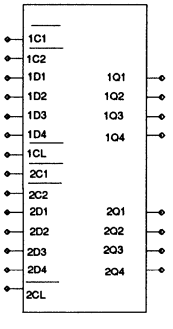
Name	Size	Description	Symbol
74LS645	54	Octal Bus Transceiver w/3-State Outputs	
74LS646	189	Octal Bus Transceiver and Register w/3-State Outputs	
74LS648	173	Octal Bus Transceiver and Register w/3-State Inverted Outputs	
74LS651	169	Octal Bus Transceiver and Register w/3-State Outputs	

Name	Size	Description	Symbol
74LS652	185	Octal Bus Transceiver and Register w/3-State Inverted Outputs	

Latches

Name	Size	Description	Symbol
74LS75	22	4 Bit Bistable Latch	
74LS77	8	4-bit Bistable Latch.	
74LS116	44	Dual 4 Bit Latches w/Clear	

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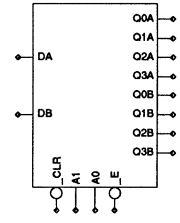
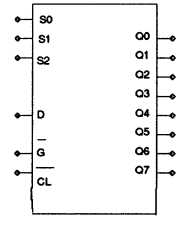
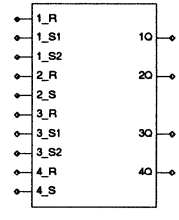
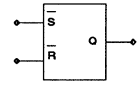
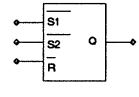
Name	Size	Description	Symbol
74LS256	74	Dual 4-bit addressable latch	
74LS259	65	8 Bit Addressable Latch	
74LS279	12	Quad SN, RN latches	
74LS279A	3	SN-RN Latch	
74LS279B	4	SN1-SN2-RN Latch	

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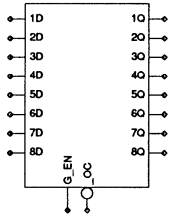
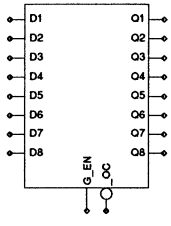
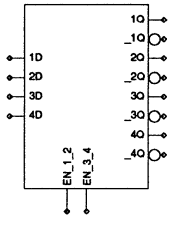
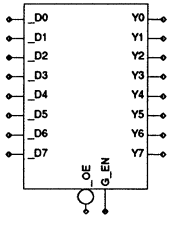
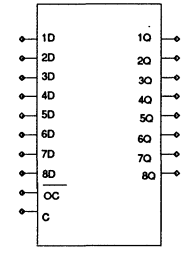
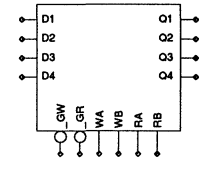
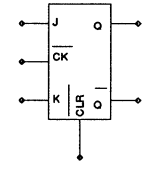
Name	Size	Description	Symbol
74LS363	50	8-bit octal transparent latch with 3-state outputs	
74LS373	42	Octal D Latch w/3-State Outputs	
74LS375	22	4 Bit Bistable Latch	
74LS533	61	8-bit latches w/inverting outputs	

Name	Size	Description	Symbol
74LS573	42	Octal D Latch w/3-State Outputs	

Memory

Name	Size	Description	Symbol
74LS670	129	4-by-4 Register Files w/3-State Outputs	

Flip Flops

Name	Size	Description	Symbol
74LS73	13	J-K Flip Flop w/clear	

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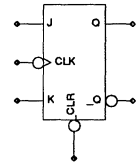
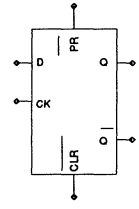
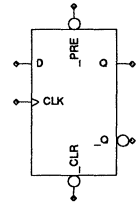
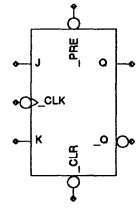
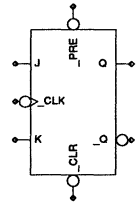
Name	Size	Description	Symbol
74LS73A	11	Dual J-K flip-flop w/clr	
74LS74	9	D Positive Edge Trig Flip Flop w/Preset and Clear	
74LS74A	7	Dual D flip-flop positive-edge triggered w/pre and clr	
74LS76	13	J-K Flip Flop w/Preset and Clear	
74LS76A	11	J-K Flip Flop w/Preset and Clear	

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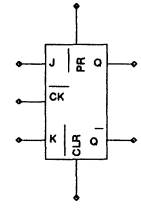
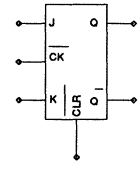
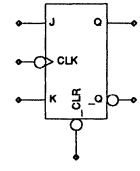
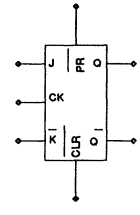
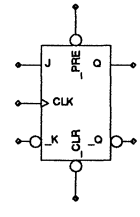
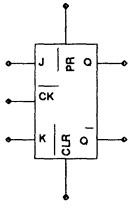
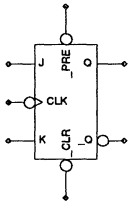
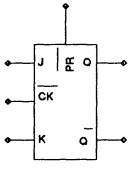
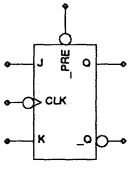
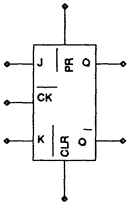
Name	Size	Description	Symbol
74LS78	13	J-K Flip Flop w/Preset and Clear	
74LS107	13	J-K Flip Flop w/Clear	
74LS107A	11	J-K Flip-Flop With Clear	
74LS109	13	J-K Positive Edge Trig Flip Flop w/Preset and Clear	
74LS109A	11	J-K Positive Edge Triggered Flip-Flop With Preset And Clear	

Name	Size	Description	Symbol
74LS112	13	J-K Flip Flop w/Preset and Clear	
74LS112A	11	J-K Negative Edge Triggered Flip-Flops with Preset And Clear	
74LS113	12	J-K Flip Flop w/Preset	
74LS113A	10	J-K Negative Edge Triggered Flip-Flops With Preset	
74LS114	13	J-K Flip Flop w/Preset and Clear	

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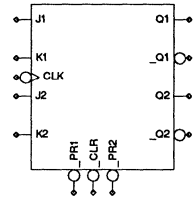
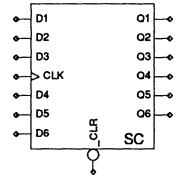
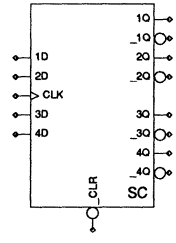
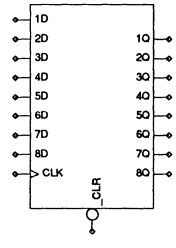
Name	Size	Description	Symbol
74LS114A	21	Dual J-K Negative Edge Triggered Flip-Flops with Preset, Clear, and Common Clock	
74LS174	46	Hex D Flip Flops w/Clear	
74LS175	35	Quadruple D Flip Flops w/Clear	
74LS273	60	Octal D Positive Edge Trig Flip Flop w/Clear	

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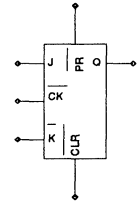
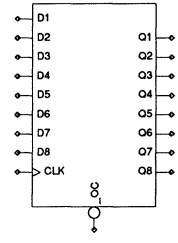
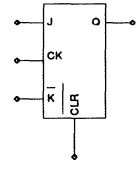
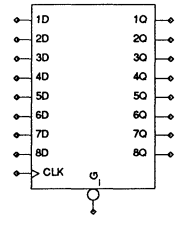
Name	Size	Description	Symbol
74LS276	13	J-KN Flip Flop w/Preset and Clear	
74LS374	59	Octal D Positive Edge Trig Flip Flop w/3-State Outputs	
74LS376	12	J-KN Positive Edge Trig Flip Flop w/Clear	
74LS377	54	Octal D Flip Flop w/Enable	

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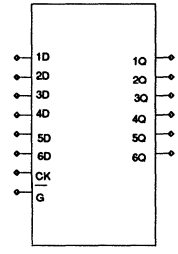
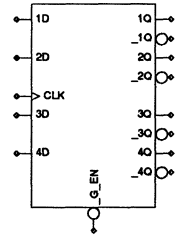
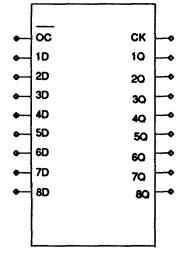
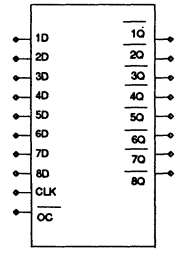
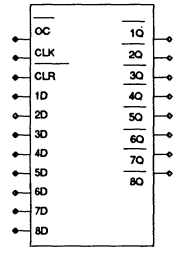
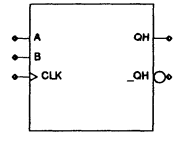
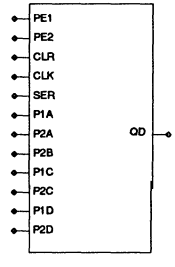
Name	Size	Description	Symbol
74LS378	42	Hex D Flip Flop w/Enable	
74LS379	34	Quad D Flip Flop w/Enable	
74LS574	59	Octal D Positive Edge Trig Flip Flops w/3-State Outputs	
74LS576	59	Octal D Positive Edge Trig Flip Flops w/3-State Inverted Outputs	

Name	Size	Description	Symbol
74LS577	68	Octal D Positive Edge Trig Flip Flops w/3-State Inverted Outputs and Synchronous Clear	

Registers

Name	Size	Description	Symbol
74LS91	46	8 Bit Shift Register	

74LS94	42	4 Bit Presettable Shift Register w/Dual Source	

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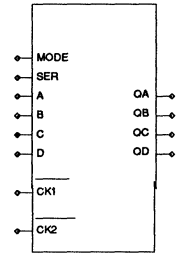
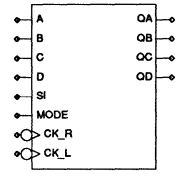
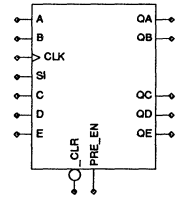
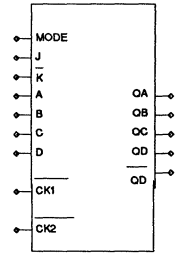
Name	Size	Description	Symbol
74LS95	37	4 Bit Right-shift Left-shift Register w/Synchronous Load	
74LS95B	45	4-bit parallel-access shift register	
74LS96	50	5 Bit Presettable Shift Register	
74LS99	56	4 bit Right-shift Left-shift Register w/Synchronous Load and J-KN Serial Input	

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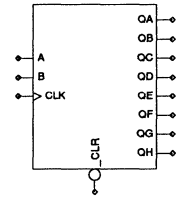
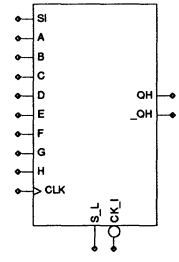
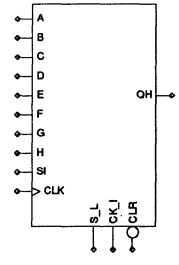
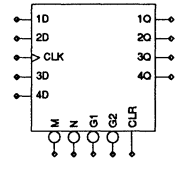
Name	Size	Description	Symbol
74LS164	62	8 Bit Parallel Out Serial Shift Register	
74LS165	88	8 Bit Presettable Shift Register	
74LS166	71	8 Bit Shift Register w/Synchronous Load	
74LS173	46	4 bit D Register w/3-State Outputs	

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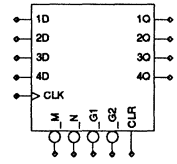
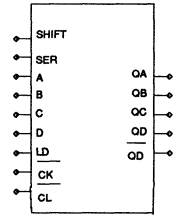
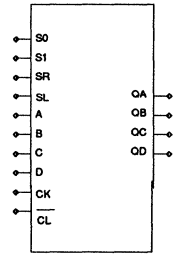
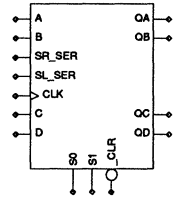
Name	Size	Description	Symbol
74LS173A	49	4-Bit D-Type Registers with 3-State Outputs	
74LS179	53	4-Bit Shift Register w/Clear, Hold and Synchronous Load	
74LS194	56	4 Bit Bidirectional Universal Shift Register	
74LS194A	56	4-Bit Bidirectional Universal Shift Register	

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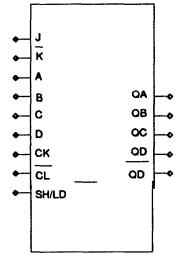
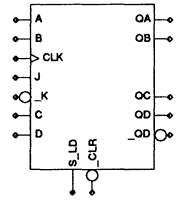
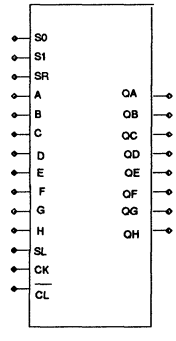
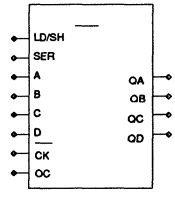
Name	Size	Description	Symbol
74LS195	44	4 Bit Shift Register w/Clear, Synchronous Load and J-KN Serial Input	
74LS195A	43	4-Bit Parallel-Access Shift-Register	
74LS198	101	8 Bit Bidirectional Shift Register w/Synchronous Load	
74LS295	39	4 Bit Right-shift Left-shift Register w/3-State Outputs and Synchronous Load	

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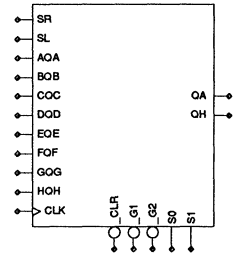
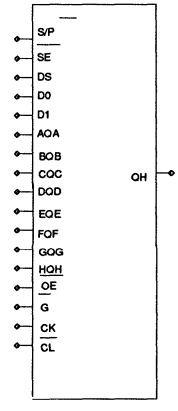
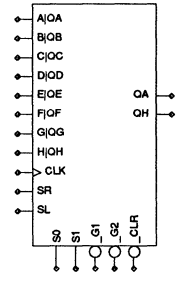
Name	Size	Description	Symbol
74LS299	127	8 Bit Universal Shift/Storage Register with I/O Ports and Asynchronous Clear	
74LS322	121	8 Bit Shift Register w/Sign Extend and I/O Ports	
74LS323	123	8 Bit Universal Shift/Storage Register with I/O Ports and Synchronous Clear	

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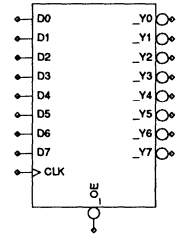
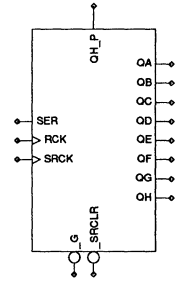
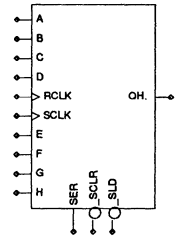
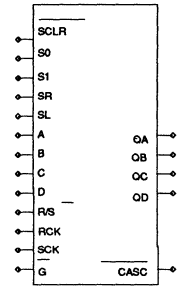
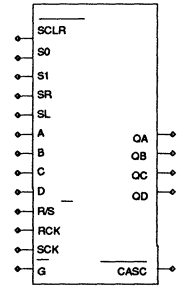
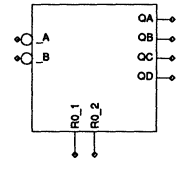
Name	Size	Description	Symbol
74LS534	69	8-bit latches w/inverting outputs and common clk, clr	
74LS595	125	8-bit shift register w/output latches	
74LS597	135	8-bit shift register w/input latches	

Name	Size	Description	Symbol
74LS671	109	4 Bit Universal Shift Register/Latch w/3/State Outputs and Asynchronous Clear	
74LS672	118	4 Bit Universal Shift Register/Latch w/3/State Outputs and Synchronous Clear	

Binary Counters

Name	Size	Description	Symbol
74LS93	31	Divide-by 2/Divide-by-4 Counter	

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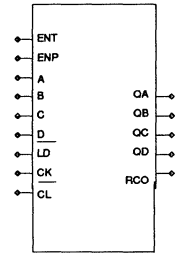
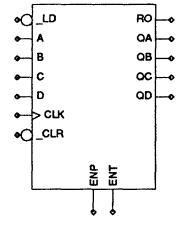
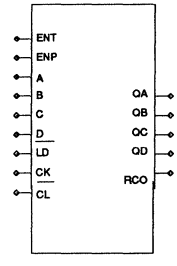
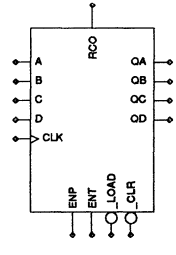
Name	Size	Description	Symbol
74LS160	71	Synchronous Decade Counter w/Asynchronous Clear	
74LS160A	74	Synchronous 4-Bit Counter	
74LS161	75	Synchronous 4-bit Binary Counter w/Asynchronous Clear	
74LS161A	77	Synchronous 4-Bit Binary Counter With Direct Clear	

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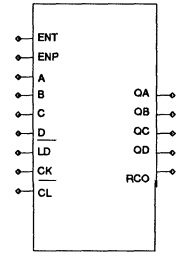
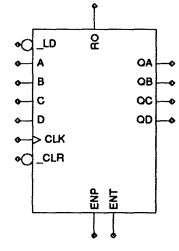
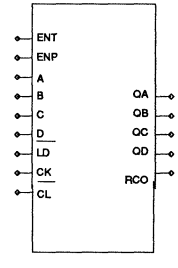
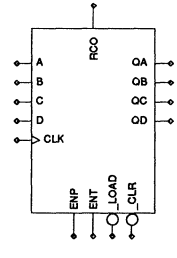
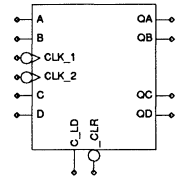
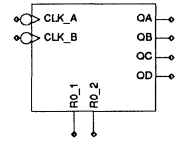
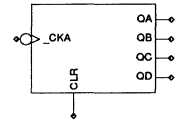
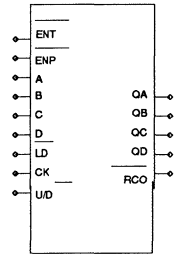
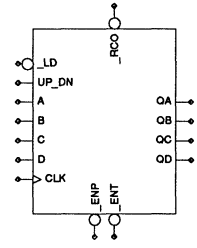
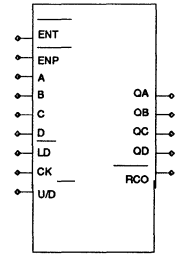
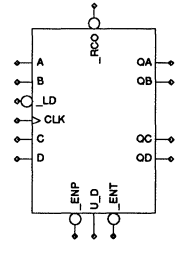
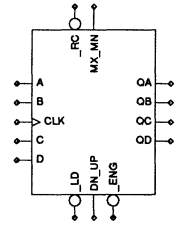
Name	Size	Description	Symbol
74LS162	70	Synchronous Decade Counter	
74LS162A	68	Synchronous 4-Bit Binary Counter With Direct Clear	
74LS163	65	Synchronous 4-bit binary Counter	
74LS163A	65	Synchronous 4-Bit Binary Counter With Direct Clear	

Name	Size	Description	Symbol
74LS197	56	Divide-by 2/Divide-by-4 Presettable Counter/Latch	
74LS293	31	Divide-by 2/Divide-by-4 Counter	
74LS393	30	Divide-by 2/Divide-by-4 Counter	

Up/Down Counters

Name	Size	Description	Symbol
74LS168	90	Synchronous Up/Down Decade Counter	

Name	Size	Description	Symbol
74LS168A	86	Synchronous 4-Bit Up/Down Decade Counter	
74LS169	81	Synchronous Up/Down 4±bit Binary Counter	
74LS169A	80	Synchronous 4-Bit Up/Down Counter	
74LS190	95	Presettable Synchronous Up/Down Decade Counter	

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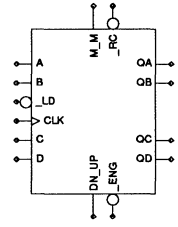
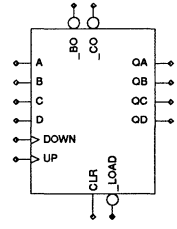
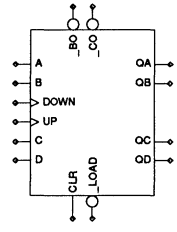
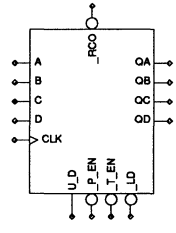
Name	Size	Description	Symbol
74LS191	88	Presettable Synchronous Up/Down 4-bit Binary Counter	
74LS192	88	Presettable Synchronous Up/Down Decade Counter w/Clear	
74LS193	81	Presettable Synchronous Up/Down 4-bit Binary Counter w/Clear	
74LS668	93	Synchronous Up/Down Decade Counter	

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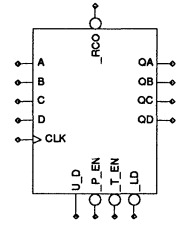
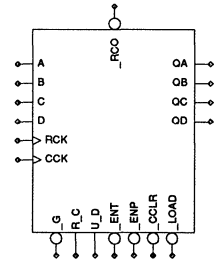
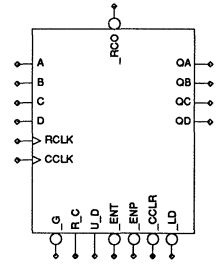
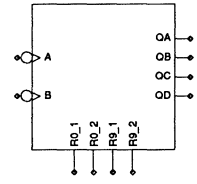
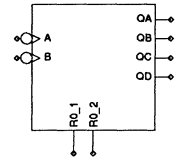
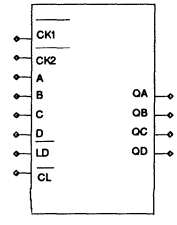
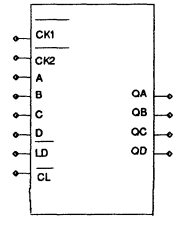
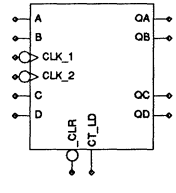
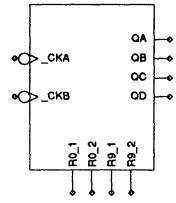
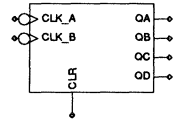
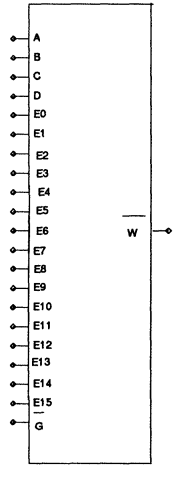
Name	Size	Description	Symbol
74LS669	81	Synchronous Up/Down 4 Bit Binary Counter	
74LS697	127	Sync. up/down counter w/output registers and multiplex 3-state outputs	
74LS699	123	Sync. up/down counter w/output registers and multiplex 3-state outputs	

Miscellaneous Counters

Name	Size	Description	Symbol
74LS90	40	Decade/Bi-quinary Counter	
74LS92	37	Divide by 2/Bi-divide-by-6 Counter	
74LS176	62	Decade/Bi-quinary Presettable Counter/Latch	
74LS177	56	Divide-by 2/Divide-by-4 Presettable Counter/Latch	
74LS196	62	Decade/Bi-quinary Presettable Counter/Latch	

Name	Size	Description	Symbol
74LS290	42	Decade/Bi-quinary Counter	
74LS390	35	Decade/Bi-quinary Counter	

Multiplexers

Name	Size	Description	Symbol
74LS150	43	1 of 16 Multiplexer w/Inverted Outputs	

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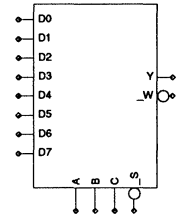
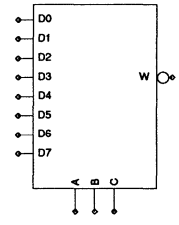
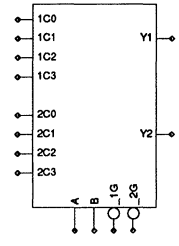
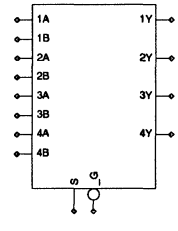
Name	Size	Description	Symbol
74LS151	23	1 of 8 Multiplexer	
74LS152	21	1 of 8 Multiplexer w/Inverted Outputs and No Strobe	
74LS153	13	Dual 4 to 1 line Multiplexer	
74LS157	14	Quadruple 2 to 1 line Multiplexer	

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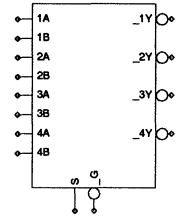
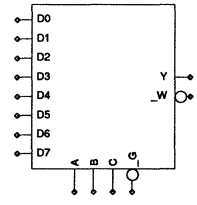
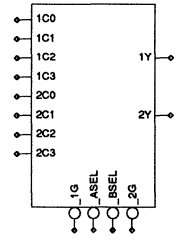
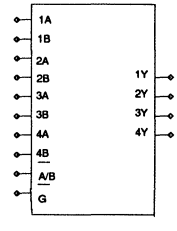
Name	Size	Description	Symbol
74LS158	18	Quadruple 2 to 1 line Multiplexer w/Inverted Outputs	
74LS251	26	1 of 8 Multiplexer w/3-State Outputs	
74LS253	16	Dual 4 to 1 line Multiplexer w/3-State Outputs	
74LS257	18	Dual 4 to 1 line Multiplexer w/3-State Outputs	

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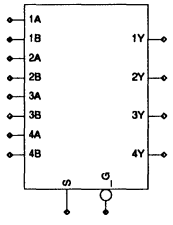
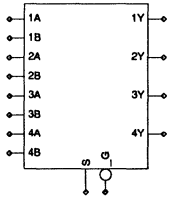
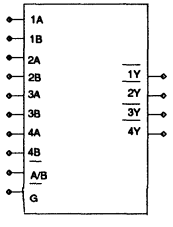
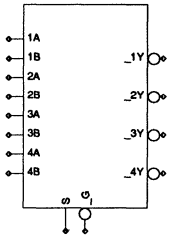
Name	Size	Description	Symbol
74LS257A	30	Quad 2 to 1 MUX	
74LS257B	18	Quad 2 to 1 MUX	
74LS258	22	Quadruple 2 to 1 line Multiplexer w/3-State inverted Outputs	
74LS258A	26	Quad 2 to 1 MUX	

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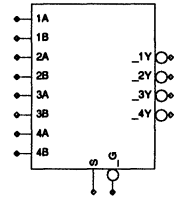
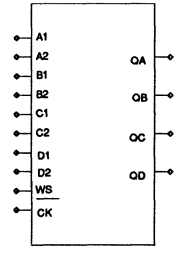
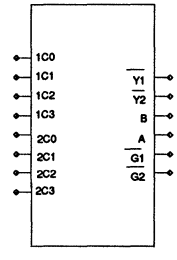
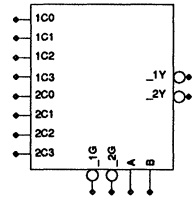
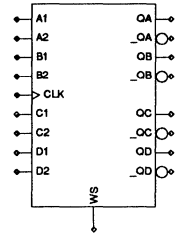
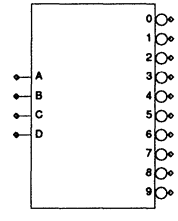
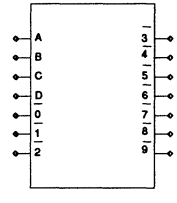
Name	Size	Description	Symbol
74LS258B	22	Quad 2 to 1 MUX	
74LS298	34	Quadruple 2 Input Multiplexer w/Storage	
74LS352	26	Dual 4 to 1 line Multiplexer w/Inverted Outputs	
74LS353	15	Dual 4 to 1 line Multiplexer w/3-State Inverted Outputs	

Name	Size	Description	Symbol
74LS398	42	Quad 2-input MUXs w/storage	

Decoders

Name	Size	Description	Symbol
74LS42	24	BCD to Decimal Decoder	

74LS43	24	Excess 3 to Decimal Decoder	

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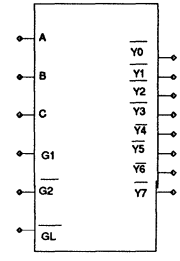
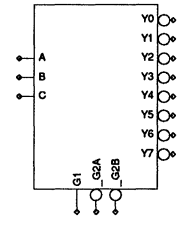
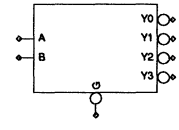
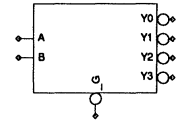
Name	Size	Description	Symbol
74LS137	37	3 to 8 line Decoder/Demultiplexer w/Address Latches	
74LS138	22	3 to 8 line Decoder/Demultiplexer	
74LS139	16	Dual 2 to 4 line Decoder/Demultiplexer	
74LS139A	8	2-line to 4-line Decoder/Demultiplexer	

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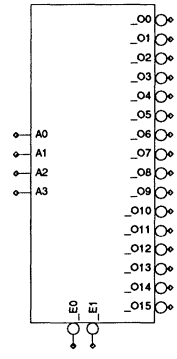
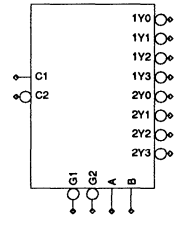
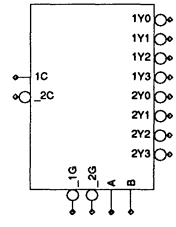
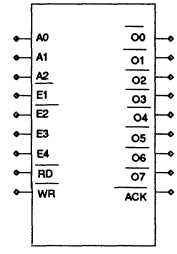
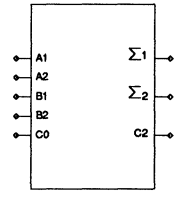
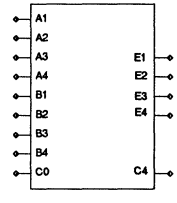
Name	Size	Description	Symbol
74LS154	48	4 to 16 line Decoder/Demultiplexer	
74LS155	21	Dual 2 to 4 line Decoder/Demultiplexer	
74LS155A	23	2-line to 4-line Decoder/Multiplexer	

Name	Size	Description	Symbol
74LS548	23	Octal Decoder and Demultiplexer	

Adders

Name	Size	Description	Symbol
74LS82	28	2 Bit Binary Full Adder	
74LS83	57	4 Bit Binary Full Adder w/Fast Carry	

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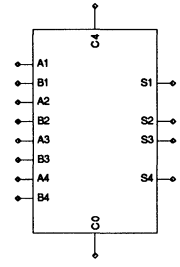
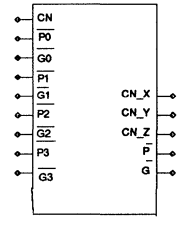
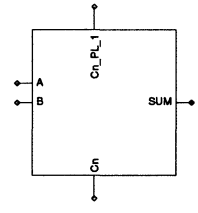
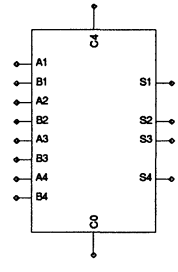
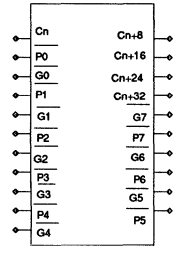
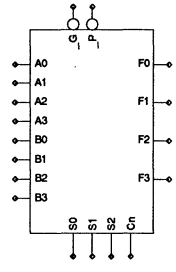
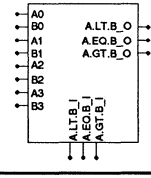
Name	Size	Description	Symbol
74LS83A	65	4 Bit Binary Full Adder w/Fast Carry	
74LS182	40	Look Ahead Carry Generator	
74LS183	26	Dual Carry-Save Full Adder	
74LS283	57	4 Bit Binary Full Adder w/Fast Carry	

Name	Size	Description	Symbol
74LS882	112	32 Bit Look Ahead Carry Generator	

ALU

Name	Size	Description	Symbol
74LS381	159	Arithmetic Logic Unit/Function Generator	

Comparators

Name	Size	Description	Symbol
74LS85	57	4 Bit Magnitude Comparator	

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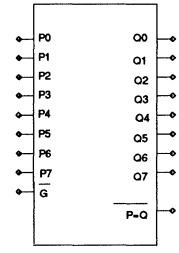
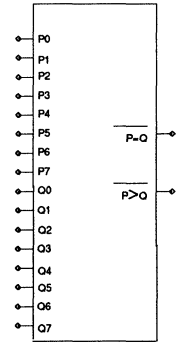
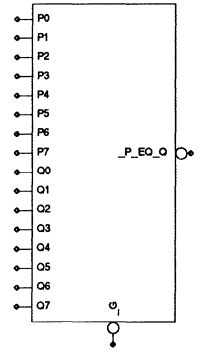
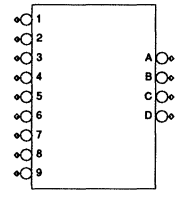
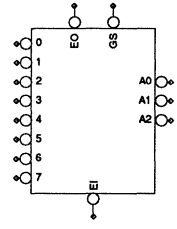
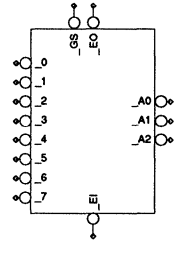
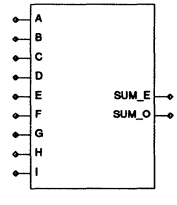
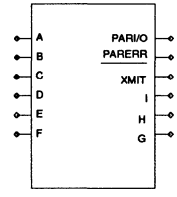
Name	Size	Description	Symbol
74LS521	30	8 Bit Identity Comparator	
74LS684	81	8 Bit Magnitude/Identity Comparator	
74LS688	96	8 Bit Magnitude/Identity Comparator	

Priority Encoders

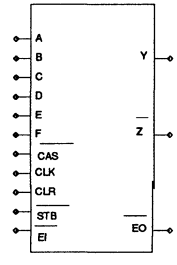
Name	Size	Description	Symbol
74LS147	39	10 to 4 line Priority Encoder	
74LS148	44	8 to 3 line Priority Encoder	
74LS348	50	8 to 3 line Priority Encoder w/3-State Outputs	

Parity Detectors

Name	Size	Description	Symbol
74LS280	26	9 Bit Odd/Even Parity Generator/Checker	

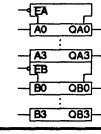
Name	Size	Description	Symbol
74LS286	31	9 Bit Parity Generator/Checker w/Bus Driver Parity I/O Port	

Clock Prescalers

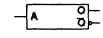
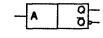
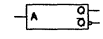
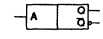
Name	Size	Description	Symbol
74LS97	117	Synchronous 6 Bit Binary Rate Multiplier	

SELECTION GUIDE FUNCTIONAL INDEX

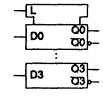
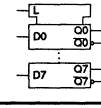
Internal Tri-State Drivers

Name	Size	Description	Symbol	Page
GSM244C	26	Dual 4 bit int TS buffer, w/ active low enables.		4-162

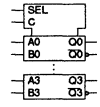
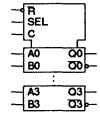
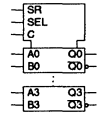
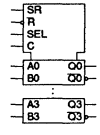
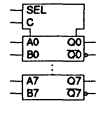
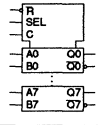
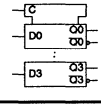
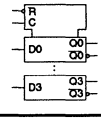
Two-Phase Clock Drivers

Name	Size	Description	Symbol	Page
GSCPG1	7	2 phase clock gen, w/ positive underlap.		4-108
GSCPG2	7	2 phase clock gen, w/ minimum underlap.		4-109
GSCPG3	9	2 phase clock gen, w/ positive underlap.		4-110
GSCPG4	9	2 phase clock gen, w/ minimum underlap.		4-111

Latches

Name	Size	Description	Symbol	Page
GSL4	13	4 bit data latch.		4-141
GSL8	25	8 bit data latch.		4-142

Registers

Name	Size	Description	Symbol	Page
GSMR41	29	4 bit reg, w/ 2 bit MUX inputs.		4-166
GSMR42	33	4 bit reg, w/ 2 bit MUX inputs and reset not.		4-167
GSMR43	31	4 bit reg, w/ 2 bit MUX inputs and sync reset.		4-168
GSMR44	35	4 bit reg, w/ 2 bit MUX inputs, sync reset and async reset not.		4-169
GSMR81	57	8 bit reg, w/ 2 bit MUX inputs.		4-170
GSMR82	65	8 bit reg, w/ 2 bit MUX inputs and reset not.		4-171
GSR41	20	4 bit data register.		4-207
GSR42	24	4 bit data reg, w/ reset not.		4-208

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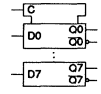
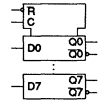
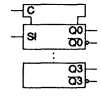
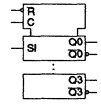
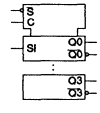
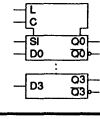
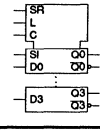
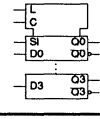
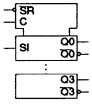
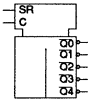
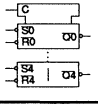
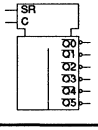
Name	Size	Description	Symbol	Page
GSR81	40	8 bit data register.		4-209
GSR82	48	8 bit data reg, w/ reset not.		4-210
GSSR41	20	4 bit shift register.		4-211
GSSR42	24	4 bit shift reg, w/ reset not.		4-212
GSSR43	24	4 bit shift reg, w/ set not.		4-213
GSSR44	30	4 bit shift reg, sync parallel load.		4-214
GSSR45	31	4 bit shift reg, sync parallel load and reset.		4-215
GSSR46	40	4 bit shift reg, async parallel load.		4-216

Name	Size	Description	Symbol	Page
GSSR47	24	4 bit shift reg, w/ sync reset not.		4-217
GSSR84	60	8 bit shift reg, w/ 2 bit MUX inputs, sync parallel load.		4-218

Binary Counters

Name	Size	Description	Symbol	Page
GSCB4C	43	Fast 4 bit bin up cntr, w/ sync reset.		4-26
GSCB4F	47	Fast 4 bit bin up cntr w/ individual set nots and reset nots.		4-27
GSCB5C	57	Fast 5 bit bin up cntr, w/ sync reset.		4-28
GSCB5F	63	Fast 5 bit bin up cntr, w/ individual set nots and reset nots.		4-29
GSCB6C	70	Fast 6 bit bin up cntr, w/ sync reset.		4-30

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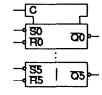
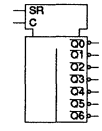
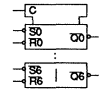
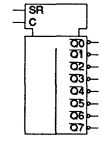
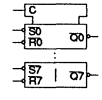
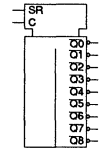
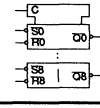
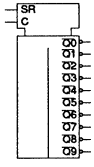
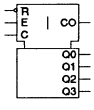
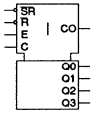
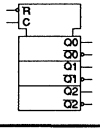
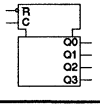
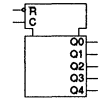
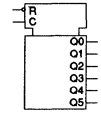
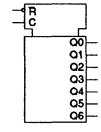
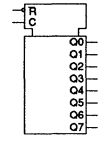
Name	Size	Description	Symbol	Page
GSCB6F	77	Fast 6 bit bin up cntr, w/ individual set nots and reset nots.		4-31
GSCB7C	85	Fast 7 bit bin up cntr, w/ sync reset.		4-32
GSCB7F	93	Fast 7 bit bin up cntr, w/ individual set nots and reset nots.		4-33
GSCB8C	100	Fast 8 bit bin up cntr, w/ sync reset.		4-34
GSCB8F	109	Fast 8 bit bin up cntr, w/ individual set nots and reset nots.		4-35
GSCB9C	115	Fast 9 bit bin up cntr, w/ sync reset.		4-36
GSCB9F	125	Fast 9 bit bin up cntr, w/ individual set nots and reset nots.		4-37

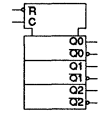
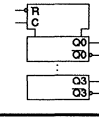
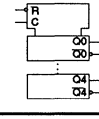
Name	Size	Description	Symbol	Page
GSCB10C	130	Fast 10 bit bin up cntr, w/ sync reset.		4-39
GSCB10F	141	Fast 10 bit bin up cntr, w/ individual set nots and reset nots.		4-40
GSCB41	50	Expandable 4 bit bin up cntr w/ reset not.		4-42
GSCB42	54	Expandable 4 bit bin up cntr w/ sync and async reset nots.		4-43

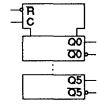
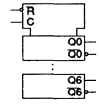
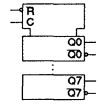
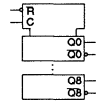
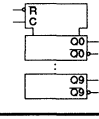
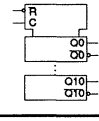
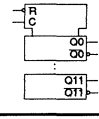
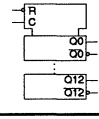
Gray Counters

Name	Size	Description	Symbol	Page
GSC2G	12	Mod 4 gray cntr, w/ reset not.		4-1
GSC3G	25	Mod 8 gray cntr, w/ reset not.		4-2
GSC4G	50	Mod 16 gray cntr, w/ reset not.		4-3

Name	Size	Description	Symbol	Page
GSC5G	63	Mod 32 gray cntr, w/ reset not.		4-4
GSC6G	76	Mod 64 gray cntr, w/ reset not.		4-5
GSC7G	90	Mod 128 gray cntr, w/ reset not.		4-6
GSC8G	104	Mod 256 gray cntr, w/ reset not.		4-7

Polynomial Counters

Name	Size	Description	Symbol	Page
GSC3LSR	22	3 bit mod 7 linear feedback shift reg, w/ reset not.		4-8
GSC4LSR	28	4 bit mod 15 linear feedback shift reg, w/ reset not.		4-9
GSC5LSR	33	5 bit mod 31 linear feedback shift reg, w/ reset not.		4-10

Name	Size	Description	Symbol	Page
GSC6LSR	40	6 bit mod 63 linear feedback shift reg, w/ reset not.		4-11
GSC7LSR	46	7 bit mod 127 poly cntr, w/ reset not.		4-12
GSC8LSR	58	8 bit mod 255 poly cntr, w/ reset not.		4-13
GSC9LSR	57	9 bit mod 511 poly cntr, w/ reset not.		4-14
GSC10LSR	63	10 bit mod 1023 poly cntr, w/ reset not.		4-15
GSC11LSR	69	11 bit mod 2047 poly cntr, w/ reset not.		4-16
GSC12LSR	81	12 bit mod 4095 poly cntr, w/ reset not.		4-17
GSC13LSR	87	13 bit mod 8191 poly cntr, w/ reset not.		4-18

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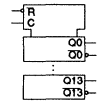
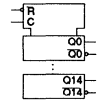
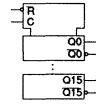
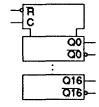
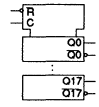
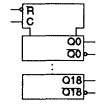
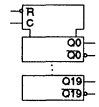
Name	Size	Description	Symbol	Page
GSC14LSR	93	14 bit mod 16383 poly cntr, w/ reset not.		4-19
GSC15LSR	93	15 bit mod 32767 poly cntr, w/ reset not.		4-20
GSC16LSR	105	16 bit mod 65535 poly cntr, w/ reset not.		4-21
GSC17LSR	105	17 bit mod 131071 poly cntr, w/ reset not.		4-22
GSC18LSR	111	18 bit mod 262143 poly cntr, w/ reset not.		4-23
GSC19LSR	123	19 bit mod 524287 poly cntr, w/ reset not.		4-24
GSC20LSR	123	20 bit mod 1040575 poly cntr, w/ reset not.		4-25

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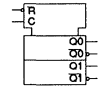
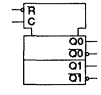
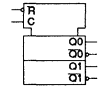
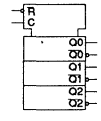
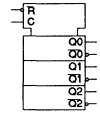
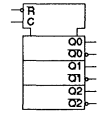
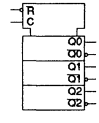
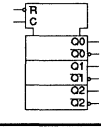
Name	Size	Description	Symbol	Page
GSCM3B	13	Mod 3 binary cntr, w/ reset not.		4-48
GSCM4B	16	Mod 4 binary cntr, w/ reset not.		4-49
GSCM4J	12	Mod 4 Johnson cntr, w/ reset not.		4-50
GSCM5B	27	Mod 5 binary cntr, w/ reset not.		4-51
GSCM5SR	19	Mod 5 shift cntr, w/ reset not.		4-52
GSCM6B	29	Mod 6 binary cntr, w/ reset not.		4-53
GSCM6J	18	Mod 6 Johnson cntr, w/ reset not.		4-54
GSCM7B	32	Mod 7 binary cntr, w/ reset not.		4-55

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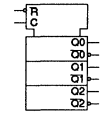
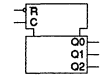
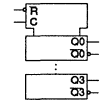
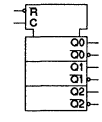
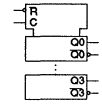
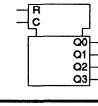
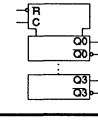
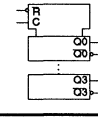
GSCM8B	27	Mod 8 binary cntr, w/ reset not.		4-56
GSCM8BR	18	Mod 8 binary ripple cntr, w/ reset not.		4-57
GSCM8J	24	Mod 8 Johnson cntr, w/ reset not.		4-58
GSCM8SR	22	Mod 8 shift cntr, w/ reset not.		4-59
GSCM9B	39	Mod 9 binary cntr, w/ reset not.		4-60
GSCM9BR	29	Mod 9 binary ripple cntr, w/ reset.		4-61
GSCM9SR	28	Mod 9 shift cntr, w/ reset not.		4-62
GSCM10B	40	Mod 10 binary cntr, w/ reset not.		4-63

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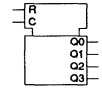
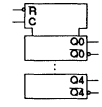
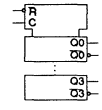
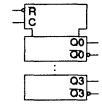
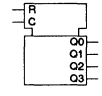
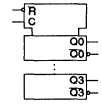
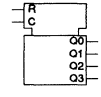
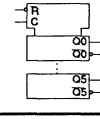
GSCM10BR	30	Mod 10 binary ripple cntr, w/ reset.		4-64
GSCM10J	30	Mod 10 Johnson cntr, w/ reset not.		4-65
GSCM10SR	32	Mod 10 shift cntr, w/ reset not.		4-66
GSCM11B	43	Mod 11 binary cntr, w/ reset not.		4-67
GSCM11BR	30	Mod 11 binary ripple cntr, w/ reset.		4-68
GSCM12B	41	Mod 12 binary cntr, w/ reset not.		4-69
GSCM12BR	31	Mod 12 binary ripple cntr, w/ reset.		4-70
GSCM12J	36	Mod 12 Johnson cntr, w/ reset not.		4-71

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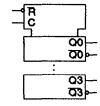
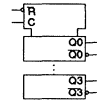
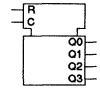
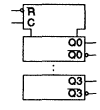
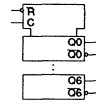
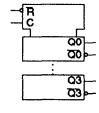
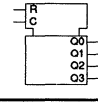
GSCM12SR	31	Mod 12 shift cntr, w/ reset not.		4-72
GSCM13B	44	Mod 13 binary cntr, w/ reset not.		4-73
GSCM13BR	30	Mod 13 binary ripple cntr, w/ reset.		4-74
GSCM14B	44	Mod 14 binary cntr, w/ reset not.		4-75
GSCM14BR	31	Mod 14 binary ripple cntr, w/ reset.		4-76
GSCM14J	42	Mod 14 Johnson cntr, w/ reset not.		4-77
GSCM15B	46	Mod 15 binary cntr, w/ reset not.		4-78
GSCM15BR	31	Mod 15 binary ripple cntr, w/ reset.		4-79

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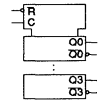
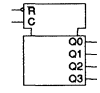
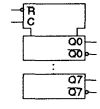
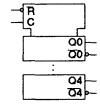
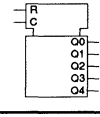
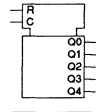
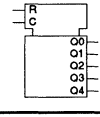
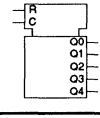
Name	Size	Description	Symbol	Page
GSCM16B	39	Mod 16 binary cntr, w/ reset not.		4-80
GSCM16BR	24	Mod 16 binary ripple cntr, w/ reset not.		4-81
GSCM16J	48	Mod 16 Johnson cntr, w/ reset not.		4-82
GSCM17B	53	Mod 17 binary cntr, w/ reset not.		4-83
GSCM17BR	35	Mod 17 binary ripple cntr, w/ reset.		4-84
GSCM18BR	36	Mod 18 binary ripple cntr, w/ reset.		4-85
GSCM19BR	36	Mod 19 binary ripple cntr, w/ reset.		4-86
GSCM20BR	37	Mod 20 binary ripple cntr, w/ reset.		4-87

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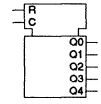
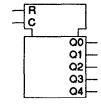
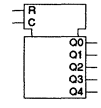
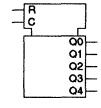
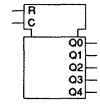
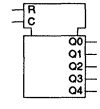
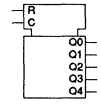
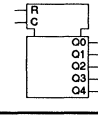
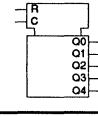
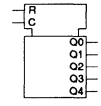
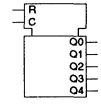
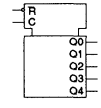
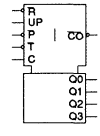
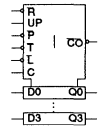
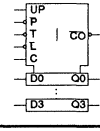
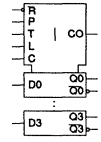
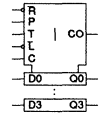
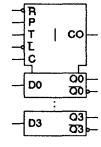
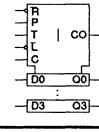
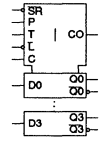
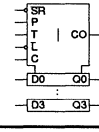
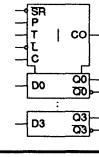
Name	Size	Description	Symbol	Page
GSCM21BR	36	Mod 21 binary ripple cntr, w/ reset.		4-88
GSCM22BR	37	Mod 22 binary ripple cntr, w/ reset.		4-89
GSCM23BR	37	Mod 23 binary ripple cntr, w/ reset.		4-90
GSCM24BR	37	Mod 24 binary ripple cntr, w/ reset.		4-91
GSCM25BR	36	Mod 25 binary ripple cntr, w/ reset.		4-92
GSCM26BR	37	Mod 26 binary ripple cntr, w/ reset.		4-93
GSCM27BR	37	Mod 27 binary ripple cntr, w/ reset.		4-94
GSCM28BR	37	Mod 28 binary ripple cntr, w/ reset.		4-96
GSCM29BR	37	Mod 29 binary ripple cntr, w/ reset.		4-98

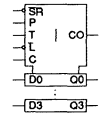
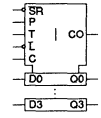
Name	Size	Description	Symbol	Page
GSCM30BR	37	Mod 30 binary ripple cntr, w/ reset.		4-100
GSCM31BR	37	Mod 31 binary ripple cntr, w/ reset.		4-102
GSCM32BR	30	Mod 32 binary ripple cntr, w/ reset not.		4-104

Up/Down Counters

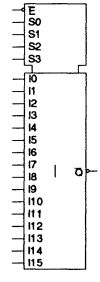
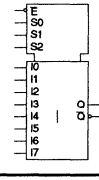
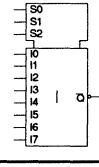
Name	Size	Description	Symbol	Page
GSCUD41	61	4 bit up/down counter, w/ reset not.		4-112
GSCUD42	79	4 bit up/down cntr, w/ reset not.		4-114
GSM169C	66	4 bit binary up/down counter.		4-161

Miscellaneous Counters

Name	Size	Description	Symbol	Page
GSM160C	58	Sync 4 bit BCD counter, w/ reset not.		4-152
GSM160D	66	Sync 4 bit BCD counter, w/ reset not.		4-153
GSM161C	55	Sync 4 bit binary counter, w/ reset not.		4-154
GSM161D	61	Sync 4 bit binary counter, w/ reset not.		4-155
GSM162C	56	Sync 4 bit BCD counter, w/ sync reset not.		4-156
GSM162D	62	Sync 4 bit BCD counter, w/ sync reset not.		4-157
GSM163C	55	Sync 4 bit binary counter, w/ sync reset not.		4-158

Name	Size	Description	Symbol	Page
GSM163D	62	Sync 4 bit binary counter, w/ sync reset not.		4-159
GSM163F	91	Sync 4 bit binary counter, w/ sync reset not.		4-160

Multiplexers

Name	Size	Description	Symbol	Page
GSM150C	36	16 input gated inverting MUX, w/ active low enable.		4-146
GSM151C	19	8 input gated MUX, with active low enable.		4-147
GSM152C	17	8 input inverting MUX.		4-148

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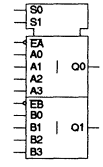
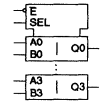
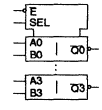
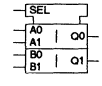
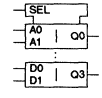
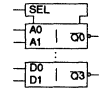
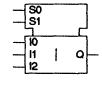
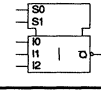
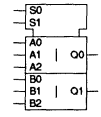
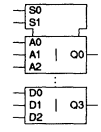
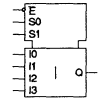
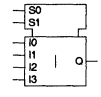
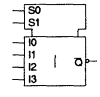
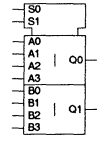
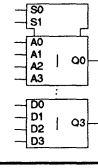
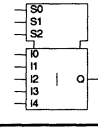
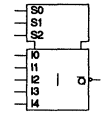
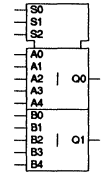
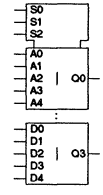
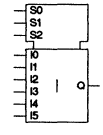
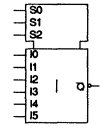
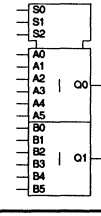
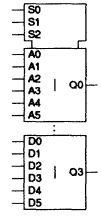
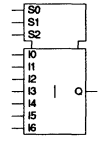
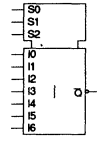
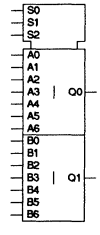
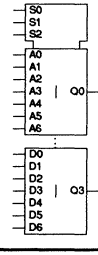
Name	Size	Description	Symbol	Page
GSM153C	18	Dual 4 input MUX, w/ active low enables.		4-149
GSM157C	13	Quad 2 input gated MUX, w/ active low enable.		4-150
GSM158C	11	Quad 2 input inverting gated MUX, w/ active low enable.		4-151
GSMX22H	6	Dual 2 bit non-inverting MUX.		4-172
GSMX24H	12	Quad 2 bit non-inverting MUX.		4-173
GSMX24L	8	Quad 2 bit inverting MUX.		4-174
GSMX31H	7	3 bit non-inverting MUX.		4-175
GSMX31L	6	3 bit inverting MUX.		4-176

Name	Size	Description	Symbol	Page
GSMX32H	12	Dual 3 bit non-inverting MUX.		4-177
GSMX34H	22	Quad 3 bit non-inverting MUX.		4-178
GSMX41GH	9	4 bit non-inverting gated MUX, w/ active low enable.		4-179
GSMX41H	8	4 bit non-inverting MUX.		4-180
GSMX41L	8	4 bit inverting MUX.		4-181
GSMX42H	14	Dual 4 bit non-inverting MUX.		4-182
GSMX44H	26	Quad 4 bit non-inverting MUX.		4-183
GSMX51H	12	5 bit non-inverting MUX.		4-184

Name	Size	Description	Symbol	Page
GSMX51L	11	5 bit inverting MUX.		4-185
GSMX52H	21	Dual 5 bit non-inverting MUX.		4-186
GSMX54H	39	Quad 5 bit non-inverting MUX.		4-187
GSMX61H	13	6 bit non-inverting MUX.		4-189
GSMX61L	14	6 bit inverting MUX.		4-190
GSMX62H	24	Dual 6 bit non-inverting MUX.		4-191

Name	Size	Description	Symbol	Page
GSMX64H	46	Quad 6 bit non-inverting MUX.		4-192
GSMX71H	17	7 bit non-inverting MUX.		4-194
GSMX71L	16	7 bit inverting MUX.		4-195
GSMX72H	31	Dual 7 bit non-inverting MUX.		4-196
GSMX74H	59	Quad 7 bit non-inverting MUX.		4-197

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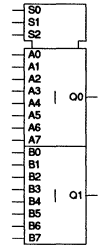
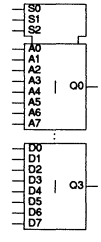
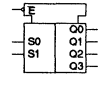
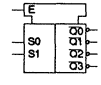
Name	Size	Description	Symbol	Page
GSMX82H	40	Dual 8 bit non-inverting MUX.		4-199
GSMX84H	75	Quad 8 bit non-inverting MUX.		4-200

Decoders

Name	Size	Description	Symbol	Page
GSD24GH	10	2 to 4 decoder, active high gated outputs.		4-116
GSD24GL	9	2 to 4 decoder, active low gated outputs.		4-117
GSD24H	6	2 to 4 decoder, active high outputs.		4-118
GSD24L	6	2 to 4 decoder, active low outputs.		4-119

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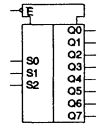
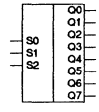
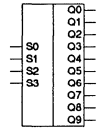
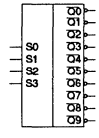
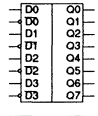
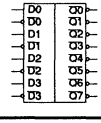
Name	Size	Description	Symbol	Page
GSD38GH	19	3 to 8 decoder, active high gated outputs.		4-120
GSD38H	19	3 to 8 decoder, active high outputs.		4-121
GSD410H	24	4 to 10 decoder, active high outputs.		4-122
GSD410L	24	4 to 10 decoder, active low outputs.		4-123
GSDM6JH	6	Active high mod 6 Johnson counter decoder.		4-124
GSDM6JL	6	Active low mod 6 Johnson counter decoder.		4-125
GSDM8JH	8	Active high mod 8 Johnson counter decoder.		4-126
GSDM8JL	8	Active low mod 8 Johnson counter decoder.		4-127

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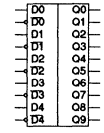
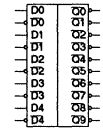
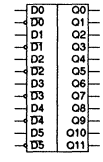
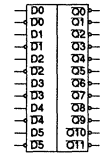
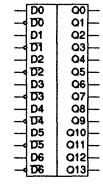
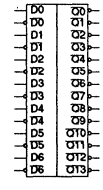
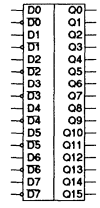
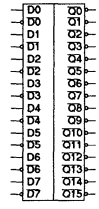
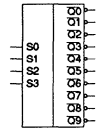
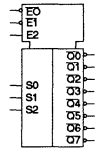
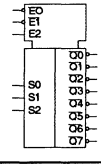
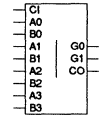
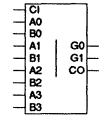
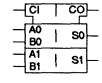
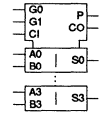
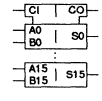
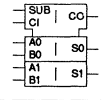
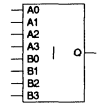
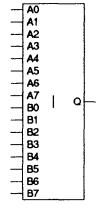
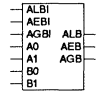
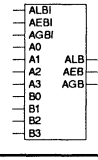
Name	Size	Description	Symbol	Page
GSDM10JH	10	Active high mod 10 Johnson counter decoder.		4-128
GSDM10JL	10	Active low mod 10 Johnson counter decoder.		4-129
GSDM12JH	12	Active high mod 12 Johnson counter decoder.		4-130
GSDM12JL	12	Active low mod 12 Johnson counter decoder.		4-131
GSDM14JH	14	Active high mod 14 Johnson counter decoder.		4-132
GSDM14JL	14	Active low mod 14 Johnson counter decoder.		4-133

Name	Size	Description	Symbol	Page
GSDM16JH	16	Active high mod 16 Johnson counter decoder.		4-134
GSDM16JL	16	Active low mod 16 Johnson counter decoder.		4-135
GSM42C	24	4 to 10 decoder.		4-143
GSM138C	21	Gated 3 to 8 line decoder.		4-144
GSM138D	22	Gated 3 to 8 active low decoder.		4-145

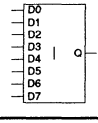
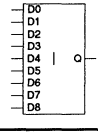
Adders

Name	Size	Description	Symbol	Page
GSCLA1	18	Carry look ahead for a 4 bit adder [LSN].		4-44
GSCLA2	20	Carry look ahead for a 4 bit adder.		4-46
GSFA2	14	2 bit full adder.		4-136
GSFA4	42	4 bit binary full adder.		4-137
GSFA16	233	16 bit full adder.		4-138
GSFAS2	30	2 bit twoscompfulladd/sub.'		4-139
GSHA1	5	Half adder.		4-140

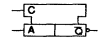
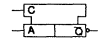
Comparators

Name	Size	Description	Symbol	Page
GSCMP4	14	4 bit equality comparator.		4-106
GSCMP8	29	8 bit equality comparator.		4-107
GSMAG2	22	2 bit extendable binary magnitude comparator.		4-163
GSMAG2H	17	2 bit binary magnitude comparator.		4-164
GSMAG4	44	4 bit expandable binary magnitude comparator.		4-165

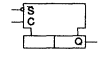
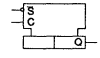
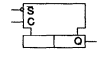
Parity Detectors

Name	Size	Description	Symbol	Page
GSPAR8	21	8 bit odd parity detector.		4-202
GSPAR9	24	9 bit odd parity detector.		4-203

Synchronizers

Name	Size	Description	Symbol	Page
GSSYNC01	11	Synchronizer for asynchronous 0 to 1 event.		4-219
GSSYNC10	11	Synchronizer for asynchronous 1 to 0 event.		4-220

Clock Prescalers

Name	Size	Description	Symbol	Page
GSPS2	13	Divide by 2 external clock prescaler.		4-204
GSPS3	19	Divide by 3 external clock prescaler.		4-205
GSPS4	25	Divide by 4 external clock prescaler.		4-206

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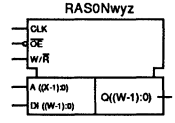
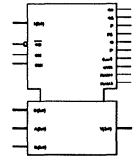
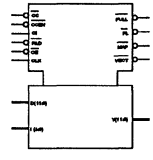
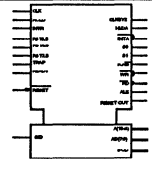
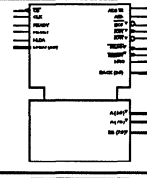
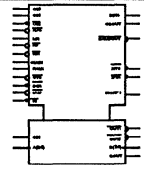
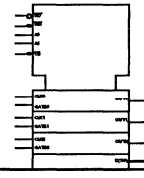
DIGITAL MEGACELL FUNCTIONAL INDEX

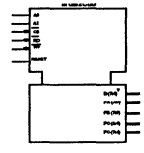
Searams

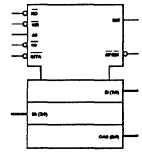
Name	Description	Symbol	Page
RAS0Nwyz	MxN synchronous static RAM compiler with active low (OEN) 3-state outputs		5-1

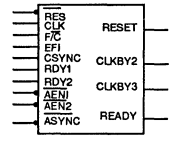
Softcells

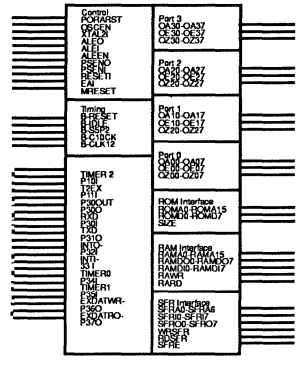
Name	Description	Symbol	Page
MG29C01	4-bit Microprocessor		5-11
MG29C10	Microprogram Controller/Sequencer		5-13
MG80C85	8-bit CMOS Microprocessor		5-15
MG82C37A	Programmable DMA Controller		5-17
MG82C50A	Asynchronous Communications Element		5-19



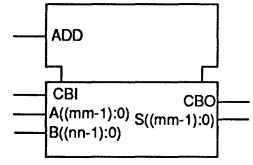
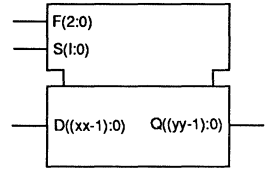
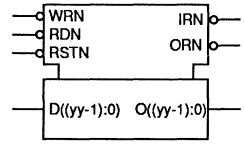
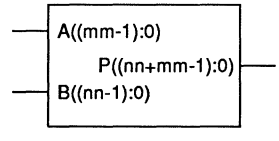








Synthesized Cells

Name	Description	Symbol	
MGAmmnnAv	Synthesizer builds mm bit by nn bit adder/subtracters which employ the look-ahead carry technique		5-31
MGBxxyyAv	Synthesizer builds barrel shifters which provide various shift functions for an input word size of xx bits		5-33
MGFxxyyAv	Synthesizer builds latch based FIFO's of xx words by yy bit sizes		5-35
MGMmmnnBv	Synthesizer builds 2's compliment multipliers of mm bit by nn bit sizes		5-37

SECTION 1

INTRODUCTION

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1.0 INTRODUCTION

1.1 This data book contains electrical and delay characteristics of the American Microsystems, Inc. (AMI) 1.0μm Gate Array library (GDx). This library is designed in AMI's 1.0μm (CYx) CMOS process with the following features: single poly, 2 or 3 metal levels, twin tub, and p- starting material. The library cells are characterized for 5V +/- 10% applications but will operate between 2.5V and 5.5V.

1.2 LIBRARY FEATURES

1.2.1 The library implements all the functions in JEDEC Standard No. 12-3. Several additional functions supplement this standard. AMI refers to this implementation as the ASIC Standard Library. The ASIC Standard Library is the core offering for both Standard Cells and Gate Array (future Standard Cell and Gate Array libraries will contain this function set).

1.2.2 Gate Array libraries are now functionally compatible with Standard Cell libraries because of the ASIC Standard approach. Both libraries use the same transistor level schematics (except for transistor sizes). Standard cells take advantage of the ability to vary transistor widths to optimize the switch point of the gates. The Gate Array cells have comparable delays with the Standard cells so that designs can be migrated from one library to the other with minimum effort.

1.2.3 This Gate Array library was developed using AMI's internal design system called Accolade. This system is a complete cell design system featuring symbolic graph compaction, mask data extraction, characterization, logic model data creation, and datasheet creation. Accolade makes the libraries process independent which facilitates faster cell migration to new process technologies.

1.2.4 Soft macro support exists for over 200, 7400 series TTL functions and over 200 MSI functions which can be used in conjunction with the ASIC Standard library. Megacells are available such as core processors, RAMs, DPRAMs, ROMS, FIFOs, and DSP type cells. Megacell offerings vary between the GDx and Standard Cell libraries (SDx). You should consult the appropriate databook before finalizing your logic design.

1.3 FORMAT OF THE DATA BOOK

1.3.1 This introduction is preceded by an alphanumeric index and selection guides for the ASIC Standard functions, the MSI functions and the Digital Megacell Functions. Following this introduction, Section 2 of the data book contains library electrical characteristics, derating factors, datasheet usage, base, and packaging information. Section 3 contains datasheets for the ASIC Standard functions. Section 4 contains datasheets for the MSI functions. Section 5 contains the datasheets for the Digital Megacell functions. Finally Section 6 contains Terms of Sales and Sales Offices Information.

SECTION 2

LIBRARY CHARACTERISTICS

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2.0 LIBRARY CHARACTERISTICS

2.1 DC OPERATING CHARACTERISTICS

2.1.1 Table 1 contains the absolute maximum ratings for 1.0 micron ASIC library chips. Table 2 and Table 3 contain the input and output operating specifications respectively for the library. Note that Table 2 contains data with a Supply Voltage range of 4.5v to 5.5v. The Library has been characterized with a Supply Voltage range of 2.5v to 5.5v. Please contact factory for further details.

Table 1 : Absolute Maximum Ratings

Parameter		Range	Units
VDD, Supply Voltage		-0.3 to 7.0	Volts
Input Pin Voltage		-0.3 to VDD+0.3	Volts
Input Pin Current		-10.0 to 10.0	mA
Storage Temperature	- Plastic Packages	-55 to 125	°C
	- Ceramic Packages	-65 to 150	°C
Lead Temperature		300	°C for 10 sec.

Note that these specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect the long term reliability of the device.

Table 2 : Operating Specifications Contact factory for 2.5 operating specifications.

Parameter		Minimum	Maximum	Units
VDD, Supply Voltage		4.5	5.5	Volts
Ambient Temperature	- Military	-55	125	°C
	- Commercial	0	70	°C
CMOS Input Specifications				
Vil	Low Level Input Voltage		0.3*VDD	Volts
Vih	High Level Input Voltage	0.7*VDD		Volts
Iil	Low Level Input Current		-1.0	µA
Iih	High Level Input Current		1.0	µA
Iil	Input Pull-Up Current	-30	-580	µA
Iih	Input Pull-Down Current	30	580	µA
Vt-	Schmitt Negative Threshold	0.2*VDD		Volts
Vt+	Schmitt Positive Threshold		0.8*VDD	Volts
Vh	Schmitt Hysteresis	1.0		Volts
TTL Input Specifications				
Vil	Low Level Input Voltage		0.8	Volts
Vih	High Level Input Voltage	2.0		Volts
Iil	Low Level Input Current		-1.0	µA
Iih	High Level Input Current		1.0	µA
Iil	Input Pull-Up Current	-30	-580	µA
Iih	Input Pull-Down Current	30	580	µA
Vt-	Schmitt Negative Threshold	0.8		Volts
Vt+	Schmitt Positive Threshold		2.3	Volts
Vh	Schmitt Hysteresis	0.4		Volts

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Table 3 : Output Operating Specifications

Parameter		Minimum	Maximum	Units
1.0 mA Driver				
Vol	Low Level Output Voltage		0.4	Volts
Voh	High Level Output Voltage	2.4		Volts
Iol	Low Level Output Current		1.0	mA
Ioh	High Level Output Current		-1.0	mA
2.0 mA Driver				
Vol	Low Level Output Voltage		0.4	Volts
Voh	High Level Output Voltage	2.4		Volts
Iol	Low Level Output Current		2.0	mA
Ioh	High Level Output Current		-2.0	mA
4.0 mA Driver				
Vol	Low Level Output Voltage		0.4	Volts
Voh	High Level Output Voltage	2.4		Volts
Iol	Low Level Output Current		4.0	mA
Ioh	High Level Output Current		-4.0	mA
8.0 mA Driver				
Vol	Low Level Output Voltage		0.4	Volts
Voh	High Level Output Voltage	2.4		Volts
Iol	Low Level Output Current		8.0	mA
Ioh	High Level Output Current		-8.0	mA

2.1.2 Figures 1 and 2 show typical current voltage curves for the pad driver transistors from 1 mA to 8 mA. References to typical means the data was characterized for Tj = 25 degrees C, vdd = 5 volts, and typical (nominal) process. Figures 3 and 4 show the typical current voltage curves for input pads with pull-up and pull-down devices.

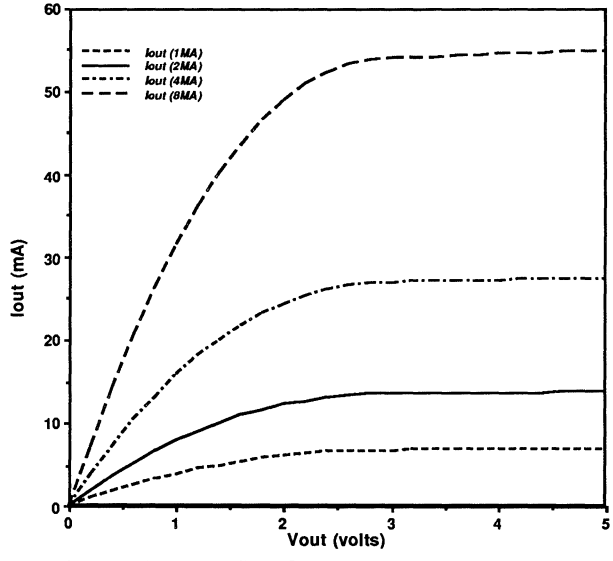

Figure 1: Typical TTL and CMOS N-Channel Driver DC Characteristics

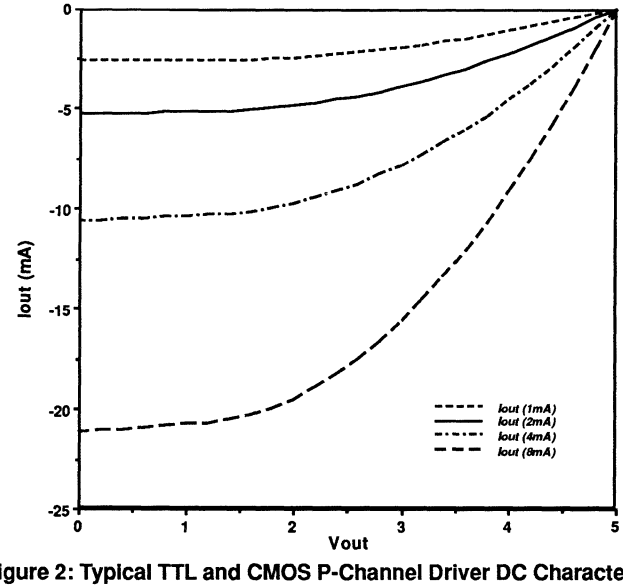

Figure 2: Typical TTL and CMOS P-Channel Driver DC Characteristics

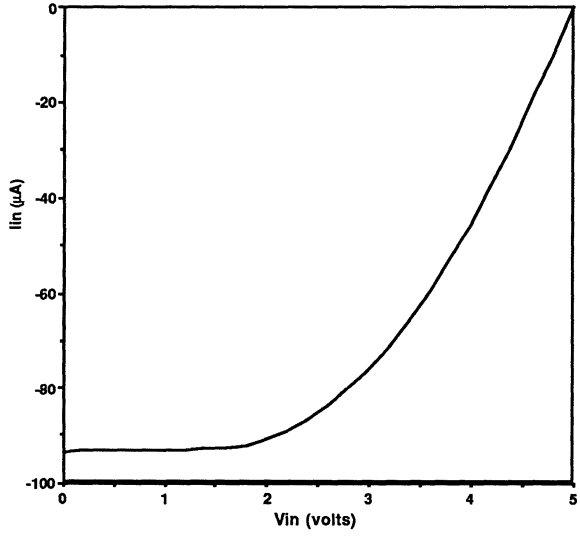

Figure 3: Typical Input Pull-up DC Characteristics

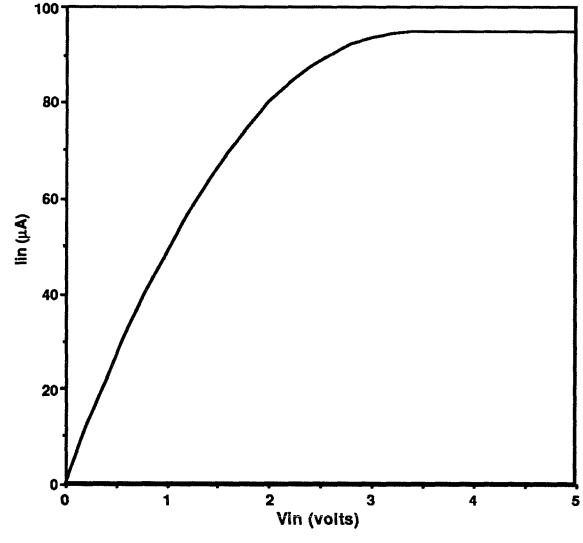

Figure 4: Typical Input Pull-down Characteristics

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2.1.3 Figure 8 and Tables 4 and 5 show derating factors for the current due to temperature voltage and process. Values are normalized to typical conditions. To obtain a current value at conditions other than typical, multiply the derating factors corresponding to those conditions to the current values from the curves in figures 1 through 4, i.e. $K_{TDC}*K_{VDC}*K_{PDC}*I_{DC}$.

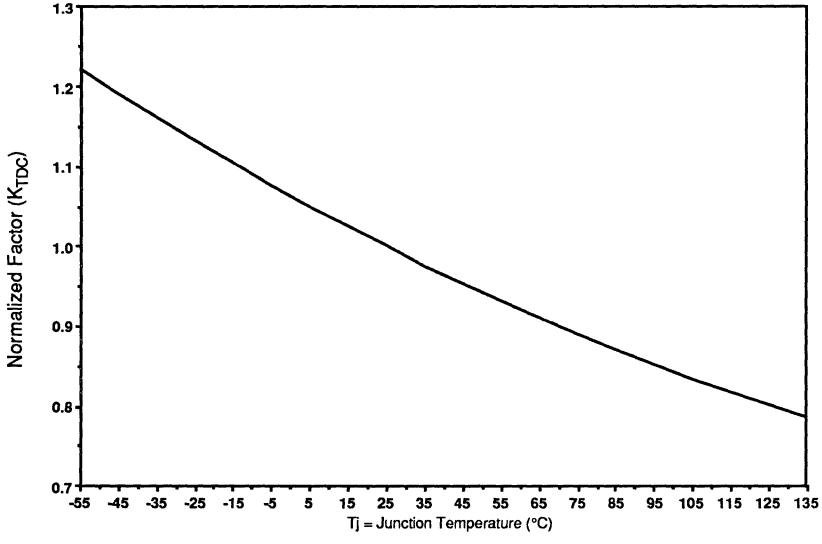

Figure 5: Temperature Derating Factors for DC Characteristics

Table 4 : Voltage Derating Factors for DC Characteristics

	N-channel (Vol = 0.4v)			P-channel (Voh = 2.4v)		
V_{DD}	4.5v	5.0v	5.5v	4.5v	5.0v	5.5v
K_{VDC}	0.93	1.00	1.05	0.79	1.00	1.22

Table 5 : Process Derating Factors for DC Characteristics

	N-channel (Vol = 0.4v)			P-channel (Voh = 2.4v)		
	WCS	TYP	BCS	WCS	TYP	BCS
K_{PDC}	0.76	1.00	1.39	0.70	1.00	1.49

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2.2 DELAY OPERATING CHARACTERISTICS

2.2.1 Delay values for CMOS cells are measured between the input and output 50% voltage supply (Vdd) crossing points. TTL input buffers are measured from the input's 1.4 volt crossing point to the output's 50% Vdd crossing point. TTL output buffers are measured from the input's 50% Vdd crossing point to the output's 1.4 volt crossing point. All delays are characterized at typical conditions (Tj = 25 degrees C, Vdd = 5 volts, and typical process).

2.2.2 Figures 6, 7, and Table 6 contain derating factors for various temperatures, voltages, and process variation respectively. To obtain a delay value at conditions other than typical, multiply the derating factors corresponding to those conditions to the current values from the delays in the datasheets, i.e. $K_T*K_V*K_P*T_D$, where T_D can be a delay from the delay characteristics table mentioned in 2.3.12 or a value calculated from the propagation delay equations as mentioned in 2.3.13:

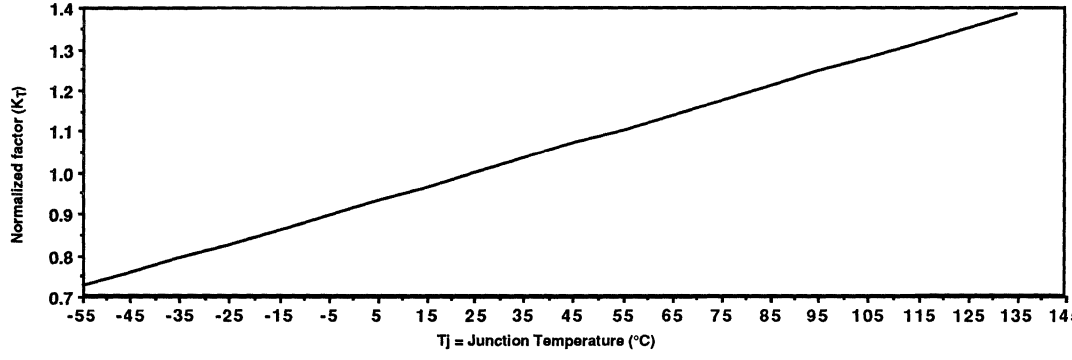

Figure 6: Temperature Derating Factors for AC Characteristics

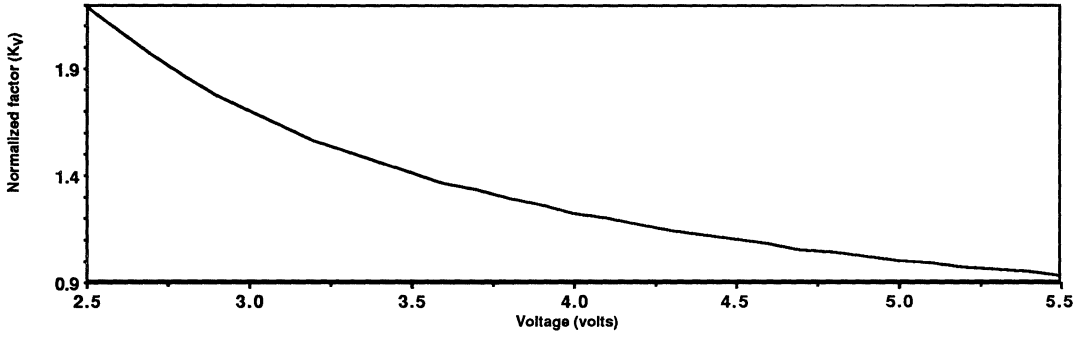

Figure 7: Process Derating Factors for AC Characteristics

Table 6 : Process Derating Factors for AC Characteristics

	Worst Case	Typical Case	Best Case
K_P	1.40	1.00	0.65

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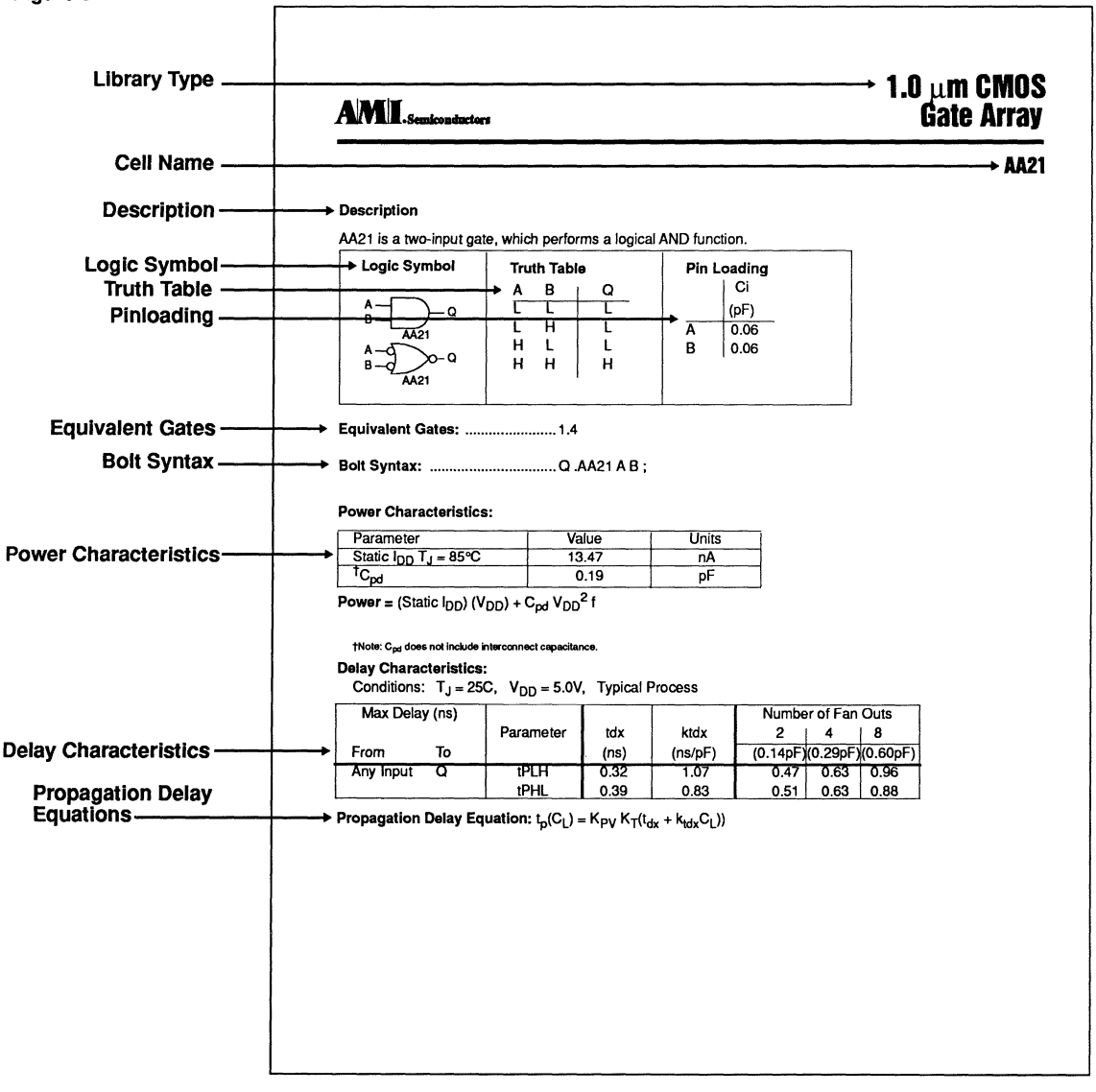
2.3 INTERPRETING THE DATASHEET

2.3.1 Figure 8 shows a typical datasheet and points out the main features of the datasheet. Not shown is a schematic which accompanies some of the more complex cells.

Figure 8



Design Information

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A description of these features of the datasheet are as follows:

2.3.2 LIBRARY TYPE: designates the feature size and library type such as Standard Cell or Gate Array.

2.3.3 CELL NAME: AMI's cell name.

2.3.4 DESCRIPTION: A brief sentence about the function of the cell.

2.3.5 LOGIC SYMBOL: Shows a picture of the symbol as it appears as an icon in the workstation design kits.

2.3.6 TRUTH TABLE: A boolean table showing the output logic levels as a function of the input logic levels. Types of logic levels found in the logic tables are as follows:

H	=	High level steady state
L	=	Low level steady state
↑	=	Transition from Low level to High level
↓	=	Transition from High level to Low level
X	=	Any level including transitions
NC	=	No Change in output level for a given set of input levels
IL	=	The output level is unknown for this set of illegal input levels
Z	=	High impedance level
UN	=	Undriven Node or input
Q(n)	=	The level of Q before an active transition on the affecting node
QN(n)	=	The level of QN before an active transition on the affecting node

2.3.7 PIN LOADING: A table of cell input capacitances in picofarads. Output pin capacitance is given for 3 state cells only. This information can be used to determine the fan-out loading on cell outputs.

2.3.8 EQUIVALENT GATES: Equivalent gates for the cell is defined as the cell area normalized to the area of the NA21 (2 input nand gate).

2.3.9 BOLT SYNTAX: BOLT (Block Oriented Logic Translator) is a AMI proprietary netlist format. This line shows the BOLT syntax for the cell. One example of the use of BOLT is as a design interface from the workstation design kits to AMI.

2.3.10 POWER CHARACTERISTICS:

2.3.10.1 Power for the cell can be described in three parts. The first part is the power dissipated due to the leakage current across the channels and through the formed diodes. The second part is due to the switching voltage across capacitance on the internal nodes of the cell. And, the third part is due to the switching voltage across a load capacitance.

2.3.10.2 The power characteristics table provides the static leakage current for a junction temperature of 85 degrees C, and the capacitance for all the switching nodes in the cell. It also gives the equation calculating power from these two values. It does not include the power due to the load capacitance. This capacitance can be obtained by adding up all the input capacitances of the driven cells and adding the interconnect capacitance. The average interconnect capacitance for the 1.0 micron ASIC Standard library is 0.047pF. AMI can prepare an estimate of the power upon submission of a netlist which uses a statistical model of the interconnect based on die size and fan-out.

$$Power = (Static\ I_{DD})\ V_{DD} + C_{pd}V^2_{DD}f + C_LV^2_{DD}f$$

where

$Static\ I_{DD}$ = *static leakage current of the cell*
V_{DD} = *operating voltage*
C_{pd} = *capacitance of the switching nodes in the cell*
f = *frequency of operation*
C_L = *capacitance of the driven pins and interconnect*

The frequency terms of the power equation dominates, making the static current term insignificant. However, the term can be used to find the standby current.

2.3.11 DELAY CHARACTERISTICS: This table contains delay data for the various input to output paths in the cells. Table 7 explains each column in the delay characteristics table.

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Table 7

EXPLANATION OF COLUMNS IN THE CELL CHARACTERISTICS TABLE		
Column Name	Explanation	
Max Delay (ns) From To	Names the two pins that identify the path for the delay	
Parameter	Mnemonic for the propagation delay or timing parameter whose value can be calculated by using the tdx and Ktdx columns in conjunction with the propagation delay equation	
	t_{PLH}	Input to output propagation delay for a rising edge on the output
	t_{PHL}	Input to output propagation delay for a falling edge on the output
	t_{ZH}	High impedance to high level delay
	t_{ZL}	High impedance to low level delay
	t_{HZ}	High level to high impedance delay
	t_{LZ}	Low level to high impedance delay
	t_{su}	Input setup time with respect to clock
	t_h	Input hold time
tdx (ns)	Contains values for the intrinsic delay through the cell. The x in t_{dx} is a variable representing r for the rising output delay (t_{PLH}), f for the falling output delay (t_{PHL}), or x for any of the other parameters. The values are given in nanoseconds.	
Ktdx (ns)	Contains delay per capacitance values to determine the delay due to capacitance loading on the "To" pin. The x in K_{tdx} has the same meaning as in the t_{dx}. The values are given in nanoseconds/picofarad.	
Number of fanouts	Contains the capacitance value and delay values for different loads. For output pad cells 25pF, 50pF, 75pF, and 100pF loads are used. For core cells and input pad cells fanouts of 2, 4, and 8 gates are used. These fanout loads are determined by the indicated number of NA21 inputs and an interconnect capacitance from a statistical table of fanout values for a chip that is 250 mils on a side.	

2.3.12 PROPAGATION DELAY EQUATION: This equation shows how to calculate the total delay for the load dependent delay paths using the delay characteristics table. Here are some notes to help in understanding how to use the equations.

2.3.12.1 $K_{PV}K_T$ are the derating factors for finding delays at conditions other than typical. Use Figures 6 and 7 for these values of K_P, K_V, and K_T. $K_{PV} = K_P{*}K_T$.

2.3.12.2 When the equations use t_{dx} and K_{tdx}, use either rise delay values or fall delay values for both variables.

2.3.12.3 If rise and fall delay numbers need to be inter-mixed, the equations will specifically state this, i.e. $t_{dr} + K_{tdf}(C_L)$.

2.3.12.4 If the equations inter-mix delays from different paths, then the delay variable will designate this with a pin value in parenthesis at the end of the variable.

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2.4 GDx Series Bases

The AMI bases are built using a "sea-of-gates" architecture; that is, they consist of a solid array of P and N channel devices built without routing channels. This allows greater flexibility in building cell macros, especially large memory macros, and allows for much tighter routing. Flexible I/O sites surround the sea-of-gates core which can be programmed to be inputs, outputs, I/Os, or power supply pins. Further, in order to minimize supply noise in the core and input buffer cells, all I/O sites contain double VSS or ground supply busses, with one set isolated from the core and dedicated to supplying output drivers only. In addition, there are three "fixed", non-programmable supply pins in each corner of the die.

The capacity of all bases in the GDx series arrays is given in Table 8. The "Base Name" column contains the names of the bases available in the GDx series. Numbers in the "Raw Gates" column represent the number of sites available for gate placement in the core of the given base, while the numbers given in the columns below "Usable Gates" are estimates of the size of netlist that can be routed into the base. Of course, due to the space taken by interconnection of cells, the number of usable gates cannot be as large as the raw sites; however, depending on the amount of interconnect required to route the netlist, very high usage can be achieved by using triple-level interconnect, as can be seen in the "Triple Metal" column. In situations where the pin count rather than core size dictates the selection of the base, or where device cost or fabrication spans are critical parameters, double metal routing can be used. The "Double Metal" column indicates an estimated maximum size for a netlist that can be routed on the given base using two levels of interconnect. Finally, the last column gives the number of programmable pins available for each base. This pin count typically includes both I/O pins and supplies. Also, note that the numbers given do not include the 12 fixed supply pins which can be used for additional supply pins if desired.

Table 8 : Capacities of GDx Series Gate Array Bases

Base Name	Raw Gates	Usable Gates		Programmable Pad Count	
		Triple Metal	Double Metal	Available 5 mil	In Development
GD170K	166,332	123,100	94,100	368	460
GD115K	115,856	85,700	64,500	304	384
GD85K	83,776	62,000	45,300	256	324
GD50K	55,664	41,200	29,400	204	256
GD35K	37,200	27,500	19,600	168	210
GD25K	26,600	19,700	14,000	140	174
GD20K	22,320	16,500	11,800	130	162
GD16K	17,264	12,800	9,100	112	142
GD12K	13,286	9,800	7,000	96	122
GD9K	9,920	7,300	5,200	84	106
GD7K	7,632	5,600	4,000	72	92
GD5K	5,104	3,800	2,700	60	76
GD3K	2,580	1,900	1,400	44	56

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2.5 Packaging

Package Lead Count	GDx Series Gate Array Base												
	170K	115K	85K	50K	35K	25K	20K	16K	12K	9K	7K	5K	3K
Plastic Quad Flat Packages - PQFP's													
44						A	A	A	A	A	A	A	A
52					A	A	A	A	A	A	A	A	A
64				A	A	A	A	A	A	A	A	A	A
80				A	A	A	A	A	A	A	A	A	A
100			A	A	A	A	A	A	A	A	A	A	
120			A	A	A	A	A	A	A	A	A		
128			A	A	A	A	A	A	A				
144		A	A	A	A	A	A	A					
160		A	A	A	A	A	A						
208		A	A	A									
256		D	D										
304	D	D											
Plastic Pin Grid Arrays - PPGA's													
68			A	A	A	A	A	A	A	A			
84				D	A	A	A	A	A	A			
100				D	A	A	A	A	A	A			
108					A	A	A	A	A				
120				A	A	A	A	A	A				
132			D	D	A	A	A	A	A				
144			A	A	D	D							
180			A	A									
208		D	D										
224	D	D	D										
Plastic Leadless Chip Carriers - PLCC's													
20									A	A	A	A	A
28						A	A	A	A	A	A	A	A
44				A	A	A	A	A	A	A	A	A	A
68				A	A	A	A	A	A	A	A	A	A
84			A	A	A	A	A	A	A	A	A	A	A
Plastic Dual-In-line Packages - PDIP's													
8													A
14													A
16												A	A
18													A
20													A
22									A	A	A	A	A
24						A	A	A	A	A	A	A	A
28						A	A	A	A	A	A	A	A
40				A	A	A	A	A	A	A	A	A	A
48					A	A	A	A	A	A	A	A	A

A - Package is available for the indicated device D - Package is under development ▨ -Not available (previously listed as available or in development)

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Package Lead Count	GDx Series Gate Array Base												
	170K	115K	85K	50K	35K	25K	20K	16K	12K	9K	7K	5K	3K
Ceramic J Leaded Chip Carriers - CLDCC's													
28										A	A	A	A
44							A	A	A	A			
48							A	A	A	A			
52							A	A	A	A			
68				A	A	A	A	A	A	A			
84		D	D	A	A	D	D	D	D	D			
Ceramic Pin Grid Arrays - CPGA's													
64								D	D	D	D		
68				A	A	A	A	A	A	A	A		
84				A	A	A	A						
100					A	A	A						
108				A									
120				A									
132				A									
144			A	A	D								
154			A										
176		D	A	A									
180	D	D	A	D									
224	D	D	D	D									
256		A											
299	D	D											
391	D	D											
512	D												
Ceramic Quad Flat Packages - CQFP's													
40							A	A	D	D	D	D	D
44					A	A	A	A	D				
84							A	A	A	A	A		
132			D	D	D								
144				A									
172					A	A							
196		D	A	A	A								
224	D	D											
256	D	D											
340	D												
Ceramic Leadless Chip Carriers - CLCC's													
20													A
24											A	A	A
28							A	A	A	A	A	A	A
36							A	A	A	A	A	A	A
40							A	A	A	A			
44					A	A	A	A	A	A	A	A	A
48					A	A	A	A	A	A			
52							A	A	A	A	A		
68				A	A	A	A	A	A				
84		D		A	A								

A - Package is available for the indicated device D - Package is under development ▨ -Not available (previously listed as available or in development)

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2.6 AMI Design Flow

The typical design flow is shown in . describes how the supported third party tools can be used to interface with AMI. A designer starts with a specification entered in a supported third-party CAE workstation. The design is captured graphically using elements from AMI's ASIC Standard Library. This is a portable library that is process and technology independent, which allows for upward migration.

Timing simulation can then be performed with user-supplied test vectors and/or automatically generated test vectors. Fault coverage of the test vector set can be verified as an additional service. AMI's ACCESS Design Tools are intended to be used interactively at each stage of the design .A final analysis is performed prior to sending the design to the factory. Design analysis tools check both the design and test vectors for correctness and compatibility with in-house ASIC testers. The design is also analyzed for inefficiencies and possible flaws that could cause problems in manufacturing the device.

When the design is received by the factory, the "Design Start Package" is reviewed by AMI engineers. This start package, which is supplied by the designer, contains the device specification, netlist, critical timing paths, and vectors. For designs that have not previously been screened by the ACCESS Design Tools this process must be performed. The design is then simulated on AMI's sign-off simulator and the results compared to the customers simulation from the third-party CAE tool.

Once the design has passed the initial screening it is then ready for placement and routing. The layout proceeds by first placing special macros, assigning priority to critical paths, and designing the distribution and buffering of clocks. The balance of the circuit is then automatically placed and routed.

After layout has been completed the interconnect data is extracted from the physical layout to be fed back to the sign-off simulator for final circuit verification. This post layout interconnect data can be sent to the customer for his final validation. When the post-layout simulation has been completed the design is then released for mask and wafer fabrication. The test program is developed in parallel with the wafer fabrication using internal automatic test pattern generation software.

AMI's factory engineers and Field Application Engineers (FAEs) offer assistance in performing any step of the design flow. These services include functional and timing simulation, fault vector grading, and test vector generation.

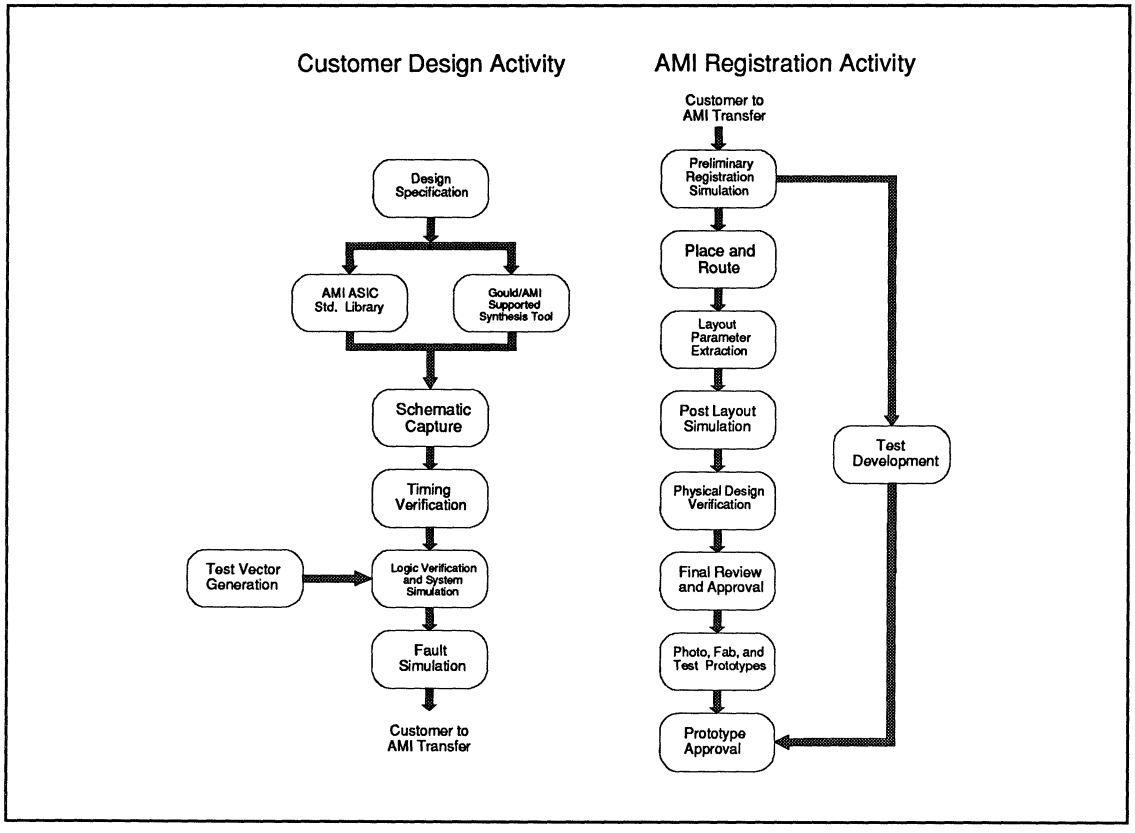

Figure 9: Typical Design Flow

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Figure 10 identifies how the designer can use AMI-supported third party tools to develop and transmit designs to AMI. AMI is developing additional tools in both the synthesis and CAE environments. Through the use of standard interface tools such as EDIF, AMI has developed libraries which are "graphically" portable among the various supported workstations. Currently, logic synthesis is supported on Synopsys™. Schematics that are generated using that tool can be ported into the other CAE environments using EDIF schematic writers and readers.

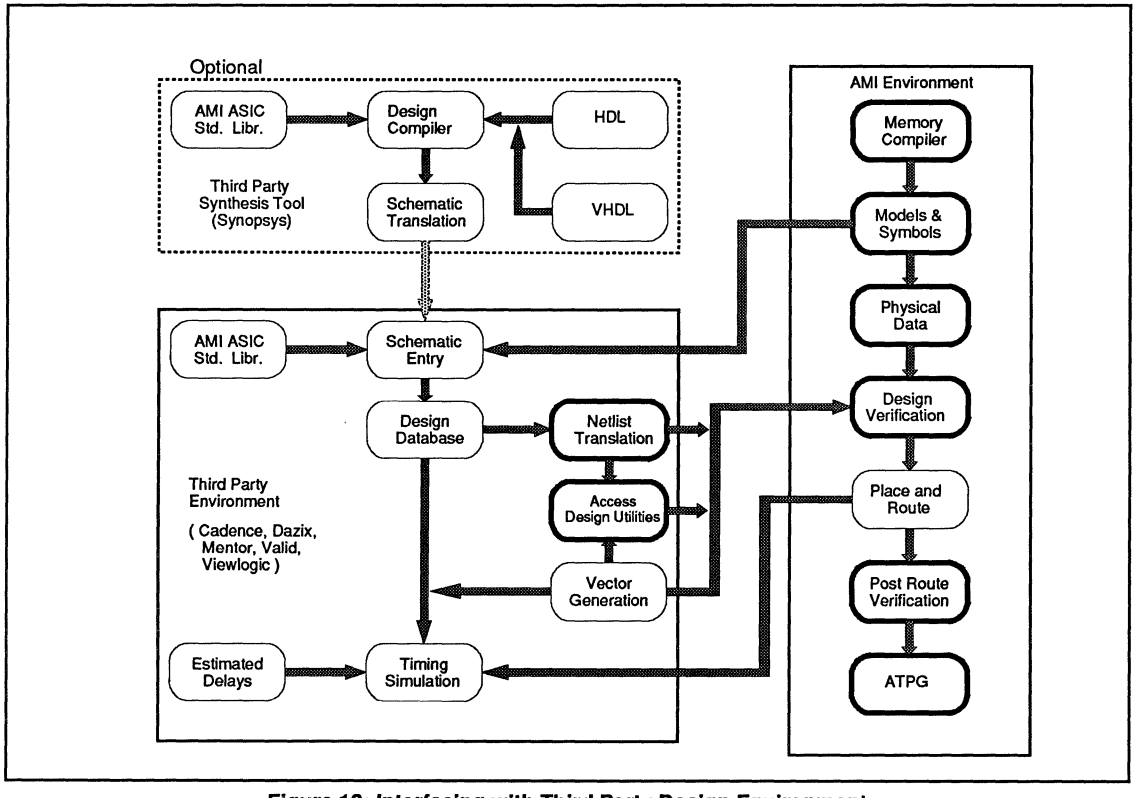

Figure 10: Interfacing with Third Party Design Environment

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2.7 Megacells

A wide array of megacells are also available in the AMI ASIC Standard library ranging from an eight bit I/O port and microcontrollers to generated cells such as adders and read/write memory. All of the megacells consist of an assemblage of low level ASIC Standard cells, therefore, the resulting megacells are portable across technologies just as the lower level cells are. Generated megacells are large cell blocks which can be built to specified dimensions. For instance, if an application requires the multiplication of two 12 bit words, a 12x12 multiplier megacell can be generated and supplied for use as an element in a netlist, likewise for an adder. Single and dual port RAM block generators are also available which utilize the sea-of-gates architecture of the gate array base core to implement a dense, fast memory core in sizes ranging from 32 x 1 to 1024 x 32. Thus, upon request, AMI will build and deliver a complete RAM macrocell on the requested workstation. The Megacell offering is listed in Table 9.

Table 9 : AMI ASIC Standard Library Megacells

Cell Name	Description	Equivalent Gates
MG29C01	4-Bit Microprocessor Slice	600
MG29C10	Microprogram Controller/Sequencer	750
MG80C85	8-Bit CMOS Microprocessor	2000
MG82C37A	Programmable DMA Controller	3000
MG82C50A	Asynchronous Communications Element	2300
MG82C54	Programmable Interval Timer	2600
MG82C55A	Programmable Peripheral Interface	750
MG82C59A	Programmable Interrupt Controller	900
MG82C84A	Clock Generator and Driver	400
MGMC51	8-Bit Microcontroller, Intel™ Equivalent	9500
Multipliers	2's Comp. Cell Generator, sizes up to 32x32	Generated
Adders	2's Comp. Cell Generator, sizes up to 32x32	Generated
FIFOs	First In First Out Register Generator	Generated
Barrel Shifter	Barrel Shift Generator	Generated
RAM	Cell Generator, sizes range from 32x1 to 1024x32	Generated

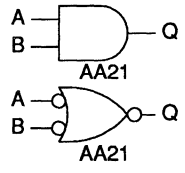
SECTION 3

ASIC STANDARD FUNCTIONS

Description:

AA21 is a two-input gate, which performs a logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .AA21 A B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	17.0	nA
†C_{pd}	0.25	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.36	1.12	0.54	0.73	1.11
		t_{PHL}	0.40	0.66	0.50	0.62	0.84

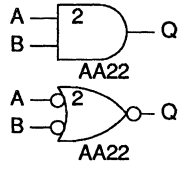
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description:

AA22 is a two-input gate, which performs a logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .AA22 A B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} T_J = 85°C	25.4	nA
†C_{pd}	0.39	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

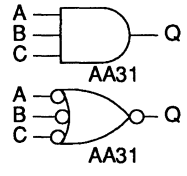
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.43	0.59	0.53	0.63	0.82
		t_{PHL}	0.47	0.44	0.54	0.61	0.76

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

AA31 is a three-input gate, which performs a logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .AA31 A B C ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	17.0	nA
†C_{pd}	0.36	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

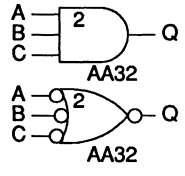
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
Any Input	Q	t_{PLH}	0.54	1.16	0.72	0.92	1.31
		t_{PHL}	0.51	0.74	0.63	0.75	1.00

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

AA32 is a three-input gate, which performs a logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.07

Equivalent Gates: 3
Bolt Syntax: .....Q .AA32 A B C ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	25.4	nA
†C_{pd}	0.51	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

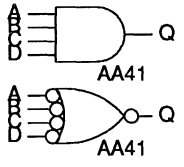
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.64	0.64	0.74	0.85	1.07
		t_{PHL}	0.59	0.48	0.66	0.74	0.91

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

AA41 is a four-input gate, which performs a logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.06
D	0.07

Equivalent Gates: 3
Bolt Syntax: .....Q .AA41 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	21.2	nA
†C_{pd}	0.41	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

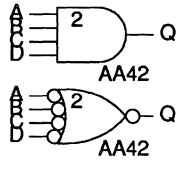
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.70	1.23	0.89	1.10	1.52
		t_{PHL}	0.57	0.77	0.70	0.83	1.09

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

AA42 is a four-input gate, which performs a logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.06
D	0.07

Equivalent Gates: 3
Bolt Syntax: .....Q .AA42 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	25.4	nA
†C_{pd}	0.55	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

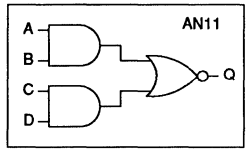
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.82	0.68	0.92	1.04	1.27
		t_{PHL}	0.64	0.51	0.72	0.81	0.98

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

AN11 is an AND-NOR circuit consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.07
D	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .AN11 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	17.0	nA
$^{\dagger}C_{pd}$	0.31	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

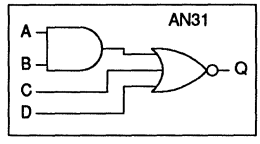
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.51	1.56	0.76	1.03	1.55
		t_{PHL}	0.27	0.81	0.40	0.54	0.81

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

AN31 is an AND-NOR circuit consisting of a 2-input AND gate and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.07
D	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .AN31 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	25.4	nA
†C_{pd}	0.30	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

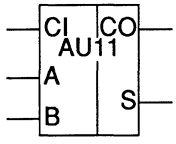
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
Any Input	Q	t_{PLH}	0.94	3.02	1.43	1.95	2.96
		t_{PHL}	0.23	0.86	0.36	0.51	0.80

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

AU11 is a combinational one bit full adder.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Pin Loading

	Ci (pF)
A	0.27
B	0.27
CI	0.21

Equivalent Gates: 7
Bolt Syntax: ..... CO S .AU11 A B CI ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	75.9	nA
†C_{pd}	1.39	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

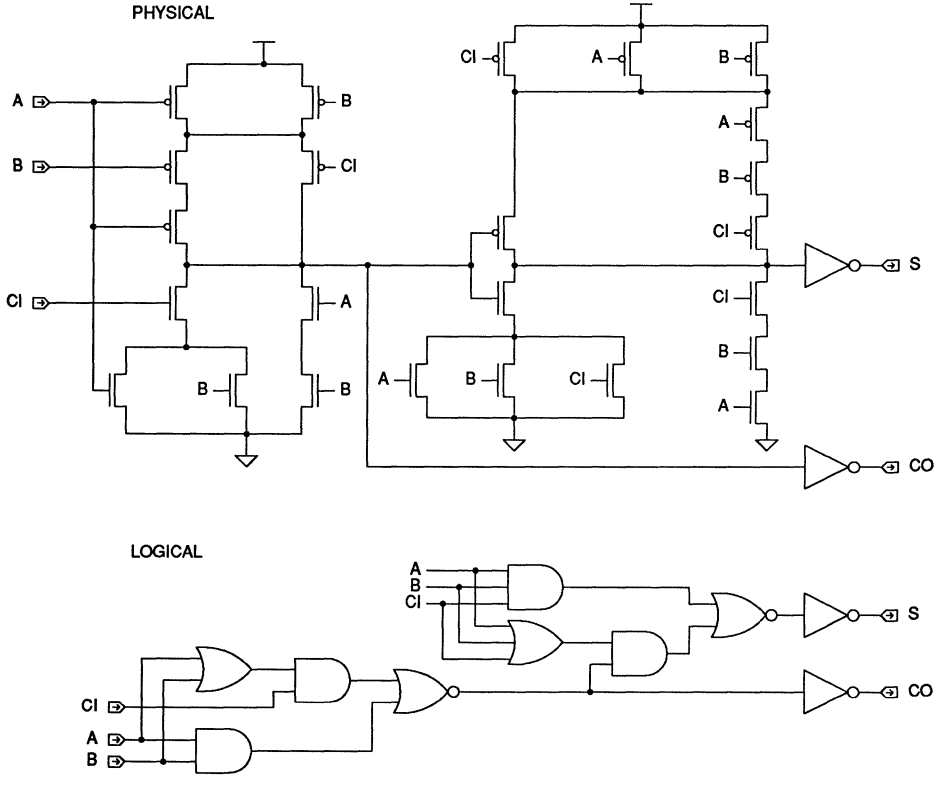
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
A	S	t_{PLH}	1.58	1.14	1.77	1.96	2.34
		t_{PHL}	1.11	1.01	1.27	1.45	1.79
B	S	t_{PLH}	1.79	1.14	1.97	2.17	2.55
		t_{PHL}	1.43	1.01	1.59	1.77	2.10
CI	S	t_{PLH}	0.69	1.14	0.87	1.07	1.45
		t_{PHL}	1.28	1.01	1.44	1.62	1.96
A	CO	t_{PLH}	0.63	1.17	0.82	1.02	1.41
		t_{PHL}	1.16	1.15	1.35	1.55	1.93
B	CO	t_{PLH}	0.63	1.17	0.82	1.02	1.42
		t_{PHL}	1.21	1.15	1.40	1.59	1.98
CI	CO	t_{PLH}	0.57	1.17	0.75	0.95	1.35
		t_{PHL}	0.82	1.15	1.01	1.21	1.59

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Logic Schematic

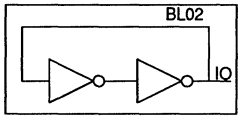


April, 1992

BL02

Description:

BL02 is a tri-state bus latch that stores the final binary level on the bus when left undriven.

Logic Symbol	Truth Table	Pin Loading
	N/A	Ci (pF) IO 0.15

Equivalent Gates: 7
Bolt Syntax: .....IO .BL02;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	17.0	nA
†C_{pd}	1.92	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)
IO	IO	t_{PLH}	0.30
		t_{PHL}	0.58

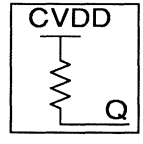
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L$

ASIC Functions

Description:

CVDD is the resistive tie-up to the core Vdd bus for all macro inputs.

Equivalent Gates: 1
Bolt Syntax: ..... Q .CVDD;



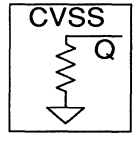
April, 1992

CVSS

Description:

CVSS is the resistive tie-down to the core Vss bus for all macro inputs.

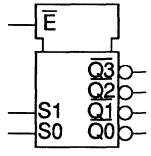
Equivalent Gates: 1
Bolt Syntax: ..... Q .CVSS;



Description:

DC24 is a two-to-four line decoder/demultiplexer with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Pin Loading

	Ci (pF)
S0	0.21
S1	0.20
EN	0.07

Equivalent Gates: 8
Bolt Syntax: .....Q0N Q1N Q2N Q3N .DC24 EN S0 S1;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	63.2	nA
†C_{pd}	1.65	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

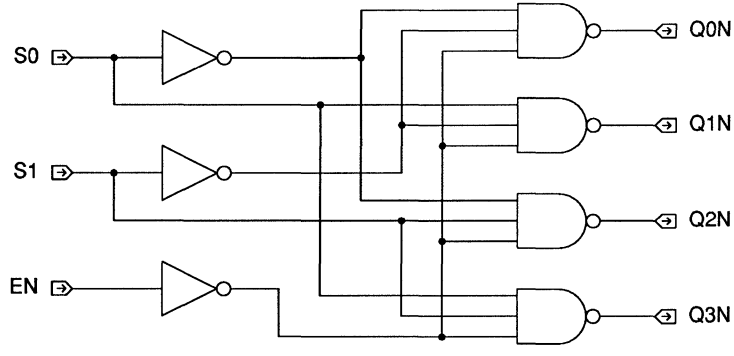
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
Sx	QN	t_{PLH}	0.44	1.15	0.63	0.82	1.21
		t_{PHL}	0.53	1.10	0.71	0.90	1.27
EN	QN	t_{PLH}	0.62	1.15	0.81	1.00	1.39
		t_{PHL}	0.75	1.10	0.93	1.11	1.39

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

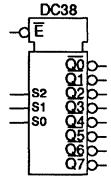
Logic Schematic



Description:

DC38 is a three-to-eight line decoder/demultiplexer with active low enable.

Logic Symbol



Truth Table

Truth Table Appears On Next Page

Pin Loading

	Ci (pF)
S0	0.35
S1	0.35
S2	0.36
EN	0.07

Equivalent Gates: 18
Bolt Syntax: .....Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N .DC38 EN S0 S1 S2 ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	151.6	nA
†C_{pd}	3.81	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

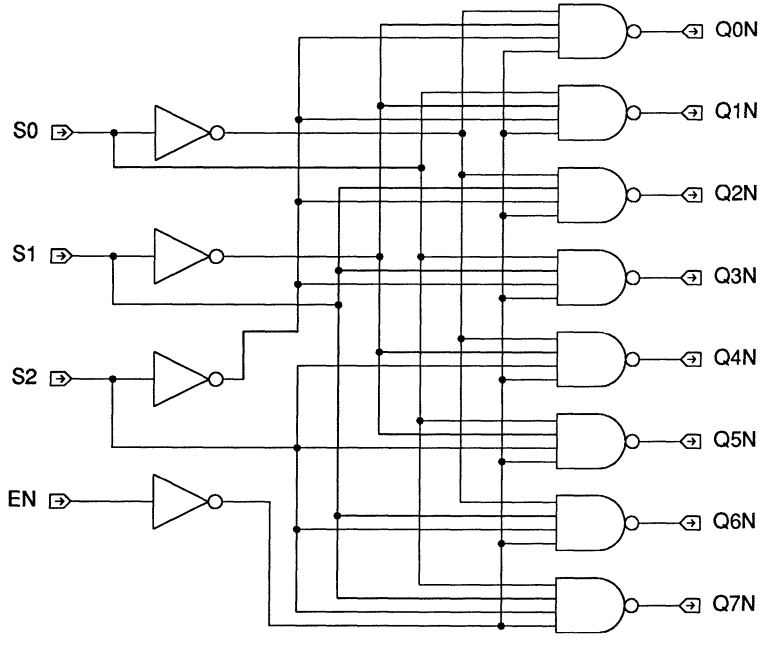
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
Sx	QN	t_{PLH}	0.69	0.72	0.80	0.93	1.17
		t_{PHL}	0.88	0.85	1.01	1.16	1.44
EN	QN	t_{PLH}	0.97	0.72	1.08	1.21	1.45
		t_{PHL}	1.24	0.85	1.38	1.52	1.80

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

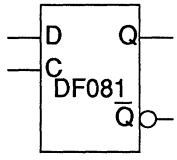
Logic Schematic



Description:

DF081 is a static master-slave D flip-flop without set or reset. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
H	↑	H	L
L	↑	L	H
X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
C	0.21

Equivalent Gates: 6
Bolt Syntax: .....Q QN .DF081 C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	59.0	nA
†C_{pd}	1.61	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

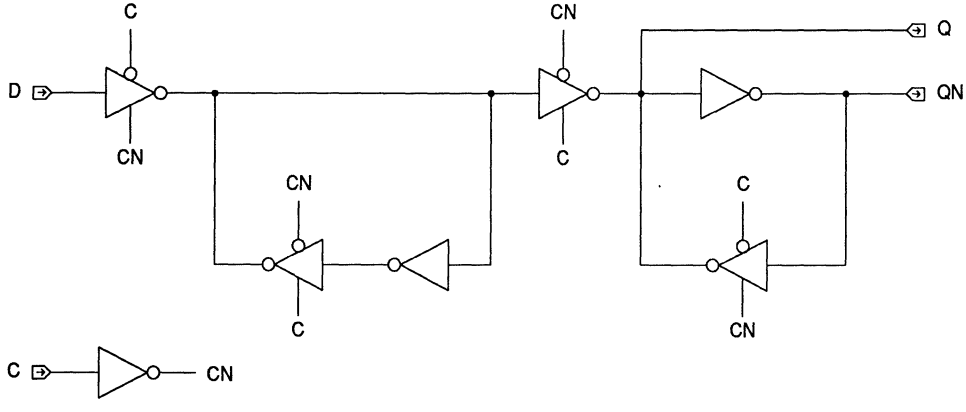
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	Q	t_{PLH}	0.78	2.02	1.10	1.45	2.12
		t_{PHL}	0.22	0.67	0.33	0.45	0.67
C	QN	t_{PLH}	0.53	1.15	0.72	0.92	1.30
		t_{PHL}	0.95	0.91	1.10	1.25	1.56
Min C Width	High	t_w				0.95	
Min C Width	Low	t_w	1.08				
Min D Setup		t_{su}	1.08				
Min D Hold		t_h	0.00				

For Q Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{dr}(QN) + (k_{tdr}(QN) \cdot C_L(QN)) + (k_{tdf}(Q) \cdot C_L(Q))]$

$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{df}(QN) + (k_{tdf}(QN) \cdot C_L(QN)) + (k_{tdr}(Q) \cdot C_L(Q))]$

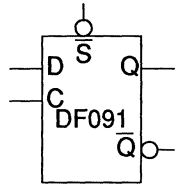
Logic Schematic



Description:

DF091 is a static master-slave D flip-flop. Set is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
C	0.21
SN	0.14

Equivalent Gates: 7
Bolt Syntax: .....Q QN .DF091 C D SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} T_J = 85°C	59.0	nA
†C_{pd}	1.92	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

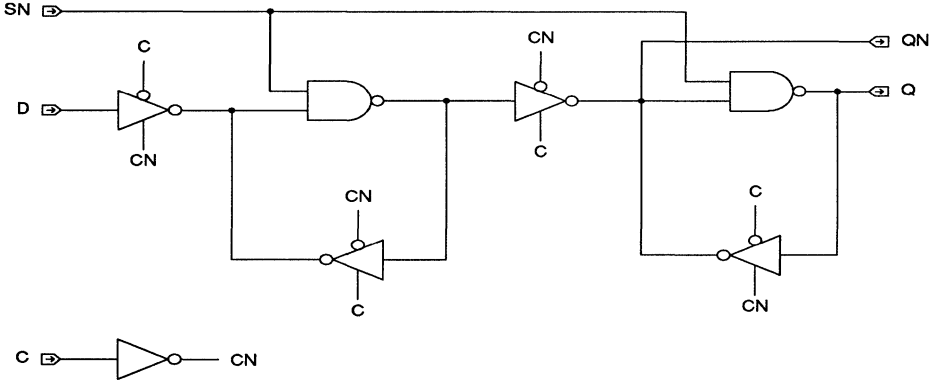
Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	0.76	2.02	1.08	1.43	2.10
		t_{PHL}	0.22	0.66	0.33	0.44	0.66
C	Q	t_{PLH}	0.56	1.15	0.75	0.95	1.33
		t_{PHL}	1.06	1.06	1.23	1.41	1.76
SN	Q	t_{PLH}	0.32	1.15	0.51	0.71	1.09
SN	QN	t_{PHL}	0.77	0.66	0.87	0.98	1.20
Min C Width	High	t_w				1.06	
Min C Width	Low	t_w	1.07				
Min SN Width	Low	t_w				0.77	
Min D Setup		t_{su}	1.07				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.30				
Min SN Hold		t_h	0.21				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

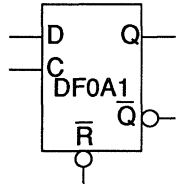
Logic Schematic



Description:

DF0A1 is a static master-slave D flip-flop with asynchronous, active low reset. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
C	0.22
RN	0.07

Equivalent Gates: 7

Bolt Syntax: .....Q QN .DF0A1 C D RN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} T_J = 85°C	84.2	nA
†C_{pd}	1.98	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

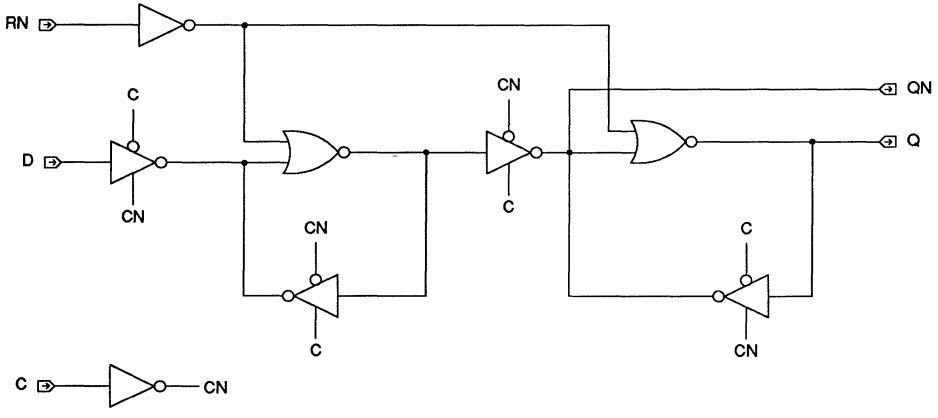
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
C	QN	t_{PLH}	0.77	2.03	1.10	1.45	2.13
		t_{PHL}	0.22	0.66	0.32	0.44	0.66
C	Q	t_{PLH}	0.67	2.05	1.00	1.35	2.04
		t_{PHL}	0.93	0.93	1.08	1.24	1.55
RN	Q	t_{PHL}	0.48	0.93	0.63	0.79	1.10
RN	QN	t_{PLH}	1.29	2.03	1.61	1.96	2.64
Min C Width	High	t_w				0.93	
Min C Width	Low	t_w	1.16				
Min RN Width	Low	t_w				1.29	
Min D Setup		t_{su}	0.92				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.80				
Min RN Hold		t_h	0.72				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$

$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

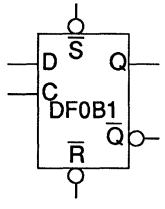
Logic Schematic



Description:

DF0B1 is a static, master-slave, D flip-flop, SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

NC = No Change
IL = Illegal

Pin Loading

	Ci (pF)
D	0.06
C	0.22
SN	0.14
RN	0.14

Equivalent Gates: 8
Bolt Syntax: ..... Q QN .DF0B1 C D RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	75.8	nA
†C_{pd}	2.42	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

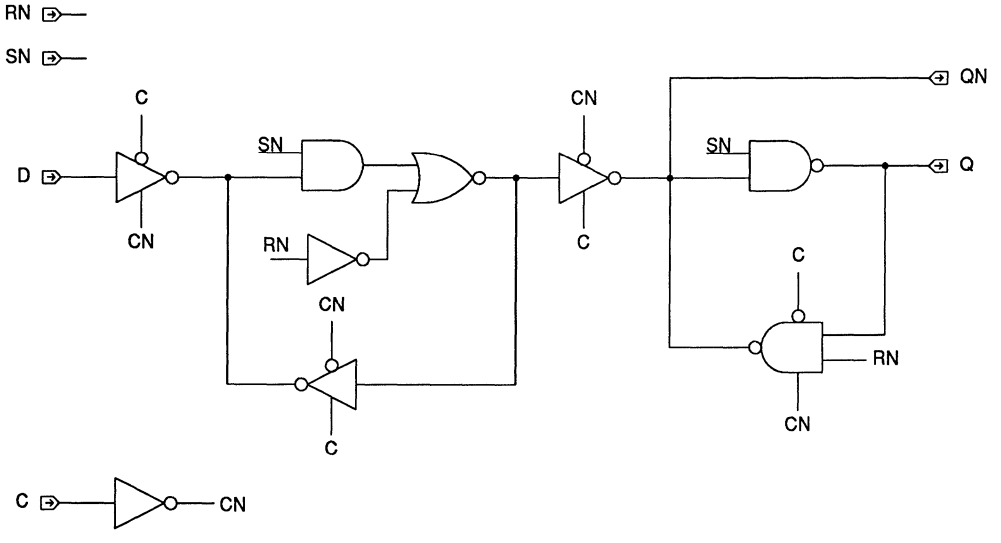
Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	0.79	2.02	1.11	1.46	2.13
		t_{PHL}	0.23	0.66	0.33	0.45	0.67
C	Q	t_{PLH}	0.55	1.17	0.74	0.94	1.33
		t_{PHL}	1.06	1.09	1.23	1.42	1.79
SN	Q	t_{PLH}	0.30	1.17	0.49	0.69	1.08
SN	QN	t_{PHL}	1.09	0.66	1.19	1.30	1.53
RN	Q	t_{PHL}	1.23	1.09	1.40	1.59	1.96
RN	QN	t_{PLH}	0.96	1.17	1.28	1.63	2.30
Min C Width	High	t_w				1.06	
Min C Width	Low	t_w	1.23				
Min RN Width	Low	t_w				1.23	
Min SN Width	Low	t_w				1.09	
Min D Setup		t_{su}	1.06				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.90				
Min RN Hold		t_h	0.74				
Min SN Setup		t_{su}	0.29				
Min SN Hold		t_h	0.21				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

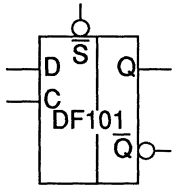
Logic Schematic



Description:

DF101 is a static, master-slave D flip-flop. Set is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
C	0.21
SN	0.14

Equivalent Gates: 8
Bolt Syntax: .....Q QN .DF101 C D SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	75.8	nA
†C_{pd}	2.19	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

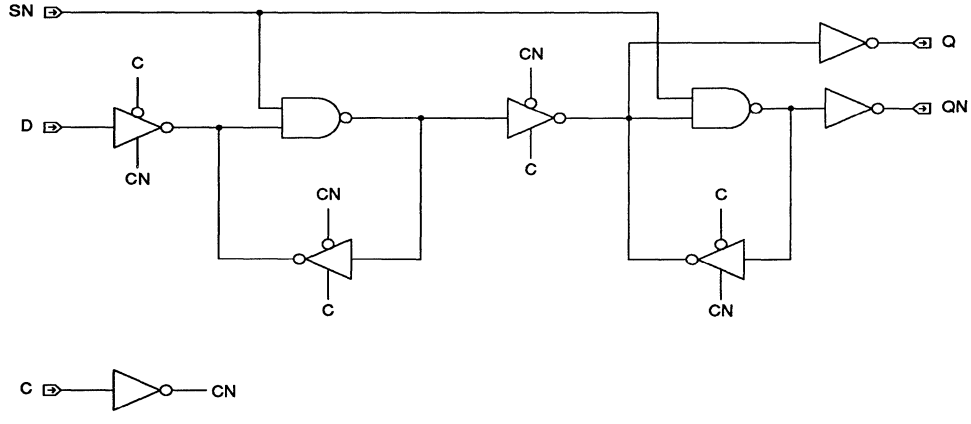
Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	1.54	1.14	1.72	1.91	2.30
		t_{PHL}	0.79	0.74	0.91	1.03	1.28
C	Q	t_{PLH}	0.47	1.17	0.66	0.86	1.25
		t_{PHL}	0.98	1.01	1.15	1.32	1.66
SN	Q	t_{PLH}	1.03	1.17	1.22	1.42	1.81
SN	QN	t_{PHL}	0.51	0.74	0.63	0.76	1.00
Min C Width	High	t_w	1.28				
Min C Width	Low	t_w	1.07				
Min SN Width		t_w	0.80				
Min D Setup		t_{su}	1.07				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.30				
Min SN Hold		t_h	0.21				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Logic Schematic



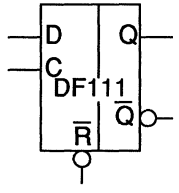
April, 1992

DF111

Description:

DF111 is a static master-slave D flip-flop. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
C	0.22
RN	0.07

Equivalent Gates: 8

Bolt Syntax: .....Q QN .DF111 C D RN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^\circ C$	101.1	nA
†C_{pd}	2.26	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

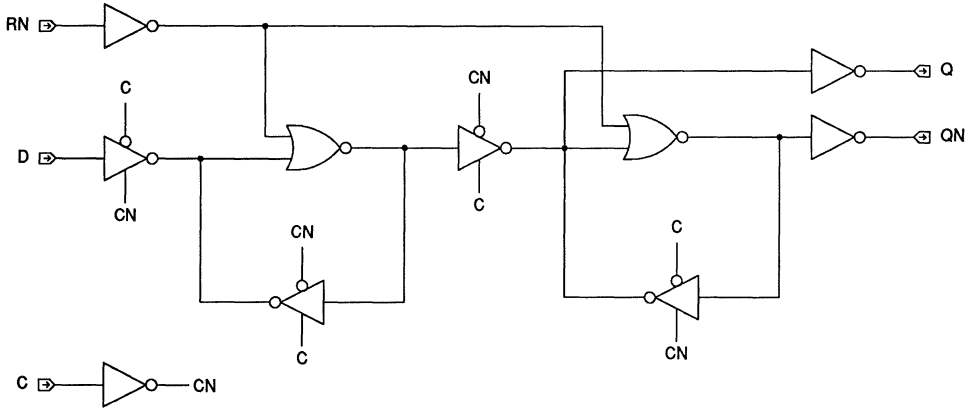
Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	1.37	1.10	1.55	1.74	2.11
		t_{PHL}	0.97	0.89	1.11	1.26	1.56
C	Q	t_{PLH}	0.47	1.16	0.65	0.85	1.24
		t_{PHL}	1.00	1.03	1.16	1.34	1.68
RN	Q	t_{PHL}	1.51	1.03	1.68	1.85	2.20
RN	QN	t_{PLH}	0.72	1.10	0.90	1.09	1.46
Min C Width	High	t_w	1.15				
Min C Width	Low	t_w	1.15				
Min RN Width		t_w	1.44				
Min D Setup		t_{su}	0.92				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.80				
Min RN Hold		t_h	0.71				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Logic Schematic



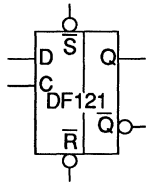
April, 1992

DF121

Description:

DF121 is a static, master-slave, D flip-flop, SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

NC = No Change
IL = Illegal

Pin Loading

	Ci (pF)
D	0.07
C	0.23
SN	0.14
RN	0.14

Equivalent Gates: 10
Bolt Syntax: .....Q QN .DF121 C D RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	92.7	nA
†C_{pd}	2.69	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

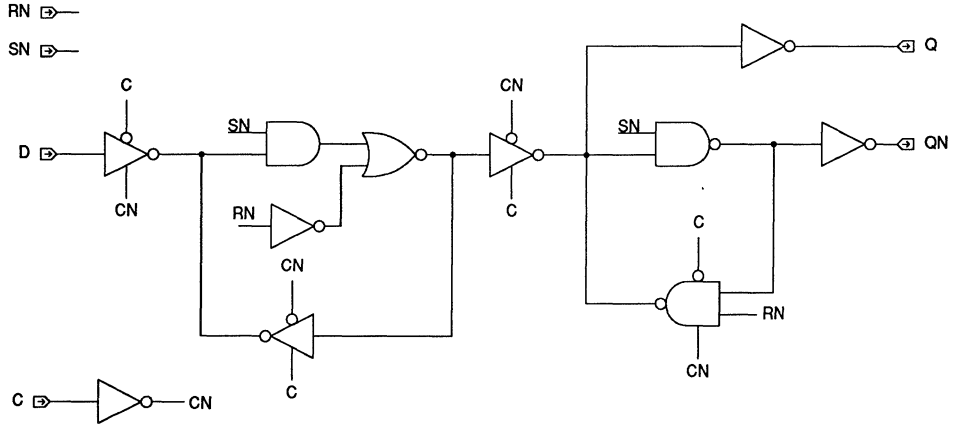
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	1.54	1.15	1.72	1.92	2.30
		t_{PHL}	0.79	0.72	0.90	1.03	1.27
C	Q	t_{PLH}	0.49	1.17	0.68	0.88	1.27
		t_{PHL}	1.02	1.03	1.18	1.36	1.71
SN	Q	t_{PLH}	1.38	1.17	1.57	1.77	2.16
SN	QN	t_{PHL}	0.49	0.72	0.61	0.73	0.97
RN	Q	t_{PHL}	1.45	1.03	1.62	1.79	2.14
RN	QN	t_{PLH}	1.97	1.15	2.15	2.35	2.73
Min C Width	High	t_w	1.29				
Min C Width	Low	t_w	1.21				
Min RN Width		t_w	1.72				
Min SN Width		t_w	1.12				
Min D Setup		t_{su}	1.04				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.89				
Min RN Hold		t_h	0.73				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.21				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Logic Schematic



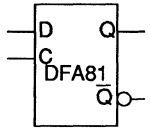
April, 1992

DFA81

Description:

DFA81 is a static master-slave D flip-flop without set or reset. Outputs are unbuffered, and change state on the rising edge of the clock. Equivalent to DF081 with transmission gates.

Logic Symbol



Truth Table

D	C	Q	QN
H	↑	H	L
L	↑	L	H
X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
C	0.21

Equivalent Gates: 5
Bolt Syntax: .....Q QN .DFA81 C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	50.6	nA
†C_{pd}	1.69	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

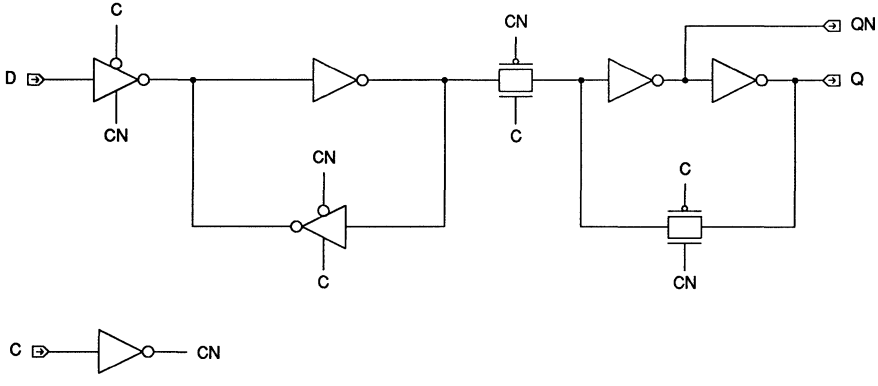
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	Q	t_{PLH}	0.85	1.11	1.03	1.22	1.59
		t_{PHL}	0.68	0.65	0.78	0.89	1.11
C	QN	t_{PLH}	0.38	1.15	0.56	0.76	1.14
		t_{PHL}	0.44	0.80	0.57	0.71	0.98
Min C Width	High	t_w				0.76	
Min C Width	Low	t_w	1.01				
Min D Setup		t_{su}	1.01				
Min D Hold		t_h	0.00				

For Q Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{dr}(QN) + (k_{tdr}(QN) \cdot C_L(QN)) + (k_{tdf}(Q) \cdot C_L(Q))]$

$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{df}(QN) + (k_{tdf}(QN) \cdot C_L(QN)) + (k_{tdr}(Q) \cdot C_L(Q))]$

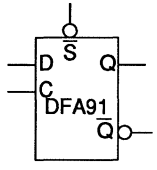
Logic Schematic



Description:

DFA91 is a static master-slave D flip-flop. Set is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Equivalent to DF091 with transmission gates.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.06
C	0.21
SN	0.13

Equivalent Gates: 6
Bolt Syntax: .....Q QN .DFA91 C D SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	50.6	nA
†C_{pd}	1.42	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

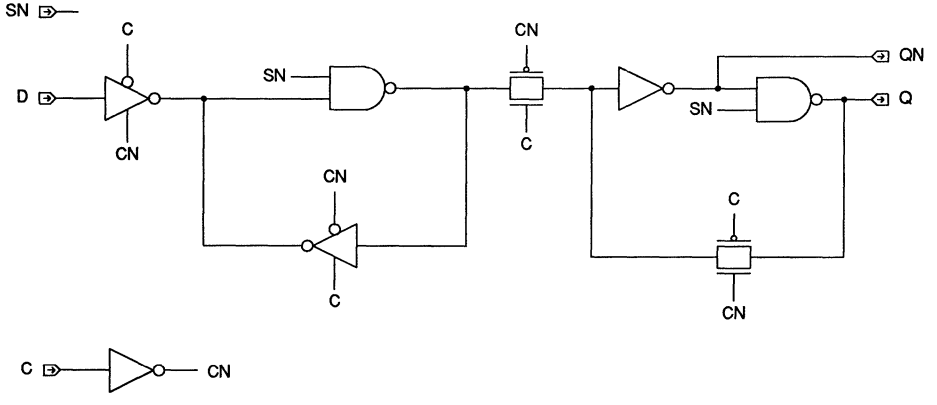
Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	0.47	1.19	0.66	0.87	1.27
		t_{PHL}	0.52	0.81	0.65	0.79	1.06
C	Q	t_{PLH}	0.81	1.12	0.99	1.18	1.55
		t_{PHL}	0.71	0.85	0.84	0.99	1.28
SN	Q	t_{PLH}	0.50	1.12	0.68	0.87	1.24
SN	QN	t_{PHL}	0.86	0.81	0.99	1.13	1.40
Min C Width	High	t_w				1.18	
Min C Width	Low	t_w	1.03				
Min SN Width	Low	t_w				1.13	
Min D Setup		t_{su}	1.03				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.21				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

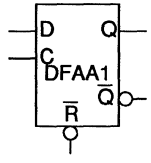
Logic Schematic



Description:

DFAA1 is a static master-slave D flip-flop with asynchronous, active low reset. Outputs are unbuffered and change state on the rising edge of the clock. Equivalent to DF0A1 with transmission gates.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
C	0.21
RN	0.14

Equivalent Gates: 6
Bolt Syntax: .....Q QN .DFAA1 C D RN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	50.6	nA
†C_{pd}	1.99	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

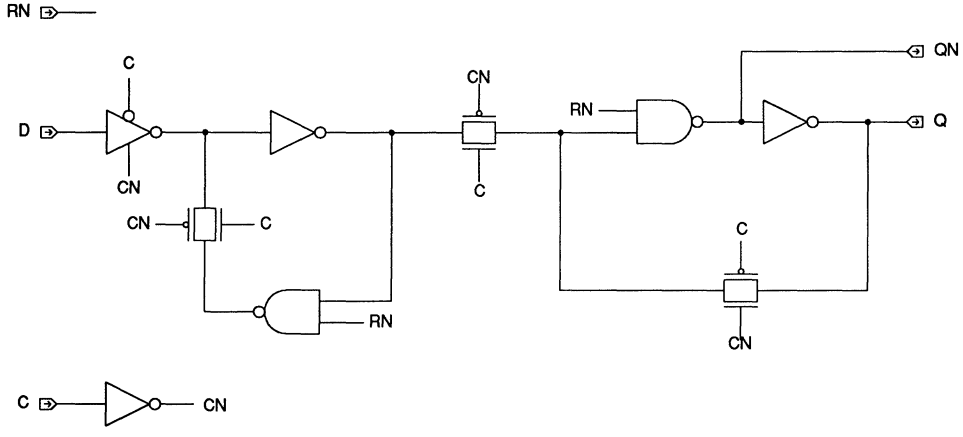
Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
C	QN	t_{PLH}	0.45	1.15	0.64	0.84	1.22
		t_{PHL}	0.60	1.00	0.76	0.93	1.27
C	Q	t_{PLH}	0.91	1.12	1.09	1.29	1.66
		t_{PHL}	0.62	0.67	0.72	0.84	1.06
RN	Q	t_{PHL}	0.57	0.67	0.67	0.79	1.01
RN	QN	t_{PLH}	0.31	1.15	0.49	0.69	1.08
Min C Width	High	t_w				1.62	
Min C Width	Low	t_w	0.94				
Min RN Width	Low	t_w				0.69	
Min D Setup		t_{su}	0.94				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.20				
Min RN Hold		t_h	0.36				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

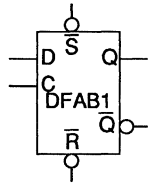
Logic Schematic



Description:

DFAB1 is a static, master-slave, D flip-flop, SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Equivalent to DF0B1 with transmission gates.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

NC = No Change
IL = Illegal

Pin Loading

	Ci (pF)
D	0.07
C	0.21
SN	0.14
RN	0.14

Equivalent Gates: 7
Bolt Syntax: ..... Q QN .DFAB1 C D RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85°C$	50.6	nA
†C_{pd}	2.22	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

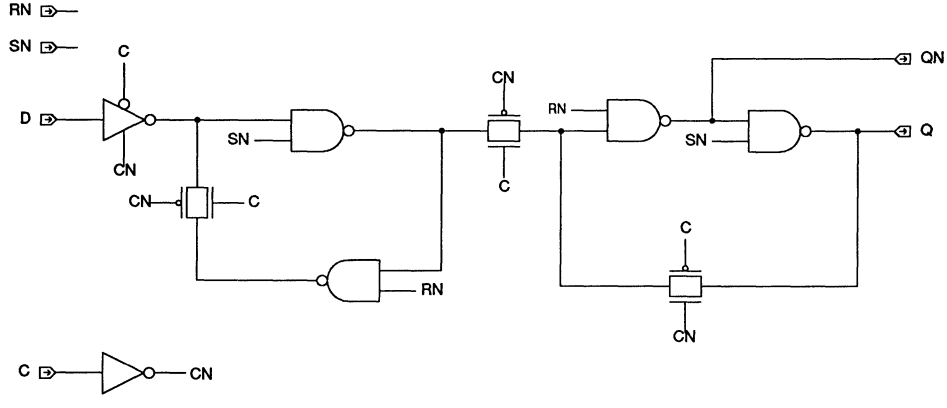
Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	0.49	1.19	0.68	0.88	1.28
		t_{PHL}	0.60	1.00	0.76	0.93	1.26
C	Q	t_{PLH}	0.90	1.13	1.08	1.28	1.65
		t_{PHL}	0.70	0.88	0.84	0.99	1.28
SN	Q	t_{PLH}	0.47	1.13	0.65	0.85	1.23
SN	QN	t_{PHL}	0.91	1.00	1.07	1.24	1.57
RN	Q	t_{PHL}	0.66	0.88	0.80	0.95	1.24
RN	QN	t_{PLH}	0.29	1.13	0.48	0.69	1.08
Min C Width	High	t_w				1.28	
Min C Width	Low	t_w	0.99				
Min RN Width	Low	t_w				0.95	
Min SN Width	Low	t_w				1.24	
Min D Setup		t_{su}	0.99				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.21				
Min RN Hold		t_h	0.36				
Min SN Setup		t_{su}	0.26				
Min SN Hold		t_h	0.17				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

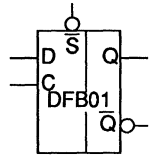
Logic Schematic



Description:

DFB01 is a static, master-slave D flip-flop. Set is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock. Equivalent to DF101 with transmission gates.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
C	0.21
SN	0.14

Equivalent Gates: 7

Bolt Syntax: .....Q QN .DFB01 C D SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	67.4	nA
†C_{pd}	2.33	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

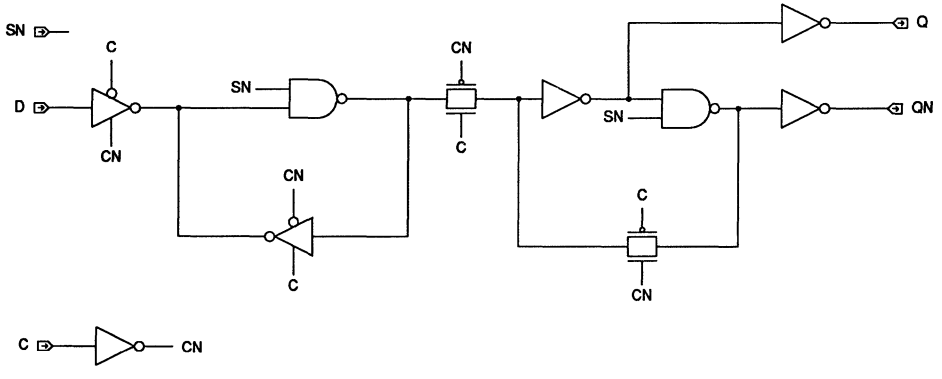
Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	1.09	1.14	1.27	1.46	1.85
		t_{PHL}	1.07	0.71	1.18	1.30	1.54
C	Q	t_{PLH}	0.77	1.12	0.95	1.14	1.51
		t_{PHL}	0.67	0.72	0.78	0.90	1.14
SN	Q	t_{PLH}	1.12	1.12	1.30	1.49	1.87
SN	QN	t_{PHL}	0.71	0.71	0.82	0.95	1.18
Min C Width	High	t_w	0.96				
Min C Width	Low	t_w	1.05				
Min SN Width		t_w	0.93				
Min D Setup		t_{su}	1.05				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.29				
Min SN Hold		t_h	0.21				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

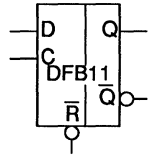
Logic Schematic



Description:

DFB11 is a static master-slave D flip-flop. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock. Equivalent to DF111 with transmission gates.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
C	0.21
RN	0.14

Equivalent Gates: 7

Bolt Syntax: .....Q QN .DFB11 C D RN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	67.4	nA
†C_{pd}	2.40	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

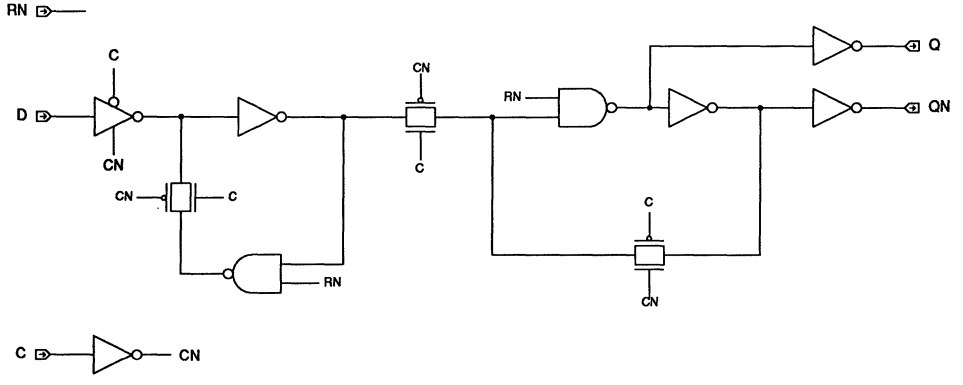
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	0.94	1.11	1.11	1.30	1.68
		t_{PHL}	1.17	0.68	1.28	1.40	1.63
C	Q	t_{PLH}	0.90	1.15	1.08	1.28	1.66
		t_{PHL}	0.64	0.73	0.76	0.88	1.13
RN	Q	t_{PHL}	0.50	0.73	0.62	0.74	0.99
RN	QN	t_{PLH}	0.97	1.11	1.14	1.34	1.71
Min C Width	High	t_w	1.06				
Min C Width	Low	t_w	0.96				
Min RN Width		t_w	0.61				
Min D Setup		t_{su}	0.96				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.20				
Min RN Hold		t_h	0.36				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

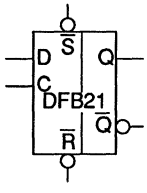
Logic Schematic



Description:

DFB21 is a static, master-slave, D flip-flop, SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock. Equivalent to DF121 with transmission gates.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

NC = No Change
IL = Illegal

Pin Loading

	Ci (pF)
D	0.07
C	0.21
SN	0.14
RN	0.14

Equivalent Gates: 8
Bolt Syntax: .....Q QN .DFB21 C D RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	67.4	nA
†C_{pd}	2.61	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

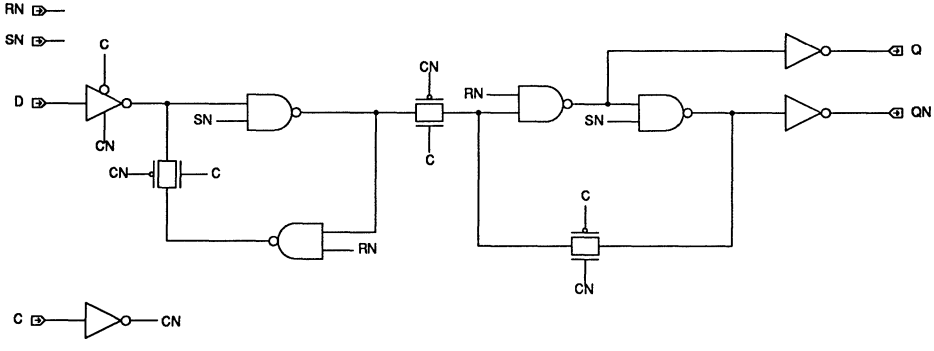
Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	1.05	1.14	1.24	1.43	1.81
		t_{PHL}	1.16	0.70	1.27	1.39	1.63
C	Q	t_{PLH}	0.89	1.15	1.08	1.28	1.66
		t_{PHL}	0.68	0.73	0.79	0.92	1.16
SN	Q	t_{PLH}	1.20	1.15	1.39	1.58	1.97
SN	QN	t_{PHL}	0.67	0.70	0.78	0.90	1.14
RN	Q	t_{PHL}	0.49	0.73	0.61	0.73	0.98
RN	QN	t_{PLH}	1.10	1.14	1.29	1.48	1.86
Min C Width	High	t_w	1.06				
Min C Width	Low	t_w	1.15				
Min RN Width		t_w	1.16				
Min SN Width		t_w	1.07				
Min D Setup		t_{su}	1.29				
Min D Hold		t_h	0.19				
Min RN Setup		t_{su}	0.21				
Min RN Hold		t_h	0.37				
Min SN Setup		t_{su}	0.56				
Min SN Hold		t_h	0.17				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

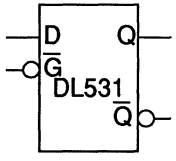
Logic Schematic



Description:

DL531 is a single phase D latch with active low gate transparency without set or reset.

Logic Symbol



Truth Table

GN	D	Q	QN
L	L	L	H
L	H	H	L
H	X	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.06
GN	0.15

Equivalent Gates: 3
Bolt Syntax: .....Q QN .DL531 D GN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} T_J = 85°C	33.8	nA
†C_{pd}	0.89	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

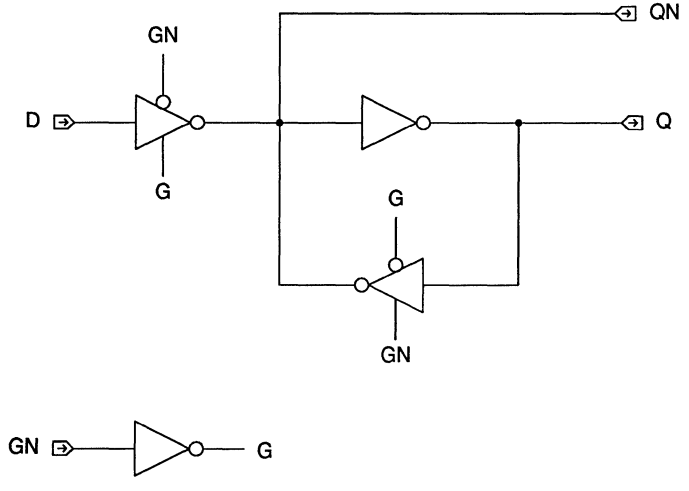
Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
D	Q	t_{PLH}	0.61	1.14	0.80	0.99	1.38
		t_{PHL}	0.88	0.92	1.03	1.19	1.50
D	QN	t_{PLH}	0.71	2.08	1.05	1.41	2.10
		t_{PHL}	0.29	0.80	0.42	0.56	0.83
GN	Q	t_{PLH}	0.78	1.14	0.97	1.16	1.55
		t_{PHL}	0.69	0.92	0.83	0.99	1.30
GN	QN	t_{PLH}	0.52	2.08	0.85	1.21	1.91
		t_{PHL}	0.46	0.80	0.59	0.72	0.99
Min GN Width	Low	t_w				0.88	
Min D Setup		t_{su}				0.88	
Min D Hold		t_h	0.00				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

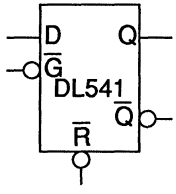
Logic Schematic



Description:

DL541 is a single phase D latch with active low gate transparency, with active low reset (unbuffered).

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
GN	0.14
RN	0.07

Equivalent Gates: 5
Bolt Syntax: ..... Q QN .DL541 D GN RN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	59.0	nA
†C_{pd}	1.27	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

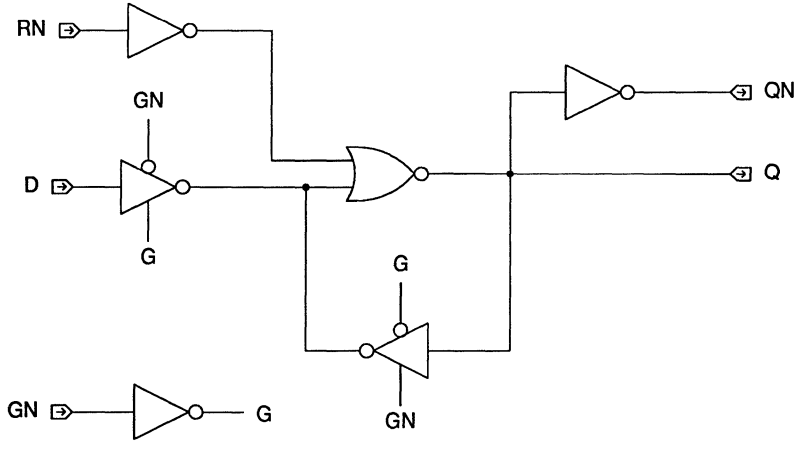
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
D	Q	t_{PLH}	0.88	2.08	1.21	1.57	2.27
		t_{PHL}	0.94	0.76	1.06	1.20	1.45
D	QN	t_{PLH}	1.16	1.11	1.34	1.53	1.90
		t_{PHL}	0.96	0.98	1.12	1.29	1.62
GN	Q	t_{PLH}	1.05	2.08	1.38	1.74	2.43
		t_{PHL}	0.75	0.76	0.87	1.00	1.26
GN	QN	t_{PLH}	0.97	1.11	1.15	1.34	1.71
		t_{PHL}	1.13	0.98	1.28	1.45	1.78
RN	Q	t_{PHL}	0.43	0.76	0.55	0.68	0.94
RN	QN	t_{PLH}	0.63	1.11	0.80	0.99	1.36
Min GN Width	Low	t_w				1.05	
Min RN Width	Low	t_w				1.15	
Min D Setup		t_{su}				0.94	
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.77				
Min RN Hold		t_h	0.65				

For Q Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{dr}(QN) + (k_{tdr}(QN) \cdot C_L(QN)) + (k_{tdf}(Q) \cdot C_L(Q))]$

$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{df}(QN) + (k_{tdf}(QN) \cdot C_L(QN)) + (k_{tdr}(Q) \cdot C_L(Q))]$

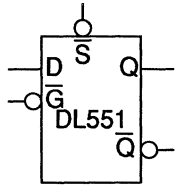
Logic Schematic



Description:

DL551 is a single phase D latch with active low gate transparency, with active low set (unbuffered).

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
GN	0.15
SN	0.07

Equivalent Gates: 4

Bolt Syntax: .....Q QN .DL551 D GN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	42.2	nA
†C_{pd}	1.12	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

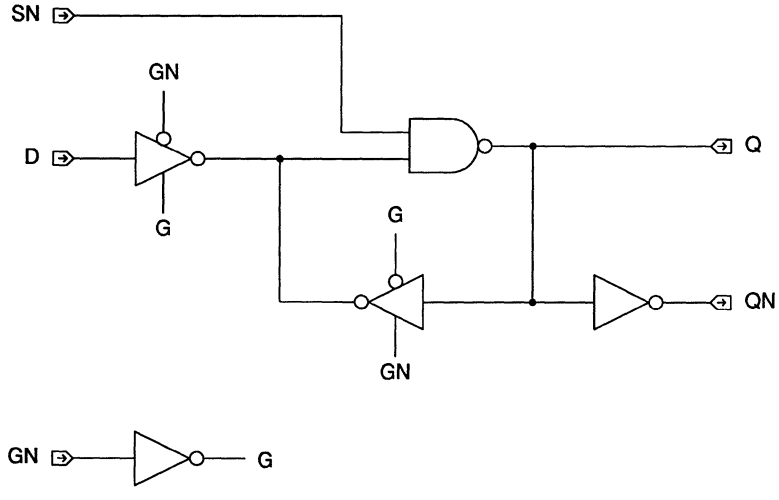
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
D	Q	t_{PLH}	0.67	1.14	0.85	1.05	1.43
		t_{PHL}	1.02	0.95	1.17	1.33	1.65
D	QN	t_{PLH}	1.27	1.17	1.46	1.66	2.05
		t_{PHL}	0.77	0.77	0.89	1.02	1.28
GN	Q	t_{PLH}	0.83	1.14	1.01	1.21	1.59
		t_{PHL}	0.82	0.95	0.97	1.14	1.45
GN	QN	t_{PLH}	1.07	1.17	1.26	1.46	1.85
		t_{PHL}	0.93	0.77	1.05	1.18	1.44
SN	Q	t_{PLH}	0.38	1.14	0.57	0.76	1.15
SN	QN	t_{PHL}	0.49	0.77	0.61	0.74	1.00
Min GN Width	Low	t_w				1.02	
Min SN Width	Low	t_w				0.71	
Min D Setup		t_{su}				1.02	
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.25				
Min SN Hold		t_h	0.35				

For Q Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{dr}(QN) + (k_{tdr}(QN) \cdot C_L(QN)) + (k_{tdf}(Q) \cdot C_L(Q))]$

$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{df}(QN) + (k_{tdf}(QN) \cdot C_L(QN)) + (k_{tdr}(Q) \cdot C_L(Q))]$

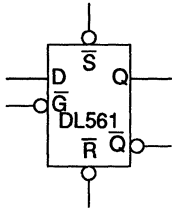
Logic Schematic



Description:

DL561 is a single phase D latch with active low gate transparency, with active low set (unbuffered).

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

NC = No Change
IL = Illegal

Pin Loading

	Ci (pF)
D	0.07
GN	0.14
SN	0.07
RN	0.06

Equivalent Gates: 5
Bolt Syntax: .....Q QN .DL561 D GN SN RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	33.8	nA
†C_{pd}	1.33	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

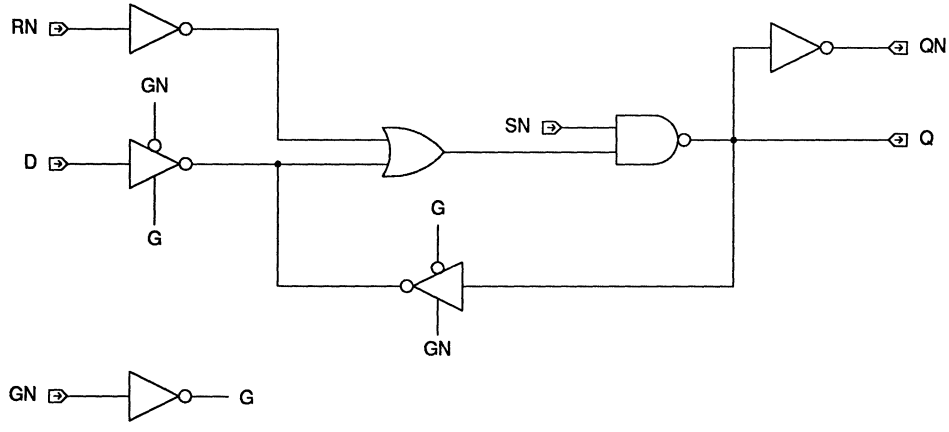
Max Delay (ns)		Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
From	To						
D	Q	t_{PLH}	0.84	1.17	1.03	1.23	1.62
		t_{PHL}	1.10	0.98	1.26	1.43	1.75
D	QN	t_{PLH}	1.68	1.25	1.88	2.10	2.51
		t_{PHL}	1.23	0.96	1.38	1.54	1.87
GN	Q	t_{PLH}	0.97	1.17	1.16	1.36	1.75
		t_{PHL}	0.90	0.98	1.06	1.23	1.55
GN	QN	t_{PLH}	1.15	1.25	1.35	1.57	1.99
		t_{PHL}	1.05	0.96	1.21	1.37	1.69
SN	Q	t_{PLH}	0.38	1.17	0.57	0.77	1.16
SN	QN	t_{PHL}	0.47	0.96	0.62	0.79	1.11
RN	Q	t_{PHL}	0.92	0.98	1.07	1.24	1.57
RN	QN	t_{PLH}	1.14	1.25	1.34	1.56	1.98
Min GN Width	Low	t_w				1.10	
Min RN Width	Low	t_w				0.92	
Min SN Width	Low	t_w				0.84	
Min D Setup		t_{su}				1.10	
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.25				
Min SN Hold		t_h	0.41				
Min RN Setup		t_{su}	0.92				
Min RN Hold		t_h	0.21				

For Q Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{dr}(QN) + (k_{tdr}(QN) \cdot C_L(QN)) + (k_{tdf}(Q) \cdot C_L(Q))]$

$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{df}(QN) + (k_{tdf}(QN) \cdot C_L(QN)) + (k_{tdr}(Q) \cdot C_L(Q))]$

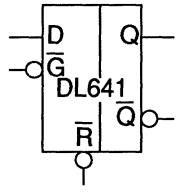
Logic Schematic



Description:

DL641 is a single phase D latch with active low gate transparency, with active low reset. Outputs are buffered.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
GN	0.14
RN	0.07

Equivalent Gates: 6
Bolt Syntax: .....Q QN .DL641 D GN RN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	75.8	nA
†C_{pd}	1.56	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

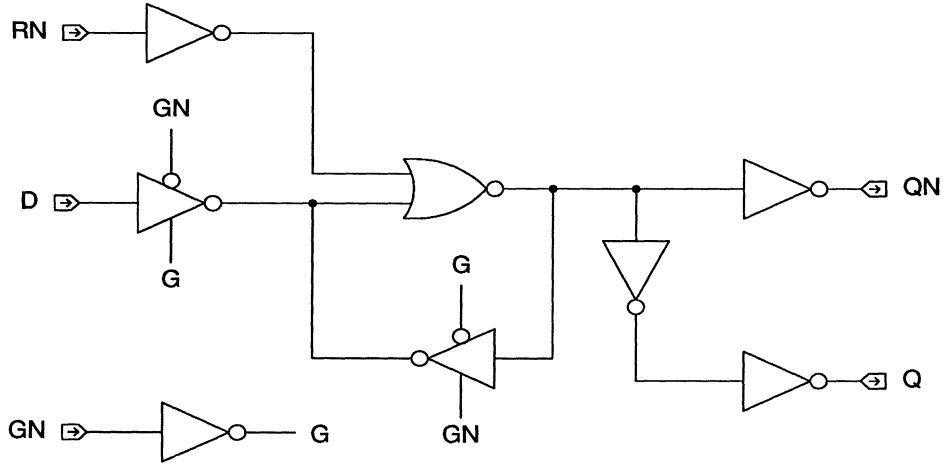
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
D	Q	t_{PLH}	1.37	1.11	1.55	1.74	2.11
		t_{PHL}	1.40	0.62	1.50	1.60	1.81
D	QN	t_{PLH}	1.21	1.12	1.39	1.59	1.96
		t_{PHL}	1.12	1.02	1.29	1.46	1.80
GN	Q	t_{PLH}	1.54	1.11	1.72	1.91	2.29
		t_{PHL}	1.20	0.62	1.30	1.41	1.62
GN	QN	t_{PLH}	1.02	1.12	1.20	1.39	1.77
		t_{PHL}	1.29	1.02	1.45	1.62	1.97
RN	Q	t_{PHL}	0.86	0.62	0.96	1.07	1.27
RN	QN	t_{PLH}	0.68	1.12	0.85	1.05	1.42
Min GN Width	High	t_w	0.33				
Min GN Width	Low	t_h	1.21				
Min RN Width	Low	t_w	1.21				
Min D Setup		t_{su}	1.05				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.94				
Min RN Hold		t_h	0.65				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

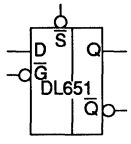
Logic Schematic



Description:

DL651 is a single phase D latch with active low gate transparency, with active low set. Outputs are buffered.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
GN	0.15
SN	0.07

Equivalent Gates: 5

Bolt Syntax: .....Q QN .DL651 D GN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	59.0	nA
†C_{pd}	1.42	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

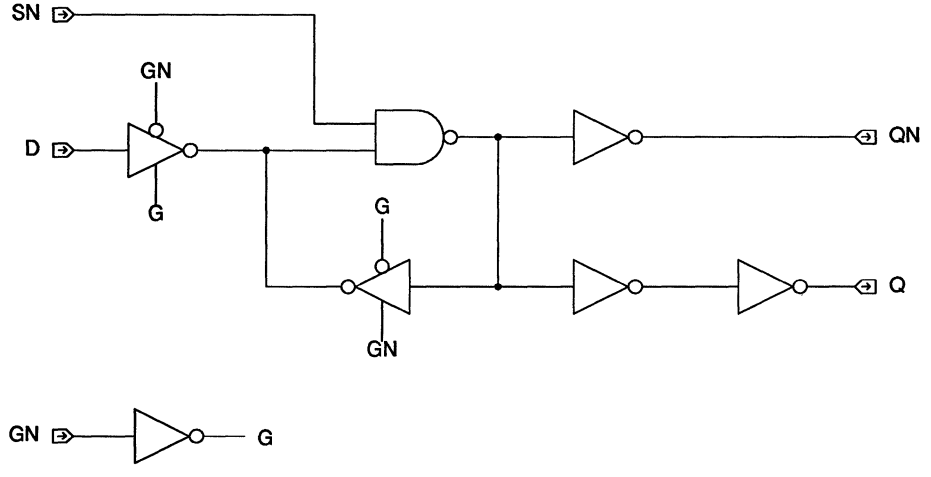
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
D	Q	t_{PLH}	1.07	1.11	1.25	1.44	1.82
		t_{PHL}	1.53	0.63	1.63	1.74	1.95
D	QN	t_{PLH}	1.34	1.17	1.53	1.73	2.12
		t_{PHL}	0.86	0.79	0.99	1.12	1.39
GN	Q	t_{PLH}	1.24	1.11	1.41	1.61	1.98
		t_{PHL}	1.33	0.63	1.43	1.54	1.76
GN	QN	t_{PLH}	1.14	1.17	1.33	1.53	1.93
		t_{PHL}	1.02	0.79	1.14	1.28	1.55
SN	Q	t_{PLH}	0.80	1.11	0.97	1.17	1.54
SN	QN	t_{PHL}	0.58	0.79	0.70	0.84	1.10
Min GN Width	High	t_w	0.30				
Min GN Width	Low	t_h	1.09				
Min SN Width	Low	t_w	0.81				
Min D Setup		t_{su}	1.09				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.32				
Min SN Hold		t_h	0.19				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

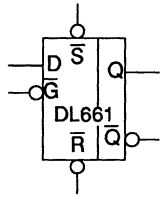
Logic Schematic



Description:

DL661 is a single phase buffered D latch with active low gate transparency, with active low set and reset.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL = Illegal
NC = No Change

Pin Loading

	Ci (pF)
D	0.07
GN	0.14
SN	0.07
RN	0.07

Equivalent Gates: 6
Bolt Syntax: .....Q QN .DL661 D GN RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	50.6	nA
†C_{pd}	1.63	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

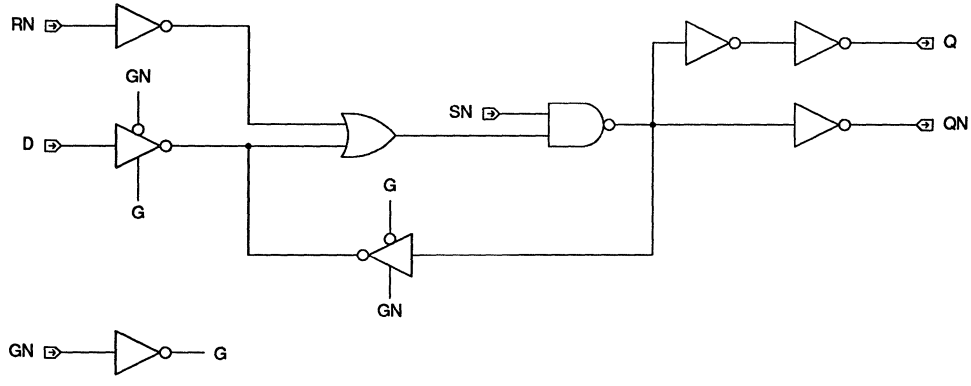
Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
D	Q	t_{PLH}	1.27	1.11	1.45	1.64	2.01
		t_{PHL}	1.63	0.63	1.73	1.84	2.05
D	QN	t_{PLH}	1.44	1.17	1.63	1.83	2.22
		t_{PHL}	1.05	0.80	1.18	1.31	1.58
GN	Q	t_{PLH}	1.39	1.11	1.57	1.76	2.13
		t_{PHL}	1.43	0.63	1.53	1.64	1.85
GN	QN	t_{PLH}	1.24	1.17	1.43	1.63	2.02
		t_{PHL}	1.17	0.80	1.29	1.43	1.70
SN	Q	t_{PLH}	0.81	1.11	0.99	1.18	1.55
SN	QN	t_{PHL}	0.58	0.80	0.71	0.85	1.12
RN	Q	t_{PHL}	1.44	0.63	1.54	1.65	1.86
RN	QN	t_{PLH}	1.24	1.17	1.43	1.63	2.03
Min GN Width	High	t_w	0.30				
Min GN Width	Low	t_h	1.18				
Min RN Width	Low	t_w	0.99				
Min SN Width	Low	t_w	0.94				
Min D Setup		t_{su}	1.18				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.32				
Min SN Hold		t_h	0.25				
Min RN Setup		t_{su}	1.02				
Min RN Hold		t_h	0.21				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

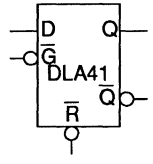
Logic Schematic



Description:

DLA41 is a single phase D latch with active low gate transparency, with active low reset (unbuffered). Equivalent to DL541 with transmission gates.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
GN	0.14
RN	0.07

Equivalent Gates: 4
Bolt Syntax: ..... Q QN .DLA41 D GN RN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	50.6	nA
†C_{pd}	1.29	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
D	Q	t_{PLH}	0.72	2.08	1.05	1.41	2.11
		t_{PHL}	0.87	0.83	1.00	1.15	1.42
D	QN	t_{PLH}	1.09	1.10	1.26	1.45	1.82
		t_{PHL}	0.83	0.87	0.97	1.12	1.41
GN	Q	t_{PLH}	0.88	2.08	1.21	1.57	2.27
		t_{PHL}	0.68	0.83	0.81	0.95	1.23
GN	QN	t_{PLH}	0.89	1.10	1.07	1.26	1.63
		t_{PHL}	0.99	0.87	1.13	1.28	1.57
RN	Q	t_{PHL}	0.38	0.83	0.51	0.65	0.93
RN	QN	t_{PLH}	0.57	1.10	0.75	0.94	1.31
Min GN Width	Low	t_w				1.57	
Min RN Width	Low	t_w				1.25	
Min D Setup		t_{su}				1.41	
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.60				
Min RN Hold		t_h	0.35				

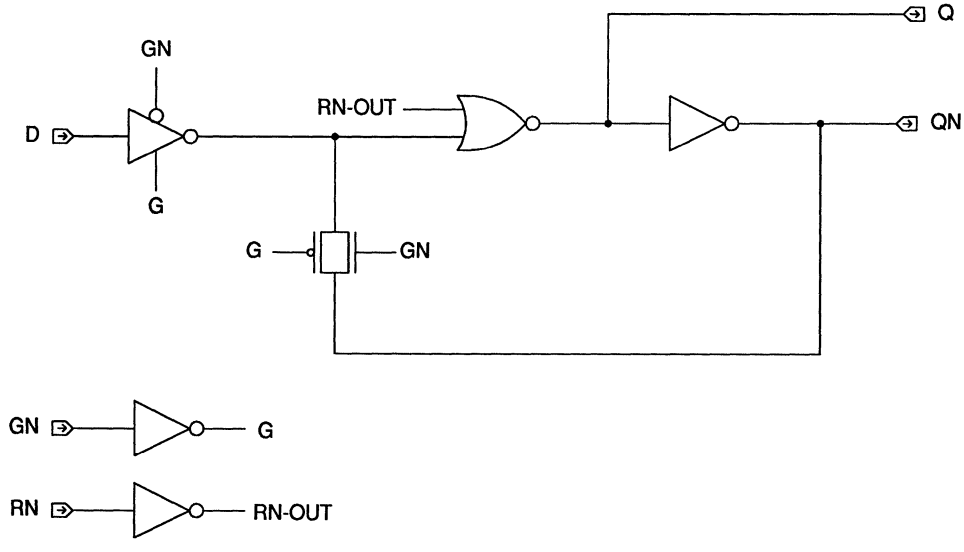
For Q Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{dr}(QN) + (k_{tdr}(QN) \cdot C_L(QN)) + (k_{tdf}(Q) \cdot C_L(Q))]$

$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_{PV}K_T[t_{df}(QN) + (k_{tdf}(QN) \cdot C_L(QN)) + (k_{tdr}(Q) \cdot C_L(Q))]$

ASIC Functions

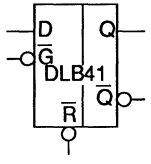
Logic Schematic



Description:

DLB41 is a single phase D latch with active low gate transparency, with active low reset. Outputs are buffered. Equivalent to DL641 with transmission gates.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

Pin Loading

	Ci (pF)
D	0.07
GN	0.15
RN	0.07

Equivalent Gates: 5
Bolt Syntax: ..... Q QN .DLB41 D GN RN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	67.4	nA
†C_{pd}	1.68	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

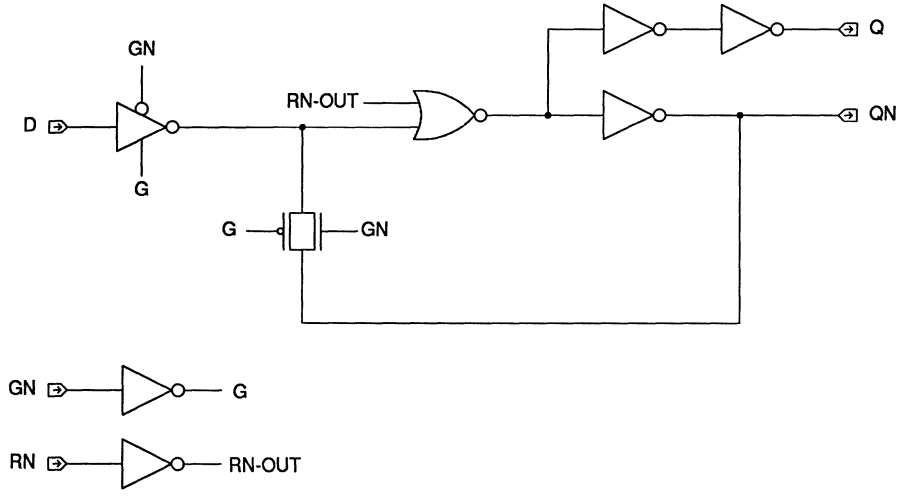
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
D	Q	t_{PLH}	1.22	1.11	1.40	1.59	1.96
		t_{PHL}	1.31	0.61	1.41	1.51	1.72
D	QN	t_{PLH}	1.14	1.12	1.32	1.51	1.89
		t_{PHL}	1.00	0.90	1.14	1.30	1.60
GN	Q	t_{PLH}	1.38	1.11	1.56	1.75	2.13
		t_{PHL}	1.12	0.61	1.22	1.32	1.53
GN	QN	t_{PLH}	0.95	1.12	1.13	1.32	1.69
		t_{PHL}	1.16	0.90	1.30	1.46	1.76
RN	Q	t_{PHL}	0.80	0.61	0.90	1.00	1.21
RN	QN	t_{PLH}	0.63	1.12	0.81	1.00	1.37
Min GN Width	High	t_w	0.33				
Min GN Width	Low	t_h	1.05				
Min RN Width	Low	t_w	0.95				
Min D Setup		t_{su}	0.93				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.78				
Min RN Hold		t_h	0.35				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

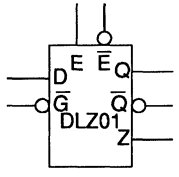
Logic Schematic



Description:

DLZ01 is a single phase D latch with active low gate transparency. Includes a dual-enable tri-state output.

Logic Symbol



Truth Table

D	GN	E	EN	Q	QN	Z
L	L	X	L	L	H	L
H	L	H	X	H	L	H
L	L	L	X	L	H	Z
H	L	X	H	H	L	Z
X	H	H	L	NC	NC	NC
X	H	L	H	NC	NC	Z

NC = No Change
Z = Hi Impedance

Pin Loading

	Ci (pF)
D	0.06
GN	0.15
E	0.03
EN	0.03
Z	0.07

Equivalent Gates: 4
Bolt Syntax: ..... Q QN Z .DLZ01 D GN E EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	42.2	nA
†C_{pd}	1.17	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

ASIC Functions

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
D	Q	t_{PLH}	0.71	1.15	0.89	1.09	1.47
		t_{PHL}	1.02	1.00	1.18	1.35	1.69
D	QN	t_{PLH}	0.87	2.08	1.20	1.56	2.25
		t_{PHL}	0.35	0.79	0.48	0.61	0.88
D	Z	t_{PLH}	0.83	2.07	1.16	1.52	2.21
		t_{PHL}	1.02	1.14	1.20	1.40	1.78
GN	Q	t_{PLH}	0.87	1.15	1.05	1.25	1.63
		t_{PHL}	0.83	1.00	0.99	1.16	1.49
GN	QN	t_{PLH}	0.67	2.08	1.00	1.36	2.06
		t_{PHL}	0.51	0.79	0.63	0.77	1.04
GN	Z	t_{PLH}	0.99	2.07	1.32	1.67	2.37
		t_{PHL}	0.82	1.14	1.01	1.20	1.58
E	Z	t_{PLZ}	0.11				
		t_{PZL}	0.11				
EN	Z	t_{PHZ}	0.14				
		t_{PZH}	0.18				
Min GN Width	Low	t_w				1.02	
Min D Setup		t_{su}				1.02	
Min D Hold		t_h	0.00				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) \cdot C_L(Q)) + (k_{tdf}(QN) \cdot C_L(QN))]$

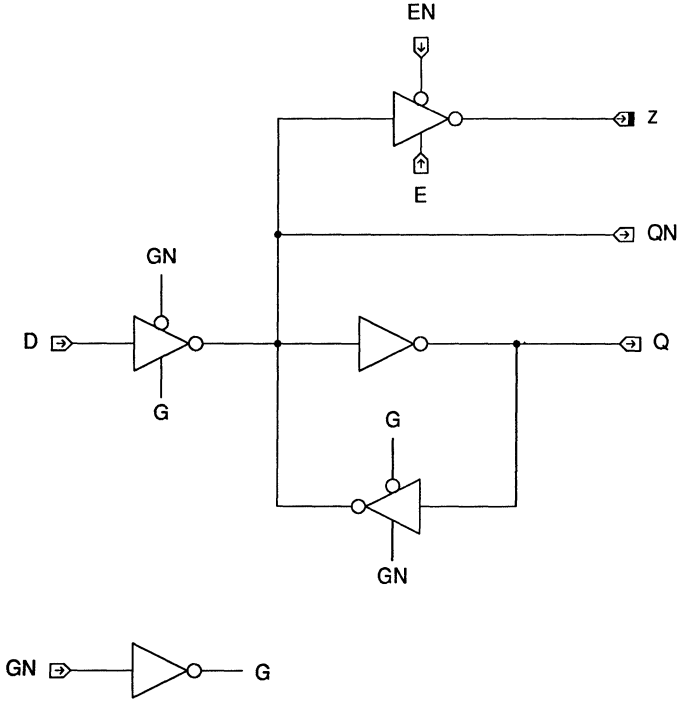
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) \cdot C_L(Q)) + (k_{tdr}(QN) \cdot C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

For Z Delays: $t_{plh}(C_{L(Z)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Z) + (K_{tdr}(Z) \cdot C_L(Z)) + (K_{tdf}(QN) \cdot C_L(QN))]$

$t_{phl}(C_{L(Z)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Z) + (K_{tdf}(Z) \cdot C_L(Z)) + (K_{tdr}(QN) \cdot C_L(QN))]$

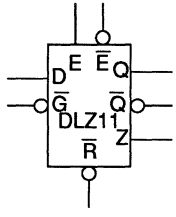
Logic Schematic



Description:

DLZ11 is a single phase D latch with active low gate transparency and reset. Includes a dual-enable tri-state output.

Logic Symbol



Truth Table

RN	D	GN	E	EN	Q	QN	Z
H	L	L	X	L	L	H	L
H	H	L	H	X	H	L	H
H	L	L	L	X	L	H	Z
H	H	L	X	H	H	L	Z
H	X	H	H	L	NC	NC	NC
H	X	H	L	H	NC	NC	Z
L	X	X	H	L	L	H	L
L	X	X	L	H	L	H	Z

NC = No Change
Z = Hi Impedance

Pin Loading

	Ci (pF)
D	0.07
GN	0.15
RN	0.06
E	0.03
EN	0.03
Z	0.07

Equivalent Gates: 5
Bolt Syntax: ..... Q QN Z .DLZ11 D GN RN E EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	33.8	nA
†C_{pd}	1.38	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
D	Q	t_{PLH}	0.92	1.22	1.11	1.32	1.73
		t_{PHL}	1.09	1.02	1.26	1.43	1.77
D	QN	t_{PLH}	0.94	2.08	1.27	1.63	2.33
		t_{PHL}	0.49	1.03	0.65	0.83	1.17
GN	Q	t_{PLH}	1.03	1.22	1.22	1.43	1.84
		t_{PHL}	0.89	1.02	1.06	1.23	1.57
GN	QN	t_{PLH}	0.74	2.08	1.07	1.43	2.12
		t_{PHL}	0.59	1.03	0.76	0.94	1.28
RN	Q	t_{PHL}	0.79	1.02	0.95	1.13	1.47
RN	QN	t_{PLH}	0.62	2.08	0.95	1.31	2.01
RN	Z	t_{PHL}	0.78	1.17	0.96	1.16	1.55
		t_{PLH}	1.09	2.07	1.42	1.78	2.47
D	Z	t_{PLH}	1.02	2.07	1.35	1.71	2.40
		t_{PHL}	1.08	1.17	1.27	1.47	1.86
GN	Z	t_{PLH}	1.13	2.07	1.46	1.82	2.51
		t_{PHL}	0.89	1.17	1.07	1.27	1.66
E	Z	t_{PLZ}	0.10				
		t_{PZL}	0.11				
EN	Z	t_{PHZ}	0.14				
		t_{PZH}	0.17				
Min GN Width	Low	t_w				1.09	
Min RN Width	Low	t_w				0.79	
Min D Setup		t_{su}				1.09	
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.98				
Min RN Hold		t_h	0.21				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) \cdot C_L(Q)) + (k_{tdf}(QN) \cdot C_L(QN))]$

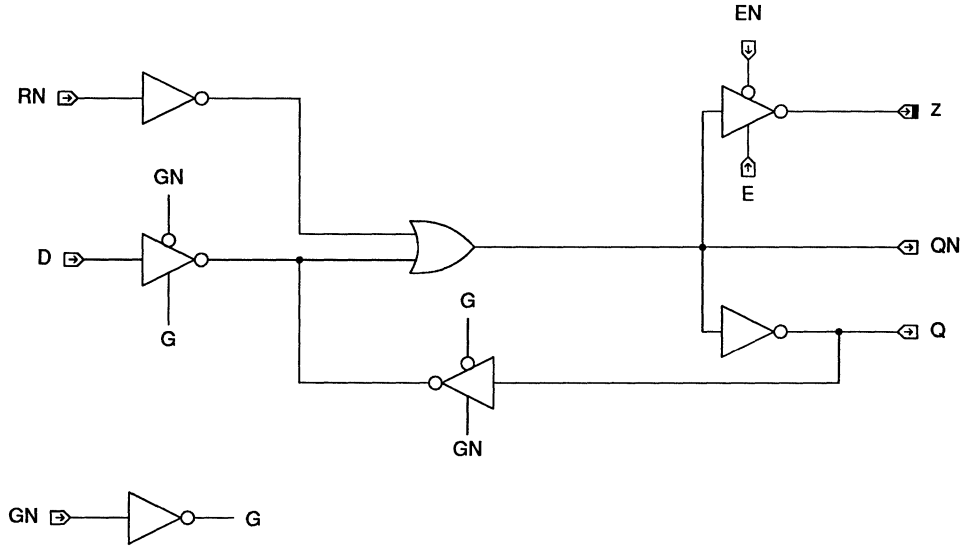
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) \cdot C_L(Q)) + (k_{tdr}(QN) \cdot C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

For Z Delays: $t_{plh}(C_{L(Z)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Z) + (K_{tdr}(Z) \cdot C_L(Z)) + (K_{tdf}(QN) \cdot C_L(QN))]$

$t_{phl}(C_{L(Z)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Z) + (K_{tdf}(Z) \cdot C_L(Z)) + (K_{tdr}(QN) \cdot C_L(QN))]$

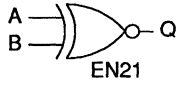
Logic Schematic



Description:

EN21 is a 2-input gate, which performs the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

Pin Loading

	Ci (pF)
A	0.14
B	0.14

Equivalent Gates: 3
Bolt Syntax: .....Q .EN21 A B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	16.9	nA
†C_{pd}	0.64	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

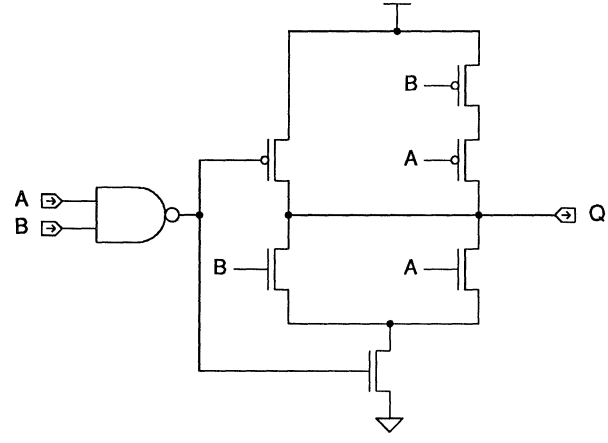
Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

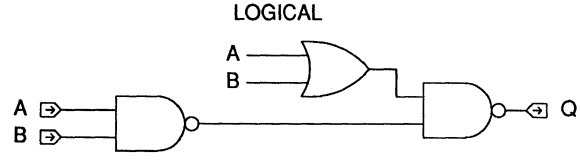
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.36	2.10	0.70	1.06	1.76
		t_{PHL}	0.46	0.80	0.59	0.72	0.99

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Logic Schematic





Description:

EO21 is a 2-input gate, which performs the logical exclusive OR (XOR) function.

Logic Symbol

Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

Pin Loading

	Ci (pF)
A	0.14
B	0.14

Equivalent Gates: 3
Bolt Syntax: .....Q .EO21 A B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	33.8	nA
†C_{pd}	0.65	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

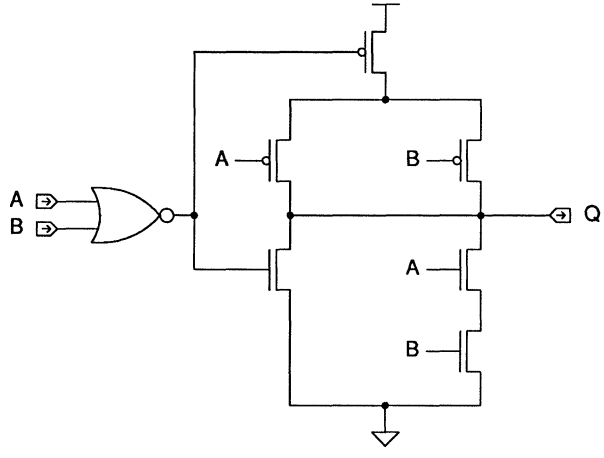
Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.60	2.01	0.92	1.27	1.94
		t_{PHL}	0.60	0.66	0.70	0.82	1.04

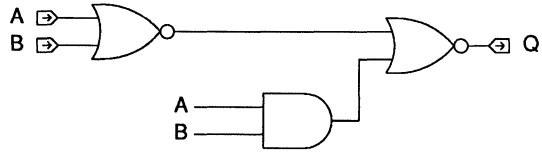
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Logic Schematic



LOGICAL



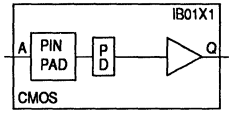
April, 1992

IB01X1

Description:

IB01X1 is a non-inverting CMOS-level input pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	2.97

Equivalent Gates: 0
Bolt Syntax: .....Q .IB01X1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	16.1	nA
†C_{pd}	0.33	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

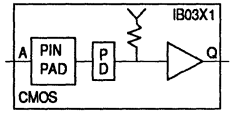
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
A	Q	t_{PLH}	0.73	0.80	0.85	0.99	1.26
		t_{PHL}	0.57	0.64	0.67	0.78	1.00

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IB03X1 is a non-inverting CMOS-level input buffer pad with pull up.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	2.97

Equivalent Gates: 0
Bolt Syntax: .....Q .IB03X1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	16.1	nA
†C_{pd}	0.33	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

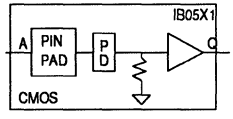
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	Q	t_{PLH}	0.73	0.80	0.85	0.99	1.26
		t_{PHL}	0.57	0.64	0.67	0.78	1.00

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IB05X1 is a non-inverting CMOS-level input buffer pad with pull down.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	3.03

Equivalent Gates: 0
Bolt Syntax: .....Q .IB05X1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	16.1	nA
†C_{pd}	0.33	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

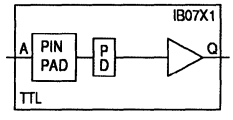
Max Delay (ns)		Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
From	To						
A	Q	t_{PLH}	0.72	0.81	0.85	0.99	1.26
		t_{PHL}	0.56	0.67	0.67	0.78	1.01

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IB07X1 is a non-inverting TTL-level input pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	2.97

Equivalent Gates: 0
Bolt Syntax: .....Q .IB07X1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	24.8	nA
†C_{pd}	0.42	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

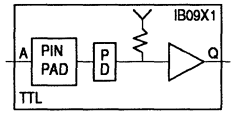
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
A	Q	t_{PLH}	1.05	1.10	1.23	1.42	1.78
		t_{PHL}	0.98	0.84	1.11	1.26	1.54

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IB09X1 is a non-inverting TTL-level input buffer pad with pull up.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	2.97

Equivalent Gates: 0
Bolt Syntax: .....Q .IB09X1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	24.8	nA
†C_{pd}	0.42	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

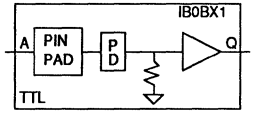
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
A	Q	t_{PLH}	1.05	1.10	1.23	1.42	1.78
		t_{PHL}	0.98	0.84	1.11	1.26	1.54

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IB0BX1 is a non-inverting TTL-level input buffer pad with pull down.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	2.98

Equivalent Gates: 0
Bolt Syntax: .....Q .IB0BX1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	24.8	nA
†C_{pd}	0.42	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

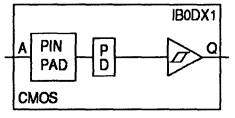
Max Delay (ns)		Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
From	To						
A	Q	t_{PLH}	1.05	1.10	1.23	1.42	1.78
		t_{PHL}	0.98	0.84	1.11	1.26	1.54

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IB0DX1 is a non-inverting CMOS-level Schmitt Trigger input buffer pad with voltage hysteresis.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	3.03

Equivalent Gates: 0
Bolt Syntax: .....Q .IB0DX1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	25.4	nA
†C_{pd}	0.64	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

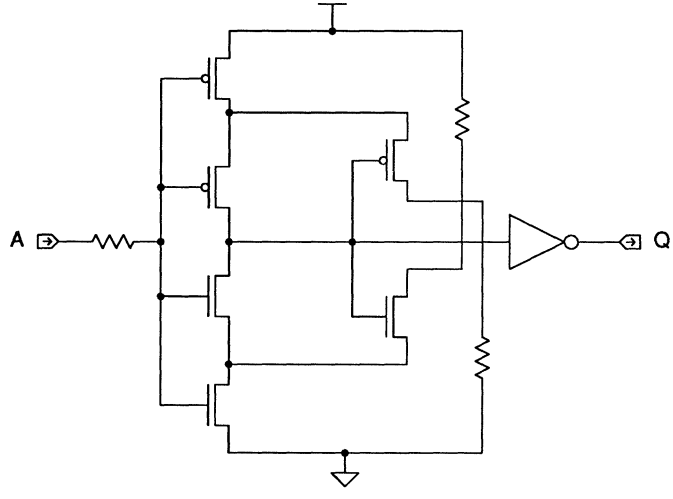
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	Q	t_{PLH}	1.89	0.89	2.03	2.18	2.48
		t_{PHL}	1.69	0.79	1.82	1.95	2.22

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

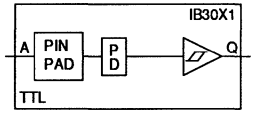
Logic Schematic



Description:

IB30X1 is a non-inverting TTL-level Schmitt Trigger input buffer pad with voltage hysteresis.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	3.09

Equivalent Gates: 0
Bolt Syntax: .....Q .IB30X1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	27.2	nA
†C_{pd}	0.64	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	Q	t_{PLH}	1.70	1.12	1.88	2.08	2.45
		t_{PHL}	2.11	1.07	2.28	2.46	2.82

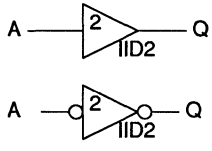
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description:

IID2 is an non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .IID2 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85°C$	25.3	nA
†C_{pd}	0.38	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

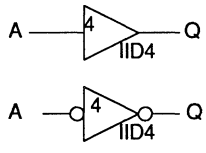
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	Q	t_{PLH}	0.31	0.56	0.40	0.49	0.68
		t_{PHL}	0.37	0.41	0.44	0.51	0.64

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IID4 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.13

Equivalent Gates: 3
Bolt Syntax: .....Q .IID4 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	50.6	nA
†C_{pd}	0.77	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

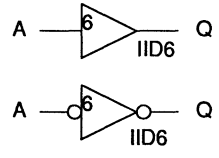
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
A	Q	t_{PLH}	0.30	0.29	0.35	0.40	0.50
		t_{PHL}	0.37	0.23	0.41	0.45	0.52

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IID6 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.13

Equivalent Gates: 4
Bolt Syntax: .....Q .IID6 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	67.4	nA
†C_{pd}	1.02	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

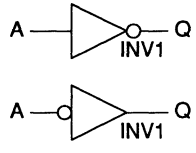
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	Q	t_{PLH}	0.36	0.20	0.39	0.43	0.50
		t_{PHL}	0.45	0.19	0.48	0.51	0.58

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

INV1 is an inverter which performs a logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.07

Equivalent Gates: 1
Bolt Syntax: .....Q .INV1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	8.5	nA
†C_{pd}	0.13	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

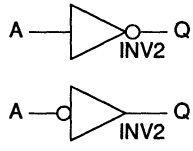
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	Q	t_{PLH}	0.14	1.12	0.32	0.51	0.89
		t_{PHL}	0.09	0.59	0.18	0.28	0.48

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

INV2 is an inverter which performs a logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.13

Equivalent Gates: 1
Bolt Syntax: .....Q .INV2 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	16.9	nA
†C_{pd}	0.26	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

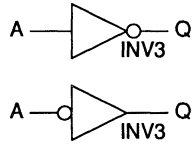
Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	Q	t_{PLH}	0.13	0.57	0.22	0.32	0.51
		t_{PHL}	0.08	0.33	0.13	0.19	0.30

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

INV3 is an inverter which performs a logical NOT function.

Logic Symbol	Truth Table	Pin Loading
	A | Q L | H H | L	Ci (pF) A | 0.20

Equivalent Gates: 2
Bolt Syntax: .....Q .INV3 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	25.3	nA
†C_{pd}	0.38	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns)		Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
From	To						
A	Q	t_{PLH}	0.13	0.38	0.19	0.26	0.38
		t_{PHL}	0.07	0.23	0.11	0.15	0.23

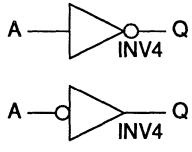
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description:

INV4 is an inverter which performs a logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.27

Equivalent Gates: 2
Bolt Syntax: .....Q .INV4 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	33.8	nA
†C_{pd}	0.51	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

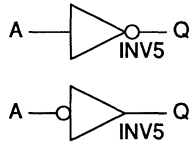
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
A	Q	t_{PLH}	0.13	0.29	0.17	0.22	0.32
		t_{PHL}	0.07	0.19	0.10	0.13	0.20

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

INV5 is an inverter which performs a logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.35

Equivalent Gates: 3
Bolt Syntax: .....Q .INV5 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	42.2	nA
†C_{pd}	0.66	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

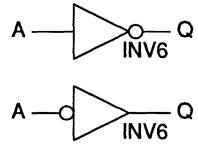
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	Q	t_{PLH}	0.13	0.23	0.17	0.21	0.28
		t_{PHL}	0.07	0.16	0.10	0.12	0.18

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

INV6 is an inverter which performs a logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.40

Equivalent Gates: 3
Bolt Syntax: .....Q .INV6 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	50.6	nA
†C_{pd}	0.77	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

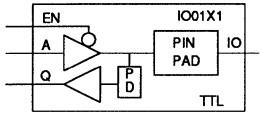
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
A	Q	t_{PLH}	0.13	0.19	0.16	0.19	0.26
		t_{PHL}	0.07	0.13	0.09	0.11	0.16

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IO01X1 is a 1ma non-inverting TTL-bidirectional input/output buffer pad cell with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.30
EN	0.19
IO	5.12

Equivalent Gates: 0

Bolt Syntax: .....IO Q .IO01X1 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	148.6	nA
†C_{pd}	8.17	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.06	1.08	1.24	1.42	1.78
		t_{PHL}	0.94	0.68	1.05	1.17	1.40

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.56	0.28	7.67	14.79	21.90	29.01
		t_{PHL}	0.65	0.29	7.95	15.25	22.55	29.85
EN	IO	t_{HZ}	1.46					
		t_{LZ}	1.12					
		t_{ZH}	0.73	0.28	7.84	14.96	22.07	29.19
		t_{ZL}	0.68	0.29	7.99	15.29	22.59	29.89

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

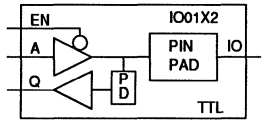
April, 1992

IO01X2

Description:

IO01X2 is a 2ma non-inverting TTL-bidirectional input/output buffer pad cell with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.30
EN	0.19
IO	5.42

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO01X2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	181.6	nA
†C_{pd}	7.08	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.09	1.06	1.26	1.44	1.80
		t_{PHL}	0.92	0.77	1.04	1.18	1.43

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

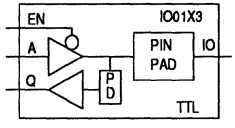
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.27	0.16	4.17	8.07	11.96	15.86
		t_{PHL}	0.41	0.19	5.21	10.01	14.81	19.61
EN	IO	t_{HZ}	1.24					
		t_{LZ}	0.81					
		t_{ZH}	0.50	0.16	4.40	8.30	12.20	16.10
		t_{ZL}	0.47	0.19	5.27	10.07	14.87	19.67

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IO01X3 is a 4ma non-inverting TTL-bidirectional input/output buffer pad cell with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.30
EN	0.22
IO	5.32

Equivalent Gates: 0

Bolt Syntax: .....IO Q .IO01X3 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	185.8	nA
†C_{pd}	7.23	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.06	1.09	1.23	1.42	1.78
		t_{PHL}	0.94	0.69	1.05	1.17	1.40

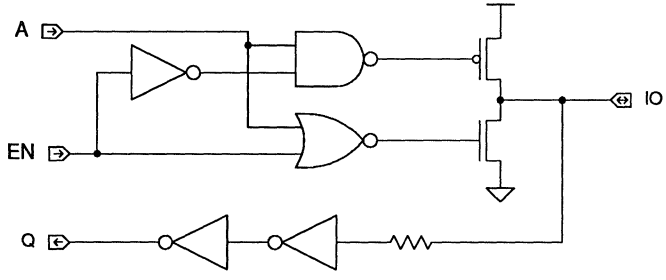
Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.48	0.08	2.42	4.36	6.30	8.24
		t_{PHL}	0.85	0.10	3.25	5.65	8.05	10.46
EN	IO	t_{HZ}	1.27					
		t_{LZ}	1.11					
		t_{ZH}	0.71	0.08	2.65	4.59	6.53	8.47
		t_{ZL}	0.91	0.10	3.31	5.71	8.11	10.52

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

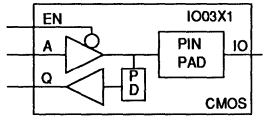
Logic Schematic



Description:

IO03X1 is a 1ma non-inverting CMOS-bidirectional input/output buffer pad cell with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.49
EN	0.31
IO	5.12

Equivalent Gates: 0

Bolt Syntax: .....IO Q .IO03X1 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	139.6	nA
†C_{pd}	7.84	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.72	0.80	0.85	0.98	1.25
		t_{PHL}	0.56	0.65	0.67	0.78	1.00

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

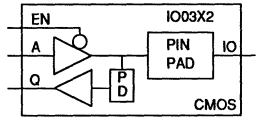
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.25	0.52	13.24	26.23	39.23	52.22
		t_{PHL}	0.77	0.20	5.66	10.55	15.44	20.32
EN	IO	t_{HZ}	1.45					
		t_{LZ}	1.13					
		t_{ZH}	0.46	0.52	13.45	26.44	39.43	52.42
		t_{ZL}	0.81	0.20	5.70	10.59	15.48	20.37

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IO03X2 is a 2ma non-inverting CMOS-bidirectional input/output buffer pad cell with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.49
EN	0.31
IO	5.42

Equivalent Gates: 0

Bolt Syntax: .....IO Q .IO03X2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	172.6	nA
†C_{pd}	6.74	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.72	0.81	0.85	0.99	1.26
		t_{PHL}	0.56	0.65	0.66	0.78	0.99

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

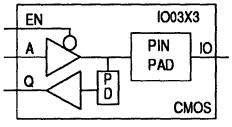
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.05	0.28	7.16	14.26	21.37	28.48
		t_{PHL}	0.48	0.13	3.76	7.04	10.33	13.61
EN	IO	t_{HZ}	1.23					
		t_{LZ}	0.81					
		t_{ZH}	0.31	0.28	7.42	14.53	21.63	28.74
		t_{ZL}	0.54	0.13	3.82	7.11	10.39	13.67

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IO03X3 is a 4ma non-inverting CMOS-bidirectional input/output buffer pad cell with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.49
EN	0.34
IO	5.32

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO03X3 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	176.8	nA
†C_{pd}	6.89	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.72	0.79	0.85	0.98	1.25
		t_{PHL}	0.56	0.64	0.66	0.77	0.99

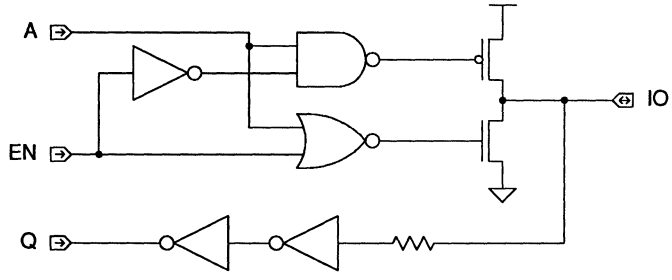
Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.37	0.14	3.91	7.45	10.99	14.53
		t_{PHL}	0.87	0.07	2.52	4.16	5.80	7.45
EN	IO	t_{HZ}	1.24					
		t_{LZ}	1.11					
		t_{ZH}	0.62	0.14	4.16	7.70	11.24	14.78
		t_{ZL}	0.94	0.07	2.58	4.22	5.86	7.51

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

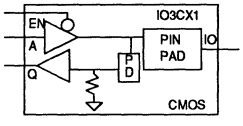
Logic Schematic



Description:

IO03CX1 is a 1ma non-inverting CMOS-bidirectional input/output buffer pad cell with active low enabled tri-state output and a pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.49
EN	0.31
IO	5.12

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO03CX3 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	139.6	nA
†C_{pd}	7.85	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.72	0.81	0.85	0.99	1.26
		t_{PHL}	0.56	0.65	0.67	0.78	1.00

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

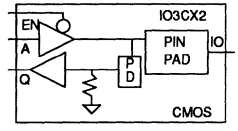
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.27	0.52	13.25	26.24	39.23	52.21
		t_{PHL}	0.78	0.20	5.66	10.55	15.44	20.33
EN	IO	t_{HZ}	1.45					
		t_{LZ}	1.13					
		t_{ZH}	0.47	0.52	13.46	26.45	39.43	52.42
		t_{ZL}	0.82	0.20	5.70	10.59	15.48	20.37

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IO03CX2 is a 2ma non-inverting CMOS-bidirectional input/output buffer pad cell with active low enabled tri-state output and a pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.49
EN	0.31
IO	5.43

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO03CX2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	172.6	nA
†C_{pd}	6.75	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.72	0.81	0.85	0.99	1.26
		t_{PHL}	0.56	0.65	0.66	0.78	0.99

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

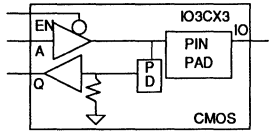
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.05	0.28	7.16	14.26	21.36	28.47
		t_{PHL}	0.48	0.13	3.76	7.05	10.33	13.61
EN	IO	t_{HZ}	1.23					
		t_{LZ}	0.81					
		t_{ZH}	0.32	0.28	7.42	14.53	21.63	28.73
		t_{ZL}	0.54	0.13	3.83	7.11	10.39	13.67

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IO03CX3 is a 4ma non-inverting CMOS-bidirectional input/output buffer pad cell with active low enabled tri-state output and a pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.49
EN	0.34
IO	5.33

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO03CX3 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	176.8	nA
†C_{pd}	6.90	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.72	0.79	0.85	0.98	1.25
		t_{PHL}	0.56	0.64	0.66	0.77	0.99

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

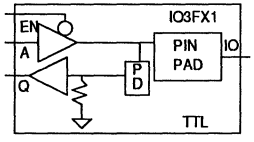
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.37	0.14	3.91	7.45	10.99	14.53
		t_{PHL}	0.87	0.07	2.52	4.16	5.80	7.45
EN	IO	t_{HZ}	1.24					
		t_{LZ}	1.11					
		t_{ZH}	0.62	0.14	4.16	7.70	11.24	14.78
		t_{ZL}	0.93	0.07	2.58	4.22	5.86	7.51

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description:

IO03FX1 is a 1ma non-inverting TTL-bidirectional input/output buffer pad cell with active low enabled tri-state output and a pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.30
EN	0.19
IO	5.12

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO03FX1 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	148.6	nA
†C_{pd}	8.17	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.06	1.09	1.23	1.42	1.79
		t_{PHL}	0.94	0.69	1.05	1.17	1.40

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

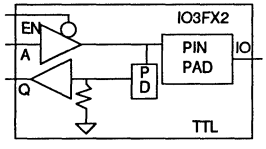
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.55	0.28	7.67	14.78	21.90	29.01
		t_{PHL}	0.64	0.29	7.95	15.25	22.56	29.86
EN	IO	t_{HZ}	1.46					
		t_{LZ}	1.12					
		t_{ZH}	0.72	0.28	7.84	14.95	22.07	29.18
		t_{ZL}	0.68	0.29	7.99	15.29	22.60	29.90

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IO03FX2 is a 2ma non-inverting TTL-bidirectional input/output buffer pad cell with active low enabled tri-state output and a pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.30
EN	0.19
IO	5.43

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO03FX2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	181.6	nA
†C_{pd}	7.08	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.08	1.07	1.26	1.44	1.80
		t_{PHL}	0.92	0.77	1.04	1.17	1.43

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

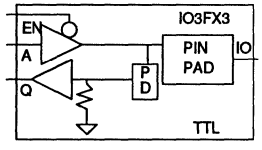
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.27	0.16	4.17	8.07	11.96	15.86
		t_{PHL}	0.40	0.19	5.20	10.01	14.82	19.63
EN	IO	t_{HZ}	1.24					
		t_{LZ}	0.81					
		t_{ZH}	0.50	0.16	4.40	8.30	12.20	16.10
		t_{ZL}	0.46	0.19	5.27	10.08	14.88	19.69

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IO03FX3 is a 4ma non-inverting TTL-bidirectional input/output buffer pad cell with active low enabled tri-state output and a pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.30
EN	0.22
IO	5.32

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO03FX3 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} T_J = 85°C	185.8	nA
†C_{pd}	7.24	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.06	1.09	1.23	1.42	1.78
		t_{PHL}	0.94	0.69	1.05	1.17	1.40

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

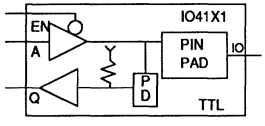
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.48	0.08	2.42	4.36	6.30	8.24
		t_{PHL}	0.85	0.10	3.25	5.65	8.05	10.46
EN	IO	t_{HZ}	1.27					
		t_{LZ}	1.11					
		t_{ZH}	0.71	0.08	2.65	4.59	6.53	8.47
		t_{ZL}	0.91	0.10	3.31	5.71	8.11	10.52

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IO41X1 is a 1ma non-inverting TTL-bidirectional input/output buffer pad cell with an active low enabled tri-state output and a pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.30
EN	0.20
IO	5.12

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO41X1 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	148.6	nA
†C_{pd}	8.16	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.07	1.08	1.24	1.43	1.79
		t_{PHL}	0.94	0.69	1.05	1.17	1.40

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

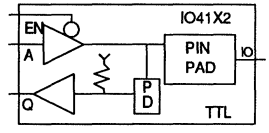
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.56	0.28	7.67	14.79	21.90	29.02
		t_{PHL}	0.64	0.29	7.94	15.25	22.56	29.87
EN	IO	t_{HZ}	1.45					
		t_{LZ}	1.12					
		t_{ZH}	9.00	0.28	16.12	23.23	30.35	37.46
		t_{ZL}	0.68	0.29	7.98	15.29	22.60	29.91

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IO41X2 is a 2ma non-inverting TTL-bidirectional input/output buffer pad cell with an active low enabled tri-state output and a pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.30
EN	0.19
IO	5.42

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO41X2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	181.6	nA
†C_{pd}	7.08	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.08	1.07	1.26	1.44	1.80
		t_{PHL}	0.92	0.77	1.04	1.17	1.43

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

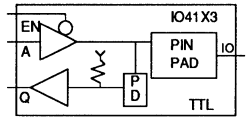
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.27	0.16	4.17	8.07	11.96	15.86
		t_{PHL}	0.40	0.19	5.21	10.01	14.82	19.63
EN	IO	t_{HZ}	1.24					
		t_{LZ}	0.81					
		t_{ZH}	0.50	0.16	4.40	8.30	12.20	16.10
		t_{ZL}	0.46	0.19	5.27	10.08	14.88	19.69

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IO41X3 is a 4ma non-inverting TTL-bidirectional input/output buffer pad cell with an active low enabled tri-state output and a pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.30
EN	0.22
IO	5.32

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO41X3 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	185.8	nA
†C_{pd}	7.21	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.05	1.09	1.23	1.42	1.78
		t_{PHL}	0.94	0.68	1.05	1.17	1.40

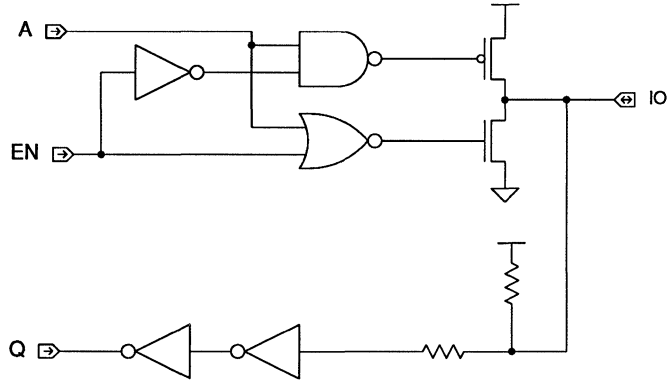
Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.48	0.08	2.42	4.36	6.30	8.24
		t_{PHL}	0.85	0.10	3.25	5.65	8.05	10.46
EN	IO	t_{HZ}	1.25					
		t_{LZ}	1.11					
		t_{ZH}	0.68	0.08	2.62	4.56	6.51	8.45
		t_{ZL}	0.91	0.10	3.31	5.71	8.11	10.52

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

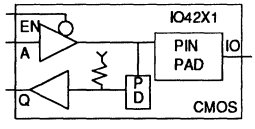
Logic Schematic



Description

IO42X1 is a 1ma non-inverting CMOS-bidirectional input/output buffer with an active low enabled tri-state output and a pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.48
EN	0.31
IO	5.12

Equivalent Gates: 0

Bolt Syntax: .....IO Q .IO42X1 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	139.6	nA
†C_{pd}	7.85	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.73	0.80	0.86	1.00	1.27
		t_{PHL}	0.57	0.65	0.68	0.79	1.01

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

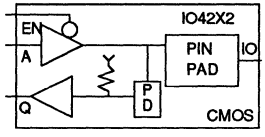
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.24	0.52	13.24	26.23	39.23	52.22
		t_{PHL}	0.77	0.20	5.66	10.55	15.44	20.33
EN	IO	t_{HZ}	1.45					
		t_{LZ}	1.13					
		t_{ZH}	0.44	0.52	13.44	26.43	39.43	52.42
		t_{ZL}	0.82	0.20	5.70	10.59	15.48	20.37

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IO42X2 is a 2ma non-inverting CMOS-bidirectional input/output buffer with an active low enabled tri-state output and a pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.48
EN	0.31
IO	5.42

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO42X2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	172.6	nA
†C_{pd}	6.75	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.73	0.82	0.86	1.00	1.28
		t_{PHL}	0.57	0.66	0.68	0.79	1.01

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

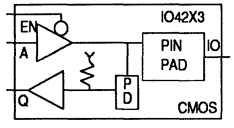
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.05	0.28	7.16	14.27	21.37	28.48
		t_{PHL}	0.48	0.13	3.76	7.04	10.33	13.61
EN	IO	t_{HZ}	1.23					
		t_{LZ}	0.81					
		t_{ZH}	0.31	0.28	7.42	14.53	21.64	28.74
		t_{ZL}	0.54	0.13	3.82	7.11	10.39	13.67

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IO42X3 is a 4ma non-inverting CMOS-bidirectional input/output buffer with an active low enabled tri-state output and a pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.48
EN	0.34
IO	5.32

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO42X3 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	176.8	nA
†C_{pd}	6.90	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.73	0.79	0.86	1.00	1.26
		t_{PHL}	0.57	0.66	0.67	0.79	1.01

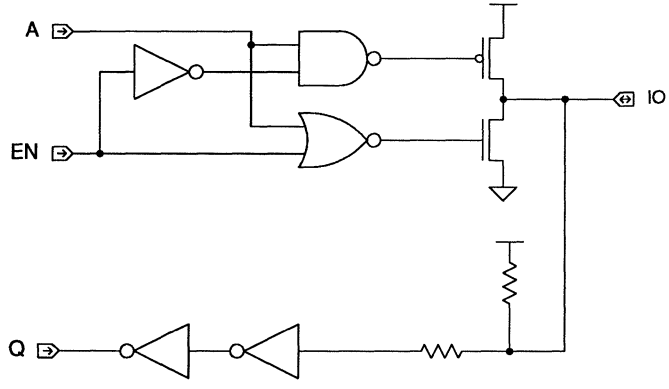
Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.37	0.14	3.91	7.45	10.99	14.53
		t_{PHL}	0.87	0.07	2.52	4.16	5.80	7.45
EN	IO	t_{HZ}	1.24					
		t_{LZ}	1.11					
		t_{ZH}	0.62	0.14	4.16	7.70	11.24	14.78
		t_{ZL}	0.93	0.07	2.58	4.22	5.86	7.51

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

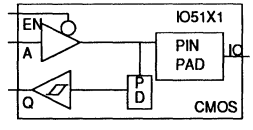
Logic Schematic



Description

IO51X1 is a 1ma non-inverting CMOS-bidirectional input/output buffer with an active low enabled tri-state output and a CMOS Schmitt Trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.46
EN	0.21
IO	5.20

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO51X1 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	158.2	nA
†C_{pd}	8.25	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.97	0.89	2.11	2.26	2.56
		t_{PHL}	1.75	0.81	1.87	2.01	2.28

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

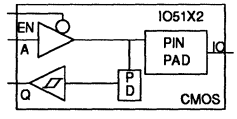
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.27	0.52	13.31	26.36	39.40	52.45
		t_{PHL}	0.86	0.20	5.75	10.64	15.53	20.42
EN	IO	t_{HZ}	1.32					
		t_{LZ}	1.20					
		t_{ZH}	0.47	0.52	13.51	26.56	39.60	52.65
		t_{ZL}	0.90	0.20	5.79	10.68	15.57	20.46

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IO51X2 is a 2ma non-inverting CMOS-bidirectional input/output buffer with an active low enabled tri-state output and a CMOS Schmitt Trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.46
EN	0.21
IO	5.50

Equivalent Gates: 0

Bolt Syntax: .....IO Q .IO51X2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	191.2	nA
$^{\dagger}C_{pd}$	7.15	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.96	0.92	2.10	2.26	2.57
		t_{PHL}	1.76	0.79	1.88	2.02	2.28

Output Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

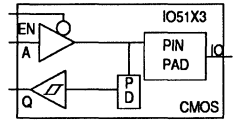
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.10	0.28	7.20	14.31	21.42	28.52
		t_{PHL}	0.56	0.13	3.85	7.13	10.41	13.69
EN	IO	t_{HZ}	1.09					
		t_{LZ}	0.88					
		t_{ZH}	0.36	0.28	7.46	14.57	21.67	28.78
		t_{ZL}	0.62	0.13	3.90	7.18	10.46	13.74

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IO51X3 is a 4ma non-inverting CMOS-bidirectional input/output buffer with an active low enabled tri-state output and a CMOS Schmitt Trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.46
EN	0.23
IO	5.40

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO51X3 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	195.4	nA
†C_{pd}	7.31	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.97	0.90	2.11	2.27	2.57
		t_{PHL}	1.75	0.79	1.88	2.02	2.28

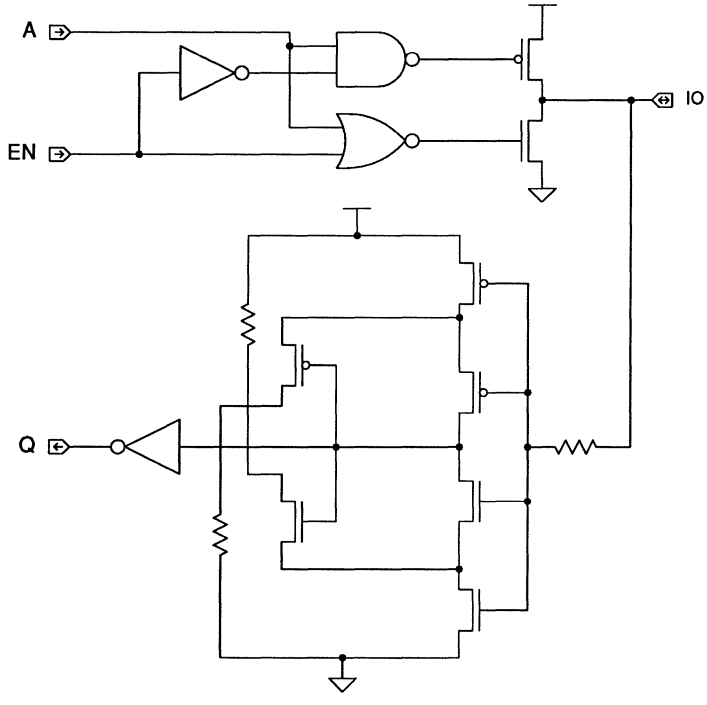
Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.45	0.14	3.99	7.53	11.07	14.62
		t_{PHL}	0.95	0.07	2.60	4.24	5.89	7.53
EN	IO	t_{HZ}	1.13					
		t_{LZ}	1.17					
		t_{ZH}	0.69	0.14	4.23	7.78	11.32	14.86
		t_{ZL}	1.02	0.07	2.66	4.31	5.95	7.59

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

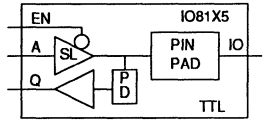
Logic Schematic



Description

IO81X5 is a 8ma non-inverting TTL-bidirectional input/output buffer with an active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.49
EN	0.38
IO	5.64

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO81X5 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	202.7	nA
†C_{pd}	8.78	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.03	1.10	1.21	1.40	1.77
		t_{PHL}	0.89	0.76	1.01	1.14	1.40

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

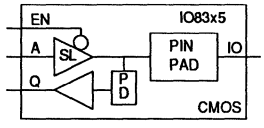
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.67	0.05	1.95	3.23	4.51	5.79
		t_{PHL}	1.02	0.09	3.38	5.74	8.11	10.47
EN	IO	t_{HZ}	2.48					
		t_{LZ}	1.30					
		t_{ZH}	0.93	0.05	2.21	3.49	4.78	6.06
		t_{ZL}	1.05	0.09	3.41	5.78	8.14	10.50

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IO83X5 is a 8ma non-inverting CMOS-bidirectional input/output buffer with an active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.49
EN	0.39
IO	5.61

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IO83X5 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	189.4	nA
†C_{pd}	8.60	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.77	0.80	0.89	1.03	1.30
		t_{PHL}	0.60	0.66	0.70	0.82	1.04

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

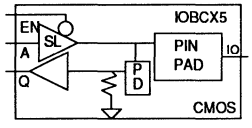
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.66	0.09	3.01	5.37	7.72	10.07
		t_{PHL}	0.92	0.07	2.55	4.19	5.83	7.46
EN	IO	t_{HZ}	2.66					
		t_{LZ}	1.37					
		t_{ZH}	0.96	0.09	3.31	5.66	8.01	10.37
		t_{ZL}	0.94	0.07	2.57	4.21	5.85	7.48

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IOBCX5 is an 8ma non-inverting CMOS-bidirectional input/output buffer with an active low enabled tri-state and controlled slew rate output, and a pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.49
EN	0.39
IO	5.62

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IOBCX5 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	189.4	nA
†C_{pd}	8.61	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.77	0.80	0.89	1.03	1.30
		t_{PHL}	0.60	0.66	0.70	0.82	1.04

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

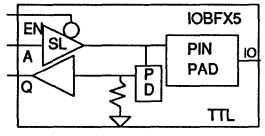
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.66	0.09	3.02	5.37	7.72	10.07
		t_{PHL}	0.92	0.07	2.56	4.19	5.83	7.46
EN	IO	t_{HZ}	2.66					
		t_{LZ}	1.37					
		t_{ZH}	0.96	0.09	3.31	5.66	8.01	10.37
		t_{ZL}	0.94	0.07	2.57	4.21	5.85	7.48

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IOBFX5 is a 8ma non-inverting TTL-bidirectional input/output buffer with an active low enabled tri-state and controlled slew rate output, and a pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.50
EN	0.38
IO	5.68

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IOBFX5 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	202.7	nA
†C_{pd}	8.84	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx}(ns) (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.03	1.10	1.21	1.40	1.77
		t_{PHL}	0.89	0.76	1.01	1.14	1.40

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

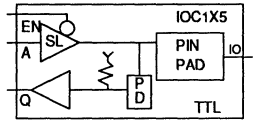
Max Delay (ns) From	To	Parameter	t_{dx}(ns) (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.67	0.05	1.95	3.23	4.51	5.79
		t_{PHL}	1.02	0.09	3.38	5.74	8.11	10.47
EN	IO	t_{HZ}	2.42					
		t_{LZ}	1.33					
		t_{ZH}	0.93	0.05	2.21	3.49	4.77	6.06
		t_{ZL}	1.05	0.09	3.41	5.77	8.14	10.50

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IOC1X5 is a 8ma non-inverting TTL-bidirectional input/output buffer with an active low enabled tri-state and controlled slew rate output, and a pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.50
EN	0.38
IO	5.68

Equivalent Gates: 0

Bolt Syntax: .....IO Q .IOC1X5 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	202.7	nA
†C_{pd}	8.83	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	1.04	1.10	1.21	1.40	1.77
		t_{PHL}	0.89	0.73	1.01	1.14	1.38

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

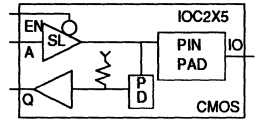
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.67	0.05	1.95	3.23	4.51	5.80
		t_{PHL}	1.02	0.09	3.38	5.74	8.10	10.47
EN	IO	t_{HZ}	2.42					
		t_{LZ}	1.33					
		t_{ZH}	0.93	0.05	2.21	3.49	4.77	6.06
		t_{ZL}	1.05	0.09	3.41	5.77	8.14	10.50

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IOC2X5 is a 8ma non-inverting CMOS-bidirectional input/output buffer with an active low enabled tri-state and controlled slew rate output, and a pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.49
EN	0.39
IO	5.61

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IOC2X5 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	189.4	nA
†C_{pd}	8.61	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	0.77	0.79	0.90	1.03	1.30
		t_{PHL}	0.60	0.66	0.70	0.82	1.04

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

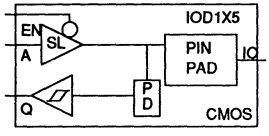
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.66	0.09	3.02	5.37	7.72	10.07
		t_{PHL}	0.92	0.07	2.56	4.19	5.83	7.47
EN	IO	t_{HZ}	2.66					
		t_{LZ}	1.37					
		t_{ZH}	0.96	0.09	3.31	5.66	8.02	10.37
		t_{ZL}	0.94	0.07	2.58	4.21	5.85	7.49

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

IOD1X5 is a 8ma non-inverting CMOS-bidirectional input/output buffer with an active low enabled tri-state and controlled slew rate output, and a CMOS Schmitt Trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.48
EN	0.38
IO	5.72

Equivalent Gates: 0
Bolt Syntax: .....IO Q .IOD1X5 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^\circ C$	210.8	nA
†C_{pd}	9.00	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristic:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
IO	Q	t_{PLH}	2.49	0.98	2.64	2.81	3.14
		t_{PHL}	2.09	0.86	2.23	2.37	2.66

Output Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	IO	t_{PLH}	0.68	0.09	3.03	5.38	7.73	10.09
		t_{PHL}	0.92	0.07	2.55	4.19	5.83	7.46
EN	IO	t_{HZ}	2.65					
		t_{LZ}	1.41					
		t_{ZH}	0.98	0.09	3.33	5.68	8.03	10.38
		t_{ZL}	0.94	0.07	2.57	4.21	5.85	7.48

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

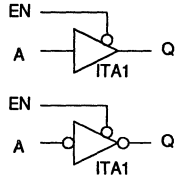
April, 1992

ITA1

Description

ITA1 is a non-inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.07
EN	0.10
Q	0.06

Equivalent Gates: 2
Bolt Syntax: .....Q .ITA1 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	25.3	nA
†C_{pd}	0.52	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

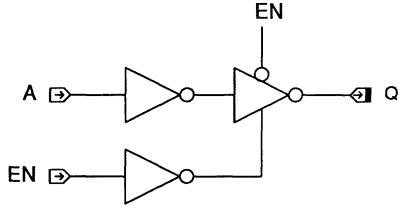
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
A	Q	t_{PLH}	0.49	2.09	0.82	1.18	1.88
		t_{PHL}	0.38	0.83	0.51	0.66	0.93
EN	Q	t_{HZ}	0.14				
		t_{LZ}	0.18				
		t_{ZH}	0.16	2.09	0.50	0.86	1.56
		t_{ZL}	0.19	0.83	0.32	0.46	0.74

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

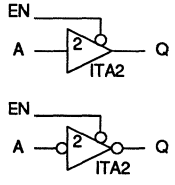
Logic Schematic



Description

ITA2 is a non-inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.07
E	0.17
Q	0.20

Equivalent Gates: 4
Bolt Syntax: .....Q .ITA2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	42.2	nA
†C_{pd}	1.05	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

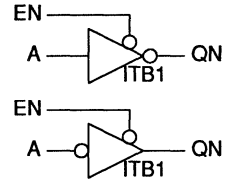
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	Q	t_{PLH}	0.59	0.71	0.71	0.83	1.07
		t_{PHL}	0.55	0.36	0.61	0.67	0.79
EN	Q	t_{HZ}	0.14				
		t_{LZ}	0.26				
		t_{ZH}	0.17	0.71	0.28	0.40	0.64
		t_{ZL}	0.22	0.36	0.28	0.34	0.46

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

ITB1 is an inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.07
E	0.10
QN	0.06

Equivalent Gates: 2
Bolt Syntax: .....QN .ITB1 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	16.9	nA
†C_{pd}	0.39	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

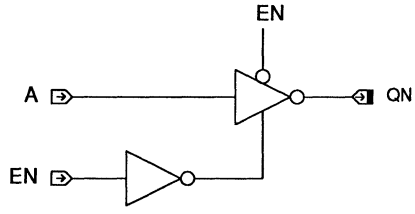
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	QN	t_{PLH}	0.36	2.08	0.70	1.06	1.75
		t_{PHL}	0.16	0.82	0.29	0.43	0.70
EN	QN	t_{HZ}	0.14				
		t_{LZ}	0.17				
		t_{ZH}	0.16	2.08	0.50	0.86	1.55
		t_{ZL}	0.19	0.82	0.32	0.46	0.73

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

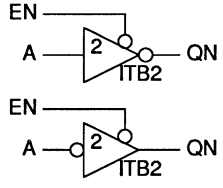
Logic Schematic



Description

ITB2 is an inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.20
E	0.18
QN	0.19

Equivalent Gates: 4
Bolt Syntax: .....QN .ITB2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	33.8	nA
†C_{pd}	0.92	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

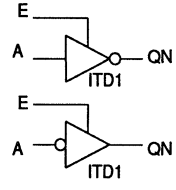
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	QN	t_{PLH}	0.35	0.72	0.47	0.59	0.83
		t_{PHL}	0.16	0.31	0.21	0.26	0.37
EN	QN	t_{HZ}	0.14				
		t_{LZ}	0.28				
		t_{ZH}	0.16	0.72	0.28	0.40	0.64
		t_{ZL}	0.23	0.31	0.28	0.34	0.44

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

ITD1 is an inverting internal tri-state buffer with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.07
E	0.10
QN	0.06

Equivalent Gates: 2
Bolt Syntax: .....QN .ITD1 A E ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85°C$	16.9	nA
†C_{pd}	0.39	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

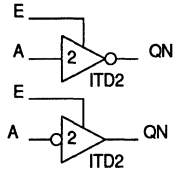
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	QN	t_{PLH}	0.37	2.08	0.70	1.06	1.76
		t_{PHL}	0.15	0.81	0.28	0.42	0.69
E	QN	t_{HZ}	0.30				
		t_{LZ}	0.10				
		t_{ZH}	0.24	2.08	0.58	0.93	1.63
		t_{ZL}	0.07	0.81	0.20	0.34	0.61

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

ITD2 is an inverting internal tri-state buffer with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.20
E	0.18
QN	0.19

Equivalent Gates: 4
Bolt Syntax: .....QN .ITD2 A E ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	33.8	nA
†C_{pd}	0.92	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

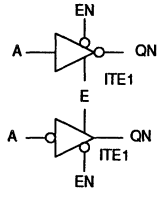
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
A	QN	t_{PLH}	0.37	0.71	0.49	0.61	0.84
		t_{PHL}	0.15	0.29	0.19	0.24	0.34
E	QN	t_{HZ}	0.50				
		t_{LZ}	0.10				
		t_{ZH}	0.30	0.71	0.42	0.54	0.77
		t_{ZL}	0.07	0.29	0.12	0.17	0.27

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

ITE1 is a two phase inverting internal tri-state buffer.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

IL = Illegal

Pin Loading

	Ci (pF)
A	0.06
E	0.03
EN	0.03
QN	0.06

Equivalent Gates: 1
Bolt Syntax: .....QN .ITE1 A E EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	8.5	nA
†C_{pd}	0.25	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

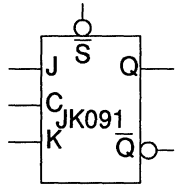
Max Delay (ns)		Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
From	To						
A	QN	t_{PLH}	0.37	2.08	0.70	1.06	1.76
		t_{PHL}	0.15	0.81	0.28	0.42	0.69
EN	QN	t_{HZ}	0.14				
		t_{ZH}	0.27	2.08	0.61	0.96	1.66
E	QN	t_{LZ}	0.10				
		t_{ZL}	0.13	0.81	0.26	0.39	0.67

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

JK091 is a static, master-slave, JK flip-flop, SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	H	L
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Change

Pin Loading

	Ci (pF)
J	0.06
K	0.07
C	0.21
SN	0.14

Equivalent Gates: 10

Bolt Syntax: .....Q QN .JK091 C J K SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85°C$	75.8	nA
†C_{pd}	2.38	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

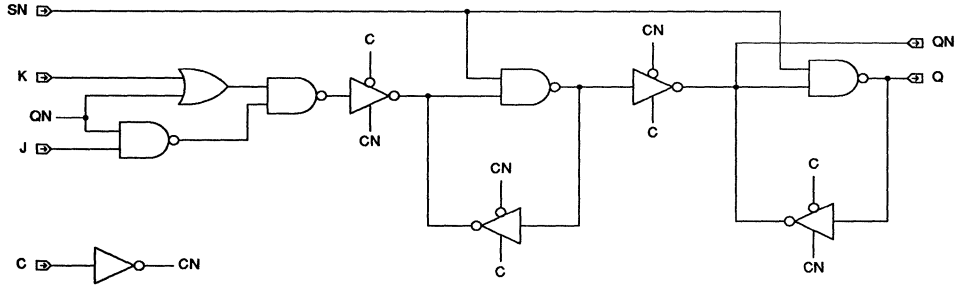
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	0.99	2.02	1.31	1.66	2.33
		t_{PHL}	0.28	0.75	0.40	0.53	0.78
C	Q	t_{PLH}	0.64	1.19	0.83	1.04	1.43
		t_{PHL}	1.24	1.21	1.43	1.64	2.05
SN	Q	t_{PLH}	0.28	1.19	0.47	0.67	1.07
SN	QN	t_{PHL}	0.81	1.21	0.93	1.06	1.31
Min C Width	High	t_w				1.24	
Min C Width	Low	t_w	1.58				
Min SN Width	Low	t_w				0.81	
Min J Setup		t_{su}	1.58				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.21				
Min K Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
MinSN Hold		t_h	0.19				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$

$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

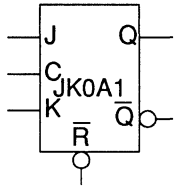
Logic Schematic



Description

JK0A1 is a static, master-slave, JK flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	L	H
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Change

Pin Loading

	Ci (pF)
J	0.07
K	0.07
C	0.22
RN	0.07

Equivalent Gates: 10
Bolt Syntax: .....Q QN .JK0A1 J K C RN;
Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	101.1	nA
†C_{pd}	2.43	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

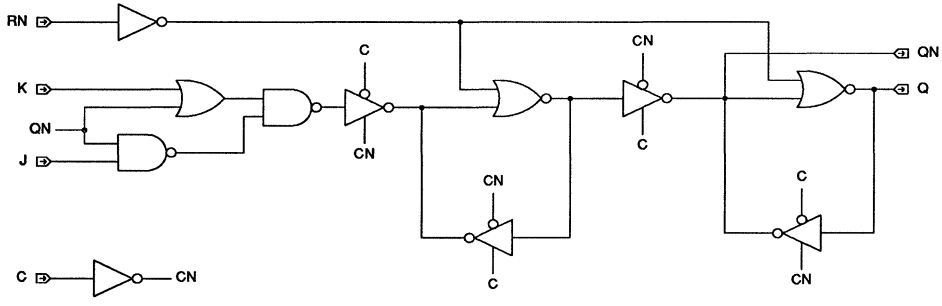
Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	0.99	2.02	1.31	1.66	2.34
		t_{PHL}	0.28	0.74	0.39	0.52	0.77
C	Q	t_{PLH}	0.77	2.05	1.09	1.45	2.13
		t_{PHL}	1.10	1.07	1.27	1.46	1.82
RN	Q	t_{PHL}	0.44	1.07	0.62	0.80	1.16
RN	QN	t_{PLH}	1.52	2.05	1.84	2.19	2.87
Min C Width	High	t_w				1.10	
Min C Width	Low	t_w	1.44				
Min RN Width	Low	t_w				1.52	
Min J Setup		t_{su}	1.44				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.27				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	0.75				
Min RN Hold		t_h	0.68				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) \cdot C_L(Q)) + (k_{tdf}(QN) \cdot C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) \cdot C_L(Q)) + (k_{tdr}(QN) \cdot C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

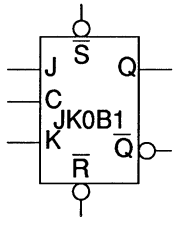
Logic Schematic



Description

JK0B1 is a static, master-slave, JK flip-flop, SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal
NC = No Change

Pin Loading

	Ci (pF)
J	0.06
K	0.07
C	0.23
SN	0.14
RN	0.14

Equivalent Gates: 13

Bolt Syntax: .....Q QN .JK0B1 C J K RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} T_J = 85°C	92.7	nA
†C_{pd}	2.94	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

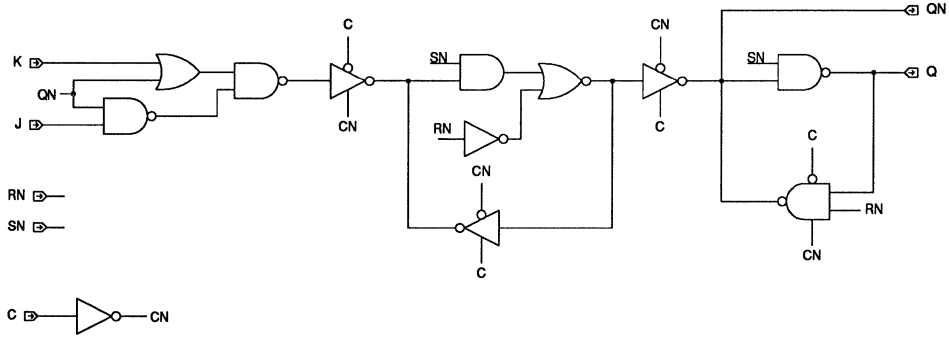
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	1.00	2.02	1.33	1.68	2.35
		t_{PHL}	0.29	0.74	0.41	0.53	0.78
C	Q	t_{PLH}	0.67	1.19	0.86	1.06	1.46
		t_{PHL}	1.29	1.19	1.48	1.68	2.08
SN	Q	t_{PLH}	0.32	1.19	0.51	0.72	1.12
SN	QN	t_{PHL}	1.14	0.74	1.26	1.39	1.63
RN	Q	t_{PHL}	1.73	1.19	1.92	2.12	2.52
RN	QN	t_{PLH}	1.45	2.02	1.78	2.12	2.80
Min C Width	High	t_w				1.29	
Min C Width	Low	t_w	1.48				
Min RN Width	Low	t_w				1.73	
Min SN Width	Low	t_w				1.14	
Min J Setup		t_{su}	1.48				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.33				
MinK Hold		t_h	0.00				
Min RN Setup		t_{su}	0.85				
Min RN Hold		t_h	0.67				
Min SN Setup		t_{su}	0.27				
Min SN Hold		t_h	0.19				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$

$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

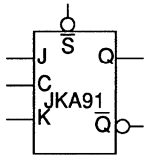
Logic Schematic



Description

JKA91 is a static, master-slave, JK flip-flop, SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Equivalent to JK091 with transmission gates.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	H	L
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	LH
H	H		↑	QN(n)	Q(n)

NC = No Change

Pin Loading

	Ci (pF)
J	0.07
K	0.07
C	0.21
SN	0.14

Equivalent Gates: 9

Bolt Syntax: .....Q QN .JKA91 C J K SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} T_J = 85°C	67.4	nA
†C_{pd}	2.84	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

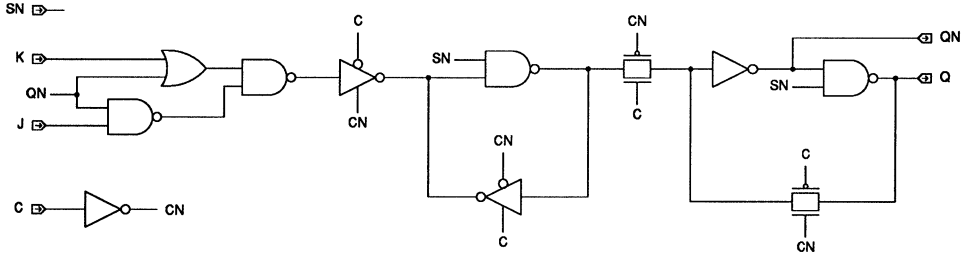
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	0.64	1.15	0.83	1.02	1.41
		t_{PHL}	0.63	0.72	0.75	0.87	1.11
C	Q	t_{PLH}	0.95	1.13	1.13	1.33	1.70
		t_{PHL}	0.89	0.93	1.04	1.20	1.52
SN	Q	t_{PLH}	0.50	1.13	0.68	0.87	1.25
SN	QN	t_{PHL}	0.99	0.93	1.11	1.23	1.47
Min C Width	High	t_w				1.33	
Min C Width	Low	t_w	1.69				
Min SN Width		t_w				1.23	
Min J Setup		t_{su}	1.69				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.29				
Min K Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
MinSN Hold		t_h	0.20				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) \cdot C_L(Q)) + (k_{tdf}(QN) \cdot C_L(QN))]$

$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) \cdot C_L(Q)) + (k_{tdr}(QN) \cdot C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

Logic Schematic



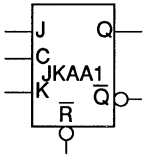
April, 1992

JKAA1

Description

JKAA1 is a static, master-slave, JK flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Equivalent to JK0A1 with transmission gates.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	L	H
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Change

Pin Loading

	Ci (pF)
J	0.07
K	0.07
C	0.21
RN	0.14

Equivalent Gates: 9
Bolt Syntax: .....Q QN .JKAA1 J K C RN ;
Power Characteristics:

Parameter	Value	Units
Static I_{DD} T_J = 85°C	67.4	nA
†C_{pd}	2.13	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

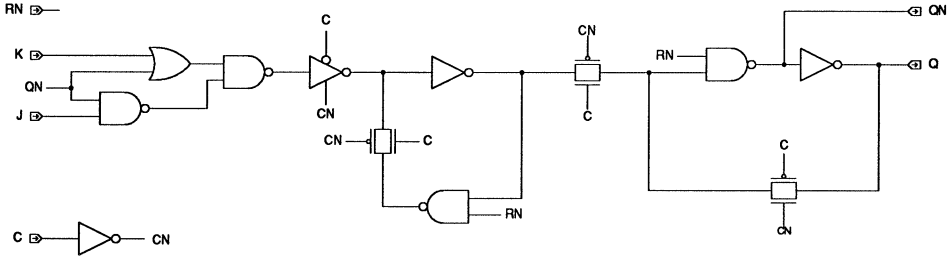
Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	0.61	1.14	0.80	0.99	1.37
		t_{PHL}	0.74	0.92	0.89	1.05	1.36
C	Q	t_{PLH}	1.10	1.16	1.29	1.49	1.88
		t_{PHL}	0.79	0.76	0.91	1.04	1.29
RN	Q	t_{PHL}	0.86	0.76	0.98	1.11	1.37
RN	QN	t_{PLH}	0.48	1.16	0.66	0.86	1.24
Min C Width	High	t_w				1.49	
Min C Width	Low	t_w	1.79				
Min RN Width		t_w				1.11	
Min J Setup		t_{su}	1.79				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.46				
Min K Hold		t_h	0.40				
Min RN Setup		t_{su}	0.20				
Min RN Hold		t_h	0.36				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

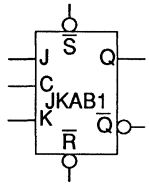
Logic Schematic



Description

JKAB1 is a static, master-slave, JK flip-flop, SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Equivalent to JK0B1 with transmission gates.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal
NC = No Change

Pin Loading

	Ci (pF)
J	0.06
K	0.07
C	0.21
SN	0.14
RN	0.14

Equivalent Gates: 10

Bolt Syntax: .....Q QN .JKAB1 C J K RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	67.4	nA
†C_{pd}	2.20	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

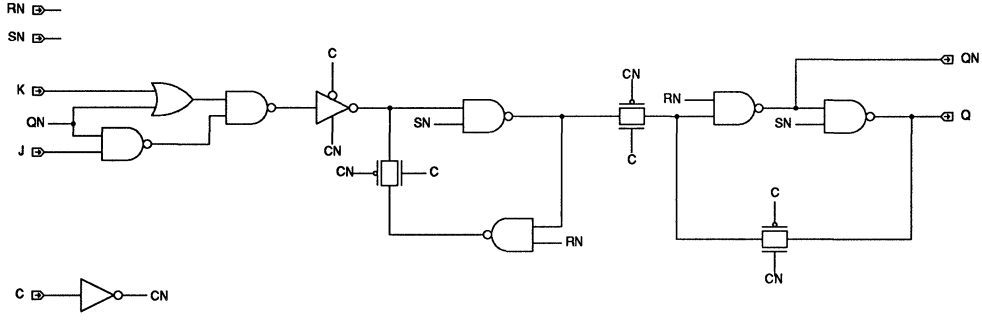
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	0.67	1.15	0.86	1.06	1.44
		t_{PHL}	0.75	0.91	0.90	1.05	1.36
C	Q	t_{PLH}	1.10	1.19	1.29	1.49	1.89
		t_{PHL}	0.90	0.96	1.05	1.22	1.54
SN	Q	t_{PLH}	0.47	1.19	0.66	0.86	1.26
SN	QN	t_{PHL}	1.07	0.91	1.22	1.37	1.68
RN	Q	t_{PHL}	0.87	0.96	1.02	1.18	1.51
RN	QN	t_{PLH}	0.48	1.15	0.66	0.86	1.24
Min C Width	High	t_w				1.49	
Min C Width	Low	t_w	1.86				
Min RN Width		t_w				1.18	
Min SN Width		t_w				1.37	
Min J Setup		t_{su}	1.86				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.54				
MinK Hold		t_h	0.00				
Min RN Setup		t_{su}	0.20				
Min RN Hold		t_h	0.41				
Min SN Setup		t_{su}	0.55				
Min SN Hold		t_h	0.18				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$

$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_{PV}K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_{PV}K_T(t_{dx} + k_{tdx} * C_L)$

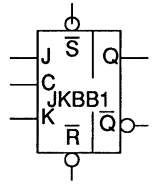
Logic Schematic



Description

JKBB1 is a static, master-slave, JK flip-flop, SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal
NC = No Change

Pin Loading

	Ci (pF)
J	0.07
K	0.07
C	0.22
SN	0.14
RN	0.14

Equivalent Gates: 13

Bolt Syntax: .....Q QN .JKBB1 C J K RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} T_J = 85°C	109.5	nA
†C_{pd}	3.21	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

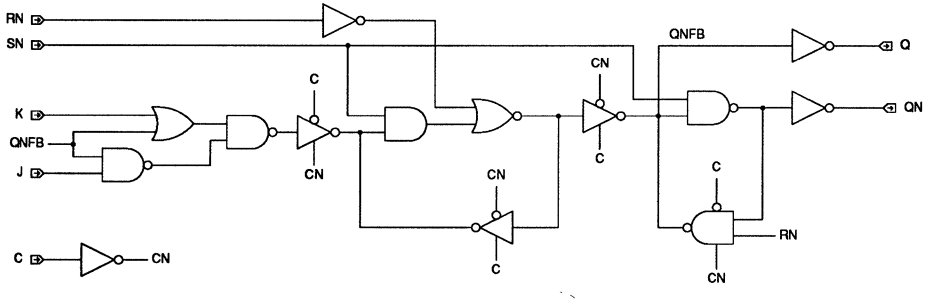
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	1.81	1.17	2.00	2.20	2.59
		t_{PHL}	0.91	0.74	1.03	1.16	1.41
C	Q	t_{PLH}	0.60	1.22	0.79	1.00	1.41
		t_{PHL}	1.22	1.17	1.40	1.60	2.00
SN	Q	t_{PLH}	1.48	1.22	1.67	1.88	2.29
SN	QN	t_{PHL}	0.51	0.74	0.63	0.75	1.00
RN	Q	t_{PHL}	1.62	1.17	1.81	2.01	2.40
RN	QN	t_{PLH}	2.21	1.17	2.40	2.60	2.99
Min C Width	High	t_w	1.54				
Min C Width	Low	t_w	1.54				
Min RN Width		t_w	1.96				
Min SN Width		t_w	1.08				
Min J Setup		t_{su}	1.54				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.33				
MinK Hold		t_h	0.00				
Min RN Setup		t_{su}	0.85				
Min RN Hold		t_h	0.68				
Min SN Setup		t_{su}	0.27				
Min SN Hold		t_h	0.19				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Logic Schematic



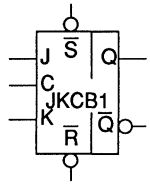
April, 1992

JKCB1

Description

JKCB1 is a static, master-slave, JK flip-flop, SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock. Equivalent to JKBB1 with transmission gates.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal
NC = No Change

Pin Loading

	Ci (pF)
J	0.06
K	0.07
C	0.21
SN	0.14
RN	0.14

Equivalent Gates: 11

Bolt Syntax: .....Q QN .JKCB1 C J K RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	84.3	nA
†C_{pd}	2.51	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

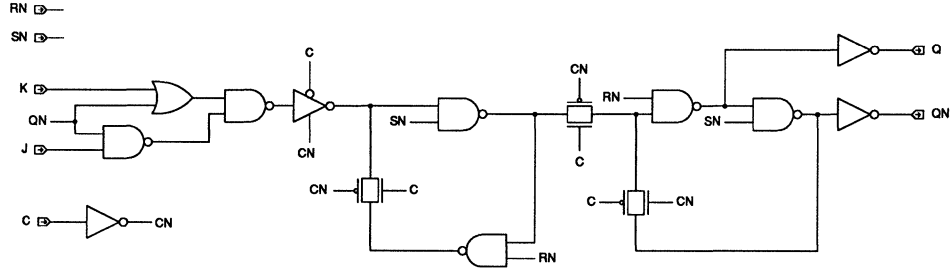
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	1.30	1.14	1.48	1.68	2.06
		t_{PHL}	1.38	0.71	1.50	1.62	1.86
C	Q	t_{PLH}	1.04	1.20	1.23	1.44	1.84
		t_{PHL}	0.78	0.85	0.91	1.06	1.34
SN	Q	t_{PLH}	1.44	1.20	1.63	1.84	2.24
SN	QN	t_{PHL}	0.68	0.71	0.80	0.92	1.16
RN	Q	t_{PHL}	0.68	0.85	0.81	0.96	1.24
RN	QN	t_{PLH}	1.35	1.14	1.53	1.73	2.11
Min C Width	High	t_w	1.08				
Min C Width	Low	t_w	1.94				
Min RN Width		t_w	1.08				
Min SN Width		t_w	1.17				
Min J Setup		t_{su}	1.94				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.54				
MinK Hold		t_h	0.00				
Min RN Setup		t_{su}	0.20				
Min RN Hold		t_h	0.41				
Min SN Setup		t_{su}	0.55				
Min SN Hold		t_h	0.18				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

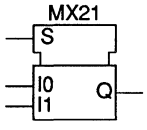
Logic Schematic



Description

MX21 is a 2-input to 1-output digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Pin Loading

	Ci (pF)
I0	0.07
I1	0.07
S	0.14

Equivalent Gates: 3
Bolt Syntax: .....Q .MX21 I0 I1 S ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	33.8	nA
†C_{pd}	0.66	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

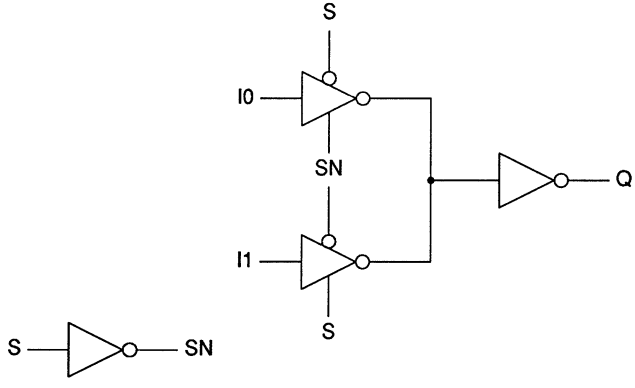
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Ix Input	Q	t_{PLH}	0.43	1.15	0.62	0.81	1.20
		t_{PHL}	0.54	1.00	0.70	0.88	1.21
S	Q	t_{PLH}	0.69	1.15	0.87	1.07	1.46
		t_{PHL}	0.91	1.00	1.07	1.24	1.57

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

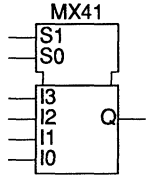
Logic Schematic



Description

MX41 is a four-to-one digital multiplexer.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

Pin Loading

	Ci (pF)
I0	0.07
I1	0.07
I2	0.08
I3	0.07
S0	0.20
S1	0.20

Equivalent Gates: 8
Bolt Syntax: .....Q .MX41 I0 I1 I2 I3 S0 S1 ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	59.0	nA
†C_{pd}	1.62	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

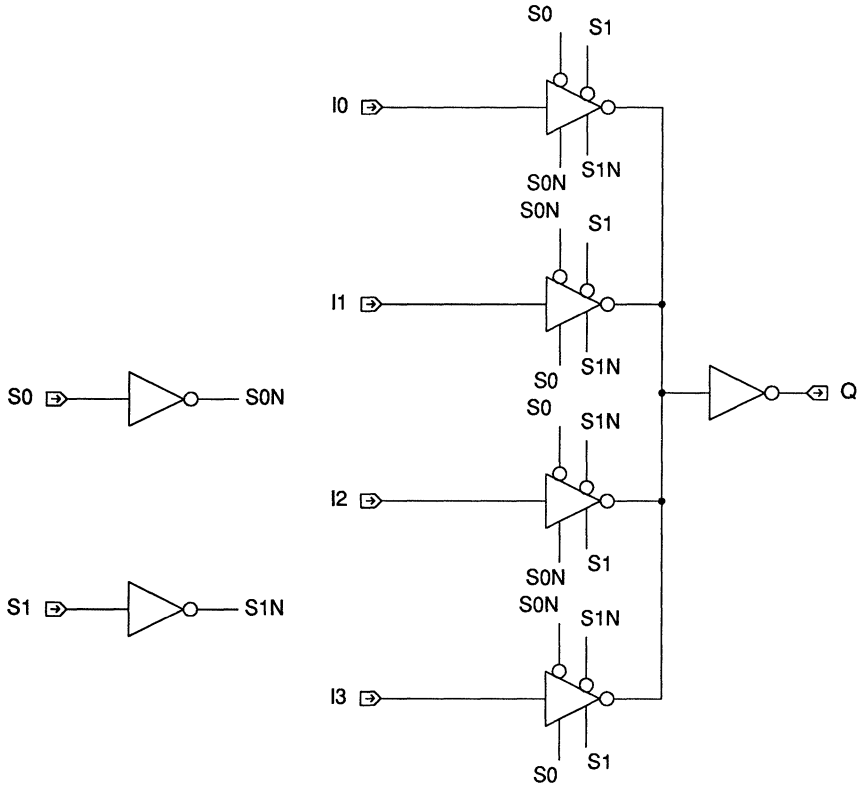
Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Ix Input	Q	t_{PLH}	0.93	1.24	1.13	1.34	1.76
		t_{PHL}	1.06	1.85	1.36	1.68	2.30
Any Sx Input	Q	t_{PLH}	1.00	1.24	1.20	1.41	1.83
		t_{PHL}	1.68	1.85	1.98	2.30	2.92

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

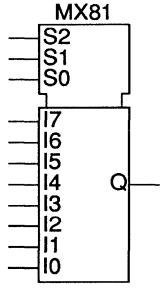
Logic Schematic



Description

MX81 is an eight-to-one digital multiplexer.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

Pin Loading

	Ci (pF)
I0	0.07
I1	0.07
I2	0.07
I3	0.07
I4	0.07
I5	0.07
I6	0.07
I7	0.07
S0	0.35
S1	0.21
S2	0.14

Equivalent Gates: 16
Bolt Syntax: .....Q .MX81 I0 I1 I2 I3 I4 I5 I6 I7 S0 S1 S2 ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	151.6	nA
†C_{pd}	3.45	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

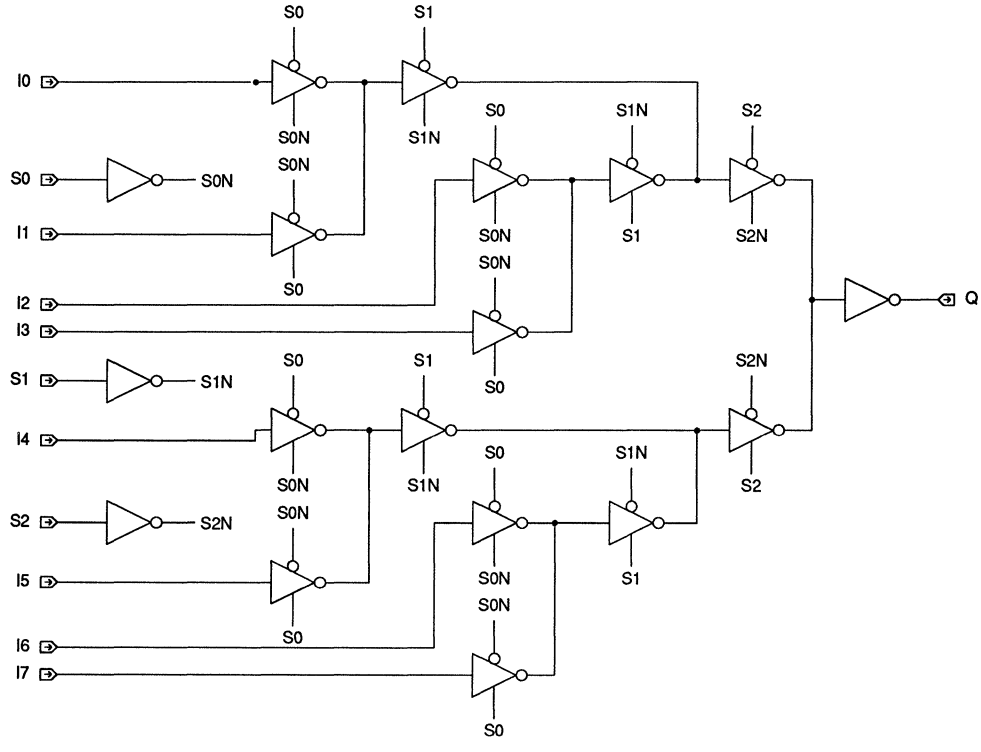
Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Ix Input	Q	t_{PLH}	1.55	1.14	1.73	1.93	2.31
		t_{PHL}	1.64	0.98	1.80	1.97	2.29
Any Sx Input	Q	t_{PLH}	1.55	1.14	1.74	1.93	2.31
		t_{PHL}	1.77	0.98	1.92	2.09	2.42

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

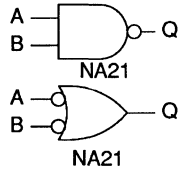
Logic Schematic



Description

NA21 is a two-input gate, which performs a logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07

Equivalent Gates: 1
Bolt Syntax: .....Q .NA21 A B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	8.6	nA
†C_{pd}	0.11	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.22	1.13	0.40	0.59	0.97
		t_{PHL}	0.14	0.79	0.27	0.40	0.67

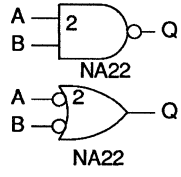
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description

NA22 is a two-input gate, which performs a logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

Pin Loading

	Ci (pF)
A	0.13
B	0.13

Equivalent Gates: 2
Bolt Syntax: .....Q .NA22 A B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	17.0	nA
†C_{pd}	0.23	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

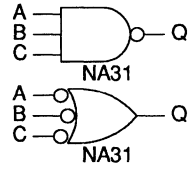
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.22	0.57	0.31	0.40	0.60
		t_{PHL}	0.14	0.42	0.20	0.28	0.42

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NA31 is a three-input gate, which performs a logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.06

Equivalent Gates: 2
Bolt Syntax: .....Q .NA31 A B C ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	12.8	nA
†C_{pd}	0.22	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.32	1.17	0.51	0.71	1.10
		t_{PHL}	0.26	1.03	0.42	0.60	0.95

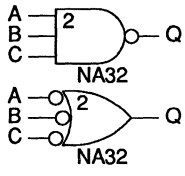
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description

NA32 is a three-input gate, which performs a logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Pin Loading

	Ci (pF)
A	0.13
B	0.13
C	0.13

Equivalent Gates: 3
Bolt Syntax: .....Q .NA32 A B C ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	25.4	nA
†C_{pd}	0.38	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

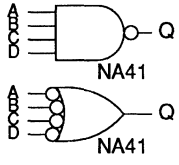
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.30	0.53	0.38	0.47	0.65
		t_{PHL}	0.23	0.47	0.31	0.39	0.55

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NA41 is a four-input gate, which performs a logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.06
D	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .NA41 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	17.0	nA
†C_{pd}	0.26	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

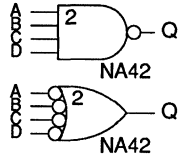
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
Any Input	Q	t_{PLH}	0.37	1.20	0.56	0.77	1.17
		t_{PHL}	0.35	1.29	0.56	0.78	1.21

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NA42 is a four-input gate, which performs a logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.13
B	0.13
C	0.13
D	0.13

Equivalent Gates: 4
Bolt Syntax: .....Q .NA42 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	33.8	nA
†C_{pd}	0.53	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

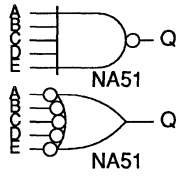
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.37	0.62	0.47	0.57	0.78
		t_{PHL}	0.35	0.65	0.46	0.57	0.79

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NA51 is a five-input gate, which performs a logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.06
D	0.07
E	0.06

Equivalent Gates: 3
Bolt Syntax: .....Q .NA51 A B C D E ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	21.2	nA
†C_{pd}	0.37	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

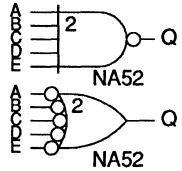
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.45	1.24	0.65	0.87	1.28
		t_{PHL}	0.53	1.54	0.78	1.04	1.56

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NA52 is a five-input gate, which performs a logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.13
B	0.13
C	0.13
D	0.13
E	0.13

Equivalent Gates: 5
Bolt Syntax: .....Q .NA52 A B C D E ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	42.2	nA
†C_{pd}	0.69	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

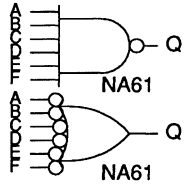
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.43	0.65	0.53	0.64	0.86
		t_{PHL}	0.50	0.78	0.63	0.76	1.02

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NA61 is a six-input gate, which performs a logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.07
D	0.07
E	0.07
F	0.07

Equivalent Gates: 5
Bolt Syntax: .....Q .NA61 A B C D E F ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	50.6	nA
†C_{pd}	1.04	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

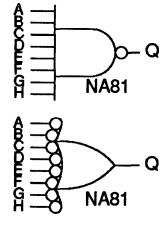
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.88	0.55	0.97	1.07	1.25
		t_{PHL}	1.15	0.52	1.23	1.32	1.49

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NA81 is a eight-input gate, which performs a logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.06
D	0.07
E	0.07
F	0.07
G	0.06
H	0.07

Equivalent Gates: 6
Bolt Syntax: .....Q .NA81 A B C D E F G H;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	50.6	nA
†C_{pd}	1.08	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

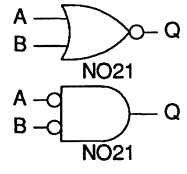
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.91	0.57	1.00	1.10	1.29
		t_{PHL}	1.25	0.54	1.33	1.43	1.61

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NO21 is a two-input gate, which performs a logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07

Equivalent Gates: 1
Bolt Syntax: .....Q .NO21 A B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	17.0	nA
†C_{pd}	0.12	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

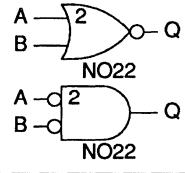
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.30	2.09	0.63	0.99	1.69
		t_{PHL}	0.12	0.59	0.22	0.32	0.51

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NO22 is a two-input gate, which performs a logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Pin Loading

	Ci (pF)
A	0.13
B	0.13

Equivalent Gates: 2
Bolt Syntax: .....Q .NO22 A B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	33.8	nA
†C_{pd}	0.24	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

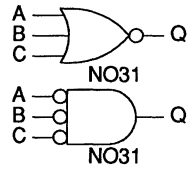
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.30	1.06	0.47	0.65	1.00
		t_{PHL}	0.11	0.34	0.16	0.22	0.33

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NO31 is a three-input gate, which performs a logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .NO31 A B C ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	25.4	nA
†C_{pd}	0.23	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

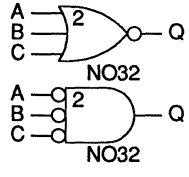
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.66	3.09	1.15	1.68	2.72
		t_{PHL}	0.14	0.61	0.24	0.34	0.55

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NO32 is a three-input gate, which performs a logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

Pin Loading

	Ci (pF)
A	0.13
B	0.13
C	0.13

Equivalent Gates: 3
Bolt Syntax: .....Q .NO32 A B C ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	50.6	nA
†C_{pd}	0.40	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

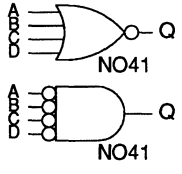
Max Delay (ns)		Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
From	To						
Any Input	Q	t_{PLH}	0.61	1.57	0.86	1.13	1.66
		t_{PHL}	0.12	0.34	0.18	0.23	0.35

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NO41 is a four-input gate, which performs a logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.07
D	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .NO41 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	33.8	nA
†C_{pd}	0.31	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	1.13	4.02	1.77	2.46	3.81
		t_{PHL}	0.16	0.61	0.25	0.36	0.56

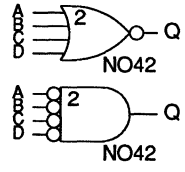
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description

NO42 is a four-input gate, which performs a logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.13
B	0.13
C	0.13
D	0.13

Equivalent Gates: 4
Bolt Syntax: .....Q .NO42 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	67.4	nA
†C_{pd}	0.56	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

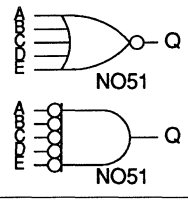
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	1.05	2.03	1.37	1.72	2.40
		t_{PHL}	0.13	0.34	0.19	0.24	0.36

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NO51 is a five-input gate, which performs a logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.06
D	0.07
E	0.06

Equivalent Gates: 3
Bolt Syntax: .....Q .NO51 A B C D E ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	42.2	nA
†C_{pd}	0.42	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

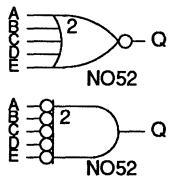
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	1.78	4.86	2.56	3.40	5.02
		t_{PHL}	0.17	0.60	0.27	0.37	0.57

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

NO52 is a five-input gate, which performs a logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.13
B	0.13
C	0.13
D	0.13
E	0.13

Equivalent Gates: 5
Bolt Syntax: .....Q .NO52 A B C D E ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	84.3	nA
†C_{pd}	0.73	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

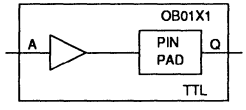
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
Any Input	Q	t_{PLH}	1.56	2.60	1.98	2.43	3.30
		t_{PHL}	0.14	0.33	0.19	0.25	0.36

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB01X1 is a 1ma non-inverting, TTL-level output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.19

Equivalent Gates: 0
Bolt Syntax: .....Q .OB01X1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	111.9	nA
†C_{pd}	6.76	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

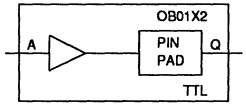
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	1.96	0.28	9.07	16.18	23.29	30.41
		t_{PHL}	1.88	0.29	9.10	16.32	23.54	30.76

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB01X2 is a 2ma non-inverting, TTL-level output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.19

Equivalent Gates: 0
Bolt Syntax: .....Q .OB01X2 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	141.4	nA
†C_{pd}	5.53	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

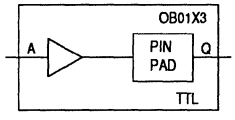
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	1.07	0.16	4.97	8.87	12.77	16.67
		t_{PHL}	1.27	0.19	6.09	10.91	15.73	20.56

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB01X3 is a 4ma non-inverting, TTL-level output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.19

Equivalent Gates: 0
Bolt Syntax: .....Q .OB01X3 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	145.0	nA
†C_{pd}	5.82	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

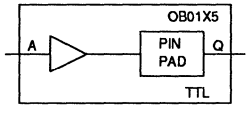
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.83	0.08	2.78	4.73	6.67	8.62
		t_{PHL}	0.96	0.10	3.35	5.74	8.12	10.51

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB01X5 is a 8ma non-inverting, TTL-level output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.36

Equivalent Gates: 0
Bolt Syntax: .....Q .OB01X5 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	157.0	nA
†C_{pd}	6.44	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

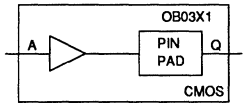
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.65	0.04	1.62	2.60	3.57	4.54
		t_{PHL}	0.71	0.05	1.91	3.11	4.31	5.51

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB03X1 is a 1ma non-inverting CMOS-level output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.19

Equivalent Gates: 0
Bolt Syntax: .....Q .OB03X1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	111.9	nA
†C_{pd}	6.76	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	2.77	0.52	15.87	28.97	42.07	55.18
		t_{PHL}	1.26	0.20	6.16	11.06	15.96	20.85

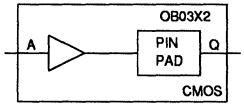
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description

OB03X2 is a 2ma non-inverting CMOS-level output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.19

Equivalent Gates: 0
Bolt Syntax: .....Q .OB03X2 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	141.4	nA
†C_{pd}	5.53	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

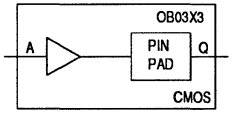
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	1.51	0.29	8.67	15.83	22.99	30.14
		t_{PHL}	1.05	0.13	4.33	7.61	10.89	14.17

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB03X3 is a 4ma non-inverting CMOS-level output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.19

Equivalent Gates: 0
Bolt Syntax: .....Q .OB03X3 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	145.0	nA
†C_{pd}	5.82	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

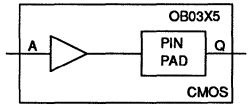
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	1.07	0.14	4.64	8.21	11.78	15.36
		t_{PHL}	0.76	0.07	2.40	4.05	5.69	7.33

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB03X5 is a 8ma non-inverting CMOS-level output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.36

Equivalent Gates: 0
Bolt Syntax: .....Q .OB03X5 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	157.0	nA
†C_{pd}	6.44	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

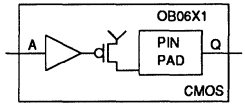
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.76	0.07	2.55	4.34	6.13	7.91
		t_{PHL}	0.63	0.03	1.45	2.27	3.09	3.91

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB06X1 is a 1ma inverting CMOS-level P-channel open-drain (pull-up) output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.13
Q	5.13

Equivalent Gates: 0
Bolt Syntax: .....Q .OB06X1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	149.8	nA
†C_{pd}	6.34	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

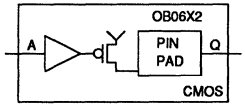
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	1.34	0.51	14.09	26.83	39.57	52.31
		t_{PZ}	0.98					

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB06X2 is a 2ma inverting CMOS-level P-channel open-drain (pull-up) output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.13
Q	5.20

Equivalent Gates: 0
Bolt Syntax: .....Q .OB06X2 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	149.8	nA
†C_{pd}	5.69	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

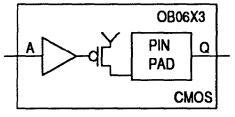
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH} t_{PZ}	0.21 0.75	0.28	7.33	14.45	21.56	28.68

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB06X3 is a 4ma inverting CMOS-level P-channel open-drain (pull-up) output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.12
Q	5.13

Equivalent Gates: 0
Bolt Syntax: .....Q .OB06X3 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	153.4	nA
†C_{pd}	5.85	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.67	0.14	4.17	7.66	11.16	14.65
		t_{PZ}	0.84					

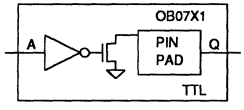
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description

OB07X1 is a 1ma non-inverting TTL-level N-channel open drain (pull-down) output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Ci (pF)
A	0.19
Q	5.00

Equivalent Gates: 0
Bolt Syntax: .....Q .OB07X1 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	108.3	nA
†C_{pd}	5.94	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

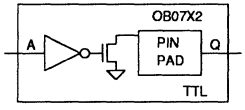
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PZ}	0.54					
		t_{PHL}	0.44	0.29	7.68	14.92	22.16	29.40

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB07X2 is a 2ma non-inverting TTL-level N-channel open drain (pull-down) output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Ci (pF)
A	0.19
Q	5.20

Equivalent Gates: 0
Bolt Syntax: .....Q .OB07X2 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	141.4	nA
†C_{pd}	5.47	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

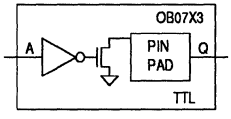
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PZ}	0.38					
		t_{PHL}	0.37	0.19	5.11	9.86	14.60	19.34

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB07X3 is a 4ma non-inverting TTL-level N-channel open drain (pull-down) output buffer pad cell.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Ci (pF)
A	0.19
Q	5.13

Equivalent Gates: 0
Bolt Syntax: .....Q .OB07X3 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	141.4	nA
†C_{pd}	5.52	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

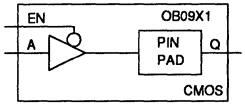
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PZ}	0.52					
		t_{PHL}	0.50	0.10	2.88	5.26	7.64	10.02

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB09X1 is a 1ma non-inverting CMOS-level tri-state output buffer pad cell, with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.24
EN	0.25
Q	4.93

Equivalent Gates: 0
Bolt Syntax: .....Q .OB09X1 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	124.5	nA
†C_{pd}	7.27	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

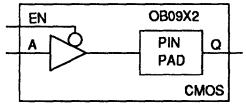
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.28	0.52	13.28	26.28	39.28	52.27
		t_{PHL}	0.86	0.20	5.74	10.62	15.49	20.37
EN	Q	t_{HZ}	1.36					
		t_{LZ}	1.14					
		t_{ZH}	0.45	0.52	13.45	26.44	39.44	52.44
		t_{ZL}	0.91	0.20	5.78	10.66	15.53	20.41

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB09X2 is a 2ma non-inverting CMOS-level tri-state output buffer pad cell, with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.24
EN	0.25
Q	5.23

Equivalent Gates: 0
Bolt Syntax: .....Q .OB09X2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	157.6	nA
†C_{pd}	6.17	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

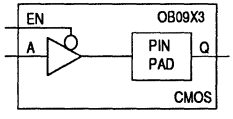
Max Delay (ns) From	To	Parameter	t_{dx}(ns) (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.05	0.29	7.18	14.31	21.44	28.57
		t_{PHL}	0.53	0.13	3.80	7.07	10.34	13.60
EN	Q	t_{HZ}	1.14					
		t_{LZ}	0.81					
		t_{ZH}	0.27	0.29	7.40	14.53	21.67	28.80
		t_{ZL}	0.60	0.13	3.86	7.13	10.40	13.67

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB09X3 is a 4ma non-inverting CMOS-level tri-state output buffer pad cell, with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.24
EN	0.27
Q	5.13

Equivalent Gates: 0
Bolt Syntax: .....Q .OB09X3 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	161.8	nA
†C_{pd}	6.32	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

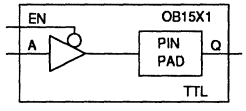
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.37	0.14	3.92	7.47	11.02	14.57
		t_{PHL}	0.88	0.07	2.52	4.17	5.81	7.45
EN	Q	t_{HZ}	1.17					
		t_{LZ}	1.11					
		t_{ZH}	0.57	0.14	4.12	7.67	11.22	14.77
		t_{ZL}	0.94	0.07	2.59	4.23	5.87	7.52

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB15X1 is a 1ma non-inverting TTL-level tri-state output buffer pad cell, with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.24
EN	0.25
Q	4.93

Equivalent Gates: 0
Bolt Syntax: .....Q .OB15X1 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	124.5	nA
†C_{pd}	7.27	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

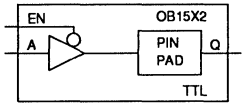
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.51	0.28	7.63	14.74	21.86	28.97
		t_{PHL}	0.91	0.29	8.18	15.45	22.72	29.99
EN	Q	t_{HZ}	1.37					
		t_{LZ}	1.14					
		t_{ZH}	0.68	0.28	7.80	14.92	22.03	29.15
		t_{ZL}	0.96	0.29	8.23	15.50	22.77	30.04

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB15X2 is a 2ma non-inverting TTL-level tri-state output buffer pad cell, with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.24
EN	0.25
Q	5.23

Equivalent Gates: 0
Bolt Syntax: .....Q .OB15X2 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	157.6	nA
†C_{pd}	6.17	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

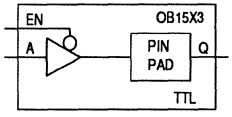
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.23	0.16	4.13	8.02	11.92	15.82
		t_{PHL}	0.56	0.19	5.35	10.13	14.91	19.70
EN	Q	t_{HZ}	1.14					
		t_{LZ}	0.81					
		t_{ZH}	0.46	0.16	4.36	8.26	12.15	16.05
		t_{ZL}	0.64	0.19	5.43	10.21	14.99	19.78

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB15X3 is a 4ma non-inverting TTL-level tri-state output buffer pad cell, with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.24
EN	0.27
Q	5.13

Equivalent Gates: 0
Bolt Syntax: .....Q .OB15X3 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^\circ C$	161.8	nA
†C_{pd}	6.32	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

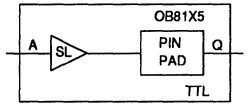
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.44	0.08	2.38	4.32	6.26	8.20
		t_{PHL}	0.88	0.10	3.29	5.70	8.11	10.52
EN	Q	t_{HZ}	1.17					
		t_{LZ}	1.11					
		t_{ZH}	0.65	0.08	2.59	4.53	6.47	8.41
		t_{ZL}	0.93	0.10	3.34	5.75	8.16	10.57

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB81X5 is a 8ma non-inverting TTL-level output buffer pad cell with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.31
Q	5.50

Equivalent Gates: 0
Bolt Syntax: .....Q .OB81X5 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	157.6	nA
†C_{pd}	7.18	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

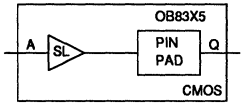
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.88	0.05	2.17	3.46	4.75	6.04
		t_{PHL}	1.15	0.09	3.44	5.74	8.03	10.32

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB83X5 is a 8ma non-inverting CMOS-level output buffer pad cell with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.31
Q	5.50

Equivalent Gates: 0
Bolt Syntax: .....Q .OB83X5 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	157.6	nA
†C_{pd}	7.18	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

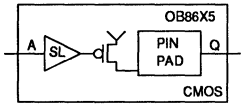
Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Capacitive Load (CL)			
From	To		(ns)	(ns/pF)	25	50	75	100
A	Q	t_{PLH}	1.07	0.09	3.42	5.76	8.11	10.46
		t_{PHL}	0.93	0.07	2.57	4.20	5.84	7.48

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB86X5 is a 8ma inverting CMOS-level output buffer pad cell with a P-channel open drain (pull-down), and controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.09
Q	5.42

Equivalent Gates: 0
Bolt Syntax: .....Q .OB86X5 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	153.4	nA
†C_{pd}	6.70	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	1.23	0.09	3.59	5.95	8.31	10.67
		t_{PZ}	1.37					

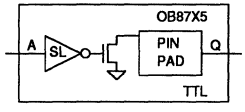
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description

OB87X5 is a 8ma non-inverting TTL-level output buffer pad cell with N-channel open drain (pull-down), and controlled slew rate output..

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Ci (pF)
A	0.23
Q	5.36

Equivalent Gates: 0
Bolt Syntax: .....Q .OB87X5 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	149.8	nA
†C_{pd}	6.29	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

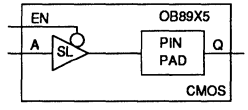
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PZ}	1.13					
		t_{PHL}	1.04	0.09	3.34	5.63	7.93	10.22

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OB89X5 is a 8ma non-inverting CMOS-level tri-state output buffer pad cell, with active low enable, and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.40
EN	0.40
Q	5.41

Equivalent Gates: 0
Bolt Syntax: .....Q .OB89X5 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	178.6	nA
†C_{pd}	7.94	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.57	0.09	2.92	5.26	7.61	9.96
		t_{PHL}	0.94	0.07	2.58	4.22	5.86	7.50
EN	Q	t_{HZ}	2.34					
		t_{LZ}	1.22					
		t_{ZH}	0.94	0.09	3.29	5.64	7.99	10.34
		t_{ZL}	0.98	0.07	2.62	4.26	5.90	7.54

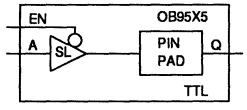
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description

OB95X5 is a 8ma non-inverting TTL-level tri-state output buffer pad cell, with active low enable, and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.41
EN	0.40
Q	5.41

Equivalent Gates: 0
Bolt Syntax: .....Q .OB95X5 A EN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	178.6	nA
†C_{pd}	7.94	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

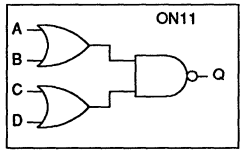
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (CL) 25	50	75	100
A	Q	t_{PLH}	0.62	0.05	1.90	3.19	4.47	5.75
		t_{PHL}	0.99	0.09	3.33	5.67	8.00	10.34
EN	Q	t_{HZ}	2.35					
		t_{LZ}	1.22					
		t_{ZH}	0.99	0.05	2.28	3.56	4.85	6.13
		t_{ZL}	1.02	0.09	3.36	5.70	8.04	10.38

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

ON11 is an OR-NAND circuit consisting of two 2-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
H	X	H	X	L
H	X	X	H	L
X	H	H	X	L
X	H	X	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.07
D	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .ON11 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	17.0	nA
†C_{pd}	0.34	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

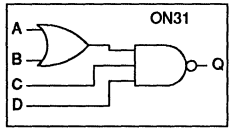
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.72	2.09	1.05	1.41	2.11
		t_{PHL}	0.23	0.61	0.33	0.43	0.64

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

ON31 is an OR-NAND circuit consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	X	H	H	L
X	H	H	H	L

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.07
D	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .ON31 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	12.8	nA
†C_{pd}	0.30	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

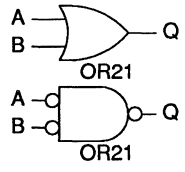
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.39	2.10	0.72	1.08	1.79
		t_{PHL}	0.28	1.04	0.45	0.63	0.97

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OR21 is a two-input gate, which performs a logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .OR21 A B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	25.4	nA
†C_{pd}	0.27	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.31	1.13	0.49	0.69	1.06
		t_{PHL}	0.56	0.77	0.68	0.81	1.07

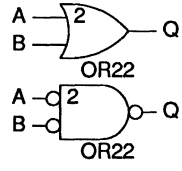
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description

OR22 is a two-input gate, which performs a logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .OR22 A B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	33.8	nA
†C_{pd}	0.65	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

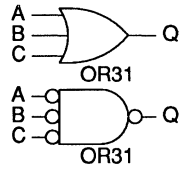
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.37	0.56	0.46	0.56	0.74
		t_{PHL}	0.70	0.51	0.78	0.87	1.04

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OR31 is a three-input gate, which performs a logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.07

Equivalent Gates: 2
Bolt Syntax: .....Q .OR31 A B C ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	33.8	nA
†C_{pd}	0.37	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

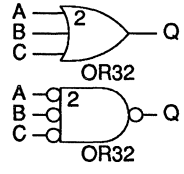
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.35	1.14	0.53	0.73	1.11
		t_{PHL}	0.98	0.95	1.13	1.29	1.61

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OR32 is a three-input gate, which performs a logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.06

Equivalent Gates: 3
Bolt Syntax: .....Q .OR32 A B C ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85°C$	42.2	nA
†C_{pd}	0.52	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

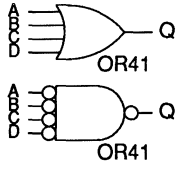
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.42	0.57	0.51	0.61	0.80
		t_{PHL}	1.18	0.64	1.28	1.39	1.61

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

OR41 is a four-input gate, which performs a logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.06
D	0.07

Equivalent Gates: 3
Bolt Syntax: .....Q .OR41 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	42.2	nA
†C_{pd}	0.45	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.37	1.16	0.56	0.76	1.15
		t_{PHL}	1.48	1.13	1.66	1.85	2.23

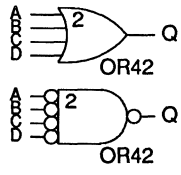
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

ASIC Functions

Description

OR42 is a four-input gate, which performs a logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Pin Loading

	Ci (pF)
A	0.07
B	0.07
C	0.06
D	0.07

Equivalent Gates: 3
Bolt Syntax: .....Q .OR42 A B C D ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	50.6	nA
†C_{pd}	0.53	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

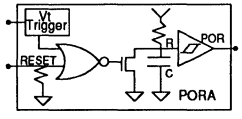
Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
Any Input	Q	t_{PLH}	0.40	0.61	0.50	0.60	0.81
		t_{PHL}	1.70	0.78	1.82	1.96	2.22

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

PORA is a Power-On-Reset circuit for 5 volt operation.

Logic Symbol



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Ci (pF)
RESET	4.60

Equivalent Gates: 0
Bolt Syntax: .....POR .PORA RESET ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	383.8	nA
†C_{pd}	93.44	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

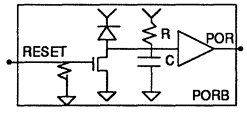
Max Delay (ns)		Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
From	To						
RESET	POR	t_{PLH}	2652	1	2652	2652	2652
		t_{PHL}	25	1	25	25	25
VDD	POR	t_{PLH}	2472	1	2472	2472	2472

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Description

PORB is a Power-On-Reset circuit for 3 volt operation.

Logic Symbol



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Ci (pF)
RESET	4.60

Equivalent Gates: 0
Bolt Syntax: .....POR .PORB RESET ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	330.0	nA
†C_{pd}	89.91	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

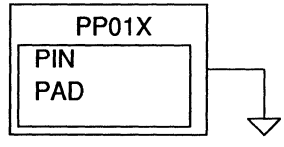
Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
RESET	POR	t_{PLH}	1555	1	1555	1556	1556
		t_{PHL}	22	1	22	23	23
VDD	POR	t_{PLH}	1550	1	1551	1551	1551

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

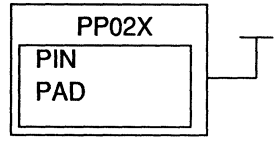
Description

PP01X is a Vss power supply pin for output buffers, input buffers, and core cells combined. The PP01X is intended for circumstances where output and core busses are to be tied together. It should not be used in conjunction with PPP1X nor PPC1X.



Description

PP02X is a Vdd power supply pin for output buffers, and input buffers, and core cells combined..



Note: One PP02X must be used for each power (VDD) pin.

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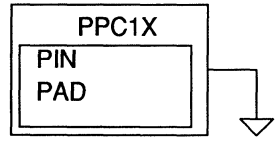
PPC1X

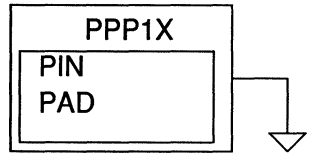
Description

PPC1X is a Vss power supply pin for core cells and input buffers only. One PPC1X must be used for each ground (VSS) pin for the core cells and input buffers.



Description

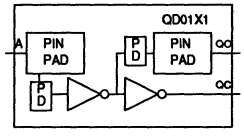
PPP1X is a Vss power supply pin for output buffers only. One PPP1X must be used for each ground (VSS) pin.



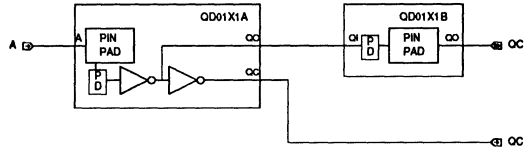
Description

QD01X1 is a 3.58 MHz(1MHz - 10MHz) cyrystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This macro is made up of two pad macros and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad macros.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Ci (pF)
A	3.01
QO	0.38

Equivalent Gates: 0
Bolt Syntax: .....QC QO .QD01x1A A ;
.....QI QO .QD01X1B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	15.8	nA
†C_{pd}	0.49	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

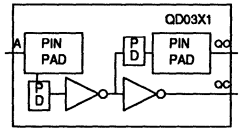
Max Delay (ns)		Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
From	To						
QO	QC	t_{PLH}	0.46	0.90	0.60	0.75	1.05
		t_{PHL}	0.48	0.97	0.63	0.80	1.12

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

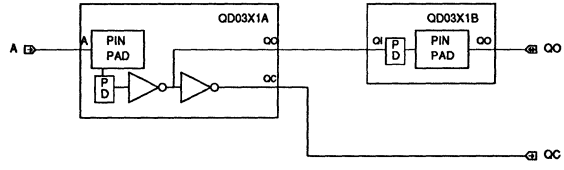
Description

QD03X1 is a 20 MHz (10MHz - 32MHz) cyrystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This macro is made up of two pad macros and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad macros.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Ci (pF)
A	3.17
QO	0.37

Equivalent Gates: 0
Bolt Syntax: .....QC QO .QD03X1A A ;
.....QI QO .QD03X1B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	27.8	nA
$^{\dagger}C_{pd}$	0.49	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
QO	QC	t_{PLH}	0.33	0.68	0.44	0.55	0.78
		t_{PHL}	0.45	0.83	0.59	0.73	1.01

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

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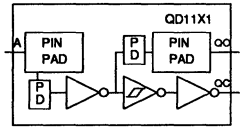
QD11X1

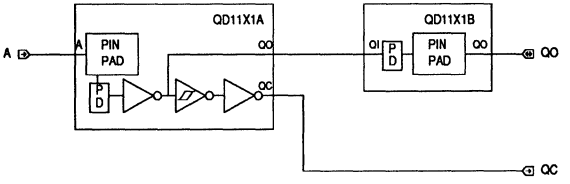
Description

QD11X1 is a 32K (1KHz - 1MHz) cyrystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This macro is made up of two pad macros and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad macros

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Ci (pF)
A	2.96
QO	0.29

Equivalent Gates: 0
Bolt Syntax: .....QC QO .QD11X1AA ;
.....QI QO .QD11X1B ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	29.0	nA
†C_{pd}	0.94	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
QO	QC	t_{PLH}	1.95	0.91	2.10	2.25	2.56
		t_{PHL}	1.68	0.78	1.80	1.94	2.20

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

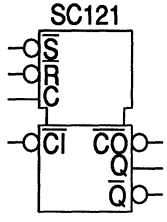
April, 1992

SC121

Description

SC121 is a static, master-slave,synchronous up counter-bit with ripple carry. SET and RESET are asynchronous and active low. Outputs are buffered. The output toggles on the rising edge of the clock when CIN is active low.

Logic Symbol



Truth Table

Truth Table Appears
On Page 3-220

Pin Loading

	Ci (pF)
C	0.23
SN	0.14
RN	0.14
CIN	0.14

Equivalent Gates: 16
Bolt Syntax: ..... CON Q QN .SC121 C CIN RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	126.3	nA
†C_{pd}	3.53	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
C	QN	t_{PLH}	1.88	1.22	2.08	2.29	2.70
		t_{PHL}	1.02	0.88	1.17	1.32	1.61
C	Q	t_{PLH}	0.54	1.18	0.72	0.93	1.32
		t_{PHL}	1.08	1.10	1.26	1.45	1.82
C	CON	t_{PLH}	1.87	1.23	2.07	2.28	2.70
		t_{PHL}	1.07	1.09	1.25	1.44	1.80
CIN	CON	t_{PLH}	0.37	1.23	0.56	0.78	1.19
		t_{PHL}	0.42	1.09	0.60	0.78	1.15
SN	Q	t_{PLH}	1.54	1.18	1.73	1.93	2.32
SN	QN	t_{PHL}	0.68	0.88	0.82	0.97	1.26
SN	CON	t_{PHL}	0.73	1.09	0.90	1.09	1.46
RN	Q	t_{PHL}	1.48	1.10	1.66	1.85	2.22
RN	QN	t_{PLH}	2.28	1.22	2.48	2.69	3.09
RN	CON	t_{PLH}	2.27	1.23	2.47	2.68	3.10
Min C Width	High	t_w	1.59				
Min C Width	Low	t_w	1.16				
Min RN Width		t_w	1.99				
Min SN Width		t_w	1.21				
Min CIN Setup		t_{su}	1.44				
Min CIN Hold		t_h	0.00				
Min SN Setup		t_{su}	0.27				
Min SN Hold		t_h	0.19				
Min RN Setup		t_{su}	0.85				
Min RN Hold		t_h	0.67				

Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

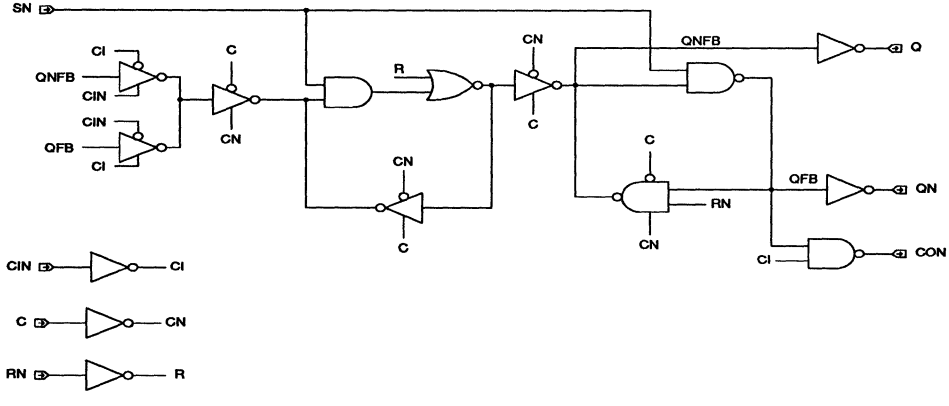
ASIC Functions

Truth Table.

RN	SN	CIN	C	CON(n+1)	Q(n+1)	QN(n+1)
L	L	X	X	-	IL	IL
L	H	X	X	-	L	H
H	L	X	X	-	H	L
H	H	L	↑	-	QN(n)	Q(n)
H	H	H	↑	-	NC	NC
X	X	L	X	QN(n+1)	-	-
X	X	H	X	H	-	-

NC = No Change
IL = Illegal

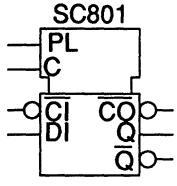
Logic Schematic



Description

SC801 is a static, master-slave, synchronous up-counter bit with ripple carry. The output toggles on the rising edge of the clock when CIN is active low. Parallel load is asynchronous and active high. Outputs are buffered.

Logic Symbol



Truth Table

Truth Table Appears On Page 3-223

Pin Loading

	Ci (pF)
DI	0.14
CIN	0.14
C	0.22
PL	0.14

Equivalent Gates: 15

Bolt Syntax: .....CON Q QN .SC801 C CIN DI PL ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	151.5	nA
†C_{pd}	3.94	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

ASIC Functions

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	1.89	1.21	2.08	2.29	2.70
		t_{PHL}	1.02	0.87	1.16	1.31	1.61
C	Q	t_{PLH}	0.55	1.19	0.74	0.94	1.34
		t_{PHL}	1.10	1.11	1.28	1.47	1.84
C	CON	t_{PLH}	1.88	1.23	2.08	2.29	2.70
		t_{PHL}	1.07	1.08	1.24	1.43	1.79
DI	Q	t_{PLH}	2.23	1.19	2.42	2.63	3.02
		t_{PHL}	2.05	1.11	2.23	2.42	2.79
DI	QN	t_{PLH}	2.84	1.21	3.03	3.24	3.65
		t_{PHL}	0.91	0.87	1.05	1.20	1.49
DI	CON	t_{PLH}	2.83	1.23	3.02	3.23	3.65
PL	Q	t_{PLH}	1.76	1.19	1.95	2.16	2.56
		t_{PHL}	1.81	1.11	1.99	2.18	2.55
PL	QN	t_{PLH}	2.59	1.21	2.79	2.99	3.40
		t_{PHL}	0.92	0.87	1.06	1.21	1.50
PL	CON	t_{PLH}	2.58	1.23	2.78	2.99	3.40
		t_{PHL}	0.96	1.08	1.14	1.32	1.69
CIN	CON	t_{PLH}	0.36	1.23	0.56	0.77	1.18
		t_{PHL}	0.42	1.08	0.59	0.78	1.14
Min C Width	High	t_w	1.60				
Min C Width	Low	t_w	1.16				
Min CIN Setup		t_{su}	1.67				
Min CIN Hold		t_h	0.00				
Min PL Width	High	t_w	2.30				
Min DI Setup to PL		t_s	0.39				
Min DI Hold to PL		t_h	2.30				

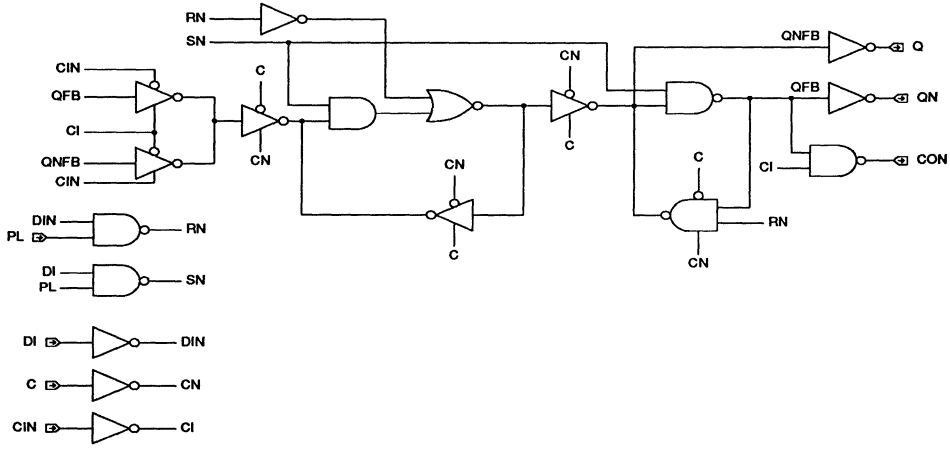
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Truth Table

DI	PL	CIN	C	CON	Q(n+1)	QN(n+1)
X	L	H	↑	-	NC	NC
X	L	L	↑	-	QN(n)	Q(n)
L	H	X	X	-	L	H
H	H	X	X	-	H	L
X	X	H	X	H	-	-
X	X	L	X	QN(n+1)	-	-

NC = No Change

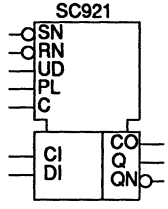
Logic Schematic



Description

SC921 is a static, master-slave, synchronous up/down-counter bit with ripple carry. The output toggles on the rising edge of the clock when CI is active high. Set and Reset are asynchronous and active low. Parallel load is asynchronous and active high. Outputs are buffered.

Logic Symbol



Truth Table

Truth Table Appears
On Page 3-226

Pin Loading

	Ci (pF)
DI	0.07
CI	0.21
C	0.22
PL	0.14
UD	0.14
RN	0.14
SN	0.14

Equivalent Gates: 19
Bolt Syntax: .....CO Q QN .SC921 C CI DI PL UD RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	193.6	nA
†C_{pd}	4.96	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan Outs 2 (0.16pF)	4 (0.33pF)	8 (0.67pF)
C	QN	t_{PLH}	2.06	1.20	2.25	2.46	2.86
		t_{PHL}	1.11	0.87	1.24	1.39	1.69
C	Q	t_{PLH}	0.62	1.21	0.82	1.03	1.43
		t_{PHL}	1.22	1.18	1.41	1.62	2.01
C	CO	t_{PLH}	1.50	1.13	1.68	1.87	2.25
		t_{PHL}	2.00	0.69	2.11	2.23	2.46
CI	CO	t_{PLH}	0.35	1.13	0.53	0.73	1.11
		t_{PHL}	0.34	0.69	0.45	0.57	0.80
UD	CO	t_{PLH}	1.07	1.13	1.26	1.45	1.83
		t_{PHL}	0.87	0.69	0.98	1.10	1.33
RN	Q	t_{PHL}	1.65	1.18	1.84	2.04	2.44
RN	QN	t_{PLH}	2.51	1.20	2.70	2.91	3.31
SN	Q	t_{PLH}	1.58	1.21	1.78	1.99	2.39
SN	QN	t_{PHL}	0.63	0.87	0.77	0.92	1.21
Min C Width	High	t_w	1.78				
Min C Width	Low	t_w	1.16				
Min RN Width		t_w	2.19				
Min SN Width		t_w	1.23				
Min CI Setup		t_{su}	2.03				
Min CI Hold		t_h	0.00				
Min CI Setup to PL		t_s	1.20				
Min DI Setup		t_{su}	1.71				
Min DI Hold		t_h	0.00				
Min DI Setup to PL		t_s	0.39				
MinPL Setup		t_{su}	1.41				
Min PL Hold		t_h	0.00				
Min RN Setup		t_{su}	0.84				
Min RN Hold		t_h	0.70				
Min SN Setup		t_{su}	0.27				
Min SN Hold		t_h	0.20				

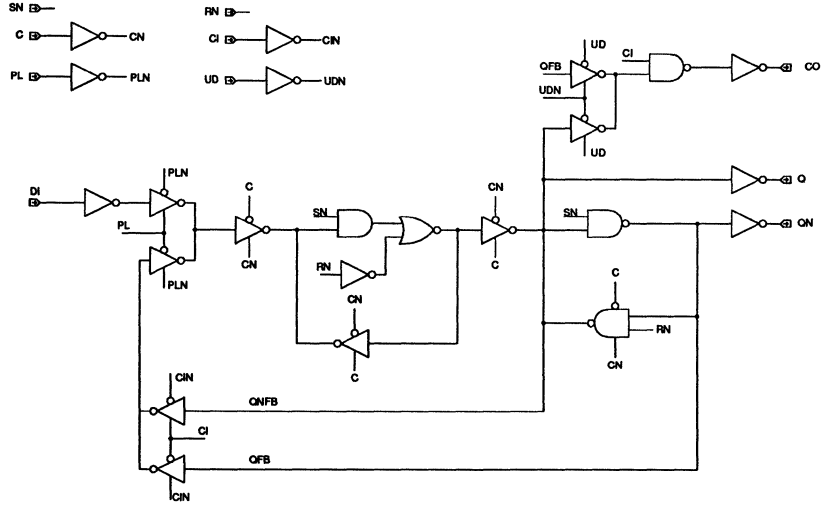
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Truth Table

RN	SN	CI	UD	PL	DI	C	CO	Q(n+1)	QN(n+1)
H	H	X	X	H	L	↑	-	L	H
H	H	X	X	H	H	↑	-	H	L
H	H	X	X	X	X	L	-	NC	NC
H	H	L	X	L	X	↑	-	NC	NC
H	H	H	X	L	X	↑	-	QN(n)	Q(n)
L	H	X	X	X	X	X	-	L	H
H	L	X	X	X	X	X	-	H	L
L	L	X	X	X	X	X	-	IL	IL
X	X	L	X	X	X	X	L	-	-
X	X	H	H	X	X	X	Q(n)	-	-
X	X	H	L	X	X	X	QN(n)	-	-

NC = No Change
IL = Illegal

Logic Schematic



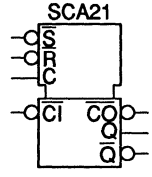
April, 1992

SCA21

Description

SCA21 is a static, master-slave,synchronous up counter-bit with ripple carry. SET and RESET are asynchronous and active low. Outputs are buffered. The output toggles on the rising edge of the clock when CIN is active low. Equivalent to SC121 with transmission gates.

Logic Symbol



Truth Table

Truth Table Appears
On Page 3-229

Pin Loading

	Ci (pF)
C	0.22
SN	0.14
RN	0.14
CIN	0.14

Equivalent Gates: 12

Bolt Syntax: ..... CON Q QN .SCA21 C CIN RN SN ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^oC$	92.7	nA
†C_{pd}	2.60	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

ASIC Functions

Delay Characteristics:

Conditions: T_J = 25C, V_{DD} = 5.0V, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
C	QN	t_{PLH}	1.40	1.18	1.59	1.79	2.19
		t_{PHL}	1.47	0.83	1.60	1.75	2.03
C	Q	t_{PLH}	1.02	1.16	1.21	1.41	1.80
		t_{PHL}	0.79	0.81	0.92	1.06	1.33
C	CON	t_{PLH}	1.40	1.20	1.59	1.79	2.19
		t_{PHL}	1.52	1.04	1.68	1.86	2.21
CIN	CON	t_{PLH}	0.37	1.20	0.56	0.76	1.16
		t_{PHL}	0.40	1.04	0.57	0.74	1.09
SN	Q	t_{PLH}	1.56	1.18	1.74	1.94	2.33
SN	QN	t_{PHL}	0.84	0.83	0.97	1.11	1.39
SN	CON	t_{PHL}	0.91	1.04	1.07	1.25	1.60
RN	Q	t_{PHL}	0.59	0.81	0.72	0.86	1.13
RN	QN	t_{PLH}	1.43	1.18	1.62	1.82	2.22
RN	CON	t_{PLH}	1.43	1.20	1.62	1.82	2.22
Min C Width	High	t_w	1.37				
Min C Width	Low	t_w	1.02				
Min RN Width		t_w	1.20				
Min SN Width		t_w	1.29				
Min CIN Setup		t_{su}	1.84				
Min CIN Hold		t_h	0.00				
Min SN Setup		t_{su}	0.54				
Min SN Hold		t_h	0.17				
Min RN Setup		t_{su}	0.20				
Min RN Hold		t_h	0.00				

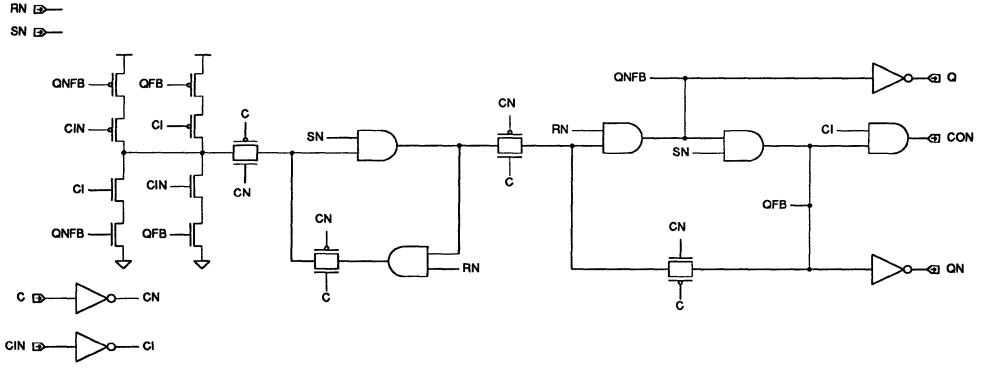
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

Truth Table

RN	SN	CIN	C	CON(n+1)	Q(n+1)	QN(n+1)
L	L	X	X	-	IL	IL
L	H	X	X	-	L	H
H	L	X	X	-	H	L
H	H	L	↑	-	QN(n)	Q(n)
H	H	H	↑	-	NC	NC
X	X	L	X	QN(n+1)	-	-
X	X	H	X	H	-	-

NC = No Change
IL = Illegal

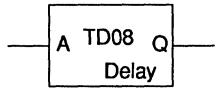
Logic Schematic



Description

TD08 is a non-inverting time delay.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.26

Equivalent Gates: 12
Bolt Syntax: .....Q .TD08 A ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} $T_J = 85^{\circ}C$	84.3	nA
†C_{pd}	3.35	pF

Power = (Static I_{DD}) (V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: $T_J = 25C$, $V_{DD} = 5.0V$, Typical Process

Max Delay (ns)		Parameter	t_{dx}	k_{tdx}	Number of Fan Outs		
					2	4	8
From	To		(ns)	(ns/pF)	(0.16pF)	(0.33pF)	(0.67pF)
A	Q	t_{PLH}	6.29	0.45	6.36	6.44	6.59
		t_{PHL}	6.55	0.39	6.61	6.68	6.81

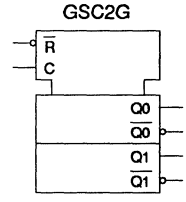
Propagation Delay Equation: $t_p(C_L) = K_{PV} K_T(t_{dx} + k_{tdx}C_L)$

SECTION 4

MSI FUNCTIONS

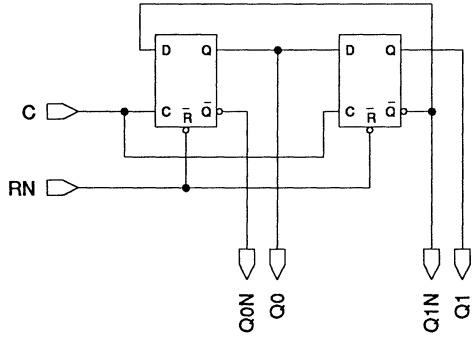
April, 1992

GSC2G



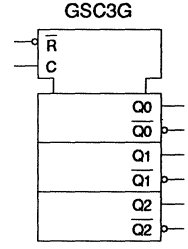
Description: GSC2G is a modulo 4 gray counter, with reset not.
Equivalent Gate Count: 12
Bolt Syntax: Q0 Q0N Q1 Q1N .GSC2G C RN ;

Logic Schematic:



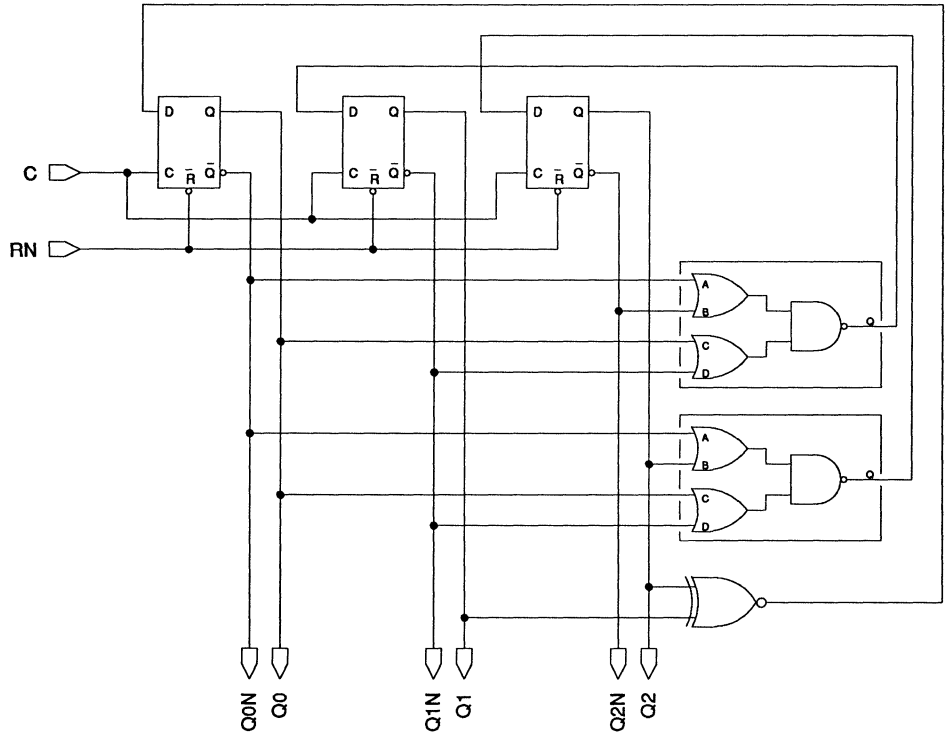
April, 1992

GSC3G



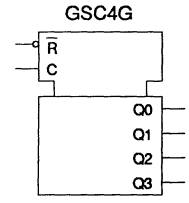
Description: GSC3G is a modulo 8 gray counter, with reset not.
Equivalent Gate Count: 25
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N .GSC3G C RN ;

Logic Schematic:



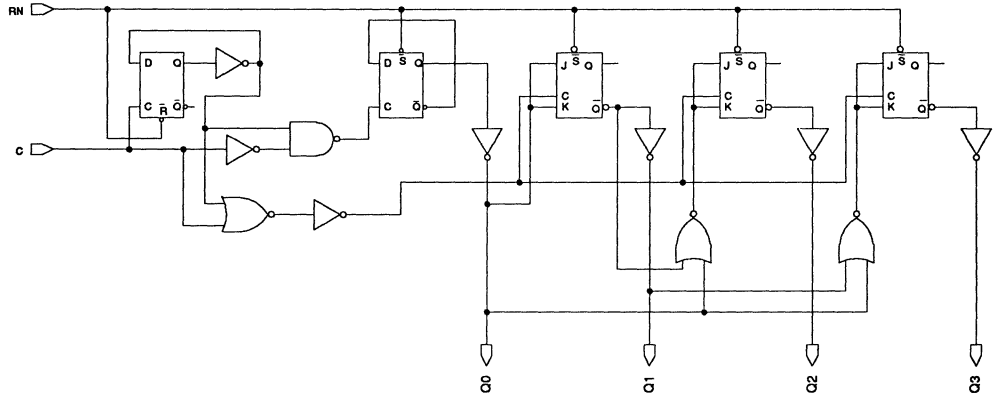
April, 1992

GSC4G



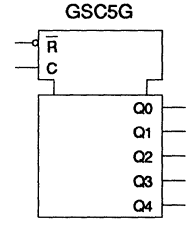
Description: GSC4G is a modulo 16 gray counter, with reset not.
Equivalent Gate Count: 50
Bolt Syntax: Q0 Q1 Q2 Q3 .GSC4G C RN ;

Logic Schematic:



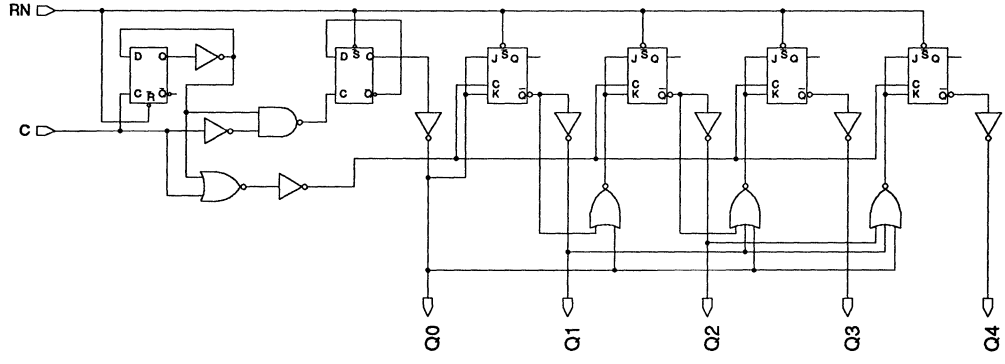
April, 1992

GSC5G



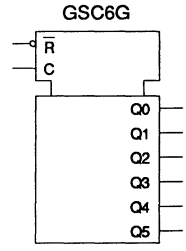
Description: GSC5G is a modulo 32 gray counter, with reset not.
Equivalent Gate Count: 63
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSC5G C RN ;

Logic Schematic:



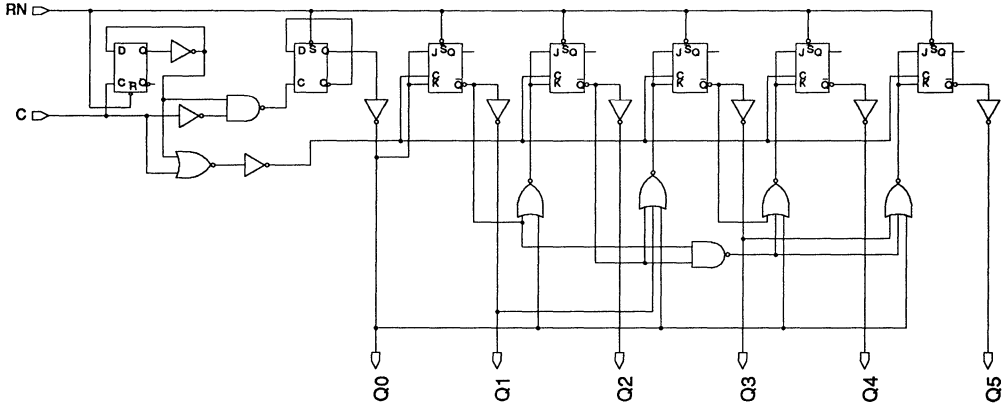
April, 1992

GSC6G



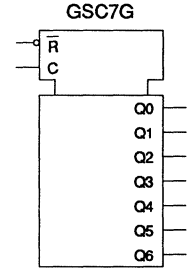
Description: GSC6G is a modulo 64 gray counter, with reset not.
Equivalent Gate Count: 76
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 .GSC6G C RN ;

Logic Schematic:



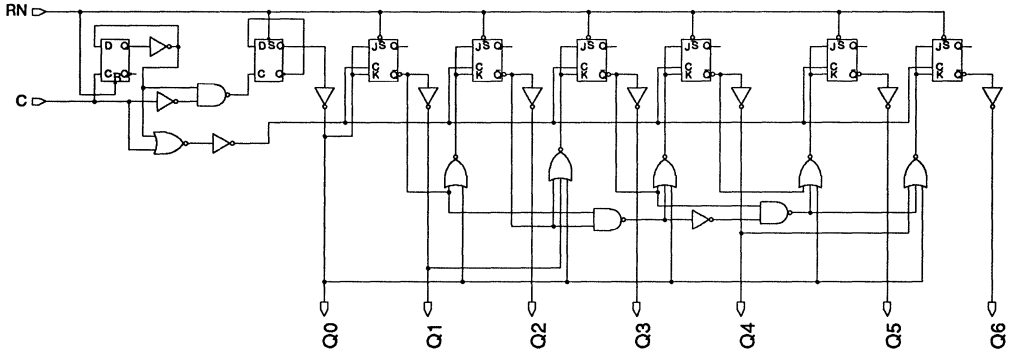
April, 1992

GSC7G



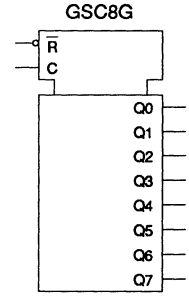
Description: GSC7G is a modulo 128 gray counter, with reset not.
Equivalent Gate Count: 90
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 .GSC7G C RN ;

Logic Schematic:



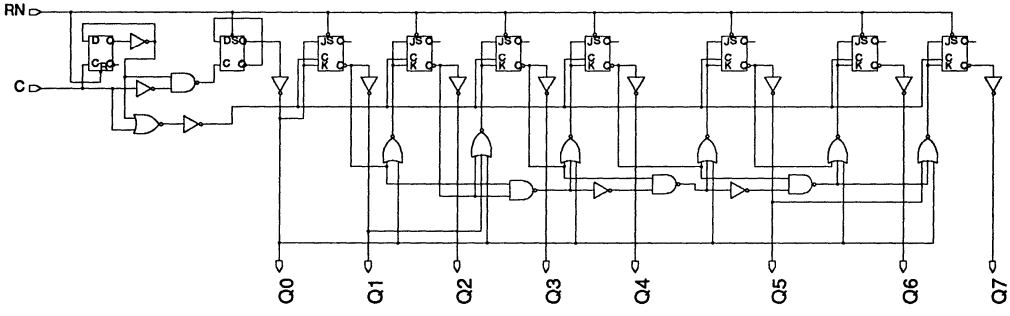
April, 1992

GSC8G



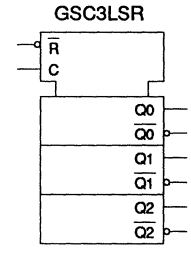
Description: GSC8G is a modulo 256 gray counter, with reset not.
Equivalent Gate Count: 104
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 .GSC8G C RN ;

Logic Schematic:



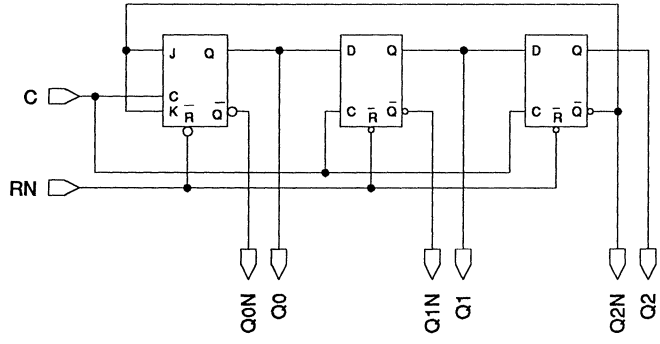
April, 1992

GSC3LSR



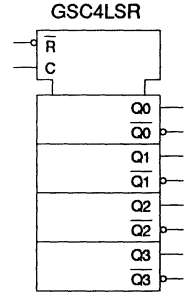
Description: GSC3LSR is a 3 bit modulo 7 linear feedback shift register, with reset not.
Equivalent Gate Count: 22
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N .GSC3LSR C RN ;

Logic Schematic:



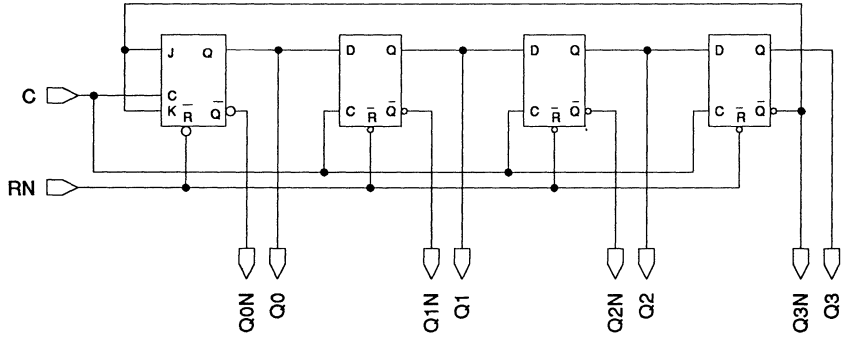
April, 1992

GSC4LSR



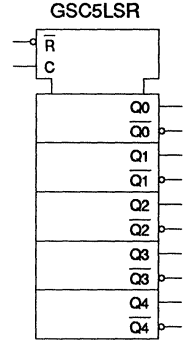
Description: GSC4LSR is a 4 bit modulo 15 linear feedback shift register, with reset not.
Equivalent Gate Count: 28
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSC4LSR C RN ;

Logic Schematic:



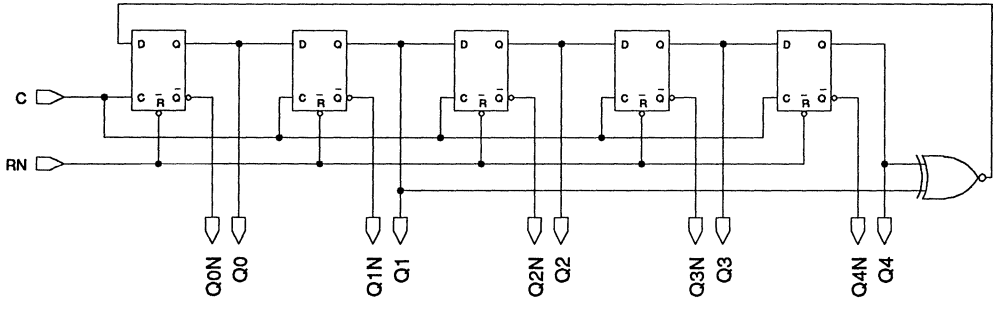
April, 1992

GSC5LSR



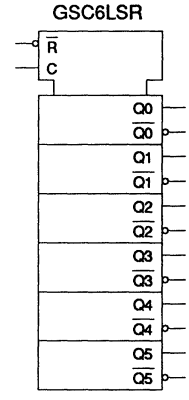
Description: GSC5LSR is a 5 bit modulo 31 linear feedback shift register, with reset not.
Equivalent Gate Count: 33
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N .GSC5LSR C RN ;

Logic Schematic:



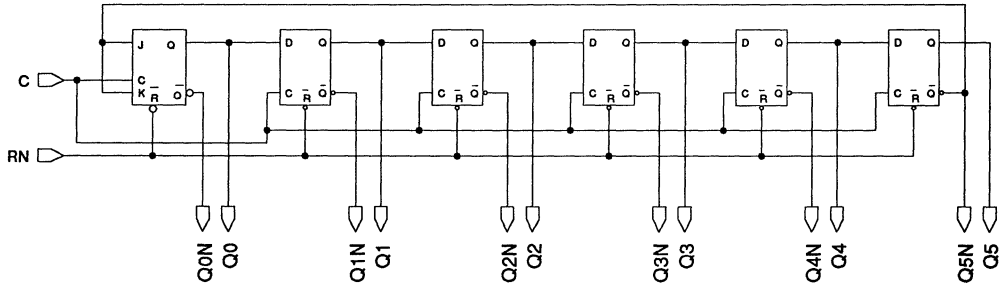
April, 1992

GSC6LSR



Description: GSC6LSR is a 6 bit modulo 63 linear feedback shift register, with reset not.
Equivalent Gate Count: 40
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N .GSC6LSR C RN ;

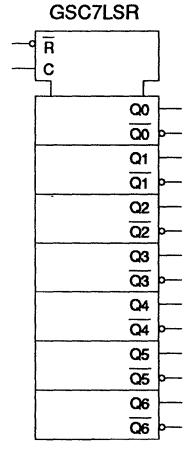
Logic Schematic:



MSI Functions

April, 1992

GSC7LSR

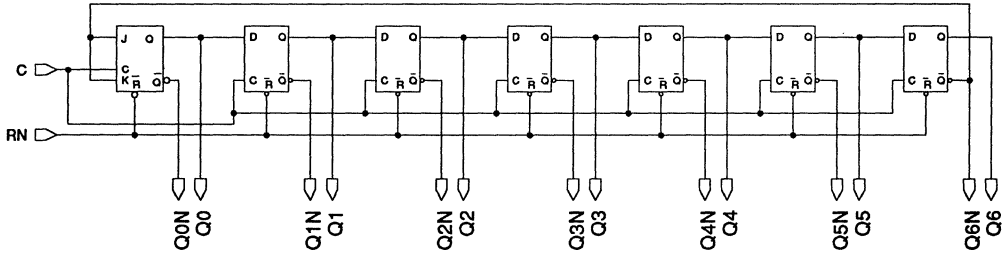


Description: GSC7LSR is a 7 bit modulo 127 polynomial counter with reset not.

Equivalent Gate Count: 46

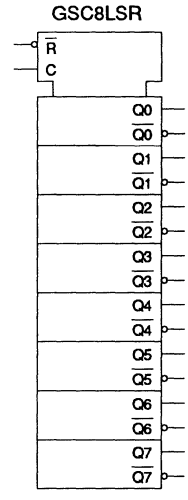
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N .GSC7LSR C RN ;

Logic Schematic:



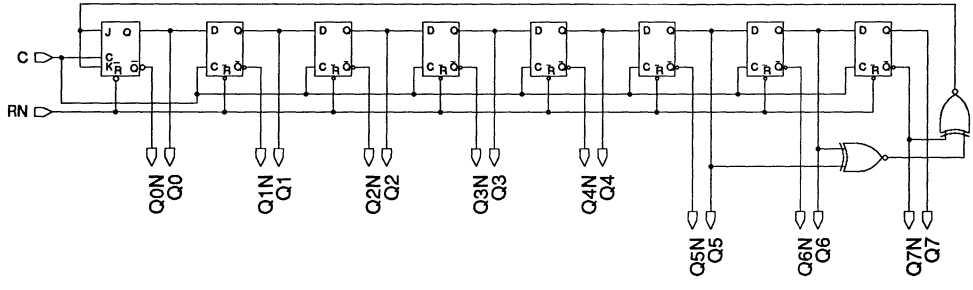
April, 1992

GSC8LSR



Description: GSC8LSR is a 8 bit modulo 255 polynomial counter, with reset not.
Equivalent Gate Count: 58
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N
.GSC8LSR C RN ;

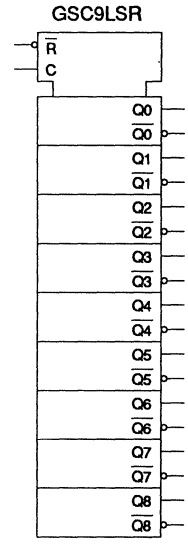
Logic Schematic:



MSI Functions

April, 1992

GSC9LSR

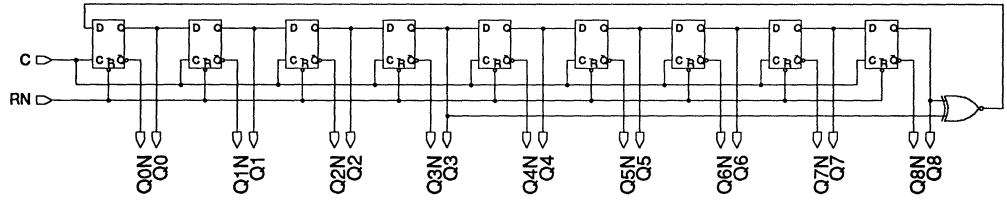


Description: GSC9LSR is a 9 bit modulo 511 polynomial counter, with reset not.

Equivalent Gate Count: 57

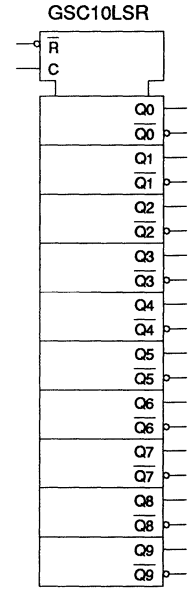
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N .GSC9LSR C RN ;

Logic Schematic:



April, 1992

GSC10LSR

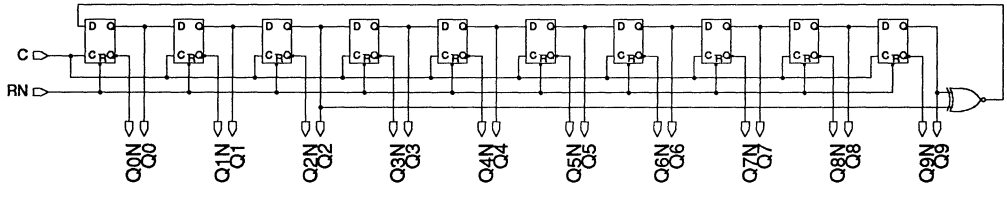


Description: GSC10LSR is a 10 bit modulo 1023 polynomial counter, with reset not.

Equivalent Gate Count: 63

Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N Q9 Q9N .GSC10LSR C RN ;

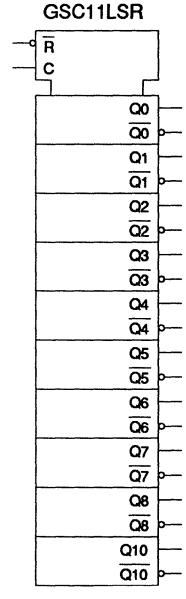
Logic Schematic:



MSI Functions

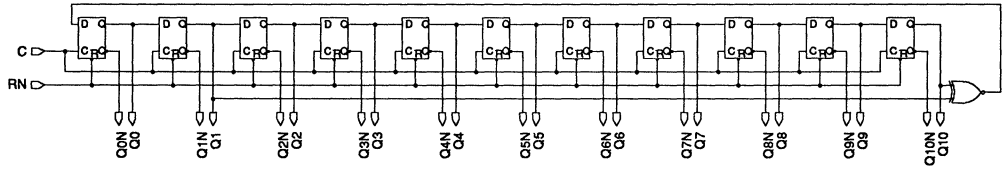
April, 1992

GSC11LSR



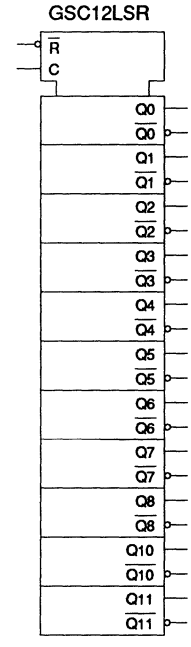
Description: GSC11LSR is a 11 bit modulo 2047 polynomial counter, with reset not.
Equivalent Gate Count: 69
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N Q9 Q9N Q10 Q10N .GSC11LSR C RN ;

Logic Schematic:



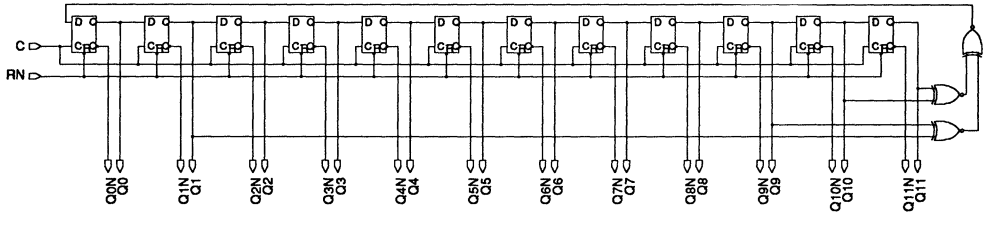
April, 1992

GSC12LSR



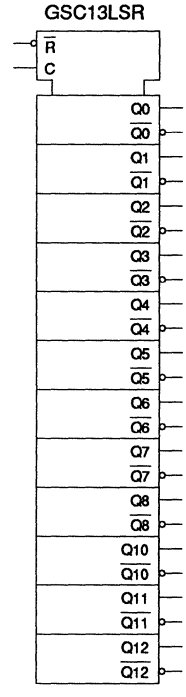
Description: GSC12LSR is a 12 bit modulo 4095 polynomial counter, with reset not.
Equivalent Gate Count: 81
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N Q9 Q9N Q10 Q10N Q11 Q11N .GSC12LSR C RN ;

Logic Schematic:



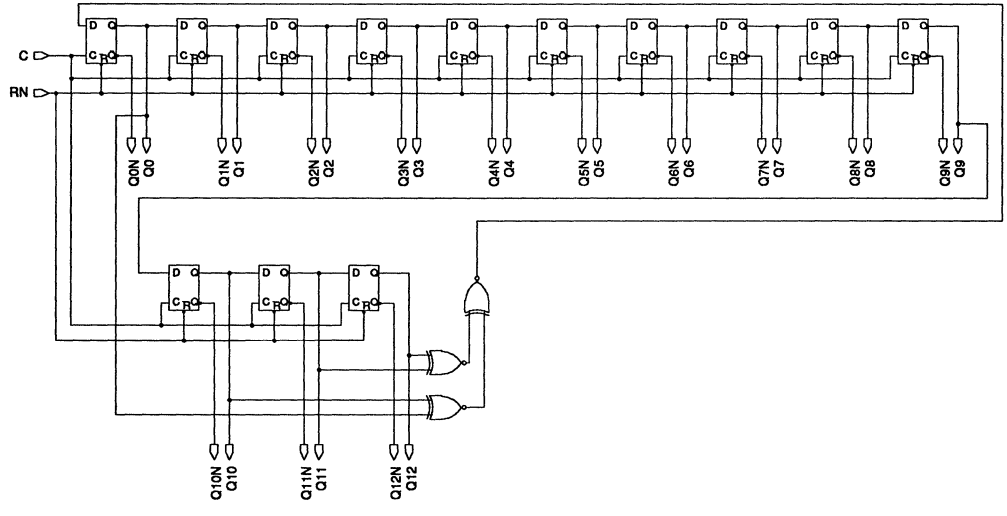
April, 1992

GSC13LSR



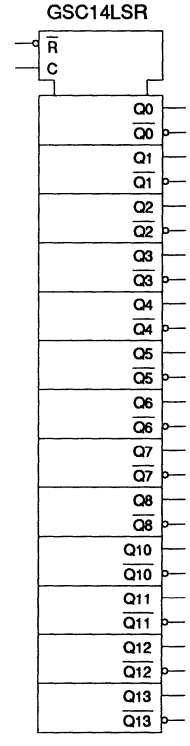
Description: GSC13LSR is a 13 bit modulo 8191 polynomial counter, with reset not.
Equivalent Gate Count: 87
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N Q9 Q9N Q10 Q10N Q11 Q11N Q12 Q12N .GSC12LSR C RN ;

Logic Schematic:



April, 1992

GSC14LSR

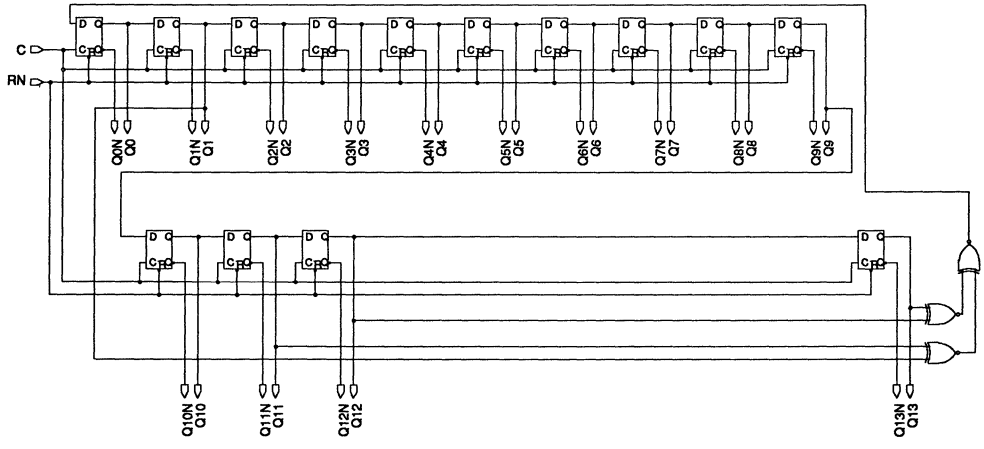


Description: GSC14LSR is a 14 bit modulo 16383 polynomial counter, with reset not.

Equivalent Gate Count: 93

Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N Q9 Q9N Q10 Q10N Q11 Q11N Q12 Q12N Q13 Q13N .GSC14LSR C RN ;

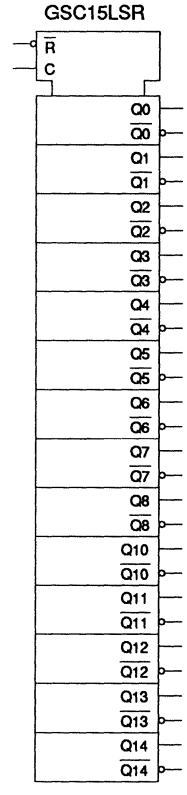
Logic Schematic:



MSI Functions

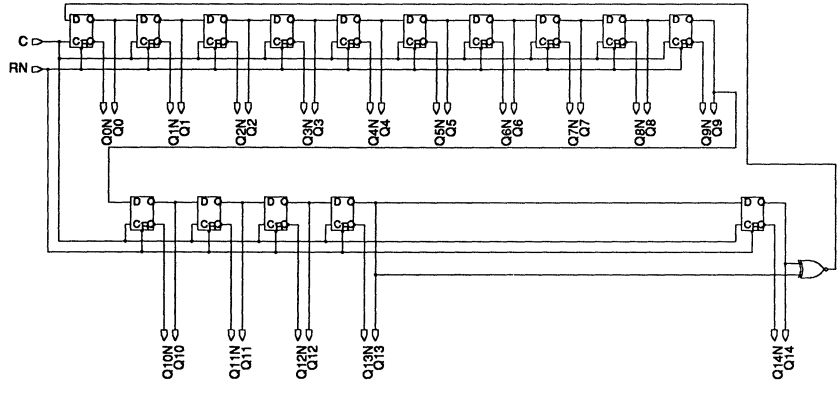
April, 1992

GSC15LSR



Description: GSC15LSR is a 15 bit modulo 32767 polynomial counter, with reset not.
Equivalent Gate Count: 93
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8
Q8N Q9 Q9N Q10 Q10N Q11 Q11N Q12 Q12N Q13 Q13N Q14 Q14N
.GSC15LSR C RN ;

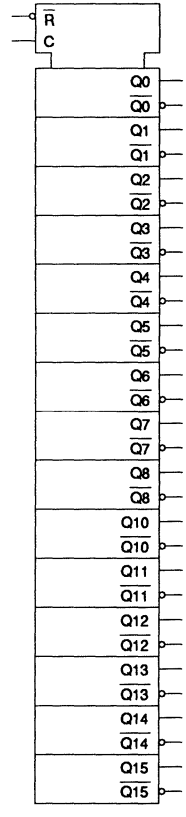
Logic Schematic:



April, 1992

GSC16LSR

GSC16LSR

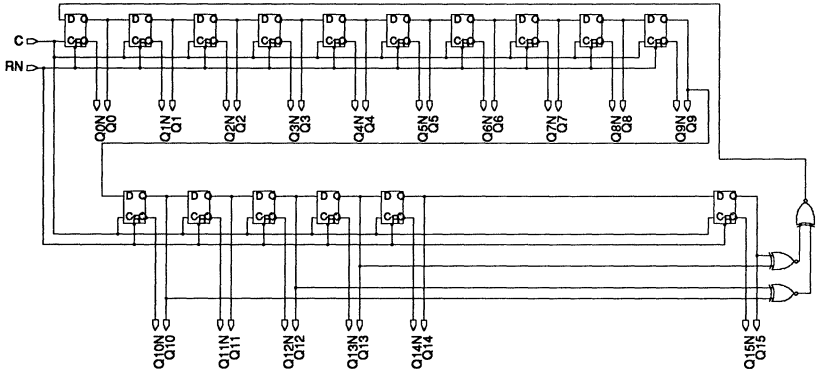


Description: GSC16LSR is a 16 bit modulo 65535 polynomial counter, with reset not.

Equivalent Gate Count: 105

Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N Q9 Q9N Q10 Q10N Q11 Q11N Q12 Q12N Q13 Q13N Q14 Q14N Q15 Q15N .GSC16LSR C RN ;

Logic Schematic:



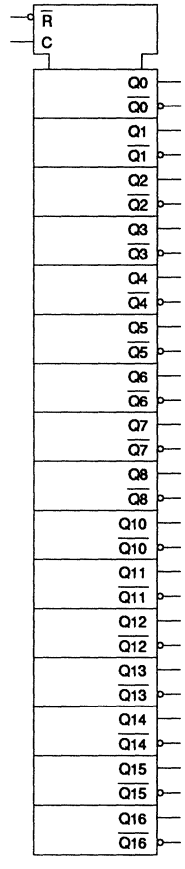
MSI Functions

April, 1992

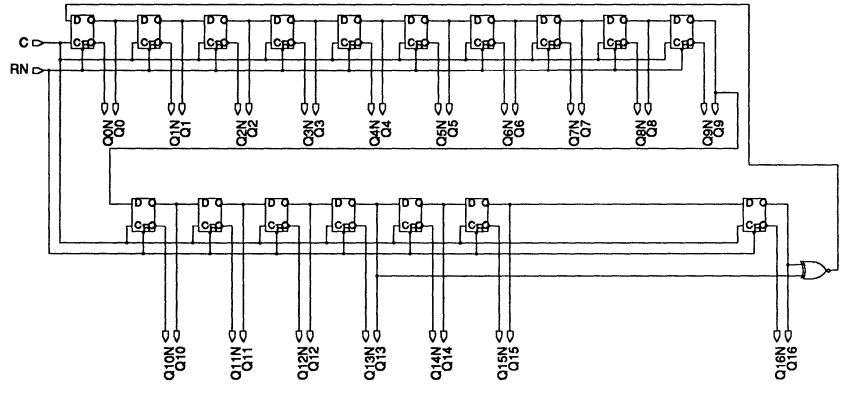
GSC17LSR

Description: GSC17LSR is a 17 bit modulo 131071 polynomial counter, with reset not.
Equivalent Gate Count: 105
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N Q9 Q9N Q10 Q10N Q11 Q11N Q12 Q12N Q13 Q13N Q14 Q14N Q15 Q15N Q16 Q16N .GSC17LSR C RN ;

GSC17LSR

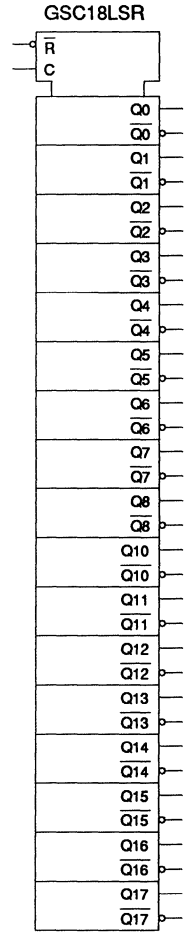


Logic Schematic:



April, 1992

GSC18LSR

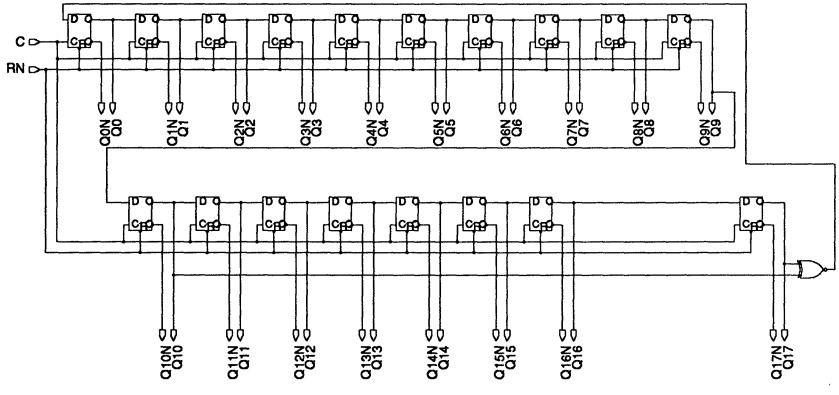


Description: GSC18LSR is a 18 bit modulo 262143 polynomial counter, with reset not.

Equivalent Gate Count: 111

Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N Q9 Q9N Q10 Q10N Q11 Q11N Q12 Q12N Q13 Q13N Q14 Q14N Q15 Q15N Q16 Q16N Q17 Q17N .GSC18LSR C RN ;

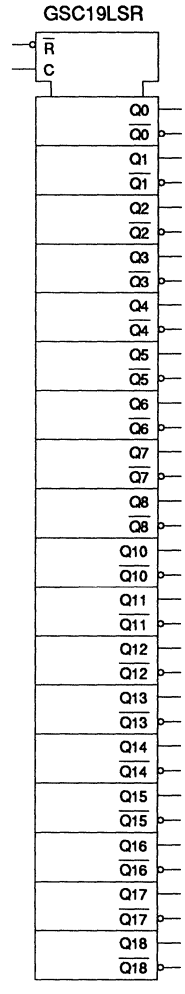
Logic Schematic:



MSI Functions

April, 1992

GSC19LSR

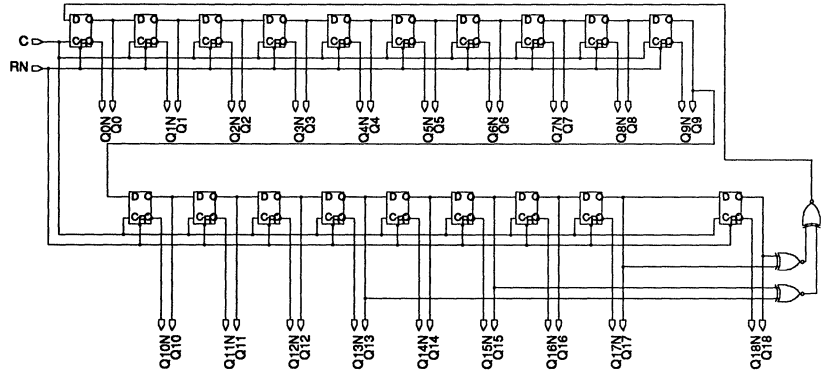


Description: GSC19LSR is a 19 bit modulo 524287 polynomial counter, with reset not.

Equivalent Gate Count: 123

Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N Q9 Q9N Q10 Q10N Q11 Q11N Q12 Q12N Q13 Q13N Q14 Q14N Q15 Q15N Q16 Q16N Q17 Q17N Q18 Q18N .GSC19LSR C RN ;

Logic Schematic:



April, 1992

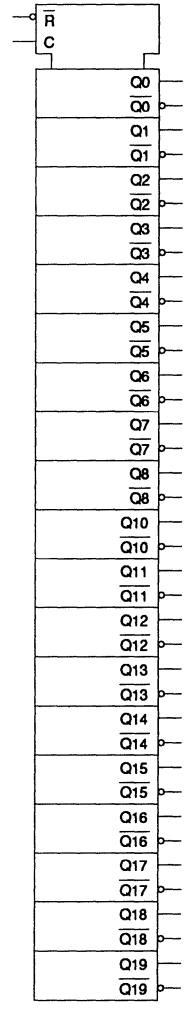
GSC20LSR

Description: GSC20LSR is a 20 bit modulo 1040575 polynomial counter, with reset not.

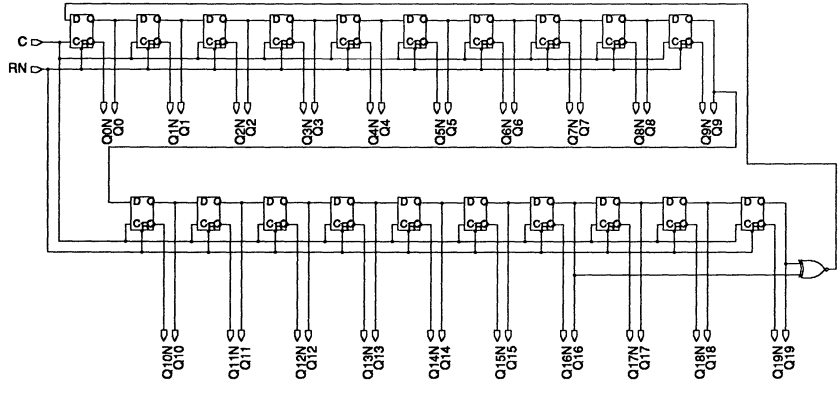
Equivalent Gate Count: 123

Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N Q8 Q8N Q9 Q9N Q10 Q10N Q11 Q11N Q12 Q12N Q13 Q13N Q14 Q14N Q15 Q15N Q16 Q16N Q17 Q17N Q18 Q18N Q19 Q19N .GSC20LSR C RN ;

GSC20LSR



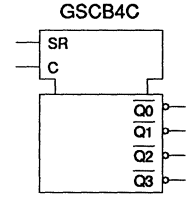
Logic Schematic:



MSI Functions

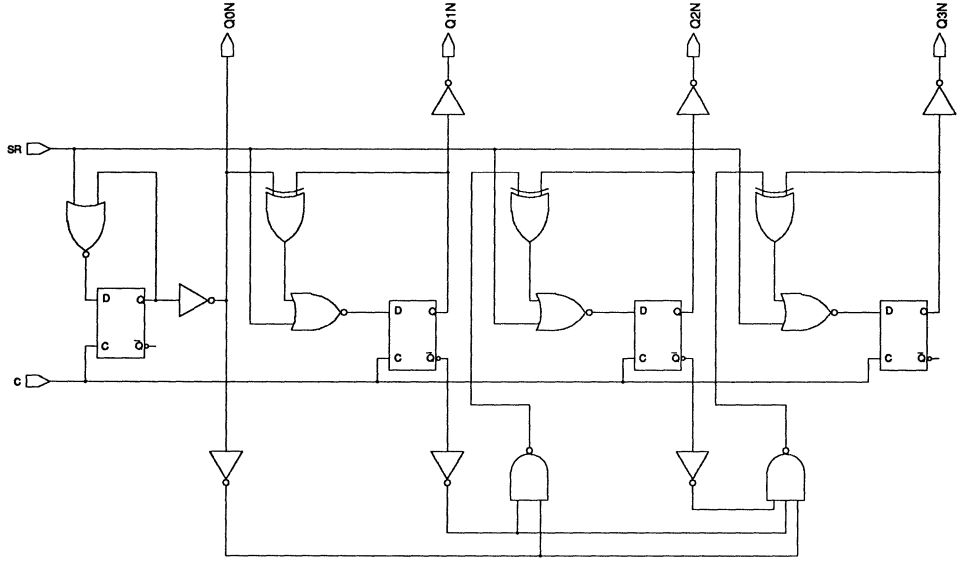
April, 1992

GSCB4C



Description: GSCB4C is a fast 4 bit binary up counter, with synchronous reset.
Equivalent Gate Count: 43
Bolt Syntax: Q0N Q1N Q2N Q3N .GSCB4C SR C ;

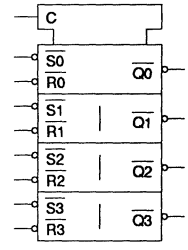
Logic Schematic:



April, 1992

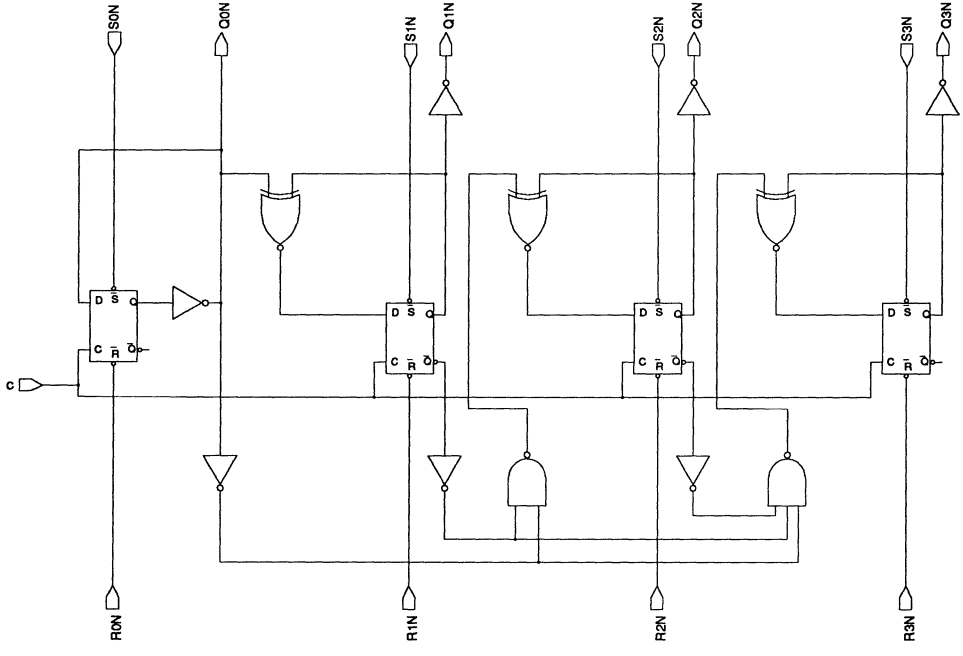
GSCB4F

GSCB4F



Description: GSCB4F is a fast 4 bit binary up counter, with individual set not and reset not.
Equivalent Gate Count: 47
Bolt Syntax: Q0N Q1N Q2N Q3N .GSCB4F C R0N R1N R2N R3N S0N S1N S2N S3N ;

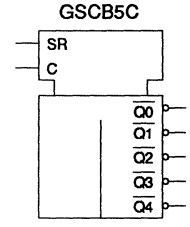
Logic Schematic:



MSI Functions

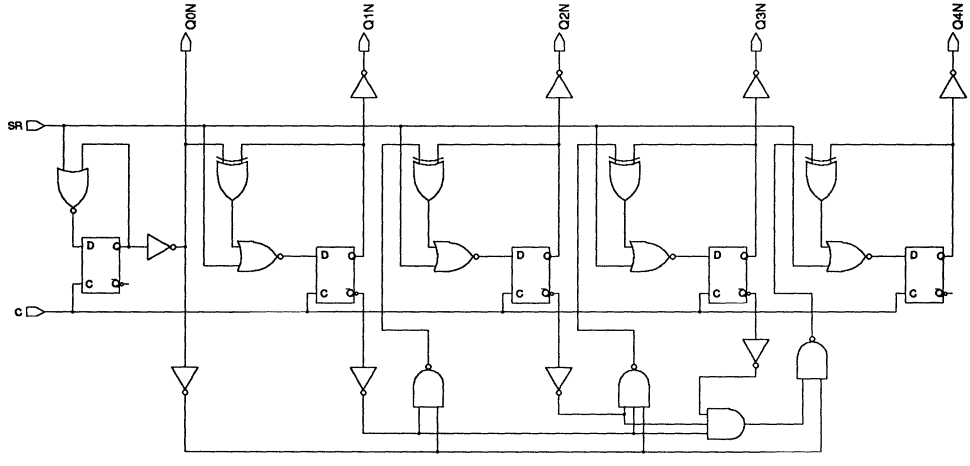
April, 1992

GSCB5C



Description: GSCB5C is a fast 5 bit binary up counter, with synchronous reset.
Equivalent Gate Count: 57
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N .GSCB5C SR C ;

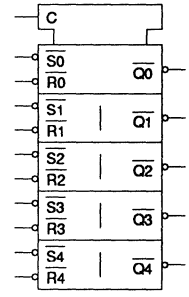
Logic Schematic:



April, 1992

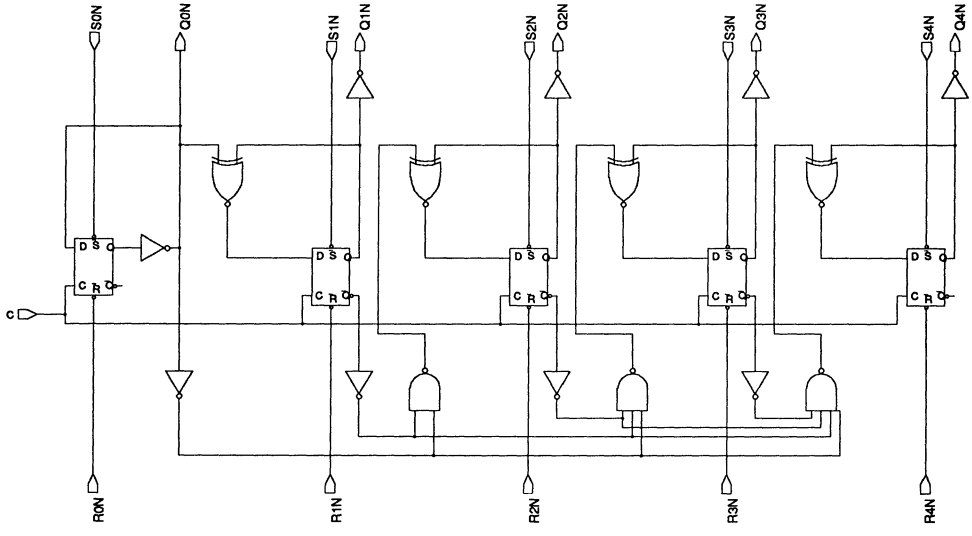
GSCB5F

GSCB5F



Description: GSCB5F is a fast 5 bit binary up counter, with individual set not and reset not.
Equivalent Gate Count: 63
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N .GSCB5F C R0N R1N R2N R3N R4N S0N S1N S2N S3N S4N ;

Logic Schematic:

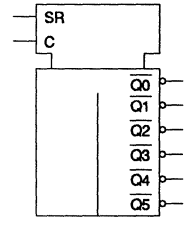


MSI Functions

April, 1992

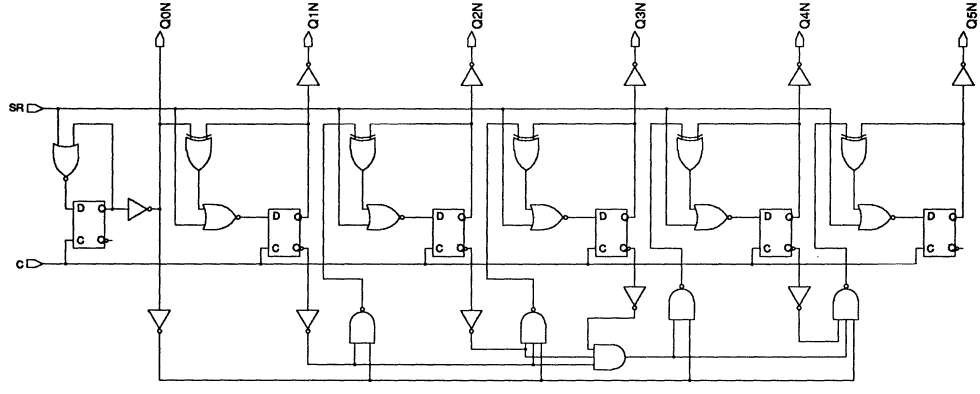
GSCB6C

GSCB6C



Description: GSCB6C is a fast 6 bit binary up counter, with synchronous reset.
Equivalent Gate Count: 70
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N .GSCB6C SR C ;

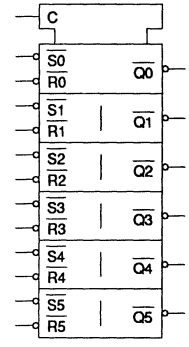
Logic Schematic:



April, 1992

GSCB6F

GSCB6F

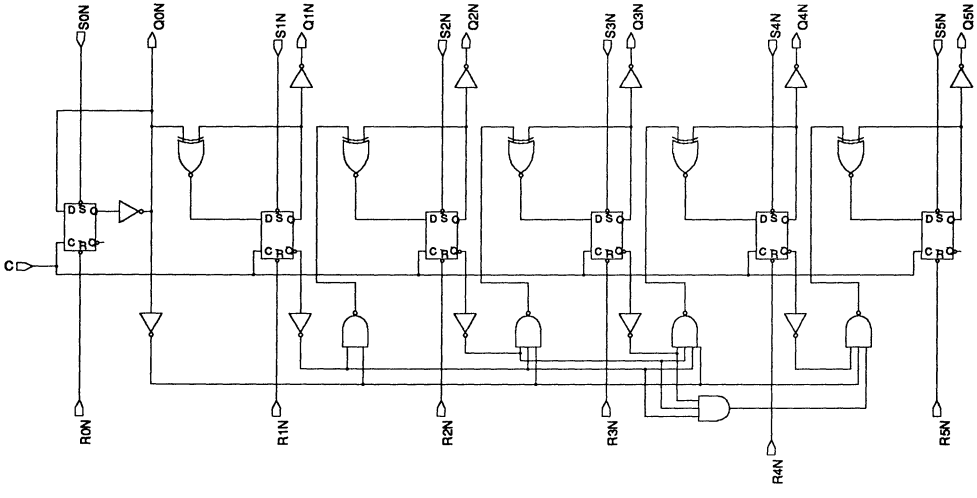


Description: GSCB6F is a fast 6 bit binary up counter, with individual set not and reset not.

Equivalent Gate Count: 77

Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N .GSCB6F C R0N R1N R2N R3N R4N R5N
S0N S1N S2N S3N S4N S5N ;

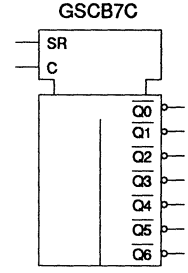
Logic Schematic:



MSI Functions

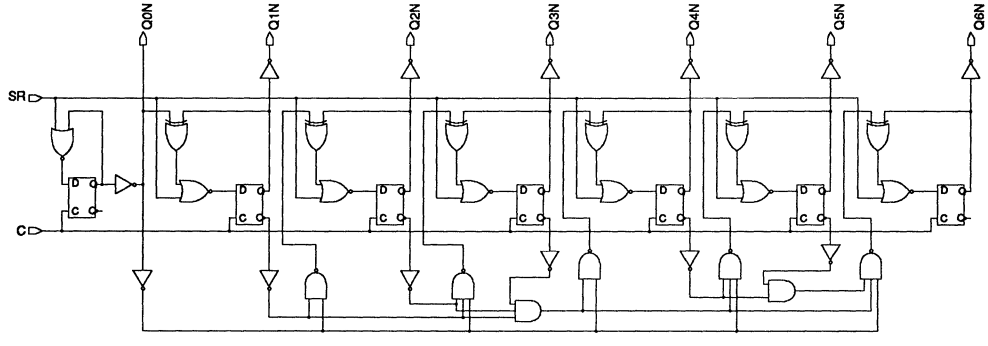
April, 1992

GSCB7C



Description: GSCB7C is a fast 7 bit binary up counter, with synchronous reset.
Equivalent Gate Count: 85
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N .GSCB7C SR C ;

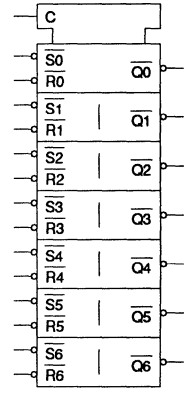
Logic Schematic:



April, 1992

GSCB7F

GSCB7F

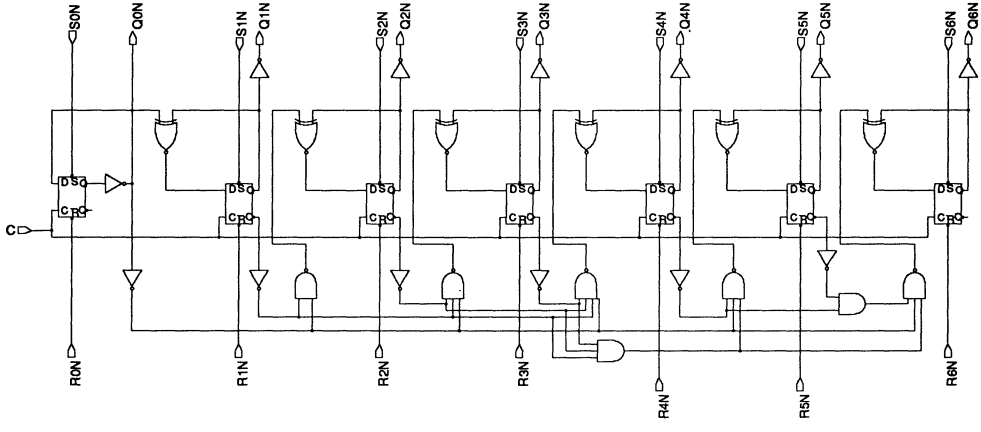


Description: GSCB7F is a fast 7 bit binary up counter, with individual set not and reset not.

Equivalent Gate Count: 93

Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N .GSCB7F C R0N R1N R2N R3N R4N R5N R6N S0N S1N S2N S3N S4N S5N S6N ;

Logic Schematic:



MSI Functions

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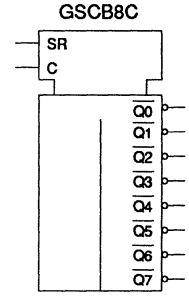
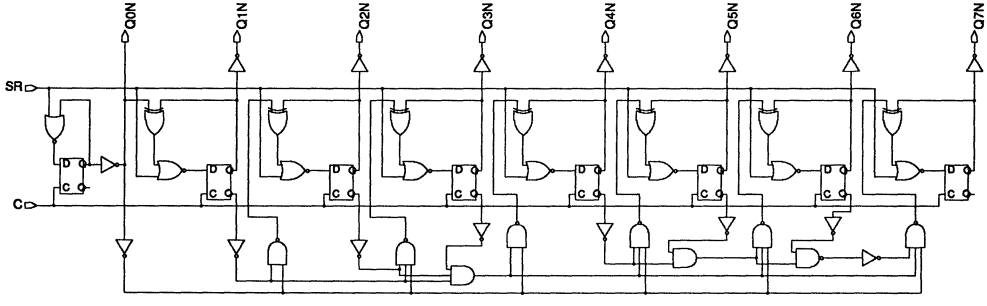
GSCB8C



Description: GSCB8C is a fast 8 bit binary up counter, with synchronous reset.
Equivalent Gate Count: 100
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N .GSCB8C SR C ;

Logic Schematic:



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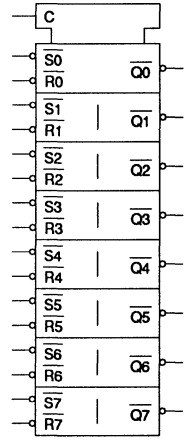
GSCB8F

Description: GSCB8F is a fast 8 bit binary up counter, with individual set not and reset not.

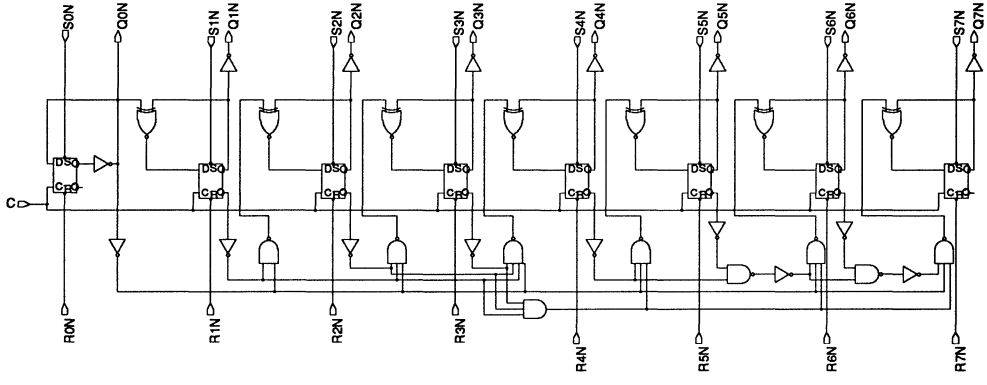
Equivalent Gate Count: 109

Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N .GSCB8F C R0N R1N R2N R3N R4N R5N R6N R7N S0N S1N S2N S3N S4N S5N S6N S7N ;

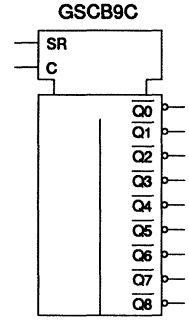
GSCB8F



Logic Schematic:

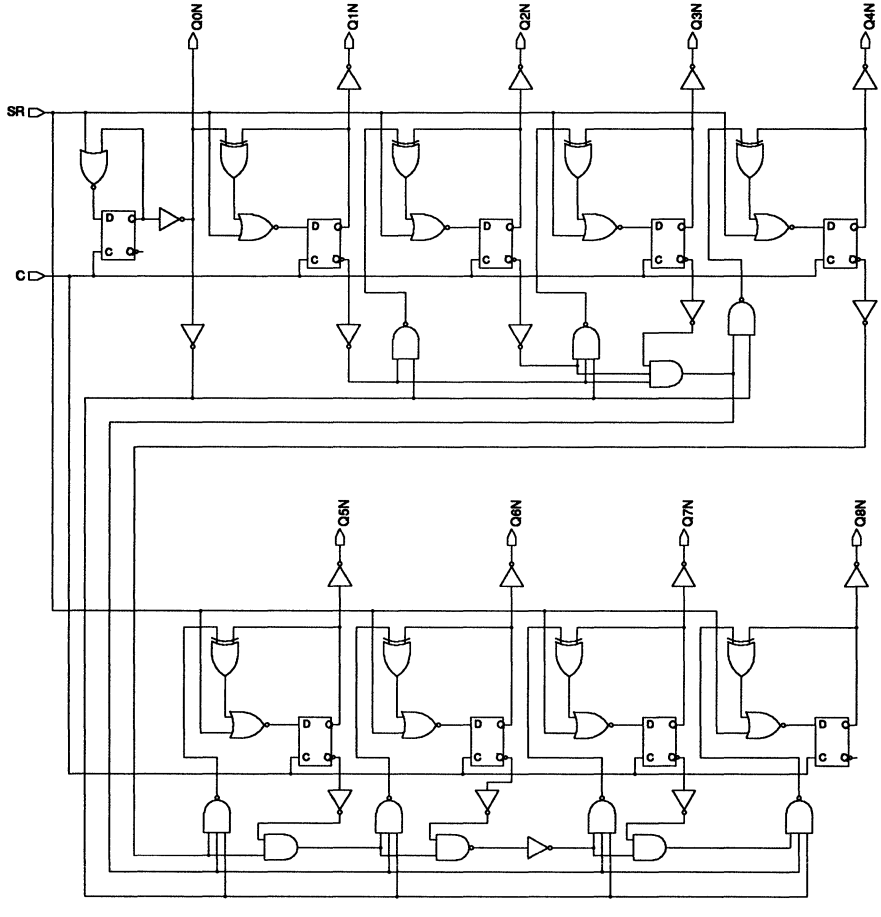


MSI Functions



Description: GSCB9C is a fast 9 bit binary up counter, with synchronous reset.
Equivalent Gate Count: 115
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N Q8N .GSCB9C SR C ;

Logic Schematic:



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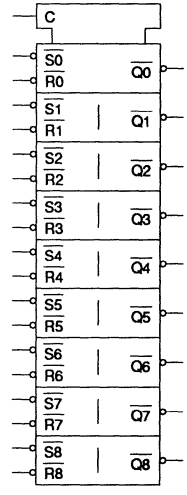
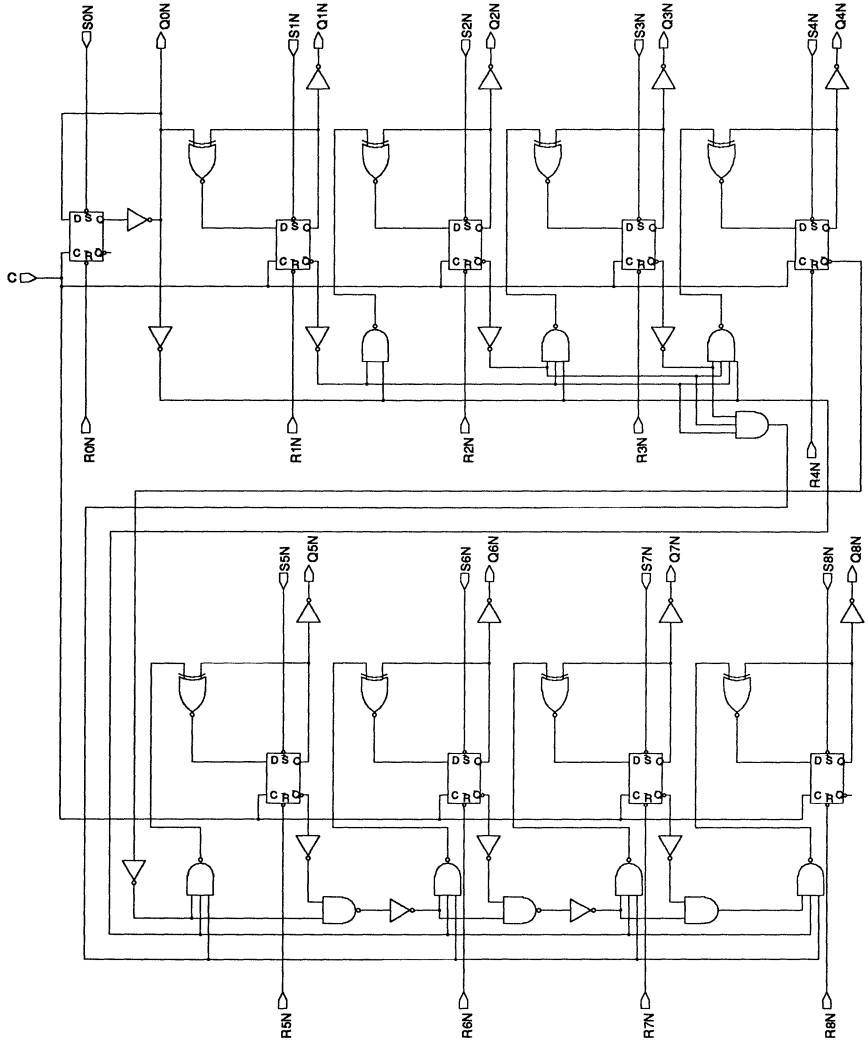
GSCB9F

Description: GSCB9F is a fast 9 bit binary up counter, with individual set not and reset not.
Equivalent Gate Count: 125
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N Q8N .GSCB9F C R0N R1N R2N R3N R4N R5N R6N R7N R8N S0N S1N S2N S3N S4N S5N S6N S7N S8N ;

GSCB9F



Logic Schematic: On Next Page


S0N
Q0N
S1N
Q1N
S2N
Q2N
S3N
Q3N
S4N
Q4N
C
R0N
R1N
R2N
R3N
R4N
S5N
Q5N
S6N
Q6N
S7N
Q7N
S8N
Q8N
R5N
R6N
R7N
R8N

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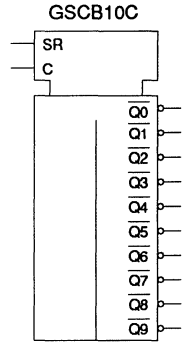
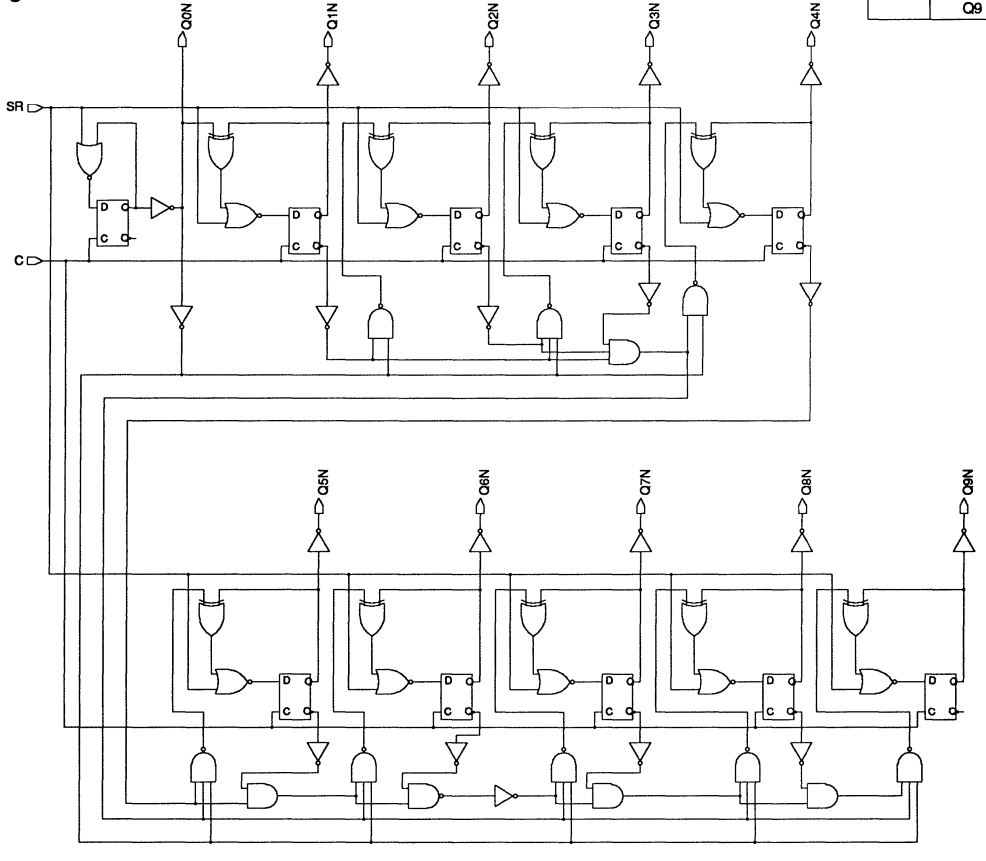
GSCB10C



Description: GSCB10C is a fast 10 bit binary up counter, with synchronous reset.
Equivalent Gate Count: 130
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N Q8N Q9N .GSCB10C SR C ;

Logic Schematic:



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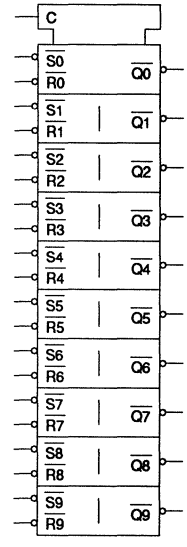
GSCB10F

GSCB10F

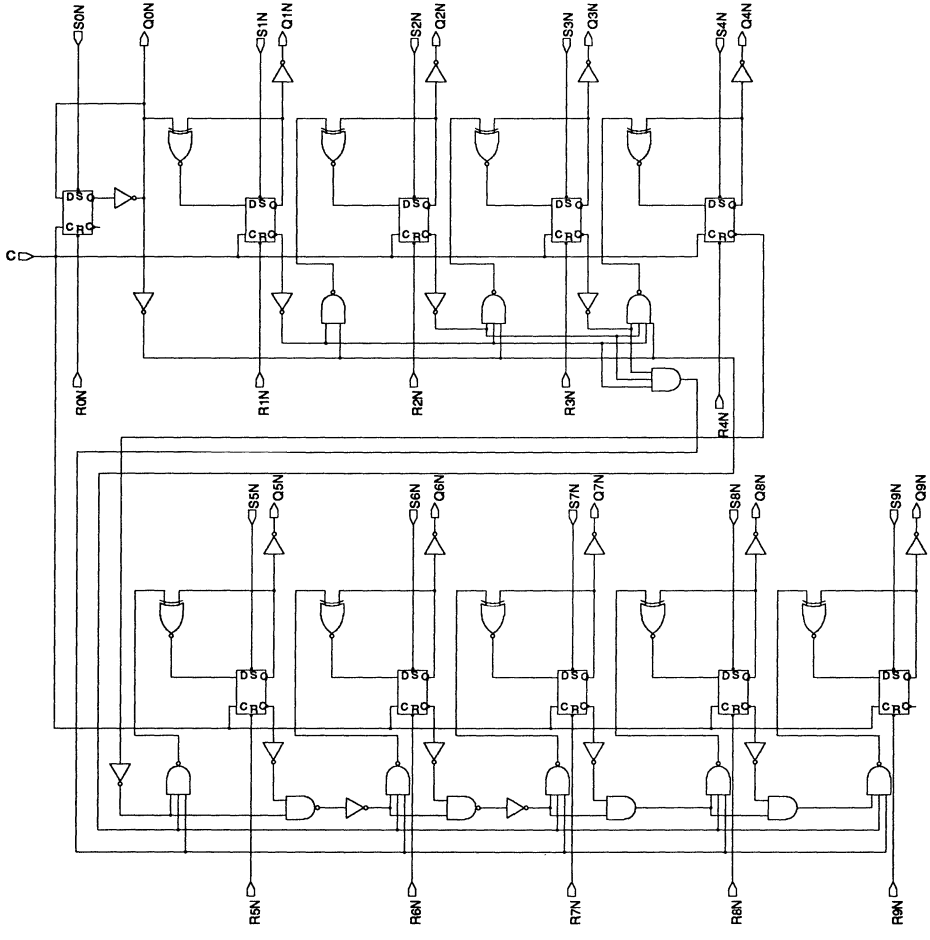


Description: GSCB10F is a fast 10 bit binary up counter, with individual set not and reset not.

Equivalent Gate Count: 141

Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N Q8N Q9N .GSCB10F C R0N R1N R2N R3N R4N R5N R6N R7N R8N R9N S0N S1N S2N S3N S4N S5N S6N S7N S8N S9N ;

Logic Schematic: On Next Page


S0N
Q0N
S1N
Q1N
S2N
Q2N
S3N
Q3N
S4N
Q4N
C
R0N
R1N
R2N
R3N
R4N
S5N
Q5N
S6N
Q6N
S7N
Q7N
S8N
Q8N
S9N
Q9N
R5N
R6N
R7N
R8N
R9N

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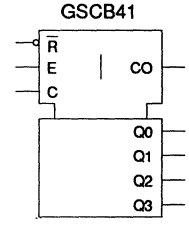
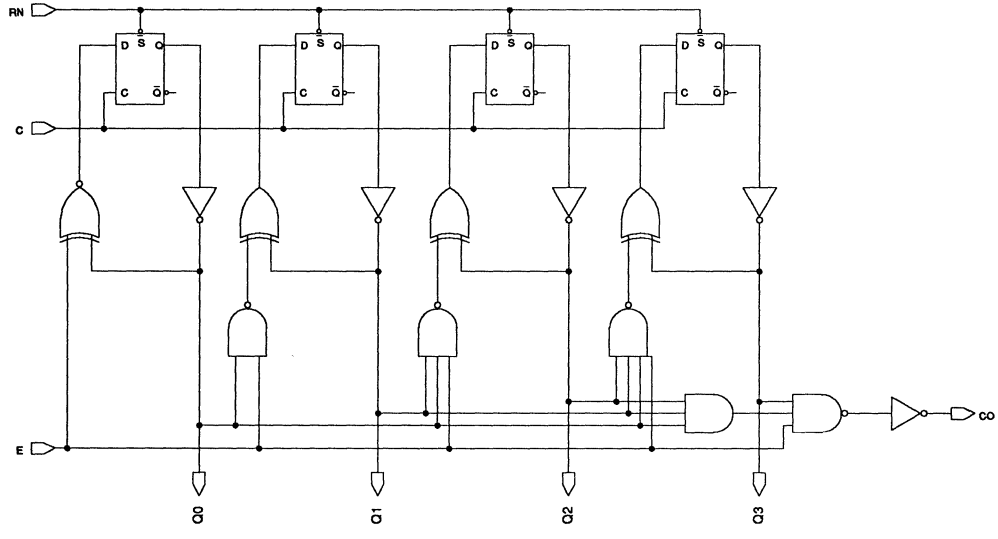
GSCB41



Description: GSCB41 is an expandable 4 bit binary up counter with reset not.
Equivalent Gate Count: 50
Bolt Syntax: Q0 Q1 Q2 Q3 CO .GSCB41 C E RN ;

Logic Schematic:



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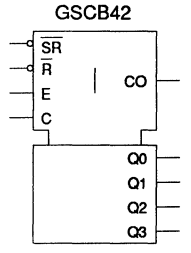
GSCB42

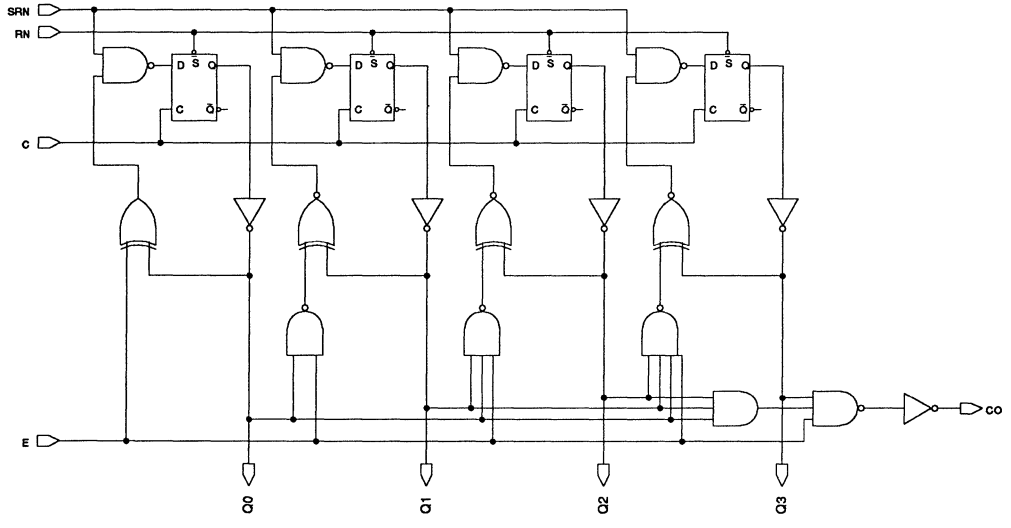


Description: GSCB42 is an expandable 4 bit binary up counter with synchronous reset not and asynchronous reset not.

Equivalent Gate Count: 54

Bolt Syntax: Q0 Q1 Q2 Q3 CO .GSCB42 C E SRN RN ;

Logic Schematic:



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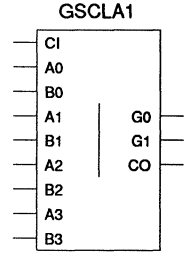
GSCLA1

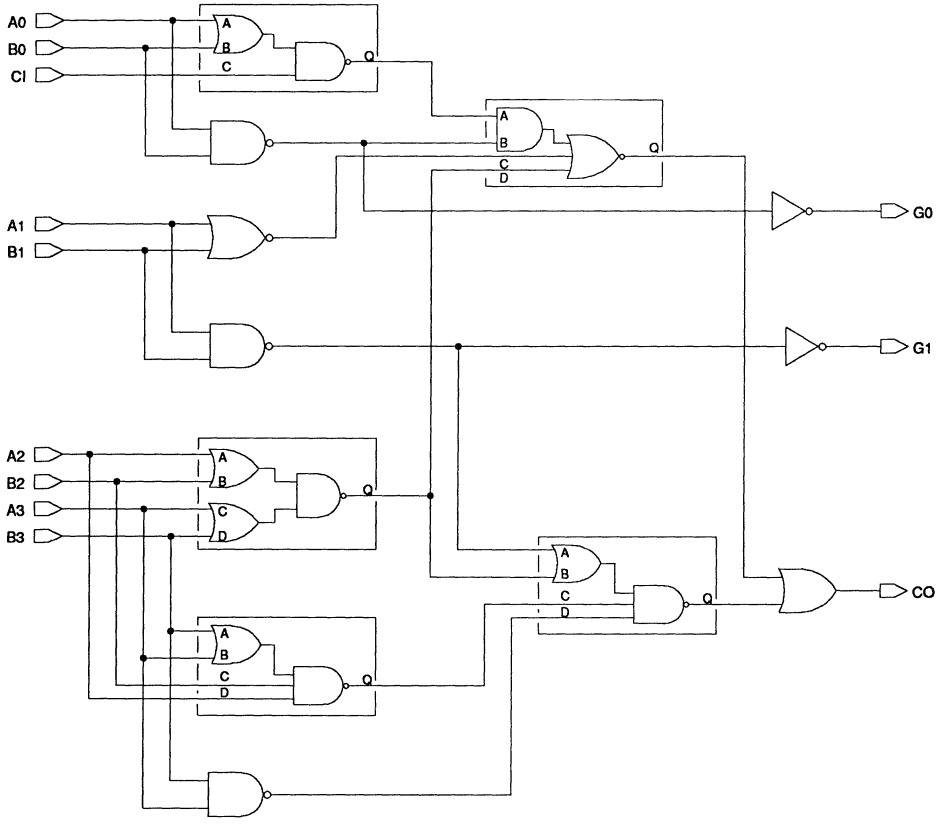


Description: GSCLA1 is a carry look ahead for a 4 bit adder [LSN].
Equivalent Gate Count: 18
Bolt Syntax: CO G0 G1 .GSCLA1 CI A0 B0 A1 B1 A2 B2 A3 B3 ;
Truth Table

CI	A0	B0	A1	B1	A2	B2	A3	B3	CO
X	X	X	X	X	X	X	L	L	L
L	X	X	X	X	X	X	H	H	H
L	X	X	X	X	H	H	P3	P3	H
L	X	X	H	H	P2	P2	P3	P3	H
L	H	H	P1	P1	P2	P2	P3	P3	H
H	P0	P0	P1	P1	P2	P2	P3	P3	H
All Other									L

Px = EITHER ONE OR BOTH OF THE PAIR HIGH
G0 = A0 AND B0
G1 = A1 AND B1

Logic Schematic: On Next Page


A0
B0
CI
A1
B1
A2
B2
A3
B3
A
B
C
D
Q
G0
G1
CO

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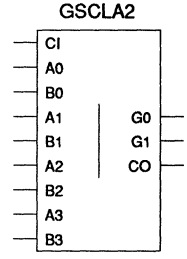
GSCLA2

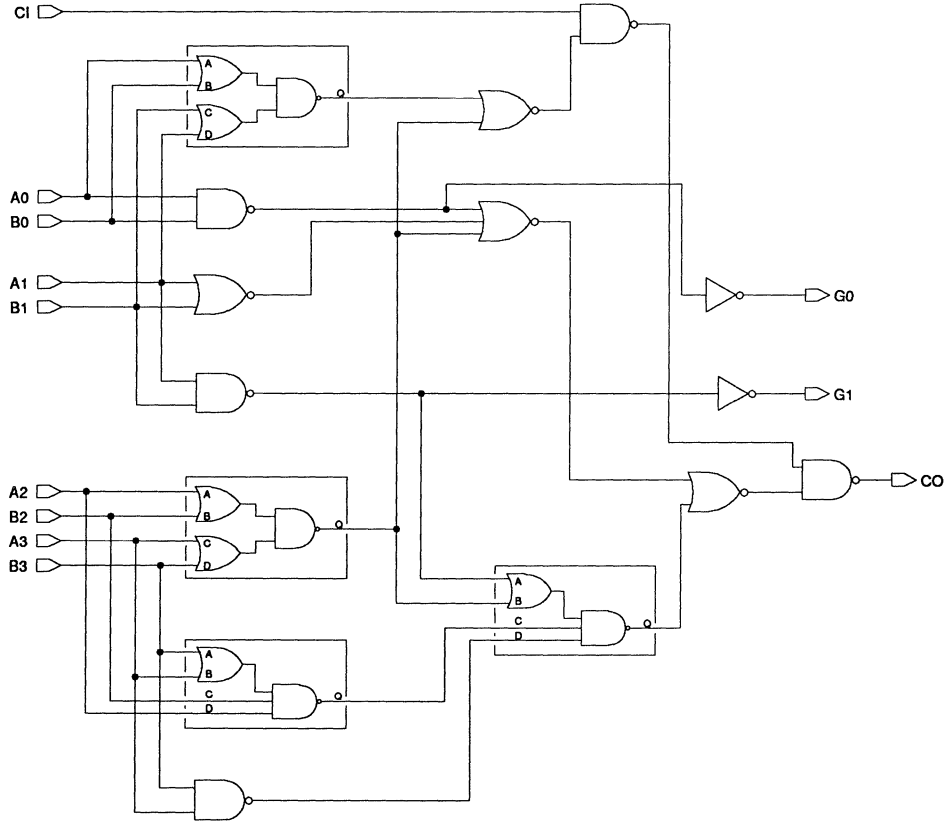


Description: GSCLA2 is a carry look ahead for a 4 bit adder.
Equivalent Gate Count: 20
Bolt Syntax: G0 G1 CO .GSCLA2 CI A0 B0 A1 B1 A2 B2 A3 B3 ;
Truth Table

CI	A0	B0	A1	B1	A2	B2	A3	B3	CO
X	X	X	X	X	X	X	L	L	L
L	X	X	X	X	X	X	H	H	H
L	X	X	X	X	H	H	P3	P3	H
L	X	X	H	H	P2	P2	P3	P3	H
L	H	H	P1	P1	P2	P2	P3	P3	H
H	P0	P0	P1	P1	P2	P2	P3	P3	H
All Other									L

Px = EITHER ONE OR BOTH OF THE PAIR HIGH.
G0 = A0 AND B0
G1 = A1 AND B1

Logic Schematic: On Next Page


CI
A0
B0
A1
B1
A2
B2
A3
B3
G0
G1
CO
A
B
C
D
Q

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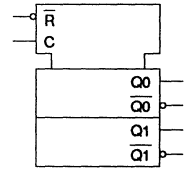
GSCM3B

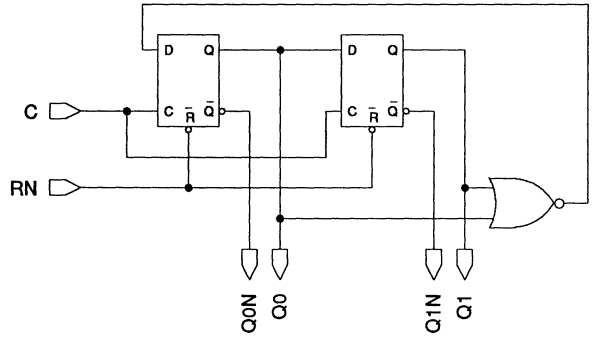
GSCM3B



Description: GSCM3B is a modulo 3 binary counter, with reset not.
Equivalent Gate Count: 13
Bolt Syntax: Q0 Q0N Q1 Q1N .GSCM3B C RN ;
Truth Table

RN	C	Q0	Q1
H	↑	L	L
H	↑	H	L
H	↑	L	H
L	X	L	L

Logic Schematic:



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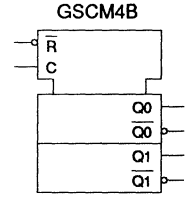
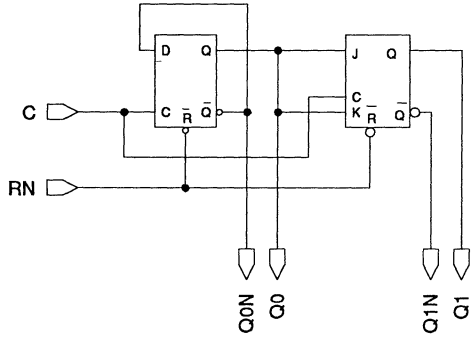
GSCM4B



Description: GSCM4B is a modulo 4 binary counter, with reset not.
Equivalent Gate Count: 16
Bolt Syntax: Q0 Q0N Q1 Q1N .GSCM4B C RN ;
Truth Table

RN	C	Q0	Q1
H	↑	L	L
H	↑	H	L
H	↑	L	H
H	↑	H	H
L	X	L	L

Logic Schematic:



MSI Functions

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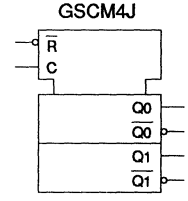
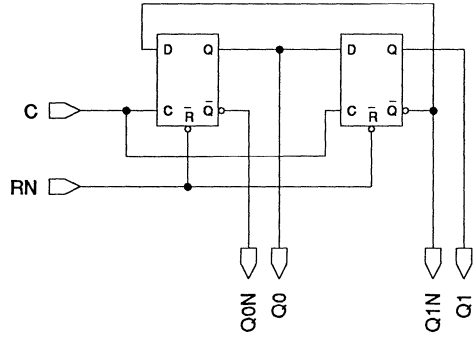
GSCM4J



Description: GSCM4J is a modulo 4 Johnson counter, with reset not.
Equivalent Gate Count: 12
Bolt Syntax: Q0 Q0N Q1 Q1N .GSCM4J C RN ;
Truth Table

RN	C	Q0	Q1
H	↑	L	L
H	↑	H	L
H	↑	H	H
H	↑	L	H
L	X	L	L

Logic Schematic:



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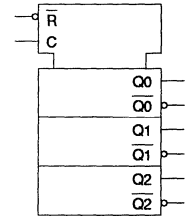
GSCM5B

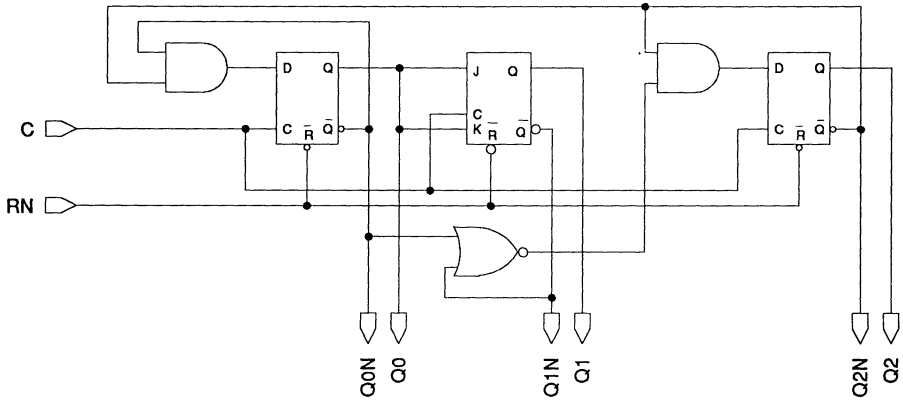
GSCM5B



Description: GSCM5B is a modulo 5 binary counter, with reset not.
Equivalent Gate Count: 27
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N .GSCM5B C RN ;
Truth Table

RN	C	Q0	Q1	Q2
H	↑	L	L	L
H	↑	H	L	L
H	↑	L	H	L
H	↑	H	H	L
H	↑	L	L	H
L	X	L	L	L

Logic Schematic:



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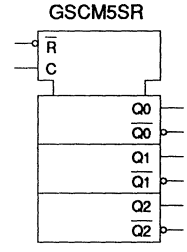
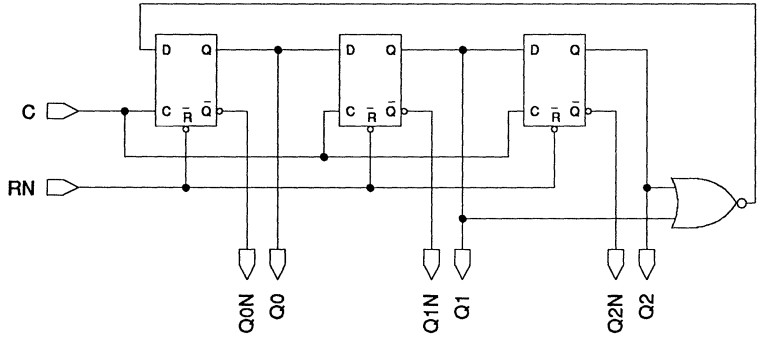
GSCM5SR

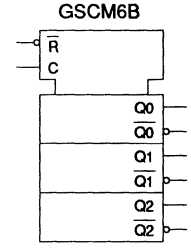


Description: GSCM5SR is a modulo 5 shift counter, with reset not.
Equivalent Gate Count: 19
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N .GSCM5SR C RN ;
Truth Table

RN	C	Q0	Q1	Q2
H	↑	L	L	L
H	↑	H	L	L
H	↑	H	H	L
H	↑	L	H	H
H	↑	L	L	H
L	X	L	L	L

Logic Schematic:

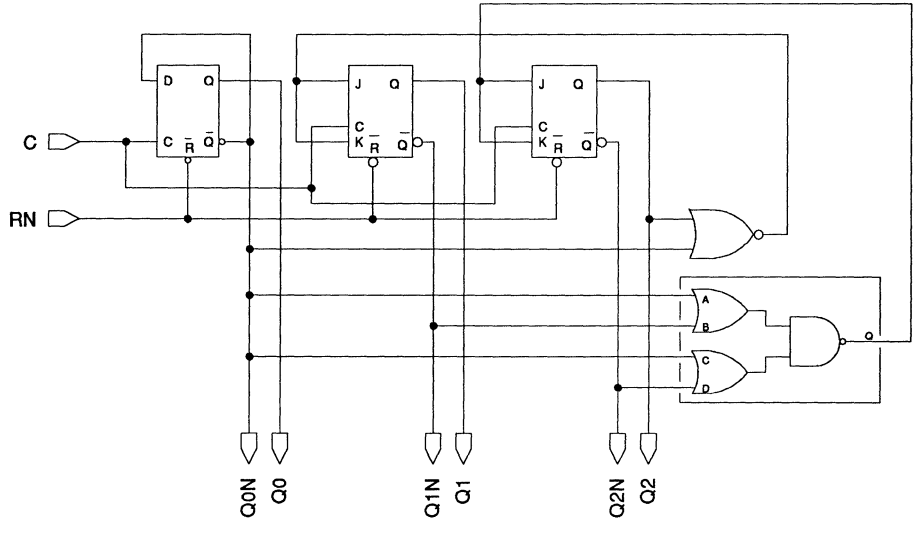




Description: GSCM6B is a modulo 6 binary counter, with reset not.
Equivalent Gate Count: 29
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N .GSCM6B C RN ;
Truth Table

RN	C	Q0	Q1	Q2
H	↑	L	L	L
H	↑	H	L	L
H	↑	L	H	L
H	↑	H	H	L
H	↑	L	L	H
H	↑	H	L	H
L	X	L	L	L

Logic Schematic:



MSI Functions

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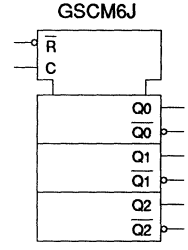
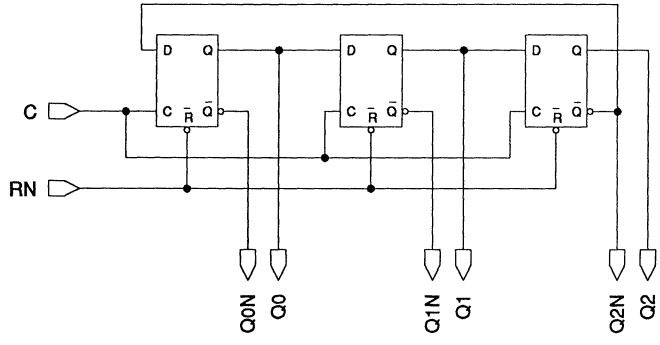
GSCM6J



Description: GSCM6J is a modulo 6 Johnson counter, with reset not.
Equivalent Gate Count: 18
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N .GSCM6J C RN ;
Truth Table

RN	C	Q0	Q1	Q2
H	↑	L	L	L
H	↑	H	L	L
H	↑	H	H	L
H	↑	H	H	H
H	↑	L	H	H
H	↑	L	L	H
L	X	L	L	L

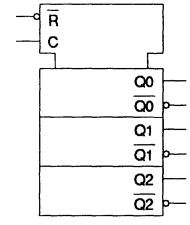
Logic Schematic:



April, 1992

GSCM7B

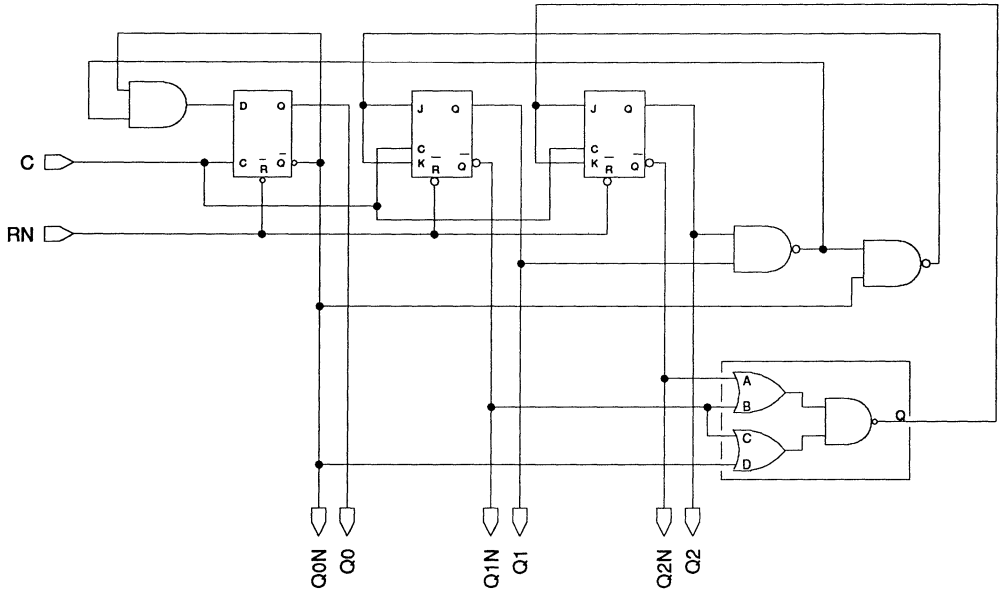
GSCM7B



Description: GSCM7B is a modulo 7 binary counter, with reset not.
Equivalent Gate Count: 32
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N .GSCM7B C RN ;
Truth Table

RN	C	Q0	Q1	Q2
H	↑	L	L	L
H	↑	H	L	L
H	↑	L	H	L
H	↑	H	H	L
H	↑	L	L	H
H	↑	H	L	H
H	↑	L	H	H
L	X	L	L	L

Logic Schematic:

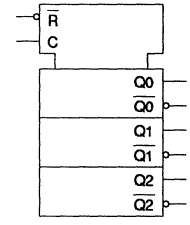


MSI Functions

April, 1992

GSCM8B

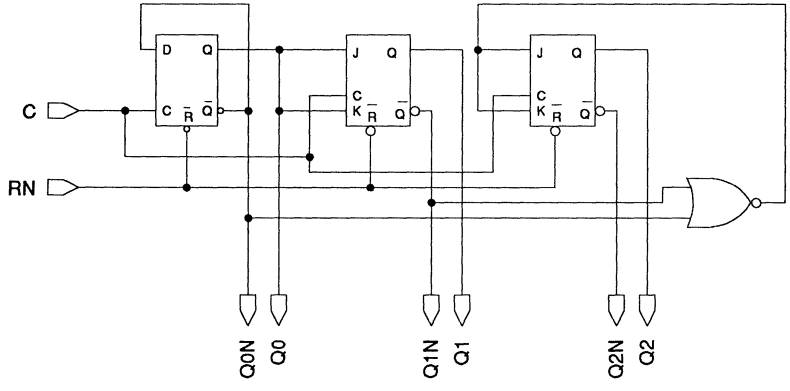
GSCM8B



Description: GSCM8B is a modulo 8 binary counter, with reset not.
Equivalent Gate Count: 27
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N .GSCM8B C RN ;
Truth Table

RN	C	Q0	Q1	Q2
H	↑	L	L	L
H	↑	H	L	L
H	↑	L	H	L
H	↑	H	H	L
H	↑	L	L	H
H	↑	H	L	H
H	↑	L	H	H
H	↑	H	H	H
L	X	L	L	L

Logic Schematic:



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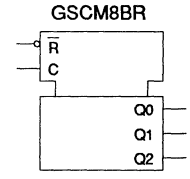
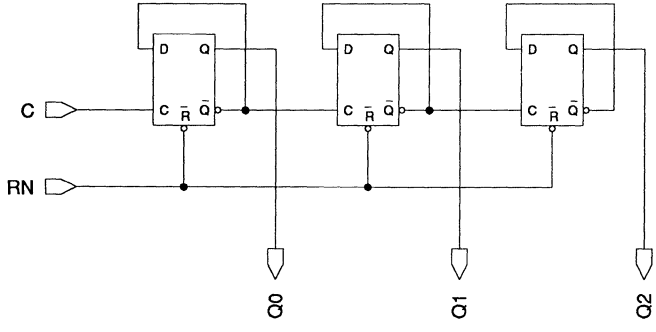
GSCM8BR



Description: GSCM8BR is a modulo 8 binary ripple counter, with reset not.
Equivalent Gate Count: 18
Bolt Syntax: Q0 Q1 Q2 .GSCM8BR C RN ;
Truth Table

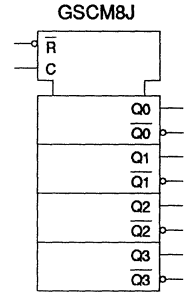
RN	C	Q0	Q1	Q2
H	↑	L	L	L
H	↑	H	L	L
H	↑	L	H	L
H	↑	H	H	L
H	↑	L	L	H
H	↑	H	L	H
H	↑	L	H	H
H	↑	H	H	H
L	X	L	L	L

Logic Schematic:



April, 1992

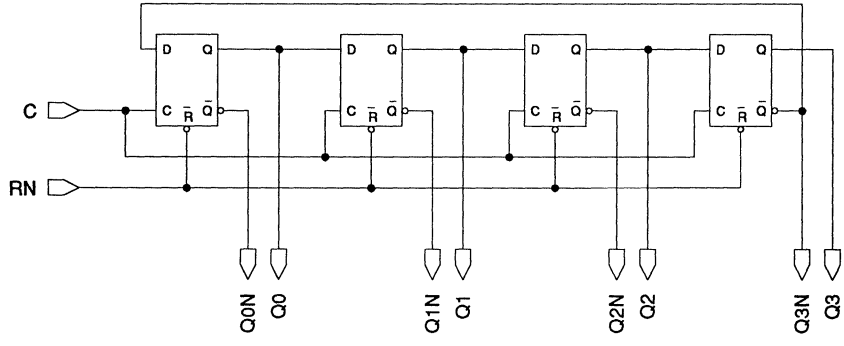
GSCM8J



Description: GSCM8J is a modulo 8 Johnson counter, with reset not.
Equivalent Gate Count: 24
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM8J C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	H	H	L	L
H	↑	H	H	H	L
H	↑	H	H	H	H
H	↑	L	H	H	H
H	↑	L	L	H	H
H	↑	L	L	L	H
L	X	L	L	L	L

Logic Schematic:



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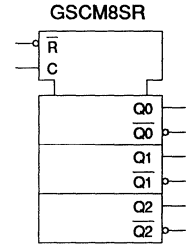
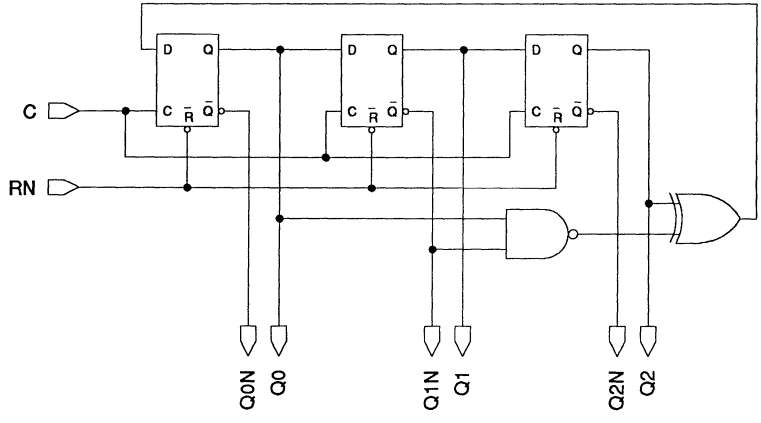
GSCM8SR



Description: GSCM8SR is a modulo 8 shift counter, with reset not.
Equivalent Gate Count: 22
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N .GSCM8SR C RN ;
Truth Table

RN	C	Q0	Q1	Q2
H	↑	L	L	L
H	↑	H	L	L
H	↑	L	H	L
H	↑	H	L	H
H	↑	H	H	L
H	↑	H	H	H
H	↑	L	H	H
H	↑	L	L	H
L	X	L	L	L

Logic Schematic:

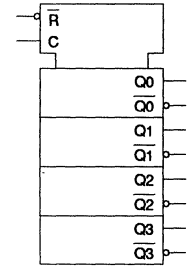


MSI Functions

April, 1992

GSCM9B

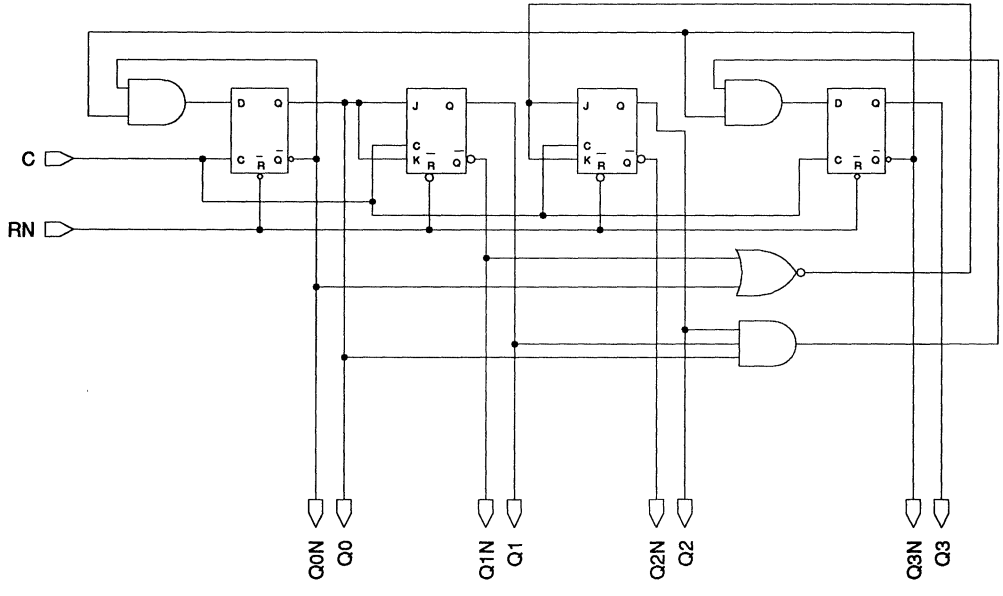
GSCM9B



Description: GSCM9B is a modulo 9 binary counter, with reset not.
Equivalent Gate Count: 39
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM9B C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	H	L	L
H	↑	L	L	H	L
H	↑	H	L	H	L
H	↑	L	H	H	L
H	↑	H	H	H	L
H	↑	L	L	L	H
L	X	L	L	L	L

Logic Schematic:



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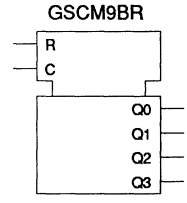
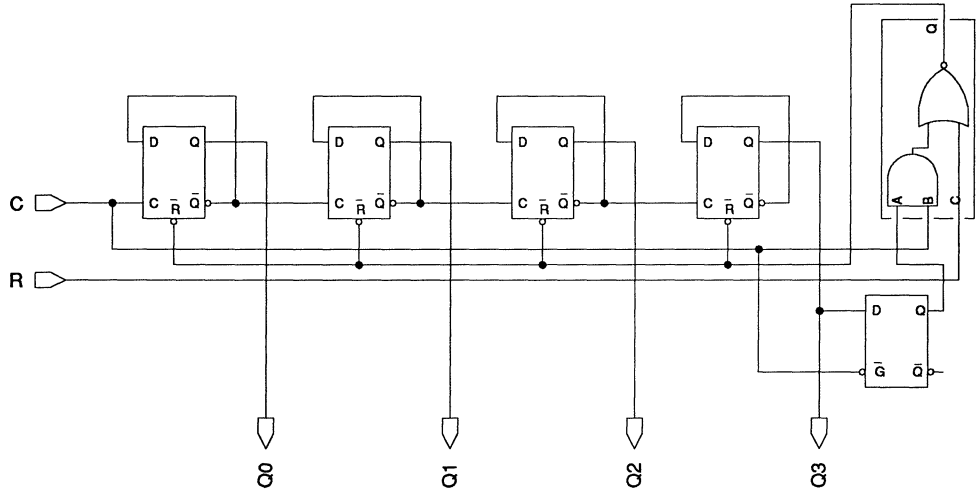
GSCM9BR



Description: GSCM9BR is a modulo 9 binary ripple counter, with reset.
Equivalent Gate Count: 29
Bolt Syntax: Q0 Q1 Q2 Q3 .GSCM9BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3
L	↑	L	L	L	L
L	↑	H	L	L	L
L	↑	L	H	L	L
L	↑	H	H	L	L
L	↑	L	L	H	L
L	↑	H	L	H	L
L	↑	L	H	H	L
L	↑	H	H	H	L
L	↑	L	L	L	H
H	X	L	L	L	L

Logic Schematic:



MSI Functions

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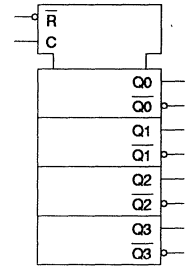
GSCM9SR

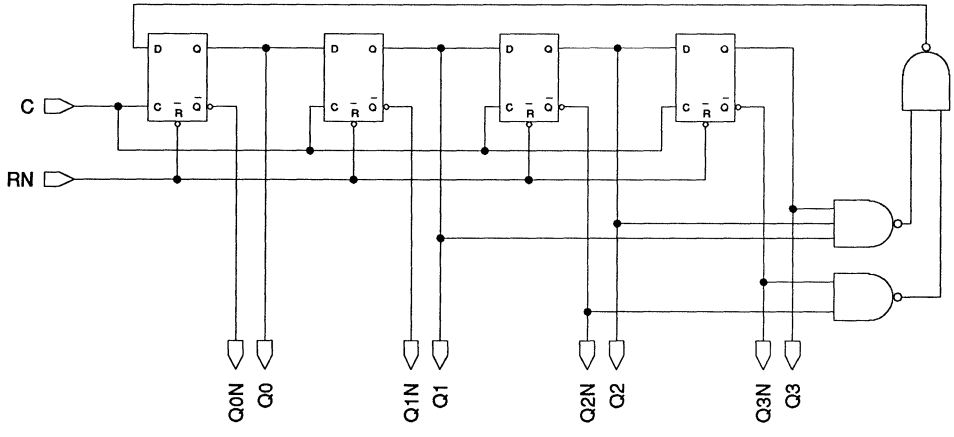
GSCM9SR



Description: GSCM9SR is a modulo 9 shift counter, with reset not.
Equivalent Gate Count: 28
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM9SR C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	H	H	L	L
H	↑	H	H	H	L
H	↑	L	H	H	H
H	↑	H	L	H	H
H	↑	L	H	L	H
H	↑	L	L	H	L
H	↑	L	L	L	H
L	X	L	L	L	L

Logic Schematic:



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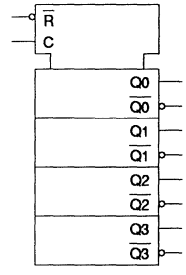
GSCM10B

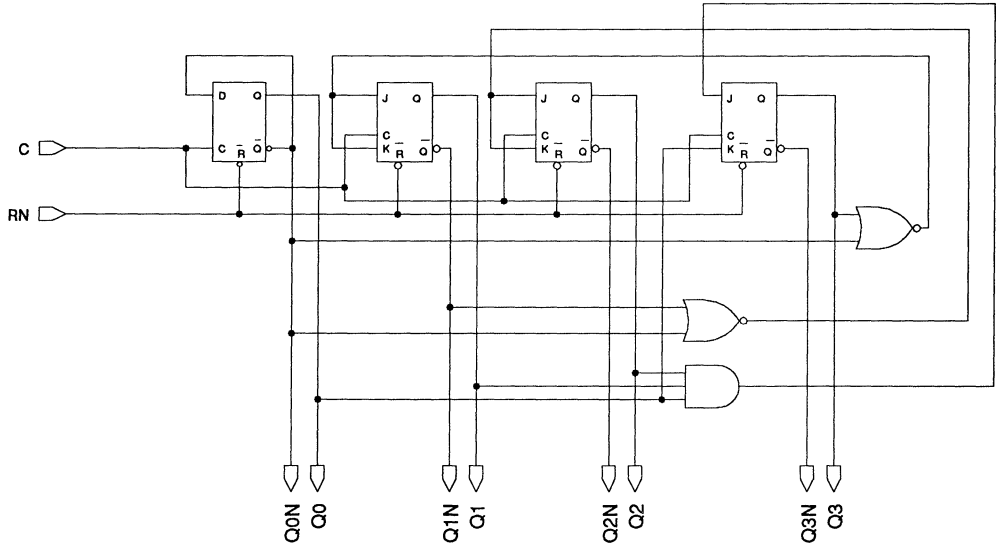
GSCM10B



Description: GSCM10B is a modulo 10 binary counter, with reset not.
Equivalent Gate Count: 40
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM10B C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	H	L	L
H	↑	L	L	H	L
H	↑	H	L	H	L
H	↑	L	H	H	L
H	↑	H	H	H	L
H	↑	L	L	L	H
H	↑	H	L	L	H
L	X	L	L	L	L

Logic Schematic:



MSI Functions

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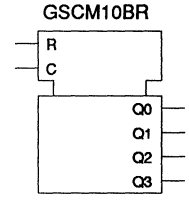
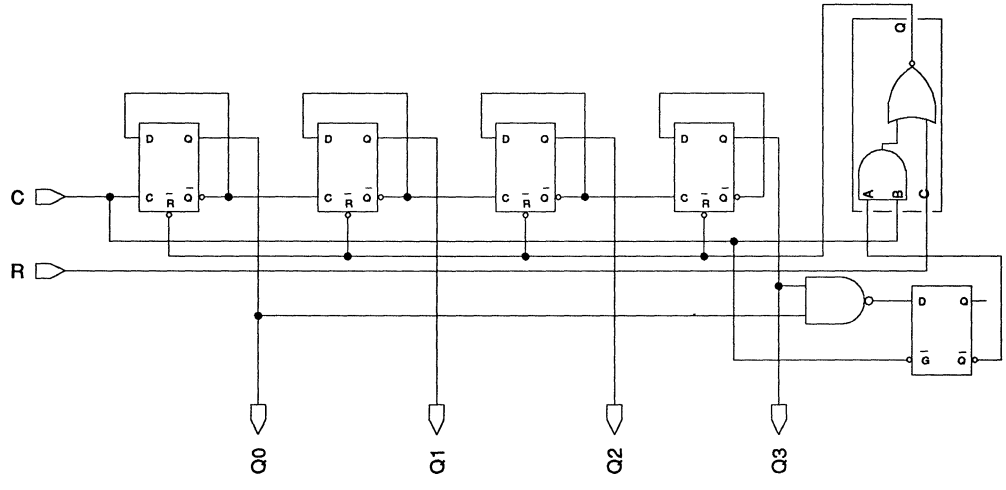
GSCM10BR



Description: GSCM10BR is a modulo 10 binary ripple counter, with reset.
Equivalent Gate Count: 30
Bolt Syntax: Q0 Q1 Q2 Q3 .GSCM10BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3
L	↑	L	L	L	L
L	↑	H	L	L	L
L	↑	L	H	L	L
L	↑	H	H	L	L
L	↑	L	L	H	L
L	↑	H	L	H	L
L	↑	L	H	H	L
L	↑	H	H	H	L
L	↑	L	L	L	H
L	↑	H	L	L	H
H	X	L	L	L	L

Logic Schematic:



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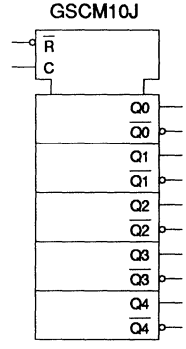
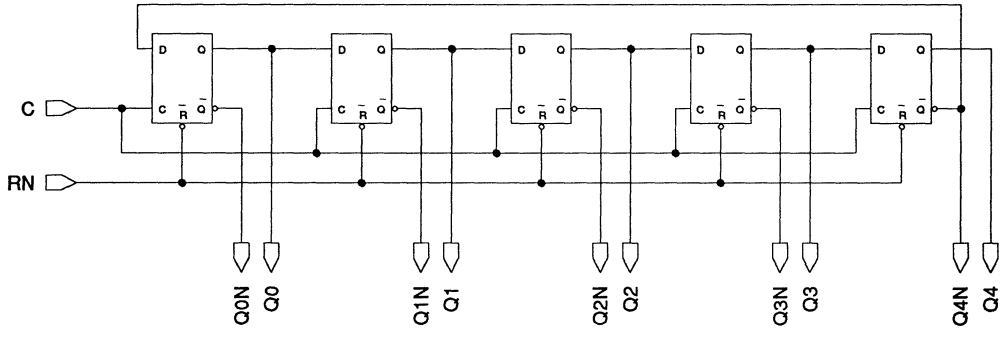
GSCM10J



Description: GSCM10J is a modulo 10 Johnson counter, with reset not.
Equivalent Gate Count: 30
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N .GSCM10J C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3	Q4
H	↑	L	L	L	L	L
H	↑	H	L	L	L	L
H	↑	H	H	L	L	L
H	↑	H	H	H	L	L
H	↑	H	H	H	H	L
H	↑	H	H	H	H	H
H	↑	L	H	H	H	H
H	↑	L	L	H	H	H
H	↑	L	L	L	H	H
H	↑	L	L	L	L	H
L	X	L	L	L	L	L

Logic Schematic:



MSI Functions

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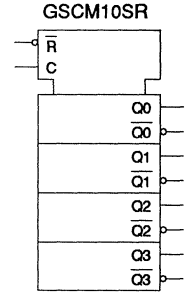
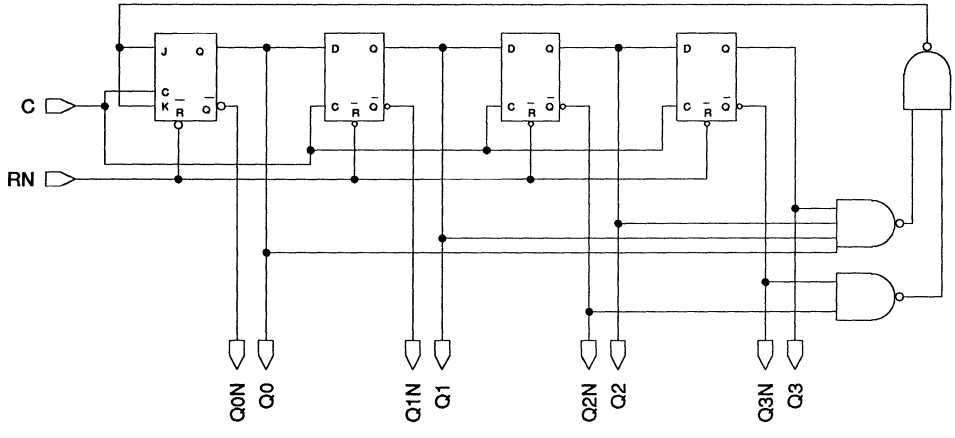
GSCM10SR



Description: GSCM10SR is a modulo 10 shift counter, with reset not.
Equivalent Gate Count: 32
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM10SR C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	L	H	L
H	↑	H	H	L	H
H	↑	H	H	H	L
H	↑	H	H	H	H
H	↑	L	H	H	H
H	↑	L	L	H	H
H	↑	L	L	L	H
L	X	L	L	L	L

Logic Schematic:



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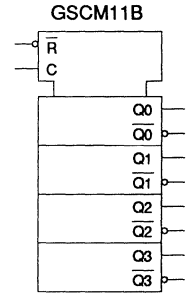
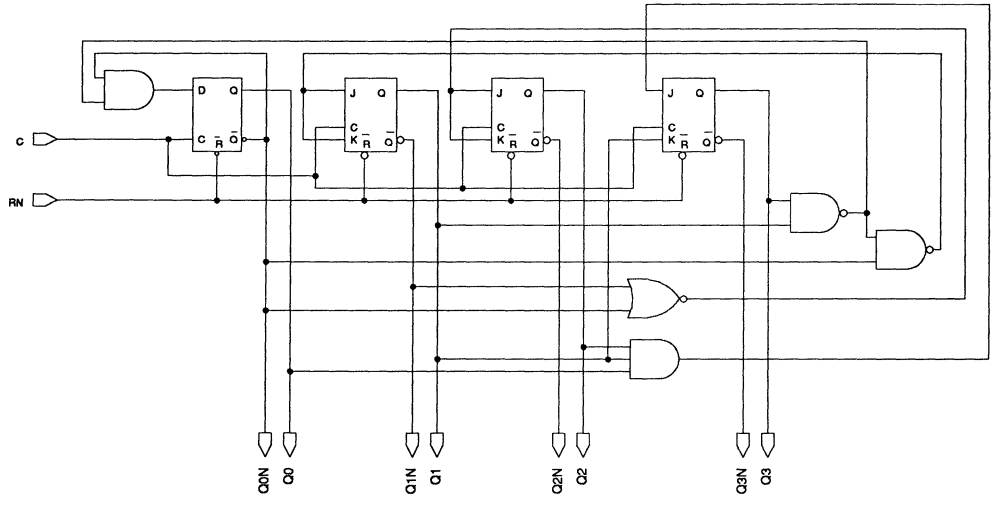
GSCM11B



Description: GSCM11B is a modulo 11 binary counter, with reset not.
Equivalent Gate Count: 43
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM11B C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	H	L	L
H	↑	L	L	H	L
H	↑	H	L	H	L
H	↑	L	H	H	L
H	↑	H	H	H	L
H	↑	L	L	L	H
H	↑	H	L	L	H
H	↑	L	H	L	H
L	X	L	L	L	L

Logic Schematic:



MSI Functions

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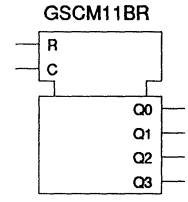
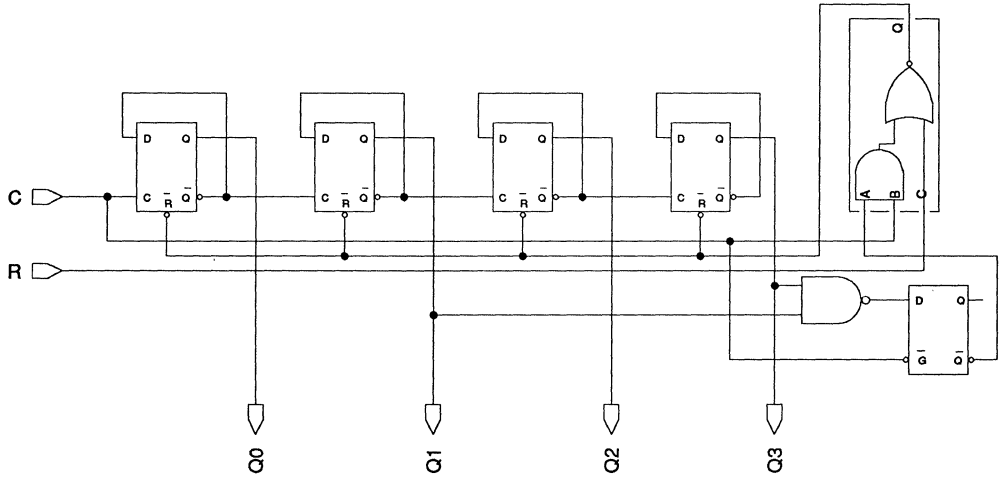
GSCM11BR



Description: GSCM11BR is a modulo 11 binary ripple counter, with reset.
Equivalent Gate Count: 30
Bolt Syntax: Q0 Q1 Q2 Q3 .GSCM11BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3
L	↑	L	L	L	L
L	↑	H	L	L	L
L	↑	L	H	L	L
L	↑	H	H	L	L
L	↑	L	L	H	L
L	↑	H	L	H	L
L	↑	L	H	H	L
L	↑	H	H	H	L
L	↑	L	L	L	H
L	↑	H	L	L	H
L	↑	L	H	L	H
H	X	L	L	L	L

Logic Schematic:



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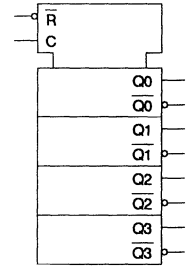
GSCM12B

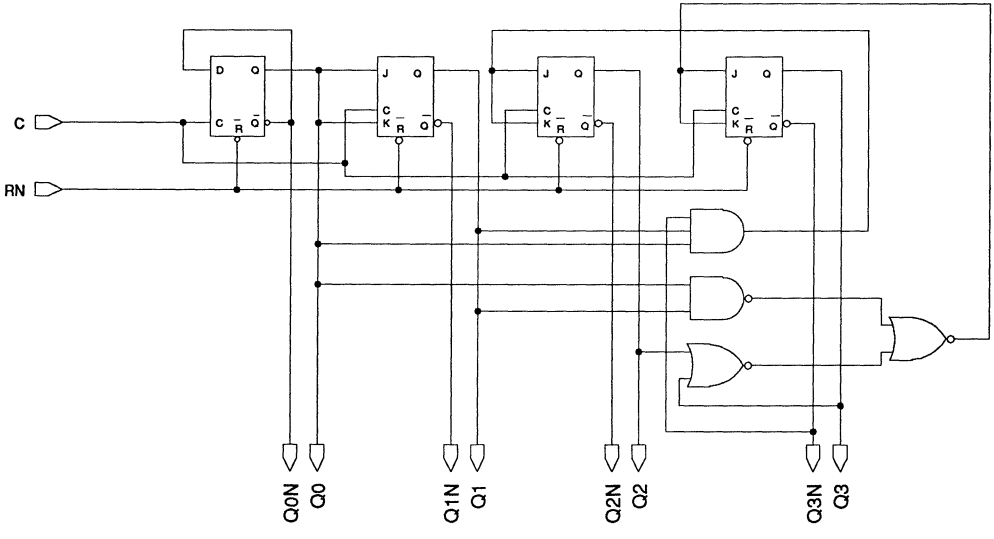
GSCM12B



Description: GSCM12B is a modulo 12 binary counter, with reset not.
Equivalent Gate Count: 41
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM12B C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	H	L	L
H	↑	L	L	H	L
H	↑	H	L	H	L
H	↑	L	H	H	L
H	↑	H	H	H	L
H	↑	L	L	L	H
H	↑	H	L	L	H
H	↑	L	H	L	H
H	↑	H	H	L	H
L	X	L	L	L	L

Logic Schematic:



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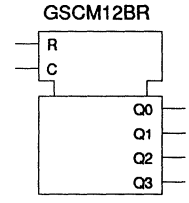
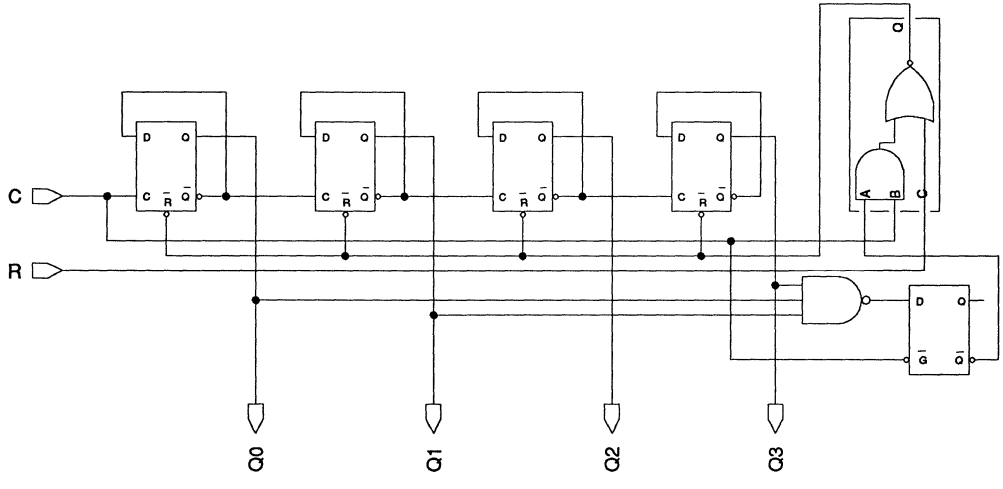
GSCM12BR



Description: GSCM12BR is a modulo 12 binary ripple counter, with reset.
Equivalent Gate Count: 31
Bolt Syntax: Q0 Q1 Q2 Q3 .GSCM12BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3
L	↑	L	L	L	L
L	↑	H	L	L	L
L	↑	L	H	L	L
L	↑	H	H	L	L
L	↑	L	L	H	L
L	↑	H	L	H	L
L	↑	L	H	H	L
L	↑	H	H	H	L
L	↑	L	L	L	H
L	↑	H	L	L	H
L	↑	L	H	L	H
L	↑	H	H	L	H
H	X	L	L	L	L

Logic Schematic:



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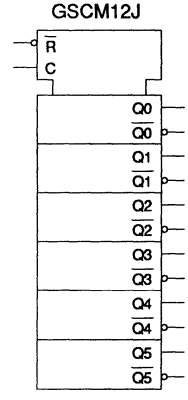
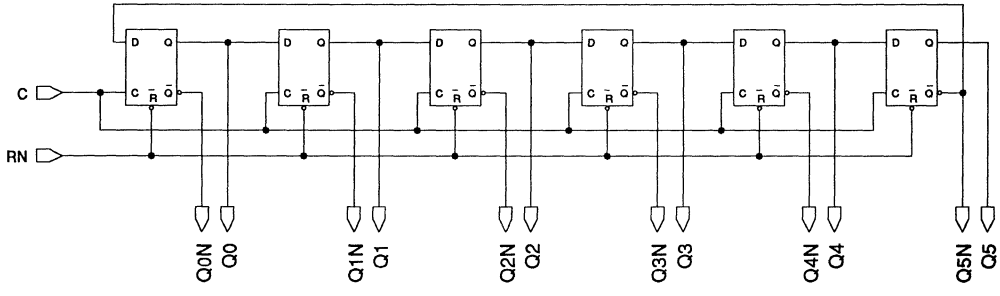
GSCM12J



Description: GSCM12J is a modulo 12 Johnson counter, with reset not.
Equivalent Gate Count: 36
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N .GSCM12J C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3	Q4	Q5
H	↑	L	L	L	L	L	L
H	↑	H	L	L	L	L	L
H	↑	H	H	L	L	L	L
H	↑	H	H	H	L	L	L
H	↑	H	H	H	H	L	L
H	↑	H	H	H	H	H	L
H	↑	H	H	H	H	H	H
H	↑	L	H	H	H	H	H
H	↑	L	L	H	H	H	H
H	↑	L	L	L	H	H	H
H	↑	L	L	L	L	H	H
H	↑	L	L	L	L	L	H
L	X	L	L	L	L	L	L

Logic Schematic:



MSI Functions

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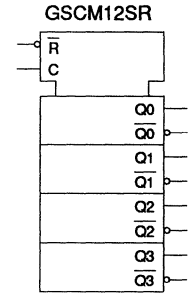
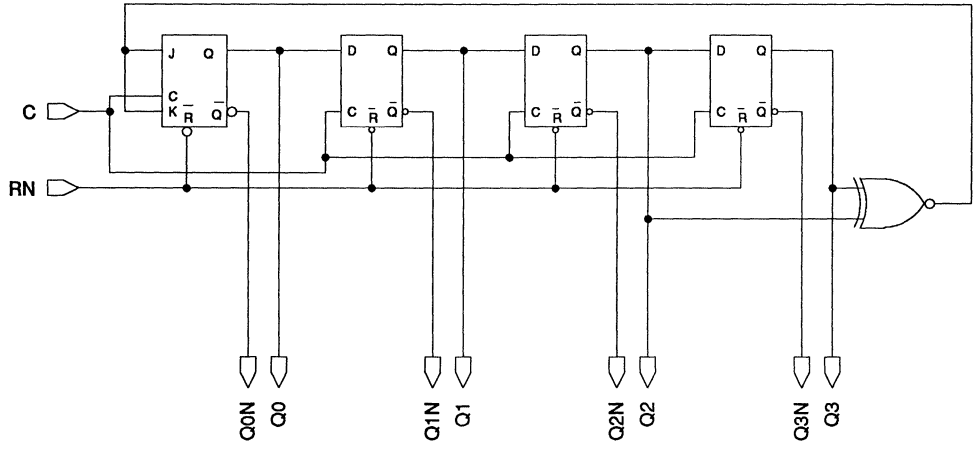
GSCM12SR



Description: GSCM12SR is a modulo 12 shift counter, with reset not.
Equivalent Gate Count: 31
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM12SR C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	L	H	L
H	↑	H	H	L	H
H	↑	H	H	H	L
H	↑	H	H	H	H
H	↑	L	H	H	H
H	↑	H	L	H	H
H	↑	L	H	L	H
H	↑	L	L	H	L
H	↑	L	L	L	H
L	X	L	L	L	L

Logic Schematic:



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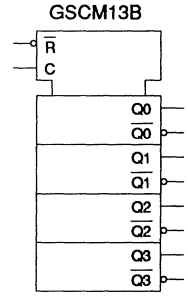
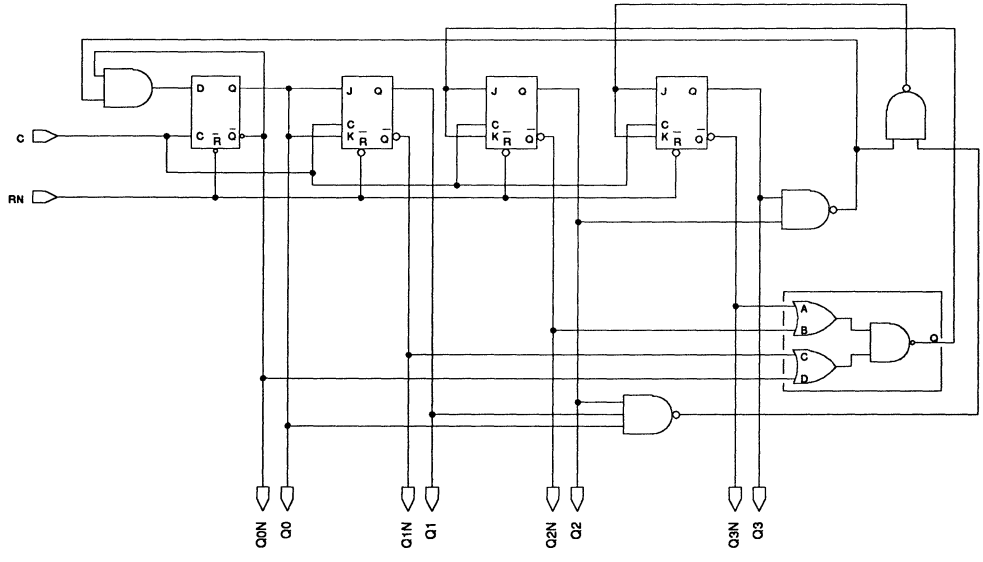
GSCM13B



Description: GSCM13B is a modulo 13 binary counter, with reset not.
Equivalent Gate Count: 44
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM13B C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	H	L	L
H	↑	L	L	H	L
H	↑	H	L	H	L
H	↑	L	H	H	L
H	↑	H	H	H	L
H	↑	L	L	L	H
H	↑	H	L	L	H
H	↑	L	H	L	H
H	↑	H	H	L	H
H	↑	L	L	H	H
L	X	L	L	L	L

Logic Schematic:



MSI Functions

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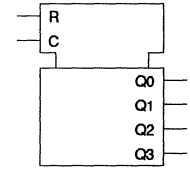
GSCM13BR

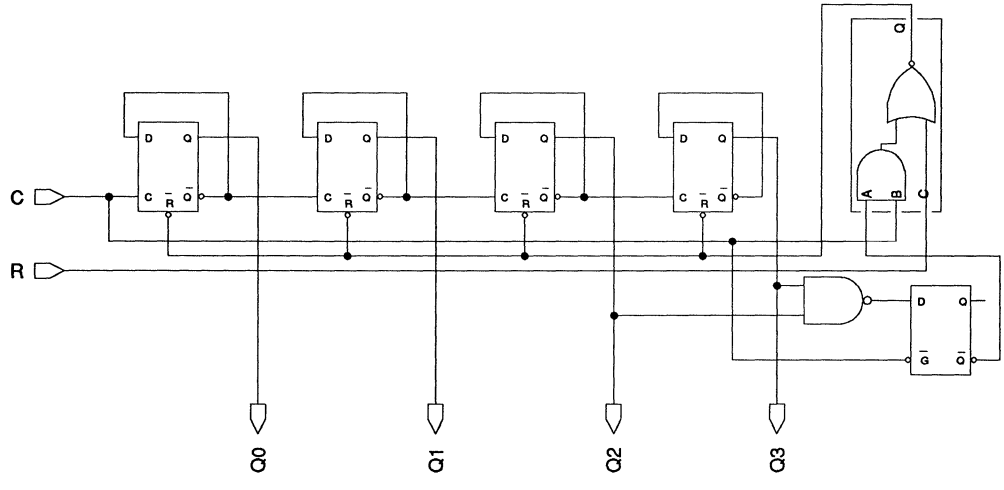
GSCM13BR



Description: GSCM13BR is a modulo 13 binary ripple counter, with reset.
Equivalent Gate Count: 30
Bolt Syntax: Q0 Q1 Q2 Q3 .GSCM13BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3
L	↑	L	L	L	L
L	↑	H	L	L	L
L	↑	L	H	L	L
L	↑	H	H	L	L
L	↑	L	L	H	L
L	↑	H	L	H	L
L	↑	L	H	H	L
L	↑	H	H	H	L
L	↑	L	L	L	H
L	↑	H	L	L	H
L	↑	L	H	L	H
L	↑	H	H	L	H
L	↑	L	L	H	H
H	X	L	L	L	L

Logic Schematic:



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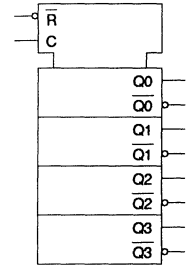
GSCM14B

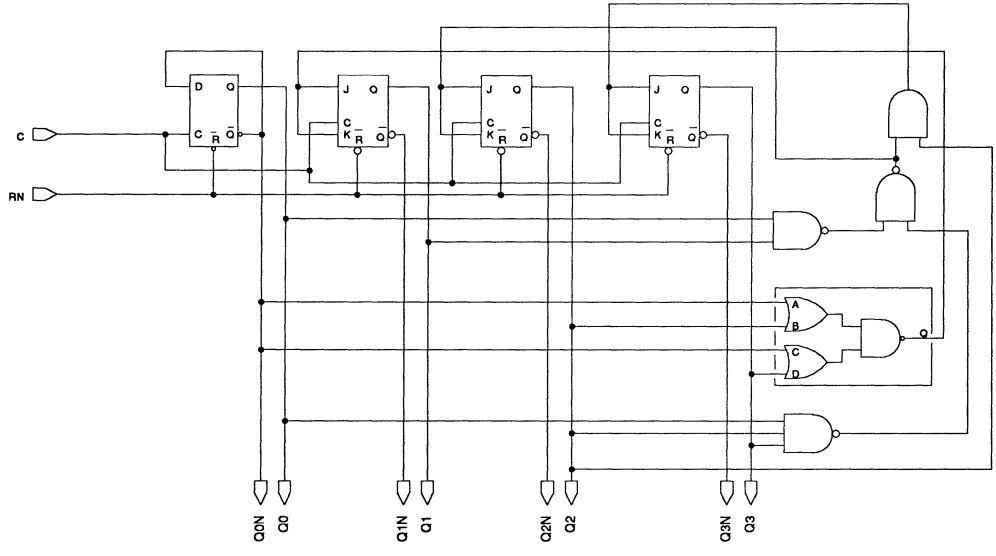
GSCM14B



Description: GSCM14B is a modulo 14 binary counter, with reset not.
Equivalent Gate Count: 44
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM14B C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	H	L	L
H	↑	L	L	H	L
H	↑	H	L	H	L
H	↑	L	H	H	L
H	↑	H	H	H	L
H	↑	L	L	L	H
H	↑	H	L	L	H
H	↑	L	H	L	H
H	↑	H	H	L	H
H	↑	L	L	H	H
H	↑	H	L	H	H
L	X	L	L	L	L

Logic Schematic:



MSI Functions

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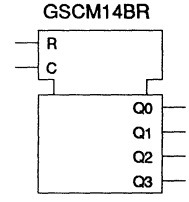
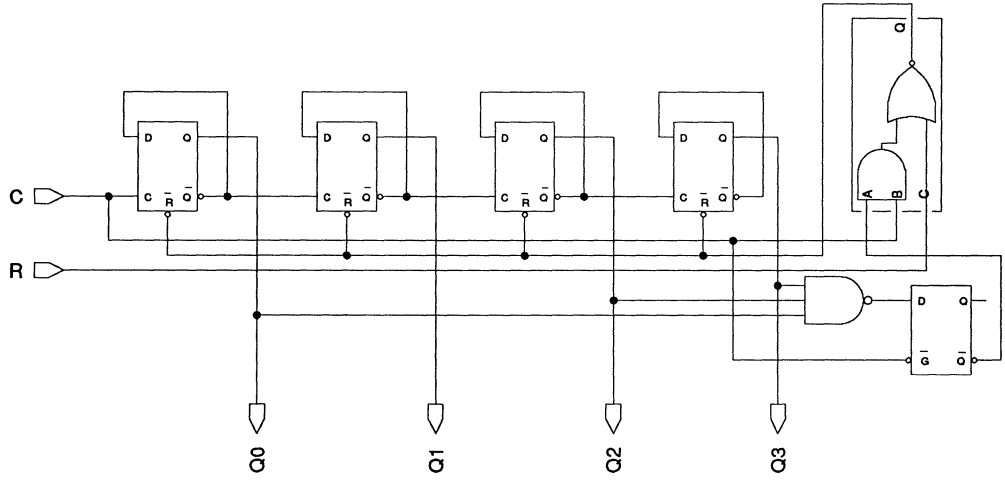
GSCM14BR



Description: GSCM14BR is a modulo 14 binary ripple counter, with reset.
Equivalent Gate Count: 31
Bolt Syntax: Q0 Q1 Q2 Q3 .GSCM14BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3
L	↑	L	L	L	L
L	↑	H	L	L	L
L	↑	L	H	L	L
L	↑	H	H	L	L
L	↑	L	L	H	L
L	↑	H	L	H	L
L	↑	L	H	H	L
L	↑	H	H	H	L
L	↑	L	L	L	H
L	↑	H	L	L	H
L	↑	L	H	L	H
L	↑	H	H	L	H
L	↑	L	L	H	H
L	↑	H	L	H	H
H	X	L	L	L	L

Logic Schematic:



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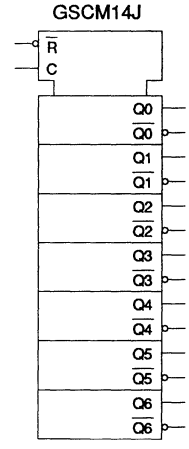
GSCM14J



Description: GSCM14J is a modulo 14 Johnson counter, with reset not.

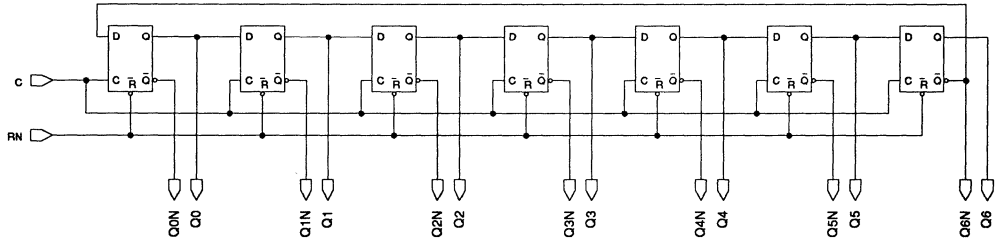
Equivalent Gate Count: 42

Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N .GSCM14J C RN ;

Truth Table

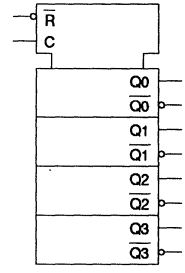
RN	C	Q0	Q1	Q2	Q3	Q4	Q5	Q6
H	↑	L	L	L	L	L	L	L
H	↑	H	L	L	L	L	L	L
H	↑	H	H	L	L	L	L	L
H	↑	H	H	H	L	L	L	L
H	↑	H	H	H	H	L	L	L
H	↑	H	H	H	H	H	L	L
H	↑	H	H	H	H	H	H	L
H	↑	H	H	H	H	H	H	H
H	↑	L	H	H	H	H	H	H
H	↑	L	L	H	H	H	H	H
H	↑	L	L	L	H	H	H	H
H	↑	L	L	L	L	H	H	H
H	↑	L	L	L	L	L	H	H
H	↑	L	L	L	L	L	L	H
L	X	L	L	L	L	L	L	L

Logic Schematic:



MSI Functions

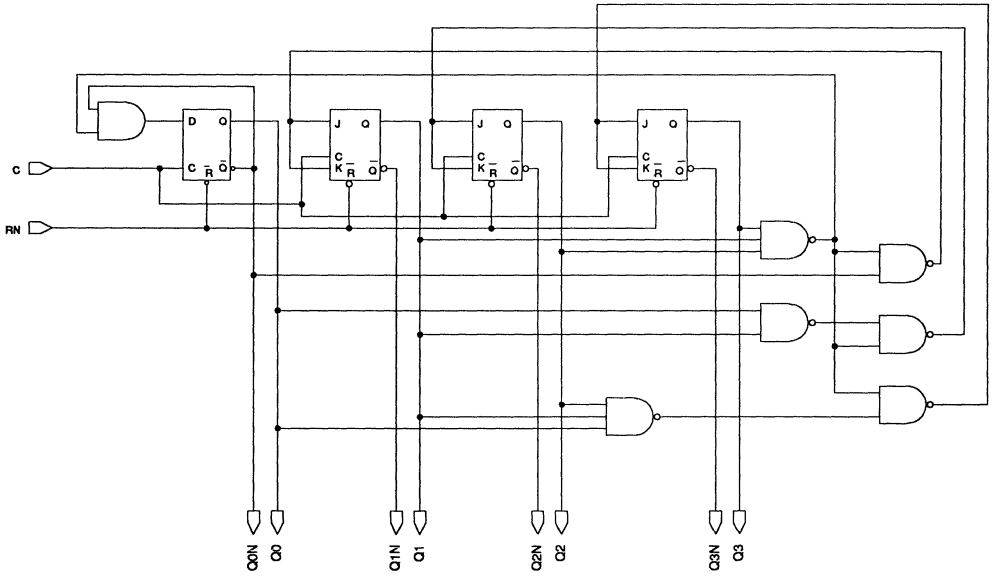
GSCM15B



Description: GSCM15B is a modulo 15 binary counter, with reset not.
Equivalent Gate Count: 46
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM15B C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	H	L	L
H	↑	L	L	H	L
H	↑	H	L	H	L
H	↑	L	H	H	L
H	↑	H	H	H	L
H	↑	L	L	L	H
H	↑	H	L	L	H
H	↑	L	H	L	H
H	↑	H	H	L	H
H	↑	L	L	H	H
H	↑	H	L	H	H
H	↑	L	H	H	H
L	X	L	L	L	L

Logic Schematic:



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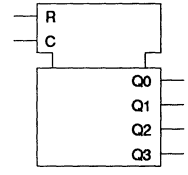
GSCM15BR

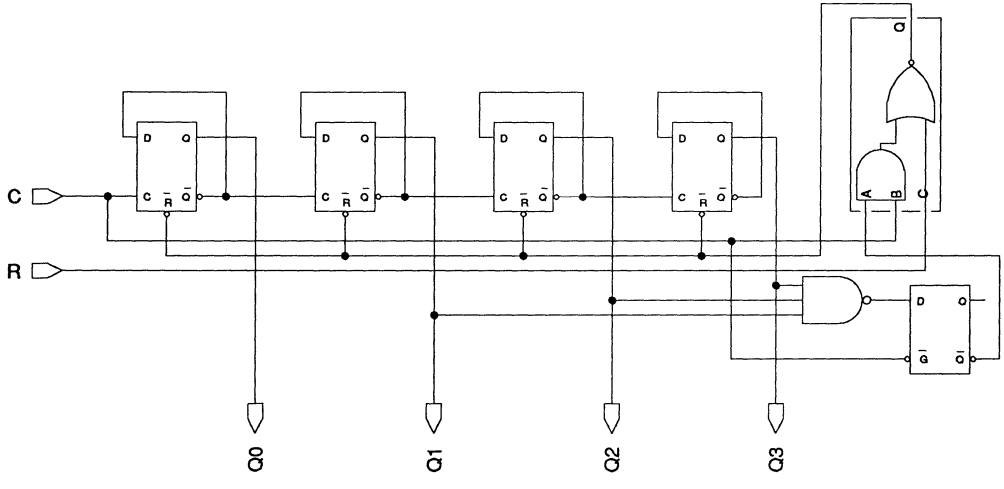
GSCM15BR



Description: GSCM15BR is a modulo 15 binary ripple counter, .with reset.
Equivalent Gate Count: 31
Bolt Syntax: Q0 Q1 Q2 Q3 .GSCM15BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3
L	↑	L	L	L	L
L	↑	H	L	L	L
L	↑	L	H	L	L
L	↑	H	H	L	L
L	↑	L	L	H	L
L	↑	H	L	H	L
L	↑	L	H	H	L
L	↑	H	H	H	L
L	↑	L	L	L	H
L	↑	H	L	L	H
L	↑	L	H	L	H
L	↑	H	H	L	H
L	↑	L	L	H	H
L	↑	H	L	H	H
L	↑	L	H	H	H
H	X	L	L	L	L

Logic Schematic:



MSI Functions

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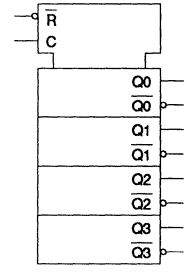
GSCM16B

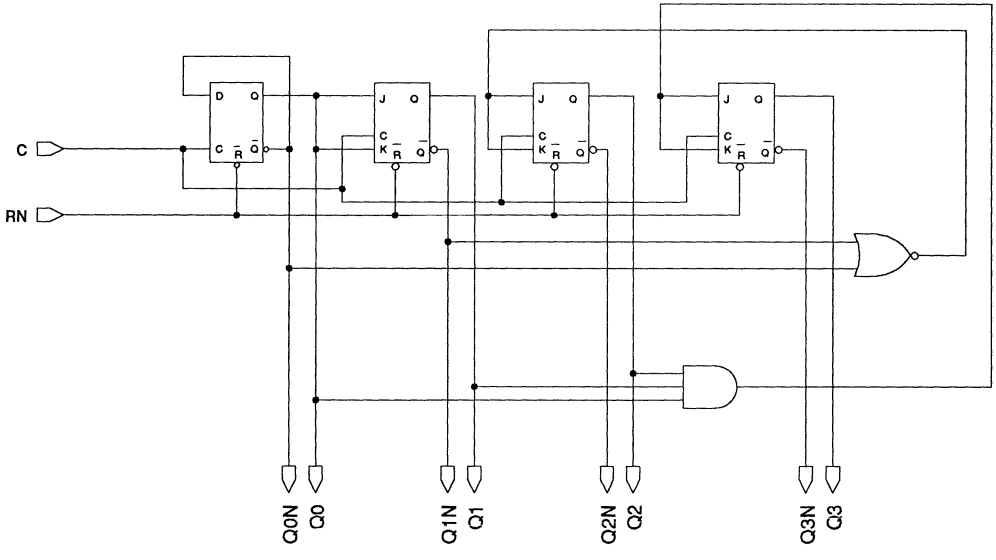
GSCM16B



Description: GSCM16B is a modulo 16 binary counter, with reset not.
Equivalent Gate Count: 39
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSCM16B C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	H	L	L
H	↑	L	L	H	L
H	↑	H	L	H	L
H	↑	L	H	H	L
H	↑	H	H	H	L
H	↑	L	L	L	H
H	↑	H	L	L	H
H	↑	L	H	L	H
H	↑	H	H	L	H
H	↑	L	L	H	H
H	↑	H	L	H	H
H	↑	L	H	H	H
H	↑	H	H	H	H
L	X	L	L	L	L

Logic Schematic:



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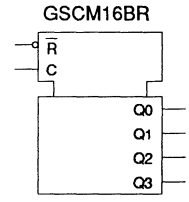
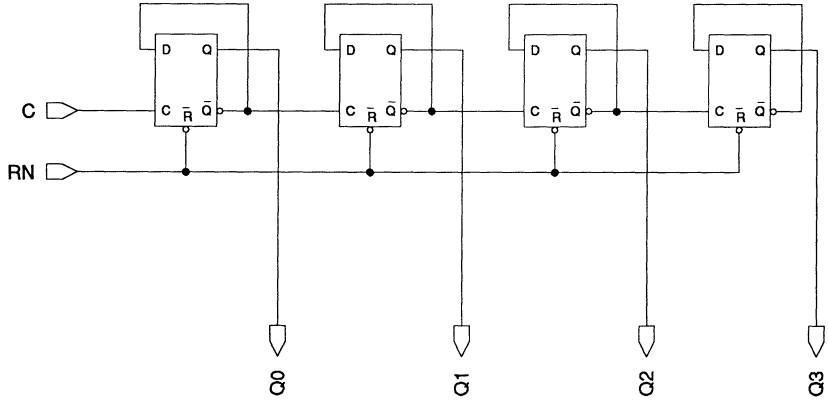
GSCM16BR



Description: GSCM16BR is a modulo 16 binary ripple counter, with reset not.
Equivalent Gate Count: 24
Bolt Syntax: Q0 Q1 Q2 Q3 .GSCM16BR C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3
H	↑	L	L	L	L
H	↑	H	L	L	L
H	↑	L	H	L	L
H	↑	H	H	L	L
H	↑	L	L	H	L
H	↑	H	L	H	L
H	↑	L	H	H	L
H	↑	H	H	H	L
H	↑	L	L	L	H
H	↑	H	L	L	H
H	↑	L	H	L	H
H	↑	H	H	L	H
H	↑	L	L	H	H
H	↑	H	L	H	H
H	↑	L	H	H	H
H	↑	H	H	H	H
L	X	L	L	L	L

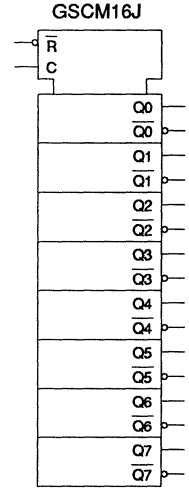
Logic Schematic:



MSI Functions

April, 1992

GSCM16J



Description: GSCM16J is a modulo 16 Johnson counter, with reset not.

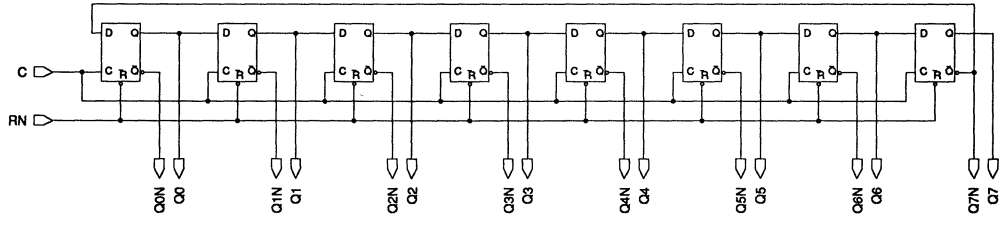
Equivalent Gate Count: 48

Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N
.GSCM16J C RN ;

Truth Table

RN	C	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
H	↑	L	L	L	L	L	L	L	L
H	↑	H	L	L	L	L	L	L	L
H	↑	H	H	L	L	L	L	L	L
H	↑	H	H	H	L	L	L	L	L
H	↑	H	H	H	H	L	L	L	L
H	↑	H	H	H	H	H	L	L	L
H	↑	H	H	H	H	H	H	L	L
H	↑	H	H	H	H	H	H	H	L
H	↑	H	H	H	H	H	H	H	H
H	↑	L	H	H	H	H	H	H	H
H	↑	L	L	H	H	H	H	H	H
H	↑	L	L	L	H	H	H	H	H
H	↑	L	L	L	L	H	H	H	H
H	↑	L	L	L	L	L	H	H	H
H	↑	L	L	L	L	L	L	H	H
H	↑	L	L	L	L	L	L	L	H
L	X	L	L	L	L	L	L	L	L

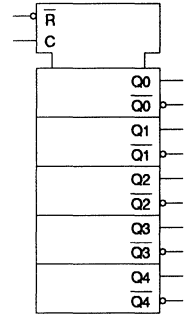
Logic Schematic:



April, 1992

GSCM17B

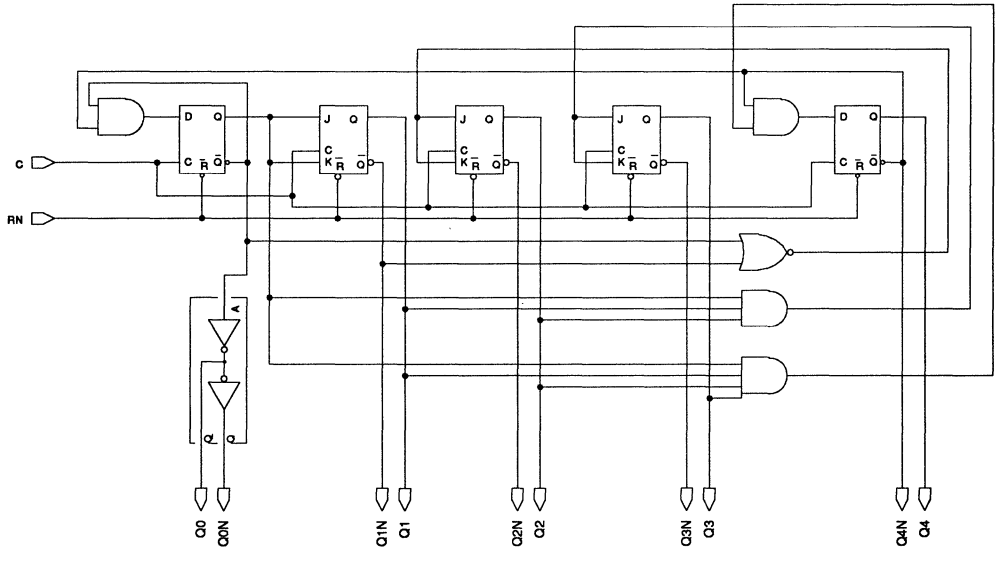
GSCM17B



Description: GSCM17B is a modulo 17 binary counter, with reset not.
Equivalent Gate Count: 53
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N .GSCM17B C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3	Q4
H	↑	L	L	L	L	L
H	↑	H	L	L	L	L
H	↑	L	H	L	L	L
H	↑	H	H	L	L	L
H	↑	L	L	H	L	L
H	↑	H	L	H	L	L
H	↑	L	H	H	L	L
H	↑	H	H	H	L	L
H	↑	L	L	L	H	L
H	↑	H	L	L	H	L
H	↑	L	H	L	H	L
H	↑	H	H	L	H	L
H	↑	L	L	H	H	L
H	↑	H	L	H	H	L
H	↑	L	H	H	H	L
H	↑	H	H	H	H	L
H	↑	L	L	L	L	H
L	X	L	L	L	L	L

Logic Schematic:

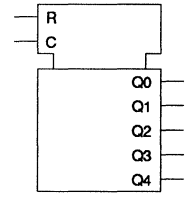


MSI Functions

April, 1992

GSCM17BR

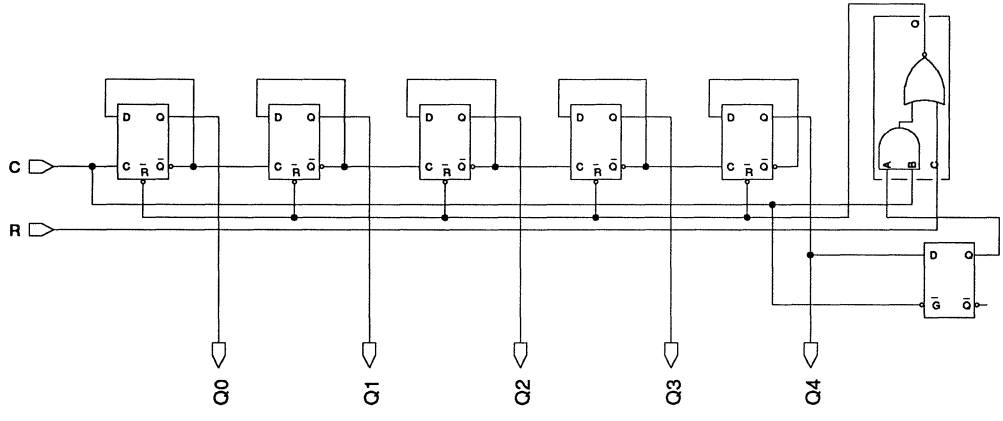
GSCM17BR



Description: GSCM17BR is a modulo 17 binary ripple counter, with reset.
Equivalent Gate Count: 35
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM17BR C R ;
Truth Table

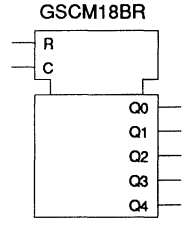
R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
H	X	L	L	L	L	L

Logic Schematic:



April, 1992

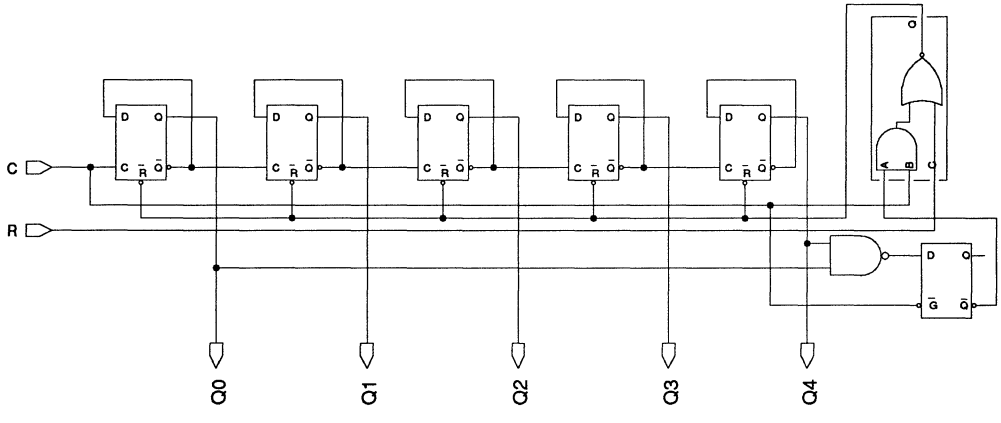
GSCM18BR



Description: GSCM18BR is a modulo 18 binary ripple counter, with reset.
Equivalent Gate Count: 36
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM18BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
H	X	L	L	L	L	L

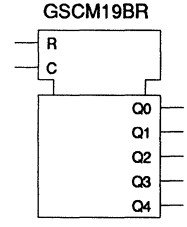
Logic Schematic:



MSI Functions

April, 1992

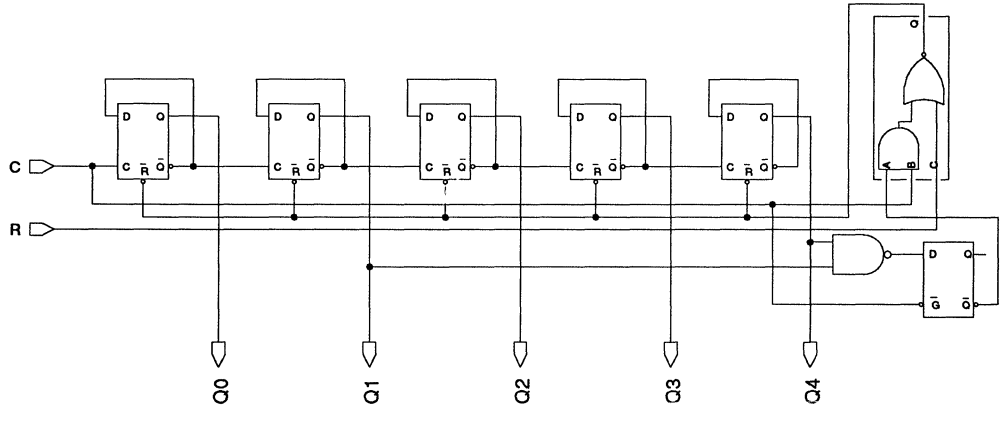
GSCM19BR



Description: GSCM19BR is a modulo 19 binary ripple counter, with reset.
Equivalent Gate Count: 36
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM19BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
H	X	L	L	L	L	L

Logic Schematic:



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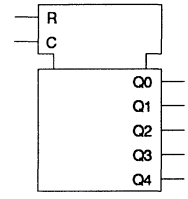
GSCM20BR

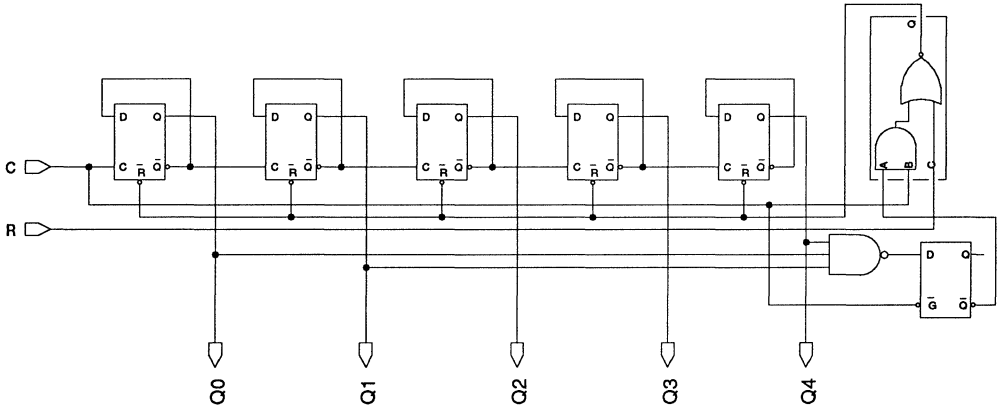
GSCM20BR



Description: GSCM20BR is a modulo 20 binary ripple counter, with reset.
Equivalent Gate Count: 37
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM20BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
H	X	L	L	L	L	L

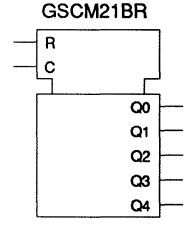
Logic Schematic:



MSI Functions

April, 1992

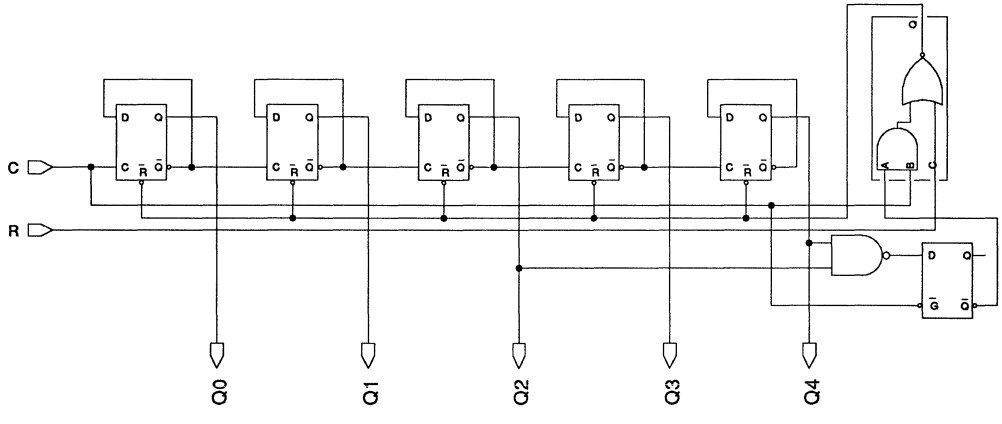
GSCM21BR



Description: GSCM21BR is a modulo 21 binary ripple counter, with reset.
Equivalent Gate Count: 36
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM21BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
H	X	L	L	L	L	L

Logic Schematic:



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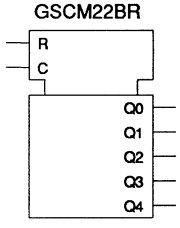
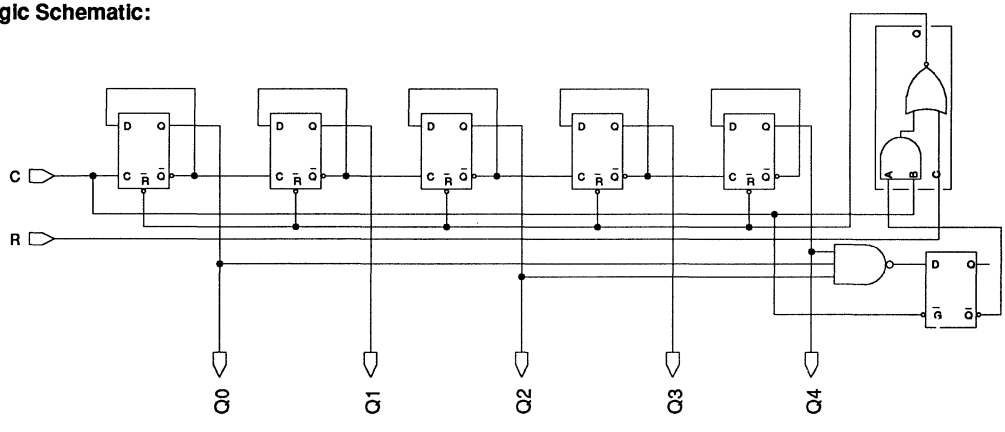
GSCM22BR



Description: GSCM22BR is a modulo 22 binary ripple counter, with reset.
Equivalent Gate Count: 37
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM22BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
L	↑	H	L	H	L	H
H	X	L	L	L	L	L

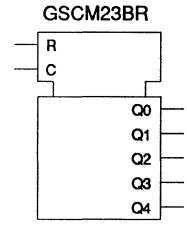
Logic Schematic:



MSI Functions

April, 1992

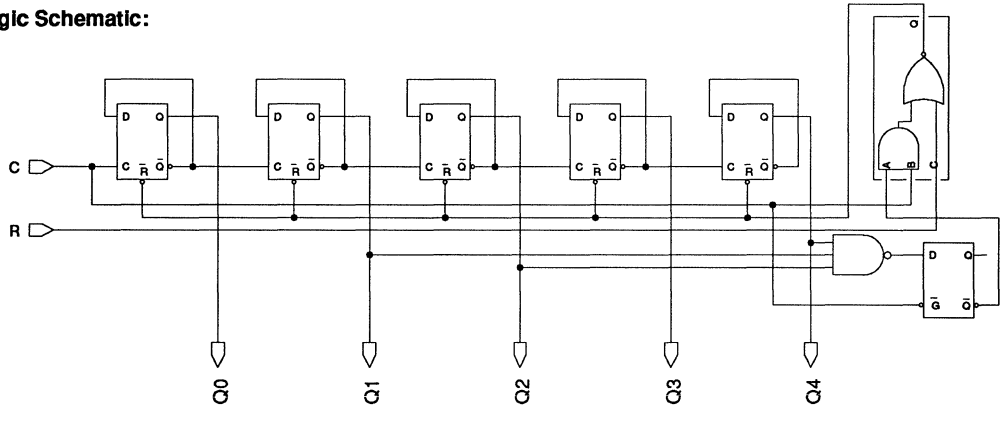
GSCM23BR



Description: GSCM23BR is a modulo 23 binary ripple counter, with reset.
Equivalent Gate Count: 37
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM23BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
L	↑	H	L	H	L	H
L	↑	L	H	H	L	H
H	X	L	L	L	L	L

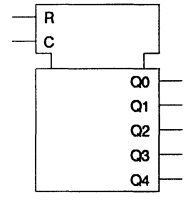
Logic Schematic:



April, 1992

GSCM24BR

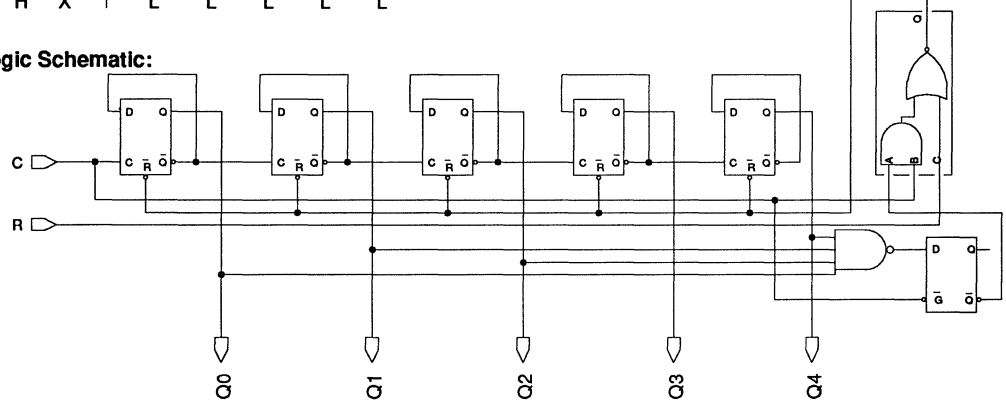
GSCM24BR



Description: GSCM24BR is a modulo 24 binary ripple counter, with reset.
Equivalent Gate Count: 37
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM24BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
L	↑	H	L	H	L	H
L	↑	L	H	H	L	H
L	↑	H	H	H	L	H
H	X	L	L	L	L	L

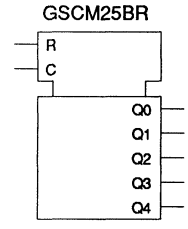
Logic Schematic:



MSI Functions

April, 1992

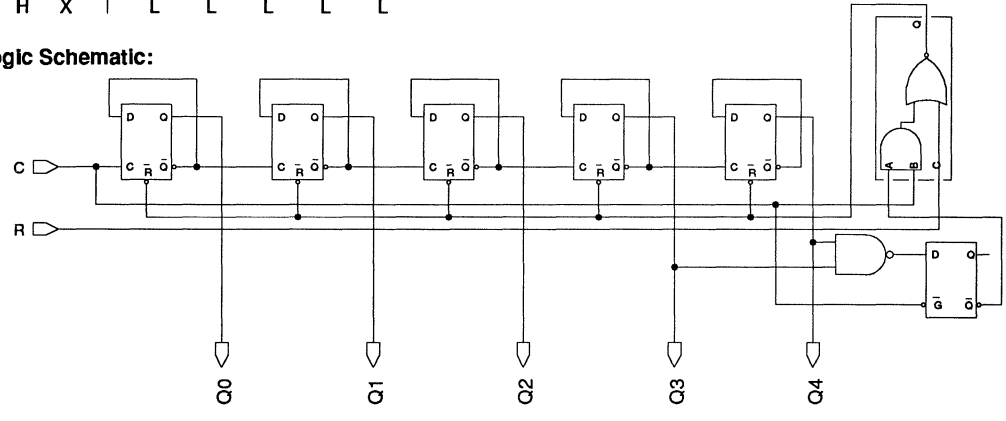
GSCM25BR



Description: GSCM25BR is a modulo 25 binary ripple counter, with reset.
Equivalent Gate Count: 36
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM25BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
L	↑	H	L	H	L	H
L	↑	L	H	H	L	H
L	↑	H	H	H	L	H
L	↑	L	L	L	H	H
H	X	L	L	L	L	L

Logic Schematic:



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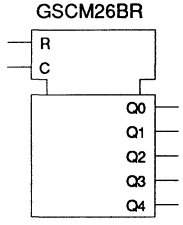
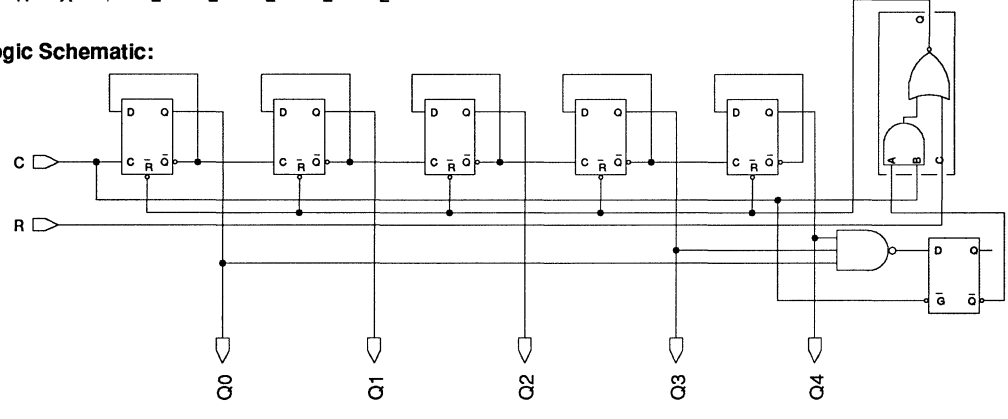
GSCM26BR



Description: GSCM26BR is a modulo 26 binary ripple counter, with reset.
Equivalent Gate Count: 37
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM26BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
L	↑	H	L	H	L	H
L	↑	L	H	H	L	H
L	↑	H	H	H	L	H
L	↑	L	L	L	H	H
L	↑	H	L	L	H	H
H	X	L	L	L	L	L

Logic Schematic:



MSI Functions

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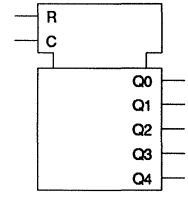
GSCM27BR

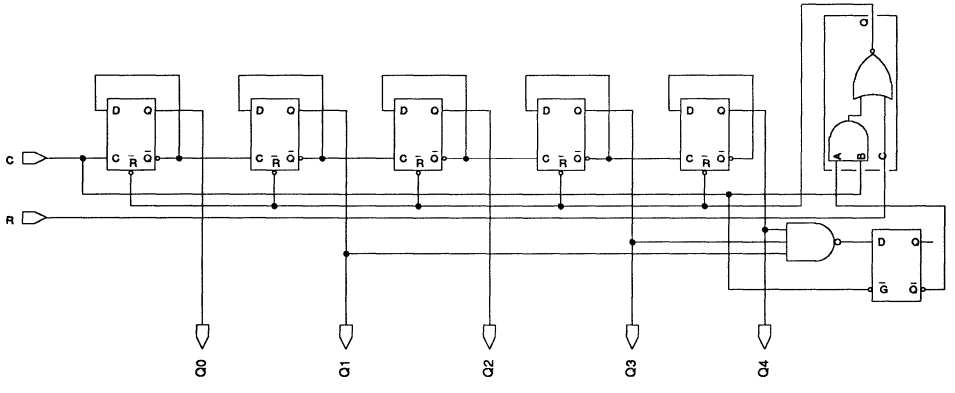
GSCM27BR



Description: GSCM27BR is a modulo 27 binary ripple counter, with reset.
Equivalent Gate Count: 37
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM27BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
L	↑	H	L	H	L	H
L	↑	L	H	H	L	H
L	↑	H	H	H	L	H
L	↑	L	L	L	H	H
L	↑	H	L	L	H	H
L	↑	L	H	L	H	H
H	X	L	L	L	L	L

Logic Schematic: On Next Page


C
R
D
Q
C
R
Q
A
B
C
D
Q
G
Q
Q0
Q1
Q2
Q3
Q4

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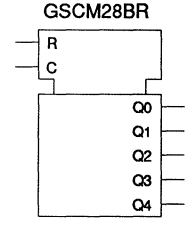
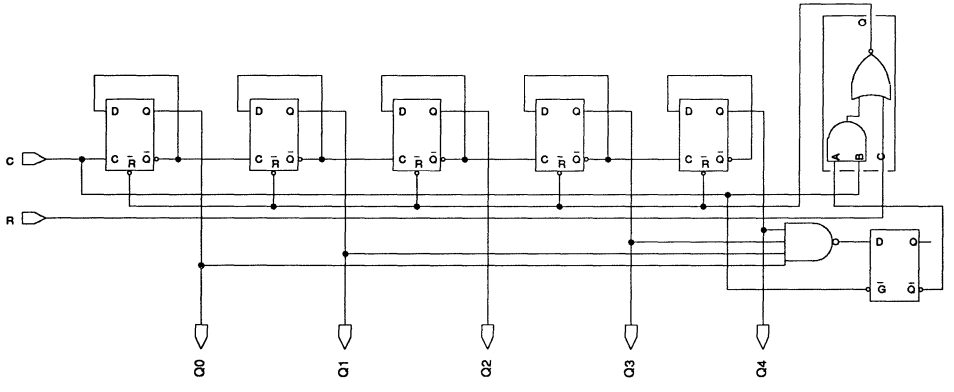
GSCM28BR



Description: GSCM28BR is a modulo 28 binary ripple counter, with reset.
Equivalent Gate Count: 37
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM28BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
L	↑	H	L	H	L	H
L	↑	L	H	H	L	H
L	↑	H	H	H	L	H
L	↑	L	L	L	H	H
L	↑	H	L	L	H	H
L	↑	L	H	L	H	H
L	↑	H	H	L	H	H
H	X	L	L	L	L	L

Logic Schematic: On Next Page


C
R
D
Q
C
R
Q
A
B
G
Q0
Q1
Q2
Q3
Q4

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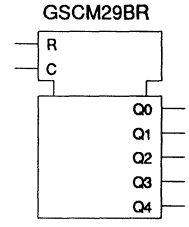
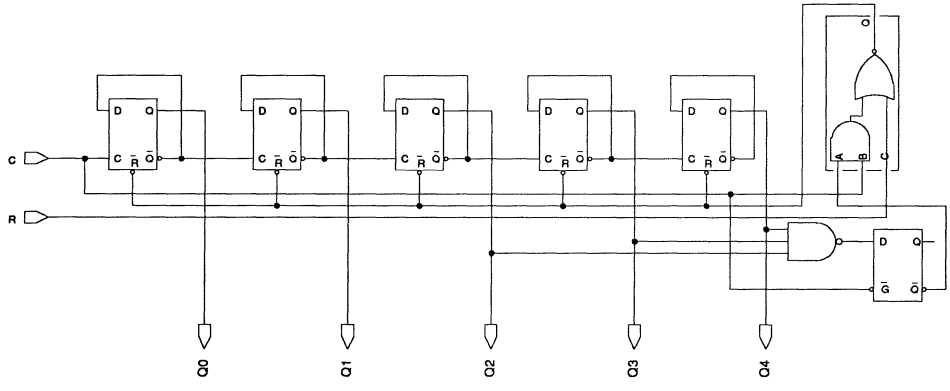
GSCM29BR



Description: GSCM29BR is a modulo 29 binary ripple counter, with reset.
Equivalent Gate Count: 37
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM29BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
L	↑	H	L	H	L	H
L	↑	L	H	H	L	H
L	↑	H	H	H	L	H
L	↑	L	L	L	H	H
L	↑	H	L	L	H	H
L	↑	L	H	L	H	H
L	↑	H	H	L	H	H
L	↑	L	L	H	H	H
H	X	L	L	L	L	L

Logic Schematic: On Next Page


C
R
D
Q
C
R
Q
Q0
Q1
Q2
Q3
Q4
A
B
C
G

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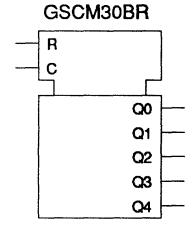
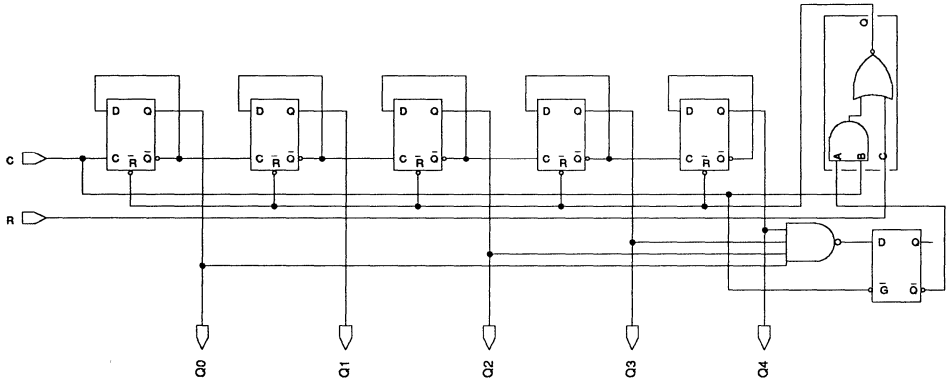
GSCM30BR



Description: GSCM30BR is a modulo 30 binary ripple counter, with reset.
Equivalent Gate Count: 37
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM30BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
L	↑	H	L	H	L	H
L	↑	L	H	H	L	H
L	↑	H	H	H	L	H
L	↑	L	L	L	H	H
L	↑	H	L	L	H	H
L	↑	L	H	L	H	H
L	↑	H	H	L	H	H
L	↑	L	L	H	H	H
L	↑	H	L	H	H	H
H	X	L	L	L	L	L

Logic Schematic: On Next Page


C
R
D
Q
C
R
Q
A
B
G
Q0
Q1
Q2
Q3
Q4

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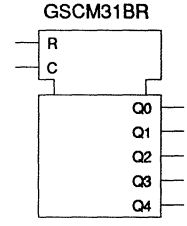
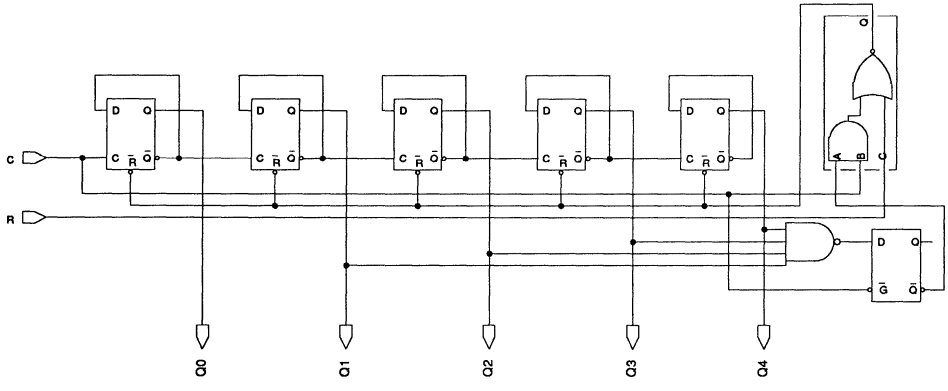
GSCM31BR



Description: GSCM31BR is a modulo 31 binary ripple counter, with reset.
Equivalent Gate Count: 37
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM31BR C R ;
Truth Table

R	C	Q0	Q1	Q2	Q3	Q4
L	↑	L	L	L	L	L
L	↑	H	L	L	L	L
L	↑	L	H	L	L	L
L	↑	H	H	L	L	L
L	↑	L	L	H	L	L
L	↑	H	L	H	L	L
L	↑	L	H	H	L	L
L	↑	H	H	H	L	L
L	↑	L	L	L	H	L
L	↑	H	L	L	H	L
L	↑	L	H	L	H	L
L	↑	H	H	L	H	L
L	↑	L	L	H	H	L
L	↑	H	L	H	H	L
L	↑	L	H	H	H	L
L	↑	H	H	H	H	L
L	↑	L	L	L	L	H
L	↑	H	L	L	L	H
L	↑	L	H	L	L	H
L	↑	H	H	L	L	H
L	↑	L	L	H	L	H
L	↑	H	L	H	L	H
L	↑	L	H	H	L	H
L	↑	H	H	H	L	H
L	↑	L	L	L	H	H
L	↑	H	L	L	H	H
L	↑	L	H	L	H	H
L	↑	H	H	L	H	H
L	↑	L	L	H	H	H
L	↑	H	L	H	H	H
L	↑	L	H	H	H	H
H	X	L	L	L	L	L

Logic Schematic: On Next Page


C
R
D
Q
C
R
Q
A
B
C
D
Q
G
Q
Q0
Q1
Q2
Q3
Q4

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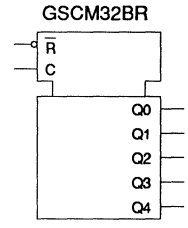
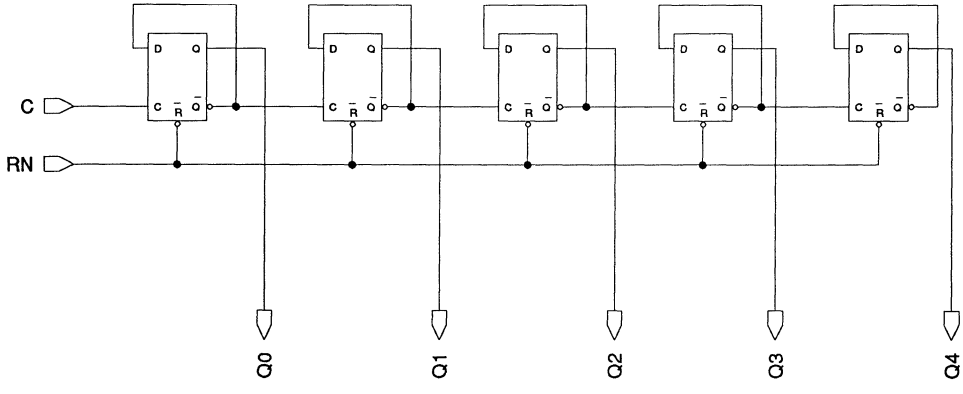
GSCM32BR



Description: GSCM32BR is a modulo 32 binary ripple counter, with reset not.
Equivalent Gate Count: 30
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 .GSCM32BR C RN ;
Truth Table

RN	C	Q0	Q1	Q2	Q3	Q4
H	↑	L	L	L	L	L
H	↑	H	L	L	L	L
H	↑	L	H	L	L	L
H	↑	H	H	L	L	L
H	↑	L	L	H	L	L
H	↑	H	L	H	L	L
H	↑	L	H	H	L	L
H	↑	H	H	H	L	L
H	↑	L	L	L	H	L
H	↑	H	L	L	H	L
H	↑	L	H	L	H	L
H	↑	H	H	L	H	L
H	↑	L	L	H	H	L
H	↑	H	L	H	H	L
H	↑	L	H	H	H	L
H	↑	H	H	H	H	L
H	↑	L	L	L	L	H
H	↑	H	L	L	L	H
H	↑	L	H	L	L	H
H	↑	H	H	L	L	H
H	↑	L	L	H	L	H
H	↑	H	L	H	L	H
H	↑	L	H	H	L	H
H	↑	H	H	H	L	H
H	↑	L	L	L	H	H
H	↑	H	L	L	H	H
H	↑	L	H	L	H	H
H	↑	H	H	L	H	H
H	↑	L	L	H	H	H
H	↑	H	L	H	H	H
H	↑	L	H	H	H	H
H	↑	H	H	H	H	H
L	X	L	L	L	L	L

Logic Schematic: On Next Page


C
RN
D
Q
C
R
Q
Q0
Q1
Q2
Q3
Q4

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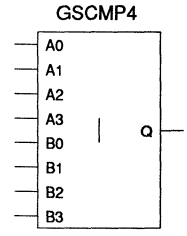
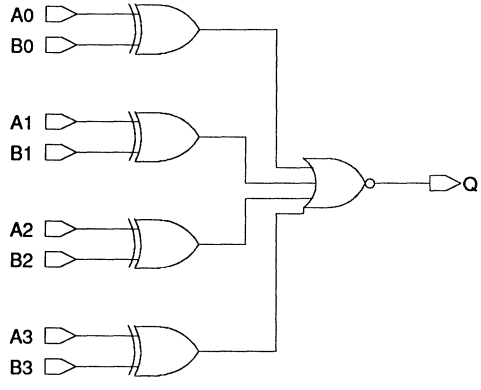
GSCMP4



Description: GSCMP4 is a 4 bit equality comparator.
Equivalent Gate Count: 14
Bolt Syntax: Q .GSCMP4 A0 B0 A1 B1 A2 B2 A3 B3 ;

Logic Schematic:



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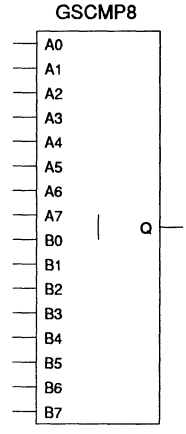
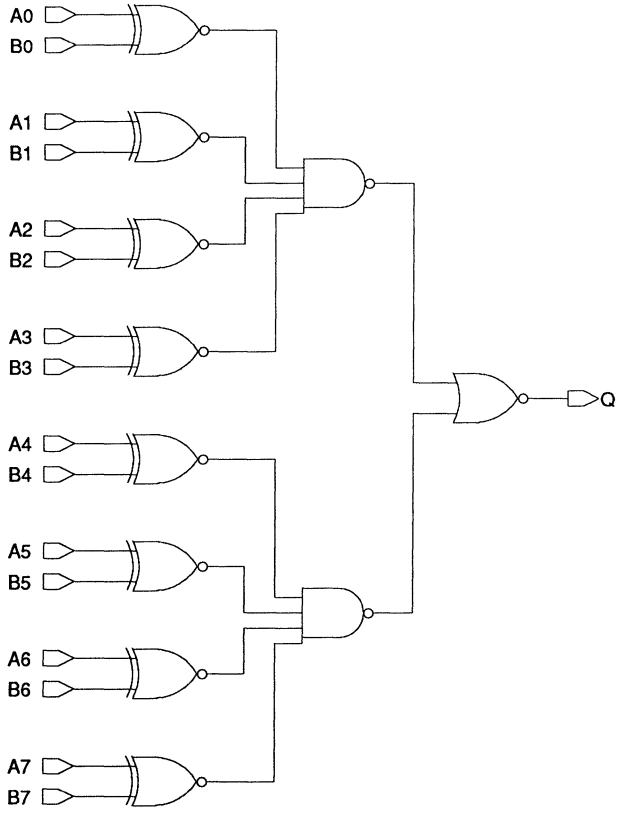
GSCMP8



Description: GSCMP8 is an 8 bit equality comparator.
Equivalent Gate Count: 29
Bolt Syntax: Q .GSCMP8 A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 ;

Logic Schematic:



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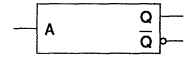
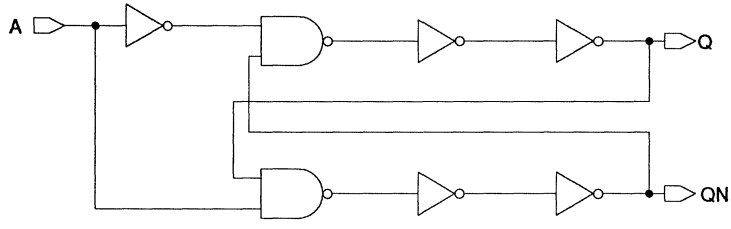
GSCPG1

GSCPG1



Description: GSCPG1 is a 2 phase clock generator, with positive underlap.
Equivalent Gate Count: 7
Bolt Syntax: Q QN .GSCPG1 A ;
Logic Schematic:



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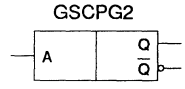
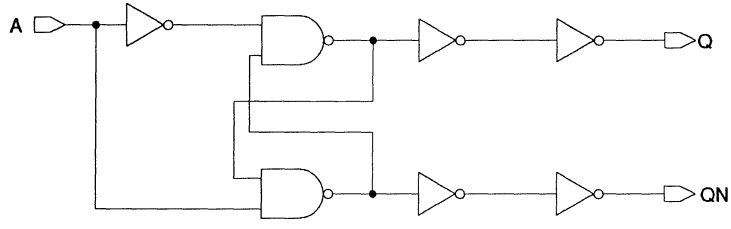
GSCPG2



Description: GSCPG2 is a 2 phase clock generator, with minimum underlap.
Equivalent Gate Count: 7
Bolt Syntax: Q QN .GSCPG2 A ;
Logic Schematic:



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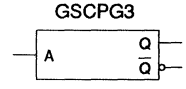
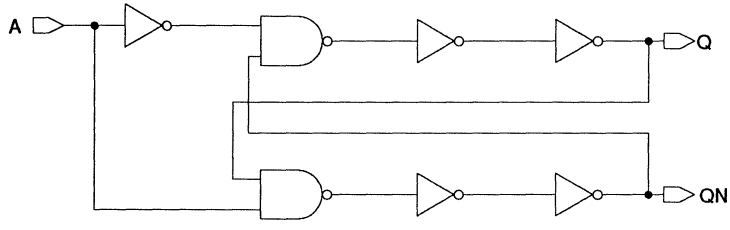
GSCPG3

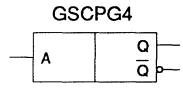


Description: GSCPG3 is a 2 phase clock generator, with positive underlap.
Equivalent Gate Count: 9
Bolt Syntax: Q QN .GSCPG3 A ;
Logic Schematic:

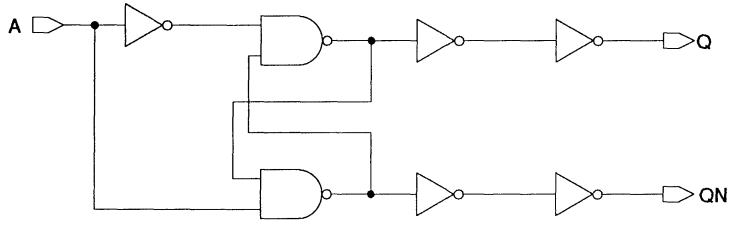


April, 1992

GSCPG4



Description: GSCPG4 is a 2 phase clock generator, with minimum underlap.
Equivalent Gate Count: 9
Bolt Syntax: Q QN .GSCPG4 A ;
Logic Schematic:



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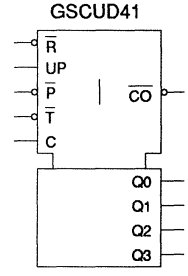
GSCUD41

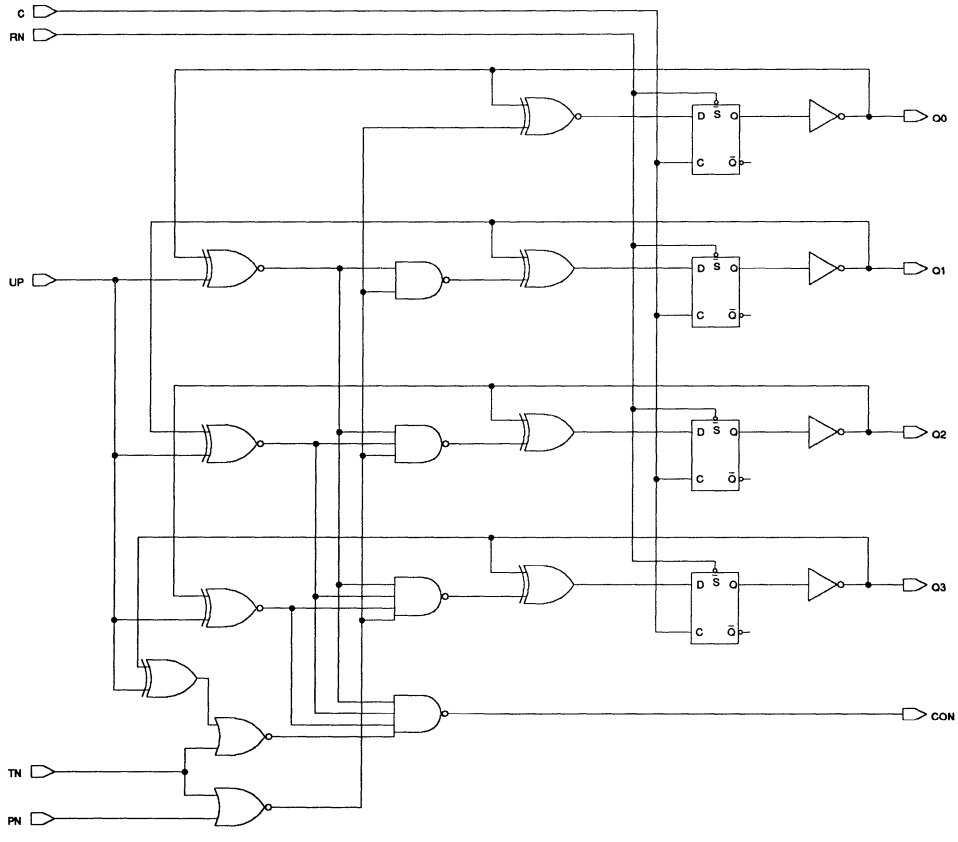


Description: GSCUD41 is a 4 bit up/down counter, with reset not.
Equivalent Gate Count: 61
Bolt Syntax: Q0 Q1 Q2 Q3 CON .GSCUD41 C PN TN UP RN ;
Truth Table

RN	PN	TN	UP	C	Q0	Q1	Q2	Q3	CON
L	X	X	X	X	L	L	L	L	LH
H	H	X	X	X	NC	NC	NC	NC	NC
H	X	H	X	X	NC	NC	NC	NC	H
H	L	L	H	↑	CU	CU	CU	CU	LH
H	L	L	L	↑	CD	CD	CD	CD	LH

NC = No Change
CD = Count Down
CU = Count Up
LH = Q0 • Q1 • Q2 • Q3 • TN, if (UP = H)
LH = Q0N • Q1N • Q2N • Q3N • TN, if (UP = L)

Logic Schematic: On Next Page


C
RN
UP
TN
PN
D S Q
C Q̄
Q0
Q1
Q2
Q3
CON

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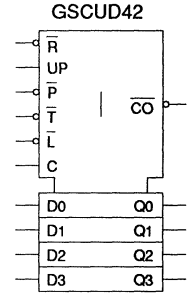
GSCUD42



Description: GSCUD42 is a 4 bit up/down counter, with reset not.

Equivalent Gate Count: 79

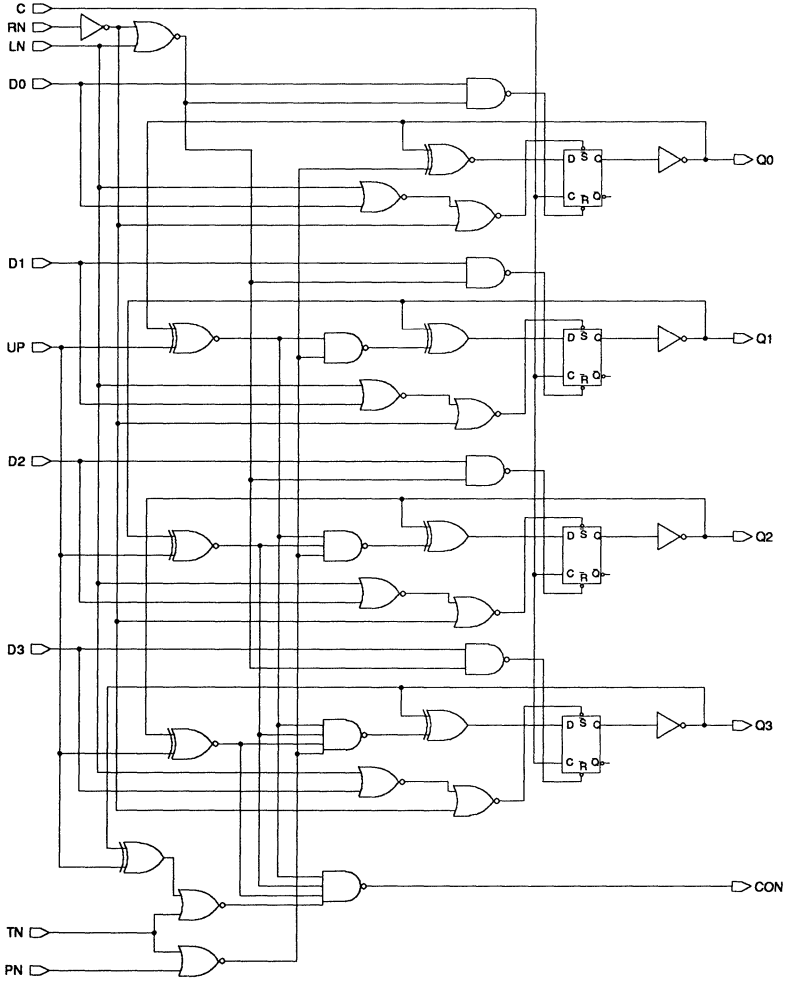
Bolt Syntax: Q0 Q1 Q2 Q3 CON .GSCUD42 D0 D1 D2 D3 LN RN C PN TN UP ;

Truth Table

RN	PN	TN	UP	LN	D0	D1	D2	D3	C	Q0	Q1	Q2	Q3	CON
L	X	X	X	X	X	X	X	X	X	L	L	L	L	LH
H	H	X	X	H	X	X	X	X	X	NC	NC	NC	NC	NC
H	X	H	X	H	X	X	X	X	X	NC	NC	NC	NC	H
H	L	L	H	H	X	X	X	X	↑	CU	CU	CU	CU	LH
H	L	L	L	H	X	X	X	X	↑	CD	CD	CD	CD	LH
H	X	X	X	L	D0	D1	D2	D3	X	D0	D1	D2	D3	LH

NC = No Change
CD = Count Down
CU = Count Up
LH = Q0 • Q1 • Q2 • Q3 • TN, if (UP = H)
LH = Q0N • Q1N • Q2N • Q3N • TN, if (UP = L)

Logic Schematic: On Next Page


C
RN
LN
D0
D1
UP
D2
D3
TN
PN
Q0
Q1
Q2
Q3
CON
D
S
C
R
Q

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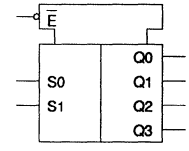
GSD24GH

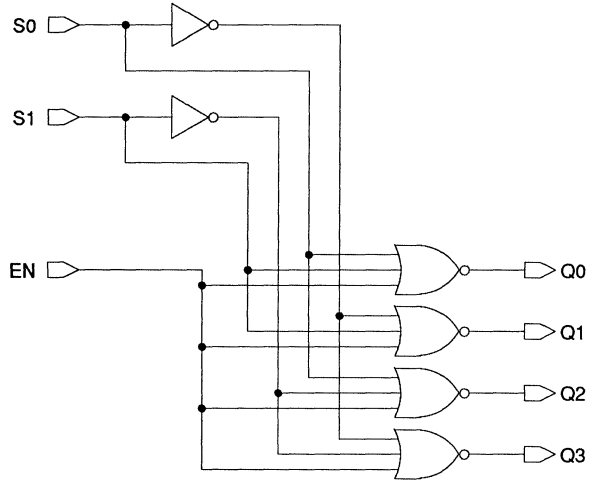
GSD24GH



Description: GSD24GH is a 2 to 4 decoder, active high outputs, with active low enable.
Equivalent Gate Count: 10
Bolt Syntax: Q0 Q1 Q2 Q3 .GSD24GH S0 S1 EN ;
Truth Table

EN	S0	S1	Q0	Q1	Q2	Q3
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

Logic Schematic:



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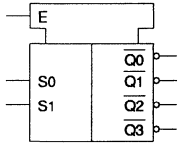
GSD24GL

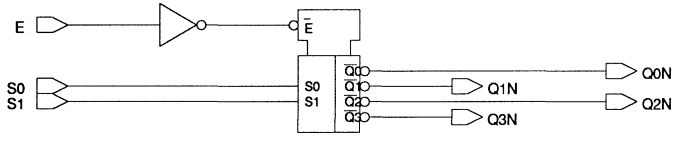
GSD24GL



Description: GSD24GL is a 2 to 4 decoder, active low outputs, with active high enable.
Equivalent Gate Count: 9
Bolt Syntax: Q0N Q1N Q2N Q3N .GSD24GL S0 S1 E ;
Truth Table

E	S0	S1	Q0N	Q1N	Q2N	Q3N
H	L	L	L	H	H	H
H	H	L	H	L	H	H
H	L	H	H	H	L	H
H	H	H	H	H	H	L
L	X	X	H	H	H	H

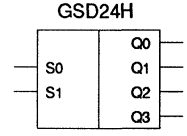
Logic Schematic:



MSI Functions

April, 1992

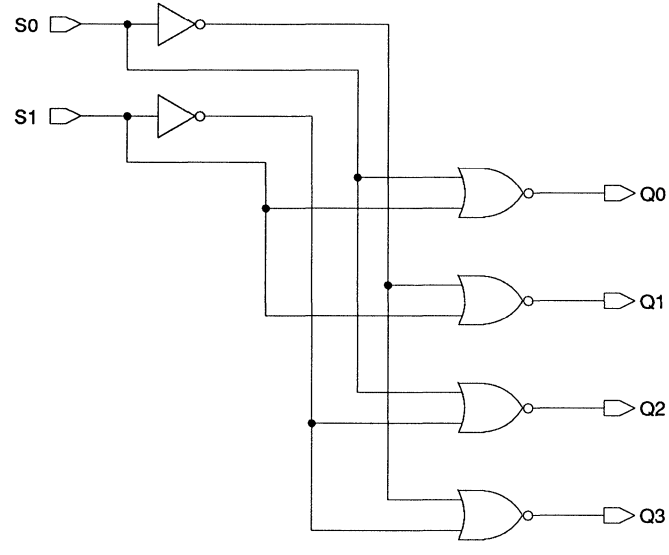
GSD24H



Description: GSD24H is a 2 to 4 decoder, active high outputs.
Equivalent Gate Count: 6
Bolt Syntax: Q0 Q1 Q2 Q3 .GSD24H S0 S1 ;
Truth Table

S0	S1	Q0	Q1	Q2	Q3
L	L	H	L	L	L
H	L	L	H	L	L
L	H	L	L	H	L
H	H	L	L	L	H

Logic Schematic:



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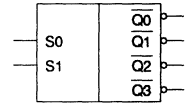
GSD24L

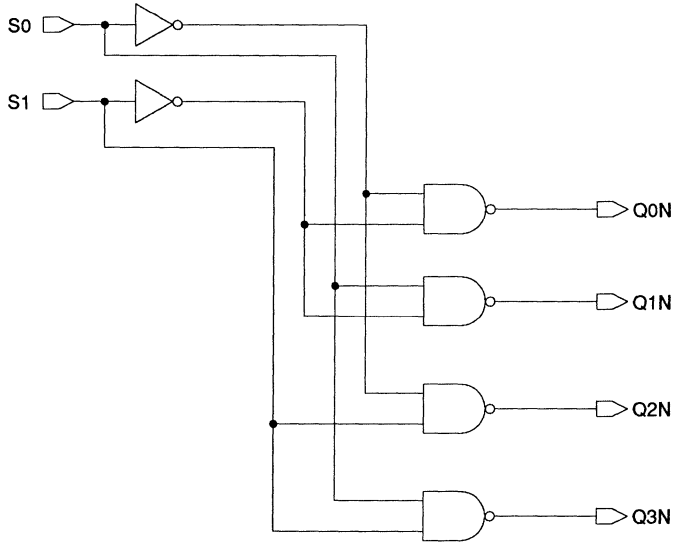
GSD24L



Description: GSD24L is a 2 to 4 decoder, active low outputs.
Equivalent Gate Count: 6
Bolt Syntax: Q0N Q1N Q2N Q3N .GSD24L S0 S1 ;
Truth Table

S0	S1	Q0N	Q1N	Q2N	Q3N
L	L	L	H	H	H
H	L	H	L	H	H
L	H	H	H	L	H
H	H	H	H	H	L

Logic Schematic:



MSI Functions

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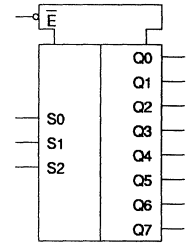
GSD38GH

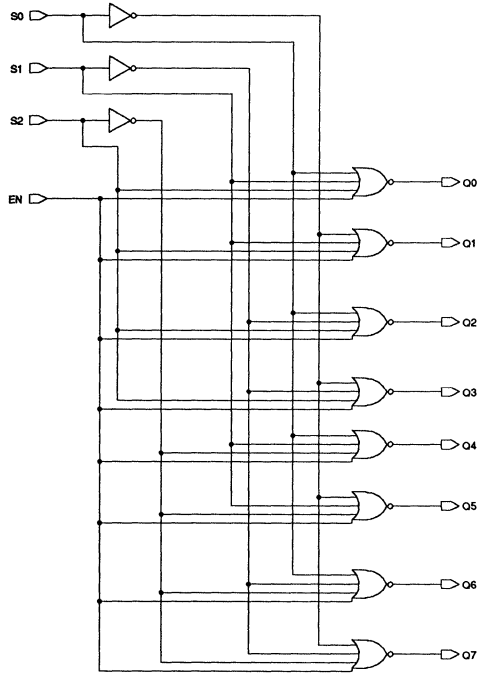
GSD38GH



Description: GSD38GH is a 3 to 8 decoder, active high outputs, with active low enable.
Equivalent Gate Count: 19
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 .GSD38GH S0 S1 S2 EN ;
Truth Table

EN	S0	S1	S2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L
L	H	H	L	L	L	L	H	L	L	L	L
L	L	L	H	L	L	L	L	H	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	H	L
L	H	H	H	L	L	L	L	L	L	L	H
H	X	X	X	L	L	L	L	L	L	L	L

Logic Schematic:



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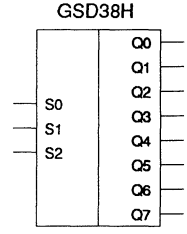
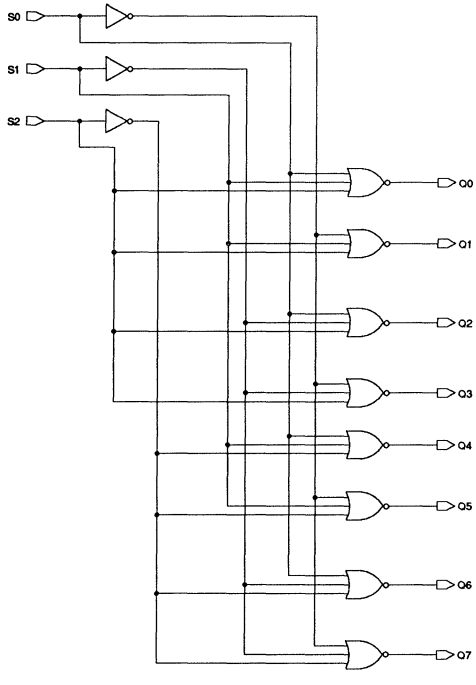
GSD38H



Description: GSD38H is a 3 to 8 decoder, active high outputs.
Equivalent Gate Count: 19
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 .GSD38H S0 S1 S2 ;
Truth Table

S0	S1	S2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	L	L	L	L	L
L	H	L	L	L	H	L	L	L	L	L
H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L
H	L	H	L	L	L	L	L	H	L	L
L	H	H	L	L	L	L	L	L	H	L
H	H	H	L	L	L	L	L	L	L	H

Logic Schematic:



MSI Functions

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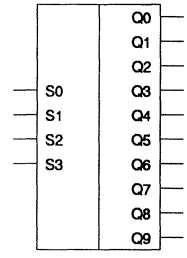
GSD410H

GSD410H



Description: GSD410H is a 4 to 10 decoder, active high outputs.

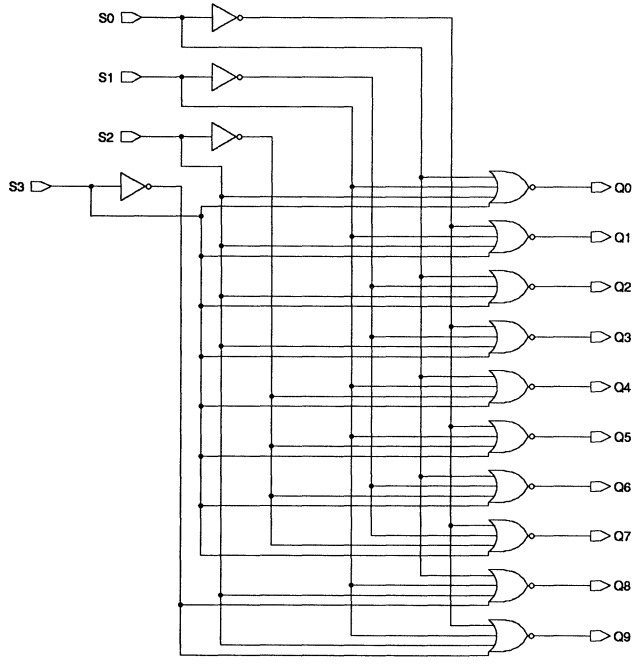
Equivalent Gate Count: 24

Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 .GSD410H S0 S1 S2 S3 ;

Truth Table

S0	S1	S2	S3	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9
L	L	L	L	H	L	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
H	H	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	L	L	L	L	H	L	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L	L
L	H	H	L	L	L	L	L	L	L	H	L	L	L
H	H	H	L	L	L	L	L	L	L	L	H	L	L
L	L	L	H	L	L	L	L	L	L	L	L	H	L
H	L	L	H	L	L	L	L	L	L	L	L	L	H
X	H	X	H	L	L	L	L	L	L	L	L	L	L
X	X	H	H	L	L	L	L	L	L	L	L	L	L

Logic Schematic:



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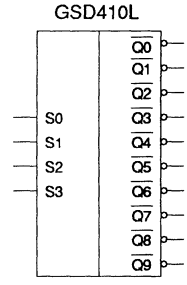
GSD410L



Description: GSD410L is a 4 to 10 decoder, active low outputs.

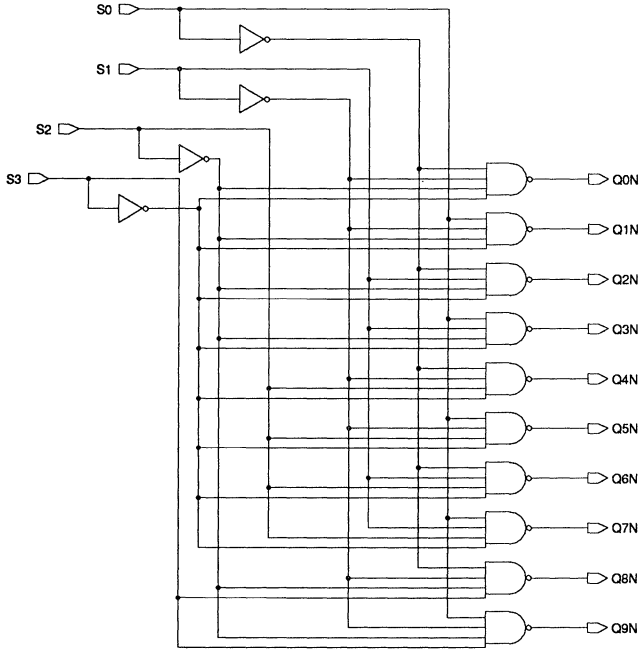
Equivalent Gate Count: 24

Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N Q8N Q9N .GSD410L S0 S1 S2 S3 ;

Truth Table

S0	S1	S2	S3	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N	Q8N	Q9N
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
X	H	X	H	H	H	H	H	H	H	H	H	H	H
X	X	H	H	H	H	H	H	H	H	H	H	H	H

Logic Schematic:



MSI Functions

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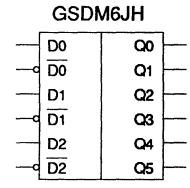
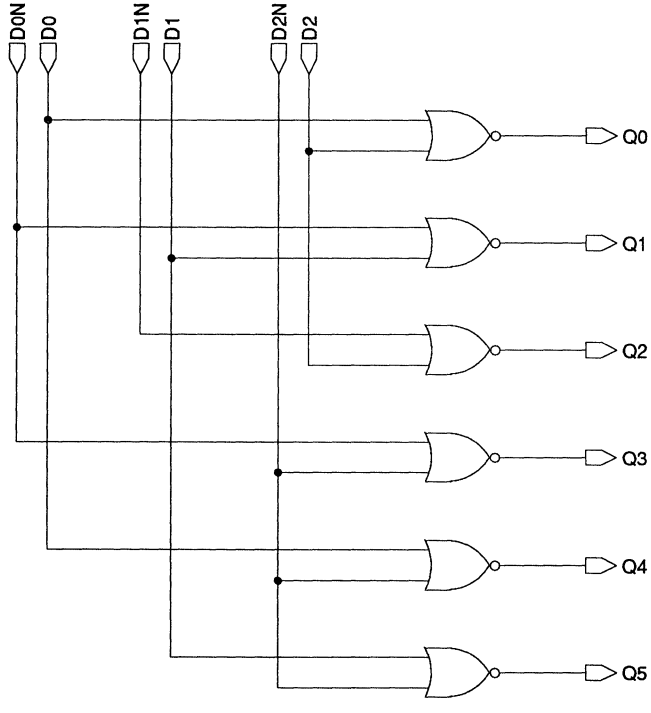
GSDM6JH



Description: GSDM6JH is an active high glitch free decoder for a modulo 6 Johnson counter.
Equivalent Gate Count: 6
Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 .GSDM6JH D0 D0N D1 D1N D2 D2N ;
Truth Table

D0	D1	D2	HIGH-OUTPUT
L	L	L	Q0
H	L	L	Q1
H	H	L	Q2
H	H	H	Q3
L	H	H	Q4
L	L	H	Q5

Logic Schematic:



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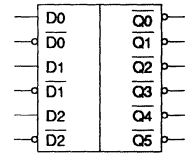
GSDM6JL

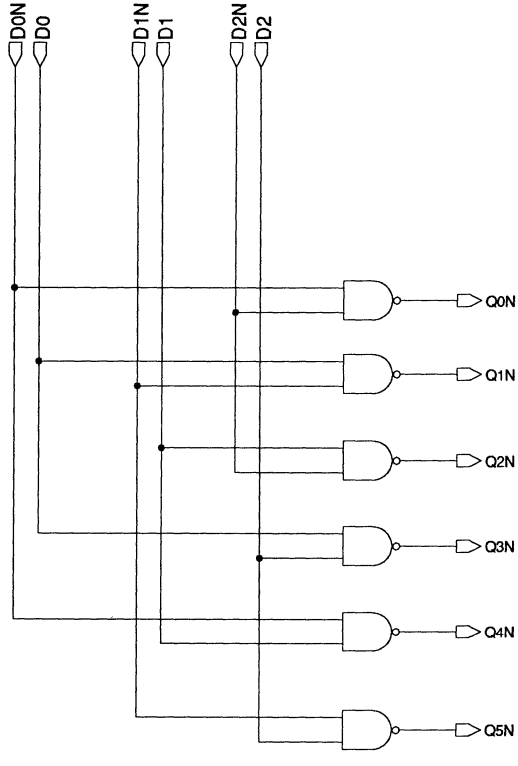
GSDM6JL



Description: GSDM6JL is an active low glitch free decoder for a modulo 6 Johnson counter.
Equivalent Gate Count: 6
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N .GSDM6JL D0 D0N D1 D1N D2 D2N ;
Truth Table

D0	D1	D2	LOW-OUTPUT
L	L	L	Q0N
H	L	L	Q1N
H	H	L	Q2N
H	H	H	Q3N
L	H	H	Q4N
L	L	H	Q5N

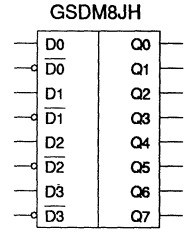
Logic Schematic:



MSI Functions

April, 1992

GSDM8JH



Description: GSDM8JH is an active high glitch free decoder for a modulo 8 Johnson counter.

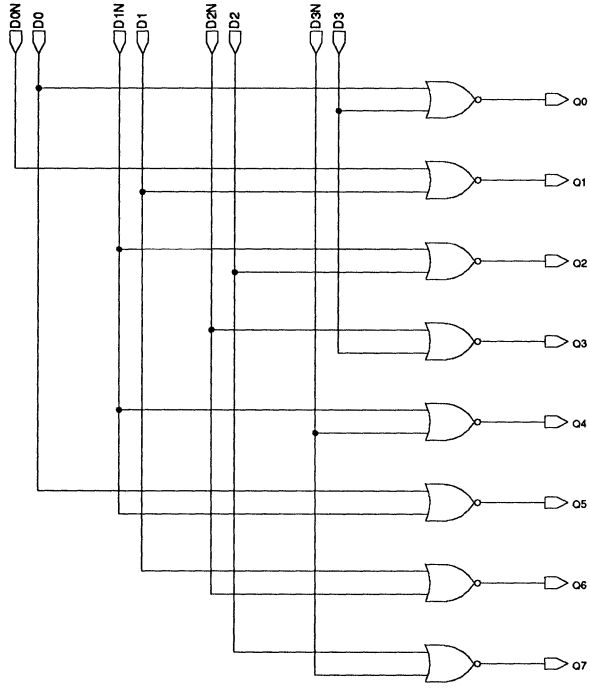
Equivalent Gate Count: 8

Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 .GSDM8JH D0 D0N D1 D1N D2 D2N D3 D3N ;

Truth Table

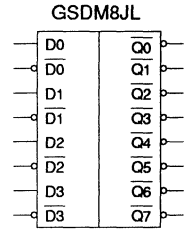
D0	D1	D2	D3	HIGH-OUTPUT
L	L	L	L	Q0
H	L	L	L	Q1
H	H	L	L	Q2
H	H	H	L	Q3
H	H	H	H	Q4
L	H	H	H	Q5
L	L	H	H	Q6
L	L	L	H	Q7

Logic Schematic:



April, 1992

GSDM8JL



Description: GSDM8JL is an active low glitch free decoder for a modulo 8 Johnson counter.

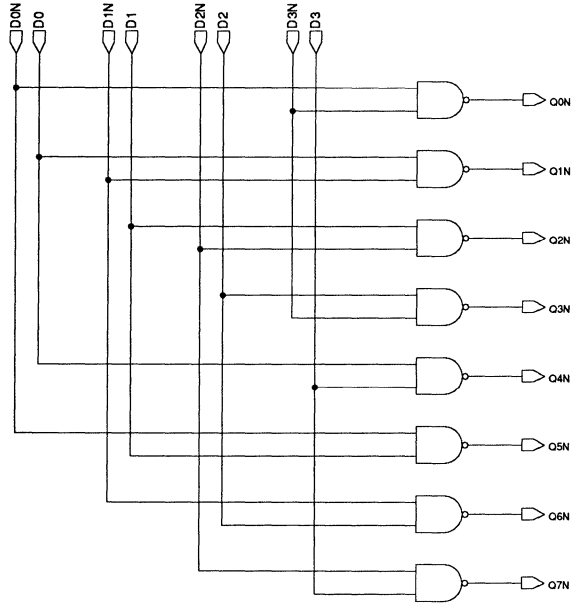
Equivalent Gate Count: 8

Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N .GSDM8JL D0 D0N D1 D1N D2 D2N D3 D3N ;

Truth Table

D0	D1	D2	D3	LOW-OUTPUT
L	L	L	L	Q0N
H	L	L	L	Q1N
H	H	L	L	Q2N
H	H	H	L	Q3N
H	H	H	H	Q4N
L	H	H	H	Q5N
L	L	H	H	Q6N
L	L	L	H	Q7N

Logic Schematic:

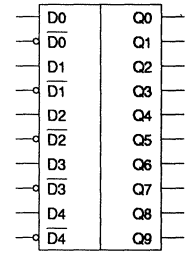


MSI Functions

April, 1992

GSDM10JH

GSDM10JH



Description: GSDM10JH is an active high glitch free decoder for a modulo 10 Johnson counter.

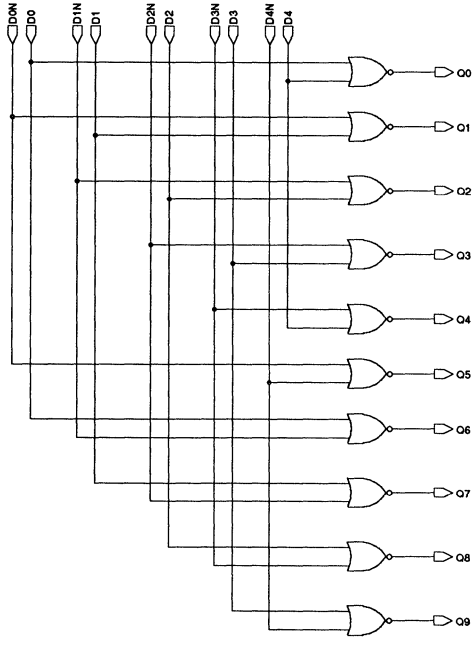
Equivalent Gate Count: 10

Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 .GSDM10JH D0 D0N D1 D1N D2 D2N D3 D3N D4 D4N ;

Truth Table

D0	D1	D2	D3	D4	HIGH-OUTPUT
L	L	L	L	L	Q0
H	L	L	L	L	Q1
H	H	L	L	L	Q2
H	H	H	L	L	Q3
H	H	H	H	L	Q4
H	H	H	H	H	Q5
L	H	H	H	H	Q6
L	L	H	H	H	Q7
L	L	L	H	H	Q8
L	L	L	L	H	Q9

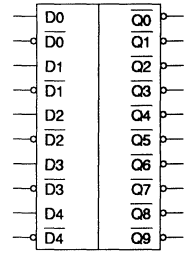
Logic Schematic:



April, 1992

GSDM10JL

GSDM10JL



Description: GSDM10JL is an active low glitch free decoder for a modulo 10 Johnson counter.

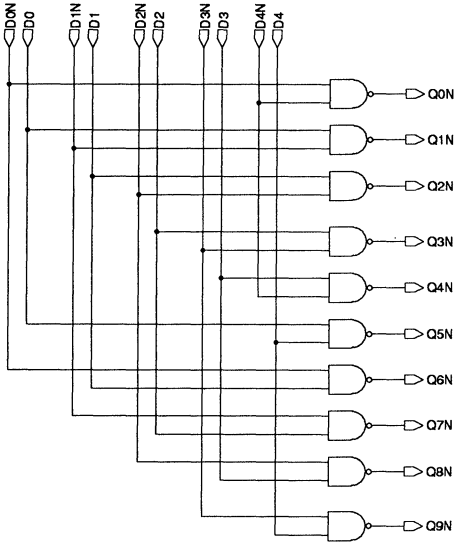
Equivalent Gate Count: 10

Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N Q8N Q9N .GSDM10JL D0 D0N D1 D1N D2 D2N D3 D3N D4 D4N ;

Truth Table

D0	D1	D2	D3	D4	LOW-OUTPUT
L	L	L	L	L	Q0N
H	L	L	L	L	Q1N
H	H	L	L	L	Q2N
H	H	H	L	L	Q3N
H	H	H	H	L	Q4N
H	H	H	H	H	Q5N
L	H	H	H	H	Q6N
L	L	H	H	H	Q7N
L	L	L	H	H	Q8N
L	L	L	L	H	Q9N

Logic Schematic:

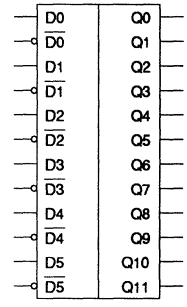


MSI Functions

April, 1992

GSDM12JH

GSDM12JH



Description: GSDM12JH is an active high glitch free decoder for a modulo 12 Johnson counter.

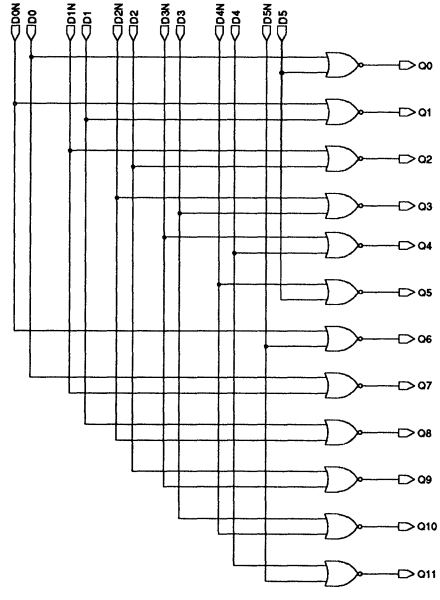
Equivalent Gate Count: 12

Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 .GSDM12JH D0 D0N D1 D1N D2 D2N D3 D3N D4 D4N D5 D5N ;

Truth Table

D0	D1	D2	D3	D4	D5	HIGH-OUTPUT
L	L	L	L	L	L	Q0
H	L	L	L	L	L	Q1
H	H	L	L	L	L	Q2
H	H	H	L	L	L	Q3
H	H	H	H	L	L	Q4
H	H	H	H	H	L	Q5
H	H	H	H	H	H	Q6
L	H	H	H	H	H	Q7
L	L	H	H	H	H	Q8
L	L	L	H	H	H	Q9
L	L	L	L	H	H	Q10
L	L	L	L	L	H	Q11

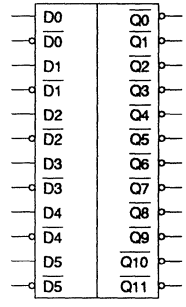
Logic Schematic:



April, 1992

GSDM12JL

GSDM12JL



Description: GSDM12JL is an active low glitch free decoder for a modulo 12 Johnson counter.

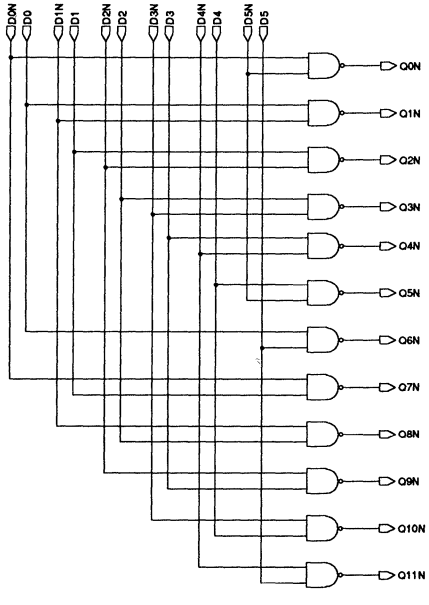
Equivalent Gate Count: 12

Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N Q8N Q9N Q10N Q11N
.GSDM12JL D0 D0N D1 D1N D2 D2N D3 D3N D4 D4N D5 D5N ;

Truth Table

D0	D1	D2	D3	D4	D5	LOW-OUTPUT
L	L	L	L	L	L	Q0N
H	L	L	L	L	L	Q1N
H	H	L	L	L	L	Q2N
H	H	H	L	L	L	Q3N
H	H	H	H	L	L	Q4N
H	H	H	H	H	L	Q5N
H	H	H	H	H	H	Q6N
L	H	H	H	H	H	Q7N
L	L	H	H	H	H	Q8N
L	L	L	H	H	H	Q9N
L	L	L	L	H	H	Q10N
L	L	L	L	L	H	Q11N

Logic Schematic:



MSI Functions

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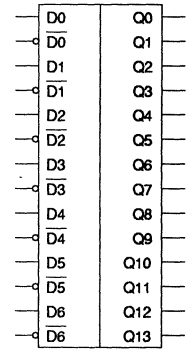
GSDM14JH

GSDM14JH



Description: GSDM14JH is an active high glitch free decoder for a modulo 14 Johnson counter.

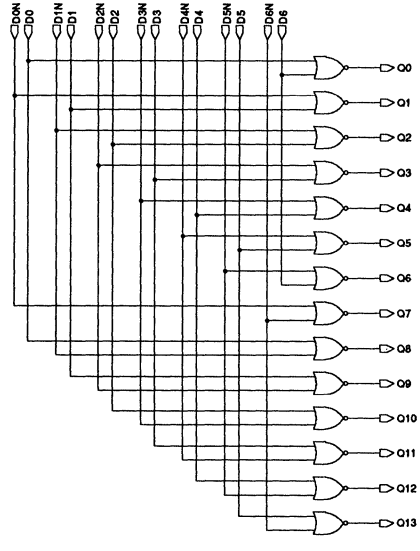
Equivalent Gate Count: 14

Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 .GSDM14JH D0 D0N D1 D1N D2 D2N D3 D3N D4 D4N D5 D5N D6 D6N ;

Truth Table

D0	D1	D2	D3	D4	D5	D6	HIGH-OUTPUT
L	L	L	L	L	L	L	Q0
H	L	L	L	L	L	L	Q1
H	H	L	L	L	L	L	Q2
H	H	H	L	L	L	L	Q3
H	H	H	H	L	L	L	Q4
H	H	H	H	H	L	L	Q5
H	H	H	H	H	H	L	Q6
H	H	H	H	H	H	H	Q7
L	H	H	H	H	H	H	Q8
L	L	H	H	H	H	H	Q9
L	L	L	H	H	H	H	Q10
L	L	L	L	H	H	H	Q11
L	L	L	L	L	H	H	Q12
L	L	L	L	L	L	H	Q13

Logic Schematic:



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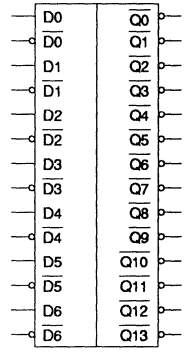
GSDM14JL

GSDM14JL



Description: GSDM14JL is an active low glitch free decoder for a modulo 14 Johnson counter.

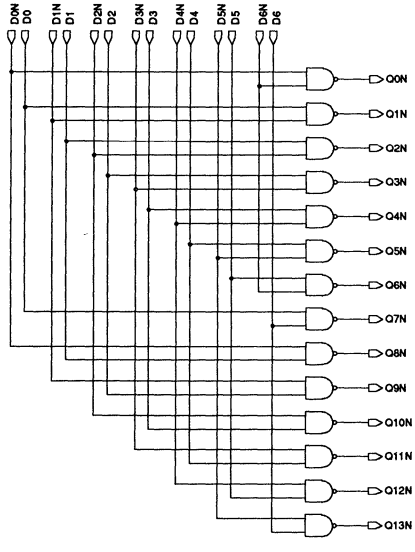
Equivalent Gate Count: 14

Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N Q8N Q9N Q10N Q11N Q12N Q13N .GSDM14JL D0 D0N D1 D1N D2 D2N D3 D3N D4 D4N D5 D5N D6 D6N ;

Truth Table

D0	D1	D2	D3	D4	D5	D6	LOW-OUTPUT
L	L	L	L	L	L	L	Q0N
H	L	L	L	L	L	L	Q1N
H	H	L	L	L	L	L	Q2N
H	H	H	L	L	L	L	Q3N
H	H	H	H	L	L	L	Q4N
H	H	H	H	H	L	L	Q5N
H	H	H	H	H	H	L	Q6N
H	H	H	H	H	H	H	Q7N
L	H	H	H	H	H	H	Q8N
L	L	H	H	H	H	H	Q9N
L	L	L	H	H	H	H	Q10N
L	L	L	L	H	H	H	Q11N
L	L	L	L	L	H	H	Q12N
L	L	L	L	L	L	H	Q13N

Logic Schematic:



MSI Functions

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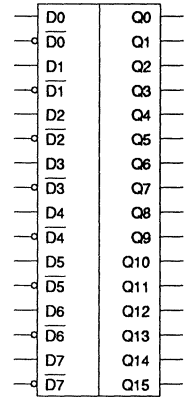
GSDM16JH

GSDM16JH



Description: GSDM16JH is an active high glitch free decoder for a modulo 16 Johnson counter.

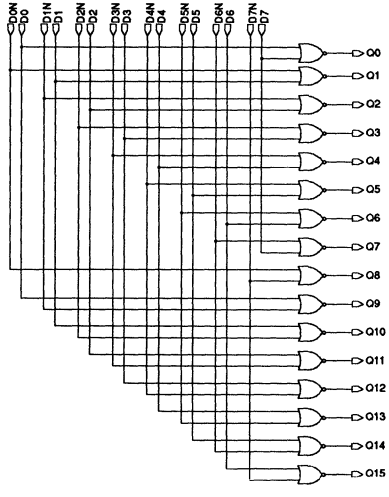
Equivalent Gate Count: 16

Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15
.GSDM16JH D0 D0N D1 D1N D2 D2N D3 D3N D4 D4N D5 D5N D6 D6N D7 D7N ;

Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	HIGH-OUTPUT
L	L	L	L	L	L	L	L	Q0
H	L	L	L	L	L	L	L	Q1
H	H	L	L	L	L	L	L	Q2
H	H	H	L	L	L	L	L	Q3
H	H	H	H	L	L	L	L	Q4
H	H	H	H	H	L	L	L	Q5
H	H	H	H	H	H	L	L	Q6
H	H	H	H	H	H	H	L	Q7
H	H	H	H	H	H	H	H	Q8
L	H	H	H	H	H	H	H	Q9
L	L	H	H	H	H	H	H	Q10
L	L	L	H	H	H	H	H	Q11
L	L	L	L	H	H	H	H	Q12
L	L	L	L	L	H	H	H	Q13
L	L	L	L	L	L	H	H	Q14
L	L	L	L	L	L	L	H	Q15

Logic Schematic:



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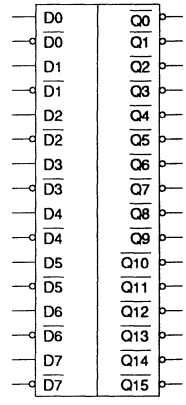
GSDM16JL

GSDM16JL



Description: GSDM16JL is an active low glitch free decoder for a modulo 16 Johnson counter.

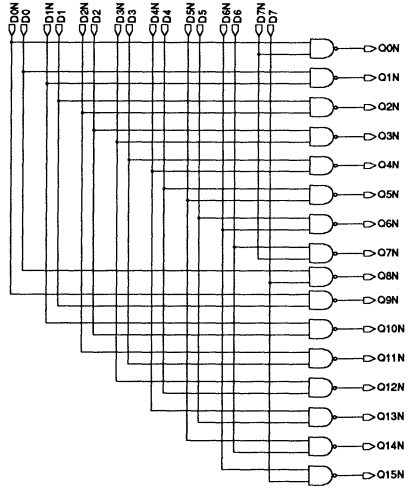
Equivalent Gate Count: 16

Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N Q8N Q9N Q10N Q11N Q12N Q13N Q14N Q15N .GSDM16JL D0 D0N D1 D1N D2 D2N D3 D3N D4 D4N D5 D5N D6 D6N D7 D7N ;

Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	LOW-OUTPUT
L	L	L	L	L	L	L	L	Q0N
H	L	L	L	L	L	L	L	Q1N
H	H	L	L	L	L	L	L	Q2N
H	H	H	L	L	L	L	L	Q3N
H	H	H	H	L	L	L	L	Q4N
H	H	H	H	H	L	L	L	Q5N
H	H	H	H	H	H	L	L	Q6N
H	H	H	H	H	H	H	L	Q7N
H	H	H	H	H	H	H	H	Q8N
L	H	H	H	H	H	H	H	Q9N
L	L	H	H	H	H	H	H	Q10N
L	L	L	H	H	H	H	H	Q11N
L	L	L	L	H	H	H	H	Q12N
L	L	L	L	L	H	H	H	Q13N
L	L	L	L	L	L	H	H	Q14N
L	L	L	L	L	L	L	H	Q15N

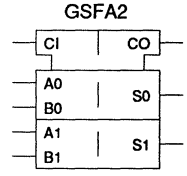
Logic Schematic:



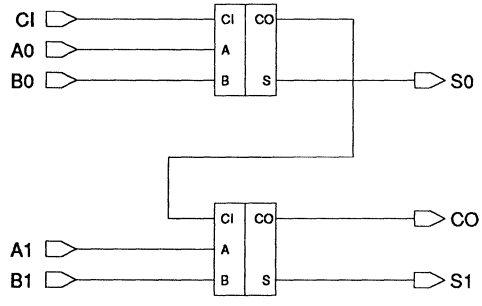
MSI Functions

April, 1992

GSFA2



Description: GSFA2 is a 2 bit full adder.
Equivalent Gate Count: 14
Bolt Syntax: S0 S1 CO .GSFA2 CI A0 B0 A1 B1 ;
Truth Equation: S0 = Sum of A0, B0, and CI
S1 = Sum of A1, B1, and the carry of S0
CO = Carry of the sum of A1, B1, and the carry of S0
Logic Schematic:



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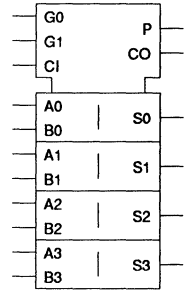
GSFA4

GSFA4



Description: GSFA4 is a 4 bit binary full adder. This adder is designed to be used in conjunction with a carry look ahead circuit.

Equivalent Gate Count: 42

Bolt Syntax: S0 S1 S2 S3 CO P .GSFA4 CI A0 B0 G0 A1 B1 G1 A2 B2 A3 B3 ;

Truth Equation: S0 = Sum of A0, B0, and CI

S1 = Sum of A1, B1, and G0

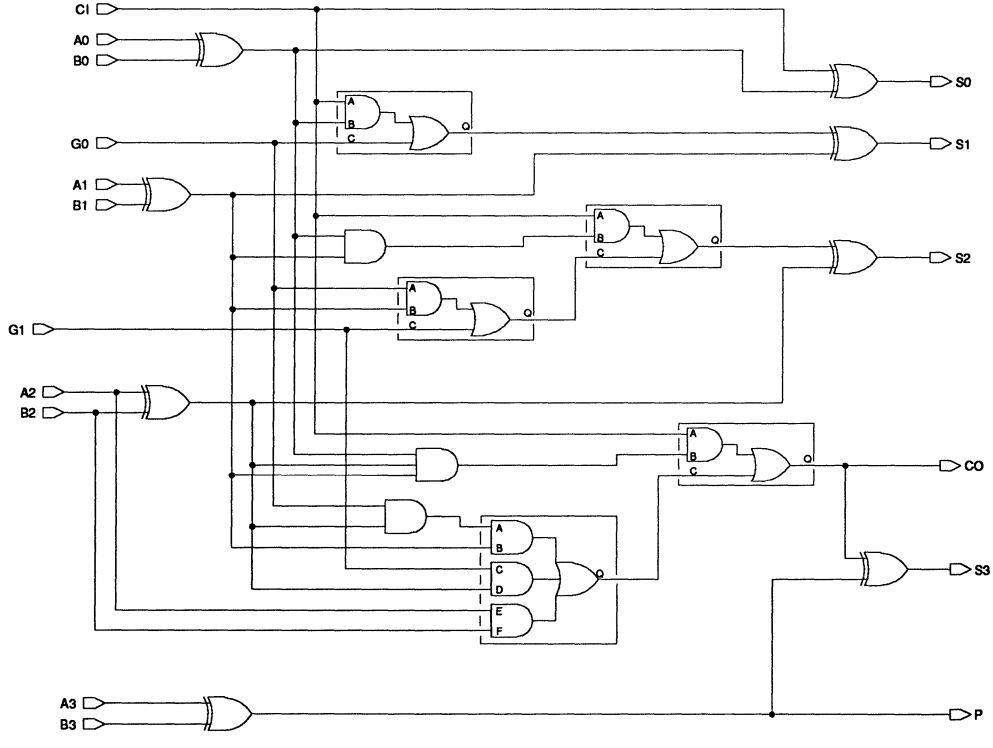
S2 = Sum of A2, B2, and G1

S3 = Sum of A3, B3, and the carry of S2

CO = Carry of the sum of A2, B2, and the carry of S2

P = EXCLUSIVE-OR of A3 and B3

Logic Schematic:



MSI Functions

April, 1992

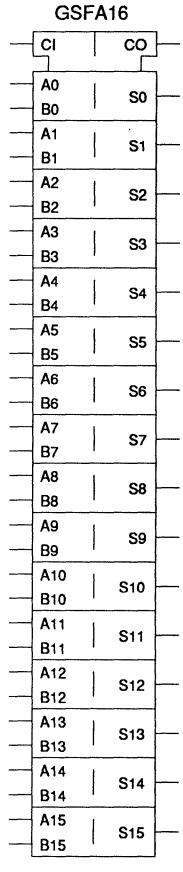
GSFA16

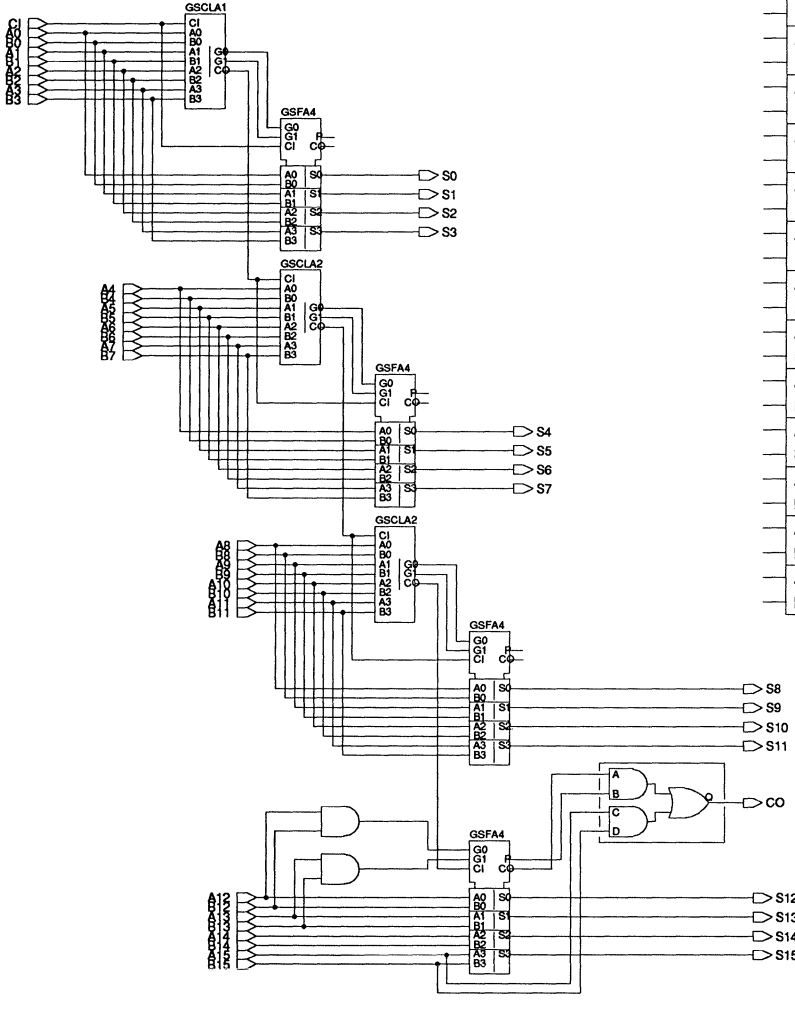
Description: GSFA16 is a 16 bit full adder.

Equivalent Gate Count: 233

Bolt Syntax: S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 CO .GSFA16 CI A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 A8 B8 A9 B9 A10 B10 A11 B11 A12 B12 A13 B13 A14 B14 A15 B15 ;

Logic Schematic:





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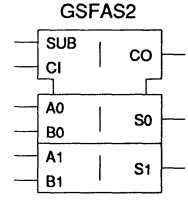
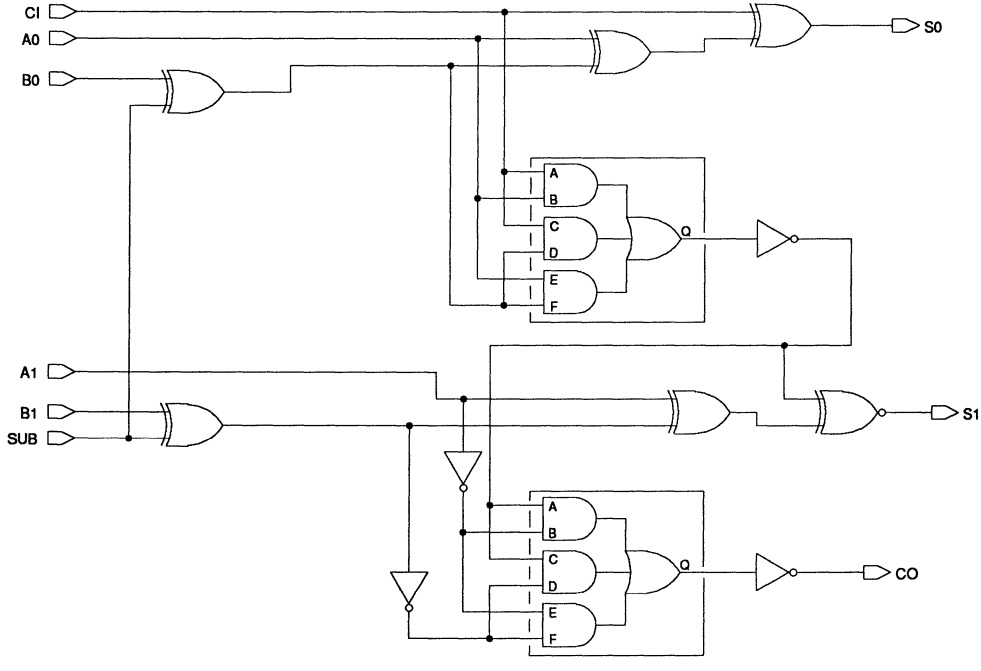
GSFAS2



Description: GSFAS2 is a 2 bit twoscomplementfulladder[A+B],withsubtractor[A-B].'
Equivalent Gate Count: 30
Bolt Syntax: S0 S1 CO .GSFAS2 CI A0 B0 A1 B1 SUB ;
Truth Equation:ADD MODE [SUB = 0]
S0 = Sum of A0, B0, and CI
S1 = Sum of A1, B1, and the carry of S0
CO = Carry of the sum of A1, B1, and the carry of S0

SUBTRACT MODE [SUB = 1]
S0 = Sum of A0, B0N, and CI
S1 = Sum of A1, B1N, and the carry of S0
CO = Carry of the sum of A1, B1N, and the carry of S0

Logic Schematic:



MSI Functions

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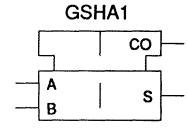
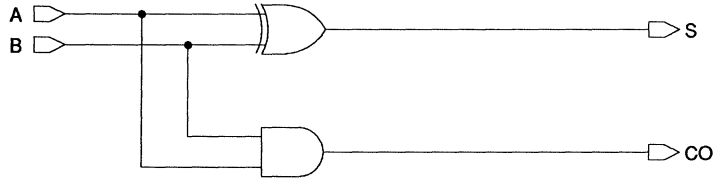
GSHA1



Description: GSHA1 is a half adder.
Equivalent Gate Count: 5
Bolt Syntax: S CO .GSHA1 A B ;
Truth Table

A	B	S	CO
L	L	L	L
H	L	H	L
L	H	H	L
H	H	L	H

Logic Schematic:



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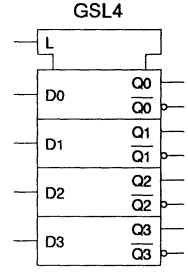
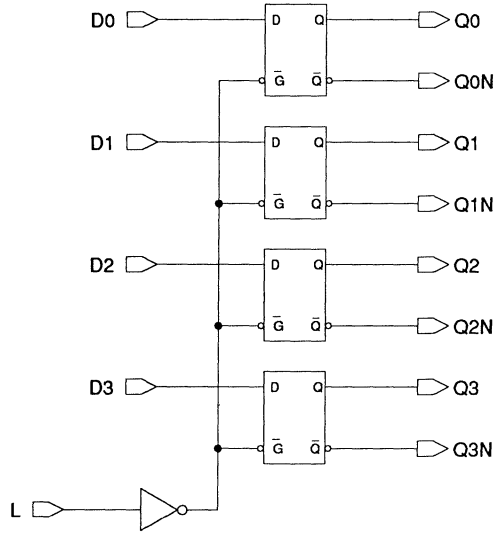
GSL4



Description: GSL4 is a 4 bit data latch.
Equivalent Gate Count: 13
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSL4 D0 D1 D2 D3 L ;

Logic Schematic:



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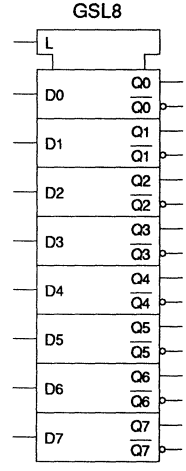
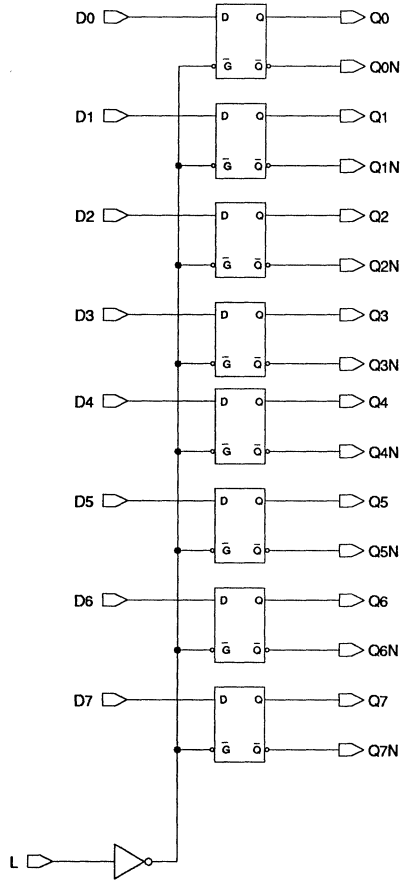
GSL8



Description: GSL8 is an 8 bit data latch.
Equivalent Gate Count: 25
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N
.GSL8 D0 D1 D2 D3 D4 D5 D6 D7 L ;

Logic Schematic:



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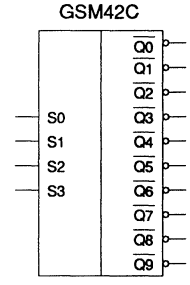
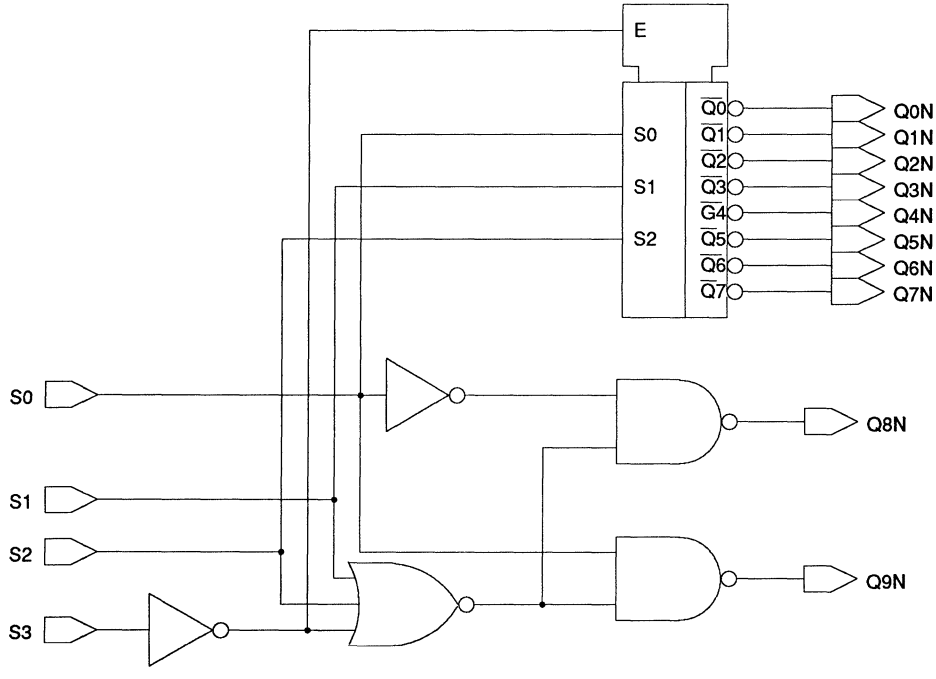
GSM42C



Description: GSM42C is a 4 to 10 decoder.
Equivalent Gate Count: 24
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N Q8N Q9N .GSM42C S0 S1 S2 S3 ;

Logic Schematic:



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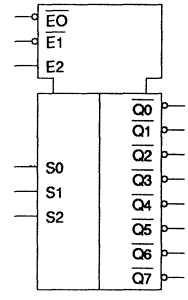
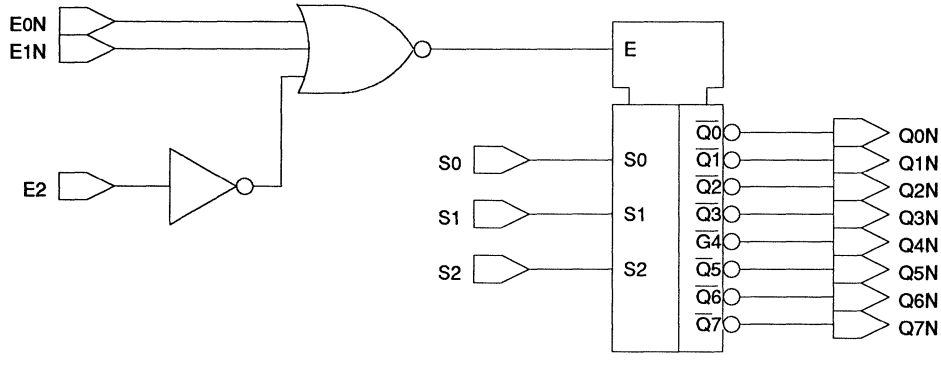
GSM138C

GSM138C



Description: GSM138C is a gated 3 to 8 line decoder.
Equivalent Gate Count: 21
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N .GSM138C E2 E0N E1N S0 S1 S2 ;

Logic Schematic:



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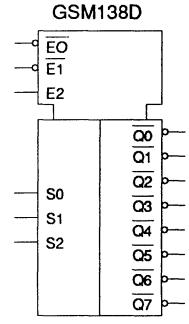
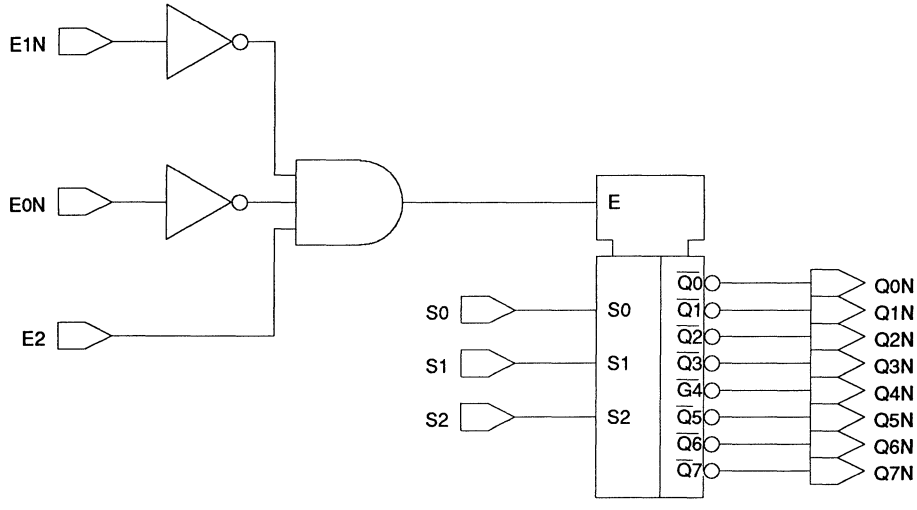
GSM138D



Description: GSM138D is a gated 3 to 8 decoder, with active low outputs.
Equivalent Gate Count: 22
Bolt Syntax: Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N .GSM138D E2 E0N E1N S0 S1 S2 ;

Logic Schematic:



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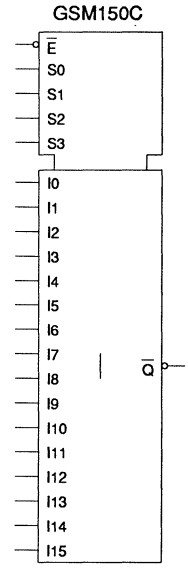
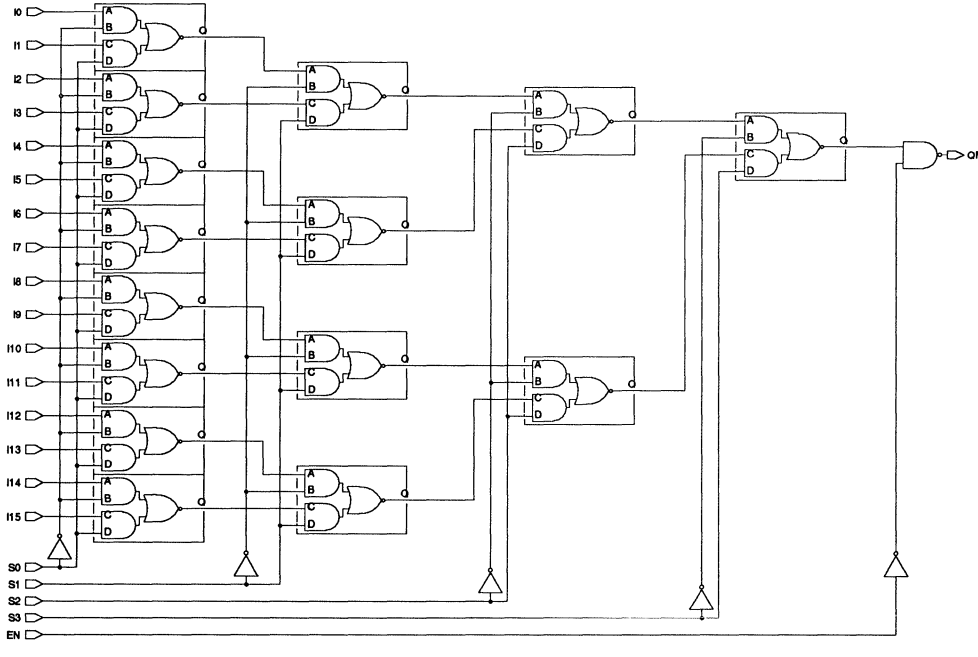
GSM150C



Description: GSM150C is a 16 input inverting gated MUX, with active low enable.
Equivalent Gate Count: 36
Bolt Syntax: QN .GSM150C I0 I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12 I13 I14 I15 S0 S1 S2 S3 EN ;

Logic Schematic:



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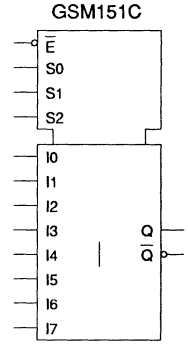
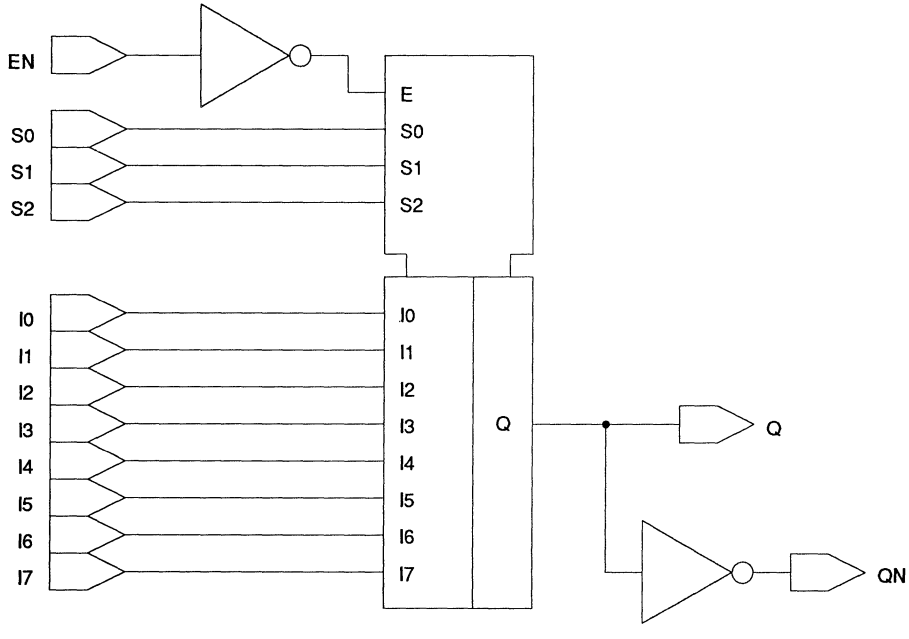
GSM151C



Description: GSM151C is an 8 input non-inverting gated MUX, with active low enable.
Equivalent Gate Count: 19
Bolt Syntax: Q QN .GSM151C I0 I1 I2 I3 I4 I5 I6 I7 S0 S1 S2 EN ;

Logic Schematic:



MSI Functions

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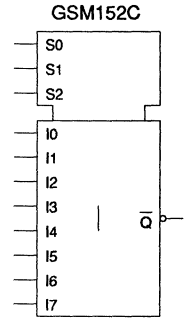
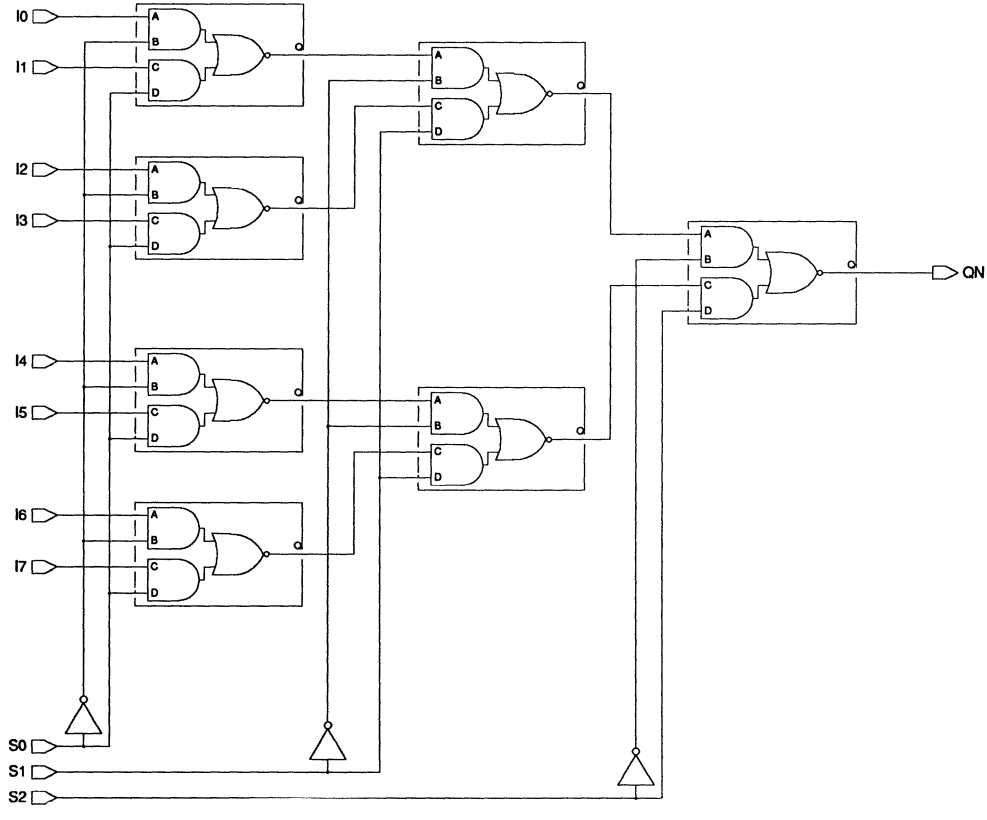
GSM152C



Description: GSM152C is an 8 input inverting MUX.
Equivalent Gate Count: 17
Bolt Syntax: QN .GSM152C I0 I1 I2 I3 I4 I5 I6 I7 S0 S1 S2 ;

Logic Schematic:



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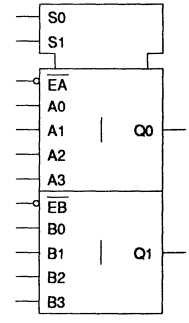
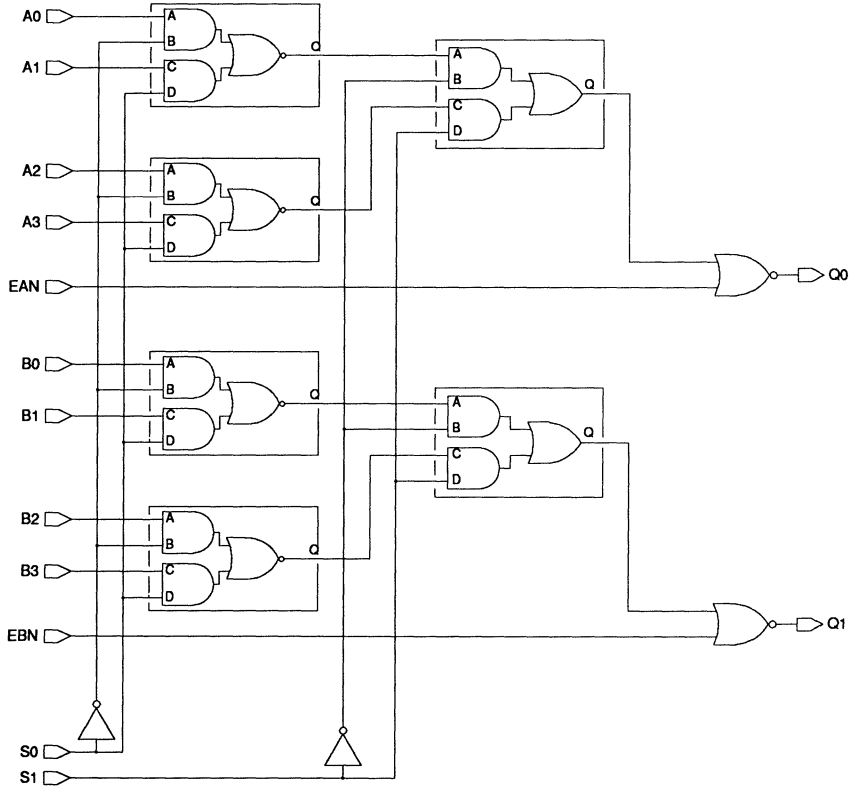
GSM153C

GSM153C



Description: GSM153C is a dual 4 input MUX, with active low enables.
Equivalent Gate Count: 18
Bolt Syntax: Q0 Q1 .GSM153C A0 A1 A2 A3 B0 B1 B2 B3 S0 S1 EAN EBN ;

Logic Schematic:



MSI Functions

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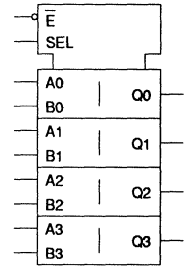
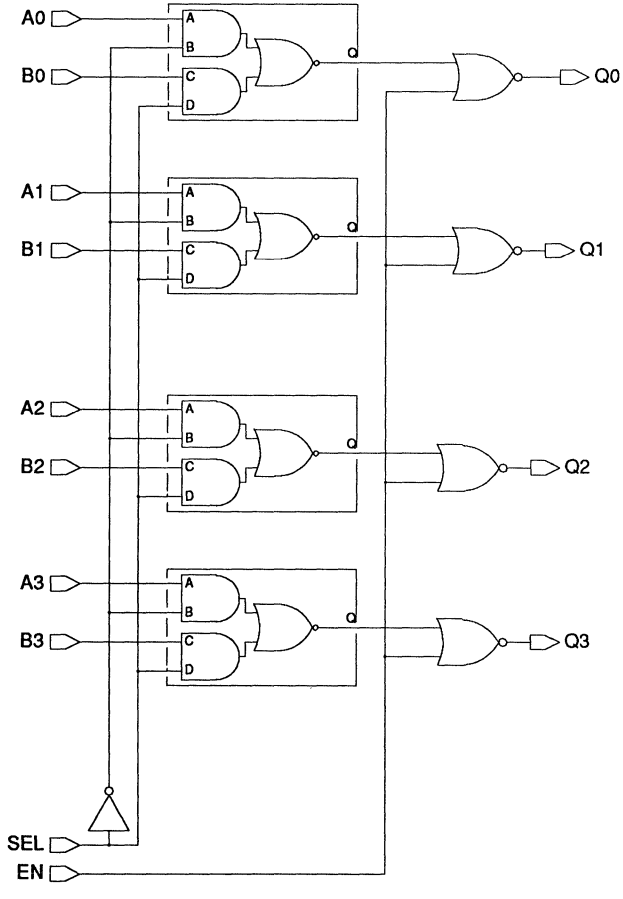
GSM157C

GSM157C



Description: GSM157C is a quad 2 input gated MUX, with active low enable.
Equivalent Gate Count: 13
Bolt Syntax: Q0 Q1 Q2 Q3 .GSM157C A0 B0 A1 B1 A2 B2 A3 B3 SEL EN ;

Logic Schematic:



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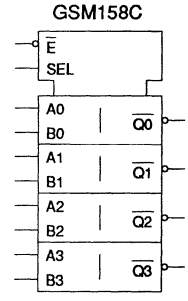
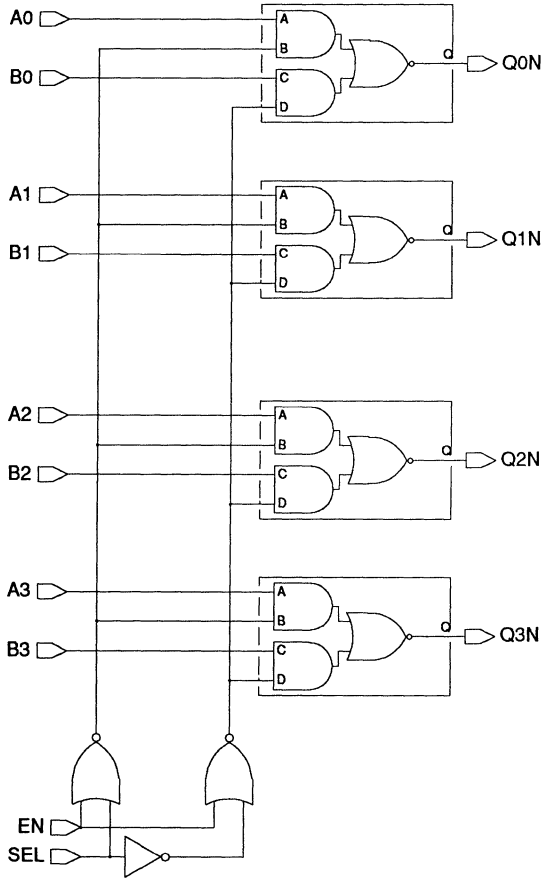
GSM158C



Description: GSM158C is a quad 2 input gated inverting MUX, with active low enable.
Equivalent Gate Count: 11
Bolt Syntax: Q0N Q1N Q2N Q3N .GSM158C A0 B0 A1 B1 A2 B2 A3 B3 SEL EN ;

Logic Schematic:



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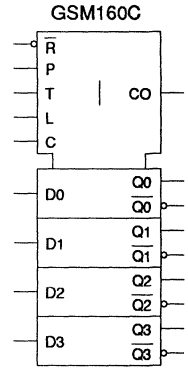
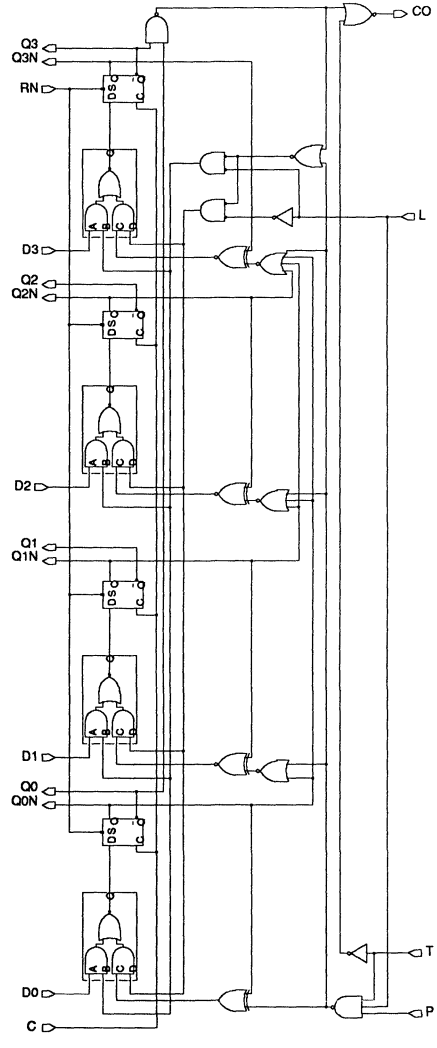
GSM160C



Description: GSM160C is a synchronous 4 bit BCD counter, with reset not [74LS160].
Equivalent Gate Count: 58
Bolt Syntax: Q0 Q1 Q2 Q3 CO Q0N Q1N Q2N Q3N .GSM160C D0 D1 D2 D3 L C RN P T ;
Logic Schematic:



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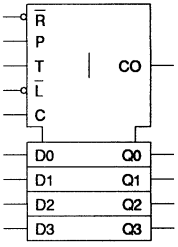
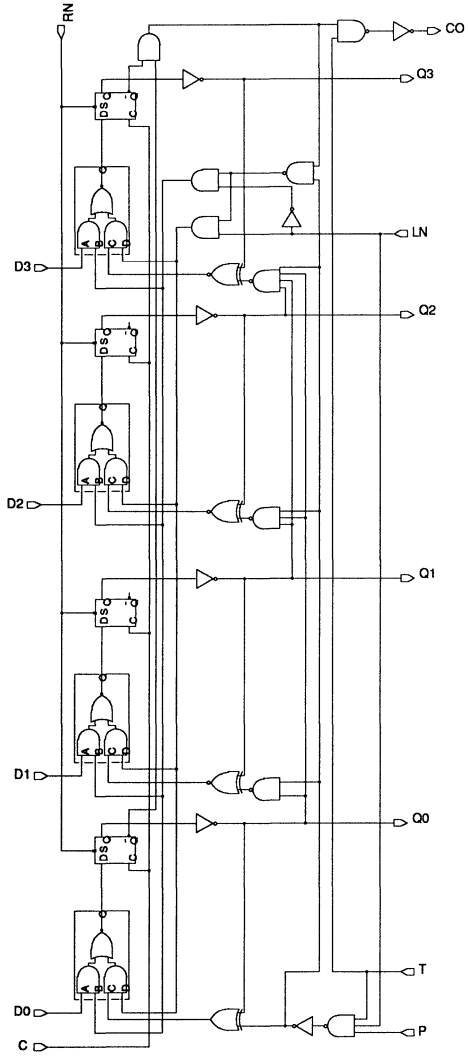
GSM160D

GSM160D



Description: GSM160D is a synchronous 4 bit BCD counter, with reset not [74LS160].
Equivalent Gate Count: 66
Bolt Syntax: Q0 Q1 Q2 Q3 CO .GSM160D D0 D1 D2 D3 LN C RN P T ;

Logic Schematic:



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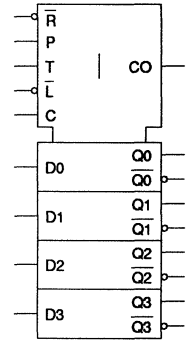
GSM161C

GSM161C

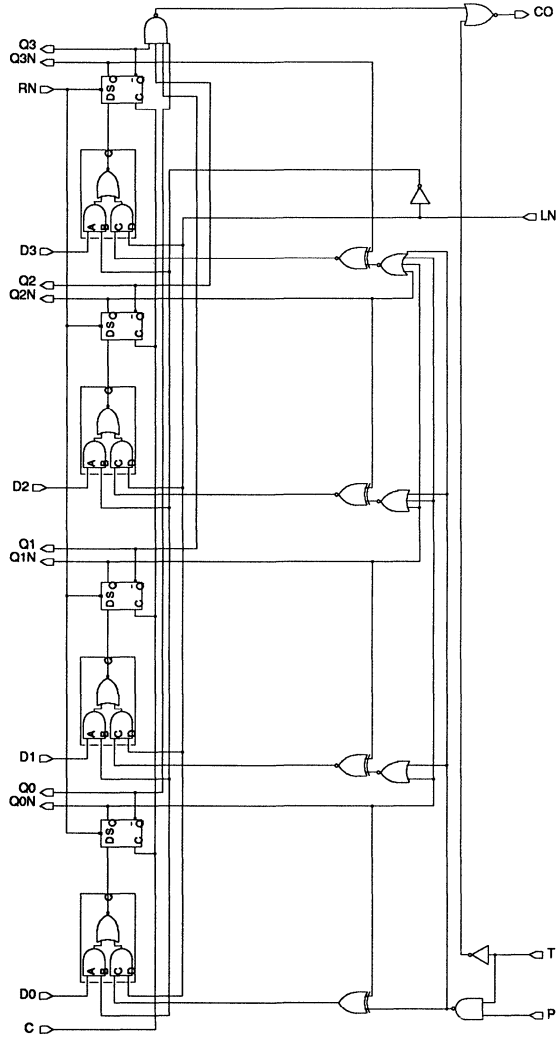


Description: GSM161C is a synchronous 4 bit binary counter, with reset not [74LS161].

Equivalent Gate Count: 55

Bolt Syntax: Q0 Q1 Q2 Q3 CO Q0N Q1N Q2N Q3N .GSM161C D0 D1 D2 D3 LN C P T RN ;

Logic Schematic:



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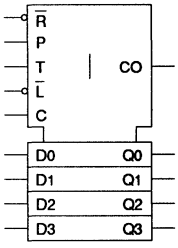
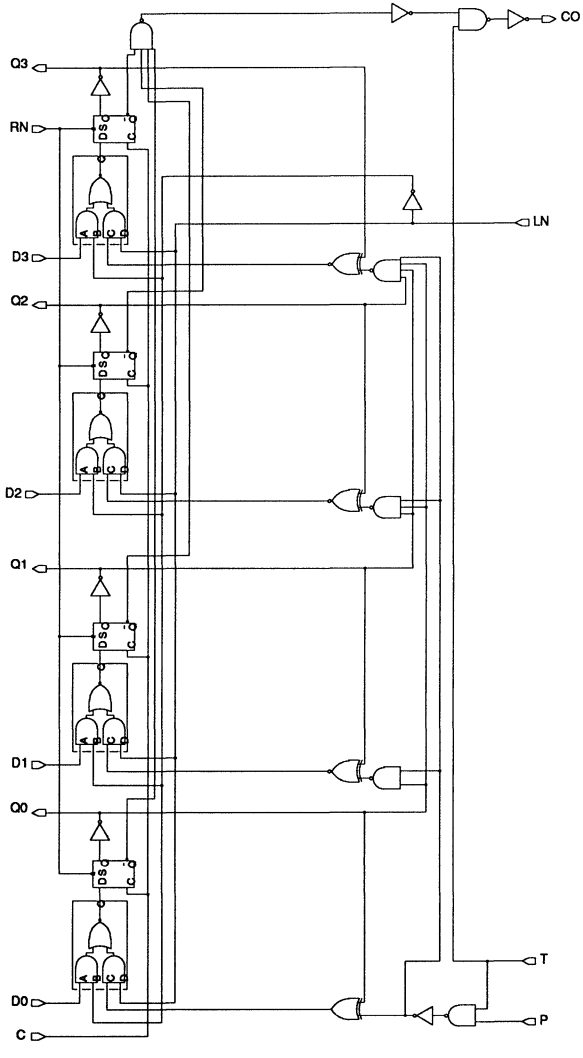
GSM161D

GSM161D



Description: GSM161D is a synchronous 4 bit binary counter, with reset not [74LS161].
Equivalent Gate Count: 61
Bolt Syntax: Q0 Q1 Q2 Q3 CO .GSM161D D0 D1 D2 D3 LN C P T RN ;

Logic Schematic:



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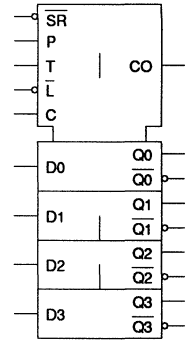
GSM162C

GSM162C

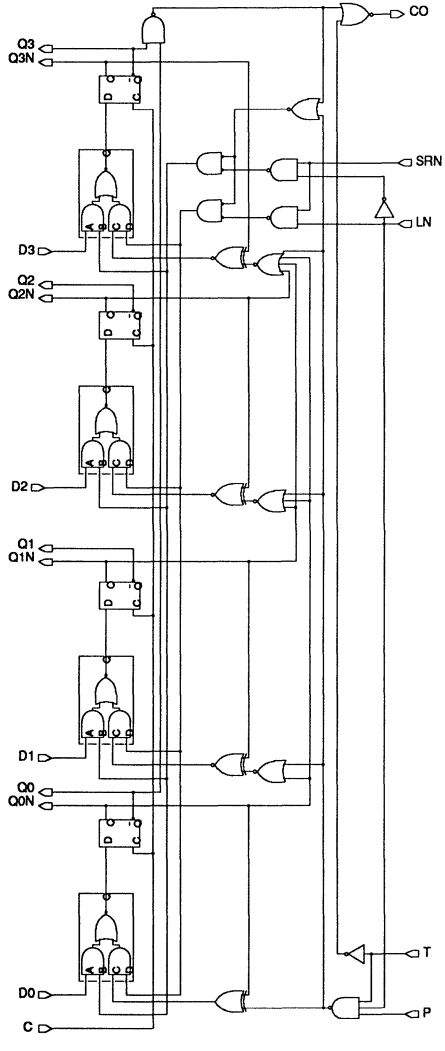


Description: GSM162C is a synchronous 4 bit BCD counter, with synchronous reset not [74LS162].

Equivalent Gate Count: 56

Bolt Syntax: Q0 Q1 Q2 Q3 CO Q0N Q1N Q2N Q3N .GSM162C D0 D1 D2 D3 LN SRN C P T ;

Logic Schematic:



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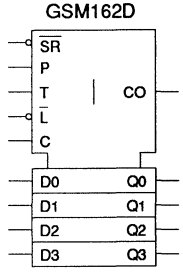
GSM162D

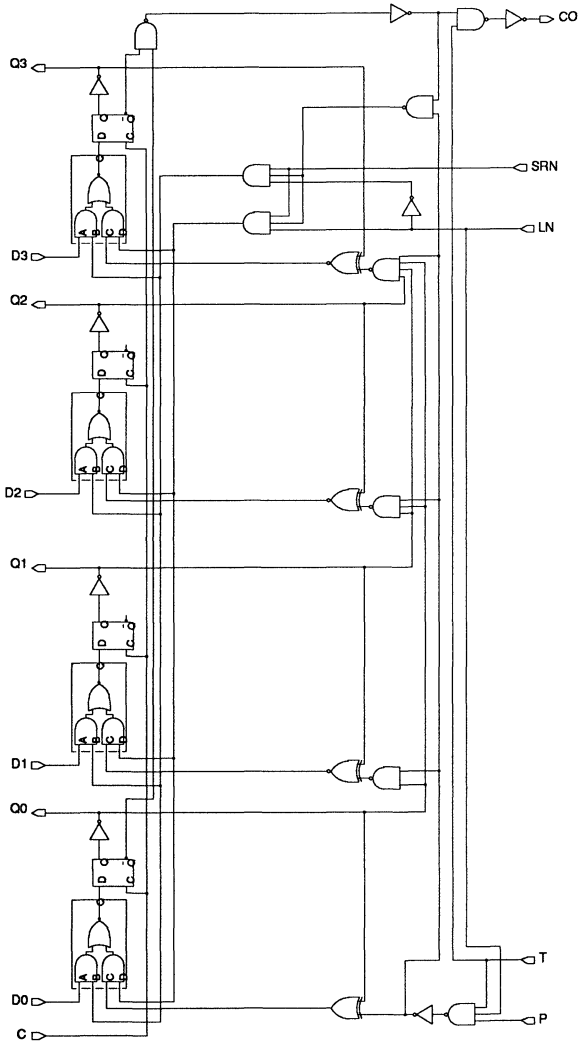


Description: GSM162D is a synchronous 4 bit BCD counter, with synchronous reset not [74LS162].

Equivalent Gate Count: 62

Bolt Syntax: Q0 Q1 Q2 Q3 CO .GSM162D D0 D1 D2 D3 LN SRN C P T ;

Logic Schematic:



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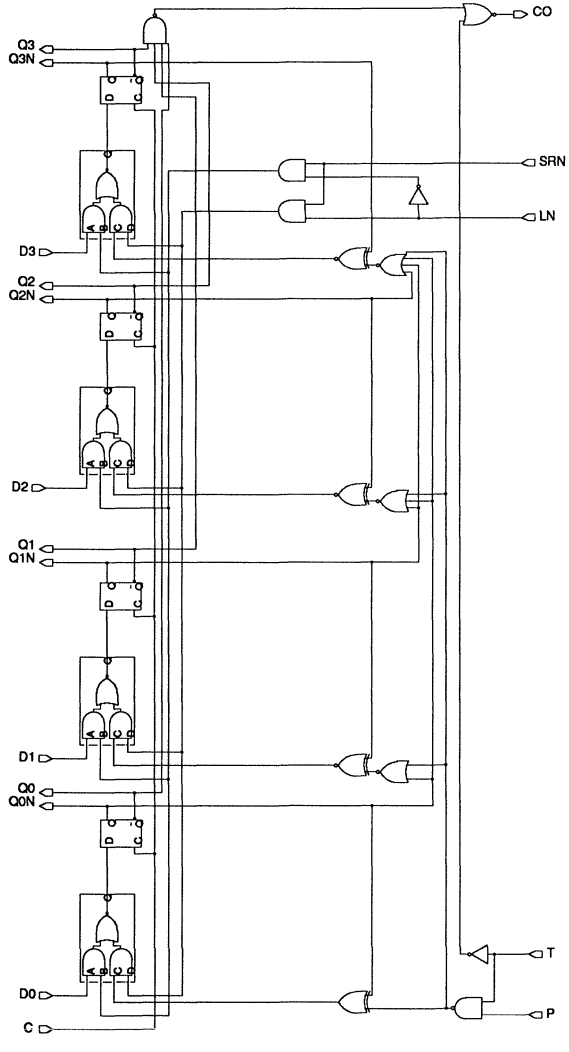
GSM163C

Description: GSM163C is a synchronous 4 bit binary counter, with synchronous reset not [74LS163].

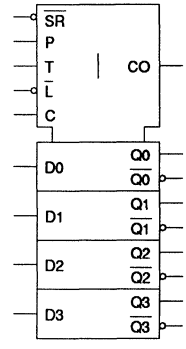
Equivalent Gate Count: 55

Bolt Syntax: Q0 Q1 Q2 Q3 CO Q0N Q1N Q2N Q3N .GSM163C D0 D1 D2 D3 LN SRN C P T ;

Logic Schematic:



GSM163C



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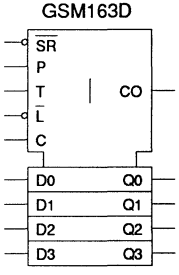
GSM163D

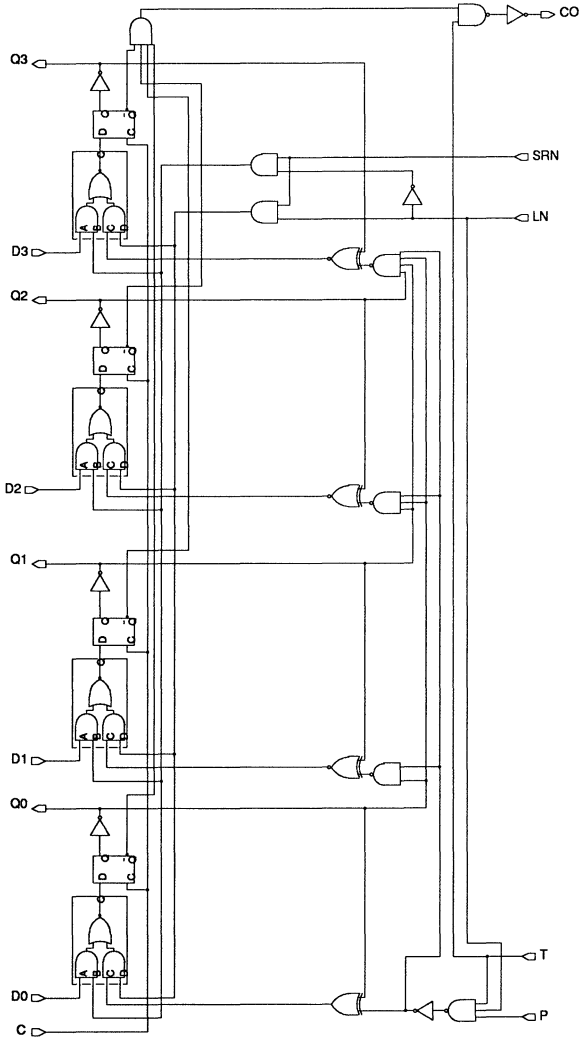


Description: GSM163D is a synchronous 4 bit binary counter, with synchronous reset not [74LS163].

Equivalent Gate Count: 62

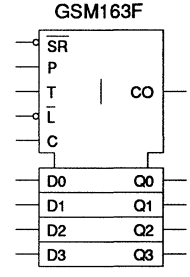
Bolt Syntax: Q0 Q1 Q2 Q3 CO .GSM163D D0 D1 D2 D3 LN SRN C P T ;

Logic Schematic:



April, 1992

GSM163F

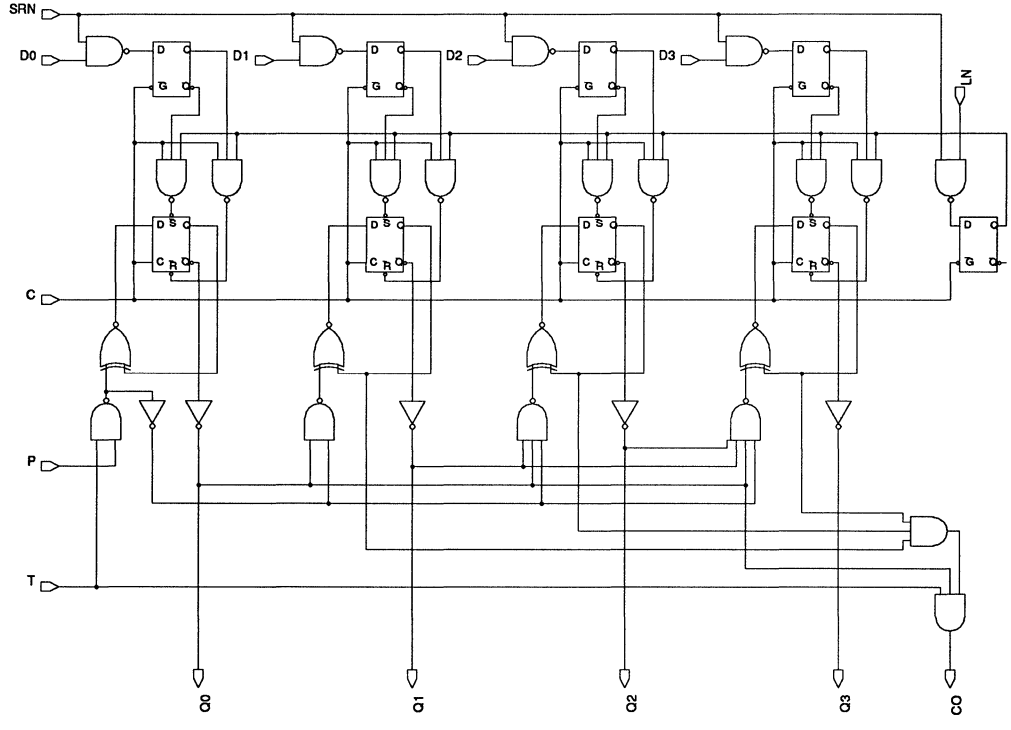


Description: GSM163F is a synchronous 4 bit binary counter, with synchronous reset not [74LS163].

Equivalent Gate Count: 91

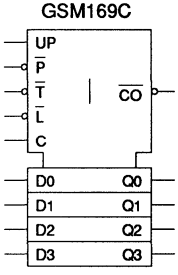
Bolt Syntax: Q0 Q1 Q2 Q3 CO .GSM163F D0 D1 D2 D3 LN SRN C P T ;

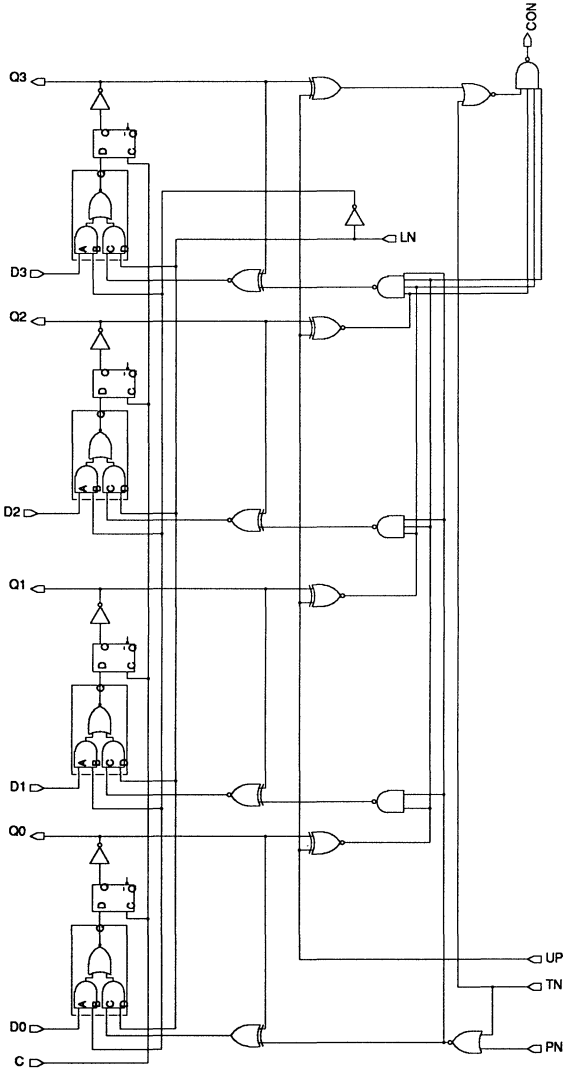
Logic Schematic:



Description: GSM169C is a 4 bit binary up/down counter [74LS169].
Equivalent Gate Count: 66
Bolt Syntax: Q0 Q1 Q2 Q3 CON .GSM169C D0 D1 D2 D3 LN C PN TN UP ;

Logic Schematic:





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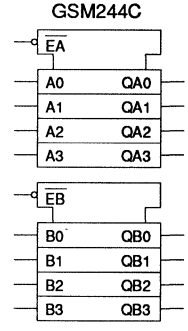
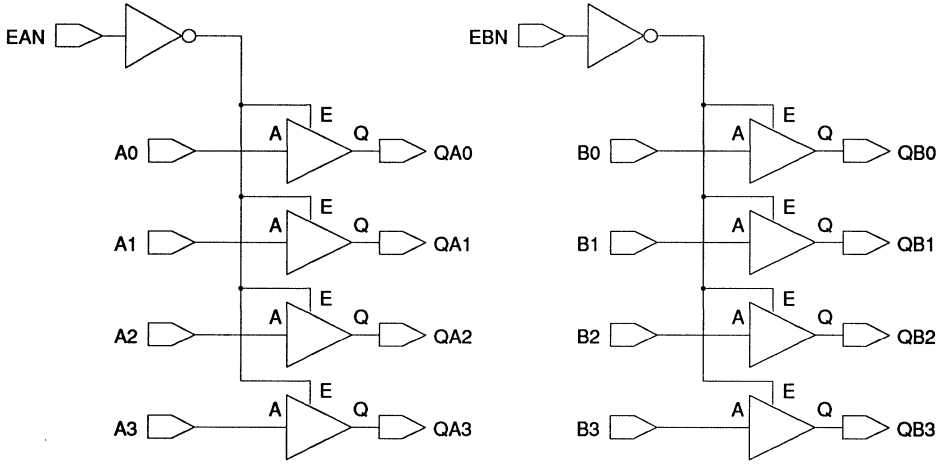
GSM244C



Description: GSM244C is a dual 4 bit internal tri-state buffer, with active low enables.
Equivalent Gate Count: 26
Bolt Syntax: QA0 QA1 QA2 QA3 QB0 QB1 QB2 QB3 .GSM244C A0 A1 A2 A3 B0 B1 B2 B3 EAN EBN ;

Logic Schematic:



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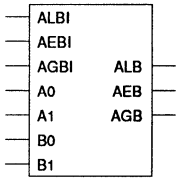
GSMAG2

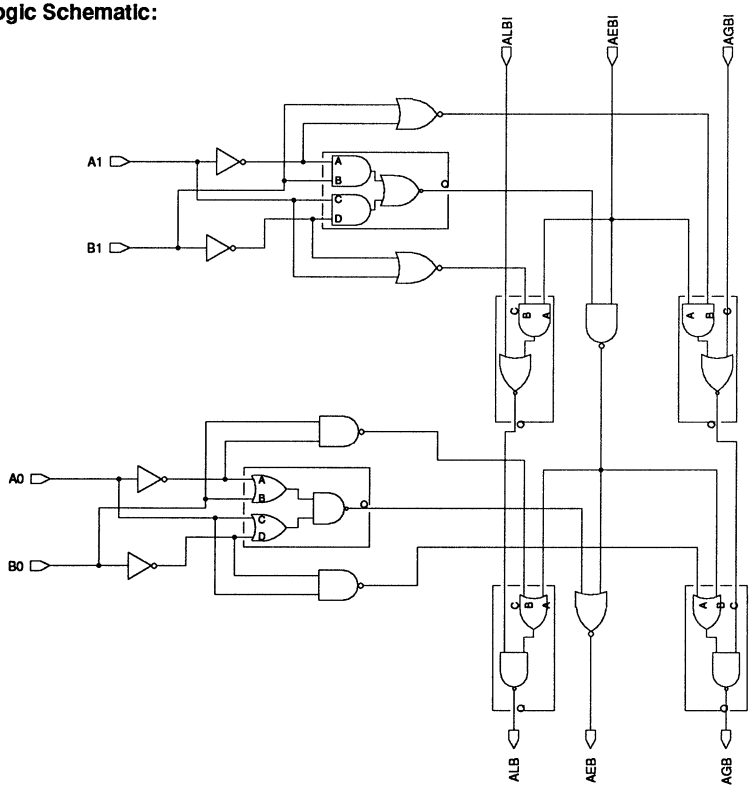
GSMAG2



Description: GSMAG2 is a 2 bit extendable binary magnitude comparator.
Equivalent Gate Count: 22
Bolt Syntax: AGB AEB ALB .GSMAG2 AGBI AEBI ALBI A1 B1 A0 B0 ;
Truth Table

AGBI	ALBI	AEBI	A1-B1	A0-B0	AGB	ALB	AEB
H	L	L	X	X	H	L	L
L	H	L	X	X	L	H	L
L	L	H	A1>B1	X	H	L	L
L	L	H	A1<B1	X	L	H	L
L	L	H	A1=B1	A0>B0	H	L	L
L	L	H	A1=B1	A0<B0	L	H	L
L	L	H	A1=B1	A0=B0	L	L	H

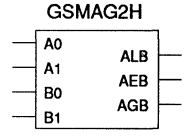
Logic Schematic:



MSI Functions

April, 1992

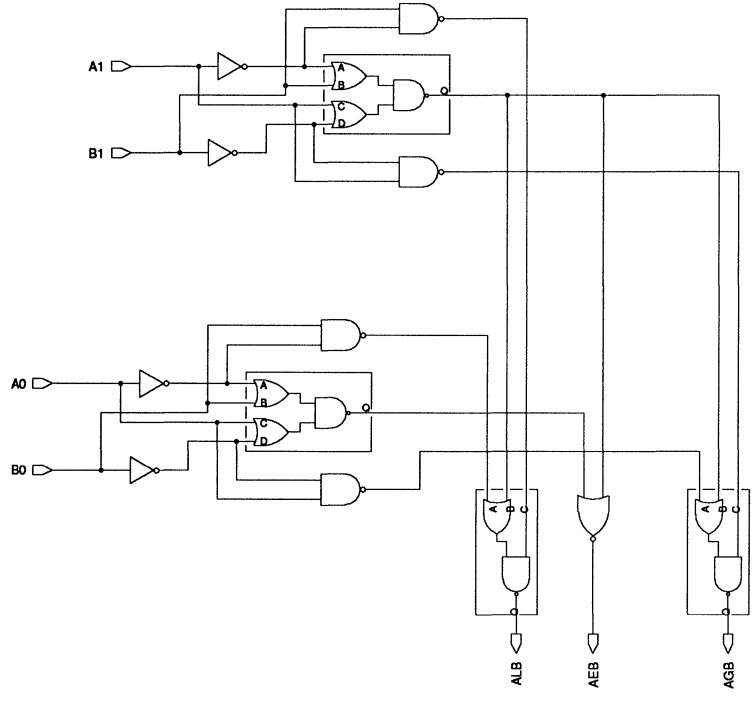
GSMAG2H



Description: GSMAG2H is a 2 bit binary magnitude comparator.
Equivalent Gate Count: 17
Bolt Syntax: AGB AEB ALB .GSMAG2H A1 B1 A0 B0 ;
Truth Table

A1-B1	A0-B0	AGB	ALB	AEB
A1>B1	X	H	L	L
A1<B1	X	L	H	L
A1=B1	A0>B0	H	L	L
A1=B1	A0<B0	L	H	L
A1=B1	A0=B0	L	L	H

Logic Schematic:



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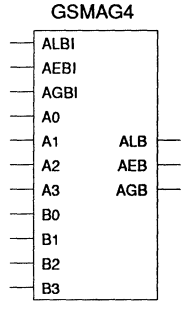
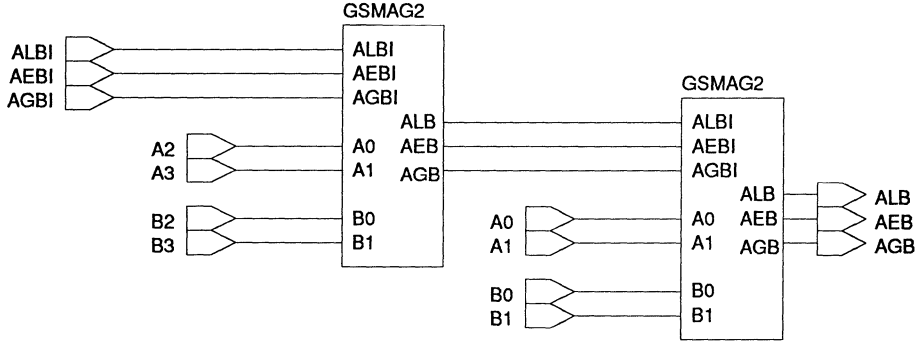
GSMAG4



Description: GSMAG4 is a 4 bit expandable binary magnitude comparator.
Equivalent Gate Count: 44
Bolt Syntax: AGB AEB ALB .GSMAG4 AGBI AEBI ALBI A3 B3 A2 B2 A1 B1 A0 B0 ;
Truth Table

AGBI	ALBI	AEBI	A3-B3	A2-B2	A1-B1	A0-B0	AGB	ALB	AEB
H	L	L	X	X	X	X	H	L	L
L	H	L	X	X	X	X	L	H	L
L	L	H	A3>B3	X	X	X	H	L	L
L	L	H	A3<B3	X	X	X	L	H	L
L	L	H	A3=B3	A2>B2	X	X	H	L	L
L	L	H	A3=B3	A2<B2	X	X	L	H	L
L	L	H	A3=B3	A2=B2	A1>B1	X	H	L	L
L	L	H	A3=B3	A2=B2	A1<B1	X	L	H	L
L	L	H	A3=B3	A2=B2	A1=B1	A0>B0	H	L	L
L	L	H	A3=B3	A2=B2	A1=B1	A0<B0	L	H	L
L	L	H	A3=B3	A2=B2	A1=B1	A0=B0	L	L	H

Logic Schematic:



MSI Functions

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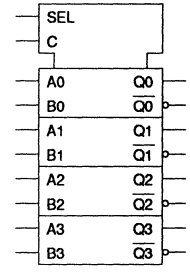
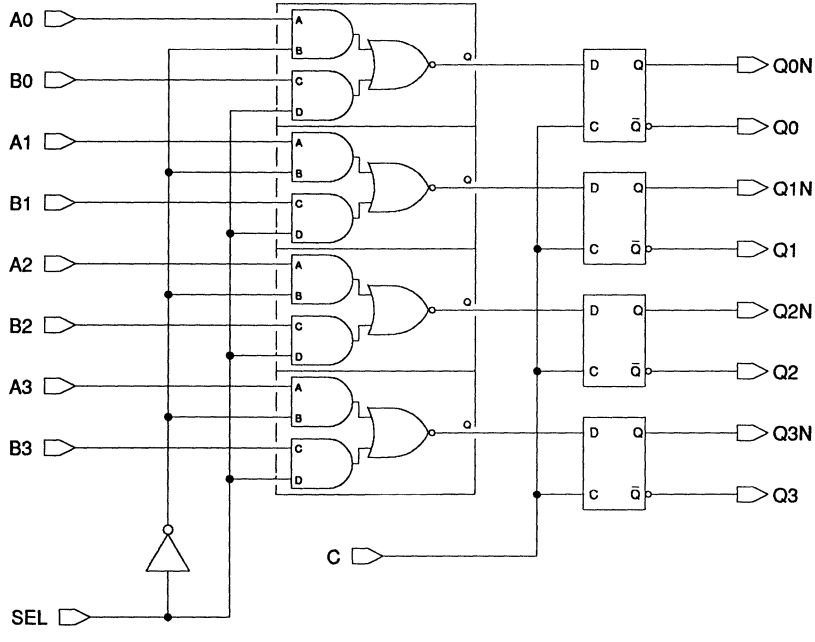
GSMR41

GSMR41



Description: GSMR41 is a 4 bit register with 2 bit multiplexed inputs.
Equivalent Gate Count: 29
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSMR41 A0 B0 A1 B1 A2 B2 A3 B3
SEL C ;

Logic Schematic:



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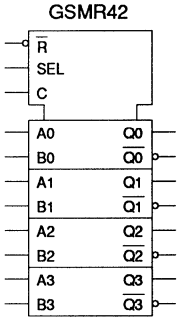
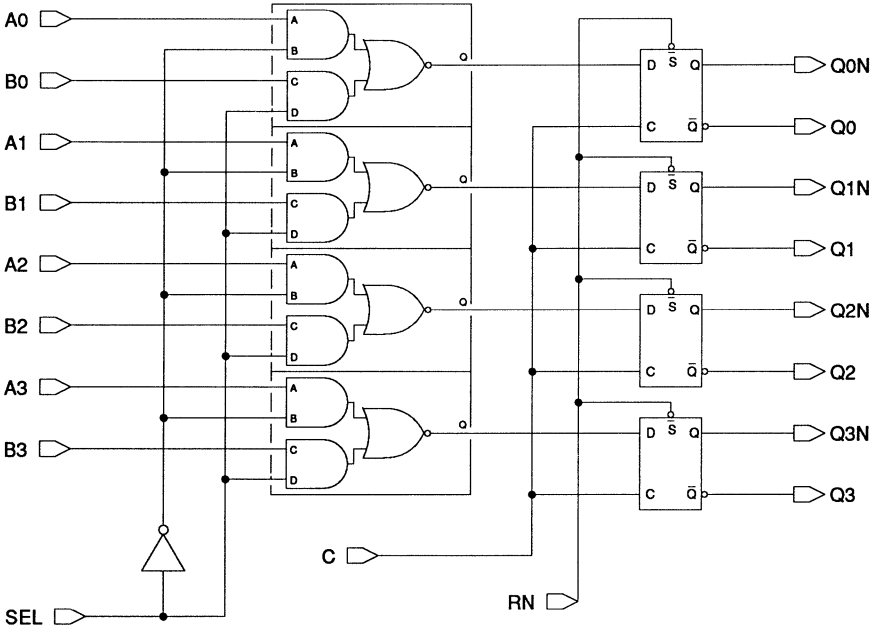
GSMR42



Description: GSMR42 is a 4 bit register with 2 bit multiplexed inputs, with reset not.
Equivalent Gate Count: 33
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSMR42 A0 B0 A1 B1 A2 B2 A3 B3
SEL C RN ;

Logic Schematic:



MSI Functions

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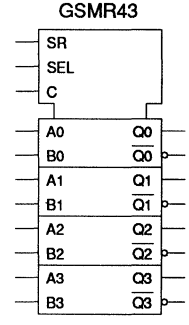
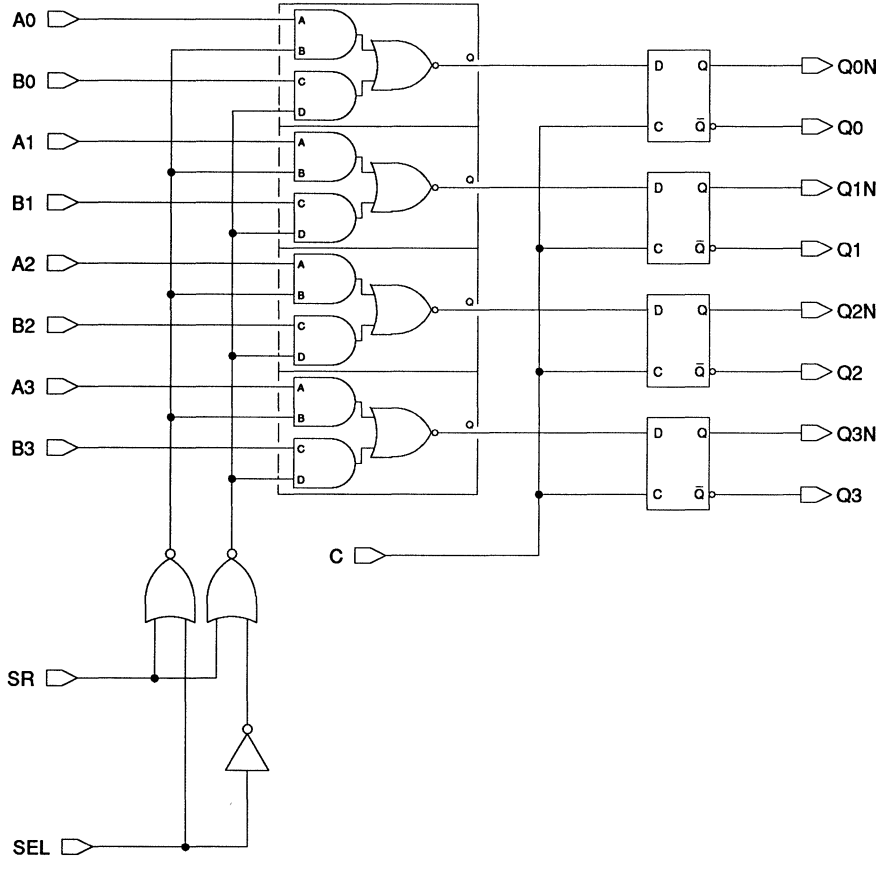
GSMR43



Description: GSMR43 is a 4 bit register with 2 bit multiplexed inputs, with synchronous reset.
Equivalent Gate Count: 31
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSMR43 A0 B0 A1 B1 A2 B2 A3 B3
SEL SR C ;

Logic Schematic:



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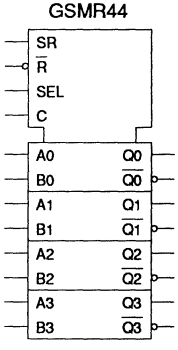
GSMR44

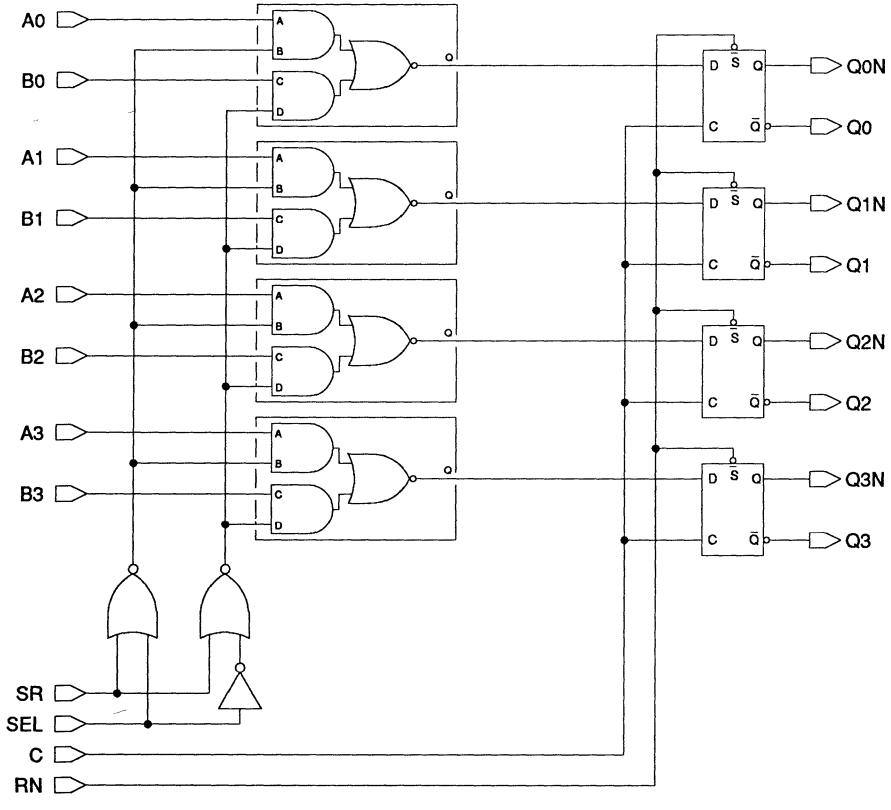


Description: GSMR44 is a 4 bit register with 2 bit multiplexed input, with synchronous reset and asynchronous reset not.

Equivalent Gate Count: 35

Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSMR44 A0 B0 A1 B1 A2 B2 A3 B3 SEL SR C RN ;

Logic Schematic:



MSI Functions

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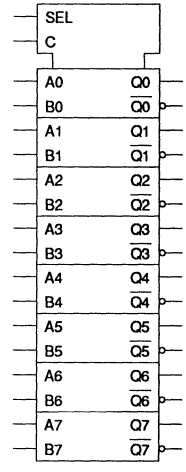
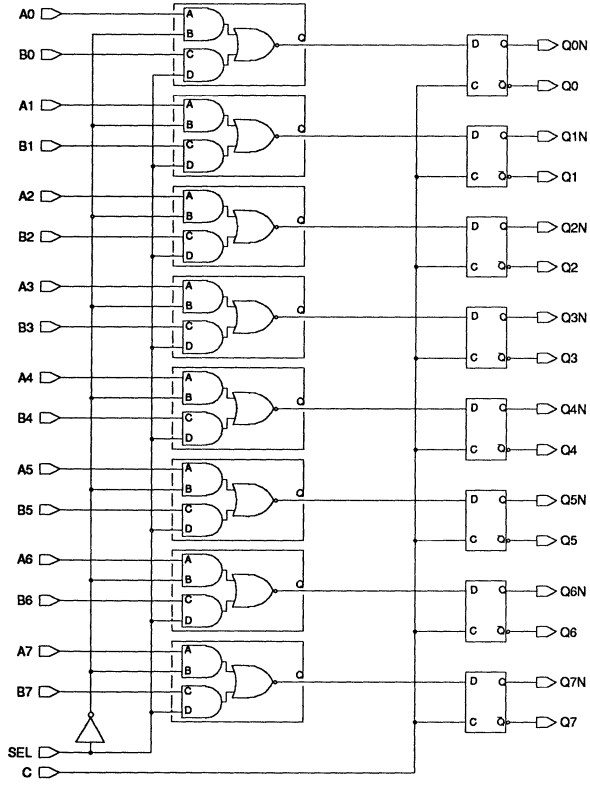
GSMR81

GSMR81



Description: GSMR81 is an 8 bit register with 2 bit multiplexed inputs.
Equivalent Gate Count: 57
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N
.GSMR81 A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 SEL C ;

Logic Schematic:



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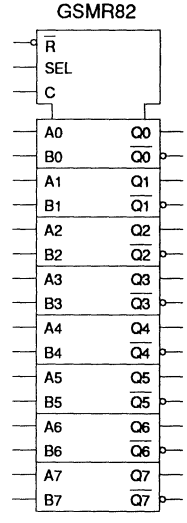
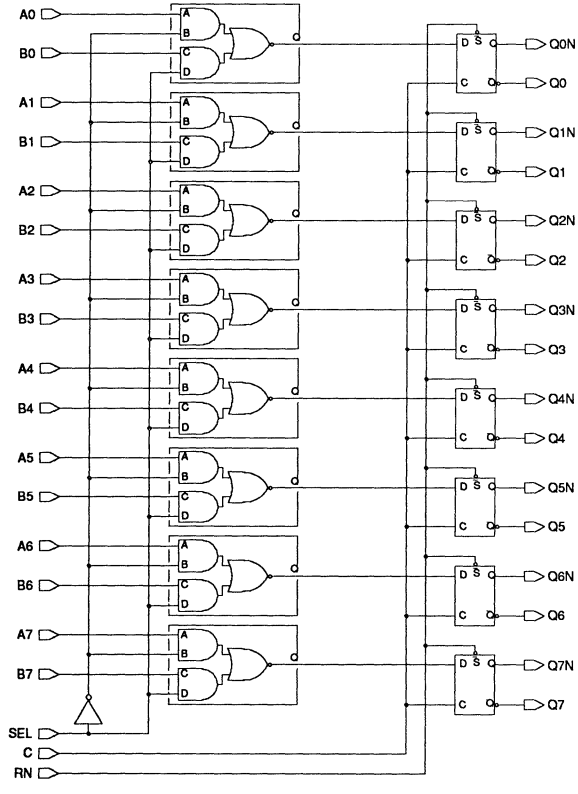
GSMR82



Description: GSMR82 is a 8 bit register with 2 bit multiplexed inputs, with reset not.
Equivalent Gate Count: 65
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N
.GSMR82 A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 SEL C RN ;

Logic Schematic:



MSI Functions

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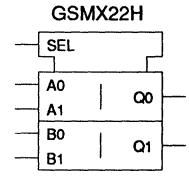
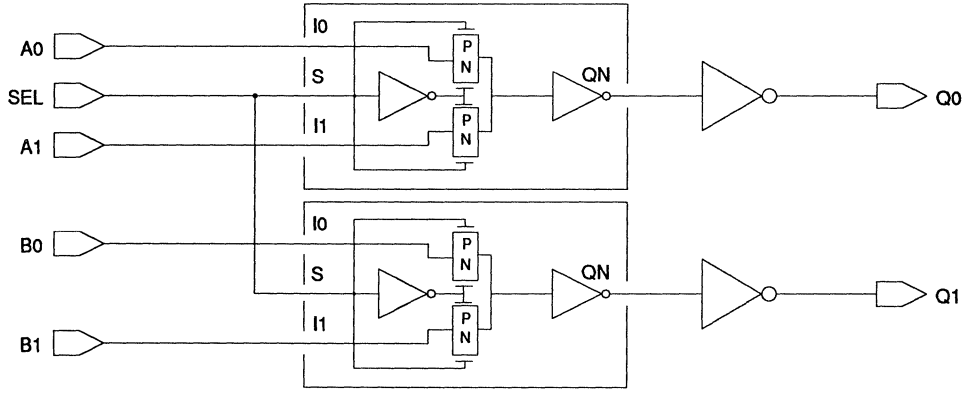
GSMX22H



Description: GSMX22H is a dual 2 bit non-inverting MUX.
Equivalent Gate Count: 6
Bolt Syntax: Q0 Q1 .GSMX22H A0 A1 B0 B1 SEL ;
Truth Table

SEL	Q0	Q1
L	A0	B0
H	A1	B1

Logic Schematic:



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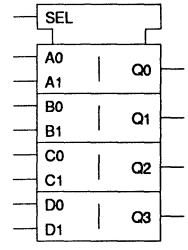
GSMX24H

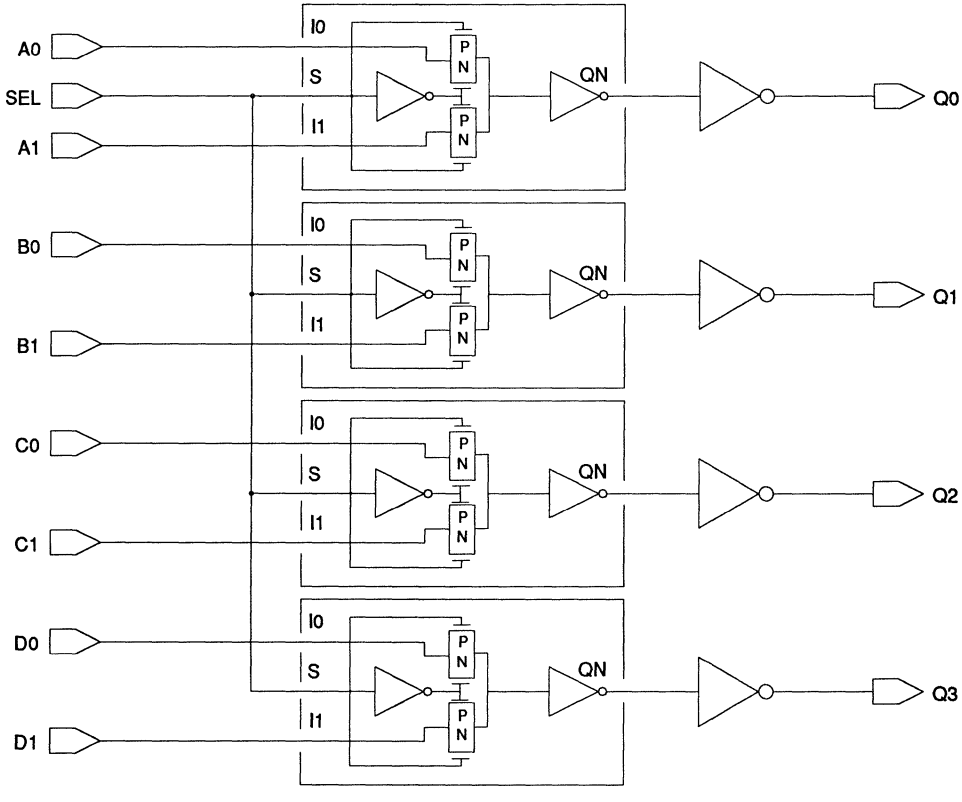
GSMX24H



Description: GSMX24H is a quad 2 bit non-inverting MUX.
Equivalent Gate Count: 12
Bolt Syntax: Q0 Q1 Q2 Q3 .GSMX24H A0 A1 B0 B1 C0 C1 D0 D1 SEL ;
Truth Table

SEL	Q0	Q1	Q2	Q3
L	A0	B0	C0	D0
H	A1	B1	C1	D1

Logic Schematic:



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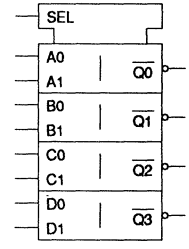
GSMX24L

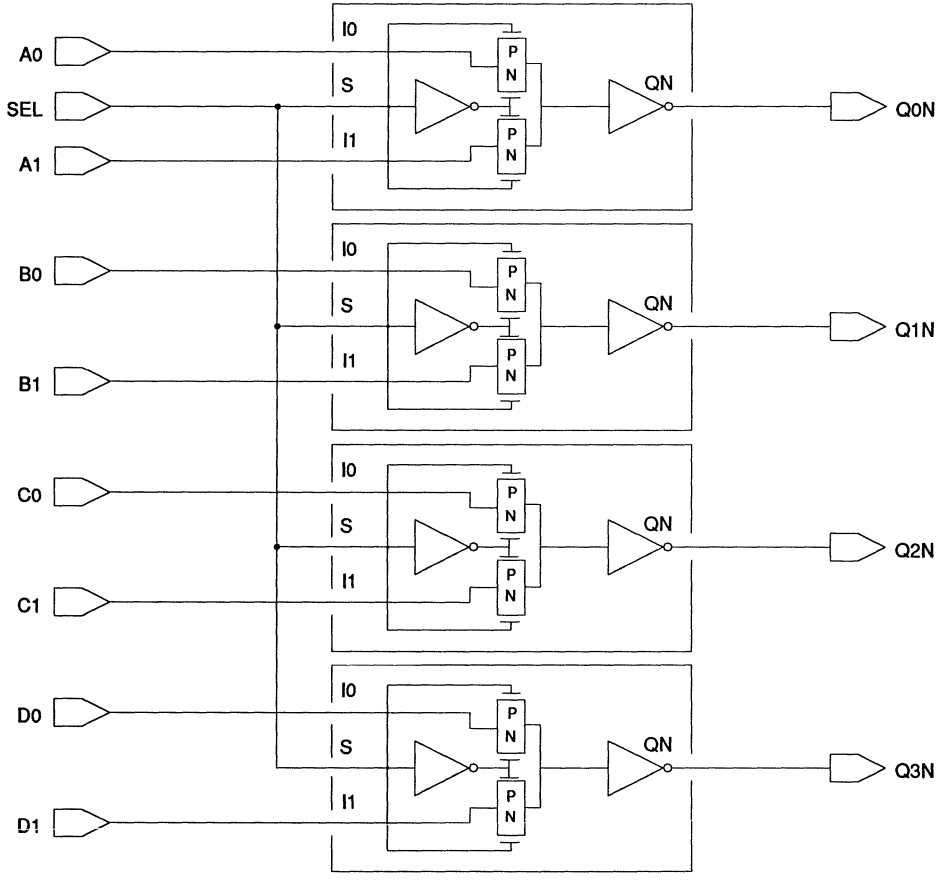
GSMX24L



Description: GSMX24L is a quad 2 bit inverting MUX.
Equivalent Gate Count: 8
Bolt Syntax: Q0N Q1N Q2N Q3N .GSMX24L A0 A1 B0 B1 C0 C1 D0 D1 SEL ;
Truth Table

SEL	Q0N	Q1N	Q2N	Q3N
L	A0N	B0N	C0N	D0N
H	A1N	B1N	C1N	D1N

Logic Schematic:



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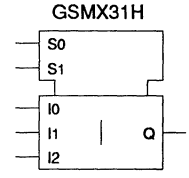
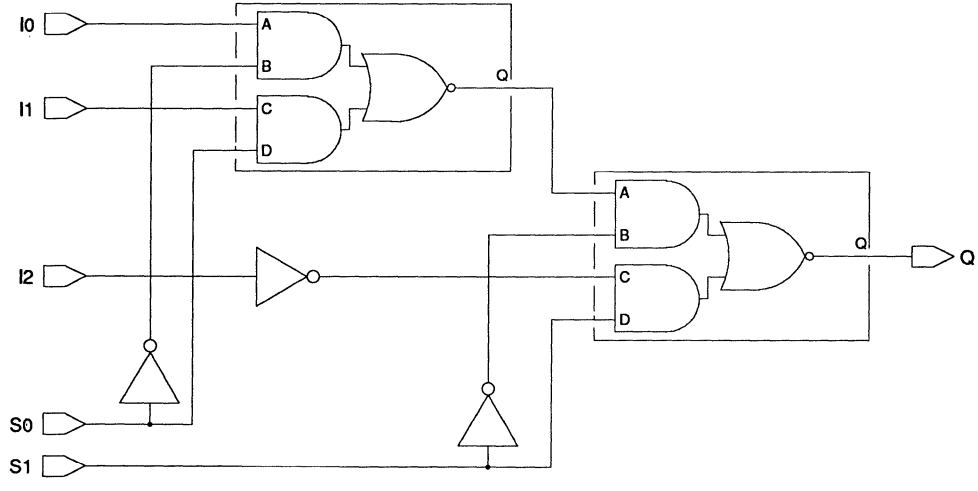
GSMX31H



Description: GSMX31H is a 3 bit non-inverting MUX.
Equivalent Gate Count: 7
Bolt Syntax: Q .GSMX31H I0 I1 I2 S0 S1 ;
Truth Table

S0	S1	Q
L	L	I0
H	L	I1
L	H	I2
H	H	I2

Logic Schematic:



MSI Functions

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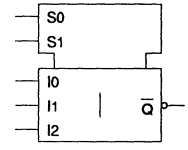
GSMX31L

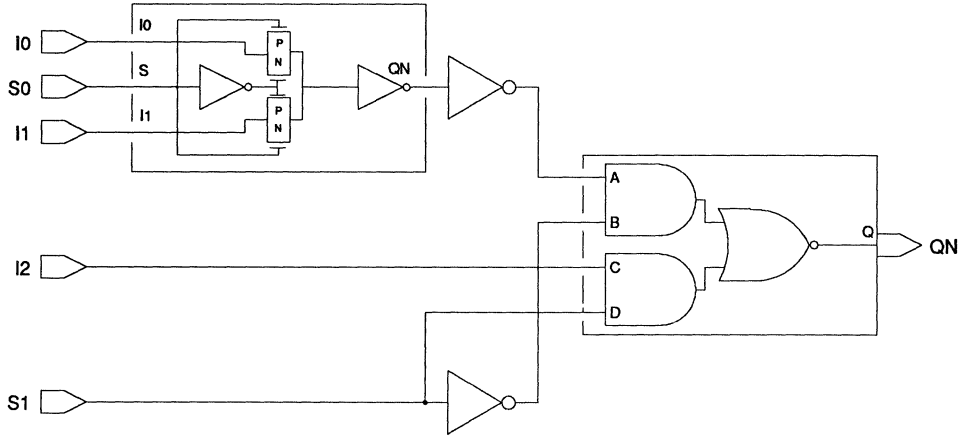
GSMX31L



Description: GSMX31L is a 3 bit inverting MUX.
Equivalent Gate Count: 6
Bolt Syntax: QN .GSMX31L I0 I1 I2 S0 S1 ;
Truth Table

S0	S1	QN
L	L	I0N
H	L	I1N
L	H	I2N
H	H	I2N

Logic Schematic:



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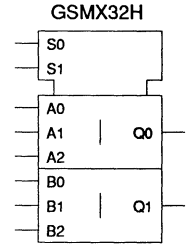
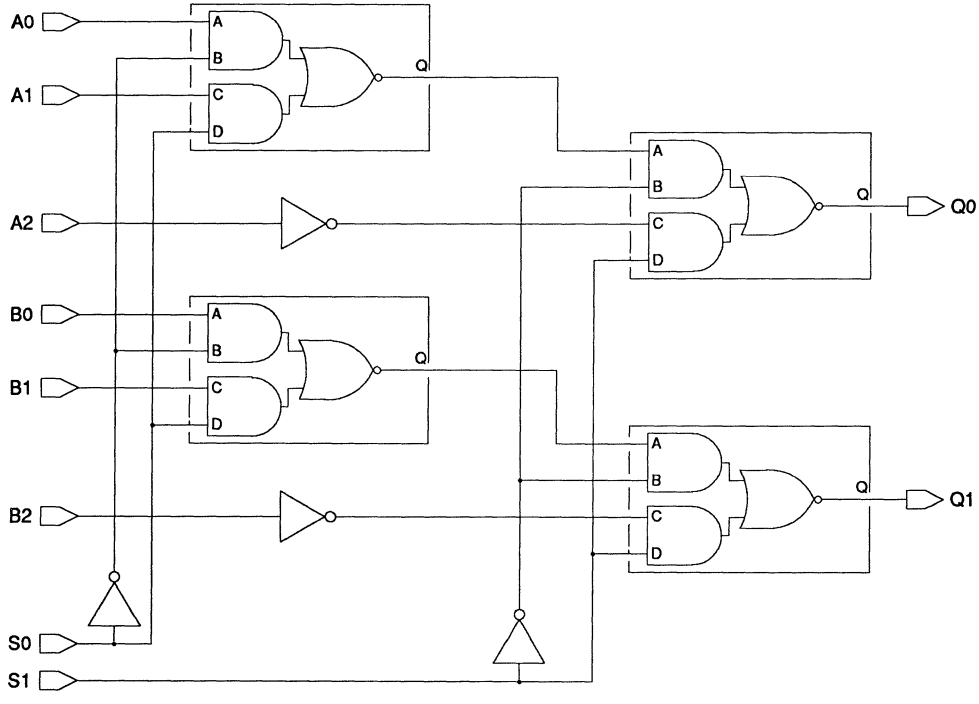
GSMX32H



Description: GSMX32H is a dual 3 bit non-inverting MUX.
Equivalent Gate Count: 12
Bolt Syntax: Q0 Q1 .GSMX32H A0 A1 A2 B0 B1 B2 S0 S1 ;
Truth Table

S0	S1	Q0	Q1
L	L	A0	B0
H	L	A1	B1
L	H	A2	B2
H	H	A2	B2

Logic Schematic:



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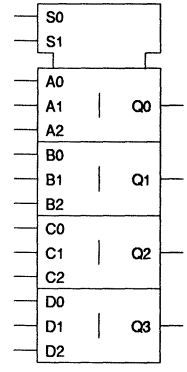
GSMX34H

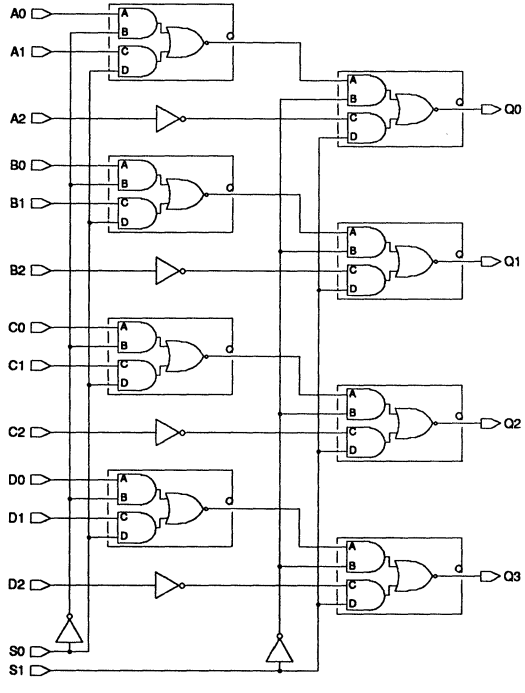
GSMX34H



Description: GSMX34H is a quad 3 bit non-inverting MUX.
Equivalent Gate Count: 22
Bolt Syntax: Q0 Q1 Q2 Q3 .GSMX34H A0 A1 A2 B0 B1 B2 C0 C1 C2 D0 D1 D2 S0 S1 ;
Truth Table

S0	S1	Q0	Q1	Q2	Q3
L	L	A0	B0	C0	D0
H	L	A1	B1	C1	D1
L	H	A2	B2	C2	D2
H	H	A2	B2	C2	D2

Logic Schematic:



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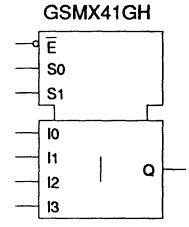
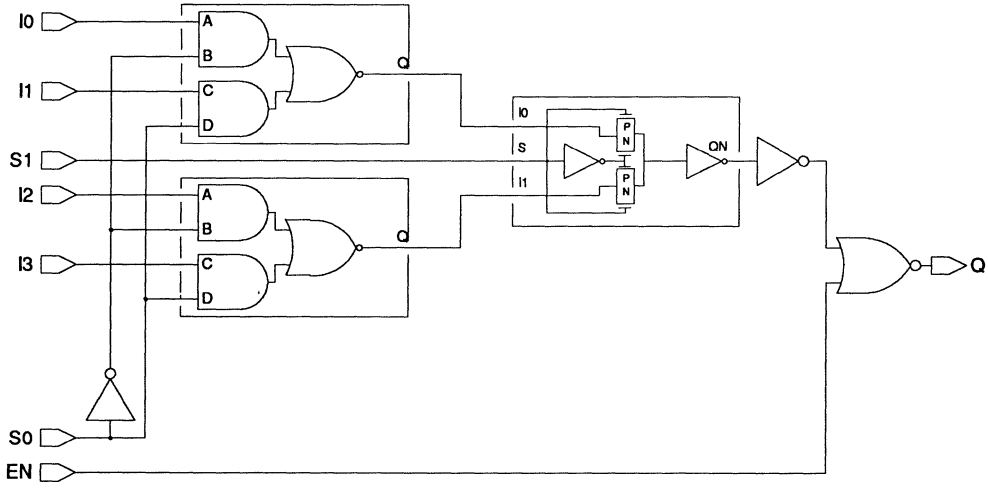
GSMX41GH



Description: GSMX41GH is a 4 bit non-inverting gated MUX, with active low enable.
Equivalent Gate Count: 9
Bolt Syntax: Q .GSMX41GH I0 I1 I2 I3 S0 S1 EN ;
Truth Table

EN	S0	S1	Q
L	L	L	I0
L	H	L	I1
L	L	H	I2
L	H	H	I3
H	X	X	L

Logic Schematic:



MSI Functions

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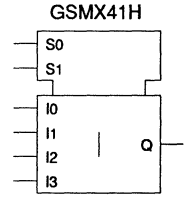
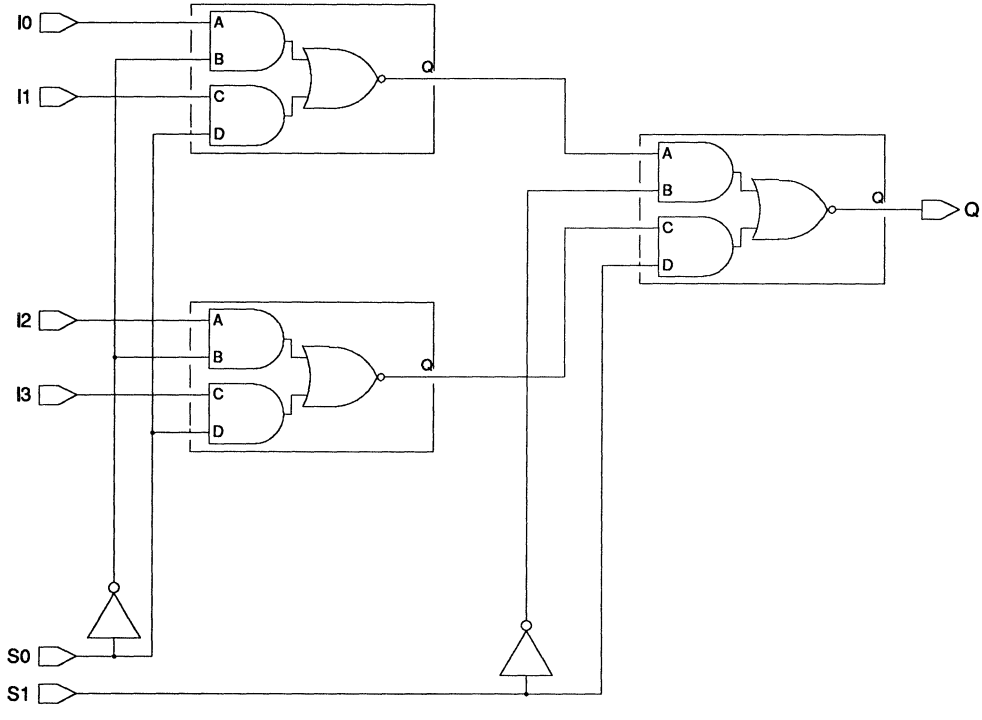
GSMX41H



Description: GSMX41H is a 4 bit non-inverting MUX.
Equivalent Gate Count: 8
Bolt Syntax: Q .GSMX41H I0 I1 I2 I3 S0 S1 ;
Truth Table

S0	S1	Q
L	L	I0
H	L	I1
L	H	I2
H	H	I3

Logic Schematic:



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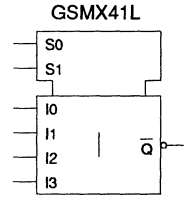
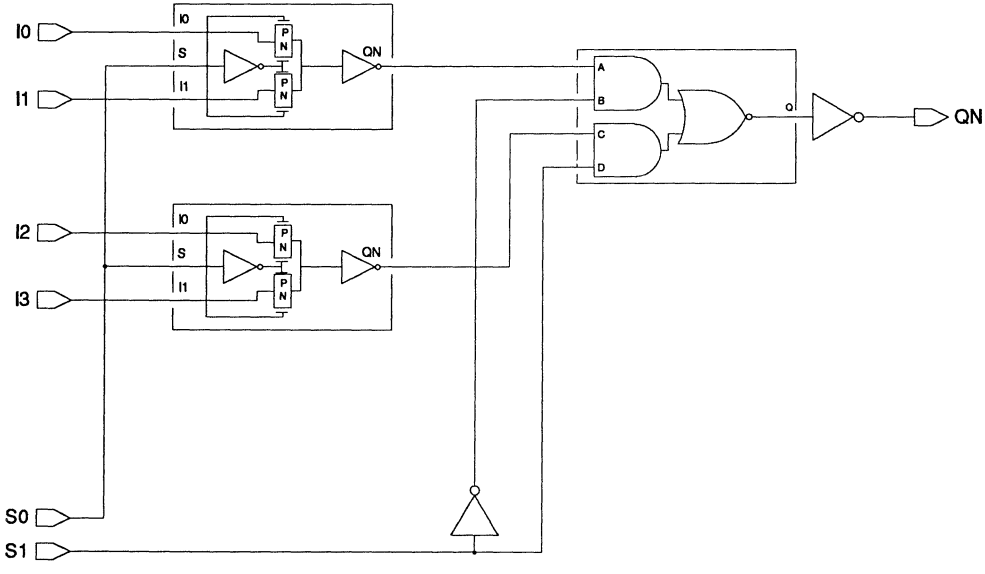
GSMX41L



Description: GSMX41L is a 4 bit inverting MUX.
Equivalent Gate Count: 8
Bolt Syntax: QN .GSMX41L I0 I1 I2 I3 S0 S1 ;
Truth Table

S0	S1	QN
L	L	I0N
H	L	I1N
L	H	I2N
H	H	I3N

Logic Schematic:



MSI Functions

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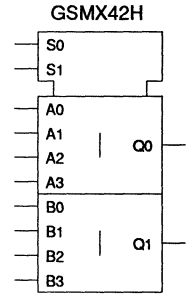
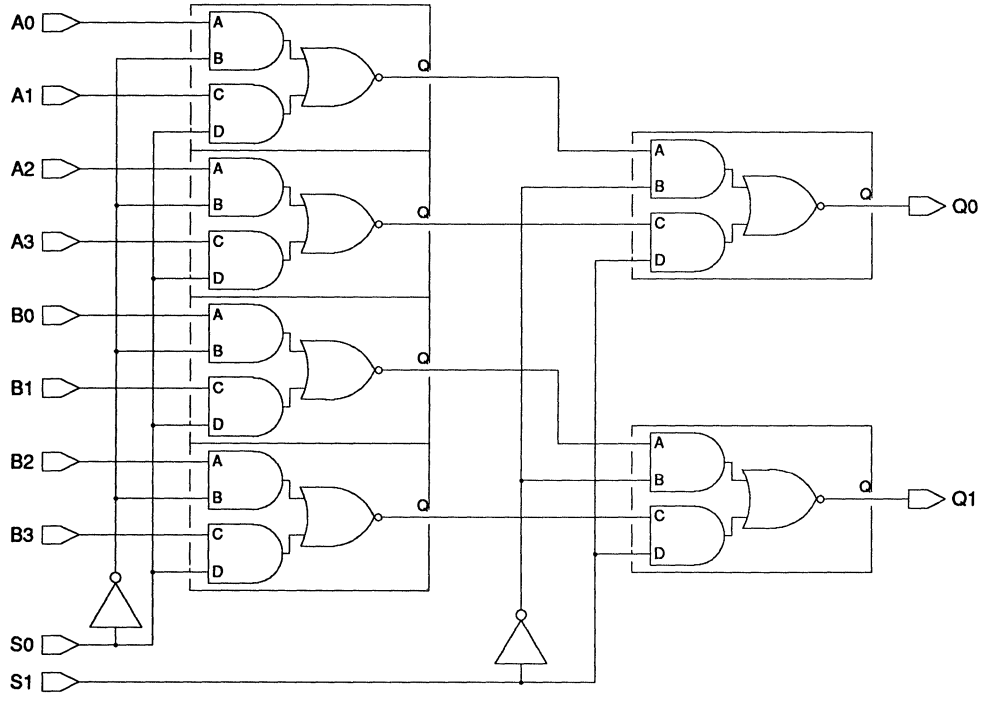
GSMX42H

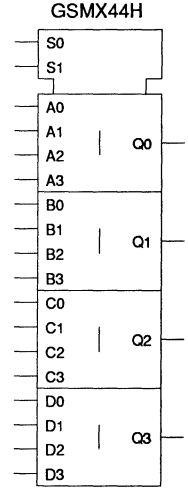


Description: GSMX42H is a dual 4 bit non-inverting MUX.
Equivalent Gate Count: 14
Bolt Syntax: Q0 Q1 .GSMX42H A0 A1 A2 A3 B0 B1 B2 B3 S0 S1 ;
Truth Table

S0	S1	Q0	Q1
L	L	A0	B0
H	L	A1	B1
L	H	A2	B2
H	H	A3	B3

Logic Schematic:





Description: GSMX44H is a quad 4 bit non-inverting MUX.

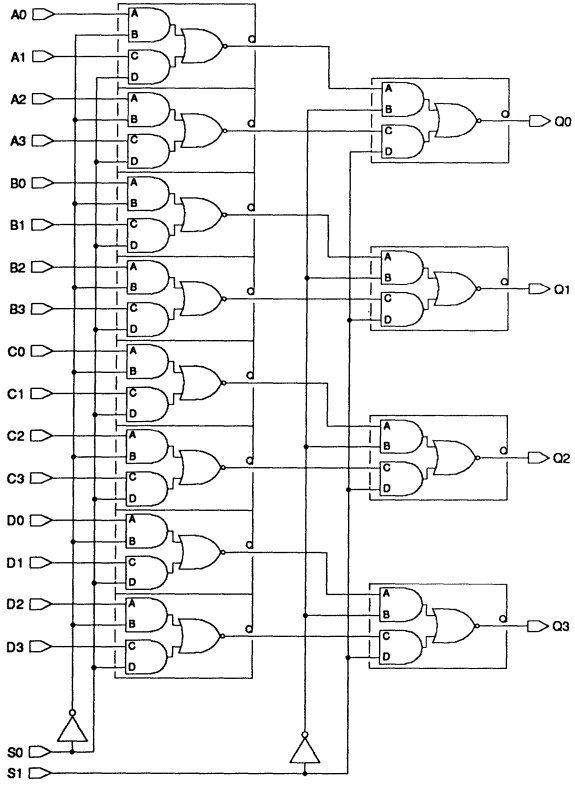
Equivalent Gate Count: 26

Bolt Syntax: Q0 Q1 Q2 Q3 .GSMX44H A0 A1 A2 A3 B0 B1 B2 B3 C0 C1 C2 C3 D0 D1 D2 D3 S0 S1 ;

Truth Table

S0	S1	Q0	Q1	Q2	Q3
L	L	A0	B0	C0	D0
H	L	A1	B1	C1	D1
L	H	A2	B2	C2	D2
H	H	A3	B3	C3	D3

Logic Schematic:



MSI Functions

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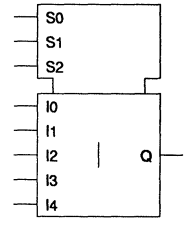
GSMX51H

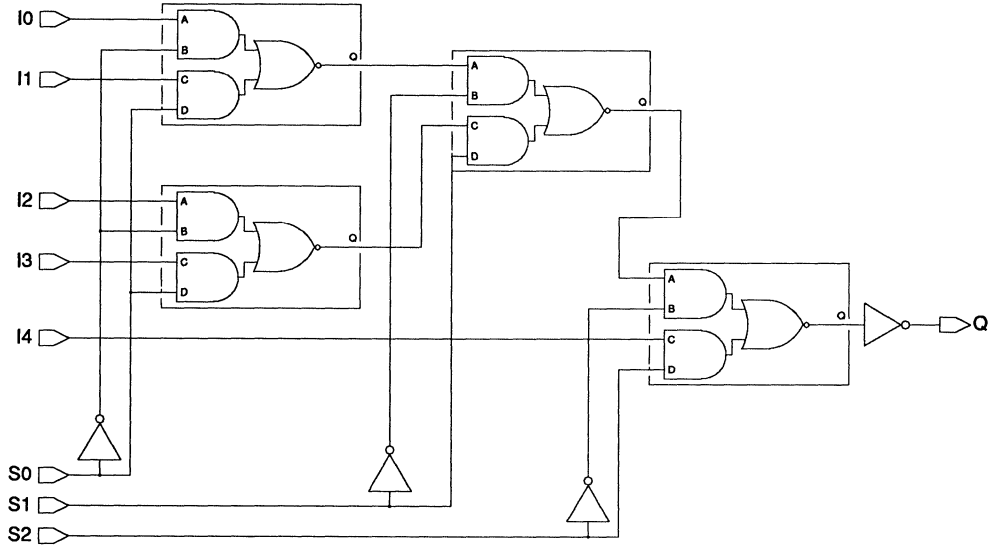
GSMX51H



Description: GSMX51H is a 5 bit non-inverting MUX.
Equivalent Gate Count: 12
Bolt Syntax: Q .GSMX51H I0 I1 I2 I3 I4 S0 S1 S2 ;
Truth Table

S0	S1	S2	Q
L	L	L	I0
H	L	L	I1
L	H	L	I2
H	H	L	I3
L	L	H	I4
H	L	H	I4
L	H	H	I4
H	H	H	I4

Logic Schematic:



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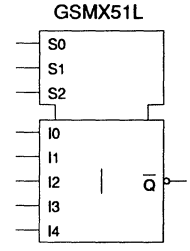
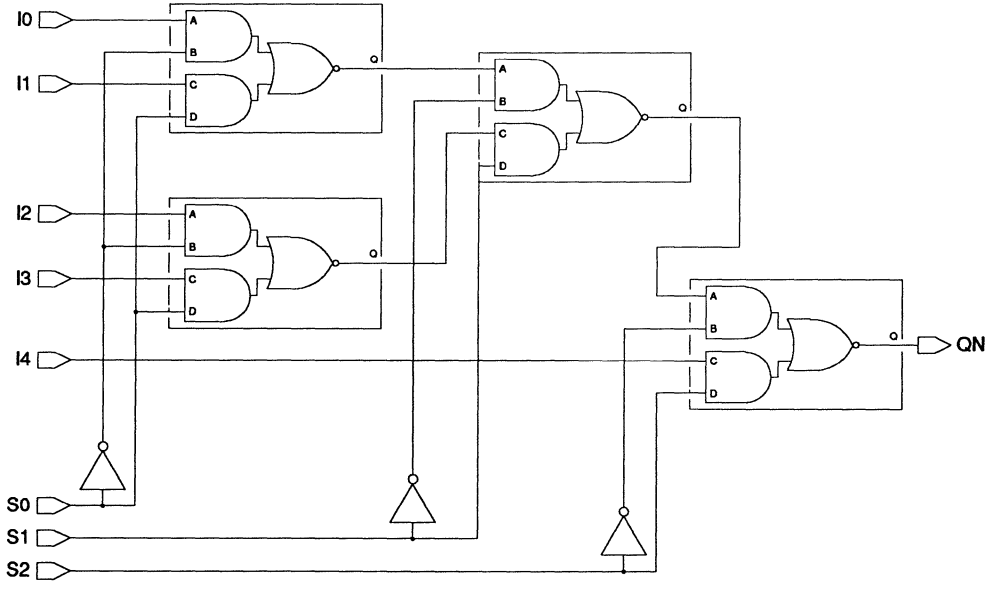
GSMX51L



Description: GSMX51L is a 5 bit inverting MUX.
Equivalent Gate Count: 11
Bolt Syntax: QN .GSMX51L I0 I1 I2 I3 I4 S0 S1 S2 ;
Truth Table

S0	S1	S2	QN
L	L	L	I0N
H	L	L	I1N
L	H	L	I2N
H	H	L	I3N
L	L	H	I4N
H	L	H	I4N
L	H	H	I4N
H	H	H	I4N

Logic Schematic:



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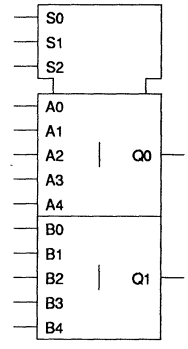
GSMX52H

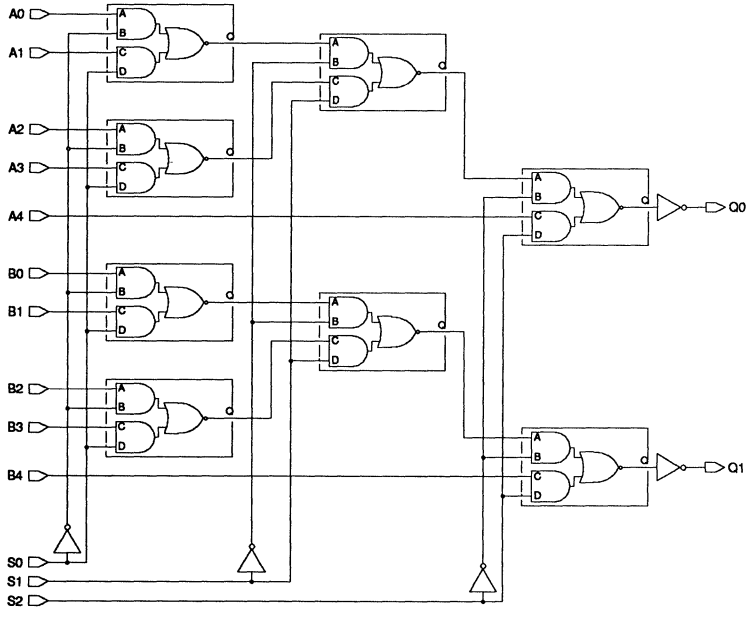
GSMX52H



Description: GSMX52H is a dual 5 bit non-inverting MUX.
Equivalent Gate Count: 21
Bolt Syntax: Q0 Q1 .GSMX52H A0 A1 A2 A3 A4 B0 B1 B2 B3 B4 S0 S1 S2 ;
Truth Table

S0	S1	S2	Q0	Q1
L	L	L	A0	B0
H	L	L	A1	B1
L	H	L	A2	B2
H	H	L	A3	B3
L	L	H	A4	B4
H	L	H	A4	B4
L	H	H	A4	B4
H	H	H	A4	B4

Logic Schematic:



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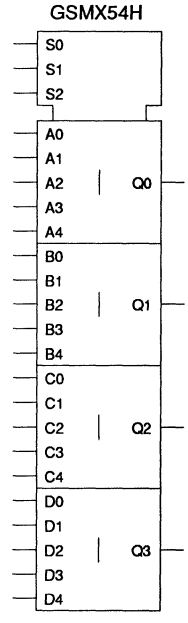
GSMX54H



Description: GSMX54H is a quad 5 bit non-inverting MUX.

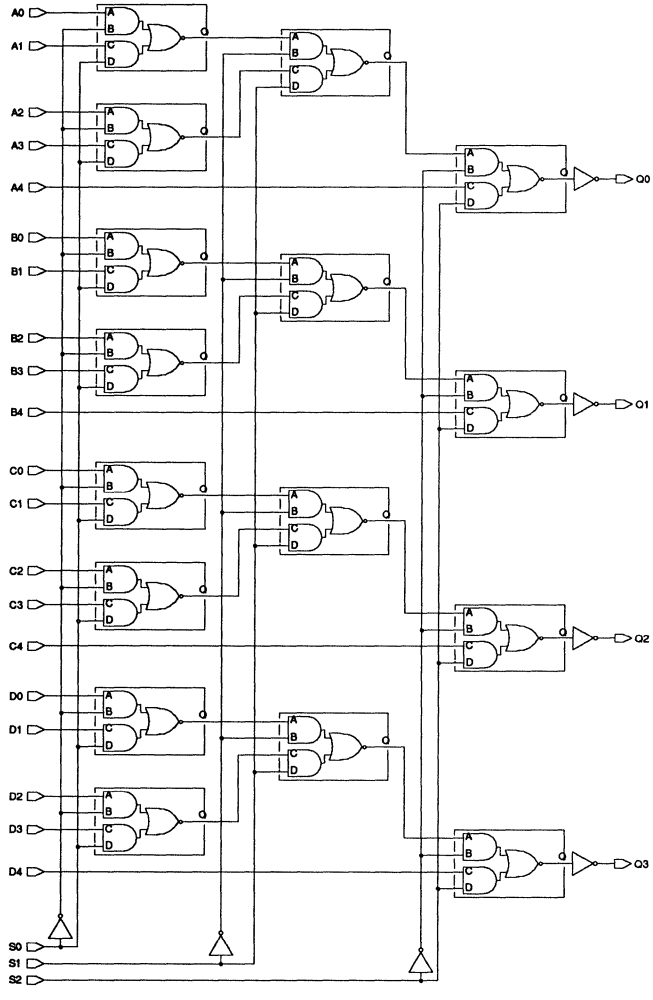
Equivalent Gate Count: 39

Bolt Syntax: Q0 Q1 Q2 Q3 .GSMX54H A0 A1 A2 A3 A4 B0 B1 B2 B3 B4 C0 C1 C2 C3 C4 D0 D1 D2 D3 D4 S0 S1 S2 ;

Truth Table

S0	S1	S2	Q0	Q1	Q2	Q3
L	L	L	A0	B0	C0	D0
H	L	L	A1	B1	C1	D1
L	H	L	A2	B2	C2	D2
H	H	L	A3	B3	C3	D3
L	L	H	A4	B4	C4	D4
H	L	H	A4	B4	C4	D4
L	H	H	A4	B4	C4	D4
H	H	H	A4	B4	C4	D4

Logic Schematic: On Next Page


A0
A1
A2
A3
A4
B0
B1
B2
B3
B4
C0
C1
C2
C3
C4
D0
D1
D2
D3
D4
S0
S1
S2
Q0
Q1
Q2
Q3

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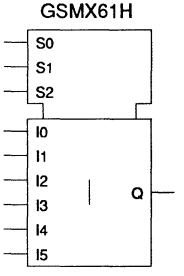
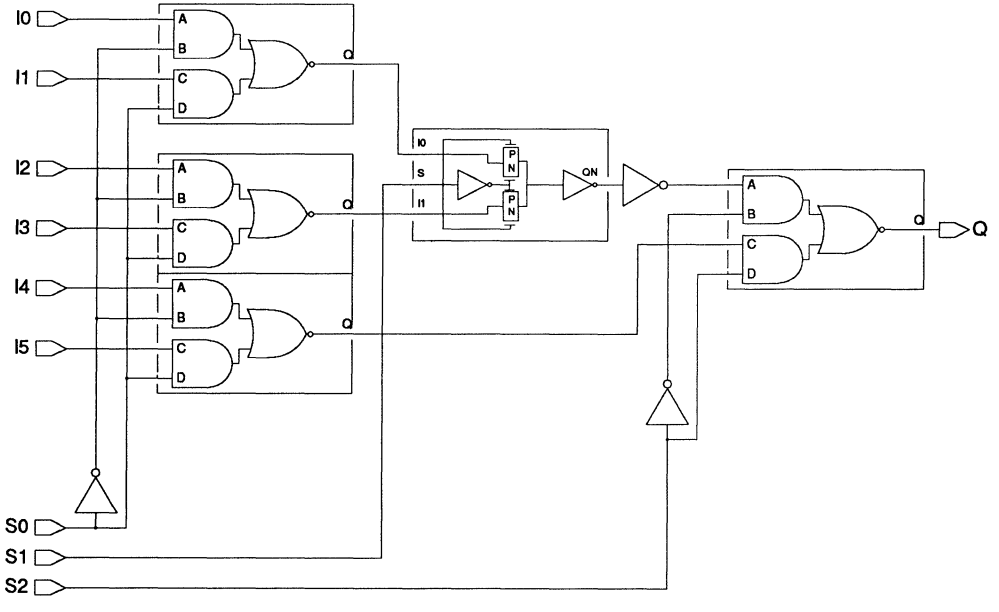
GSMX61H



Description: GSMX61H is a 6 bit non-inverting MUX.
Equivalent Gate Count: 13
Bolt Syntax: Q .GSMX61H I0 I1 I2 I3 I4 I5 S0 S1 S2 ;
Truth Table

S0	S1	S2	Q
L	L	L	I0
H	L	L	I1
L	H	L	I2
H	H	L	I3
L	L	H	I4
H	L	H	I5
L	H	H	I4
H	H	H	I5

Logic Schematic:



MSI Functions

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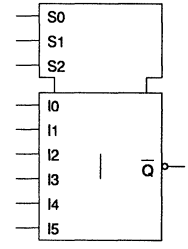
GSMX61L

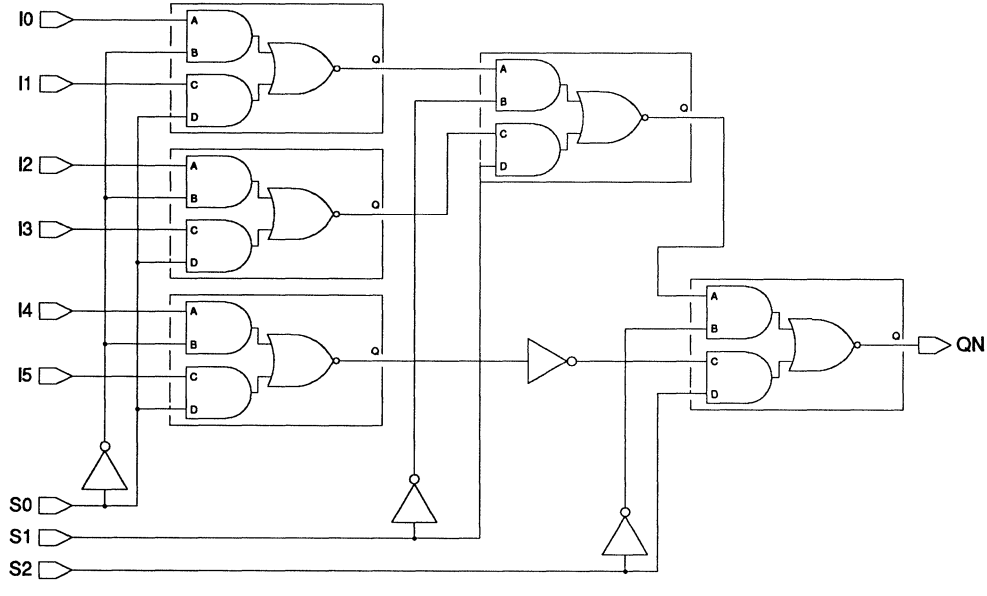
GSMX61L



Description: GSMX61L is a 6 bit inverting MUX.
Equivalent Gate Count: 14
Bolt Syntax: QN .GSMX61L I0 I1 I2 I3 I4 I5 S0 S1 S2 ;
Truth Table

S0	S1	S2	QN
L	L	L	I0N
H	L	L	I1N
L	H	L	I2N
H	H	L	I3N
L	L	H	I4N
H	L	H	I5N
L	H	H	I4N
H	H	H	I5N

Logic Schematic:



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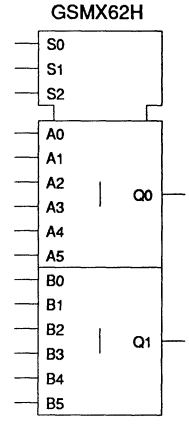
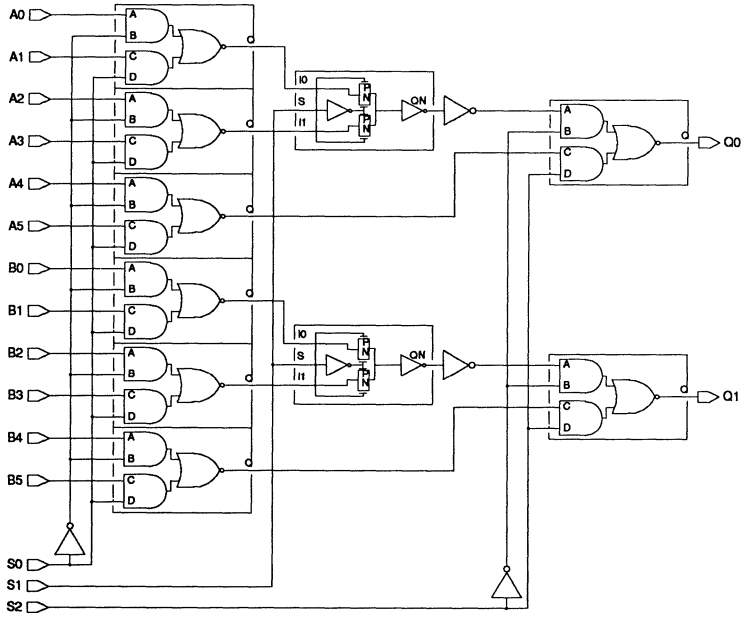
GSMX62H



Description: GSMX62H is a dual 6 bit non-inverting MUX.
Equivalent Gate Count: 24
Bolt Syntax: Q0 Q1 .GSMX62H A0 A1 A2 A3 A4 A5 B0 B1 B2 B3 B4 B5 S0 S1 S2 ;
Truth Table

S0	S1	S2	Q0	Q1
L	L	L	A0	B0
H	L	L	A1	B1
L	H	L	A2	B2
H	H	L	A3	B3
L	L	H	A4	B4
H	L	H	A5	B5
L	H	H	A4	B4
H	H	H	A5	B5

Logic Schematic:



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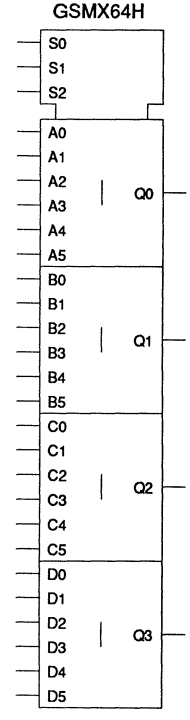
GSMX64H



Description: GSMX64H is a quad 6 bit non-inverting MUX.

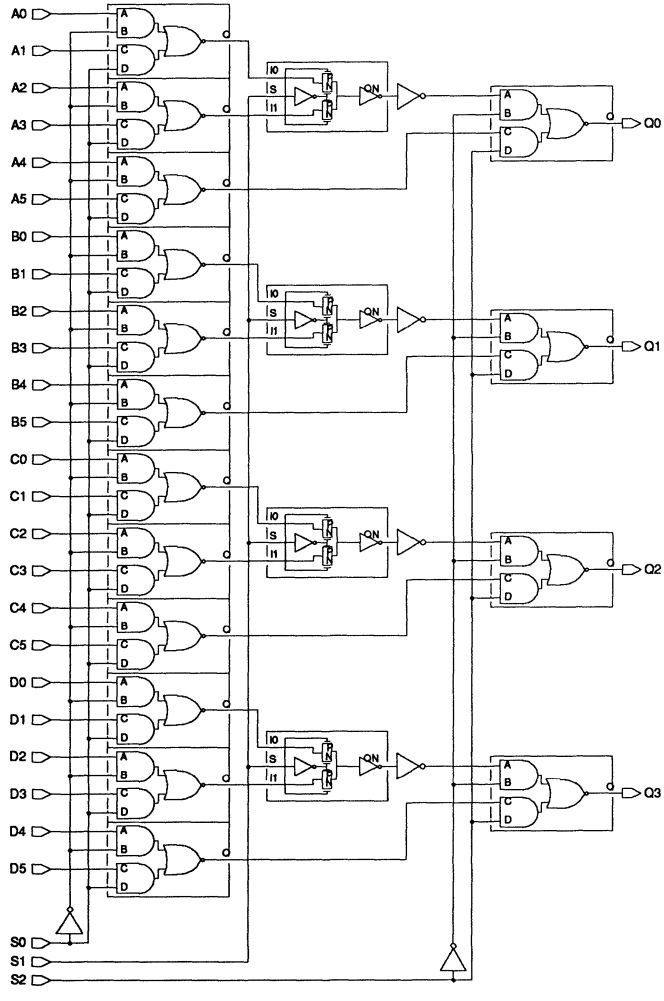
Equivalent Gate Count: 46

Bolt Syntax: Q0 Q1 Q2 Q3 .GSMX64H A0 A1 A2 A3 A4 A5 B0 B1 B2 B3 B4 B5 C0 C1 C2 C3 C4 C5 D0 D1 D2 D3 D4 D5 S0 S1 S2 ;

Truth Table

S0	S1	S2	Q0	Q1	Q2	Q3
L	L	L	A0	B0	C0	D0
H	L	L	A1	B1	C1	D1
L	H	L	A2	B2	C2	D2
H	H	L	A3	B3	C3	D3
L	L	H	A4	B4	C4	D4
H	L	H	A5	B5	C5	D5
L	H	H	A4	B4	C4	D4
H	H	H	A5	B5	C5	D5

Logic Schematic: On Next Page


A0
A1
A2
A3
A4
A5
B0
B1
B2
B3
B4
B5
C0
C1
C2
C3
C4
C5
D0
D1
D2
D3
D4
D5
S0
S1
S2
I0
S
I1
ON
Q0
Q1
Q2
Q3

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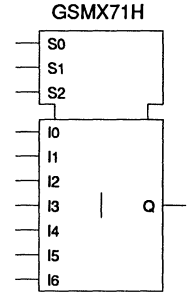
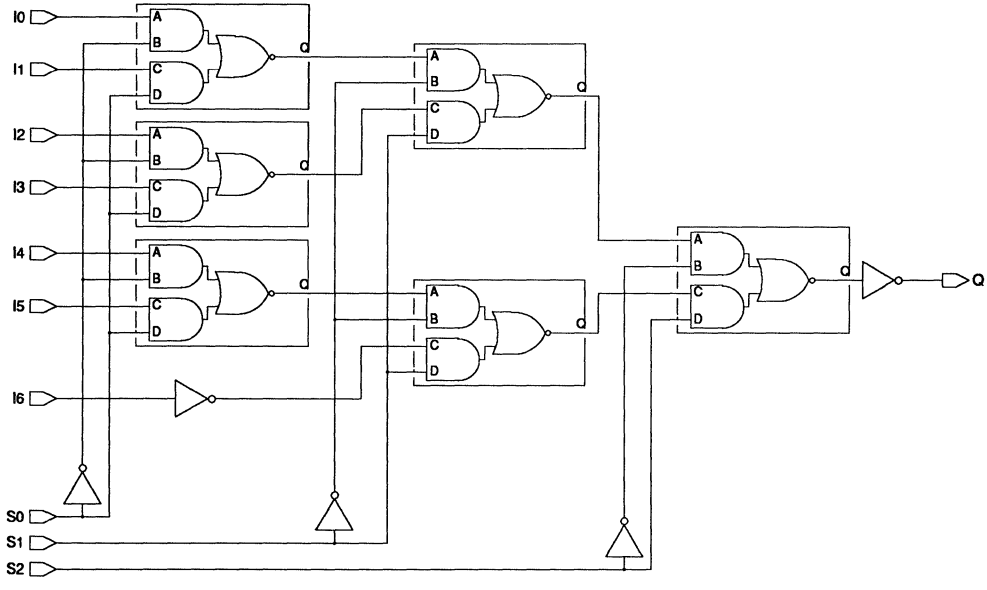
GSMX71H



Description: GSMX71H is a 7 bit non-inverting MUX.
Equivalent Gate Count: 17
Bolt Syntax: Q .GSMX71H I0 I1 I2 I3 I4 I5 I6 S0 S1 S2 ;
Truth Table

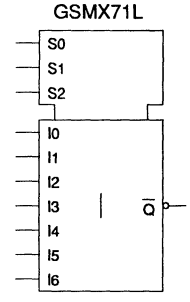
S0	S1	S2	Q
L	L	L	IO
H	L	L	I1
L	H	L	I2
H	H	L	I3
L	L	H	I4
H	L	H	I5
L	H	H	I6
H	H	H	I6

Logic Schematic:



April, 1992

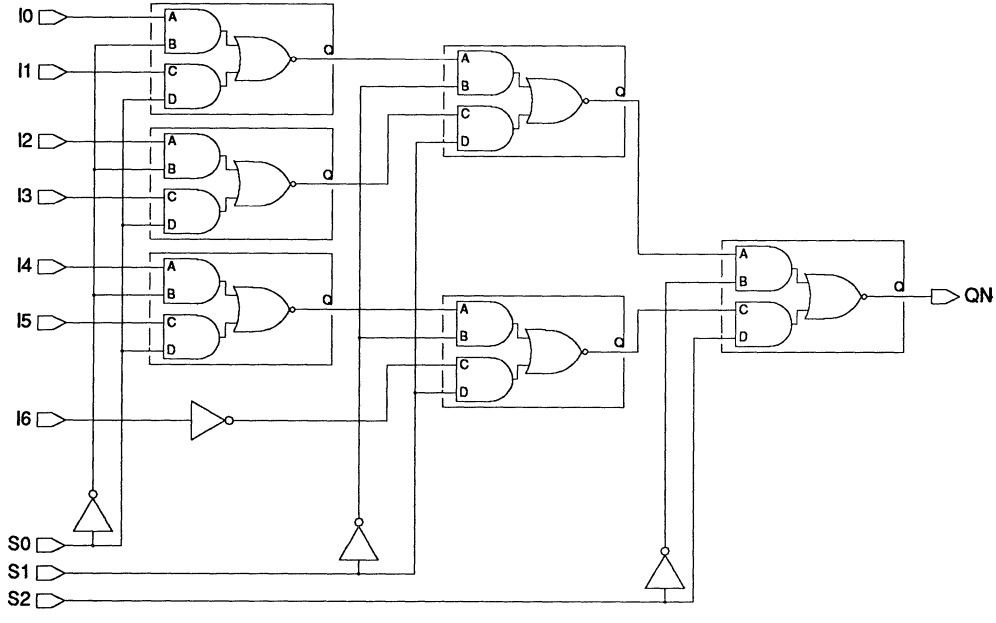
GSMX71L



Description: GSMX71L is a 7 bit inverting MUX.
Equivalent Gate Count: 16
Bolt Syntax: QN .GSMX71L I0 I1 I2 I3 I4 I5 I6 S0 S1 S2 ;
Truth Table

S0	S1	S2	QN
L	L	L	I0N
H	L	L	I1N
L	H	L	I2N
H	H	L	I3N
L	L	H	I4N
H	L	H	I5N
L	H	H	I6N
H	H	H	I6N

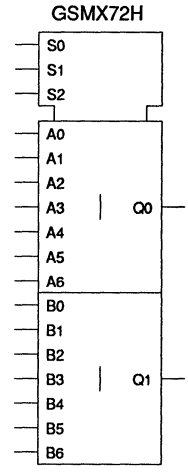
Logic Schematic:



MSI Functions

April, 1992

GSMX72H



Description: GSMX72H is a dual 7 bit non-inverting MUX.

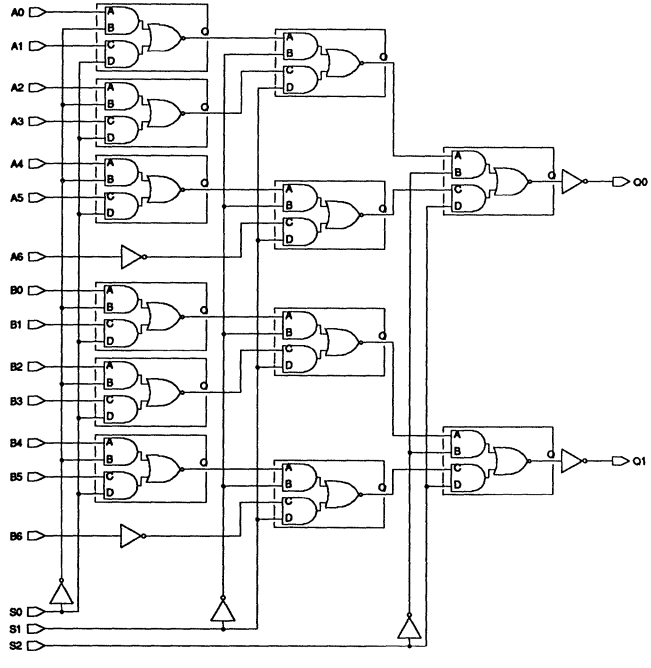
Equivalent Gate Count: 31

Bolt Syntax: Q0 Q1 .GSMX72H A0 A1 A2 A3 A4 A5 A6 B0 B1 B2 B3 B4 B5 B6 S0 S1 S2 ;

Truth Table

S0	S1	S2	Q0	Q1
L	L	L	A0	B0
H	L	L	A1	B1
L	H	L	A2	B2
H	H	L	A3	B3
L	L	H	A4	B4
H	L	H	A5	B5
L	H	H	A6	B6
H	H	H	A6	B6

Logic Schematic:



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GSMX74H

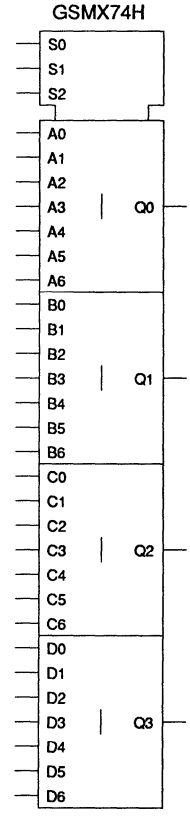
Description: GSMX74H is a quad 7 bit non-inverting MUX.

Equivalent Gate Count: 59

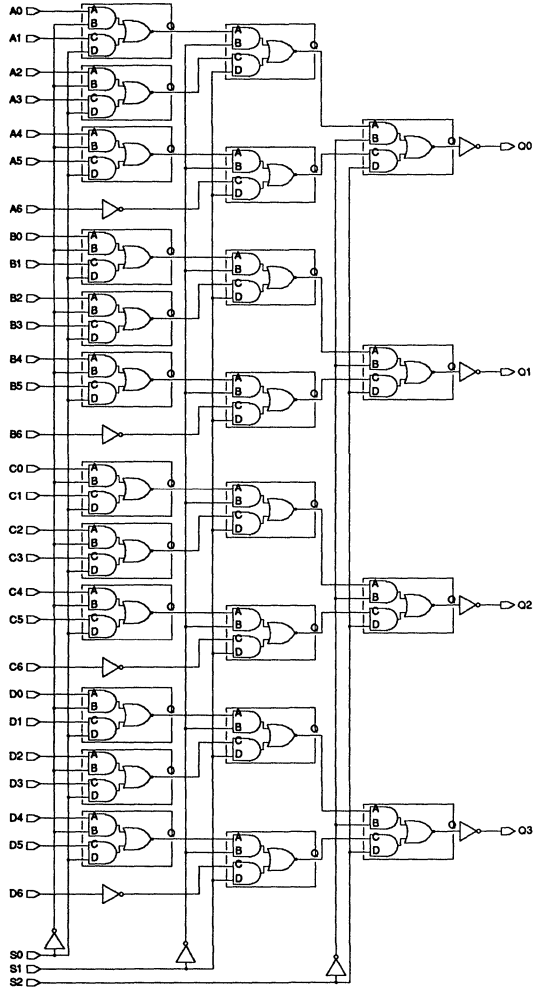
Bolt Syntax: Q0 Q1 Q2 Q3 .GSMX74H A0 A1 A2 A3 A4 A5 A6 B0 B1 B2 B3 B4 B5 B6 C0 C1 C2 C3 C4 C5 C6 D0 D1 D2 D3 D4 D5 D6 S0 S1 S2 ;

Truth Table

S0	S1	S2	Q0	Q1	Q2	Q3
L	L	L	A0	B0	C0	D0
H	L	L	A1	B1	C1	D1
L	H	L	A2	B2	C2	D2
H	H	L	A3	B3	C3	D3
L	L	H	A4	B4	C4	D4
H	L	H	A5	B5	C5	D5
L	H	H	A6	B6	C6	D6
H	H	H	A6	B6	C6	D6



Logic Schematic: On Next Page


A0
A1
A2
A3
A4
A5
A6
B0
B1
B2
B3
B4
B5
B6
C0
C1
C2
C3
C4
C5
C6
D0
D1
D2
D3
D4
D5
D6
S0
S1
S2
Q0
Q1
Q2
Q3

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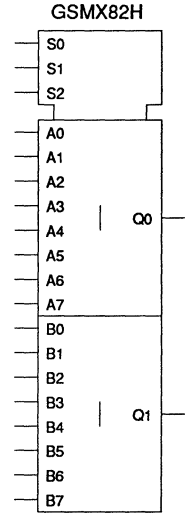
GSMX82H



Description: GSMX82H is a dual 8 bit non-inverting MUX.

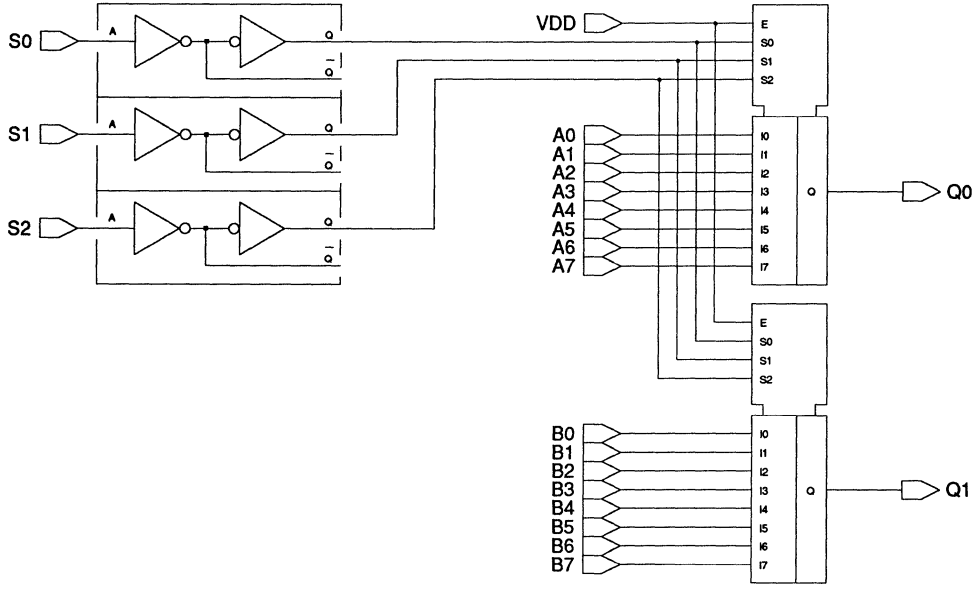
Equivalent Gate Count: 40

Bolt Syntax: Q0 Q1 .GSMX82H A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 S0 S1 S2 ;

Truth Table

S0	S1	S2	Q0	Q1
L	L	L	A0	B0
H	L	L	A1	B1
L	H	L	A2	B2
H	H	L	A3	B3
L	L	H	A4	B4
H	L	H	A5	B5
L	H	H	A6	B6
H	H	H	A7	B7

Logic Schematic:



MSI Functions

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GSMX84H

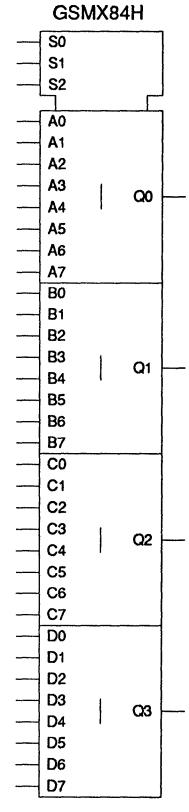
Description: GSMX84H is a quad 8 bit non-inverting MUX.

Equivalent Gate Count: 75

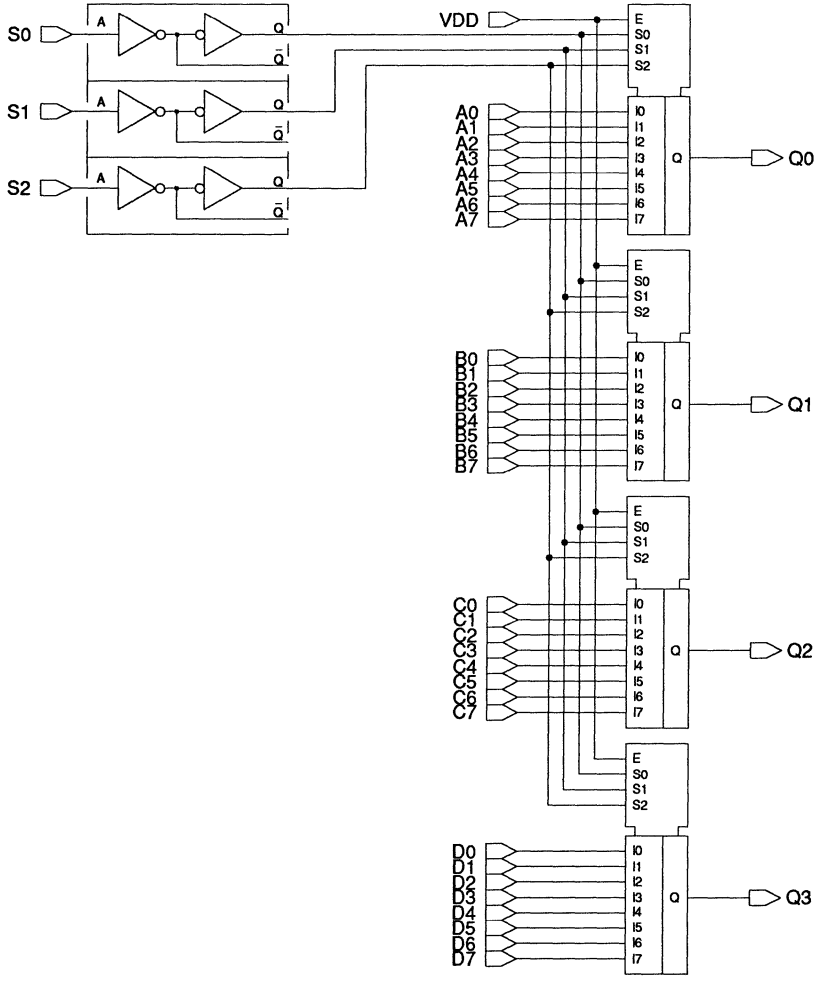
Bolt Syntax: Q0 Q1 Q2 Q3 .GSMX84H A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 C0 C1 C2 C3 C4 C5 C6 C7 D0 D1 D2 D3 D4 D5 D6 D7 S0 S1 S2 ;

Truth Table

S0	S1	S2	Q0	Q1	Q2	Q3
L	L	L	A0	B0	C0	D0
H	L	L	A1	B1	C1	D1
L	H	L	A2	B2	C2	D2
H	H	L	A3	B3	C3	D3
L	L	H	A4	B4	C4	D4
H	L	H	A5	B5	C5	D5
L	H	H	A6	B6	C6	D6
H	H	H	A7	B7	C7	D7



Logic Schematic: On Next Page


S0
S1
S2
A
Q
VDD
E
S0
S1
S2
A0
A1
A2
A3
A4
A5
A6
A7
I0
I1
I2
I3
I4
I5
I6
I7
Q0
B0
B1
B2
B3
B4
B5
B6
B7
Q1
C0
C1
C2
C3
C4
C5
C6
C7
Q2
D0
D1
D2
D3
D4
D5
D6
D7
Q3

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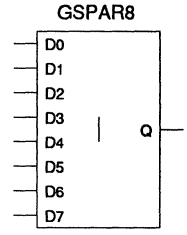
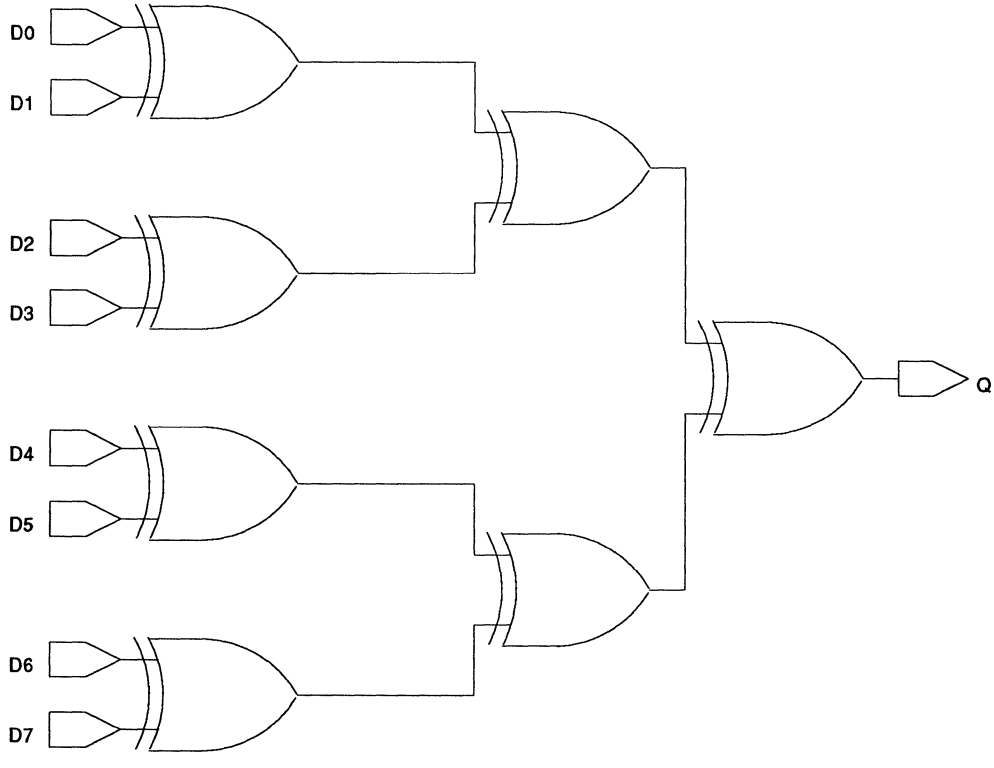
GSPAR8



Description: GSPAR8 is an 8 bit odd parity detector.
Equivalent Gate Count: 21
Bolt Syntax: Q .GSPAR8 D0 D1 D2 D3 D4 D5 D6 D7 ;

Logic Schematic:



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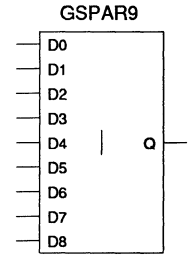
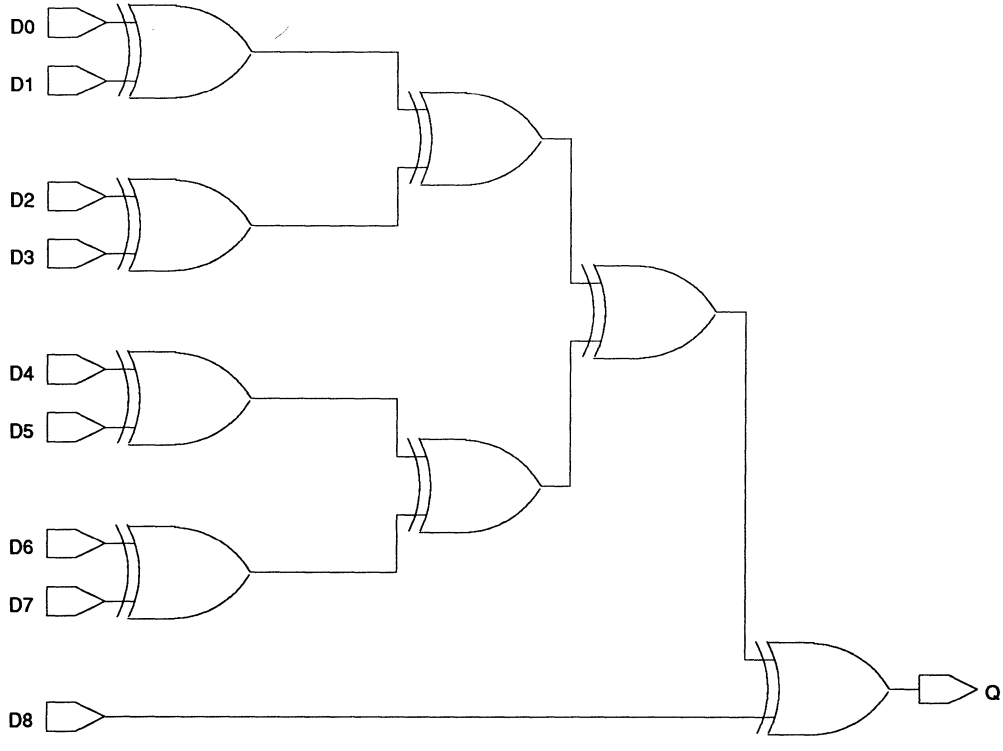
GSPAR9



Description: GSPAR9 is a 9 bit odd parity detector.
Equivalent Gate Count: 24
Bolt Syntax: Q .GSPAR9 D0 D1 D2 D3 D4 D5 D6 D7 D8 ;

Logic Schematic:



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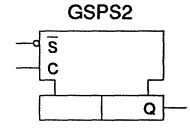
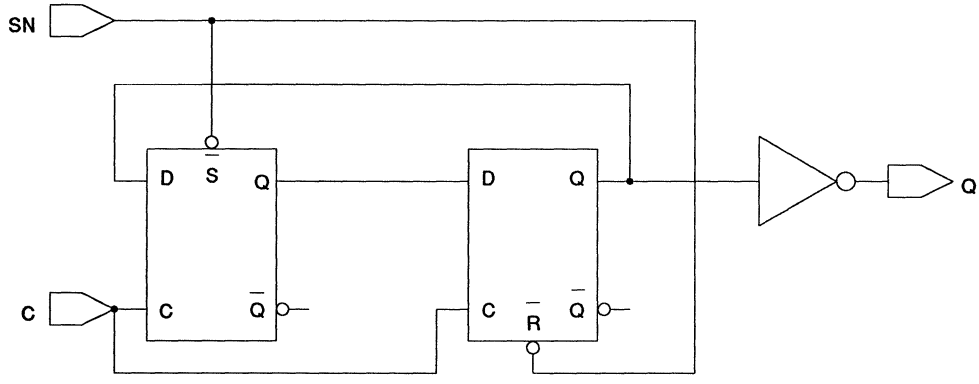
GSPS2



Description: GSPS2 is a divide by 2 external clock prescaler.
Equivalent Gate Count: 13
Bolt Syntax: Q .GSPS2 C SN ;

Logic Schematic:



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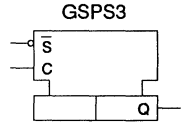
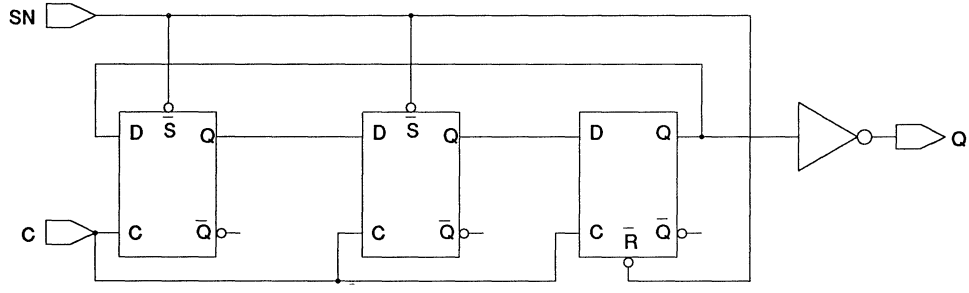
GSPS3



Description: GSPS3 is a divide by 3 external clock prescaler.
Equivalent Gate Count: 19
Bolt Syntax: Q .GSPS3 C SN ;

Logic Schematic:



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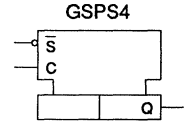
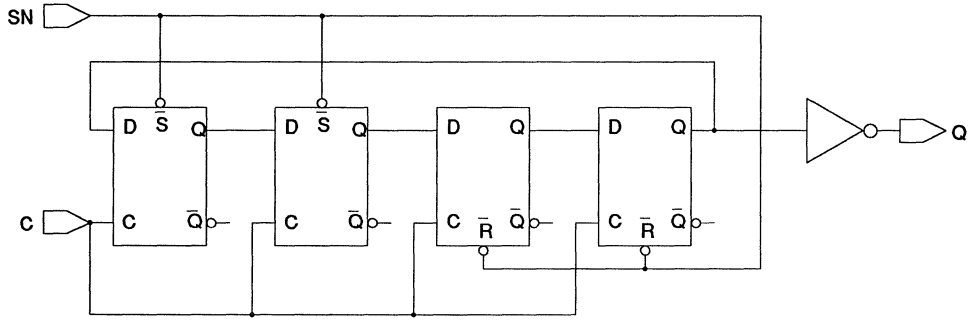
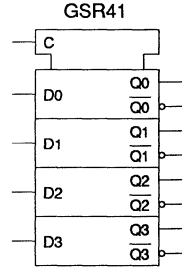
GSPS4



Description: GSPS4 is a divide by 4 external clock prescaler.
Equivalent Gate Count: 25
Bolt Syntax: Q .GSPS4 C SN ;

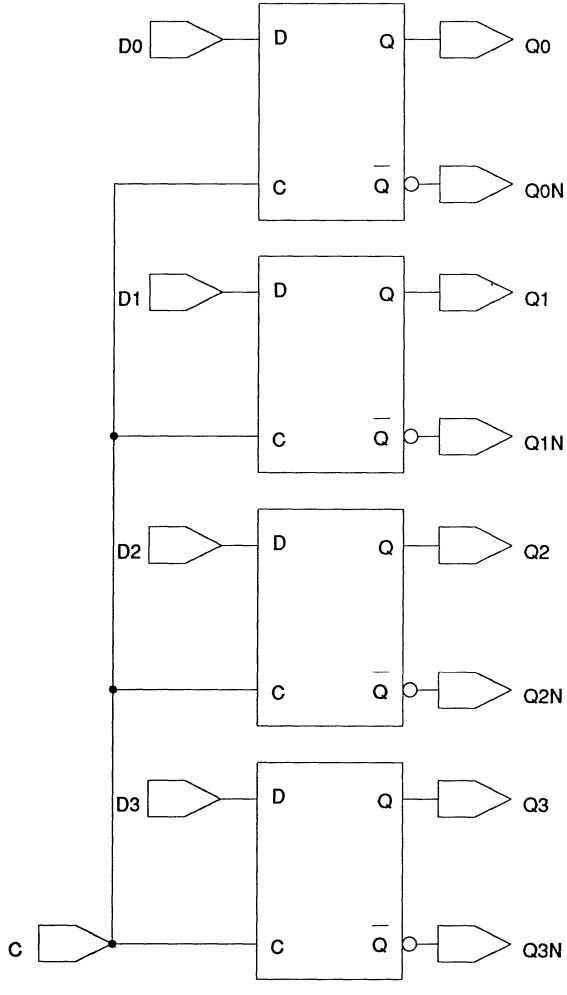
Logic Schematic:





Description: GSR41 is a 4 bit data register.
Equivalent Gate Count: 20
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSR41 D0 D1 D2 D3 C ;

Logic Schematic:



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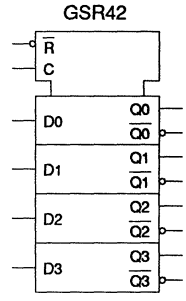
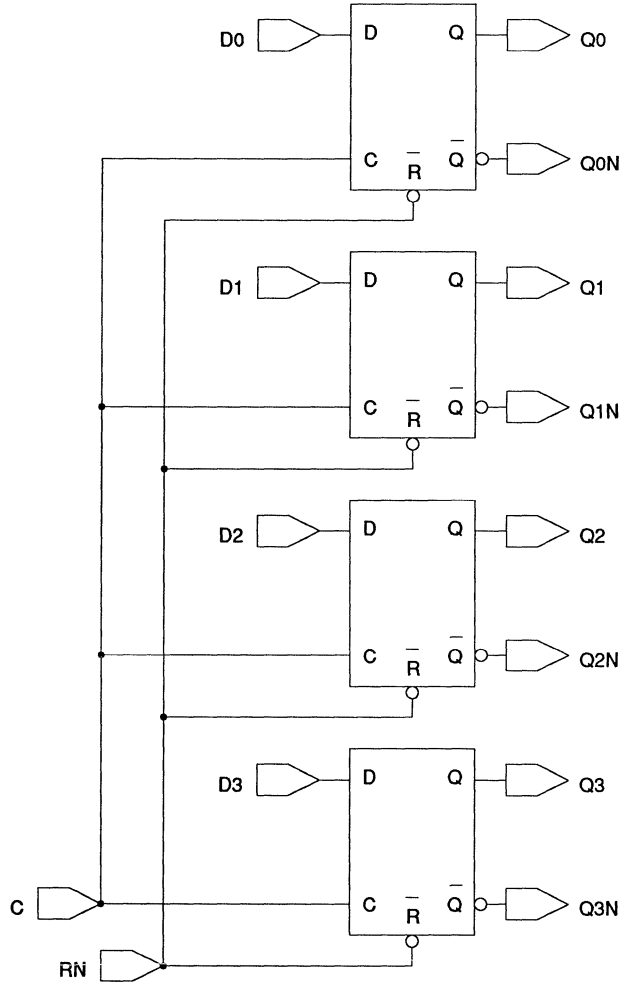
GSR42



Description: GSR42 is a 4 bit data register, with reset not.
Equivalent Gate Count: 24
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSR42 D0 D1 D2 D3 C RN ;

Logic Schematic:



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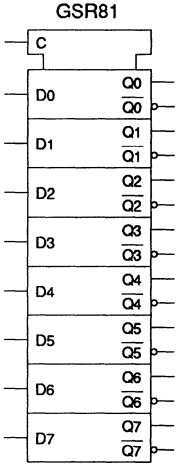
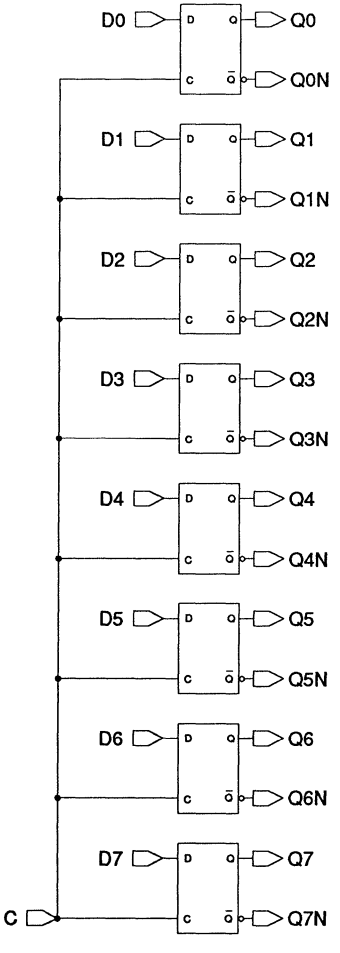
GSR81



Description: GSR81 is an 8 bit data register.
Equivalent Gate Count: 40
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N
.GSR81 D0 D1 D2 D3 D4 D5 D6 D7 C ;

Logic Schematic:



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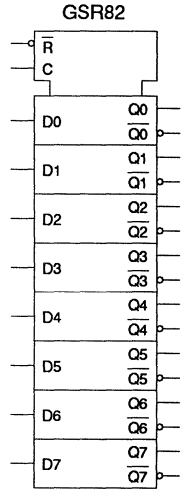
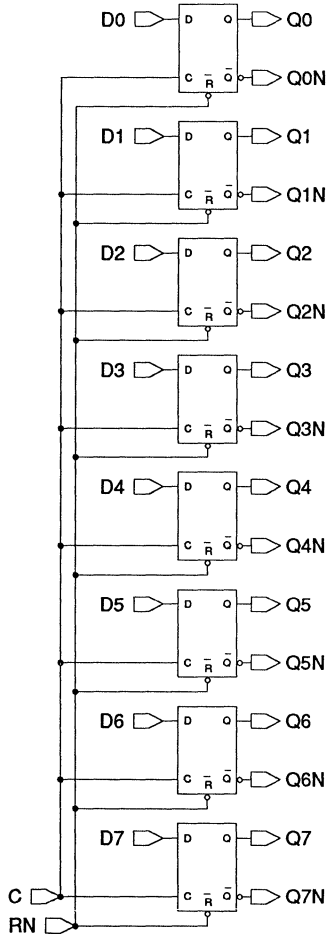
GSR82



Description: GSR82 is an 8 bit data register, with reset not.
Equivalent Gate Count: 48
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N Q4 Q4N Q5 Q5N Q6 Q6N Q7 Q7N
.GSR82 D0 D1 D2 D3 D4 D5 D6 D7 C RN ;

Logic Schematic:



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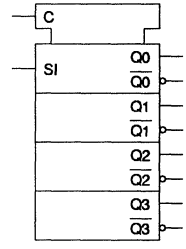
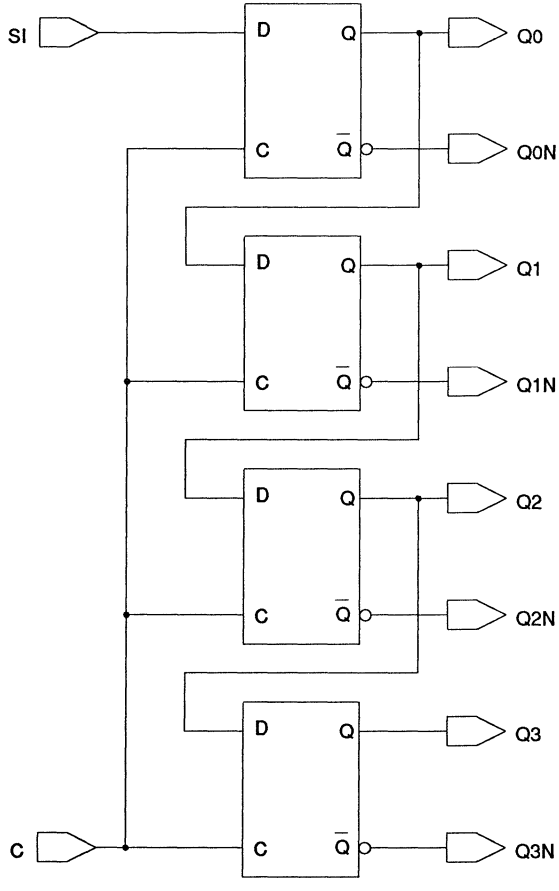
GSSR41

GSSR41



Description: GSSR41 is a 4 bit shift register.
Equivalent Gate Count: 20
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSSR41 SI C ;

Logic Schematic:



MSI Functions

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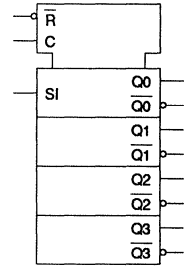
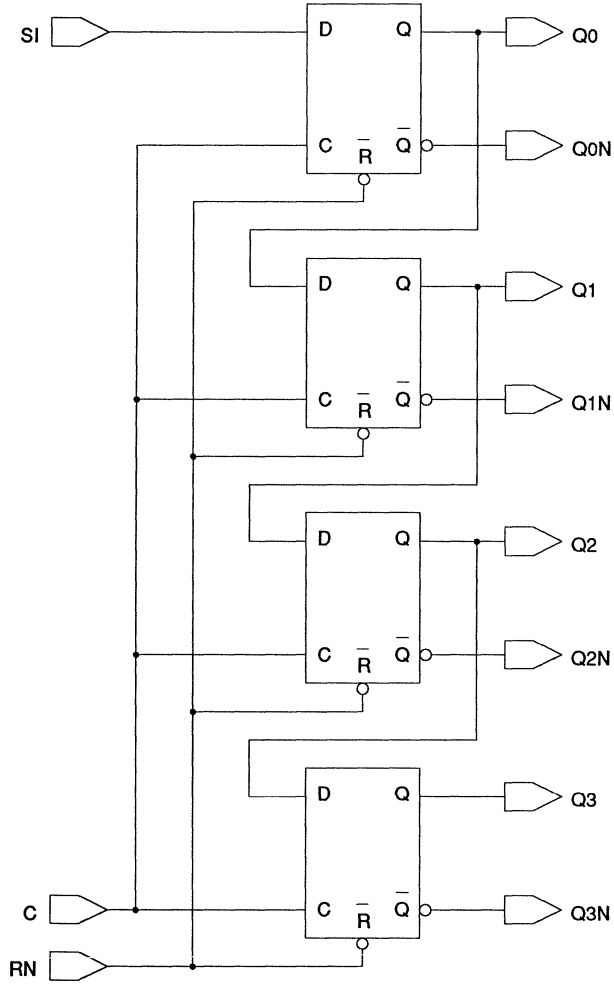
GSSR42

GSSR42



Description: GSSR42 is a 4 bit shift register, with reset not.
Equivalent Gate Count: 24
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSSR42 SI C RN ;

Logic Schematic:



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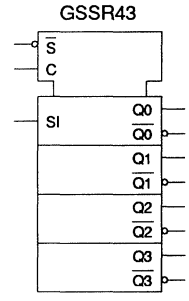
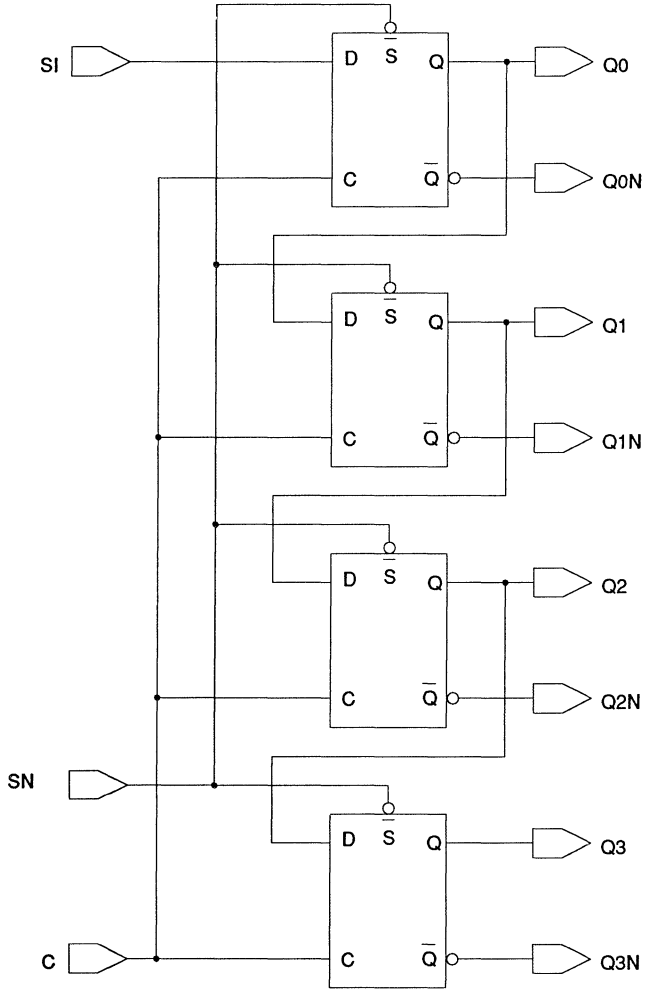
GSSR43



Description: GSSR43 is a 4 bit shift register, with set not.
Equivalent Gate Count: 24
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSSR43 SI C SN ;

Logic Schematic:



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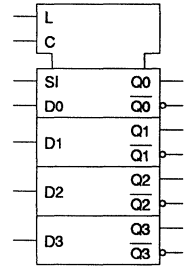
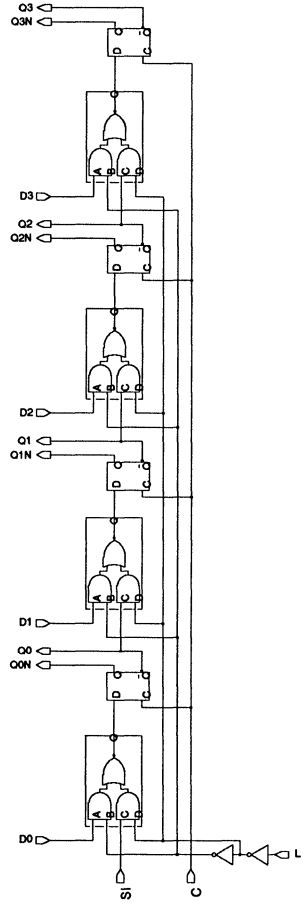
GSSR44

GSSR44



Description: GSSR44 is a 4 bit shift register, synchronous parallel load.
Equivalent Gate Count: 30
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSSR44 SI D0 D1 D2 D3 L C ;

Logic Schematic:



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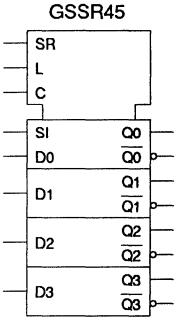
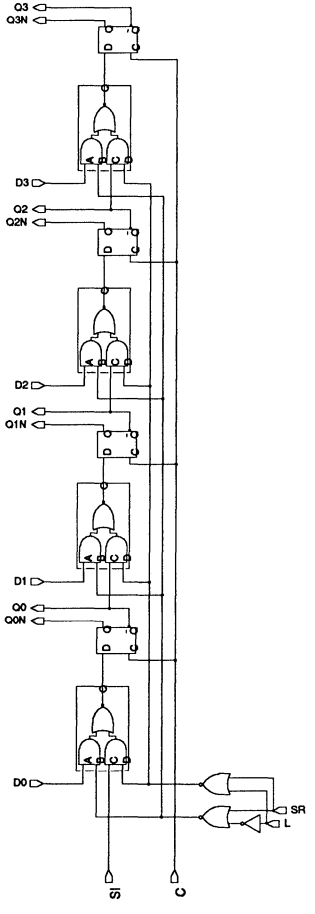
GSSR45



Description: GSSR45 is a 4 bit shift register, synchronous parallel load and reset.
Equivalent Gate Count: 31
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSSR45 SI D0 D1 D2 D3 L SR C ;

Logic Schematic:



MSI Functions

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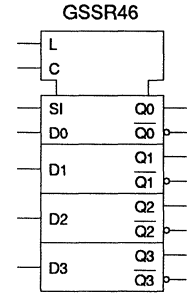
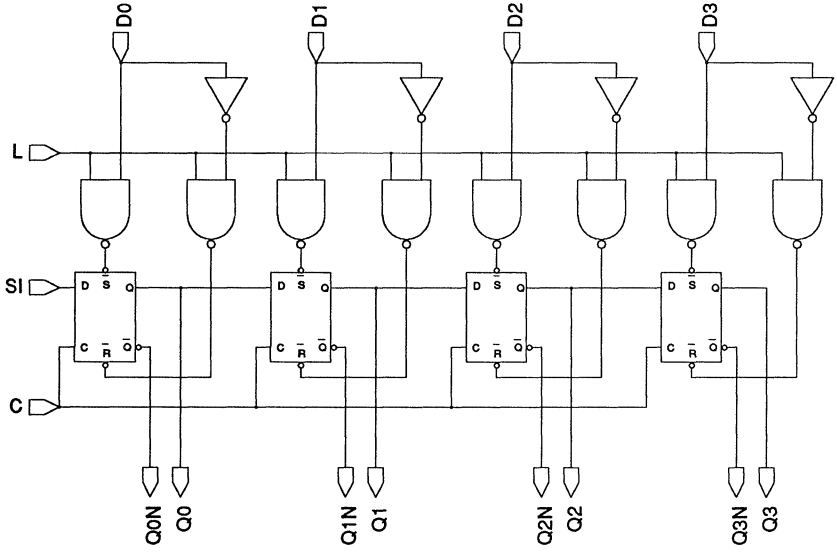
GSSR46



Description: GSSR46 is a 4 bit shift register, asynchronous parallel load.
Equivalent Gate Count: 40
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSSR46 SI D0 D1 D2 D3 L C ;

Logic Schematic:



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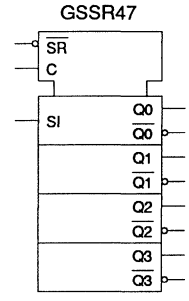
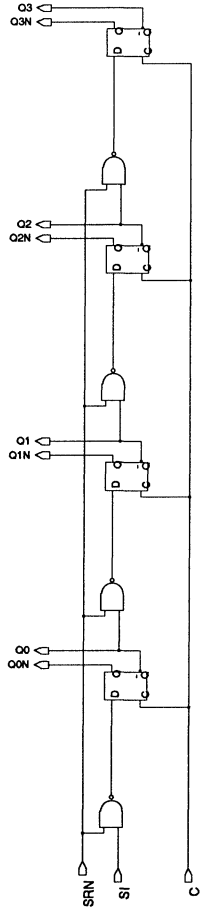
GSSR47



Description: GSSR47 is a 4 bit shift register, with synchronous reset not.
Equivalent Gate Count: 24
Bolt Syntax: Q0 Q0N Q1 Q1N Q2 Q2N Q3 Q3N .GSSR47 SI SRN C ;

Logic Schematic:



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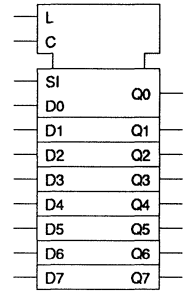
GSSR84

GSSR84

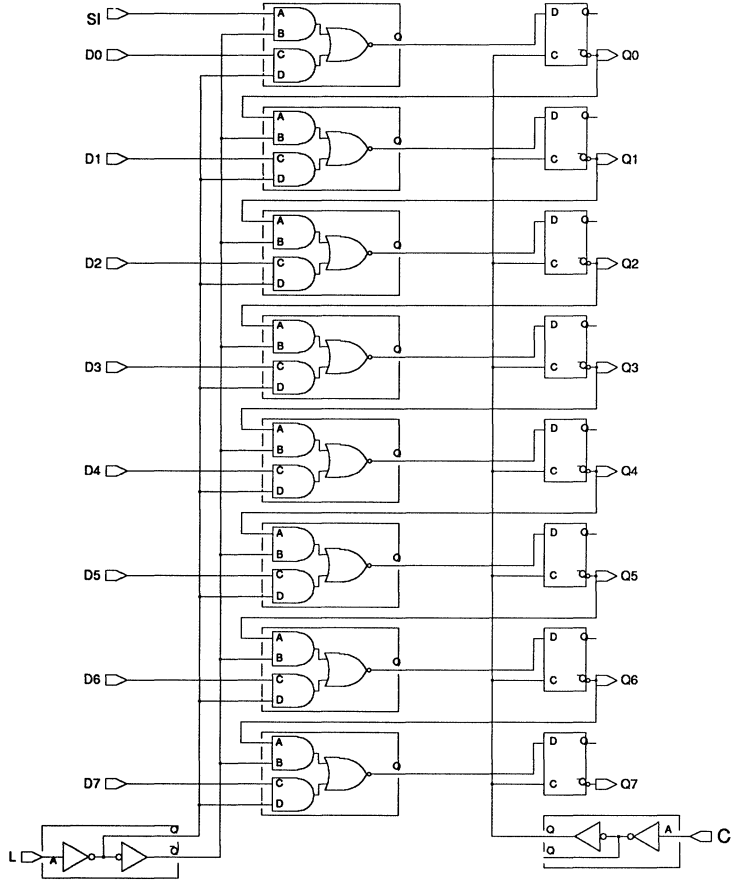


Description: GSSR84 is a 8 bit shift register with 2 bit multiplexed inputs with sync parallel load.

Equivalent Gate Count: 60

Bolt Syntax: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 .GSSR84 SI D0 D1 D2 D3 D4 D5 D6 D7 L C ;

Logic Schematic:



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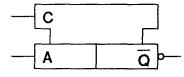
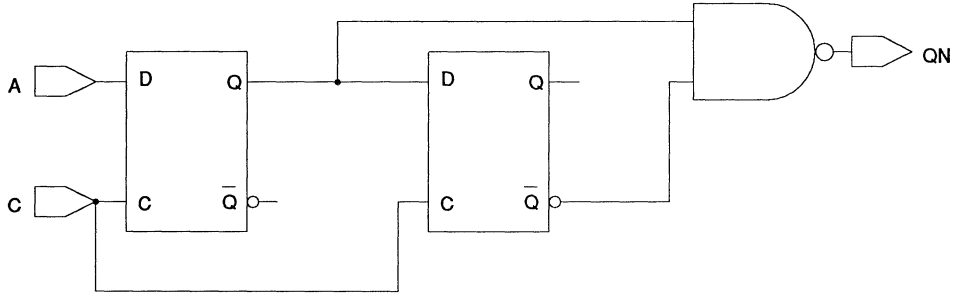
GSSYNC01

GSSYNC01



Description: GSSYNC01 is a synchronizer for asynchronous 0 to 1 event.
Equivalent Gate Count: 11
Bolt Syntax: QN .GSSYNC01 A C ;
Logic Schematic:



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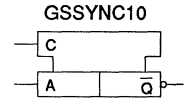
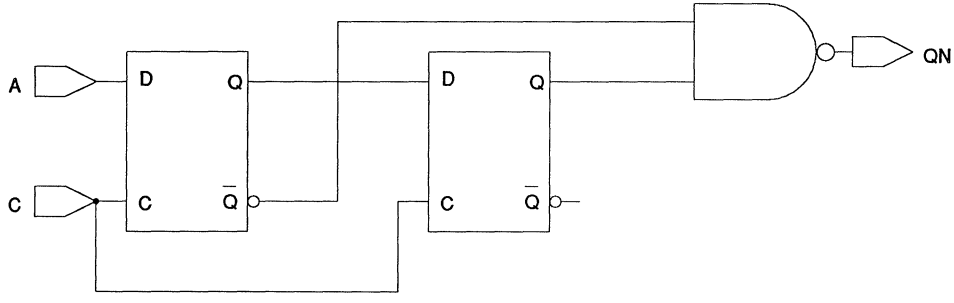
GSSYNC10



Description: GSSYNC10 is a synchronizer for asynchronous 1 to 0 event.
Equivalent Gate Count: 11
Bolt Syntax: QN .GSSYNC10 A C ;
Logic Schematic:



SECTION 5

DIGITAL MEGACELL FUNCTIONS

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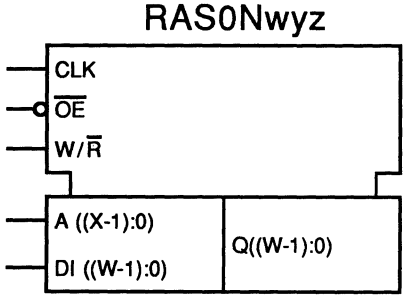
RASONwyz MxN Static RAM

Features

- 9.62 nsec typical cycle time for a 32 x 4 RAM with a 0.33pF load
- Read-Modify-Write cycle possible
- Low standby power when the clock is stopped
- Separate input and output ports with full parallel access
- 3-State outputs interface internal data buses directly
- Precharged design for faster operation with less silicon area

LOGIC SYMBOL



Note 1: A0 is the LSB

Note 2: X represents the number of address lines

Description

This series of 1.0m double-metal MxN RAMs operates within a power supply voltage range of 4.5V to 5.5V. The RASON series has 3-state outputs with active low Output Enable Not (OEN). The circuit is precharged when the clock is high, and the read and write operations occur when the clock is low. The outputs become valid a short time after the falling edge of the clock and stay valid until the next falling edge of the clock. The address lines are latched on the falling edge of the clock. The clock is used only to precharge the circuit and operate the latches; the memory does not need a refresh signal. The clock and all of the other inputs can be held stable indefinitely with no loss of memory as long as power is supplied to the RAM.

Within limits specified below, the user has flexibility in specifying the logical size of the RAM, including both word size and number of address locations. Within the name as shown above, the "wyz" represents a three character sequence assigned to each RAM configuration which uniquely identifies that particular configuration. Furthermore, the "S", "0", and "N" represent a single port RAM, version 0, and an active low output enable, respectively. The "W" represents a mod-36 alpha-numeric digit using the integers 1-9 and letters A-Z excluding O,Q,and V. For example, "N" represents a word-length of 23 and "P" represents a word-length of 24. The "yz" represents a hexadecimal value for the number of address locations divided by 16. For example, "04" represents 64 address locations.

In the logic symbol of figure 1, the "X" denotes the number of address lines. This value can be calculated by taking the log to the base 2 of the number of address locations. If the value returned is not an integer, round up. For example, for 64 address locations, "X" would be 6; for 80 address locations, "X" would be 7.

Performance data is listed below for two example sizes. To obtain data and a workstation installation (symbol and simulation model) for a specific size, contact the factory.

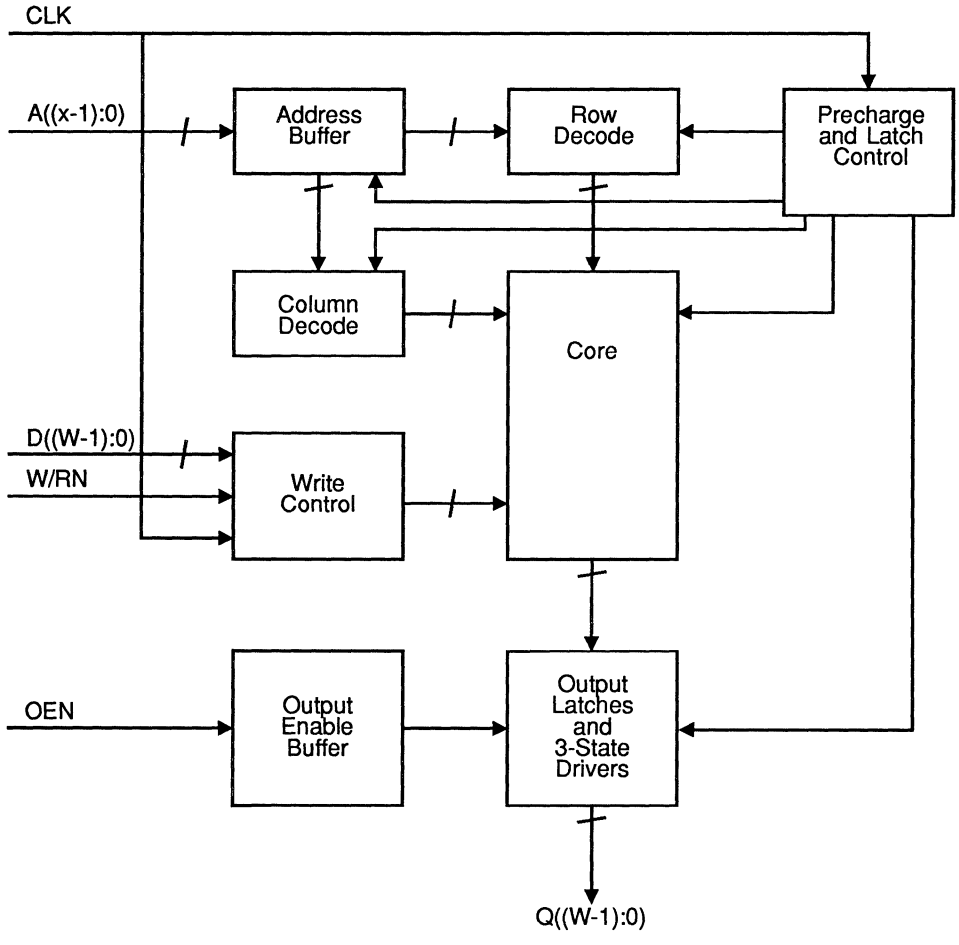


Figure 2: M X N RAM BLOCK DIAGRAM

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RASONwyz MxN Static RAM

Address and Word Size Range

Parameter	Minimum	Maximum	Increment
Address Inputs	5	10	1 (A0 is the LSB)
Word Size (Data Outputs)	1 bit	32 bits	1 bit
Address Locations (Words)	32	1024 (1k)	16
Total bits in a core. (Word size times address locations)	32	32,768(32k)	

Pin Description and Input Capacitance

Signal	Type	32 x 4	1k x 16	Signal Descriptions
Ai	Input	0.06pF	0.06pF	Address Inputs
CLK	Input	0.34pF	0.34pF	Clock Input
OEN	Input	0.40pF	0.40pF	3-State Output Control
Q (hi Z)	Output	0.07pF	0.07pF	Data Outputs
W/RN	Input	0.07pF	0.07pF	Write/Read Not Control
Di	Input	0.41pF	0.41pF	Data Inputs

Contact the factory to obtain capacitance information about MXN RAM

Area relative to a 2 Input Nand

32 x 4: 894

1k x 16: 30,160

Bolt Syntax

Q00 Q01 . . . Qw, .RASONwyz A0 A1 . . . Ax CLK DI00 DI01 . . . DIw OEN WRN;

Note: A0 is the LSB

AC Characteristics: t(CL)=tdx + Ktdx * CL

The data in the following examples are specified at 5.OV, Tj = 25 C, and typical process performance parameters. Performance at other operating points may be estimated by use of the Voltage, Process, and Temperature derating curves. Contact the factory to obtain the AC characteristics and input capacitance for different logical sizes of RAMs.

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RASONwyz MxN Static RAM

32 x 4

Characteristic	Symbol	tdx (ns)	ktdx (ns/pF)	t(0.33pF)(ns)
Min CLK Period Read	tclkr	8.94	2.06	9.62
Min CLK Period Write	tclkw	8.37		
Min CLK Width High	twch	3.01		
Min CLK Width Low During Read	twclr	5.92		
Max CLK Low to Q Delay	tpcq	5.92	2.06	6.60
Max OEN to Q Delay	toenq	0.50	2.06	1.18
Max OEN to Hi-Z Delay	toenz	0.21		
Min Address Setup Time**	tasu	3.05		
Min Address Hold Time**	tah	0.87		
Min W/RN High to Valid Write*	twvw	5.22		
Min Data in (Di) Stable to Valid Write*	tdvw	4.13		
Min CLK Low to Valid Write*	tcvw	5.36		
Min Data in (Di) Hold Time after Rising edge of CLK when W/RN is High*	tdh	1.61		
Min W/RN Hold Time After Read	twh	1.08		
Min Q Hold Time	tqh	1.35		

1k x 16

Characteristic	Symbol	tdx (ns)	ktdx (ns/pF)	t(0.33pF) (ns)
Min CLK Period Read	tclkr	10.76	2.05	11.44
Min CLK Period Write	tclkw	10.22		
Min CLK Width High	twch	4.63		
Min CLK Width Low During Read	twclr	6.13		
Max CLK Low to Q Delay	tpcq	6.13	2.05	6.81
Max OEN to Q Delay	toenq	0.58	2.05	1.26
Max OEN to Hi-Z Delay	toenz	0.28		
Min Address Setup Time**	tasu	3.23		
Min Address Hold Time**	tah	0.97		
Min W/RN High to Valid Write*	twvw	5.42		
Min Data in (Di) Stable to Valid Write*	tdvw	4.12		
Min CLK Low to Valid Write*	tcvw	5.59		
Min Data in (Di) Hold Time after Rising edge of CLK when W/RN is High*	tdh	1.78		
Min W/RN Hold Time After Read	twh	1.17		
Min Q Hold Time	tqh	1.40		

* If the W/RN line is high at the same time that the CLK line is low, all three timing terms twvw, tdvw, and tcvw must be met or else invalid data may be written into the RAM. A Read-Modify-Write cycle may be executed by leaving W/RN low until the read is accomplished, then meet the twvw, tdvw, and tcvw timing terms to accomplish a valid write. The Q outputs will change to the value that is written. After a write, the Data In (Di) pins must be held stable until after W/RN falls or CLK rises.

** If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it will not show corrupted data.

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RASONwyz MxN Static RAM

Power Dissipation:

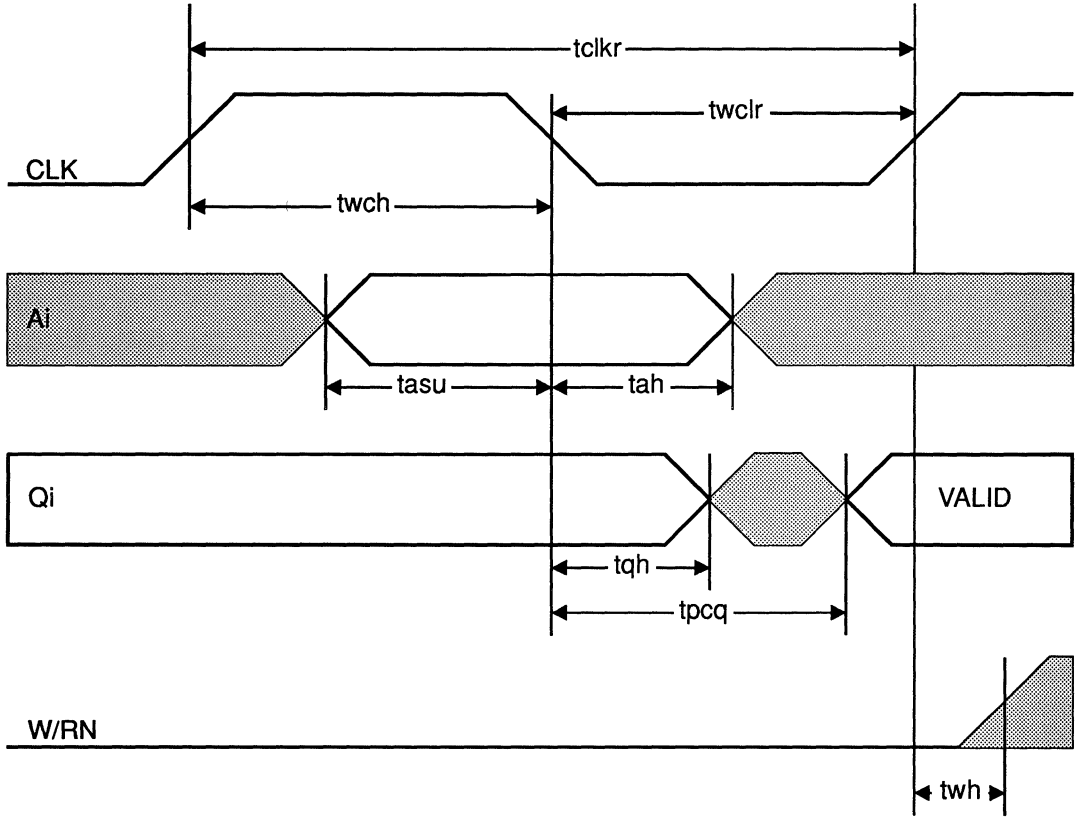
PARAMETER	32 x 4	1k x 16
Typical Co (Equivalent Power Dissipation Capacitance (pF))	44	271
Typical Static IDD Tj=85∞ C (ua)	4.38	43

(See data book for power dissipation notes.)

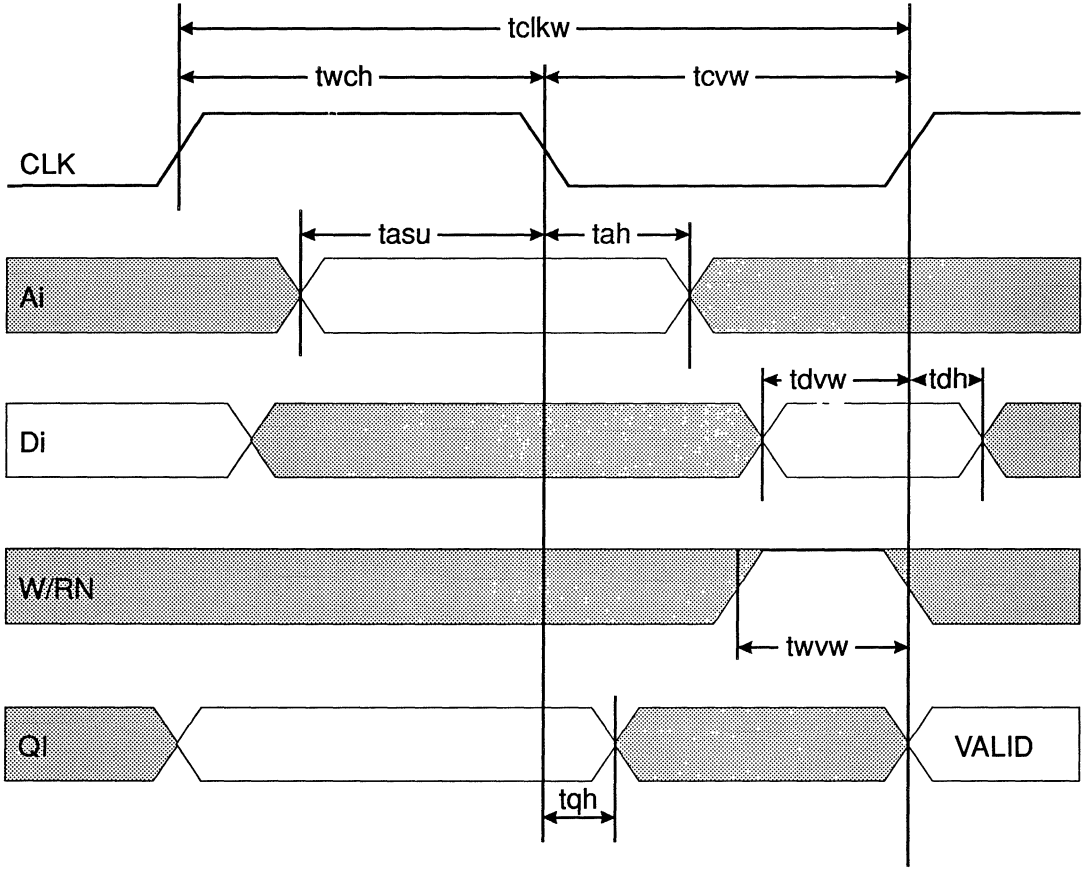
Testing Notes:

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. For a more detailed description of the testing of memory elements in IC's, refer to the RAM testing application notes.

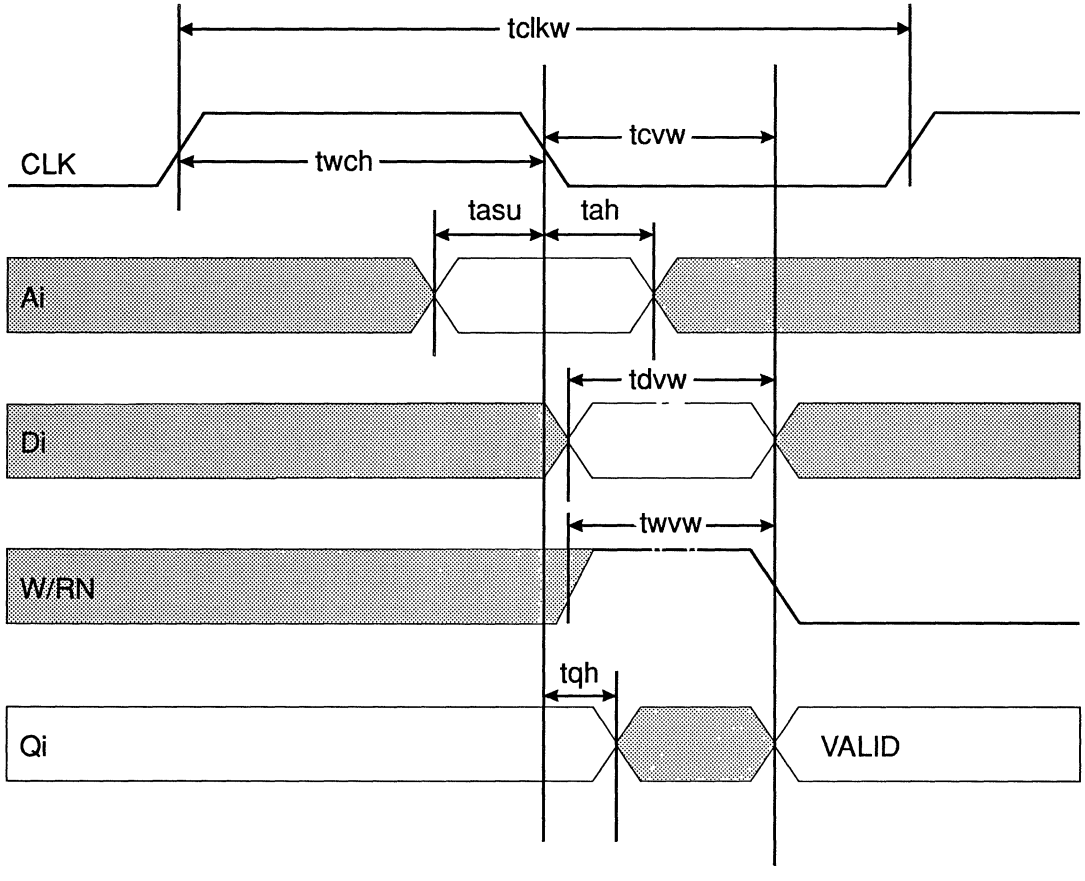
M X N RAM
Timing Diagram
Read Cycle



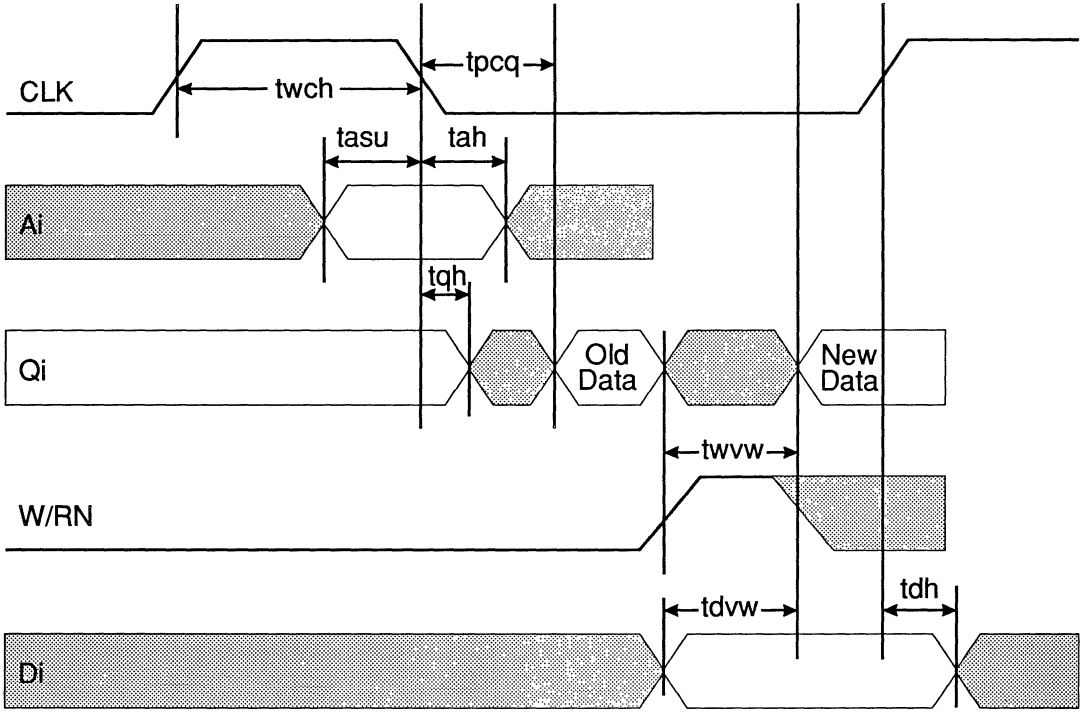
M X N RAM
Timing Diagram
Write Cycle 1 (See Notes 1 and 2)



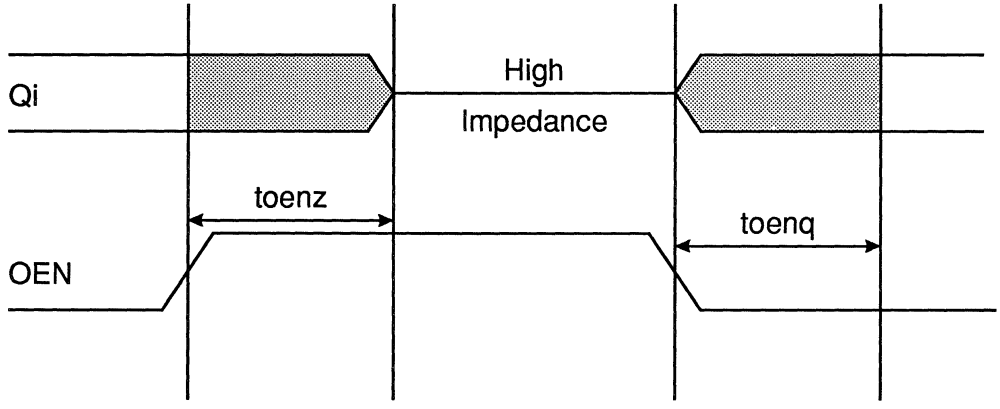
M X N RAM
Timing Diagram
Write Cycle 2 (See Notes 1 and 3)



M X N RAM
Timing Diagram
Read-Modify-Write Cycle (See Note 4)



3-State Control Timing



M X N RAM
Timing Diagram
Timing Diagram Notes

1. During a write cycle, the data that is written in becomes valid at the Q outputs as soon as the tcvw, tdvw, and twvw timing terms are met. The clock does not have to rise, and the W/RN signal does not have to fall first.
2. The data hold time in write cycle 1 is referenced to the rising edge of CLK when W/RN is held high.
3. The data hold time in write cycle 2 is referenced to the falling edge of W/RN and is equal to zero.
4. The data hold time in the Read-Modify-Write cycle has to be met only when W/RN is held high.

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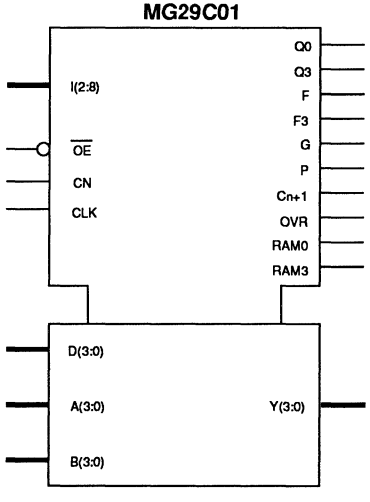
MG29C01 4-Bit Microprocessor

Features

- A high performance, low power CMOS megacell featuring functional compatibility with the industry standard 2901
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence.
- 4-Bit cascadable bit-slicing
- Eight function ALU including addition, two subtraction and five logic operations on two operands
- Microprogrammable with three groups of three bits each for ALU function, destination control and source operand
- Two address architecture provides independant access to two working registers
- Five source ports for data selection
- Four status flags including carry, zero, overflow and sign

LOGIC SYMBOL



Description

The MG29C01 is a high performance 4-bit cascadable microprocessor. It consists of a fast ALU, a 16-word by 4-bit two part RAM and the required decoding, multiplexing and shifting circuits. The microinstruction word consists of nine bits divided into three groups. Bits 0-2 select the ALU source operads. Bits 3-5 select the ALU function and bits 6-8 select the destination register.

The MG29C01 has four sources for providing the 12-bit address during each microinstruction. These four sources are as follows:

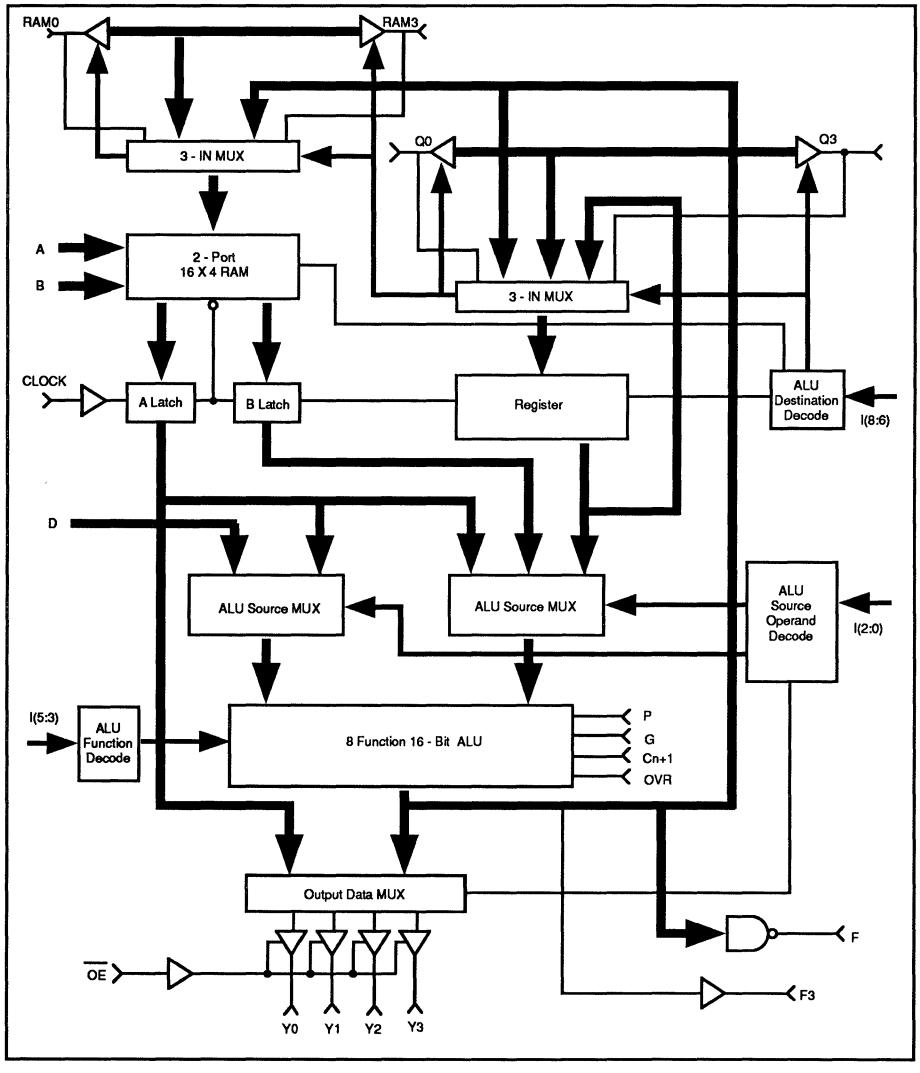
1. A direct external input.
2. A register/counter (R) which retains data loaded during an earlier microinstruction.
3. The last-in, first-out stack/file (F).
4. The address counter/register which usually increments the addresses.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG29C01 Block Diagram



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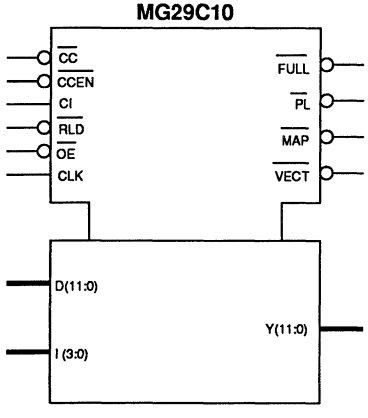
MG29C10 12-Bit Microprogram Controller/Sequencer

Features

- A high performance, low power CMOS megacell featuring functional compatibility with the industry standard 2910
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence.
- 12-Bit internal elements can address up to 4069 words of microcode
- 16 sequence control instructions, most are conditional on state of internal loop counter and/or external conditional input
- 12-Bit down counter is pre-settable for repeating instructions or counting loop iterations internally
- Four microprogram address sources including 9-level stack, microprogram counter, branch address bus, and internal holding register
- Internal decoder function controls output enables for three branch address devices

LOGIC SYMBOL



Description

The MG29C10 is a high performance 12-bit microprogram controller. It functions as an address sequencer for controlling the execution of microinstructions in microprogram memory. It also controls conditional branching to any microinstruction within its 4096 word range. There are nine levels of subroutine nesting with return linkage and looping capability provided by a last-in, first-out stack.

The MG29C10 has four sources for providing the 12-bit address during each microinstruction. These four sources are as follows:

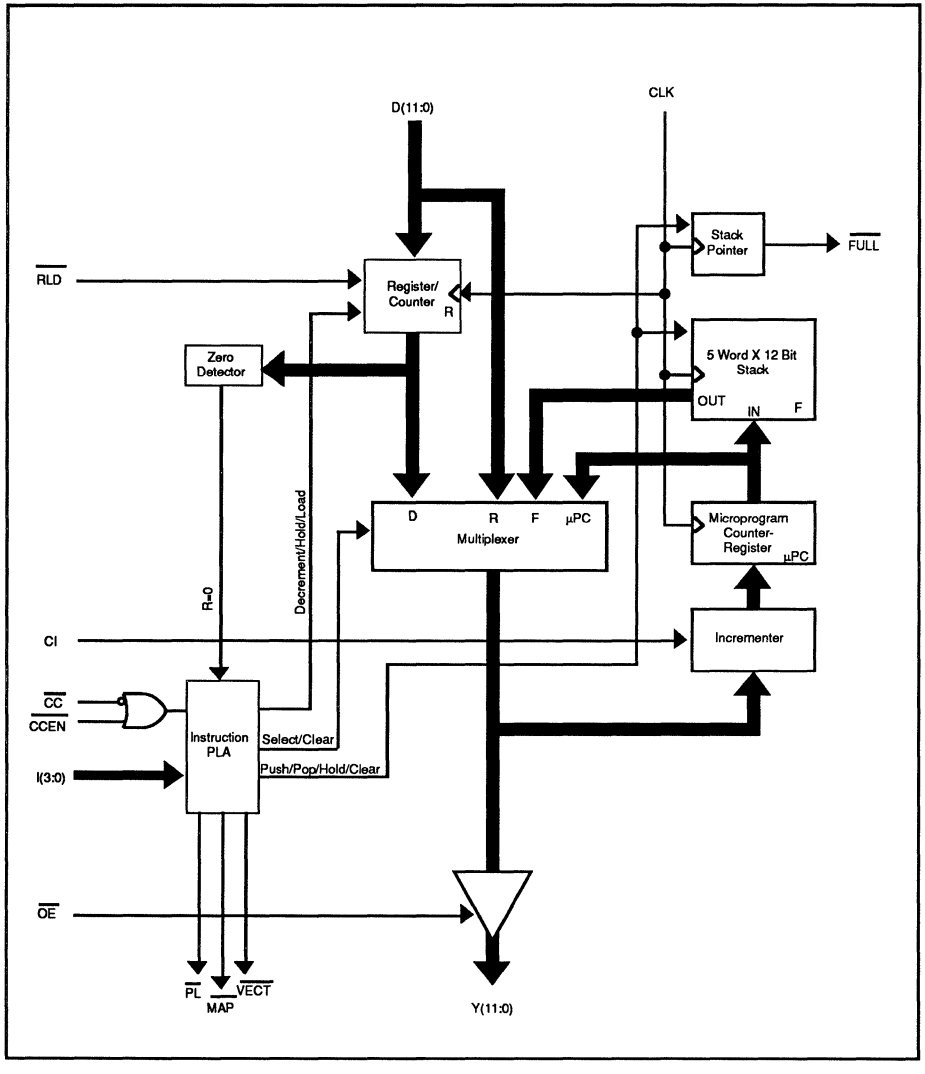
1. A direct external input.
2. A register/counter (R) which retains data loaded during an earlier microinstruction.
3. The last-in, first-out stack/file (F).
4. The address counter/register which usually increments the addresses.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG29C10 Block Diagram



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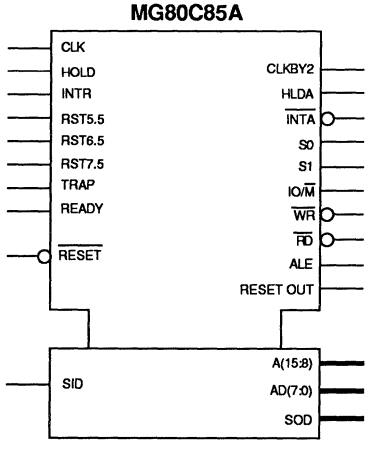
MG80C85 8-bit CMOS Microprocessor

Features

- A high performance low power CMOS megacell featuring functional compatibility with the industry standard 8085 and 8085A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence.
- Full support of extended instruction set, and standard 8080 and 8085/8085A instruction sets
- Runs over 10,000 CP/M® programs
- Direct addressing to 64K bytes
- Four Interrupt inputs (one non-maskable)

LOGIC SYMBOL



Description

The MG80C85 is an 8-bit microprocessor which features complete functional compatibility with industry standard 8085s and 8085As, and includes support for the special extended instruction set. Its design incorporates an on-board system controller, clock generator, serial I/O port and direct addressing capability to 64K bytes of memory. The MG80C85 utilizes a multiplexed data bus, with 16-bit addresses split between an 8-bit address bus and an 8-bit data bus.

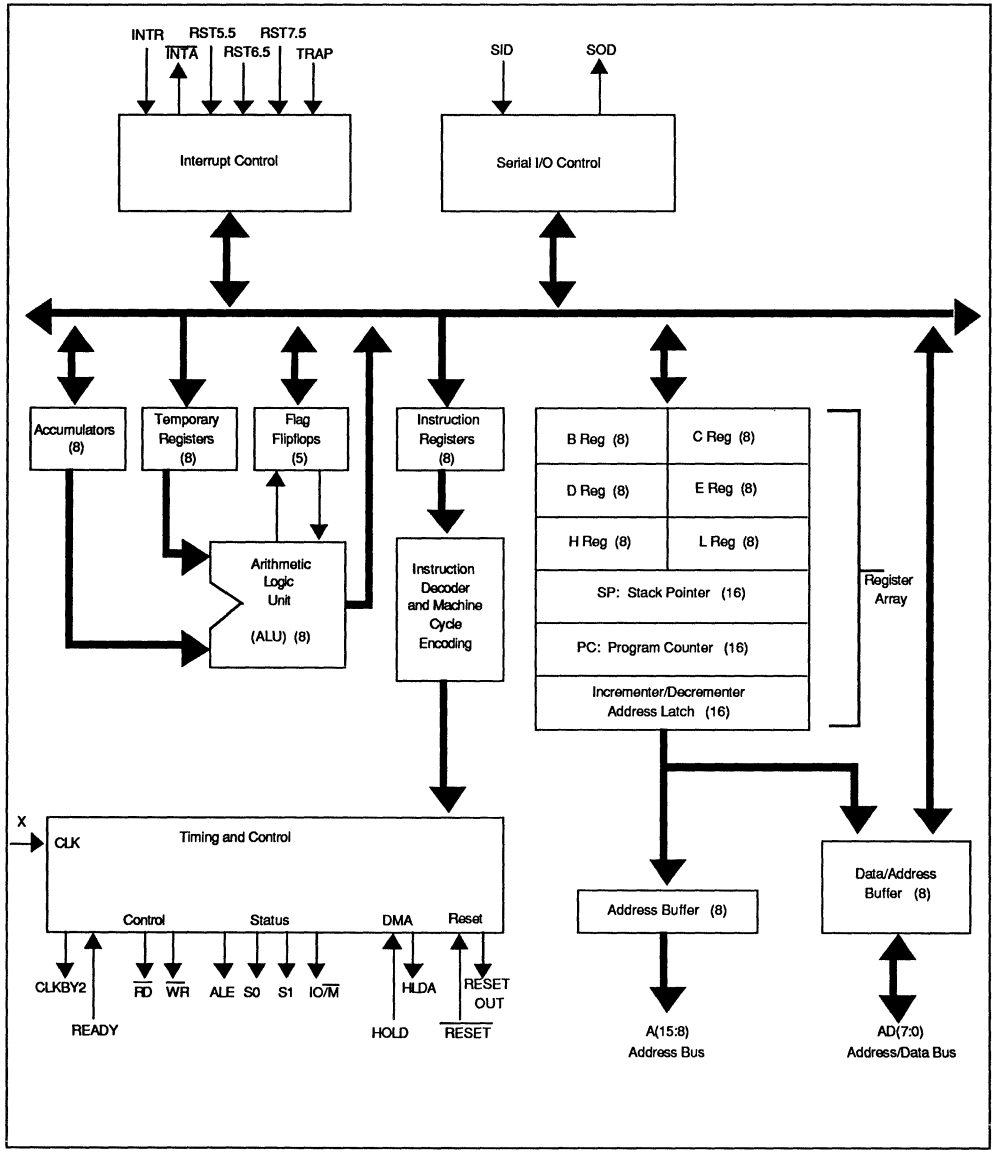
The MG80C85 is a macrocell building block for ASIC Logic design. Thus it can be used in conjunction with existing standard cell and gate array libraries to incorporate into original customer IC designs for lower overall system costs.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG80C85 BLOCK DIAGRAM



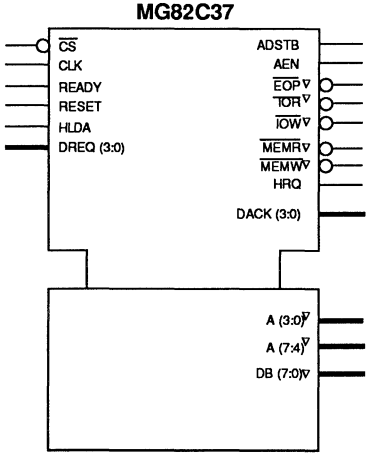
April, 1992

MG82C37A Programmable DMA Controller

Features

- A high performance low power CMOS megacell featuring functional compatibility with the industry standard 8237/8237A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence.
- Fully static
- Compatible with 8080/85, 8086/88, 80286/386 and 68000 µP families
- Four independent maskable DMA channels with autoinitialize capability
- Memory-to-memory transfer
- Fixed or rotating DMA request priority
- Independent polarity control for DREQ and DACK signals
- Address increment or decrement selection
- Cascadable to any number of channels

LOGIC SYMBOL



Description

The MG82C37A is a high performance, programmable Direct Memory Access (DMA) controller offering functional compatibility with the industry standard 8237/8237A. It features four channels, each independently programmable, and is cascadable to any number of channels. Each channel can be programmed to autoinitialize following DMA termination.

In addition, the MG82C37A supports both memory-to-memory transfer capability and memory block initialization, as well as a programmable transfer mode.

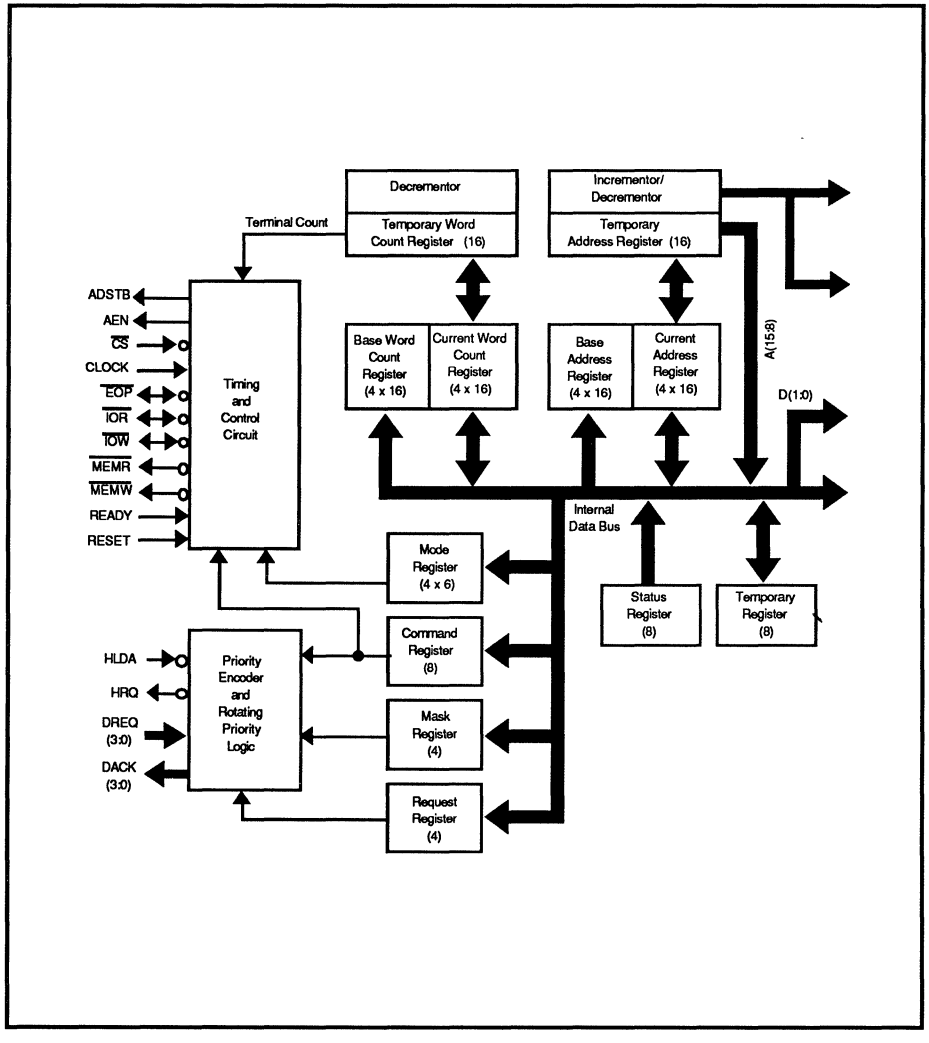
The MG82C37A is designed to improve system performance by allowing external devices to transfer data directly from the system memory. High speed and very low power consumption make it an ideal component for aerospace and defence applications. The low power consumption also makes it an attractive addition in portable systems or systems with low power standby modes.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG82C37A BLOCK DIAGRAM



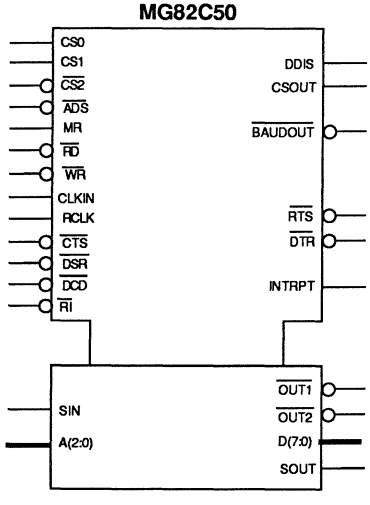
April, 1992

MG82C50A Asynchronous Communications Element

Features

- A high performance low power CMOS megacell featuring functional compatibility with the industry standard 8250
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence.
- Single megacell UART/BRG
- DC to 10MHz operation (DC to 625K baud)
- On chip baud rate generator 1 to 65535 Divisor generates the BAUDOUTN (16x) clock
- Prioritized interrupt mode
- Microprocessor bus oriented interface
- 80C86/80C88 compatible
- Modem interface
- Line break generation and detection
- Loopback mode
- Double buffered transmitter and receiver

LOGIC SYMBOL



Description

The MG82C50A Asynchronous Communications Element (ACE) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single megacell. The device supports data rate from DC to 625K baud (0-10MHz clock).

The ACE receiver circuitry converts start, data, stop and parity bits into a parallel data word. The transmitter circuitry converts a parallel data word into serial form and appends the start, parity and stop bits. The word length is programmable to 5, 6, 7 or 8 data bits. Stop bit selection provides a choice of 1, 1.5 or 2 stop bits.

The Baud Rate Generator divides the clock frequency by a divisor programmable from 1 to 2^{16}-1 to provide standard RS-232C baud rates. The BAUDOUT programmable clock output provides a buffered oscillator or a 16x (16 times the data rate) baud rate clock for general purpose system use.

To meet the system requirements of a CPU interfacing to an asynchronous channel, the modem control signals RTS, CTS, DSR, RI, DCD are provided.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both Standard Cells and Gate Arrays.

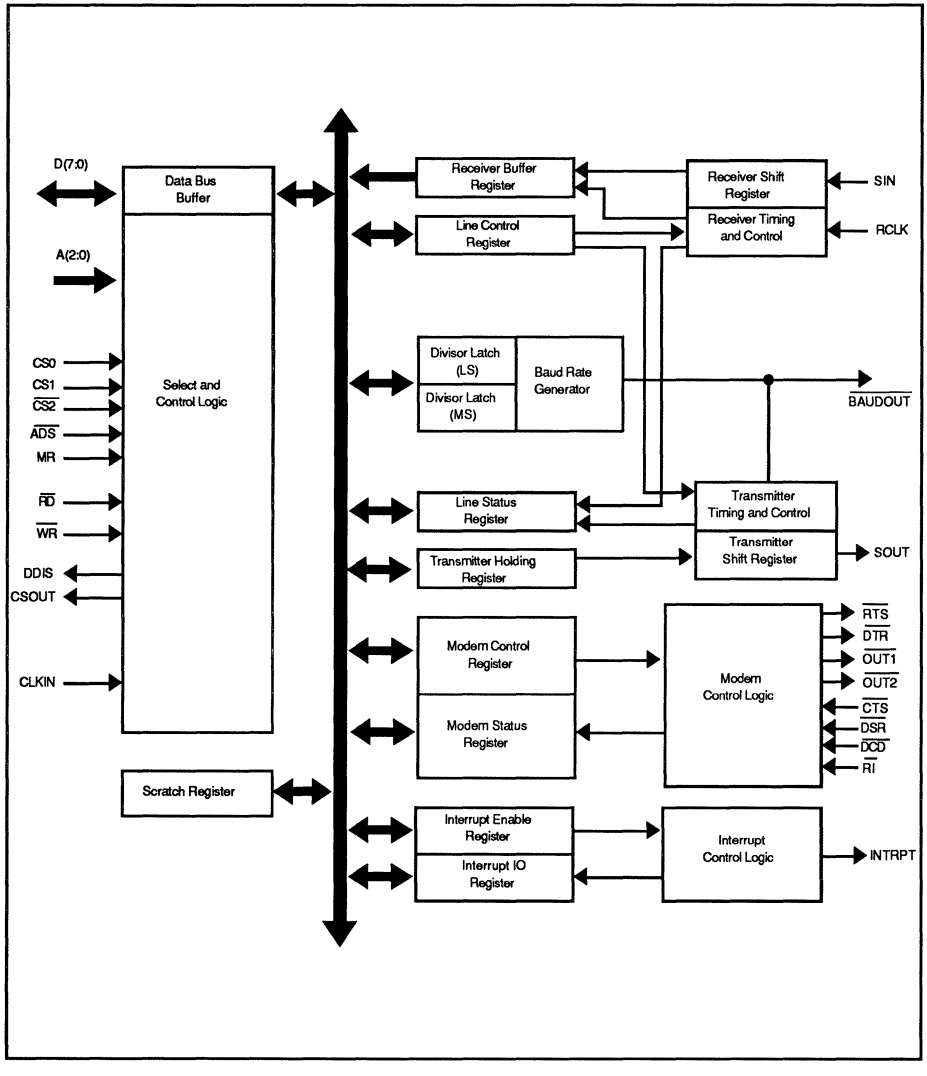
A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

April, 1992

MG82C50A Asynchronous Communications Element

MG82C50A BLOCK DIAGRAM



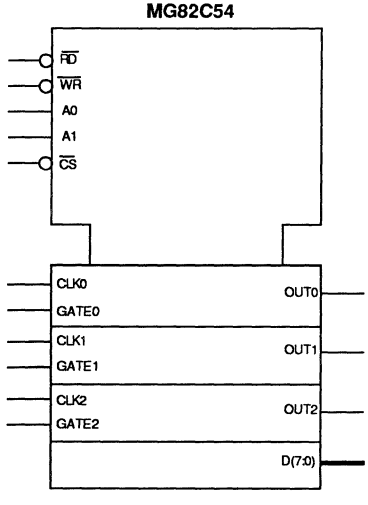
April, 1992

MG82C54 Programmable Interval Timer

Features

- A high performance low power megacell featuring functional compatibility with the industry standard 8254
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence.
- Supports 8086/88 and 80186/188 micro-processors
- Available in several Gould process technolgies
- Compatible with 8080/85 , 8086/88, 80286/386 and 68000 μP families
- Three independent 16 bit counters
- Six programmable counter modes
- Status read-back command
- Binary or BCD counting

LOGIC SYMBOL



Description

The MG82C54 is a counter/timer megacell that includes complete functional compatibility with the industry standard 8254. Designed for fast operation, it has three independently programmable 16 bit counters and six programmable counter modes. Counting can be performed in both binary and BCD formats. Speed will depend on what Gould process technology is chosen.

The MG82C54 offers a very flexible, hardware solution to the generation of accurate time delays in microprocessor systems. A general purpose, multi-timing element, it can be used to implement event counters, elapsed time indicators, waveform generators plus a host of other functions.

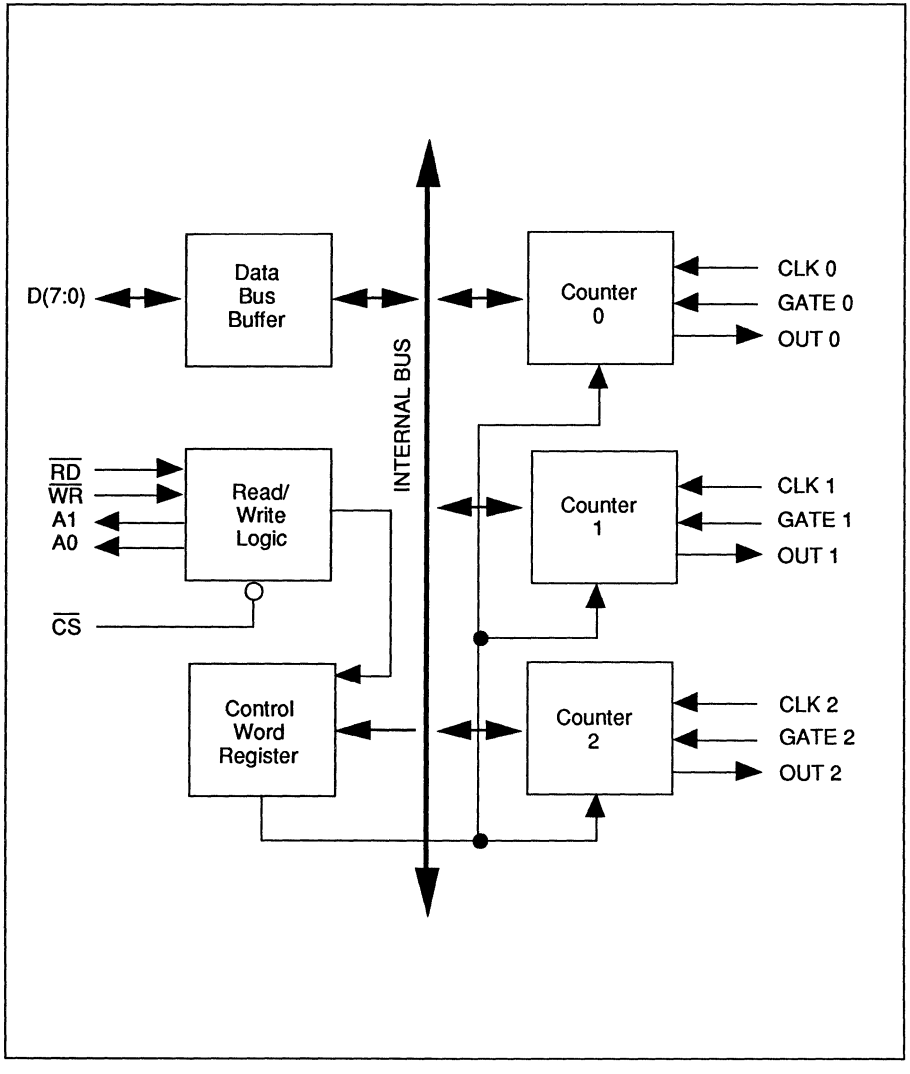
The low power consumption of the MG82C54 makes it ideally suited to portable systems or those with low power standby modes.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG82C54 BLOCK DIAGRAM



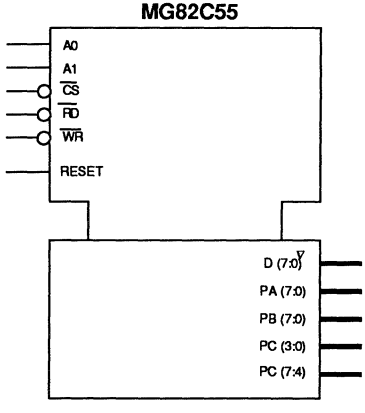
April, 1992

MG82C55A Programmable Peripheral Interface

Features

- A high performance low power CMOS megacell featuring functional compatibility with the industry standard 8255A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence.
- Supports 8086/8088 and 80186/188 microprocessors
- 24 programmable I/O pins
- Direct bit set/reset capability
- Bidirectional bus operation
- Enhanced control word read capability

LOGIC SYMBOL



Description

The MG82C55A Programmable Peripheral Interface is a high performance CMOS megacell offering functional compatibility with the industry standard 8255A. It includes 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation.

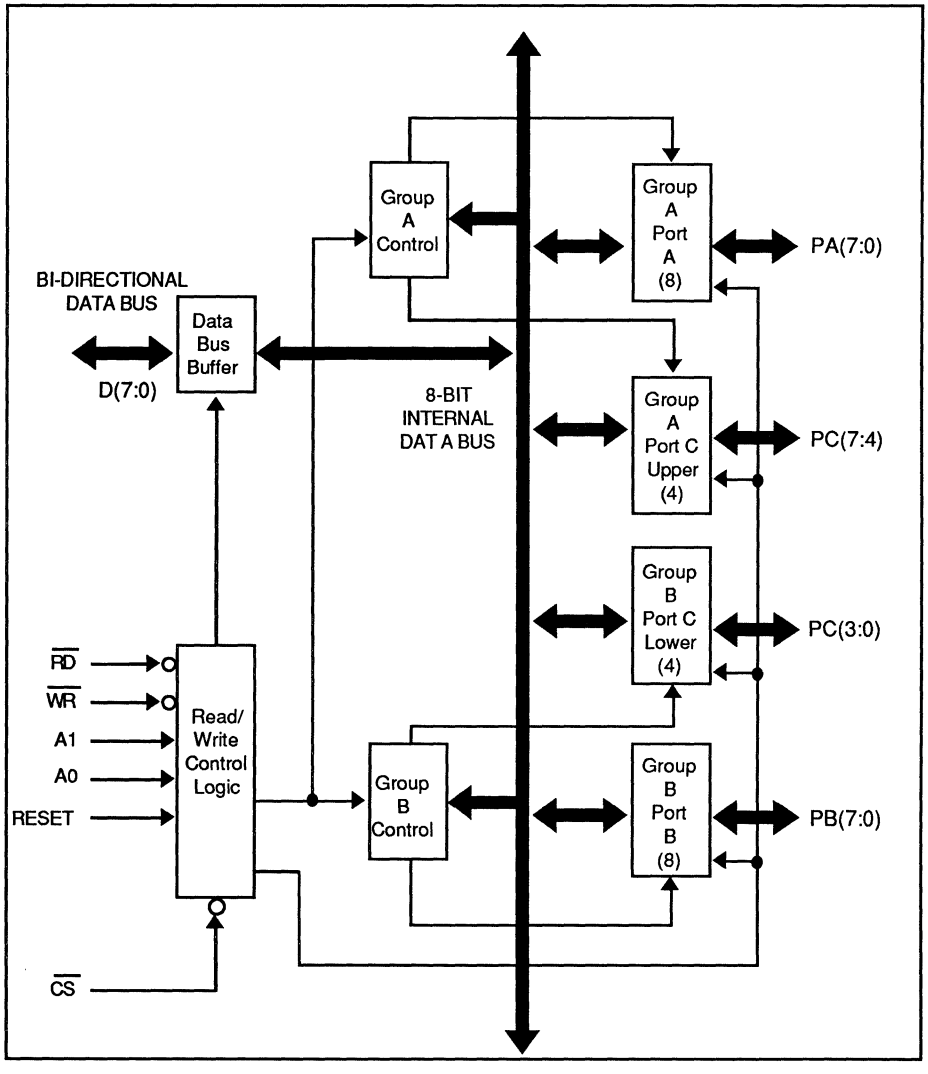
The MG82C55A is a general purpose programmable I/O megacell designed for use with several different microprocessors. Its high speed and high performance make it ideally suited for aerospace and defense applications, while the low power consumption suits it to portable systems and systems with low power standby modes.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG82C55A BLOCK DIAGRAM



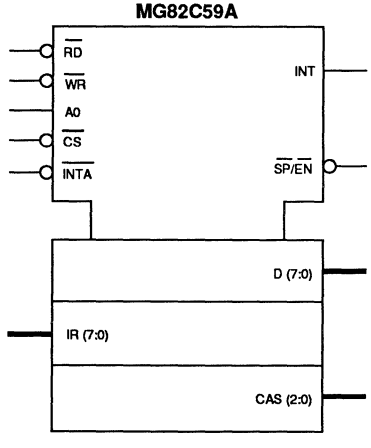
April, 1992

MG82C59A Programmable Interrupt Controller

Features

- A high performance low power megacell featuring functional compatibility with the industry standard 8259/8259A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence.
- Compatible with 8080/85, 8086/88, 80286/386 and 68000 family microprocessor systems
- Eight level priority controller
- Expandable to 64 levels
- Programmable interrupt modes, with each interrupt maskable
- Edge- or level-triggered interrupt request inputs
- Polling operation

LOGIC SYMBOL



Description

The MG82C59A is a high performance, completely programmable interrupt controller. It can process eight interrupt request inputs, assigning a priority level to each one, and is cascadable up to 64 interrupt requests. Individual interrupting sources are maskable. Its two modes of operation (Call and Vector) allow it to be used with virtually all 8000 and 80000 type processors, as well as with 68000 family microprocessors.

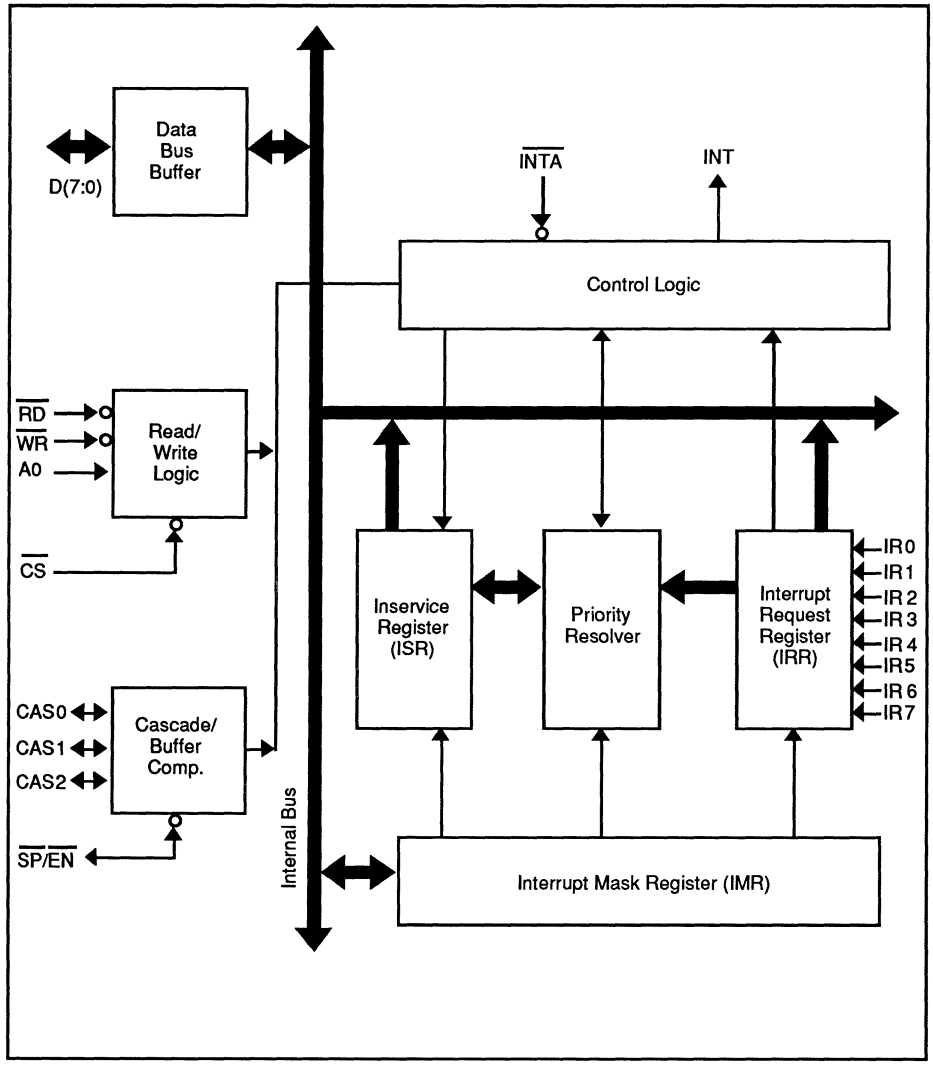
Featuring fully static, very high speed operation, the MG82C59A is designed to relieve the system CPU from polling in a multi-level priority interrupt system. Its high performance makes it ideally suited for aerospace and defense applications. Its very low power consumption makes it useful in portable systems and systems with low power standby modes.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG82C59 BLOCK DIAGRAM



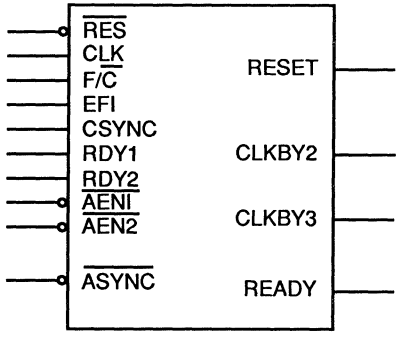
April, 1992

MG82C84A Clock Generator & Driver

Features

- A high performance low power CMOS megacell featuring functional compatibility with the industry standard 8284/8284A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence.
- Generates system clock for 80C86/88 microprocessors
- Provides Local READY and Multibus™ READY Synchronization
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with other 8284As
- Soft megacell technology allows customizing of function

LOGIC SYMBOL



Description

The MG82C84A is a high performance clock generator/driver for the 8088/86 type processors, offering functional compatibility with the industry standard 8284/8284A. It features a divide-by-three counter, complete Multibus™ READY synchronization, and reset logic.

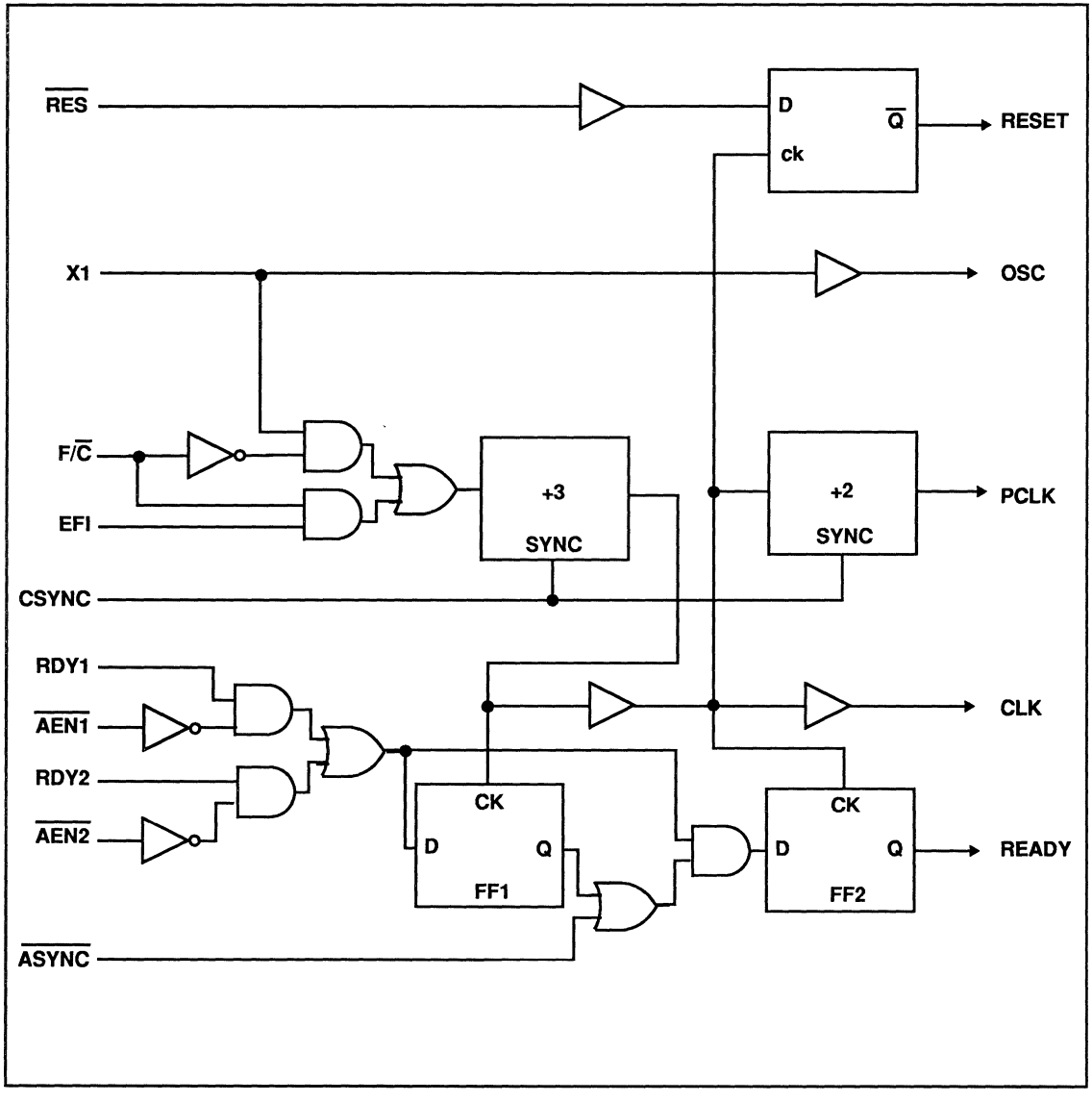
The MG82C84A is manufactured using CMOS technology. Its high speed makes it ideally suited for aerospace and defense applications. Its very low power consumption also makes it suitable for portable systems and systems with low power standby modes.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG82C84A BLOCK DIAGRAM



April, 1992

MGMC51 8-bit Core Microcontroller

Features

- A high performance low power CMOS megacell featuring functional compatibility with the industry standard 8051 family
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence.
- 8 Bit CMOS Microcomputer
- Fully Static Design
- Low Standby Current At Full Supply Voltage
- 0-40 MHz Operation
- 256 Bytes of on-chip scratchpad RAM
- 64K Bytes Program Address Space
- 64K Bytes Data Address Space
- Four 8-Bit Bidirectional Ports
- Three 16 Bit Timer/Counters
- Full Duplex Serial Channel With Hardware Address Decode
- Boolean Processor
- Six Source, Two Level Interrupt Capability
- In-circuit Emulation Mode
- Built In Power Management
- Access To SFR Bus
- Soft Megacell Technology Allows Use of Different Processes
- Can Be Customized to User Specification
- Useable with Additional Logic and Megacells
- Special Function and Control Pins Available
- Alternate Port Functions Available Through Separate Pins

General Description

The MGMC51 microcomputer is an 8-bit microcomputer which is compatible with the industry standard 80C31, 80C32, 80C51 and 80C52 microcomputer series. The MGMC51 contains four 8-bit bidirectional parallel ports, three timer/counters, and a serial port. These peripherals are supported by a six source, two level interrupt capability. There are 256 bytes of scratchpad RAM available.

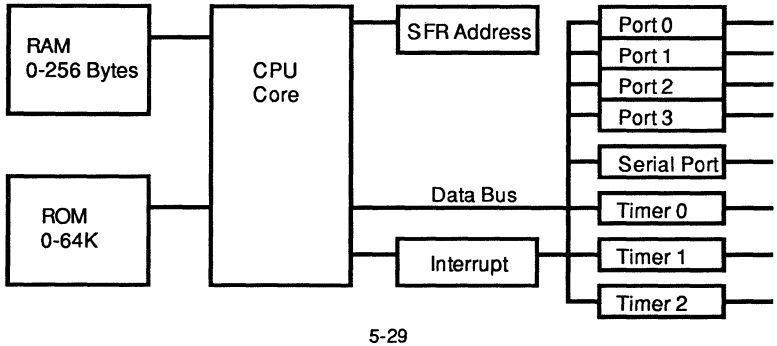
The MGMC51 is designed as a soft megacell in the ASIC standard library which allows it to be used with other logic and/or megacells. The soft megacell approach has advantages of design flexibilty and portability, and a path for future cost reduction by process migration. The MGMC51 can be customized for a specific use, and it can be built in gate array, standard cell, etc. The MGMC51 core allows access to pins and functions not available in the industry standard 8051.

The MGMC51 supports all of the advanced features of the 80C32 family, which include a power-on-reset status flag, an up/down counting mode in timer/counter 2, a hardware address decode and mask for serial interrupts, and a frame error detect flag.

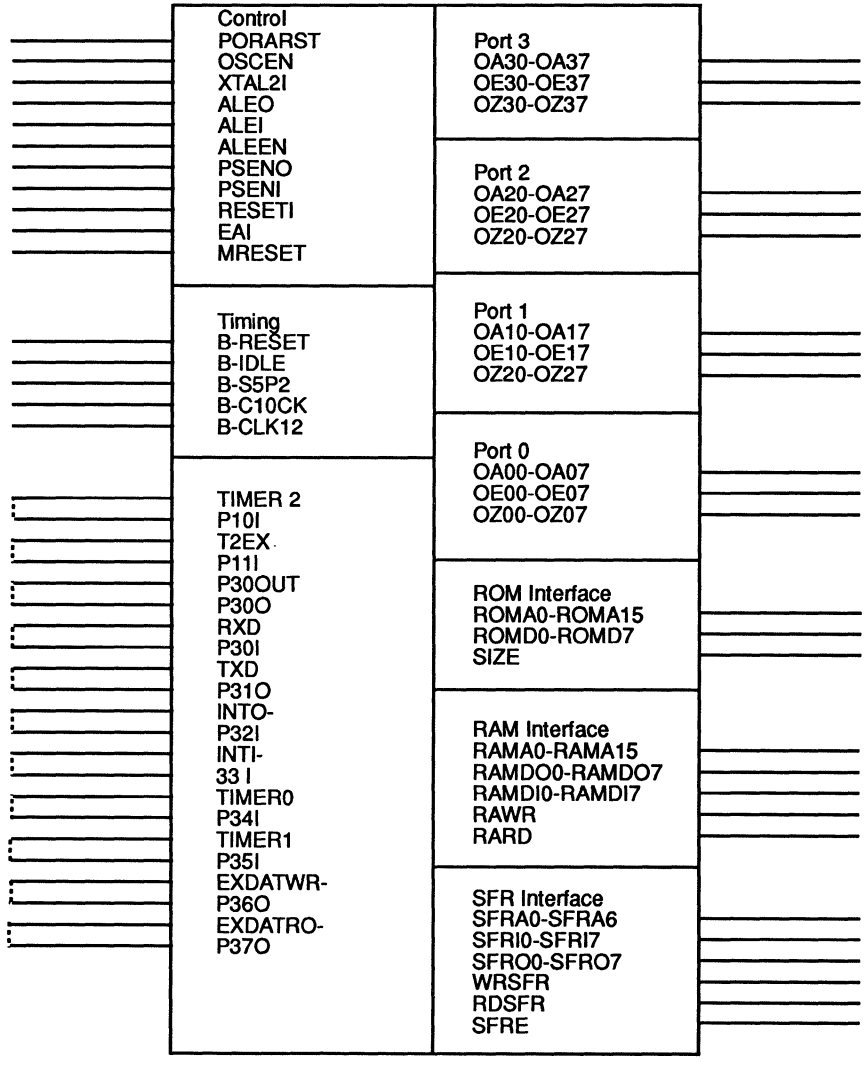
The MGMC51 microcomputer contains several power reduction modes. The idle mode turns off the processor clock, but allows for continued peripheral operation. The power down mode stops the crystal oscillator for minimum power consumption. Also, the external clock can be stopped at any time and in any state without affecting the processor. Unlike other versions, the fully static MGMC51 can be maintained at full supply voltage in the power down mode without excessive standby currents.

The MGMC51 provides access to the SFR address space. This feature allows the addition of external peripherals directly into the SFR address space, where they may be directly acted upon by the MGMC51 instruction set.

BLOCK DIAGRAM



ASIC CELL PINOUT



April, 1992

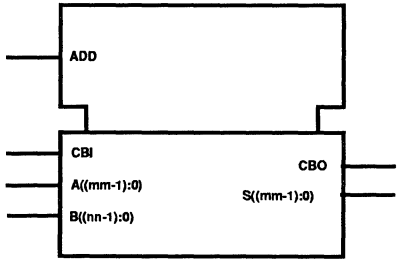
MGAmmnnAv mm by nn Adder

Features

- Schematic-based CMOS soft megacell synthesizer.
- Uses ASIC Standard Library for technology independence.
- High-performance, low-power, CMOS megacell.
- Adds or subtracts two's compliment inputs of size mm and nn bits.
- Sizes for inputs A and B are user definable.
- Uses fast look-ahead carry technique.
- Fully buffered inputs and outputs.

LOGIC SYMBOL

MGAmmnnAv



General Description

The MGAmmnnAv adder synthesizer builds fast mm bit by nn bit adder/subtracters which employs the look-ahead carry technique. The ADD input determines the function of the adder, the CBI input and the CBO output are the carry/borrow inputs and outputs respectively. Inputs A and B and output S are in the two's compliment format. The S output is the same size as the largest of inputs A or B.

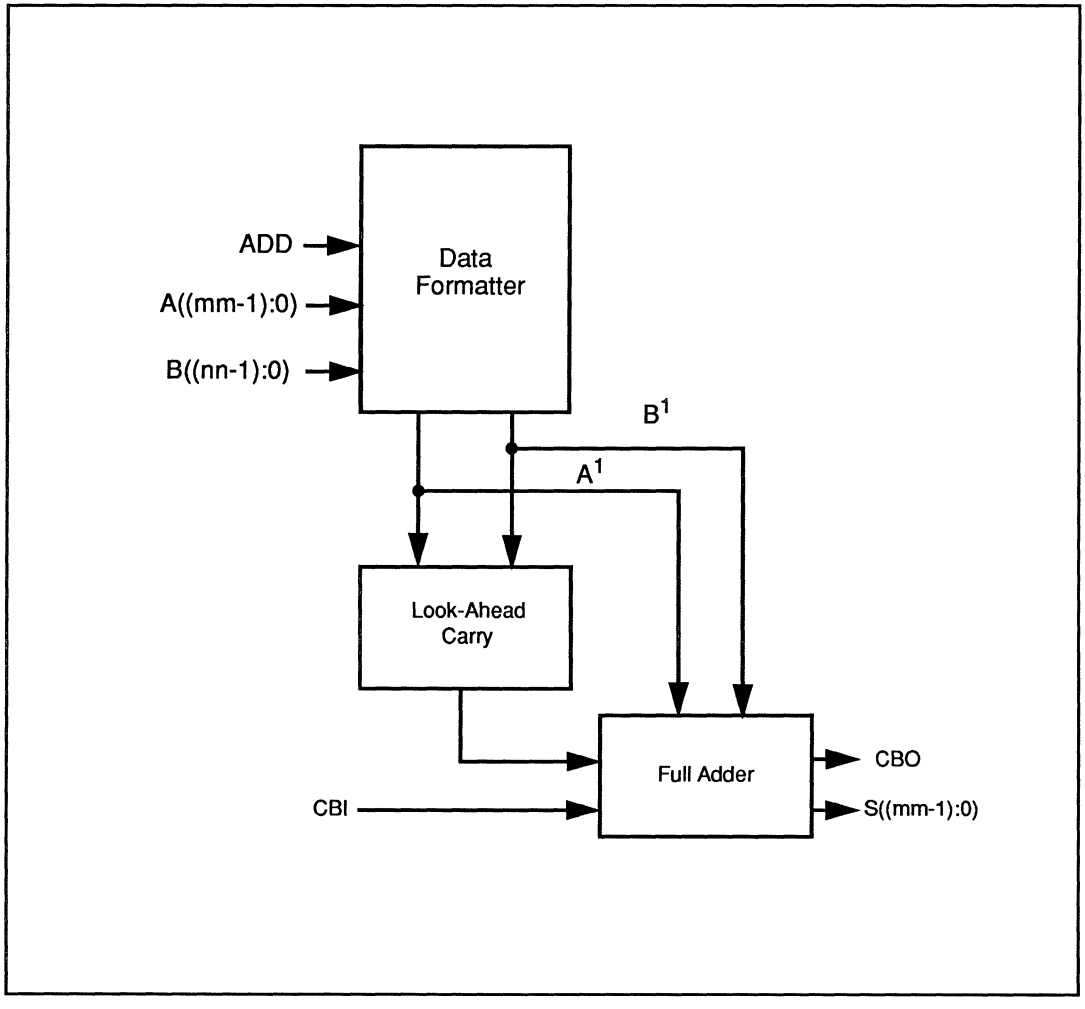
Inputs can be sized from two to 32 bits. In the name "mm" represents the A input size and "nn" represents the B input size, the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two, each implementation is given a different version number.

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for information on specific speeds and sizes or to have an adder built.

BLOCK DIAGRAM



April, 1992

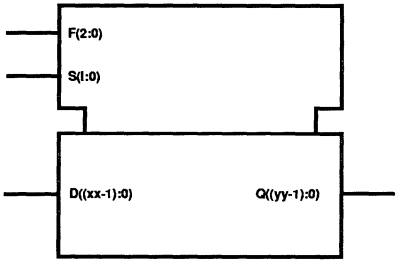
MGBxxyyAv Barrel Shifter

Features

- Schematic-based CMOS soft megacell synthesizer.
- Uses ASIC Standard Library for technology independence.
- High-performance, low-power, CMOS megacell.
- High-speed flash shift operations.
- Logical and arithmetic shifts available.
- Input data bus sizes and output window size are each user definable
- Full control of shifting output window position.
- Fully buffered inputs and outputs.

LOGIC SYMBOL

MGBxxyyAv



General Description

The MGBxxyyAv barrel shifter synthesizer builds barrel shifters which provide various shift functions for an input word size of "xx" bits. The shifts are performed completely through combinational logic which allows for very fast operations. All commonly used logical and arithmetic shift functions are available.

The type of shift function is controlled by the F inputs and can be:

1. Left or right circular shift.
2. Logic shift with zeros fill.
3. Logic shift with ones fill.
4. Arithmetic shift with sign extended.
5. Logic shift with D0 fill.

For a right circular shift, the S inputs select the number of bits to be shifted. For a left circular shift, the two's compliment of the number of bits to be shifted is placed on the S inputs. In the case of an 8-bit shifter, for example, an input select value of two (010) operating on the input 00001100 will generate the output 00000011 a right shift of two bits. If S has the value of seven (111) the output would become 00011000, which would represent a right shift of seven or a left shift of one.

The user has flexibility in specifying the word sizes of both the data input bus and output window. Within the name shown above, the "xx" represents the size of the data input word. The size of the S bus is dependent on the size of the data input word. The "zz" represents the size of the output window. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two, each implementation is given a different version number.

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both Standard Cells and Gate Arrays.

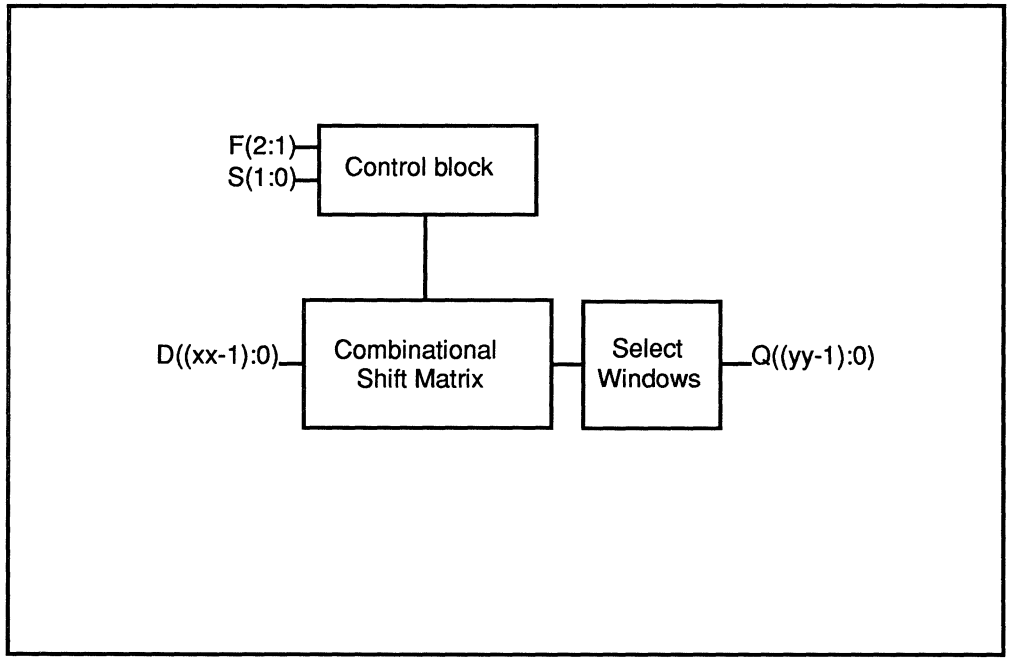
A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for information on specific speeds and sizes or to have a shifter built.

April, 1992

MGBxxyyAv Barrel Shifter

BLOCK DIAGRAM



April, 1992

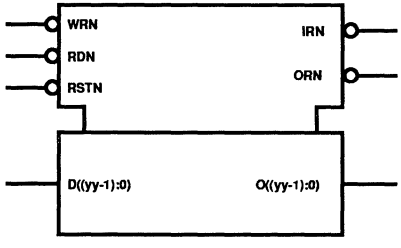
MGFxxyyAv x by y FIFO

Features

- Schematic-based CMOS soft megacell synthesizer.
- Uses ASIC Standard Library for technology independence.
- High-performance, low-power, CMOS megacell.
- Uses latch array architecture.
- Array sizes are definable, limited only by gate count.
- Fully buffer inputs and outputs.

LOGIC SYMBOL

MGFxxyyAv



General Description

The MGFxxyyAv FIFO (First In First Out) memory synthesizer builds latch based FIFO's of various sizes. FIFO's built with this synthesizer use the pointer algorithm to improve "fall through" time. These FIFO's have separate asynchronous read and write clocks. Flags include ORN (output ready not) which determines if the FIFO is empty and IRN (input ready not) which determines if the FIFO is full. Writes are inhibited if the FIFO is full and reads are inhibited if the FIFO is empty.

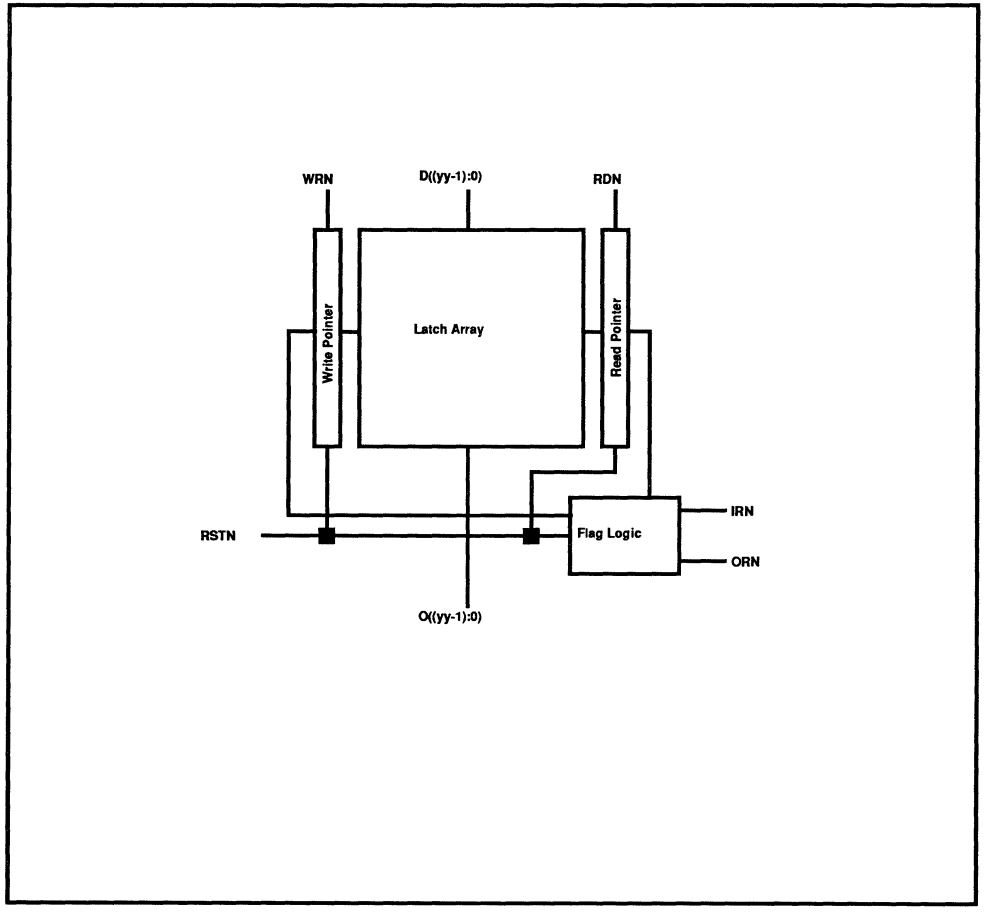
The "xxyy" in the name represents a four character sequence assigned to each FIFO configuration where "xx" represents the number of words and "yy" represents the number of bits per word. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two, each implementation is given a different version number.

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for information on specific speeds and sizes or to have a FIFO built.

BLOCK DIAGRAM



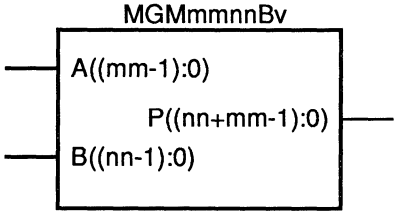
April, 1992

MGMmmnnBv m x n Multiplier

Features

- Schematic-based CMOS soft megacell synthesizer.
- Uses ASIC Standard Library for technology independence.
- High-performance, low-power, CMOS megacell.
- Two's complement multiplication.
- Input sizes are definable, up to 32-bits each.
- Uses a carry-save adder for high-speed operation.

LOGIC SYMBOL



General Description

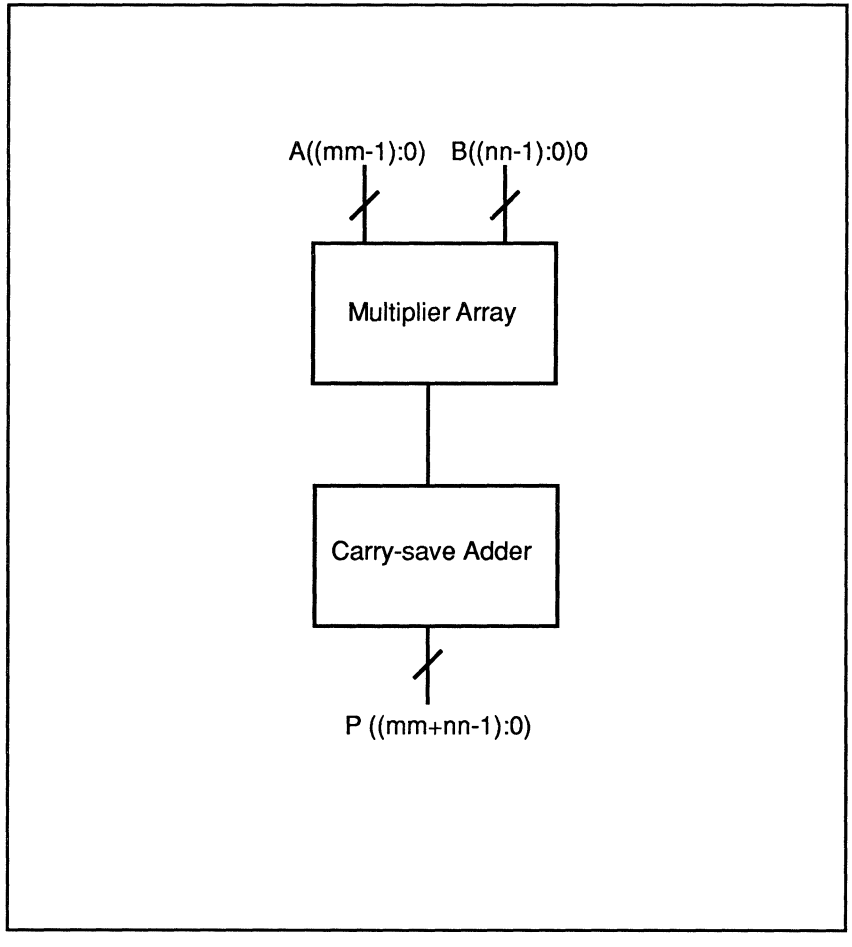
The MGMmmnnBv Multiplier logic synthesizer builds 2's compliment multipliers of various sizes. The "mmnn" represents a four character sequence assigned to each multiplier configuration where "mm" represents the number of A input bits and "nn" represents the number of B input bits. The number of products bits is equal to "mm" + "nn". The A, B inputs and the product are in two's compliment format. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two, each implementation is given a different version number.

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for information on specific speeds and sizes or to have a multiplier built.

BLOCK DIAGRAM



SECTION 6

SALES INFORMATION

Terms of Sale

April, 1992

1. ACCEPTANCE: THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. PAYMENT:

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. TAXES: Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or charges of any nature, imposed by any public authority (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. F.O.B. POINT: All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, United Parcel Service (UPS), Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. DELIVERY: Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any reprocurement costs, nor for delay or nondelivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. PATENTS: The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. INSPECTION: Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at the place of manufacture, such inspection shall be so conducted as to not interfere unreasonably with Seller's operations, and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY: The Seller warrants that the products to be delivered under this purchase order will be free from defects

in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. PRODUCTS NOT WARRANTED BY SELLER: The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES EXPRESSED, STATUTORY OR IMPLIED INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INFRINGEMENT AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products contact Seller.

10. PRICE ADJUSTMENTS: Seller's unit prices are based on certain material costs. These materials include, among other things, gold packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in the cost of other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. VARIATION IN QUANTITY: If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. CONSEQUENTIAL DAMAGES: In no event shall Seller be liable for special, incidental or consequential damages.

13. GENERAL:

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities domestic or foreign.

(g) Unless otherwise agreed in a writing signed by both Buyer and Seller, Seller shall retain title to and possession of all tooling of any kind (including but not limited to masks and pattern generator tapes) used in the production of products furnished hereunder.

(h) Buyer, by accepting these products, certifies that he will not export or re-export the products furnished hereunder unless he complies fully with all laws and regulations of the United States relating to such export or re-export, including but not limited to the Export Administration Act of 1979 and the Export Administration Regulations of the U.S. Department of Commerce.

(i) Seller shall own all copyrights in or relating to each product developed by Seller whether or not such product is developed under contract with a third party.

14. GOVERNMENT CONTRACT PROVISIONS: If Buyer's original purchase order indicates by contract number that it is placed under a government contract, only the following provisions of the current Federal Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be - i.e., "Contracting Officer" shall mean "Buyer", "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

52.202-1 Definitions; 52.232-11 Extras; 52.212-9 Variation in Quantity; 52.232-23 Assignment of Claims; 52.228-2 Additional Bond Security; 52.224-11 Certain Communist Areas; 52.222-4 Contract Work Hours and Safety Standards Act-Overtime Compensation; 52.222-20 Walsh-Healey Public Contracts Act, if this order exceeds $10,000; 52.222-26 Equal Opportunity; 52.203-1 Officials Not to Benefit; 52.203-5 Covenant Against Contingent Fees; 52.249-1 Termination for Convenience of the Government if this order does not exceed $500,000 (only to the extent that Buyer's contract is terminated for the convenience of the government); 52.246-1 Contractor Inspection Requirements; 52.247-1 Commercial Bills of Lading; 52.222-35 Affirmative Action Viet Nam Veterans if this order exceeds $10,000; 52.222-36 Affirmative Action Handicapped Workers, if this order exceeds $2,500; 52.222-1 Notice to the Government of Labor Disputes; 52.215-1 Examination of Records by Comptroller General; 52.220-3 Utilization of Labor Surplus Area Subcontracting Concerns.

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(205) 534-2384 (FAX)

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Scottsdale, AZ 85258
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(602) 451-0172 (FAX)

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3350 Scott Blvd., Bldg. 10
Santa Clara, CA 95054
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(408) 988-2079 (FAX)

Centaur Corporation
18006 Skypark Circle
Suite 106
Irvine, CA 92714
(714) 261-2905
(714) 261-2123 (FAX)

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9085 E. Mineral Circle
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(303) 649-9719 (FAX)

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Altamonte Springs, FL 32701
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(407) 339-1966 (FAX)

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Emerging Technology Sales
10451 W. Garverdale Court,
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Boise, ID 83704
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Control Sales, Inc.
2330 Brickvale Drive
Elk Grove Village, IL 60007
(708) 595-2110
(708) 595-9592 (FAX)

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R.F. Welch Co., Inc.
3349 Southgate Court, S.W.
Cedar Rapids, IA 52404
(319) 362-6824
(319) 362-7734 (FAX)

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Midtec Assoc. Inc.
11900 West 87th St. Parkway
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(913) 541-1729 (FAX)

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Waltham, MA 02154
(617) 891-4600
(617) 899-0393 (FAX)

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J.L. Montgomery Assoc., Inc.
33405 W. 12 Mile Rd.,Suite
149
P.O. Box 2726
Farmington Hills, MI 48333-
2726
(313) 489-0099
(313) 489-0189 (FAX)

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Vector Component Sales, Inc.
3101 Old Hiway 8, Suite 202
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(612) 631-1329 (FAX)

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265 Sunrise Highway
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(516) 536-4242
(516) 536-9638 (FAX)

T-Squared Electronics Co., Inc.
6443 Ridings Road
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(315) 463-0355 (FAX)

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4445 Alpha Road, Suite 109
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Micro Sales, Inc.
2122 112th Ave. N.E., Suite B
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(206) 451-0568
(206) 453-0092 (FAX)

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Electronic Technical Sales, Inc.
2A19 Nogal Avenue
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J-Squared Technologies, Inc.
300 March Road, Suite 401
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SABRE ADVANCED MICRO-ELECTRONICS LTD
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