American Microsystems, Inc.

Mixed-Signal Data Book

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AMI SEMICONDUCTORS

Mixed-Signal Data Book

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Printed in U.S.A.

AMI SEMICONDUCTORS

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GENERAL INTRODUCTION

AMI Semiconductors - Making ASICs Easier for More Than a Quarter Century

American Microsystems, Inc. (AMI) pioneered the development of the world's first custom MOS ICs in 1966. With more experience than any other ASIC vendor, you can be assured that when you bring your ASIC development project to AMI, you are working with a dependable team that has the depth of experience to provide you with an optimum solution, on time and on budget.

The vision shared by all employees at AMI is to delight customers through microsystem solutions. AMI strives to realize this vision by offering a range of products and services aimed at improving cycle time, reducing overall design cost, achieving world-class reliability, and designing to customer need. AMI provides a full range of gate array, standard cell, and mixed-signal ASICs, mixed-signal and digital ASIC design software and services, and modular foundry services. AMI's Standard Products division offers mask-programmable ROMs and programmable electrically erasable logic devices (PEELs™). AMI's Application-Specific Integrated Systems (ASIS®) division specializes in contract manufacturing solutions.

AMI is a California corporation whose headquarters and ASIC design and manufacturing operations are located in a 317,000 square foot facility in Pocatello, Idaho; the Standard Products and ASIS divisions are also headquartered in Pocatello. AMI has a software R&D facility in Twain Harte, California, and owns a subsidiary called AMI (Philippines), Inc., located in a 45,000 square foot facility in Manila, Philippines, for test and assembly of AMI's products.

Markets

- Communications
- Computers
- Military
- Automotive
- Consumer
- Industrial

Sales and Distribution

- Six full-service sales and technical support offices located in key markets throughout North America
- Six additional satellite offices in secondary markets
- Two technical service centers, located in San Jose and Tokyo, which offer customers a full range of digital ASIC design resources and services
- Twenty-one manufacturers' sales representatives comprising more than 110 outside salespeople in 30 locations throughout North America
- Four major and several regional distributors for AMI's standard product offerings, comprising more than 100 locations nationwide
- European sales headquarters in Bristol, England, supplemented by design houses and distributors in key markets

General Introduction

Products

ASICs

- Mixed-signal, standard cell, and gate array ASICs. AMI's ASIC products are supported with a library of more than 500 digital cells and megacells, designed in the company's 1.0 and 1.25 micron CMOS process technologies and compatible with all popular industry-standard CAE environments.

PLDs

- CMOS PEEL™ (Programmable Electrically Erasable Logic) and PEEL Array devices. Built with an advanced CMOS EEPROM process and offering operating speeds as fast as 7.5 nanoseconds, AMI's high performance PEEL products bring the benefits of reprogrammability and low power consumption to logic configurations in high density printed circuit boards.

Mask Programmable ROMs (read-only memories)

- AMI's ROMs offer capacities from 16 megabits to 16 kilobits, response times as fast as 90 nanoseconds, and require only a 3 to 5 volt power supply. Design flexibility is afforded by multiple user-definable control pins and a variety of packaging options.

ASIC Design Software

- Mixed-Signal Design Solution (MSDS)™ software—the first mixed-signal design package that enables ASIC designers to automatically generate customized analog behavioral models at their own workstations.
- ACCESS Design Tools™ software—for optimizing ASIC design at customer sites. AMI's ACCESS product line includes Design Analyzer and Pattern Analyzer software, as well as the company's NETRANS™ FPGA-to-ASIC conversion software for use at customer sites.

System-Level Solutions (ASIS® Div.)

- Contract design and manufacturing—Thru-Hole Technology (THT), Surface-Mount Technology (SMT), Hybrids, and Multichip Modules. PC Cards (JEIDA 4.0/4.1, PCMCIA 1.0/2.0).

Services

PLD/ASIC Conversions

- NETRANS/PALTRANS™—the first fully automated PLD-to-ASIC conversion service offered by an ASIC vendor.
- NETRANSplus™—the first fully automated ASIC-to-FPGA conversion service offered by an ASIC vendor to provide quick-turn prototyping.

ASIC Test

- NETSCAN™—AMI's automated ASIC test-pattern generator software for increasing fault coverage.
- NETTAG™—AMI's automated JTAG insertion tool for boundary scan testing.

ASIC Design

- Design Analyzer™, Gate Gobbler™, Five-Corner Logic Simulator™, and Accolade™ cell-compiler software—for optimizing customers' ASIC design and swiftly tailoring logic functions to customers' specific requirements.

Foundry/Manufacturing

- Advanced CMOS technology—brings low power consumption, high noise immunity, and high circuit densities to digital and analog/digital ASICs.
- Feature sizes as small as 1.0 micron (drawn).
- Process modularity—enables automated fabrication steps to be variously combined in ways tailored to meet the specific manufacturing requirements of analog, digital and mixed-signal devices.
- "Flexible factory"—provides a diversity of fabrication processes and schedule options to meet customer requirements.
- Low cost plastic assembly—pin counts up to 208 QFP.
- Wafer gold bumping—available as a foundry service or as an extension of AMI's ASIC services to support TAB, flip-chip, or chip-on-chip applications.

Corporate Headquarters

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Clock Drivers

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ABX 3.5 micron CMOS Standard Cells

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Power Cells

SECTION 3
MSDS DESCRIPTION

Mixed-Signal Design Solution

AMI's Mixed-Signal Design Solution (MSDS) consists of a suite of software tools for use both on customers' design workstations and at AMI. MSDS is the most comprehensive mixed-signal design system to deliver a total design-to-manufacturing solution for the swift creation of cost-effective, analog/digital ASICs with first-time silicon success. The system incorporates three capabilities critical to the cost-effective development of mixed-signal ASICs: 1) automatic generation of custom analog cells and behavioral level analog simulation models; 2) simulation software that enables customers to perform behavioral level, concurrent analog/digital simulations of their designs early in the ASIC design cycle; and 3) mixed-signal test generation. Used in tandem with AMI's mixed-signal fabrication processes, MSDS offers a comprehensive design-to-manufacturing solution to the challenge of complex mixed-signal ASIC design.

MSDS: Overall Capabilities

MSDS is specifically aimed at driving the mixed-signal design process "down the digital path." That means keeping time to market and development costs for mixed analog/digital ASICs equivalent to those for complex all-digital ASIC designs – or holding down development time and significantly reducing costs to those required to produce a full custom chip. The design system achieves these goals by providing the following capabilities.

Automatic capture of specifications and generation of pre-layout simulation models for custom analog functions on MSDS users' own workstations

This capability streamlines the complex analog specification task and reduces the miscommunications that frequently occur between customers and ASIC vendors over analog performance requirements. It also enables MSDS users to swiftly incorporate into their designs complex analog functions that are optimally suited to the target system. Using the MSDS-generated analog behavioral models and AMI's digital cell library, designers then can simulate a complete analog/digital ASIC – including the critical interface between analog and digital circuitry – with MSDS simulation software.

Expert analog design tools

MSDS software enables users who are unfamiliar with analog integrated circuit design to detect and eliminate design errors early in the design cycle. This software includes AMI's proprietary Design Critiquer, which identifies combinations of functional blocks that can create design problems.

Design for testability features

AMI's proprietary MSTEST software captures customers' performance requirements for each analog block, and advises users early in the design process if a function cannot be tested as specified. MSTEST uses AMI's unique design-for-test strategies which permit high-visibility of the circuit for easy evaluation during the electronic design stage. Users thus can make any needed performance/testability trade-offs before committing their designs to silicon, which spares them costly changes later in the ASIC development cycle.

ASIC development tasks occur at the MSDS customer site. Because analog performance specification, analog model generation, analog and digital design capture, and chip-level simulation of mixed-signal ASICs are accomplished on customers' own workstations, users achieve total control over the design of their mixed-signal circuits. With MSDS, the actual layout and fabrication of a mixed-signal ASIC does not begin until AMI receives the ASIC developers' design database and simulation files. The results include fewer design iterations, reduced ASIC development cycles, and lower ASIC vendor charges.

Automated generation at AMI of analog building blocks that are customized to target applications

This MSDS capability avoids the lengthy ASIC design cycles incurred by manually designing custom analog functions. It also eliminates the disadvantages associated with using standard "fixed" analog cells, which typically cannot achieve the exact performance parameters required for each unique analog application.

Automatic test program generation from customer-supplied simulation files

MSDS customers are spared time-consuming involvement in the development of manufacturing tests for mixed-signal ASICs. This process occurs at AMI as part of MSTEST and shaves months off development times.

MSDS Components - Installed at the Customer Site

MSDS software runs on Apollo workstations. It includes AMI's extensive digital standard cell library, comprised of more than 180 cells ranging from simple inverters to RAMs and ROMs. MSDS supports industry standard schematic capture software from Mentor Graphics, Inc., which is integrated with the other MSDS programs installed on customer' workstations under the MSDS X-Windows compliant graphical user interface. The programs comprise the following:

Analog Model Builder (AMB)

This AMI-developed application captures users' analog performance requirements and analog cell specifications - such as slew rate, offset voltage, and bandwidth – for a variety of analog functions of subcircuits. The AMB accepts two types of specification: those for analog blocks that already exist in AMI's configurable cell library, and those for user-defined functions required by the customer. The software includes AMI's specification advisor, which advises users if their desired analog cell specification cannot be realized in silicon. It also provides area estimates for specified cells.

For existing analog model builder cells, the software outputs a behavioral level model (BLM) with cell specifications inserted, and a schematic capture symbol with needed properties attached for creating the analog/digital design database used to simulate a complete mixed-signal ASIC. For user-defined functions, the AMB creates the schematic capture symbol and AMI creates the BLM, which is forwarded to the customer.

Additional AMB outputs include data sheets and specification files that drive the parameterized analog building block generators (PABBGs) at AMI, as well as performance parameters used by MSTEST to create test programs for mixed-signal ASICs.

Design Critiquer

AMI's Design Critiquer is an expert system tool that reviews a mixed-signal design database and pinpoints combinations of functional blocks that can create design flaws.

MSDS customers can use the Design Critiquer at the schematic stage to identify and eliminate problems rapidly, before errors compound themselves as the design task proceeds. Because the software is rule-based, it can follow a chain of reasoning to identify a problem.

Types of problems identified by the Design Critiquer include power supply bussing problems, mixed-signal schematic construction errors, and insufficient drive and sense levels, among others.

Mixed-Signal Simulator

The mixed-signal simulation software integrated with MSDS is Saber/CADAT™, jointly developed by Analogy, Inc., and Racal-Redac, Inc. Saber/CADAT fully simulates both the analog and the digital portions of a mixed-signal ASIC, integrating and analyzing both functions simultaneously.

The simulator offers a number of advanced capabilities, including the simulation of "feedback loops" containing both analog and digital components (such as an analog-to-digital converter). Designers thus can observe circuit performance in "real world" situations.

Using their MSDS-generated design database and MSDS analog behavioral level models, MSDS customers can employ Saber/CADAT to simulate complete mixed-signal ASIC designs before committing them to silicon. Once they are confident that their designs will perform as specified, their simulation files and design database serve as input for physical chip construction and MSTEST test program generation at AMI.

Saber™ and Analogy® are registered trademarks of Analogy, Inc. CADAT® is a registered trademark of Racal-Redac.

MSDS Components - Installed at AMI

Parameterized Analog Building Block Generators (PABBGs)

At the heart of the MSDS system is AMI's suite of proprietary parameterized analog building block generators (PABBGs). Each PABBG is a specialized system that captures in software the electrical and physical design expertise needed to create an analog block from the specification provided by the analog model builder (AMB).

A key feature of each PABBG is that it is parameterized. AMI's experience has shown that a library of "fixed" analog cells is not robust enough to meet the area and performance demands of every application without substantial cost penalties. In fact, because each analog function incorporated into a mixed signal ASIC typically must meet unique, one-time-only performance parameters, a single fixed analog cell frequently is useful for only one design.

By allowing the variation of analog cell performance parameters, AMI's PABBGs provide the customers with all the benefits of full custom cell design as well as the primary advantage of fixed cell libraries: rapid development times for mixed-signal ASICs.

MSTEST

The MSTEST component of MSDS performs two functions aimed at decreasing time to market for mixed-signal ASIC designs. It enables customers to incorporate "design for testability" into their circuits, and it speeds the creation of ASIC manufacturing test programs by AMI engineers.

A test multiplexer has been designed into each of the analog blocks that are specified with the MSDS analog model builder software. The MSDS application tool interfaces (ATIs) connect the test muxes so that inputs and outputs are routed to test pads, and builds the control logic to enable and disable test paths. As a result of this "scan design" technique, each analog function incorporated into a mixed-signal ASIC will be tested individually, and test circuitry will be simulated in place. These capabilities reduce debug time as well as increase designers' awareness of the impact of test strategies on a design's performance at the onset of a design project.

At AMI, engineers use the performance parameters output by the analog model builder to create test modules for each analog block. These modules are implemented in the test program for a mixed-signal ASIC that uses that particular block. The modules aid automation of test program generation at AMI, which greatly reduces test time for any mixed-signal device.

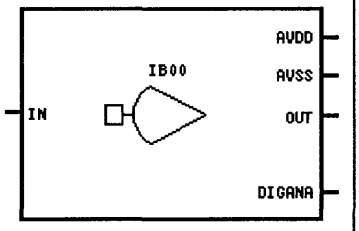
SECTION 4
ANALOG MODEL BUILDERS

Analog Model Builder
IB00

AMI	Buffered Input Pad	Rev 1.00

A high performance dual mode input pad used to bring signals onto the integrated circuit. In analog mode the pad is coupled to a high input impedance unity gain buffer amplifier which features wide bandwidth and rail to rail input common mode range. In digital mode the pad is coupled to a high speed digital buffer.

Cell Name: IB00



NAME	TYPE	PIN DESCRIPTION
IN	Analog Input	
OUT	Analog Output	
DIGANA	Control I/P	Analog/Digital mode selector.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6					Positive supply
AVSS	-6	-2.5				V	Negative supply
Input Offset(+-)					5	mV	
Input Capacitance			1		20	pf	
Cload		1000				pf	
Rload	100					kohms	
Bandwidth (analog)	0	1000				kHz	
Rise & Fall (digital)	1	100				nsec	
Common Mode Input Range						V	.99*AVSS<CMR<.99AVDD
Area			300		900		mils

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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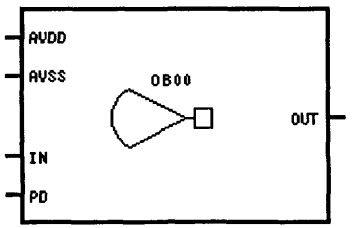
AMI SEMICONDUCTORS

AMI	Variable Drive Output Buffer	Rev 1.00

An analog output pad and unity gain buffer amplifier designed to drive circuits external to the integrated circuit. The cell features high output current drive, high common mode range, etc.

Cell Name: OB00



NAME	TYPE	PIN DESCRIPTION
IN	Analog Input	Input pin.
OUT	Analog Output	Output pin.
PD	Digital Input	Powerdown signal. Active high.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
Input Offset(+-)					5	mV	
Input Capacitance			1		20	pf	
Cload	1	1000				pf	
Rload	100					ohms	
Bandwidth	0.001	1				megHz	
Slew Rate	0.1	10				V/us	
Common Mode Range						V	.99*AVSS<CMR<.99*AVDD
Area			300		900		mils

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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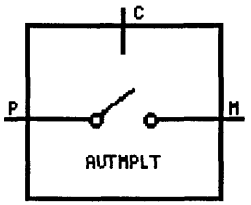
AMI	Analog Switch	Rev 1.00

A precision analog switch with charge injection cancellation and clock feedthrough compensation. This switch includes specialized control/clock generation circuitry which allows the switch to be controlled by a single signal line.

Cell Name: SW00



NAME	TYPE	PIN DESCRIPTION
P	Analog Input	
M	Analog Output	
C	Digital Input	Switch control.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
Closed On Resistance	0.1	100				kohms	
Open Off Resistance			1e+13		1e+15	ohms	
Port Capacitance	0.2	2				pf	
Switching Time	20	200				nsec	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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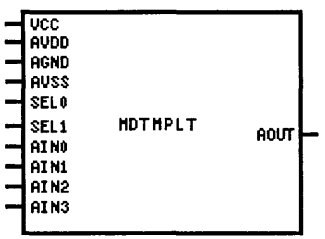
AMI	4:1 Analog Mux	Rev 1.00

This cell multiplexes one of four analog lines to a single analog line. All connections from input to output use break-before-make switches. No buffering is included to prevent the addition of unwanted offset. The analog switches in the multiplexer have higher input to output isolation than simple CMOS couplers.

Cell Name: MD00



NAME	TYPE	PIN DESCRIPTION
SEL0,SEL1	Digital Input	Select analog input to output.
AIN0-AIN3	Analog Input	Analog inputs multiplexed to output.
AOUT	Analog Output	Multiplexed output.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
AGND	Analog Supply	Analog Ground.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				VOLTS	(global spec)
AVSS	-6	-2.5				VOLTS	
Ron	50	100000				OHMS	
Roff	1e+08		1e+08			OHMS	
Tsel		100			100	nSEC	MAXIMUM
Input Range	-6	6		0		VOLTS	AVss < Vin < AVdd
Output Range	-6	6		0		VOLTS	AVss < Vout < AVdd

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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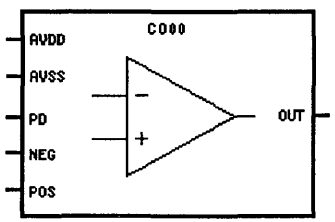
AMI SEMICONDUCTORS

AMI	Comparator	Rev 1.00

The comparator is capable of driving mixed capacitive and resistive loads. It has sufficient gain bandwidth and slew rate for high speed applications. All inputs and the output are accessible to internal circuitry.

Cell Name: C000



NAME	TYPE	PIN DESCRIPTION
NEG	Analog Input	Inverting input.
POS	Analog Input	Non-inverting input.
OUT	Analog Output	Comparator output.
PD	Digital Input	Powerdown signal. Active high.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	
AVSS	-6	-2.5				V	
Vout/Vin	100	100000				ratio	
Common-Mode Input Range						V	
Input Offset(+-)					5	mv	
Cload	0	1000				pf	
Rload	100					ohms	
Response time	150	600				ns	
IDD	5	50				ma	
Area			200		600	Mils	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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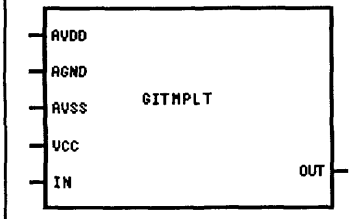
AMI	Inverting Resistive Gain Stage	Rev 1.00

An inverting resistive gain stage with a user definable gain (k) which is established by the ratio of two resistors. The accuracy of the gain is +-0.5% over temperature, voltage and process variation. The cell is capable of driving internal (or chip) mixed capacitive and resistive loads. All inputs and outputs of the gain stage are accessible using the MSTEST strategy.

Cell Name: GI00



NAME	TYPE	PIN DESCRIPTION
IN	Analog Input	
OUT	Analog Output	
AGND	Analog Supply	Analog Ground.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
F3dB	69.5622	1105.53				kHz	
K	0.995	10.05					gain
Rload	10					kohms	
Cload		25				pf	
Vin Range							
Slew Rate	0.1	10				V/us	
Vout Range							-Vsupply+1.25 to +vsupply-1.25
Input Refered offset(Vos)					5	mV	
Rin	4.8					kohms	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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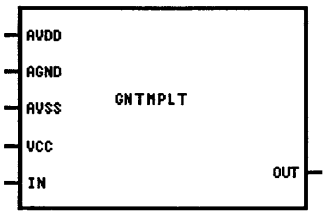
AMI	Non-inverting Resistive Gain Stage	Rev 1.00

A non-inverting resistive gain stage with a user definable gain (k) which is established by the ratio of two resistors. The accuracy of the gain is +-0.5% over temperature, voltage and process variation. The cell is capable of driving internal (on chip) mixed capacitive and resistive loads. The cell also features a very high input impedance. All inputs and outputs of the gain stage are accessible using the MSTEST strategy.

Cell Name: GN00



NAME	TYPE	PIN DESCRIPTION
IN	Analog Input	
OUT	Analog Output	
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
AGND	Analog Supply	Analog Ground.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
F3dB	69.5622	1105.53				kHz	
K	0.995	10.05					
Rload	10					kohms	
Cload		25				pf	
Vin Rnage							
Slew Rate	0.1	10				V/us	
Vout Range						V	-Vsupply+1.25 to +vsupply-1.25
Input Refered offset(Vos)					5	mV	
Cin					20	pf	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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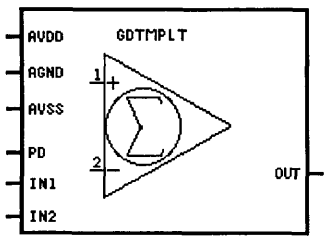
AMI	Difference Resistive Gain Stage	Rev 1.00

An difference resistive gain stage implements the function (V1-V2)(K), where K is a user definable gain. The accuracy of the gain is +-0.5% over temperature, voltage and process variation. The cell is capable of driving internal (on chip) mixed capacitive and resistive loads. All inputs and outputs of the gain stage are accessible using the MSTEST strategy.

Cell Name: GD00



NAME	TYPE	PIN DESCRIPTION
IN1	Analog Input 1	(relative to avss)
IN2	Analog Input 2	(relative to avss)
OUT	Analog Output	(relative to analog ground)
AGND	Analog Supply	Analog Ground.
AVDD	Analog Supply	Positive analog supply. (measured from agnd)
AVSS	Analog Supply	Negative analog supply. (measured from agnd)
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
F3dB	89.5522	1105.53				kHz	
K	0.995	10.05					
Rload	10					kohms	
Cload		25				pf	
Vin1 Range							
Vin2 Range							
Slew Rate	0.1	10				V/us	
Vout Range							-Vsupply+1.25 to +vsupply-1.25
Input Refered offset(Vos)					5	mV	
Rin	4.8					kohms	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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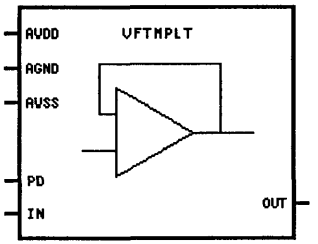
AMI	Voltage Follower	Rev 1.00

A This cell is implemented with an opamp in a voltage follower configuration. The cell has the input impedance of a MOSFET gate. The cell is not a pad cell, so the input can only be driven by on-chip signals. The cell is capable of driving internal (on chip) mixed capacitive and resistive loads. All inputs and outputs of the gain stage are accessible using the MSTEST strategy.

Cell Name: VF00



NAME	TYPE	PIN DESCRIPTION
IN	Analog Input	input signal
OUT	Analog Output	output signal
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
AGND	Analog Supply	Analog Ground.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
Opamp Open Loop Bandidth	117.9	131	117.9	124.45	131	Hz	unity gain bandwidth of cell
Opamp Open Loop Gain	1600	3200	1600	2400	3200		open loop opamp gain
Cell bandwidth	188640	419200	188640	303920	419200	Hz	gain bandwidth product
Rload	35000					ohms	
Cload	0	2.5e-11				Farad	
Vin Range	-4.6	5.95				Volts	
Slew Rate	100000	1e+07	100000	5.05e+06	1e+07	V/sec	
Vout Range	-5.9	5.5				V	-Vsupply+1.25 to +vsupply-1.25
Input Refered offset(Vos)	-0.005	0.005	-0.005	0	0.005	Volt	
Cin	5e-14	2e-13	5e-14	1.25e-13	2e-13	Farad	capacitance at input to ground
rout	100	1000	100	550	1000	Ohms	opamp open loop output resistance

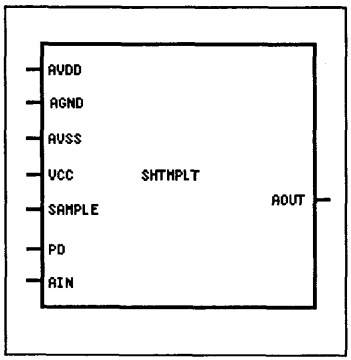
◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

Creating postscript file...

AMI	Sample and Hold	Rev 1.00

Sample and hold circuitry with a unity gain amplifier. The analog input is sampled on the rising edge of SAMPLE. The output does not track the analog input on either phase of SAMPLE. In powerdown mode AOUT is in a high impedance state.

Cell Name: SH00



NAME	TYPE	PIN DESCRIPTION
SAMPLE	Digital Input	Sample control. Samples AIN on rising edge.
PD	Digital Input	Powerdown signal. Active high.
AIN	Analog Input	Sample and hold input.
AOUT	Analog Output	Sample and hold output.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
AGND	Analog Supply	Analog Ground.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	
AVSS	-6	-2.5				V	
Gain Bandwidth		1				meghz	
Input Range							AVSS+.25 to AVDD-.25
Slew Rate		2				V/us	
Offset			-10		10	mV	
Cload		30				pf	
Rload	20					kohms	
Hold Step			-10		10	mV	
Sample Time	3.3					usec	
Aperture Time					50	nsec	
Settling Time	1					usec	
Droop Rate					1	V/sec	
Idd	100					uA	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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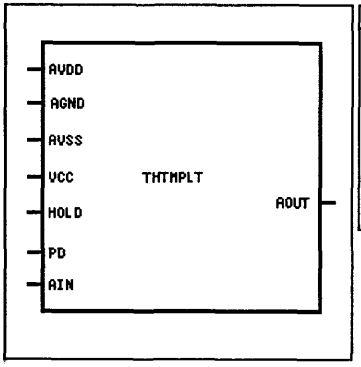
Analog Model Builder
TH00

AMI	Track and Hold	Rev 1.00

Track and hold circuitry with a unity-gain amplifier. The output tracks the input when HOLD is low. Powerdown mode places the output in a high impedance state.

Cell Name: TH00



NAME	TYPE	PIN DESCRIPTION
HOLD	Digital Input	Track and hold control. Hold when high.
PD	Digital Input	Powerdown signal. Active high.
AIN	Analog Input	Track and hold input.
AOUT	Analog Output	Track and hold output.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
AGND	Analog Supply	Analog Ground.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	
AVSS	-6	-2.5				V	
Gain Bandwidth		1				megHz	
Input Range							AVSS+.25 to AVDD-.25
Slew Rate		2				V/us	
Offset			-10		10	mV	
Cload		30				pf	
Rload	20					kohms	
Hold Step			-10		10	mV	
Aquisition Time	3.3					usec	
Aperture Time					50	nsec	
Settling Time	1					usec	
Droop Rate					1	V/sec	
Idd	100					uA	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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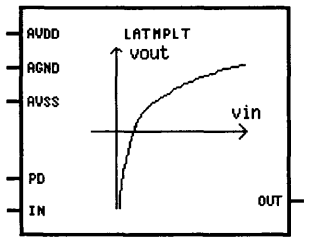
SDSW

AMI	Natural Logarithm Amplifier	Rev 1.00

preliminary! Implements the function Vout = - Vt * N * ln(Vin/(Iss * Rin) + 1) for Vin > agnd, for Vin <= agnd, Vout is held at agnd. See the "model notes" section of the info file for a more detailed description. The cell is capable of driving internal (on chip) mixed capacitive and resistive loads. All inputs and outputs of the logrithmic amplifier are accessible using the MSTEST strategy.

Cell Name: LA00



NAME	TYPE	PIN DESCRIPTION
IN	Analog Input	Input Voltage signal.
OUT	Analog Output	logarithmic voltage output.
pd	Digital Input	Power down signal (active high)
AGND	Analog Supply	Analog Ground.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
F3dB	900000	1.1e+06	900000	1e+06	1.1e+06	Hz	bandwidth of rectifier
Rload	35000					Ohms	resistance to agnd
Cload		35				pf	capacitance to agnd
Vin Range	0	6	0			Volts	-vsupply+1.5 to +vsupply-1.5
Slew Rate	100000	1e+07	100000	5.05e+06	1e+07	V/sec	Slew rate
Vout Range	-6	0			0	Volts	-Vsupply+1.25 to +vsupply-1.25
Input Refered offset(Vos)	-0.005	0.005	-0.005	0	0.005	Volts	input referenced opamp offset
Rin	4800	54000				Ohms	resistance to agnd
multiplier	1	3					integer multiplier of ln voltage
Iss	2.75617e-20	1.24555e-09				Amps	diode leakage current at temperature
Temperature range	-40	125				Celsius	degrees celseius
Open loop Gain opamp	3000	9000	3000	6000	9000		oepn loop gain of opamp

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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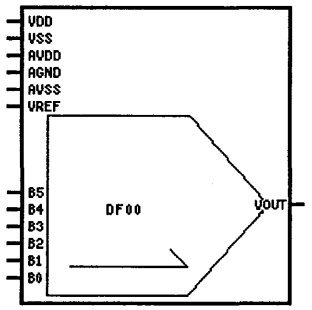
AMI	6-bit Resistive DAC	Rev 1.00

A resistive digital to analog converter that converts a 6-bit digital input into an accurate analog output. Conversion occurs asynchronously with changes on the digital input. The full scale range of the output is determined by the Vref voltage input. The inputs and the outputs are accessible using the MSTEST strategy.

Cell Name: D600



NAME	TYPE	PIN DESCRIPTION
B0 - B5	Digital Input(s)	6 bit data bus.
VOUT	Analog Output	DAC output voltage.
VREF	Analog Input	Reference voltage.
AVDD	Analog Supply	Positive supply.
AGND	Analog Supply	Analog Ground.
AVSS	Analog Supply	Negative supply.
VDD	Digital Supply	Digital voltage supply.
VSS	Digital Supply	Digital ground.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
Differential nonlinearity							+- .5 LSB
Integral nonlinearity							+- 2 LSB
Conversion time					5	us	Settling time to 1 LSB
Load capacitance	0	25				pF	
Load resistance	100	1000				meg ohm	
Digital Word Format							Offset binary
Power supply current	4	7				ma	
Temperature (junction)	-65	125				deg C	
Offset Error			5		15	mV	
Vref	1					V	
Most positive output						V	
Most negative output						V	
Least Significant Bit(LSB)						V	LSB

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

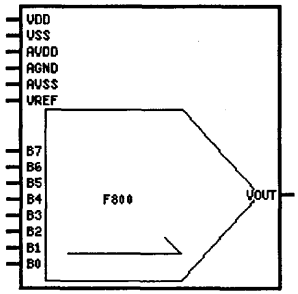
Creating postscript file...

MSDS

AMI	8-bit FET Current DAC (dual polarity)	Rev 1.00

A digital to analog converter provides an accurate dual polarity analog output voltage in response to the binary input code. The full scale output voltage is established by VREF and Rout. The FET DAC provides resolution of 8 bits with less chip area and less conversion time than the resistive DAC.

Cell Name: F800



NAME	TYPE	PIN DESCRIPTION
B0 - B7	Digital Input(s)	8 bit data bus.
VOUT	Analog Output	DAC output voltage.
VREF	Analog Input	Reference voltage.
AVDD	Analog Supply	Positive supply.
AGND	Analog Supply	Analog Ground.
AVSS	Analog Supply	Negative supply.
VDD	Digital Supply	Digital voltage supply.
VSS	Digital Supply	Digital ground.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
DAC resolution					8	bits	
Full Scale Output Voltage	0	4				V	
Power supply current	2	10				ma	
Temperature (junction)	-65	140				deg C	
Vref	1	2.5				V	
Conversion time	0.5	5				us	Settling time to 1 LSB
Full Scale Error	0.006						
Load capacitance	0					pF	
Load resistance						meg ohm	
Differential nonlinearity					0.25	LSB	
Integral nonlinearity					0.5	LSB	2 DNL
Digital Word Format							Offset binary
Offset Error					15	mV	
Least Significant Bit(LSB)						V	LSB
Rout						ohm	

◯ Check/Install. ◯ Toggle SABER params. ◯ Toggle TEST params.
◯ Exit. ● Print. ◯ Info. ◯ MSDS TEST DISABLED.

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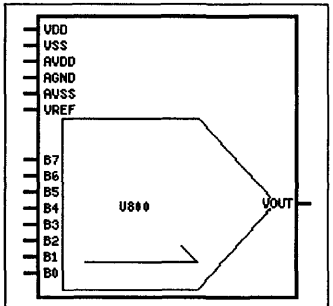
AMI	8-bit FET Current DAC (unipolar)	Rev 1.00

A digital to analog converter provides an accurate analog unipolar positive output voltage in response to the binary input code. The full scale output voltage is established by VREF and Rout. The FET DAC provides resolution of 8 bits with less chip area and less conversion time than the resistive DAC.

Cell Name: U800



NAME	TYPE	PIN DESCRIPTION
B0 - B7	Digital Input(s)	8 bit data bus.
VOUT	Analog Output	DAC output voltage. (relative to avss)
VREF	Analog Input	Reference voltage. (relative to analog ground)
AVDD	Analog Supply	Positive supply. (relative to analog ground)
AGND	Analog Supply	Analog Ground.
AVSS	Analog Supply	Negative supply. (relative to analog ground)
VDD	Digital Supply	Digital voltage supply.
VSS	Digital Supply	Digital ground.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
DAC resolution					8	bits	
Full Scale Output Voltage	0	4				V	
Power supply current	2	10				ma	
Temperature (junction)	-65	140				deg C	
Vref	1	2.5				V	
Conversion time	0.5	5				us	Settling time to 1 LSB
Full Scale Error	0.006						
Load capacitance	0					pF	
Load resistance						meg ohm	
Differential nonlinearity					0.25	LSB	
Integral nonlinearity					0.5	LSB	2 DNL
Digital Word Format							Unipolar,positive
Offset Error					15	mV	
Least Significant Bit(LSB)						V	LSB
Rout						ohm	

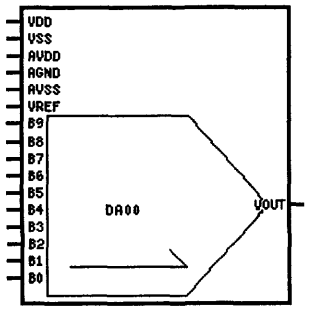
◯ Check/Install. ◯ Toggle SABER params. ◯ Toggle TEST params.
◯ Exit. ● Print. ◯ Info. ◯ MSDS TEST DISABLED.

Creating postscript file...

AMI	10-bit Resistive DAC	Rev 1.00

A resistive digital to analog converter that converts a 10-bit digital input into an accurate analog output. Conversion occurs asynchronously with changes on the digital input. The full scale range of the output is determined by the Vref voltage input. The inputs and the outputs are accessible using the MSTEST strategy.

Cell Name: DA00



NAME	TYPE	PIN DESCRIPTION
B0 - B9	Digital Input(s)	10 bit data bus.
VOUT	Analog Output	DAC output voltage.
VREF	Analog Input	Reference voltage.
AVDD	Analog Supply	Positive supply.
AGND	Analog Supply	Analog Ground.
AVSS	Analog Supply	Negative supply.
VDD	Digital Supply	Digital voltage supply.
VSS	Digital Supply	Digital ground.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
Differential nonlinearity							+- .5 LSB
Integral nonlinearity							+- 2 LSB
Conversion time					5	us	Settling time to 1 LSB
Load capacitance	0	25				pF	
Load resistance	100	1000				meg ohm	
Digital Word Format							Offset binary
Power supply current	4	7				ma	
Temperature (junction)	-55	125				deg C	
Offset Error			5		15	mV	
Vref	1					V	
Most positive output						V	
Most negative output						V	
Least Significant Bit(LSB)						V	LSB

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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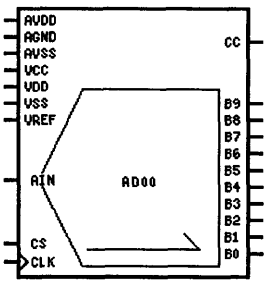
Analog Model Builder
AD00

AMI	10-bit ADC	Rev 1.00

A successive approximation analog to digital converter that provides a 10-bit digital representation of the analog input. The conversion is initiated by a pulse on the convert start input (CS). The conversion takes 60 cycles of the clock input (CLK). When the conversion is complete, the conversion complete signal (CC) goes high. The inputs and the outputs are accessible using the MSTEST strategy.

Cell Name: AD00



NAME	TYPE	PIN DESCRIPTION
B0 - B9	Digital Output(s)	10 bit data bus.
CC	Digital Output	Convert complete.
CLK	Digital Input	Main clock.
CS	Digital Input	Convert start.
AIN	Analog Input	Analog input pin.
VREF	Analog Input	Reference voltage.
AGND	Analog Supply	Analog Ground.
VCC	Analog Supply	Supply, substrate supply, or greater.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
VDD	Digital Supply	Positive digital supply.
VSS	Digital Supply	Negative digital supply.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6					Positive supply
AVSS	-6	-2.5				V	Negative supply
ADC resolution		10				bits	
Full Scale Error							+- 2% FSR
Offset Error	5	15				mV	
Differential nonlinearity							+- .5 LSB
Integral nonlinearity							+- 2 LSB
Clock rate	500	1000				kHz	
Conversion time							
At clock rate						us	60 clock cycles
Vref	1					V	
Input voltage range(+/-)							+- VREF
Power supply current	5	8				ma	
Temperature (junction)	-55	125				deg C	
Area		6000					mils

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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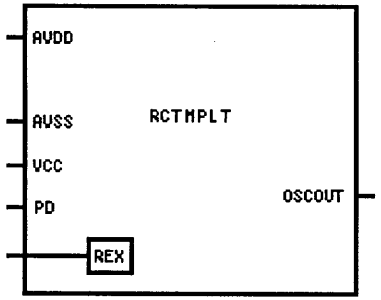
AMI	RC Oscillator	Rev 1.00

A RC sinusoidal oscillator. This circuit uses one external resistor and an external capacitor to oscillate at the desired frequency. The output frequency is very stable. The center frequency is accurate to 10%.

Cell Name: RC00



NAME	TYPE	PIN DESCRIPTION
OSCOUT	Analog Output	
REX		External resistor.
PD		Power down.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
Frequency	0.9	1100				kHz	+-10%
Rex	0.99	1010				kohms	external resistor +- 1%
Cosc	10	100				pf	
Idd	50	200				uA	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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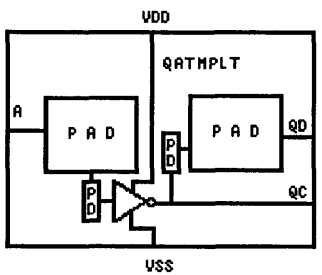
AMI	Crystal Oscillator	Rev 1.00

The Crystal Oscillator Cell contains a CMOS inverter amplifier and two capacitors to form a Pierce type oscillator. The capacitor can be either internal or external and it does not affect the accuracy of the oscillation frequency.

Cell Name: QD00



NAME	TYPE	PIN DESCRIPTION
A	Analog Input	Xtal input.
QO	Analog Input	Xtal input.
OUT	Digital Output	Oscillator frequency output.
VDD	Digital Supply	Positive digital supply.
VSS	Digital Supply	Negative digital supply.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
VDD	2.5	6				V	
VSS	-6	-2.5				V	
Oscillation frequency	0	20				megHz	
Delta Oscillation frequency	10	10000				%	of osc frequency
Crystal Model							
R=motional arm resistance						ohms	
L=motional arm inductance						mH	
C=motional arm capacitance						pF	
Co=shunt capacitance						pF	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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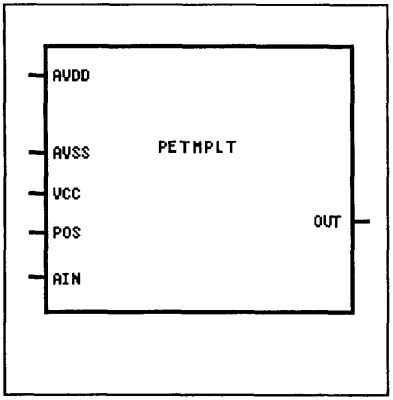
AMI	Peak Detector	Rev 1.00

A general purpose positive peak detector. This circuit uses an external holding capacitor, and two external resistors. The attack time constant (Y1), and holding time constant (Y2) are controlled by the external resistors and capacitor.

Cell Name: PE00



NAME	TYPE	PIN DESCRIPTION
AIN	Analog Input	
OUT	Analog Output	Peak output. Connects to external components.
POS	Analog Input	Peak input. Connects to external components.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
Cext	100					pf	
R1						kohms	
R2						kohms	
Rtotal	100					kohms	
Y1	50					usec	R1//R2*C
Y2		10000				usec	R2*C (Y1<Y2<1000)
Vpeak						V	(VDD-VSS)/2 to (VDD-100mV)R2/Rt

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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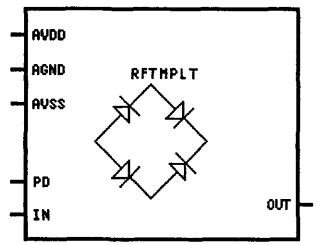
AMI	Full Wave Rectifier	Rev 1.00

preliminary! A full wave rectifier with a user definable gain (k) which is established by resistive ratios. The accuracy of the gain is +-0.5% over temperature, voltage and process variation. The cell is capable of driving internal (on chip) mixed capacitive and resistive loads. All inputs and outputs of the gain stage are accessible using the MSTEST strategy.

Cell Name: RF00



NAME	TYPE	PIN DESCRIPTION
IN	Analog Input	Voltage signal to be rectified.
OUT	Analog Output	Rectified output.
pd	Digital Input	Power down signal (active high)
AGND	Analog Supply	Analog Ground.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
F3dB	89.5622	1105.53				Hz	bandwidth of rectifier
Gain	0.995	10.05					(Vpeak out)/(Vpeak in)
Rload	10000					Ohms	resistance to agnd
Cload		2.5e-11				Farads	capacitance to agnd
Vin Range						Volts	-vsupply+1.5 to +vsupply-1.5
Slew Rate	100000	1e+07				V/sec	Slew rate
Vout Range						Volts	-Vsupply+1.25 to +vsupply-1.25
Opamp Input Refered offset(Vos)	-0.005	0.005	-0.005	0	0.005	Volts	input referenced opamp offset
Rin	4000	45000				Ohms	resistance to agnd
poserr	0.95	1.05	0.95	1	1.05		positive peak error
negerr	0.95	1.05	0.95	1	1.05		negative peak error
Comparator offset	-0.005	0.005	-0.005	0	0.005	Volts	comparator offset

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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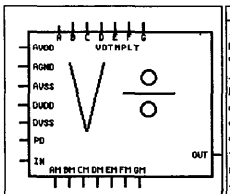
AMI	Voltage Divider	Rev 1.00

This cell produces 7 pairs of output voltages symmetrical around agnd from a negative input voltage. The cell is not a pad cell, so the input and output must be on-chip signals. The cell is capable of driving mixed capacitive and resistive loads, but the maximum permited capacitive load is relatively small, and the minimum permited resitive load relativley large. All inputs and outputs are compliant with the HSTEST strategy.

Cell Name: VD00



NAME	TYPE	PIN DESCRIPTION
IN	Analog Input	input signal
PD	Input	power down signal (active high)
VOUT	Analog Output	output signal symmetric around AGND with VIN
am	Analog Output	negative voltage output (most negative tap voltage)
bm	Analog Output	negative voltage output (voltage between cm and am)
cm	Analog Output	negative voltage output (voltage between dm and bm)
dm	Analog Output	negative voltage output (voltage between em and cm)
em	Analog Output	negative voltage output (voltage between fm and dm)
fm	Analog Output	negative voltage output (voltage between gm and em)
gm	Analog Output	negative voltage output (voltage between AGND and fm)
a	Analog Output	positive voltage output symmetric around AGND with am
b	Analog Output	positive voltage output symmetric around AGND with bm
c	Analog Output	positive voltage output symmetric around AGND with cm
d	Analog Output	positive voltage output symmetric around AGND with dm
e	Analog Output	positive voltage output symmetric around AGND with em
f	Analog Output	positive voltage output symmetric around AGND with fm
g	Analog Output	positive voltage output symmetric around AGND with gm
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.
AGND	Analog Supply	Analog Ground.
DVDD	Digital Supply	Positive digital supply.
DVSS	Digital Supply	Negative digital supply.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
DVDD	2.5	6				V	Positive digital supply
DVSS	-6	-2.5				V	Negative digital supply
Vin Range	-5	0				Volts	Voltage at input relative to AGND
Rin	5000	150000				ohms	input resistance to AGND
Rload	1.5e+06					ohms	output load resistance to AGND
Vout Range	-5	0				V	symmetric to vin except for offset & ratio errors
A voltage Range	-0.009					V	symmetric to am except for ratio & offset errors
B voltage Range	-0.009					V	symmetric to bm except for ratio & offset errors
C voltage Range	-0.009					V	symmetric to cm except for ratio & offset errors
D voltage Range	-0.009					V	symmetric to dm except for ratio & offset errors
E voltage Range	-0.009					V	symmetric to em except for ratio & offset errors
F voltage Range	-0.009					V	symmetric to fm except for ratio & offset errors
G voltage Range	-0.009					V	symmetric to gm except for ratio & offset errors
AH voltage Range		-0.009				V	greater than vin by at least tap seperation
BH voltage Range		-0.009				V	greater than am by at least tap seperation
CH voltage Range		-0.009				V	greater than bm by at least tap seperation
DH voltage Range		-0.009				V	greater than cm by at least tap seperation
EH voltage Range		-0.009				V	greater than dm by at least tap seperation
FH voltage Range		-0.009				V	greater than em by at least tap seperation
GH voltage Range		-0.009				V	greater than fm by at least tap seperation
Input Refered offset(Vos)	-0.005	0.005	-0.005	0	0.005	Volt	opamp input refered offset
Cload	0	2e-11				Farad	capacitance at output to ground
Cin	0	2e-12	0	1e-12	2e-12	Farad	capacitance at input to ground
Opamp Open Loop Gain	1000	3000	1000	2000	3000		open loop opamp gain
Opamp Open Loop Bandwidth	500000	2e+06	500000	1.25e+06	2e+06	Hz	unity gain bandwidth of cell
rout	100	1000	100	550	1000	Ohms	opamp open loop output resistance
Tap seperation	0.009		0.009			volts	voltage between sequential taps
Resistor ratio error	0.995	1.005	0.995	1	1.005		error in resistor ratios

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ● Print. ◯ Info.

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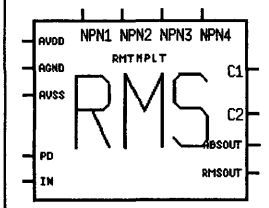
AMI	RMS to DC Converter	Rev 1.00

Preliminary!!! This cell implements an RMS converter whose DC component of the output voltage is proportional to the RMS voltage of the input waveform. The formula that is used is Vout = ave(vin**2) / vout. See the info notes for more detail on the model and AMB operation. This cell is temperature compensated to first order. The cell is capable of driving internal (on chip) mixed capacitive and resistive loads and an external integrating capacitor (Cint). All inputs and outputs of the logrithmic amplifier are accessible using the HSTEST strategy.

Cell Name: RM00



NAME	TYPE	PIN DESCRIPTION
IN	Analog Input	Input Voltage signal.
ABSOUT	Analog Output	output voltage rectified from input voltage.
RMSOUT	Analog Output	RMS output voltage from input voltage.
C1	Analog I/O	External integrating Capacitor
C2	Analog I/O	External integrating Capacitor
pd	Digital Input	Power down signal (active high)
NPN1	Analog I/O	collector 2*ln amp
NPN2	Analog I/O	emitter 2*ln amp, exponentiator
NPN3	Analog I/O	base, emitter exponentiator & ln amp
NPN4	Analog I/O	collector ln amp
AGND	Analog Supply	Analog Ground.
AVDD	Analog Supply	Positive analog supply.
AVSS	Analog Supply	Negative analog supply.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive analog supply
AVSS	-6	-2.5				V	Negative analog supply
Vin Range	-6	6				Volts	-vsupply+1.5 to +vsupply-1.5
Vout Range	0	6				Volts	sine input of vin_max peak. Freqency 10x integrator pole
Rload	35000					Ohms	output resistance to agnd of load
Cload		2e-11				Farads	output capacitance to agnd of load
Rin	4800	54000				Ohms	cell's input resistance to agnd
Cint	1e-08	1e-07				Farads	external integrator capacitor
Rint	9600	14400	9600	12000	14400	Ohms	internal integrator resistor
Gain rectifier	0.95	10.5					(Vpeak out)/(Vpeak in)
temperature range	-40	125				Celsius	operating temperature
Comparator offset (rect)	-0.005	0.005	-0.005		0.005	Volts	rectifier's comparitor offset
poserr rectifier	0.95	1.05	0.95	1	1.05		rectifier's positive peak error
negerr rectifier	0.95	1.05	0.95	1	1.05		rectifier's negative peak error
F3dB integrator	3.87e+06	4.73e+06	3.87e+06	4.3e+06	4.73e+06	Hz	bandwidth of integrator opamp
opamp offset (integrator)	-0.007	0.007	-0.007	0	0.007	Volts	integrator opamp input referenced offset
opamp rout (integrator)	100	2000	100	1050	2000	Ohms	integrator opamp rout open loop
open loop gain (integrator)	1000	3000	1000	2000	3000		integrator opamp open loop gain
F3dB function	372600	455400	372600	414000	455400	Hz	bandwidth of function opamps
opamp offset (function)	-0.005	0.005	-0.005	0	0.005	Volts	function opamp input referenced offset
opamp rout (function)	100	1000	100	550	1000	Ohms	function opamp rout open loop
open loop gain (function)	372600	455400	372600	414000	455400		function opamp open loop gain
Iss	2.75617e-20	1.24655e-09				Amps	diode leakage current
Beta Forward	100	200	100	150	200		transistor forward current gain
Beta Reverse	0.98	0.99	0.98	0.985	0.99		transistor reverse current gain
Input Resistance logamps	9600	14400	9600	12000	14400	Ohms	input resistance of log amps

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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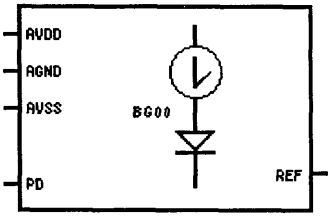
AMI	Band Gap Voltage Reference	Rev 1.00

This cell provides references virtually independent of temperature and power supply. In power down mode the output is pulled to AGND. The reference voltage is typically used as input to A/D's, D/A's, comparators, etc.

Cell Name: BG00



NAME	TYPE	PIN DESCRIPTION
REF	Analog Output	Reference relative to AGND.
PD	Digital Input	Powerdown signal. Active high.
AVDD	Analog Supply	Positive analog supply.
AGND	Analog Supply	Analog Ground.(=0V)
AVSS	Analog Supply	Negative analog supply.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive supply
AVSS	-6	-2.5				V	Negative supply
REF	0	5				V	
REF Capacitive Load	0	20				pF	
REF Resistive Load	10					k ohm	RL to AGND
Power Supply Rejection						N/A	N/A
REF-VDD			60		80	dB	At DC
REF-VSS			60		80	dB	At DC
Temperature Coefficient	-300	300					ppm/C
Idd (operating)	0.2					mA	PDN high, no load
Idd (standby)					10	nA	PDN low
Recovery time REF	10					us	Charging 20pF to within 0.25%

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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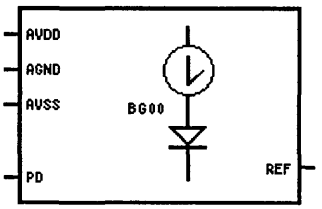
AMI	Trimmable Band Gap Voltage Reference	Rev 1.00

This cell provides references virtually independent of temperature and power supply. The reference voltage is fuse trimmable through the use of five external pad inputs. The fuses are blown at wafer sort. In power down mode the output is pulled to AGND. The reference voltage is typically used as input to A/D's, D/A's, comparators, etc.

Cell Name: BT00



NAME	TYPE	PIN DESCRIPTION
REF	Analog Output	Reference relative to AGND.
PD	Digital Input	Powerdown signal. Active high.
TRIM1	Analog Supply	Trim input pad
TRIM2	Analog Supply	Trim input pad
TRIM3	Analog Supply	Trim input pad
TRIM4	Analog Supply	Trim input pad
TRIM5	Analog Supply	Trim input pad
AVDD	Analog Supply	Positive analog supply.
AGND	Analog Supply	Analog Ground.(=0V)
AVSS	Analog Supply	Negative analog supply.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVDD	2.5	6				V	Positive supply
AVSS	-6	-2.5				V	Negative supply
REF	-5	0				V	
REF Capacitive Load	0	20				pF	
REF Resistive Load	10					k ohm	RL to AGND
Power Supply Rejection						N/A	N/A
REF-VDD			60		80	dB	At DC
REF-VSS			60		80	dB	At DC
Temperature Coefficient	-300	300					ppm/C
Idd (operating)	0.2					mA	PDN high, no load
Idd (standby)					10	nA	PDN low
Recovery time REF	10					us	Charging 20pF to within 0.25%
Tolerance	60	600				%	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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AMI	Voltage Regulator	Rev 1.00

Provides a regulated power supply from an external unregulated voltage. An external resistor and an external capacitor are required. In powerdown mode VREG may be driven from the pad with no loading from this cell.

Cell Name: VR00

NAME	TYPE	PIN DESCRIPTION
PD	Digital Input	Powerdown signal. Active low.
VREG	Analog Supply	Regulated supply output.
AVSS	Analog Supply	Negative analog supply.
VCC	Analog Supply	Supply, substrate supply, or greater.

PARAMETER	ALLOWABLE RANGE min	ALLOWABLE RANGE max	DESIRED RANGE min	DESIRED RANGE typ	DESIRED RANGE max	UNITS	CONDITIONS
AVSS	-6	-2.5				V	
Vreg	3.3	6				V	+-10%
Vunreg						V	
Rext	100	20000				ohms	
Ivreg	200					uA	
Iload	0					uA	
Cext	0.01	1				uf	

◯ Check/Install. ◯ Show/Clear SABER parameters.
◯ Exit. ◯ Print. ◯ Info.

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SECTION 5
DIGITAL SOFT MEGACELLS

AMI SEMICONDUCTORS

Digital Soft Megacells

Overview

This section describes AMI's offering of digital soft megacells. Megacells are blocks of memory or complex blocks of logic consisting of fundamental building primitives such as nand gates, nor gates, flip-flops, and latches. Such megacells can be either soft or hard. The Digital Soft Megacell offering is listed in Table 1.

A hard megacell is one in which the megacell function is defined by the physical mask layout; thus, each instance of the hard megacell has exactly the same physical layout within the boundaries of the megacell.

A soft megacell is defined only at the functional schematic level. In this case, each instance of the megacell will have exactly the same functional definition; however, the physical mask layout will be different for each instance, depending on other functions being used, the place-and-route tools, and process technology.

AMI's soft megacells are developed in AMI's ASIC Standard Library. This library is technology and process-independent and is available in both standard cells and gate arrays.

Because a soft megacell is both process and technology-independent, it has the advantages of design flexibility, portability, and a path for future cost reduction by process migration.

As process technologies have improved to permit the integration of more functions onto a single die, the demand for ASIC megacells has increased. Highly complicated megacells, such as AMI's MGMC51, become practical with process technologies at 1.0 micron feature sizes.

Soft megacells can be used with other megacells including ROM, RAM, and logic from the ASIC Standard Library to build a complete system on a chip.

The current offering consists of a selection of soft megacells which duplicate the function of industry standard parts, plus soft megacells that are developed using parameterized logic synthesizers.

Why Megacells

Using megacells in designing ASICs has several advantages. Megacells help decrease design time and costs by providing large building blocks that are the equivalent of standard products and functions. The power consumption of a soft megacell can be greatly reduced in comparison to the HMOS standard products they replace. Also, because several functions can be put on a single die, printed circuit board space and capacitances can be saved and the power requirements to get signals on and off ICs are minimized.

Reliability and system costs can be improved because of decreased part and pin counts. Also, because the megacell is typically implemented in a process technology smaller than the original standard product, performance can be several times that of the standard product.

What Are Soft Megacells

A soft megacell is defined as schematic pages. This approach provides extreme flexibility with regard to design changes, testability, fault grading, design checking, process selection, and whether the design is implemented as a gate array or standard cell. Also, to improve the robustness of the megacell, soft megacells are built with fully static logic. Design tools, methodologies and libraries available today greatly reduce the design risks associated with soft megacells. Since each instance of the cell can be back annotated with actual capacitive loading data, detailed timing analysis can validate each instance in the given application.

Since the megacell is just a schematic, its characteristics and functions can be changed or deleted by just changing the appropriate schematic pages. For example, to change the initial conditions of the MGMC51 output ports, it is only necessary to change the output port flip-flop in each port cell from a set type of flop to a reset type of flop.

By deleting unused functions, gate count can be minimized. For example, if a timer or UART is not being used, the associated gates can be deleted resulting in a lower gate count. Re-running the simulations, as one would do after any design change, validates correct implementation of the design change.

However, it is in design checking where the strengths of the soft megacell approach become obvious. Electronic design has benefited from the recent introduction of software programs that check many aspects of the design, including set up and hold times for flip-flops, the possibility of asynchronous race conditions, and the fault coverage of the test vectors. The schematic implementation of the megacell can be subjected to these checks along with the rest of the circuitry. Behavioral models, which are frequently used with hard megacells, bypass these checks.

Since the soft megacell uses only components of the ASIC Standard Library, process dependencies in the design are minimized, if not completely removed. As a result, the design can be ported to new technologies as they become available. This means not only future cost savings, but extended voltage and temperature operation as well.

Logic Synthesizers

Some of the soft megacells are produced by logic synthesizers. Examples are the MGMxxyyzv (multiplier) and the MGFxxyycv (latched-based FIFO). These synthesizers are parameterized, allowing the creation of various sizes. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each particular implementation is given a version number.

These logic synthesizers produce soft megacell schematics in the ASIC Standard Library and a schematic symbol. They are available on the various workstations.

Testing

Testability of soft megacells in IC designs must be considered when designing and simulating the circuits.

In most cases additional logic is necessary to facilitate testing the megacells. Providing either direct or multiplexed input and output pins for controlling and observing the soft megacells can greatly simplify both the testing of the IC and any system debugging. This dictates that designs be contained in packages having at least as many pins as the megacell with the highest pin count. To select the megacell pins, an unused condition on the interface is often used, which would normally never occur in an application. When enabled, the pins of a specific megacell are connected to the pins of the ASIC. The supplied simulations patterns, or your own, can then be run to develop a test or to verify the functionality of the megacell.

Ordering information

To order a megacell, see the digital megacell order form on the next page. For information on the availability of soft megacells on various workstations, or for information on specific speeds and sizes of synthesized soft megacells, contact the factory.

Table 1: AMI ASIC Standard Library Digital Soft Megacells

Cell Name	Description	Equivalent Gates
MG1468C18	Real-Time Clock	2000
MG29C01	4-Bit Microprocessor Slice	600
MG29C10	Microprogram Controller/Sequencer	750
MG65C02	8-Bit Core Processor	4000
MG80C85	8-Bit CMOS Microprocessor	2000
MG82C37A	Programmable DMA Controller	3000
MG82C50A	Asynchronous Communication Element	2300
MG82C54	Programmable Interval Timer	2600
MG82C55A	Programmable Peripheral Interface	750
MG82C59A	Programmable Interrupt Controller	900
MG82C84A	Clock Generator Driver	400
MGMC51	8-Bit Microcontroller Intel™ Equivalent	9500
MGMmmnnzv	Two's Complement / Unsigned Multiplier, sizes up to 32x32	Synthesized
MGAmmnnzv	Two's Complement / Unsigned Adder, sizes up to 32x32	Synthesized
MGFxxyyCv	First in First Out Register Generator	Synthesized
MGBxxyyAv	Barrel Shift Generator	Synthesized

Digital Soft Megacell Request Form

Company and division: _____

Engineering contact: _____

Address: _____

_____

Phone: _____

FAE/FSE: _____

Date needed: _____

Send this form to

American Microsystems, Inc.
2300 Buckskin Road
Pocatello, ID 83201
Fax (208) 234-6795
Attn: Steve Wadsworth

Schematic-based soft megacells[1]

- ❑ MG29C01
- ❑ MG29C10
- ❑ MG80C85
- ❑ MG1468C18
- ❑ MG82C37A
- ❑ MG82C50A
- ❑ MG82C54
- ❑ MG82C55A
- ❑ MG82C59A
- ❑ MG82C84A
- ❑ MGMC51
- ❑ MGMC51FB
- ❑ MG65C02

Synthesized soft megacells

❑ Adder (MGAxxyyzv)
- Number of A inputs_____
- Number of B inputs _____
- Throughput_____
- ❑ Military
- ❑ Commercial
- ❑ Two's complement
- ❑ Unsigned Magnitude

❑ FIFO (MGFxxyyCv)
- Number of words_____
- Number of bits/word_____
- Throughput_____
- ❑ Military
- ❑ Commercial

❑ Multiplier (MGMmmnnzv)
- Number of A inputs _____
- Number of B inputs _____
- Number of product outputs_____
- Throughput_____
- ❑ Military
- ❑ Commercial
- ❑ Two's complement
- ❑ Unsigned Magnitude

Requested data

- ❑ Schematics
- ❑ Simulation Patterns
- ❑ BOLT Netlist
- ❑ EDIF Netlist

Technology

- ❑ 1.25 micron Standard Cell
- ❑ 1.0 micron Standard Cell
- ❑ 1.25 micron Gate Array
- ❑ 1.0 micron Gate Array
- ❑ MSDS

Workstation[2]

- ❑ Mentor
- ❑ Viewlogic
- ❑ Valid
- ❑ Verilog
- ❑ Dazix
- ❑ Synopsys

Media type

- ❑ 3.5 inch Sun floppy
- ❑ 3.5 inch DOS floppy
- ❑ 5.25 inch floppy
- ❑ Cartridge

1. A customized confidential disclosure agreement must be in place before data can be shipped for schematic based megacells.
2. Contact the factory for more information and delivery times.

SECTION 6
MIXED-SIGNAL CAPABILITIES

CAPABILITIES

Custom Digital

AMI can support your custom digital applications. Custom digital design expertise is available for those high-volume or high-performance designs for which other approaches are not cost effective, or when the desired performance cannot be met in standard ASIC approaches. These cost/performance improvements are achieved through the careful design of a circuit which specifically meets the needs of the customer. Cost is minimized, when possible, through the use of standard cell libraries and compilers, and through a mix of Auto Place and Route (APAR) combined with hand-packing of layouts. Some of the custom digital design services that AMI offers include Dynamic Logic, Dynamic RAM, Specialty Logic, and Custom I/O.

Custom Analog

Custom ADCs and DACs

AMI has designed a variety of custom ADCs and DACs. Custom converters and some of their specifications are shown in the following table.

Custom ADCs and DACs

Type	Resolution	Conversion Time	Comments
Charge Redistribution (DAC)	6-10 bits	10μsec	No calibration required
Self-Calibrating Charge Redistribution (ADC)	12-16 bits	16μsec	
Tapped Resistor (DAC)	6-13	10μs	Subranging technique
Current Mirror (DAC)	6-7	2μs	10μA-10mA
μLaw (DAC)	6-8	10μs	
Video (DAC)	8	150ns	
Flash (ADC)	6	100ns	
Dual Slope (ADC)	10-16	100ms	Smaller area than self-calibrating ADC

Custom Operational Amplifiers

AMI has the ability to design a variety of custom op amps. Types of op amp customization include:

- Low voltage/current
- High gain-bandwidth
- Extended output drive (voltage/current)
- Low offset voltage (chopper stabilization)
- Power-down (sleep) mode
- Programmable slew rate/gain-bandwidth

AMI SEMICONDUCTORS

Filters

Switched Capacitor Filters

AMI has a long history in the design and implementation of Switched Capacitor Filter (SCF) circuits, dating back to some of the first commercially available codec filters. FILGEN allows automatic construction of filters in the standard approximations of Butterworth, Chebyshev, inverse Chebyshev and Elliptic, and in the standard realizations of lowpass, highpass, bandpass and bandstop. FILGEN uses cascaded, biquad techniques for implementation of SCFs. Our mixed-signal processes are ideally suited to switched-capacitor filter implementations with linear, poly-to-poly capacitors that allow precise ratio matching with small voltage and temperature coefficients. Digital standard cell libraries can be used to implement the control and clocking logic as well as other digital functions that may be required.

Typical Switched Cap Filter Performance	
Signal Swing	+V - 1.5 to -V + 1.5
Clock Rate	1 kHz to 500 kHz
Gain	20dB per stage (maximum)
Noise	0.5μv/√Hz (spectral density)
Crosstalk	-70dB in the passband
Dynamic Range	90dB (maximum)
Power Supply Rejection	40dB
Voltage	50mV
Harmonic Distortion	-65dB (2nd & 3rd harmonics)

Custom Filters

Custom filter capabilities include:

- Differential Group Delay Equalization utilizing all-pass filters
- Fully differential filters
- Ladder filters
- Custom transfer equations that do not fit the standard approximations
- Multiple sample rates within a single filter
- Programmable transfer functions

Other Analog Functions

Many other types of analog functions can be realized by AMI's expert analog design team, including:

- Voltage controlled oscillator
- Programmable gain stage
- Phase detector
- Phase-locked loop
- Precision Schmitt trigger
- Differential capacitance measurement
- Bus transceivers
- Hall-effect detector
- Amplitude modulator/mixer
- Programmable gain stage
- Rectifier
- Waveform synthesis
- Audio amplifier
- Automatic gain control
- Compressor/expander
- Energy detector
- Crosspoint switch
- DC to DC converter
- Voltage regulator
- Oscillator
- Integrator
- Charge pump

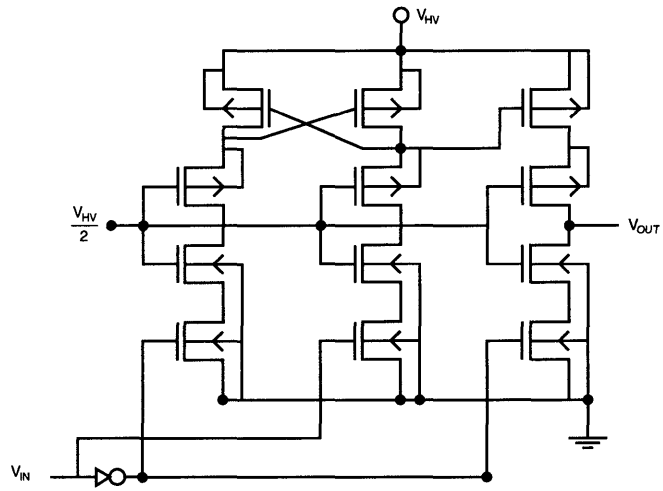
SECTION 7
HIGH VOLTAGE

High Voltage Output Drivers

AMI's patented techniques for designing high-voltage digital output drivers using our highly versatile, relatively inexpensive mixed-signal CMOS processes give us a competitive edge in high-voltage output driver design. AMI has been designing high-voltage outputs for low-voltage VLSI circuits since 1981 for both the custom and standard product markets.

Some of the many applications for our high-voltage output drivers include vacuum fluorescent displays, dichroic LCDs, solenoids, print head drives, DC and stepping motors, and relays. These applications serve the military, avionic, automotive and other high-reliability markets.

High Voltage Output Buffer: 1.5/3.5 micron CMOS



Characteristic	1.5/3.5 micron CMOS
H.V. Output Max. Voltage	to 50V
Source Current Capability	to 30mA
Sink Current Capability	to 30mA
Typical Switching Speed (100pF Load)	<1μs
Logic Voltage Supply	2.5V to 12V
Logic Speeds	to 50MHz

SECTION 8
INTRODUCTION TO CYX LIBRARY
WITH LIBRARY CHARACTERISTICS

CYX 1.0 micron CMOS Standard Cells

INTRODUCTION

The CYX Standard Cell Library sections 8 through 10 of the data book contain electrical characteristics, delay characteristics, and data sheets. Each library is designed for operation from 2.5V to 5.5V. Two libraries are provided. Both libraries are implemented in the CY n-well process and are characterized at 5V with derating factors from 2.5V to 5.5V. The CYB library has implicit power pin connections simplifying the schematic capture task. This library is ideal for mixed-signal applications that do not require digital noise isolation. The CYBS library has explicit power pins and a separate p-substrate bus for digital noise isolation. This library is ideal for mixed-signal applications that have critical noise requirements. Since the two libraries have similar timing, only the CYB data is included and is adequate for estimating delays. Models exist for each library which can be provided through design kits for the chip design.

The CYBL and CYBLS libraries are not included in this data book; they are 3V versions of the CYB and CYBS libraries, respectively. Preliminary values can be obtained by derating the CYX data to 3V values. Actual 3V data sheets can be obtained by contacting the sales offices or the factory.

LIBRARY FEATURES

The libraries implement all the functions in JEDEC Standard No. 12-3. They also implement several additional functions as a supplement to the standard. AMI refers to this implementation as the ASIC Standard Library. The ASIC Standard Library is the core offering for both standard cells and gate arrays.

Standard cell libraries are functionally compatible with gate array libraries because of the ASIC Standard approach. Standard cell and gate array libraries use the same transistor level schematics, except for transistor sizes, since standard cells take advantage of the ability to vary transistor widths to optimize the switch point of the gates. The standard cells have comparable delays with the gate array cells so that designs can be migrated from one library to the other with minimum effort.

These standard cell libraries were developed using AMI's internal design system called Accolade. This system is a complete cell design system featuring symbolic graph compaction, mask data extraction, characterization, logic model data creation, and data sheet creation. This system makes the libraries more process independent for faster cell migration to new process technologies.

Megacells are available, such as core processors, RAMs, DPRAMs, ROMs, FIFOs, and DSP type cells. These libraries also support mixed-signal applications requiring polysilicon linear capacitors.

CYX 1.0 micron CMOS Standard Cells

LIBRARY CHARACTERISTICS
DC OPERATING CHARACTERISTICS

Table 1 contains the absolute maximum ratings for CYX ASIC library chips using the standard cell libraries. Tables 2 through 4 contain the input and output operating specifications for the library at 5V. The library is characterized for operation from 2.5V to 5.5V. The output current drive in table 4 will vary with the supply voltage, Vol, and Voh specifications. Contact the factory for operating specifications at supply voltages other than 5V.

Table 1: Absolute Maximum Ratings

Parameter	Range	Units
VDD, Supply Voltage	-0.3 to 7.0	Volts
Input Pin Voltage	-0.3 to VDD+0.3	Volts
Input Pin Current	-10.0 to 10.0	mA
Storage Temperature Plastic Packages	-55 to 125	°C
Storage Temperature Ceramic Packages	-65 to 150	°C
Lead Temperature	300	°C for 10 sec.

Note that these specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect the long term reliability of the device.

Table 2: Operating Specifications

Parameter	Minimum	Maximum	Units
VDD, Supply Voltage	2.5	5.5	Volts
Ambient Temperature - Military	-55	125	°C
Ambient Temperature - Commercial	0	70	°C

Table 3: Input Operating Specifications

Parameter	Minimum	Maximum	Units
CMOS Input Specifications, (4.5V ≤ VDD ≤ 5.5V, Military T_A)			
Vil Low Level Input Voltage		0.3*VDD	Volts
Vih High Level Input Voltage	0.7*VDD		Volts
Iil Low Level Input Current		-1.0	µA
Iih High Level Input Current		1.0	µA
Iil Input Pull-up Current	-43	-190	µA
Iih Input Pull-down Current	39	217	µA
Vt- Schmitt Negative Threshold	0.2*VDD		Volts
Vt+ Schmitt Positive Threshold		0.8*VDD	Volts
Vh Schmitt Hysteresis	1.0		Volts

Parameter	Minimum	Maximum	Units
TTL Input Specifications, (4.5V ≤ VDD ≤ 5.5V, Military T_A)			
Vil Low Level Input Voltage		0.8	Volts
Vih High Level Input Voltage	2.0		Volts
Iil Low Level Input Current		-1.0	µA
Iih High Level Input Current		1.0	µA
Iil Input Pull-up Current	-30	-560	µA
Iih Input Pull-down Current	30	560	µA
Vt- Schmitt Negative Threshold	0.8		Volts
Vt+ Schmitt Positive Threshold		2.3	Volts
Vh Schmitt Hysteresis	0.4		Volts

Table 4: Output Operating Specifications

	VDD = 5.0V ± 10%		
Parameter	**Minimum**	**Maximum**	**Units**
1.0mA Driver			
Vol Low Level Output Voltage		0.4	Volts
Voh High Level Output Voltage	2.4		Volts
Iol Low Level Output Current		1.0	mA
Ioh High Level Output Current		-1.0	mA
2.0mA Driver			
Vol Low Level Output Voltage		0.4	Volts
Voh High Level Output Voltage	2.4		Volts
Iol Low Level Output Current		2.0	mA
Ioh High Level Output Current		-2.0	mA
4.0mA Driver			
Vol Low Level Output Voltage		0.4	Volts
Voh High Level Output Voltage	2.4		Volts
Iol Low Level Output Current		4.0	mA
Ioh High Level Output Current		-4.0	mA
8.0mA Driver			
Vol Low Level Output Voltage		0.4	Volts
Voh High Level Output Voltage	2.4		Volts
Iol Low Level Output Voltage		8.0	mA
Ioh High Level Output Current		-8.0	mA

Figures 1 and 2 show typical current voltage curves for the pad driver transistors from 1mA to 8mA. References to "typical" mean the data was characterized for Tj = 25°C, Vdd = 5 volts, and typical (nominal) process. Figures 3 and 4 show the typical current voltage curves for input pads with pull-up and pull-down devices.

CYX 1.0 micron CMOS Standard Cells

Figure 1: Typical N-Channel Driver DC Characteristics at VDD = 5V

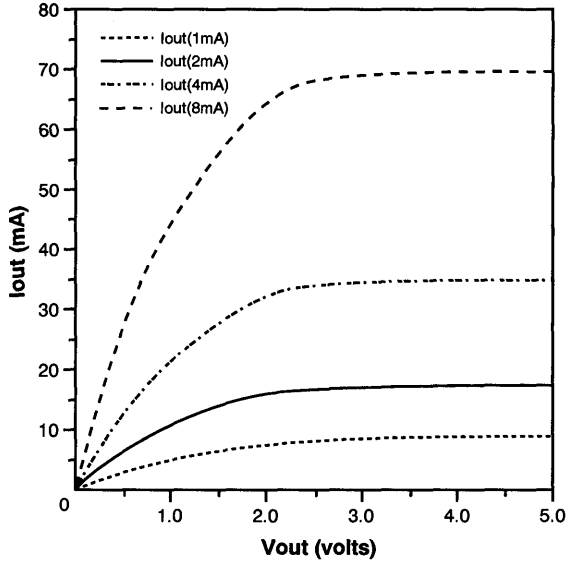


Figure 2: Typical P-Channel Driver DC Characteristics at VDD = 5V

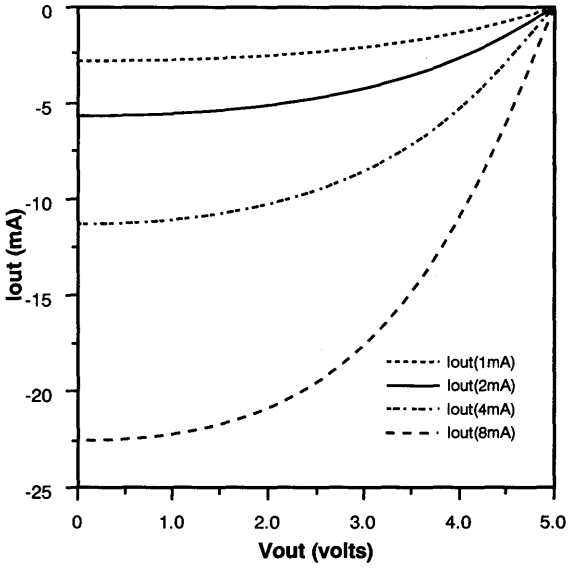


Figure 3: Typical Pull-down Characteristics at VDD = 5V

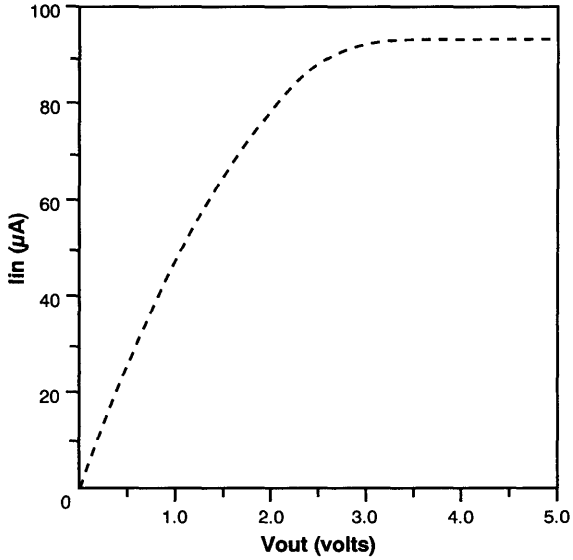
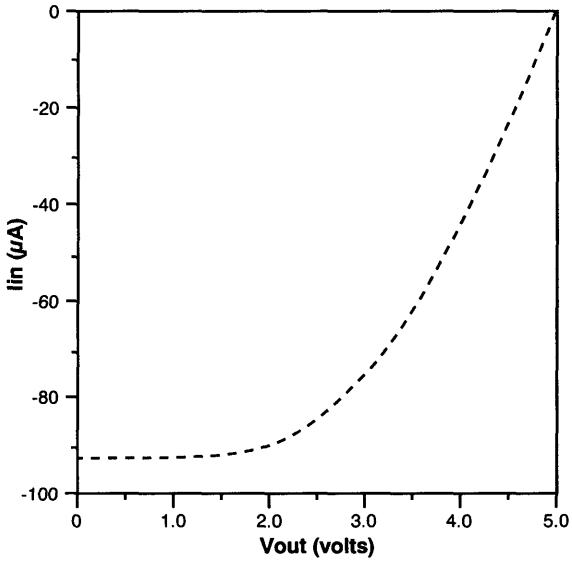


Figure 4: Typical Pull-up Characteristics at VDD = 5V



CYX 1.0 micron CMOS Standard Cells

Figure 5 and tables 5 and 6 show derating factors for the current due to temperature voltage and process. Values are normalized to typical conditions. To obtain a current value at conditions other than typical, multiply the derating factors corresponding to those conditions by the current values from the curves in figures 1 through 4, i.e. $K_{TDC}*K_{VDC}*K_{PDC}*I_{DC}$.

Figure 5: Temperature Derating Factors for DC Characteristics at VDD = 5V

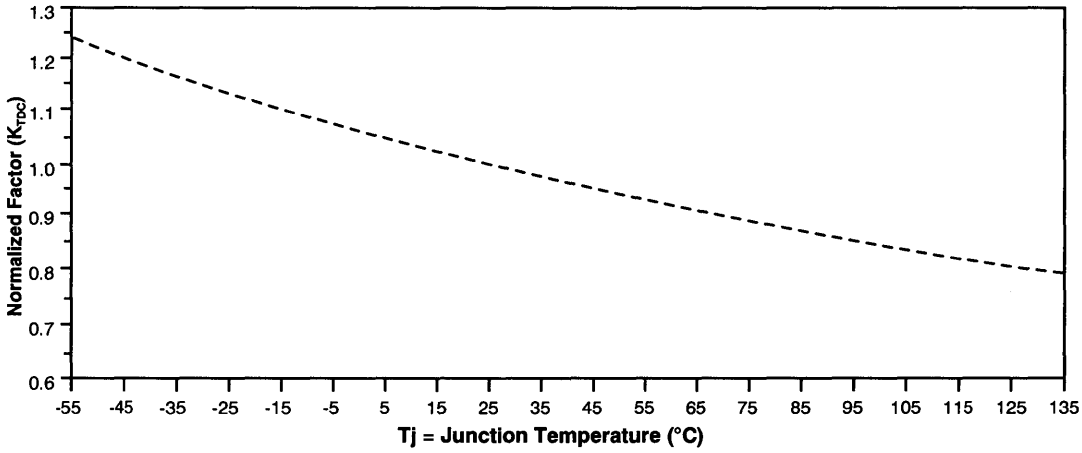


Table 5: Voltage Derating Factors for DC Characteristics at VDD = 5V

	N-Channel (Vol = 0.4V)			P-Channel (Voh = 2.4V)		
VDD	4.5	5.0	5.5	4.5	5.0	5.5
K_{VDC}	0.93	1.00	1.06	0.79	1.00	1.22

Table 6: Process Derating Factors for DC Characteristics at VDD = 5V

	N-Channel (Vol = 0.4V)			P-Channel (Voh = 2.4V)		
Process	WCS	TYP	BCS	WCS	TYP	BCS
K_{PDC}	0.55	1.00	1.44	0.63	1.00	1.50

DELAY OPERATING CHARACTERISTICS

Delay values for CMOS cells are measured between the input and output 50% voltage supply (Vdd) crossing points. TTL input buffers are measured from the input's 1.4 volt crossing point to the output's 50% Vdd crossing point. TTL output buffers are measured from the input's 50% Vdd crossing point to the output's 1.4 volt crossing point. All delays are characterized at typical conditions (Tj = 25°C, Vdd = 5 Volts, and typical process).

Figures 6, 7, and table 7 contain derating factors for various temperatures, voltages, and process variations respectively. To obtain a delay value at conditions other than typical, multiply the derating factors corresponding to those conditions to the current values from the delays in the data sheets; i.e., $K_T*K_V*K_P*T_D$, where T_D can be a delay from the delay characteristics table mentioned on page 8-10 or a value calculated from the propagation delay equations, also mentioned on page 8-10.

Figure 6: Temperature Derating Factors for Delay Characteristics

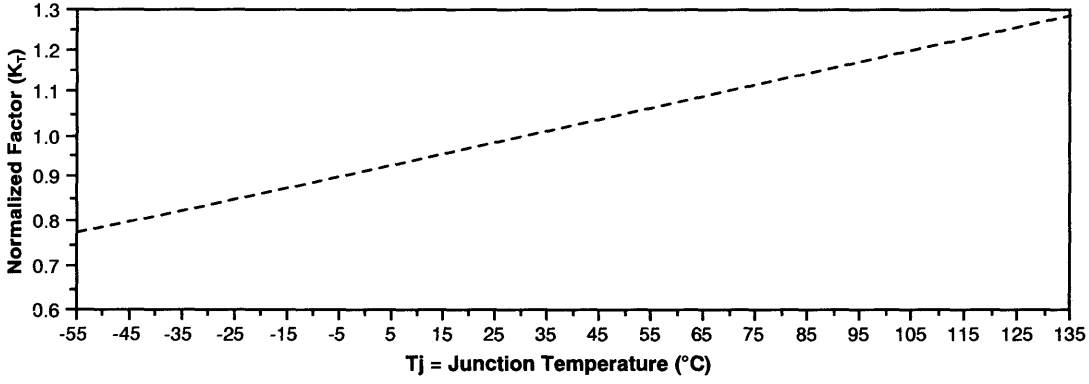


Figure 7: Voltage Derating Factors for Delay Characteristics

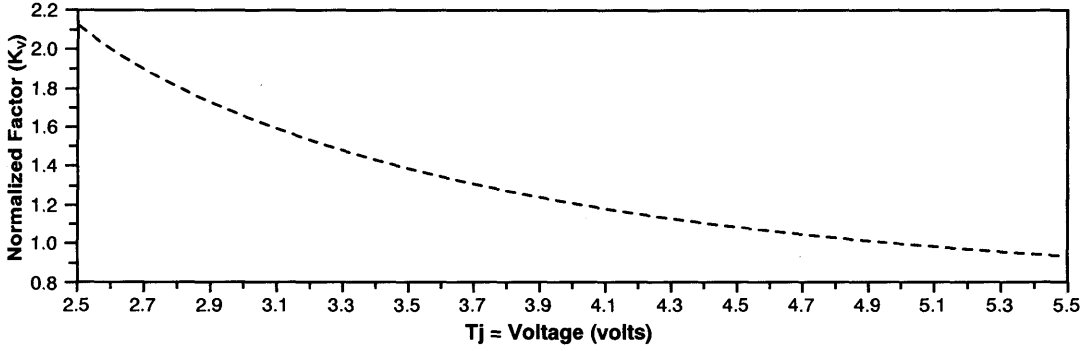


Table 7: Process Derating Factors for Delay Characteristics

	WORST CASE	TYPICAL CASE	BEST CASE
K_P	1.38	1.00	0.60

CYX 1.0 micron CMOS Standard Cells

INTERPRETING THE DATA SHEET

Figure 8 shows a typical data sheet and points out the main features of the data sheet. Not shown is a schematic which accompanies some of the more complex cells.

Figure 8

Cell Name → **AA21**

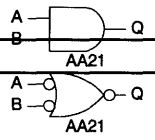
AMI SEMICONDUCTORS

Library Type → **CYX 1.0 micron CMOS Standard Cells**

Description → **Description:**
AA21 is a two-input gate which performs the logical AND function.

Logic Symbol	Truth Table	Pin Loading

Logic Symbol →



Truth Table →

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading →

	Ci (pF)
A	0.06
B	0.06

Equivalent Gates → **Equivalent Gates:**.....1.4

Bolt Syntax → **Bolt Syntax:**.....Q .AA21 A B;

Power Characteristics → **Power Characteristics:**

Parameter	Value	Units
Static $I_{DD}(T_J = 85°C)$	2.60	nA
$^{\dagger}C_{pd}$	0.19	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics → **Delay Characteristics:**
Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.35	1.15	0.52	0.69	1.04
		t_{PHL}	0.43	0.88	0.55	0.68	0.95

Propagation Delay Equations → **Propagation Delay Equation:** $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

A description of these features of the data sheet are as follows.

LIBRARY TYPE: Designates the feature size and library type such as standard cell or gate array.

CELL NAME: AMI's cell name.

DESCRIPTION: A brief sentence about the function of the cell.

LOGIC SYMBOL: Shows a picture of the symbol as it appears as an icon in the workstation design kits.

TRUTH TABLE: A boolean table showing the output logic levels as a function of the input logic levels.

Types of logic levels found in the logic tables are as follows:

H	=	High level steady state,
L	=	Low level steady state,
↑	=	Transition from Low level to High level,
↓	=	Transition from High level to Low level,
X	=	Any level including transitions,
NC	=	No Change in output level for a given set of input levels,
IL	=	The output level is unknown for this set of Illegal input levels,
Z	=	High impedance level,
UN	=	Undriven Node or input,
Q(n)	=	The level of Q before an active transition on the affecting node, and
QN(n)	=	The level of QN before an active transition on the affecting node.

PIN LOADING: A table of cell input capacitances in picofarads. Output pin capacitance is given for 3 state cells only. This information can be used to determine the fan-out loading on cell outputs.

EQUIVALENT GATES: Equivalent gates for the cell is defined as the cell area normalized to the area of the NA21 (2 input nand gate).

BOLT SYNTAX: BOLT (Block Oriented Logic Translator) is an AMI proprietary netlist format. This line shows the BOLT syntax for the cell. One example of the use of BOLT is as a design interface from the workstation design kits to AMI.

POWER CHARACTERISTICS:

Power for the cell can be described in three parts. The first part is the power dissipated due to the leakage current across the channels and through the formed diodes. The second part is due to the switching voltage across capacitance on the internal nodes of the cell. Finally, the third part is due to the switching voltage across a load capacitance.

The power characteristics table provides the static leakage current for a junction temperature of 85°C, and the capacitance for all the switching nodes in the cell. It also gives the equation calculating power from these two values. It does not include the power due to the load capacitance. This capacitance can be obtained by adding up all the input capacitances of the driven cells and adding the interconnect capacitance. The average interconnect capacitance for the 1.0 micron ASIC Standard Library is 0.047pF. AMI can prepare an estimate of the power upon submission of a netlist which uses a statistical model of the interconnect based on die size and fan-out.

$$POWER = (Static\ I_{DD})\ V_{DD} + C_{pd}\ V^2_{DD} f + C_L V^2_{DD} f$$

where

$Static\ I_{DD}$ = *static leakage current of the cell*
V_{DD} = *operating voltage*
C_{pd} = *capacitance of the switching nodes in the cell*
f = *frequency of operation*
C_L = *capacitance of the driven pins and interconnect*

The frequency term of the power equation dominates, making the static current term insignificant. However, the term can be used to find the standby current.

CYX 1.0 micron CMOS Standard Cells

DELAY CHARACTERISTICS: This table contains delay data for the various input to output paths in the cells. Table 8 explains each column in the delay characteristics table.

Table 8: Explanation of Columns in the Cell Characteristics Table

Column Name	Explanation	
Delay (ns) From To	Names the two pins that identify the path for the delay	
Parameter	Mnemonic for the propagation delay or timing parameter whose value can be calculated by using the tdx and Ktdx columns in conjunction with the propagation delay equation.	
	t_{PLH}	Input to output propagation delay for a rising edge on the output
	t_{PHL}	Input to output propagation delay for a falling edge on the output
	t_{ZH}	High impedance to high level delay
	t_{ZL}	High impedance to low level delay
	t_{HZ}	High level to high impedance delay
	t_{LZ}	Low level to high impedance delay
	t_{su}	Input setup time with respect to clock
	t_h	Input hold time
	t_w	Input pulse width
tdx (ns)	Contains values for the intrinsic delay through the cell. The x in t_{dx} is a variable representing r for the rising output delay (t_{PLH}), f for the falling output delay (t_{PHL}), or x for any of the other parameters. The values are given in nanoseconds.	
Ktdx (ns/pF)	Contains delay per capacitance values to determine the delay due to capacitance loading on the "To" pin. The x in K_{tdx} has the same meaning as in the t_{dx}. The values are given in nanoseconds/picofarad.	
Number of fan-outs	Contains the capacitance value and delay values for different loads. For output pad cells 25pF, 50pF, 75pF, and 100pF loads are used. For core cells and input pad cells fan-outs of 2, 4, and 8 gates are used. These fan-out loads are determined by the indicated number of NA21 inputs and an interconnect capacitance from a statistical table of fan-out values for a chip that is 250 mils on a side.	

PROPAGATION DELAY EQUATION: This equation shows how to calculate the total delay for the load dependent delay paths using the delay characteristics table. Following are some notes to help in understanding how to use the equations.

$K_PK_VK_T$ equals $K_P*K_V*K_T$, which are the derating factors for finding delays at conditions other than typical. Use figures 6 and 7 and table 7 for these values of K_P, K_V, and K_T.

When the equations use t_{dx} and K_{tdx}, use either rise delay values or fall delay values for both variables.

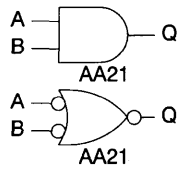
If rise and fall delay numbers need to be inter-mixed, the equations will specifically state this, i.e. $t_{dr} + K_{tdf}(CL)$.

If the equations inter-mix delays from different paths, then the delay variable will designate this with a pin value in parenthesis at the end of the variable.

SECTION 9
CYX LIBRARY

Description:
AA21 is a two-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06

Equivalent Gates:.....1.4
Bolt Syntax:.....Q .AA21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.60	nA
†C_{pd}	0.19	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

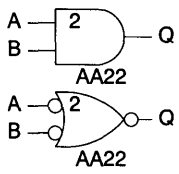
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH} t_{PHL}	0.35 0.43	1.15 0.88	0.52 0.55	0.69 0.68	1.04 0.95

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
AA22 is a two-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06

Equivalent Gates:.....1.6
Bolt Syntax:.....Q .AA22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.55	nA
†C_{pd}	0.25	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

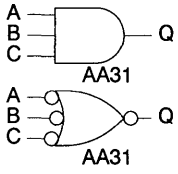
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.40	0.63	0.49	0.58	0.78
		t_{PHL}	0.47	0.56	0.55	0.63	0.81

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
AA31 is a three-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .AA31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.42	nA
†C_{pd}	0.24	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

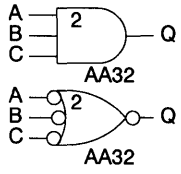
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.55	1.23	0.72	0.90	1.28
		t_{PHL}	0.53	0.97	0.67	0.81	1.11

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
AA32 is a three-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06

Equivalent Gates:.....1.9
Bolt Syntax:.....Q .AA32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	4.37	nA
†C_{pd}	0.30	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

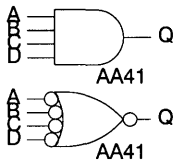
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.60	0.71	0.70	0.81	1.02
		t_{PHL}	0.57	0.62	0.65	0.75	0.94

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

Description:
AA41 is a four-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06

Equivalent Gates:.....1.9
Bolt Syntax:.....Q .AA41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.98	nA
†C_{pd}	0.26	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

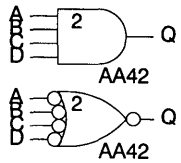
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.68	1.29	0.87	1.06	1.46
		t_{PHL}	0.64	1.04	0.79	0.94	1.26

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
AA42 is a four-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06

Equivalent Gates:.....2.3
Bolt Syntax:.....Q .AA42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.93	nA
†C_{pd}	0.32	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

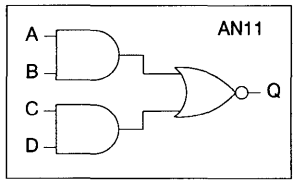
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.75	0.76	0.86	0.98	1.21
		t_{PHL}	0.68	0.69	0.77	0.88	1.08

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
AN11 is an AND-NOR circuit consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06

Equivalent Gates:.....1.8
Bolt Syntax:.....Q .AN11 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.04	nA
†C_{pd}	0.22	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.42	1.50	0.63	0.86	1.32
		t_{PHL}	0.44	1.40	0.64	0.85	1.28

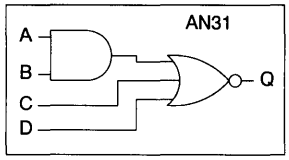
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:

AN31 is an AND-NOR circuit consisting of a 2-input AND gate and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06

Equivalent Gates:.....1.6
Bolt Syntax:.....Q .AN31 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.16	nA
†C_{pd}	0.20	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

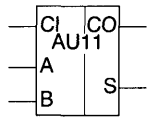
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.65	2.72	1.04	1.45	2.28
		t_{PHL}	0.39	1.71	0.63	0.88	1.40

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
AU11 is a combinational one-bit full adder.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Pin Loading

	Ci (pF)
A	0.28
B	0.27
CI	0.22

Equivalent Gates:.....6.2
Bolt Syntax:.....CO S .AU11 A B CI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.93	nA
†C_{pd}	0.99	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

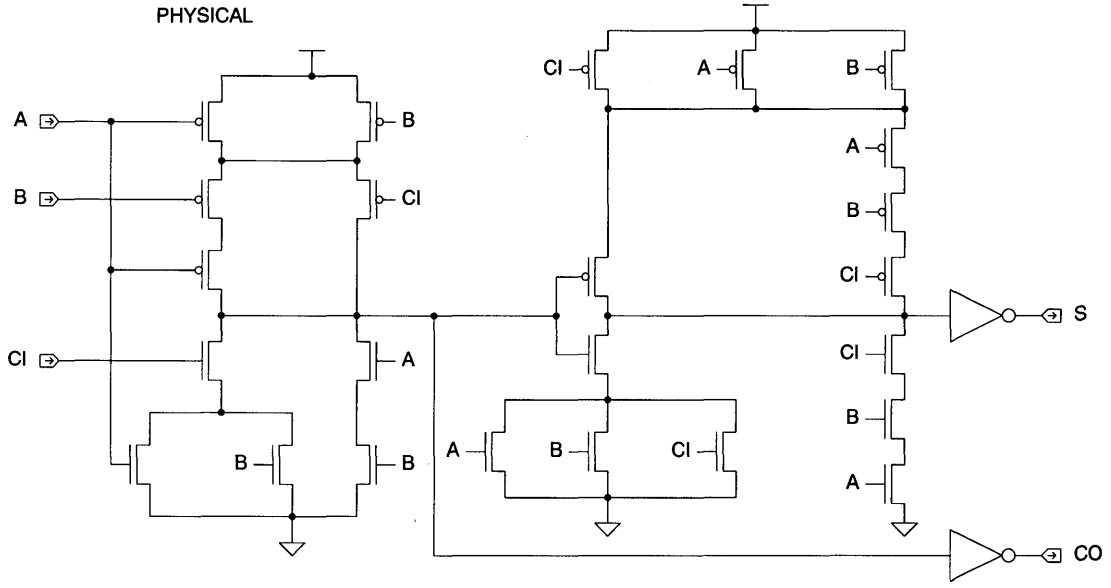
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

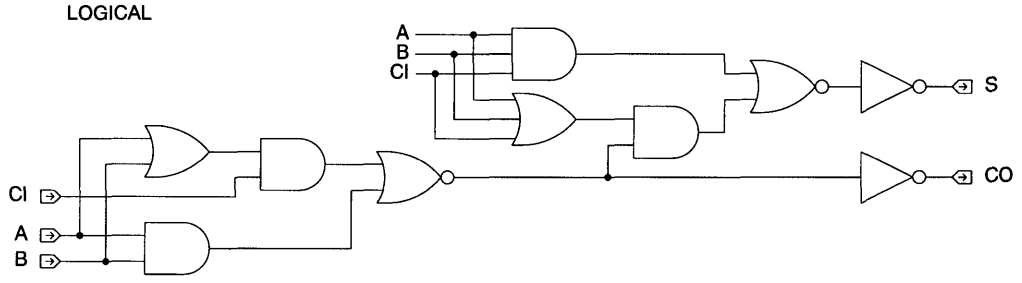
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	S	t_{PLH}	1.26	1.18	1.43	1.61	1.97
		t_{PHL}	1.33	1.17	1.50	1.67	2.03
B	S	t_{PLH}	1.37	1.18	1.54	1.72	2.08
		t_{PHL}	1.15	1.17	1.32	1.49	1.85
CI	S	t_{PLH}	0.85	1.18	1.02	1.20	1.56
		t_{PHL}	1.04	1.17	1.20	1.38	1.74
A	CO	t_{PLH}	0.92	1.28	1.11	1.30	1.68
		t_{PHL}	0.83	1.22	1.00	1.18	1.55
B	CO	t_{PLH}	0.90	1.28	1.08	1.27	1.66
		t_{PHL}	0.89	1.22	1.06	1.24	1.61
CI	CO	t_{PLH}	0.72	1.28	0.91	1.10	1.49
		t_{PHL}	0.59	1.22	0.76	0.94	1.32

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

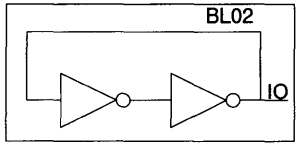
CYX 1.0 micron CMOS Standard Cells

Logic Schematic





Description:
BL02 is a tri-state bus latch that stores the final binary level on the bus when left undriven.

Logic Symbol	Truth Table	Pin Loading
	N/A	Ci (pF): IO 0.10

Equivalent Gates:.....1.4
Bolt Syntax:.....IO .BL02;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.50	nA
†C_{pd}	0.26	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)
IO	IO	t_{PLH} t_{PHL}	0.46 0.63

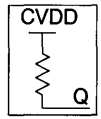
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CVDD

CYX 1.0 micron CMOS Standard Cells

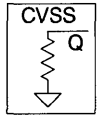
Description:
CVDD is the resistive tie-up to the core Vdd bus for all cell inputs.

Equivalent Gates:.....1.0
Bolt Syntax:..... Q .CVDD;



Description:
CVSS is the resistive tie-down to the core Vss bus for all cell inputs.

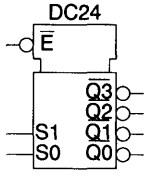
Equivalent Gates:.....1.0
Bolt Syntax: ..... Q .CVSS;



CYX 1.0 micron CMOS Standard Cells

Description:
DC24 is a two-to-four line decoder/demultiplexer with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Pin Loading

	Ci (pF)
S0	0.18
S1	0.17
EN	0.06

Equivalent Gates:.....6.9
Bolt Syntax:.....Q0N Q1N Q2N Q3N .DC24 EN S0 S1;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	12.72	nA
†C_{pd}	1.15	pF

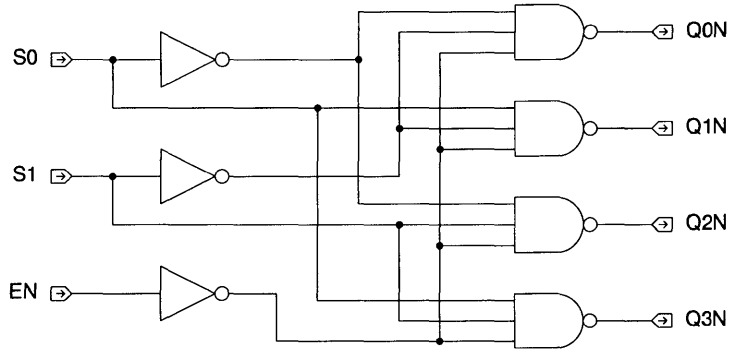
Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Sx	QN	t_{PLH}	0.50	1.31	0.69	0.88	1.28
		t_{PHL}	0.53	1.42	0.73	0.94	1.38
EN	QN	t_{PLH}	0.68	1.31	0.86	1.06	1.46
		t_{PHL}	0.68	1.42	0.88	1.10	1.53

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

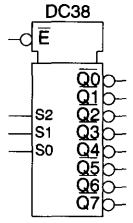


DC38

CYX 1.0 micron CMOS Standard Cells

Description:
DC38 is a three-to-eight line decoder/demultiplexer with active low enable.

Logic Symbol



Truth Table

Truth Table Appears On Next Page

Pin Loading

	Ci (pF)
S0	0.32
S1	0.30
S2	0.29
EN	0.06

Equivalent Gates:.....16.5
Bolt Syntax:.....Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N .DC38 EN S0 S1 S2;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	28.07	nA
†C_{pd}	2.64	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

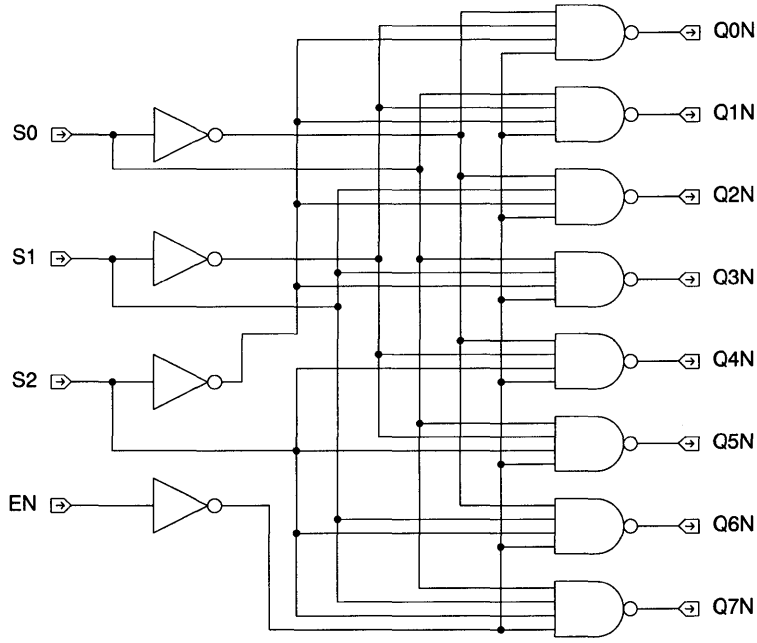
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Sx	QN	t_{PLH} t_{PHL}	0.78 0.80	0.89 1.02	0.90 0.94	1.04 1.09	1.31 1.40
EN	QN	t_{PLH} t_{PHL}	1.07 1.06	0.89 1.02	1.20 1.20	1.33 1.35	1.61 1.66

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

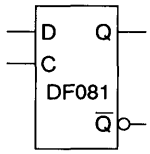
Logic Schematic



CYX 1.0 micron CMOS Standard Cells

Description:
DF081 is a static, master-slave D flip-flop without SET or RESET. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
H	↑	H	L
L	↑	L	H
X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.06
C	0.16

Equivalent Gates:.....3.8
Bolt Syntax:.....Q QN .DF081 C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.11	nA
†C_{pd}	0.77	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.59 0.29	1.93 1.35	0.87 0.48	1.15 0.68	1.74 1.09
C	QN	t_{PLH} t_{PHL}	0.60 0.81	1.21 1.07	0.77 0.96	0.95 1.12	1.32 1.45
Min C Width	High	t_w				1.12	
Min C Width	Low	t_w	0.76				
Min D Setup		t_{su}	0.76				
Min D Hold		t_h	0.00				

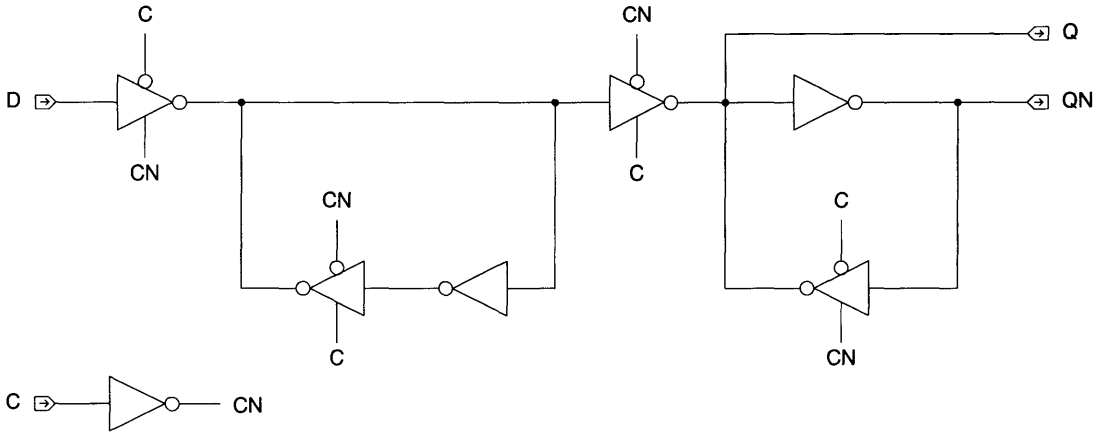
For Q Delays:

$$t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$$

For QN Delays:

$$t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{dr}(QN) + (k_{tdr}(QN)\ C_L(QN)) + (k_{tdf}(Q)\ C_L(Q))]$$
$$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{df}(QN) + (k_{tdf}(QN)\ C_L(QN)) + (k_{tdr}(Q)\ C_L(Q))]$$

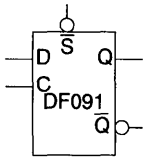
Logic Schematic



CYX 1.0 micron CMOS Standard Cells

Description:
DF091 is a static, master-slave D flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.06
C	0.18
SN	0.12

Equivalent Gates:.....4.7
Bolt Syntax:.....Q QN .DF091 C D SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.31	nA
†C_{pd}	0.95	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

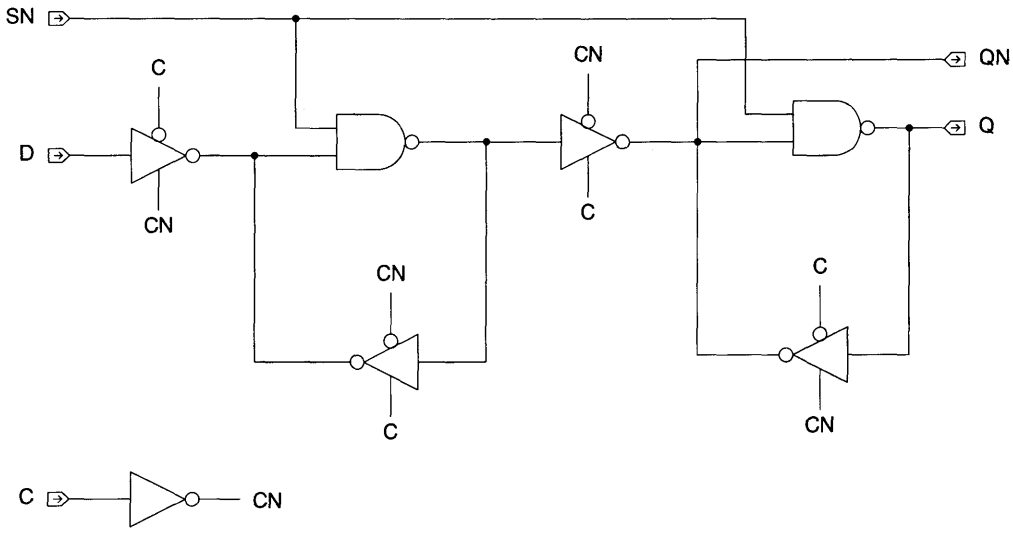
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.70 0.93	1.37 1.27	0.90 1.11	1.10 1.30	1.52 1.69
C	QN	t_{PLH} t_{PHL}	0.64 0.31	1.93 1.36	0.92 0.51	1.21 0.71	1.79 1.12
SN	Q	t_{PLH}	0.30	1.37	0.49	0.70	1.12
SN	QN	t_{PHL}	0.79	1.36	0.99	1.19	1.60
Min C Width	High	t_w				1.30	
Min C Width	Low	t_w	1.02				
Min SN Width	Low	t_w				1.19	
Min D Setup		t_{su}	0.79				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.27				
Min SN Hold		t_h	0.28				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

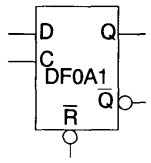


DF0A1

CYX 1.0 micron CMOS Standard Cells

Description:
DF0A1 is a static, master-slave D flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.06
C	0.18
RN	0.06

Equivalent Gates:.....5.4
Bolt Syntax:..... Q QN .DF0A1 C D RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.00	nA
†C_{pd}	1.11	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

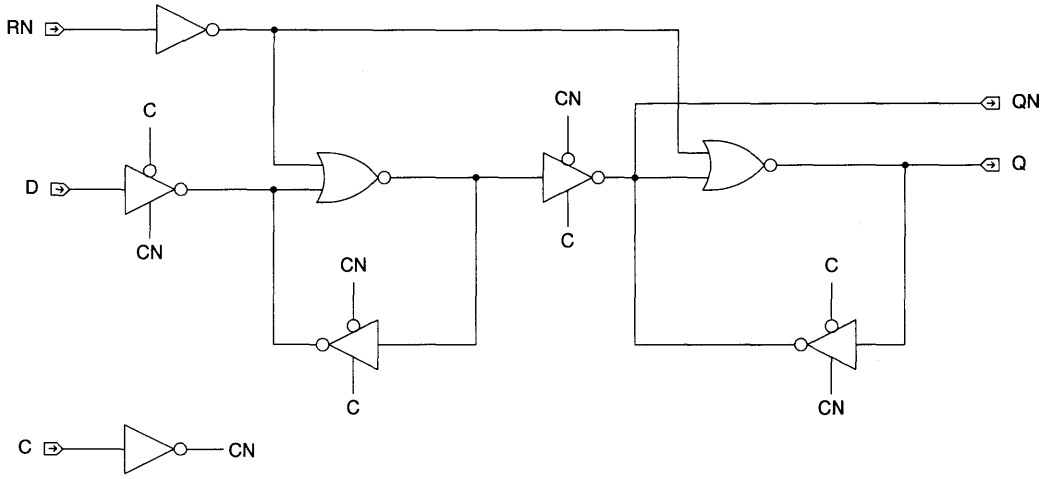
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.76 0.89	1.98 1.17	1.04 1.06	1.34 1.23	1.94 1.59
C	QN	t_{PLH} t_{PHL}	0.63 0.30	1.94 1.36	0.91 0.50	1.20 0.70	1.79 1.11
RN	Q	t_{PHL}	0.51	1.17	0.67	0.84	1.20
RN	QN	t_{PLH}	1.13	1.94	1.41	1.70	2.29
Min C Width	High	t_w				2.35	
Min C Width	Low	t_w	1.14				
Min RN Width	Low	t_w				1.70	
Min D Setup		t_{su}	0.88				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.74				
Min RN Hold		t_h	0.57				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

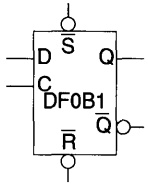
Logic Schematic



CYX 1.0 micron CMOS Standard Cells

Description:
DF0B1 is a static, master-slave D flip-flop. SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

NC = No Change
IL = Illegal

Pin Loading

	Ci (pF)
D	0.06
C	0.18
SN	0.12
RN	0.13

Equivalent Gates:.....6.5
Bolt Syntax:.....Q QN .DF0B1 C D RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.71	nA
†C_{pd}	1.25	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.72 0.98	1.40 1.27	0.92 1.16	1.13 1.35	1.56 1.74
C	QN	t_{PLH} t_{PHL}	0.69 0.32	1.94 1.36	0.96 0.51	1.25 0.72	1.84 1.13
RN	Q	t_{PHL}	1.44	1.27	1.62	1.81	2.20
RN	QN	t_{PLH}	1.15	1.94	1.42	1.71	2.30
SN	Q	t_{PLH}	0.31	1.40	0.51	0.71	1.14
SN	QN	t_{PHL}	0.96	1.36	1.16	1.36	1.77
Min C Width	High	t_w				1.35	
Min C Width	Low	t_w	1.13				
Min RN Width	Low	t_w				1.81	

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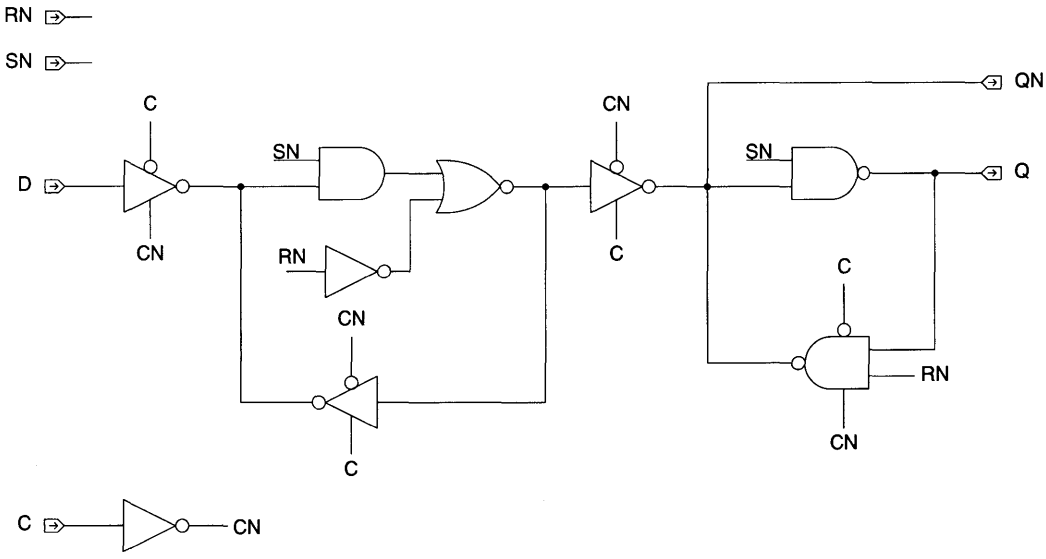
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min SN Width	Low	t_w				1.36	
Min D Setup		t_{su}	0.98				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.26				
Min RN Hold		t_h	0.57				
Min SN Setup		t_{su}	0.42				
Min SN Hold		t_h	0.27				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

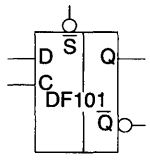
Logic Schematic



CYX 1.0 micron CMOS Standard Cells

Description:
DF101 is a static, master-slave D flip-flop. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.06
C	0.17
SN	0.12

Equivalent Gates:.....5.9
Bolt Syntax:.....Q QN .DF101 C D SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.39	nA
†C_{pd}	1.05	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.60 0.84	1.25 1.14	0.78 1.01	0.96 1.18	1.34 1.52
C	QN	t_{PLH} t_{PHL}	1.24 0.95	1.19 0.95	1.41 1.09	1.59 1.23	1.95 1.52
SN	Q	t_{PLH}	1.11	1.25	1.28	1.47	1.85
SN	QN	t_{PHL}	0.52	0.95	0.65	0.79	1.08
Min C Width	High	t_w	1.04				
Min C Width	Low	t_w	0.81				
Min SN Width		t_w	1.03				
Min D Setup		t_{su}	0.71				
Min D Hold		t_h	0.00				

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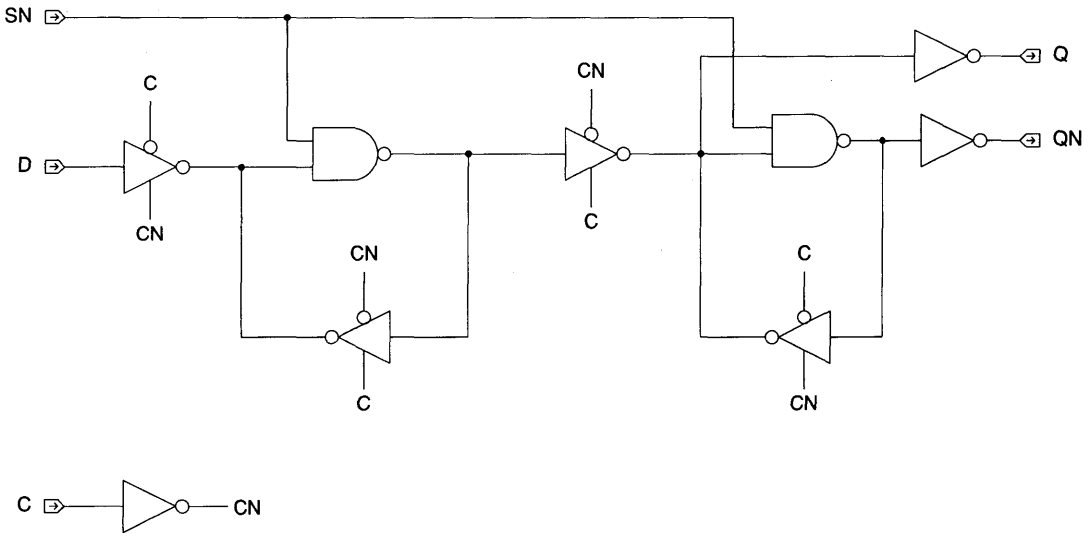
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min SN Setup		t_{su}	0.23				
Min SN Hold		t_h	0.58				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

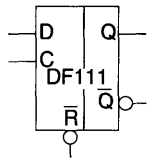


DF111

CYX 1.0 micron CMOS Standard Cells

Description:
DF111 is a static, master-slave D flip-flop. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.06
C	0.17
RN	0.07

Equivalent Gates:.....7.3

Bolt Syntax:..... Q QN .DF111 C D RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.10	nA
†C_{pd}	1.25	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

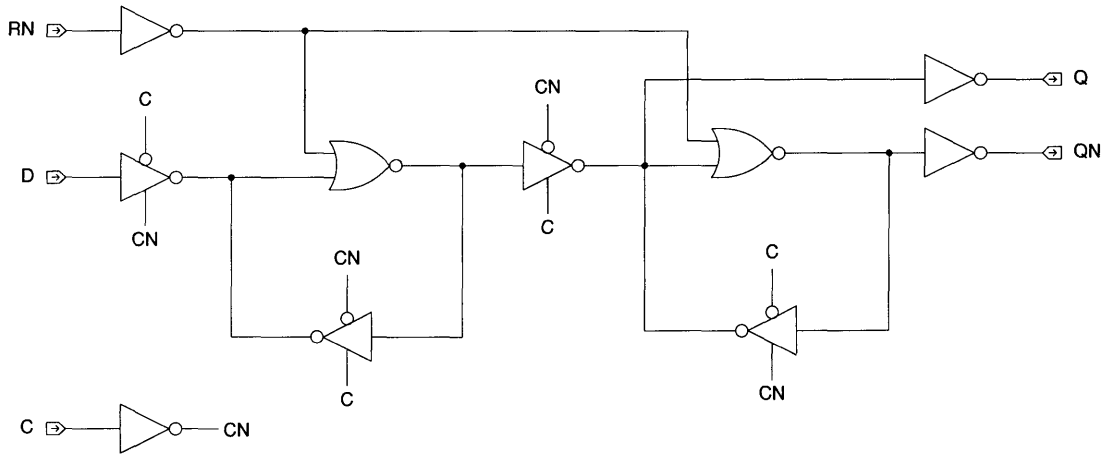
Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.59 0.86	1.24 1.16	0.77 1.02	0.95 1.20	1.33 1.55
C	QN	t_{PLH} t_{PHL}	1.24 1.09	1.13 1.08	1.40 1.25	1.57 1.41	1.91 1.74
RN	Q	t_{PHL}	1.37	1.16	1.54	1.71	2.06
RN	QN	t_{PLH}	0.76	1.13	0.92	1.09	1.43
Min C Width	High	t_w	1.04				
Min C Width	Low	t_w	0.91				
Min RN Width		t_w	2.12				
Min D Setup		t_{su}	0.76				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.37				
Min RN Hold		t_h	1.40				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

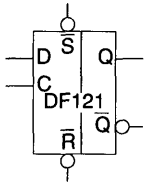


DF121

CYX 1.0 micron CMOS Standard Cells

Description:
DF121 is a static, master-slave D flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL=Illegal NC=No Change

Pin Loading

	Ci (pF)
D	0.06
C	0.17
SN	0.12
RN	0.13

Equivalent Gates:.....8.0
Bolt Syntax:.....Q QN .DF121 C D RN SN;
Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.81	nA
†C_{pd}	1.37	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.61 0.89	1.25 1.16	0.79 1.05	0.98 1.22	1.36 1.58
C	QN	t_{PLH} t_{PHL}	1.33 0.99	1.20 0.97	1.50 1.13	1.68 1.28	2.04 1.57
SN	Q	t_{PLH}	1.25	1.25	1.43	1.62	2.00
SN	QN	t_{PHL}	0.53	0.97	0.67	0.81	1.11
RN	Q	t_{PHL}	1.33	1.16	1.50	1.67	2.02
RN	QN	t_{PLH}	1.78	1.20	1.95	2.12	2.49
Min C Width	High	t_w	1.11				
Min C Width	Low	t_w	0.88				
Min RN Width	Low	t_w	2.05				
Min SN Width	Low	t_w	1.07				

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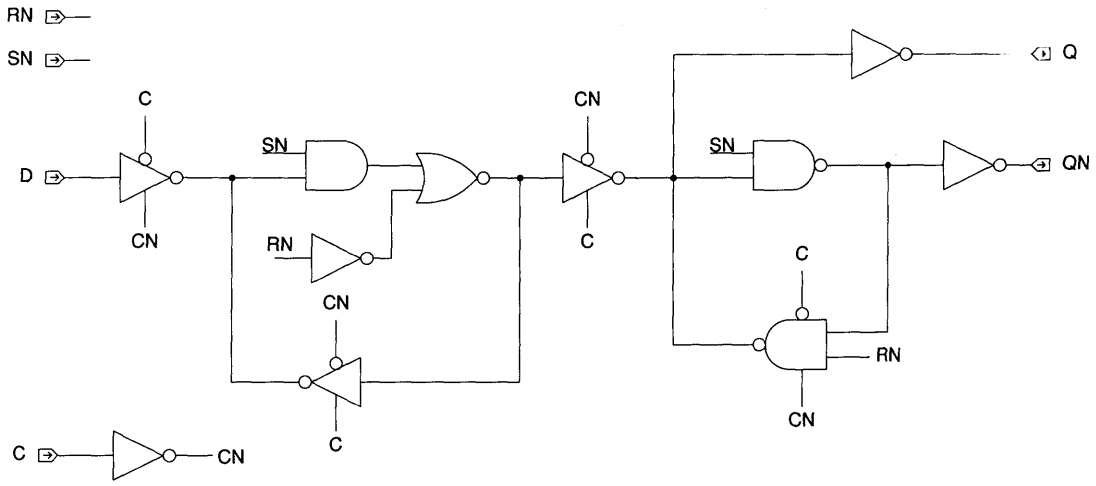
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min D Setup		t_{su}	0.86				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.67				
Min RN Hold		t_h	1.30				
Min SN Setup		t_{su}	0.36				
Min SN Hold		t_h	0.54				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

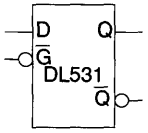


DL531

CYX 1.0 micron CMOS Standard Cells

Description:
DL531 is a single-phase, unbuffered D latch with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

GN	D	Q	QN
L	L	L	H
L	H	H	L
H	X	NC	NC

NC=No Change

Pin Loading

	Ci (pF)
D	0.06
GN	0.12

Equivalent Gates:.....2.2
Bolt Syntax:.....Q QN .DL531 D GN;
Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.93	nA
†C_{pd}	0.43	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

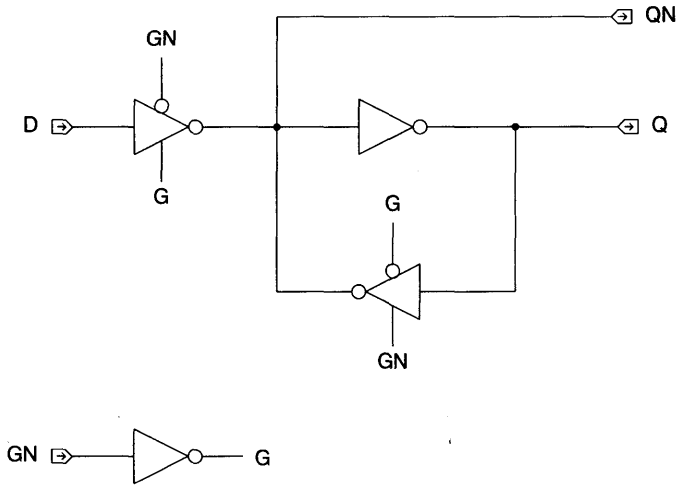
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
D	Q	t_{PLH} t_{PHL}	0.67 0.70	1.20 1.08	0.84 0.85	1.02 1.01	1.39 1.34
D	QN	t_{PLH} t_{PHL}	0.48 0.36	1.99 1.36	0.76 0.55	1.06 0.75	1.67 1.17
GN	Q	t_{PLH} t_{PHL}	0.83 0.57	1.20 1.08	1.00 0.72	1.18 0.88	1.54 1.21
GN	QN	t_{PLH} t_{PHL}	0.35 0.52	1.99 1.36	0.63 0.71	0.93 0.91	1.53 1.32
Min GN Width	Low	t_w				1.18	
Min D Setup		t_{su}				1.02	
Min D Hold		t_h	0.00				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

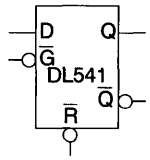
Logic Schematic



CYX 1.0 micron CMOS Standard Cells

Description:
DL541 is a single-phase, unbuffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC=No Change

Pin Loading

	Ci (pF)
D	0.06
GN	0.10
RN	0.06

Equivalent Gates:.....3.5
Bolt Syntax:.....Q QN .DL541 D GN RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.10	nA
†C_{pd}	0.59	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
D	Q	t_{PLH} t_{PHL}	0.77 0.74	1.98 1.01	1.05 0.88	1.35 1.03	1.95 1.34
D	QN	t_{PLH} t_{PHL}	0.92 0.92	1.14 1.11	1.08 1.08	1.25 1.24	1.60 1.58
GN	Q	t_{PLH} t_{PHL}	0.82 0.61	1.98 1.01	1.10 0.75	1.40 0.90	2.00 1.21
GN	QN	t_{PLH} t_{PHL}	0.79 0.97	1.14 1.11	0.95 1.12	1.12 1.29	1.47 1.63
RN	Q	t_{PHL}	0.43	1.01	0.57	0.72	1.03
RN	QN	t_{PLH}	0.61	1.14	0.78	0.95	1.29
Min GN Width	Low	t_w				1.40	
Min RN Width	Low	t_w				2.38	
Min D Setup		t_{su}				1.35	

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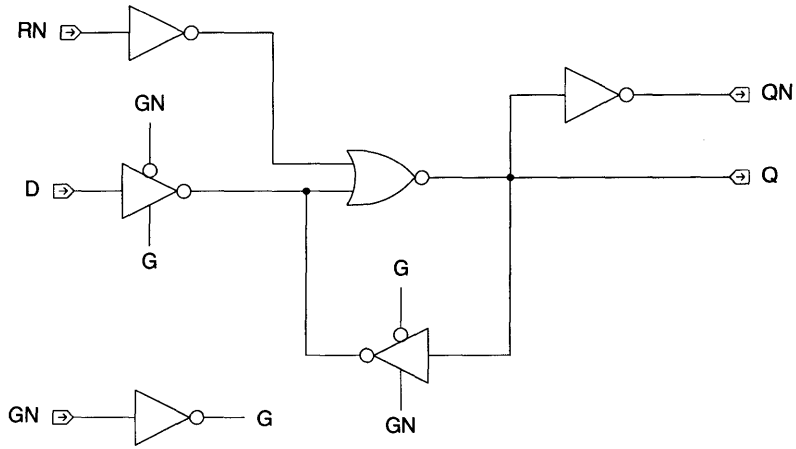
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.58				
Min RN Hold		t_h	1.40				

For Q Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} * C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{dr}(QN) + (k_{tdr}(QN)\ C_L(QN)) + (k_{tdf}(Q)\ C_L(Q))]$

Logic Schematic

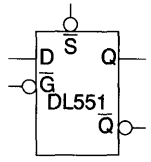


DL551

CYX 1.0 micron CMOS Standard Cells

Description:
DL551 is a single-phase, unbuffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC=No Change

Pin Loading

	Ci (pF)
D	0.06
GN	0.10
SN	0.07

Equivalent Gates:.....3.0
Bolt Syntax:.....Q QN .DL551 D GN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.77	nA
†C_{pd}	0.47	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
D	Q	t_{PLH} t_{PHL}	0.67 0.71	1.32 1.12	0.86 0.87	1.05 1.04	1.46 1.38
D	QN	t_{PLH} t_{PHL}	0.91 0.80	1.20 0.98	1.08 0.94	1.26 1.09	1.63 1.39
GN	Q	t_{PLH} t_{PHL}	0.72 0.58	1.32 1.12	0.91 0.74	1.10 0.91	1.51 1.25
GN	QN	t_{PLH} t_{PHL}	0.78 0.85	1.20 0.98	0.95 0.99	1.13 1.14	1.50 1.44
SN	Q	t_{PLH}	0.33	1.32	0.52	0.71	1.12
SN	QN	t_{PHL}	0.47	0.98	0.61	0.75	1.05
Min GN Width	Low	t_w				1.10	
Min SN Width	Low	t_w				1.40	
Min D Setup		t_{su}				1.05	

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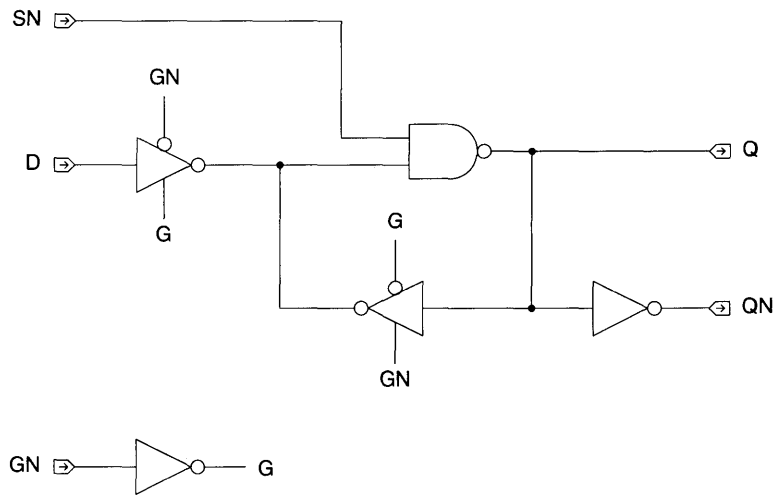
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.23				
Min SN Hold		t_h	0.70				

For Q Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} * C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{dr}(QN) + (k_{tdr}(QN)\ C_L(QN)) + (k_{tdf}(Q)\ C_L(Q))]$
$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{df}(QN) + (k_{tdf}(QN)\ C_L(QN)) + (k_{tdr}(Q)\ C_L(Q))]$

Logic Schematic



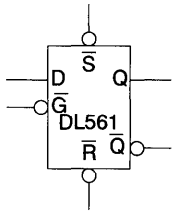
DL561

AMI SEMICONDUCTORS

CYX 1.0 micron CMOS Standard Cells

Description:
DL561 is a single-phase, unbuffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

NC=No Change IL = Illegal

Pin Loading

	Ci (pF)
D	0.07
GN	0.11
SN	0.06
RN	0.06

Equivalent Gates:.....3.6
Bolt Syntax:.....Q QN .DL561 D GN RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.72	nA
†C_{pd}	0.54	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
D	Q	t_{PLH} t_{PHL}	0.80 0.84	1.36 1.17	1.00 1.01	1.20 1.18	1.61 1.54
D	QN	t_{PLH} t_{PHL}	1.39 1.26	1.32 1.18	1.57 1.43	1.77 1.60	2.17 1.96
GN	Q	t_{PLH} t_{PHL}	0.82 0.68	1.36 1.17	1.01 0.84	1.21 1.02	1.63 1.37
GN	QN	t_{PLH} t_{PHL}	0.88 0.95	1.32 1.18	1.07 1.11	1.27 1.29	1.67 1.65
SN	Q	t_{PLH}	0.33	1.36	0.52	0.72	1.14
SN	QN	t_{PHL}	0.46	1.18	0.63	0.81	1.17
RN	Q	t_{PHL}	0.59	1.17	0.76	0.93	1.29
RN	QN	t_{PLH}	0.79	1.32	0.98	1.18	1.58
Min GN Width	Low	t_w				1.21	

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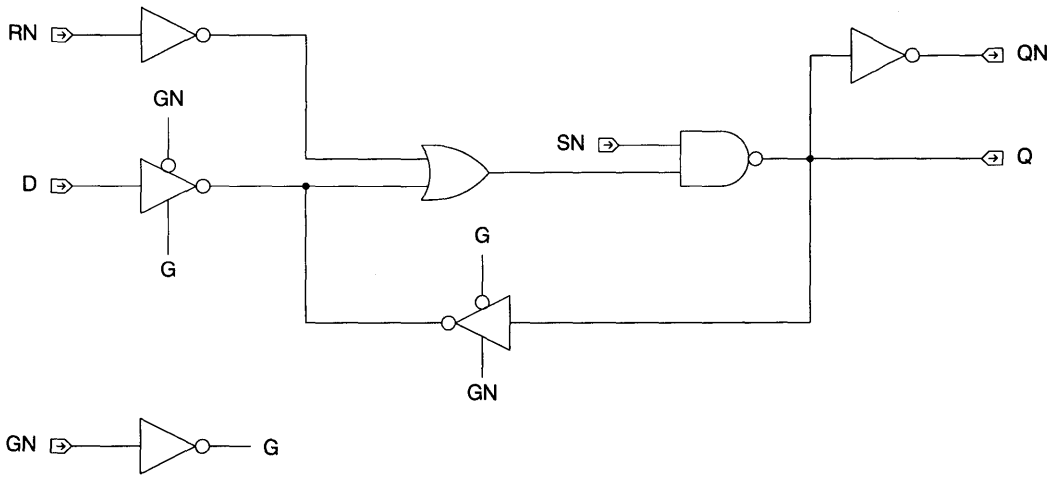
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min RN Width	Low	t_w				0.93	
Min SN Width	Low	t_w				1.26	
Min D Setup		t_{su}				1.20	
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.23				
Min SN Hold		t_h	0.89				
Min RN Setup		t_{su}	0.85				
Min RN Hold		t_h	0.20				

For Q Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} * C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{dr}(QN) + (k_{tdr}(QN)\ C_L(QN)) + (k_{tdf}(Q)\ C_L(Q))]$

$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{df}(QN) + (k_{tdf}(QN)\ C_L(QN)) + (k_{tdr}(Q)\ C_L(Q))]$

Logic Schematic

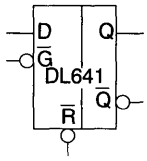


1.0 micron Mixed Signal

CYX 1.0 micron CMOS Standard Cells

Description:
DL641 is a single-phase, buffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC=No Change

Pin Loading

	Ci (pF)
D	0.06
GN	0.10
RN	0.06

Equivalent Gates:.....4.5
Bolt Syntax:.....Q QN .DL641 D GN RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.00	nA
†C_{pd}	0.82	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
D	Q	t_{PLH} t_{PHL}	1.20 1.11	1.11 0.82	1.36 1.23	1.52 1.35	1.86 1.60
D	QN	t_{PLH} t_{PHL}	0.94 1.01	1.16 1.13	1.10 1.17	1.27 1.34	1.63 1.68
GN	Q	t_{PLH} t_{PHL}	1.25 0.98	1.11 0.82	1.41 1.10	1.58 1.22	1.92 1.47
GN	QN	t_{PLH} t_{PHL}	0.81 1.06	1.16 1.13	0.97 1.22	1.14 1.39	1.50 1.73
RN	Q	t_{PHL}	0.84	0.82	0.96	1.08	1.33
RN	QN	t_{PLH}	0.67	1.16	0.83	1.00	1.35
Min GN Width	High	t_w	0.35				
Min GN Width	Low	t_h	0.91				
Min RN Width	Low	t_w	2.06				

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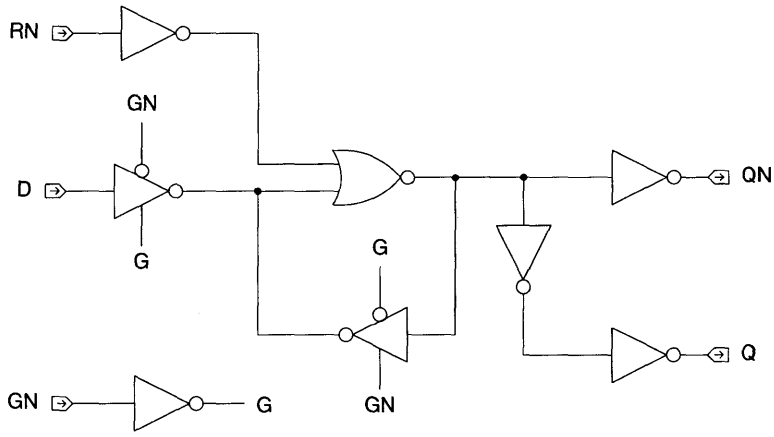
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min D Setup		t_{su}	0.87				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.71				
Min RN Hold		t_h	1.31				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



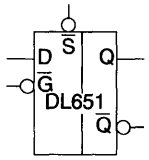
DL651

AMI SEMICONDUCTORS

CYX 1.0 micron CMOS Standard Cells

Description:
DL651 is a single-phase, buffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC=No Change

Pin Loading

	Ci (pF)
D	0.07
GN	0.11
SN	0.06

Equivalent Gates:.....4.2
Bolt Syntax:.....Q QN .DL651 D GN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.67	nA
†C_{pd}	0.68	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

10 micron Mixed Signal

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
D	Q	t_{PLH} t_{PHL}	1.07 1.15	1.12 0.83	1.22 1.27	1.39 1.39	1.73 1.65
D	QN	t_{PLH} t_{PHL}	0.97 0.89	1.21 0.98	1.14 1.03	1.32 1.17	1.69 1.47
GN	Q	t_{PLH} t_{PHL}	1.11 1.02	1.12 0.83	1.27 1.14	1.44 1.26	1.78 1.52
GN	QN	t_{PLH} t_{PHL}	0.84 0.93	1.21 0.98	1.01 1.07	1.19 1.22	1.56 1.52
SN	Q	t_{PLH}	0.71	1.12	0.87	1.03	1.37
SN	QN	t_{PHL}	0.53	0.98	0.67	0.82	1.12
Min GN Width	High	t_w	0.33				
Min GN Width	Low	t_h	0.80				
Min SN Width	Low	t_w	1.13				

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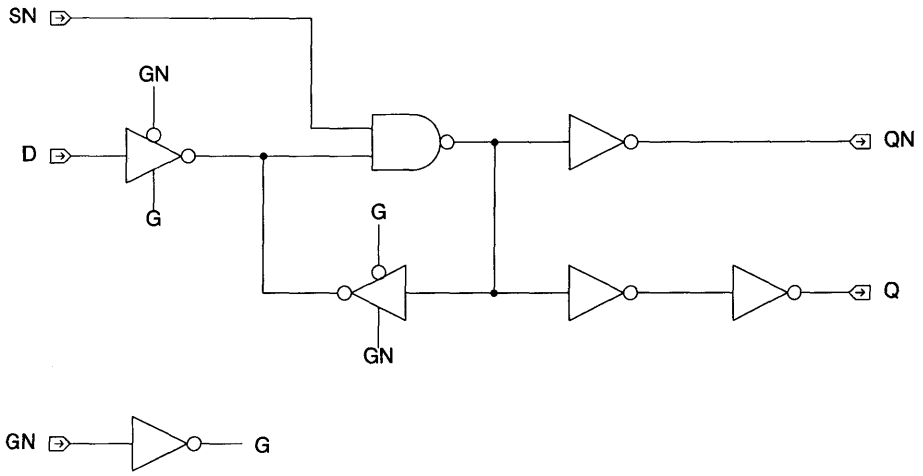
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min D Setup		t_{su}	0.78				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.59				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

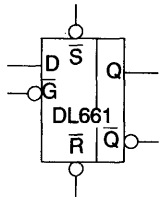


AMI SEMICONDUCTORS

CYX 1.0 micron CMOS Standard Cells

Description:
DL661 is a single-phase, buffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL=Illegal NC=No Change

Pin Loading

	Ci (pF)
D	0.07
GN	0.11
SN	0.06
RN	0.06

Equivalent Gates:.....4.9
Bolt Syntax:.....Q QN .DL661 D GN RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.63	nA
†C_{pd}	0.78	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
D	Q	t_{PLH} t_{PHL}	1.21 1.29	1.11 0.82	1.37 1.41	1.54 1.53	1.88 1.79
D	QN	t_{PLH} t_{PHL}	1.12 1.04	1.22 1.00	1.30 1.18	1.48 1.33	1.85 1.64
GN	Q	t_{PLH} t_{PHL}	1.23 1.13	1.11 0.82	1.38 1.25	1.55 1.37	1.89 1.62
GN	QN	t_{PLH} t_{PHL}	0.96 1.05	1.22 1.00	1.13 1.20	1.31 1.35	1.68 1.65
SN	Q	t_{PLH}	0.73	1.11	0.89	1.06	1.40
SN	QN	t_{PHL}	0.56	1.00	0.70	0.85	1.16
RN	Q	t_{PHL}	1.13	0.82	1.25	1.37	1.62
RN	QN	t_{PLH}	0.96	1.22	1.14	1.32	1.69
Min GN Width	High	t_w	0.33				

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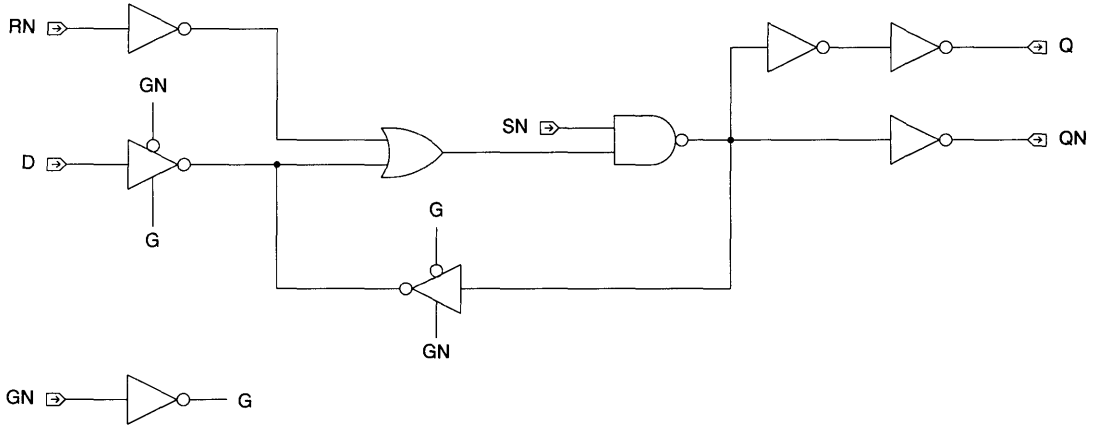
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min GN Width	Low	t_w	0.91				
Min RN Width	Low	t_w	0.62				
Min SN Width	Low	t_w	1.37				
Min D Setup		t_{su}	0.91				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.29				
Min SN Hold		t_h	0.78				
Min RN Setup		t_{su}	0.95				
Min RN Hold		t_h	0.20				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

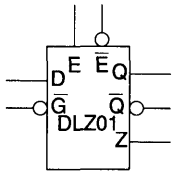
Logic Schematic



CYX 1.0 micron CMOS Standard Cells

Description:
DLZ01 is a single-phase, unbuffered D latch with active low gate transparency and with a dual-enable tri-state output.

Logic Symbol



Truth Table

D	GN	E	EN	Q	QN	Z
L	L	H	X	L	H	L
H	L	X	L	H	L	H
L	L	L	X	L	H	Z
H	L	X	H	H	L	Z
X	H	H	L	NC	NC	NC
X	H	L	H	NC	NC	Z

Z = High Impedance NC=No Change

Pin Loading

	Ci (pF)
D	0.06
GN	0.12
E	0.03
EN	0.04
Z	0.06

Equivalent Gates:.....3.5
Bolt Syntax:.....Q QN Z .DLZ01 D E EN GN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.08	nA
$^{\dagger}C_{pd}$	0.66	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
D	Q	t_{PLH} t_{PHL}	0.82 0.92	1.18 1.21	0.99 1.09	1.17 1.28	1.53 1.64
D	QN	t_{PLH} t_{PHL}	0.64 0.47	1.98 1.36	0.92 0.66	1.22 0.87	1.82 1.28
D	Z	t_{PLH} t_{PHL}	0.88 0.94	1.99 1.51	1.16 1.15	1.46 1.38	2.07 1.84
GN	Q	t_{PLH} t_{PHL}	0.96 0.76	1.18 1.21	1.13 0.93	1.30 1.11	1.66 1.48
GN	QN	t_{PLH} t_{PHL}	0.48 0.61	1.98 1.36	0.76 0.80	1.05 1.00	1.66 1.42
GN	Z	t_{PLH} t_{PHL}	1.02 0.77	1.99 1.51	1.30 0.99	1.59 1.21	2.20 1.67
E	Z	t_{PLZ} t_{PZL}	0.12 0.21				

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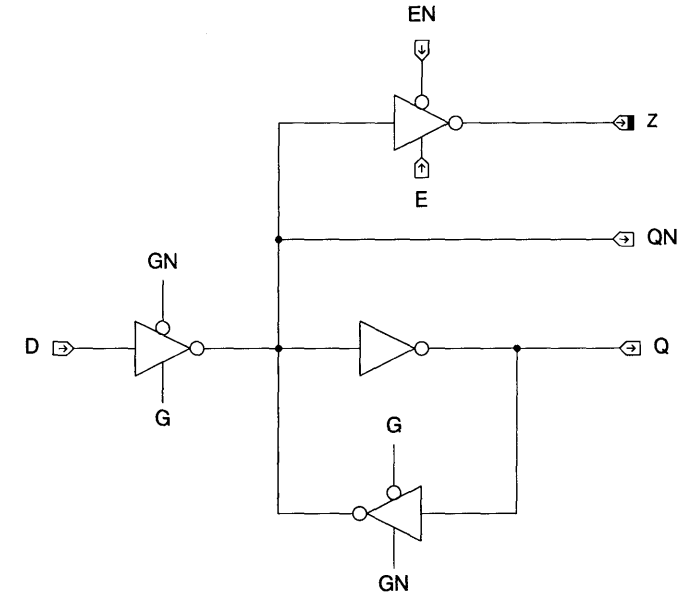
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
EN	Z	t_{PHZ} t_{PZH}	0.17 0.17				
Min GN Width	Low	t_w				1.28	
Min D Setup		t_{su}				1.28	
Min D Hold		t_h	0.00				

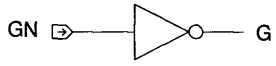
For Q Delays:
$t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays:
$t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

For Z Delays:
$t_{plh}(C_{L(Z)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Z) + (K_{tdr}(Z) * C_L(Z)) + (K_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Z)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Z) + (K_{tdf}(Z) * C_L(Z)) + (K_{tdr}(QN) * C_L(QN))]$

Logic Schematic

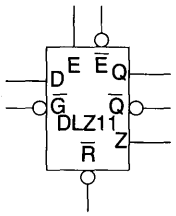




CYX 1.0 micron CMOS Standard Cells

Description:
DLZ11 is a single-phase, unbuffered D latch with active low gate transparency and with a dual-enable tri-state output. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	E	EN	Q	QN	Z
H	L	L	H	X	L	H	L
H	H	L	X	L	H	L	H
H	L	L	L	X	L	H	Z
H	H	L	X	H	H	L	Z
H	X	H	H	L	NC	NC	NC
H	X	H	L	H	NC	NC	Z
L	X	X	H	L	L	H	L
L	X	X	L	H	L	H	Z

Z = High Impedance NC=No Change

Pin Loading

	Ci (pF)
D	0.07
GN	0.12
RN	0.07
E	0.03
EN	0.04
Z	0.07

Equivalent Gates:.....4.3
Bolt Syntax:.....Q QN Z .DLZ11 D E EN GN RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.10	nA
†C_{pd}	0.73	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
D	Q	t_{PLH} t_{PHL}	1.13 1.01	1.31 1.25	1.32 1.19	1.51 1.38	1.92 1.76
D	QN	t_{PLH} t_{PHL}	0.72 0.69	1.98 1.84	1.00 0.95	1.30 1.23	1.90 1.79
GN	Q	t_{PLH} t_{PHL}	1.19 0.88	1.31 1.25	1.38 1.06	1.57 1.24	1.98 1.62
GN	QN	t_{PLH} t_{PHL}	0.59 0.75	1.98 1.84	0.87 1.01	1.16 1.29	1.77 1.85
RN	Q	t_{PHL}	0.69	1.25	0.87	1.05	1.44
RN	QN	t_{PLH}	0.41	1.98	0.69	0.99	1.59
RN	Z	t_{PHL} t_{PLH}	0.70 1.26	1.54 2.02	0.92 1.54	1.15 1.84	1.62 2.46

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Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
D	Z	t_{PLH} t_{PHL}	1.19 1.03	2.02 1.54	1.48 1.24	1.78 1.47	2.39 1.94
GN	Z	t_{PLH} t_{PHL}	1.25 0.89	2.02 1.54	1.54 1.11	1.84 1.34	2.45 1.81
E	Z	t_{PLZ} t_{PZL}	0.12 0.21				
EN	Z	t_{PHZ} t_{PZH}	0.17 0.17				
Min GN Width	Low	t_w				1.57	
Min RN Width	Low	t_w				1.05	
Min D Setup		t_{su}				1.51	
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	1.20				
Min RN Hold		t_h	0.28				

For Q Delays:

$$t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$$
$$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$$

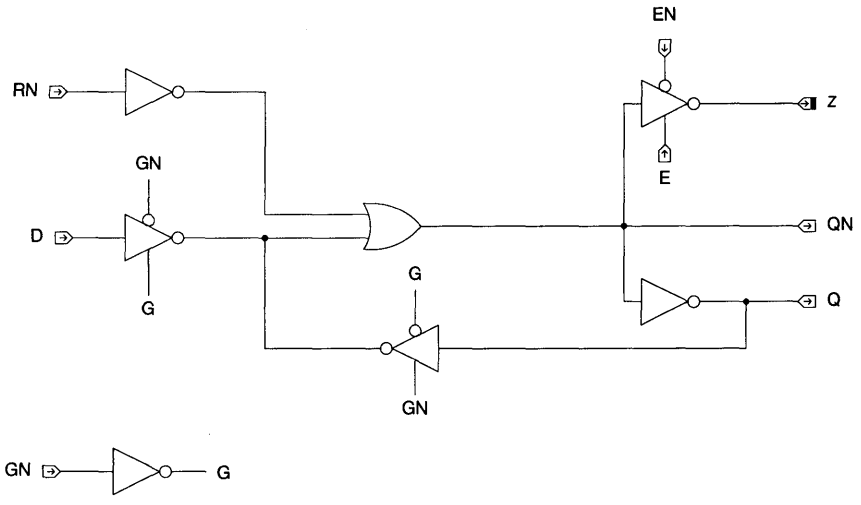
For QN Delays:

$$t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$$

For Z Delays:

$$t_{plh}(C_{L(Z)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Z) + (K_{tdr}(Z) * C_L(Z)) + (K_{tdf}(QN) * C_L(QN))]$$
$$t_{phl}(C_{L(Z)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Z) + (K_{tdf}(Z) * C_L(Z)) + (K_{tdr}(QN) * C_L(QN))]$$

Logic Schematic

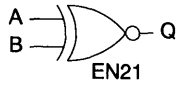


EN21

CYX 1.0 micron CMOS Standard Cells

Description:
EN21 is a 2-input gate which performs the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

Pin Loading

	Ci (pF)
A	0.12
B	0.11

Equivalent Gates:.....1.9
Bolt Syntax:.....Q .EN21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.29	nA
†C_{pd}	0.27	pF

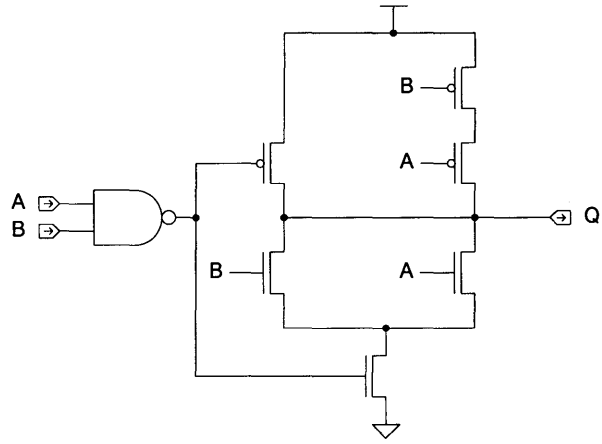
Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

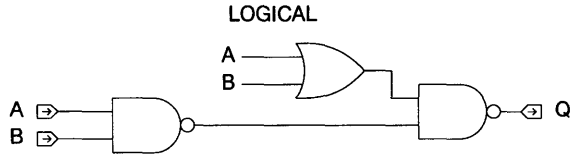
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.36	2.47	0.71	1.08	1.83
		t_{PHL}	0.50	1.03	0.64	0.79	1.11

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

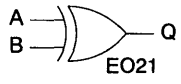




CYX 1.0 micron CMOS Standard Cells

Description:
EO21 is a 2-input gate which performs the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

Pin Loading

	Ci (pF)
A	0.12
B	0.12

Equivalent Gates:.....1.9
Bolt Syntax:.....Q .EO21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.04	nA
†C_{pd}	0.30	pF

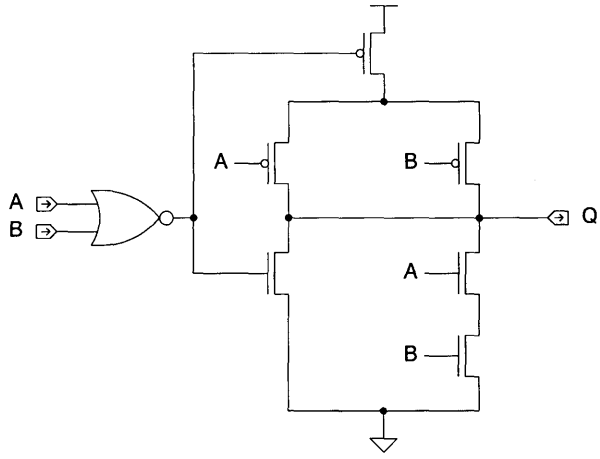
Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

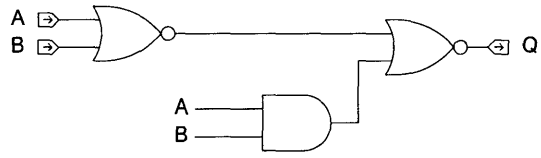
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.58	1.97	0.86	1.16	1.76
		t_{PHL}	0.67	0.94	0.81	0.95	1.23

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



LOGICAL

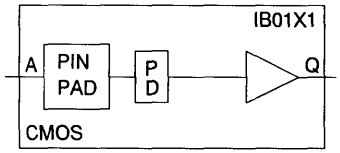


IB01X1

CYX 1.0 micron CMOS Standard Cells

Description:
IB01X1 is a non-inverting, CMOS-level input buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	5.20

Bolt Syntax: ..... Q .IB01X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.04	nA
†C_{pd}	0.24	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

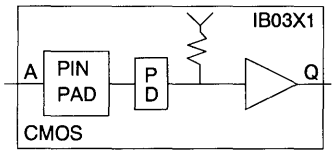
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.61	0.87	0.74	0.87	1.14
		t_{PHL}	0.46	0.73	0.57	0.67	0.90

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IB03X1 is a non-inverting, CMOS-level input buffer pad with pull-up.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	5.47

Bolt Syntax: .....Q .IB03X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.55	nA
†C_{pd}	0.20	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

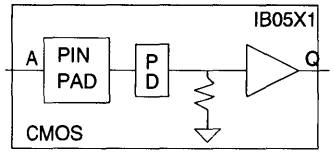
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.57	0.85	0.69	0.87	1.08
		t_{PHL}	0.43	0.69	0.53	0.63	0.84

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
IB05X1 is a non-inverting, CMOS-level input buffer pad with pull-down.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	5.45

Bolt Syntax: ..... Q .IB05X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.23	nA
†C_{pd}	0.21	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

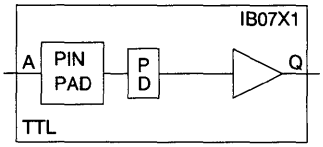
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.58	0.86	0.70	0.83	1.09
		t_{PHL}	0.44	0.70	0.54	0.65	0.86

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IB07X1 is a non-inverting, TTL-level input buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	5.19

Bolt Syntax: ..... Q .IB07X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.18	nA
†C_{pd}	0.18	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

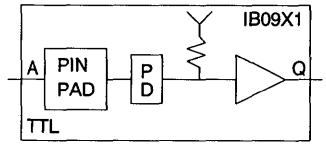
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.67	1.16	0.84	1.01	1.36
		t_{PHL}	0.61	0.82	0.73	0.85	1.10

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
IB09X1 is a non-inverting, TTL-level input buffer pad with pull-up.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	5.43

Bolt Syntax: ..... Q .IB09X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.69	nA
†C_{pd}	0.17	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

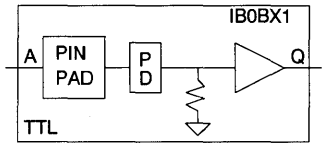
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.66	1.15	0.82	0.99	1.34
		t_{PHL}	0.59	0.81	0.71	0.83	1.07

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IB0BX1 is a non-inverting, TTL-level input buffer pad with pull-down.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	5.43

Bolt Syntax: ..... Q .IB0BX1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.37	nA
†C_{pd}	0.18	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.67	1.16	0.83	1.01	1.36
		t_{PHL}	0.61	0.82	0.73	0.85	1.10

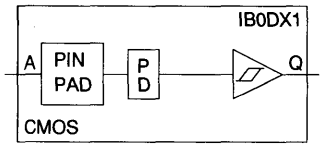
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IB0DX1

CYX 1.0 micron CMOS Standard Cells

Description:
IB0DX1 is a non-inverting, CMOS-level Schmitt trigger input buffer pad with voltage hysteresis.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	5.18

Bolt Syntax: ..... Q .IB0DX1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.48	nA
†C_{pd}	0.42	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

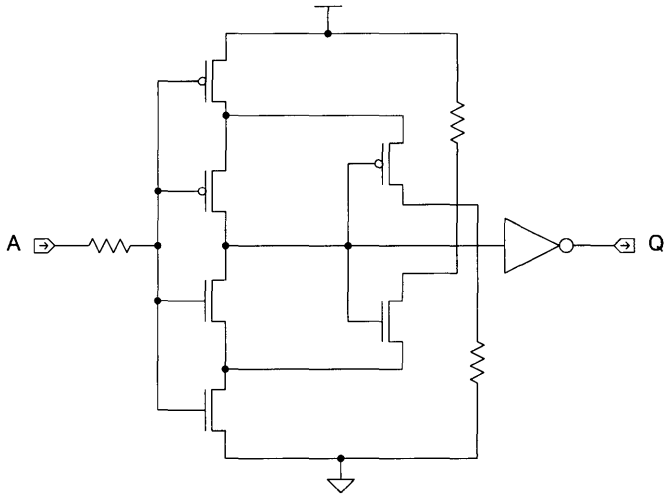
Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	2.02	1.02	2.17	2.32	2.63
		t_{PHL}	1.65	0.84	1.77	1.89	2.15

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

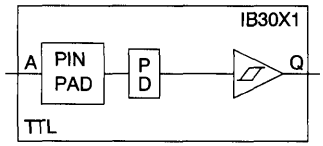
Logic Schematic



CYX 1.0 micron CMOS Standard Cells

Description:
IB30X1 is a non-inverting, TTL-level Schmitt trigger input buffer pad with voltage hysteresis.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	5.31

Bolt Syntax: .....Q .IB30X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.57	nA
†C_{pd}	0.40	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

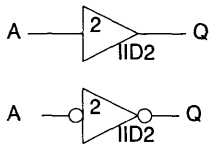
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	1.45	1.23	1.62	1.81	2.18
		t_{PHL}	1.53	1.20	1.70	1.88	2.24

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IID2 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.11

Equivalent Gates:.....1.6
Bolt Syntax:.....Q .IID2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.80	nA
†C_{pd}	0.23	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

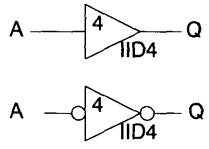
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.23	0.57	0.31	0.39	0.57
		t_{PHL}	0.25	0.45	0.32	0.38	0.52

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
IID4 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.11

Equivalent Gates:.....2.2
Bolt Syntax:.....Q .IID4 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.70	nA
†C_{pd}	0.39	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

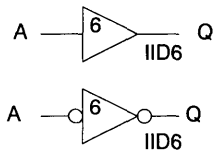
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.29	0.31	0.33	0.38	0.47
		t_{PHL}	0.32	0.28	0.36	0.40	0.49

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IID6 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.11

Equivalent Gates:.....2.6
Bolt Syntax:.....Q .IID6 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.60	nA
†C_{pd}	0.58	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.35	0.22	0.38	0.41	0.48
		t_{PHL}	0.39	0.22	0.42	0.45	0.52

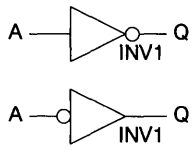
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

INV1

CYX 1.0 micron CMOS Standard Cells

Description:
INV1 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.06

Equivalent Gates:.....0.8
Bolt Syntax:.....Q .INV1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.95	nA
†C_{pd}	0.06	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

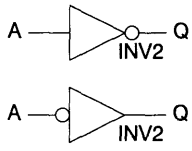
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.14	1.12	0.30	0.46	0.81
		t_{PHL}	0.12	0.85	0.24	0.36	0.62

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
INV2 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.11

Equivalent Gates:.....1.0
Bolt Syntax:.....Q .INV2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.90	nA
†C_{pd}	0.13	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.14	0.57	0.22	0.30	0.48
		t_{PHL}	0.11	0.47	0.18	0.25	0.39

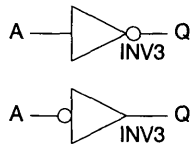
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

INV3

CYX 1.0 micron CMOS Standard Cells

Description:
INV3 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.16

Equivalent Gates:..... 1.4
Bolt Syntax:..... Q .INV3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.85	nA
†C_{pd}	0.13	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

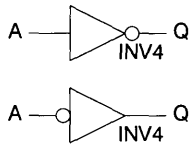
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.12	0.40	0.17	0.23	0.35
		t_{PHL}	0.09	0.34	0.14	0.19	0.29

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

1.0 micron Mixed Signal

Description:
INV4 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.22

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .INV4 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.80	nA
†C_{pd}	0.13	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.11	0.31	0.15	0.20	0.29
		t_{PHL}	0.08	0.28	0.12	0.16	0.24

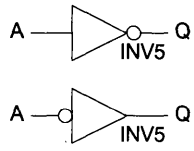
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

INV5

CYX 1.0 micron CMOS Standard Cells

Description:
INV5 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.26

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .INV5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.75	nA
†C_{pd}	0.16	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

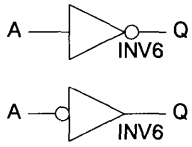
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.11	0.25	0.14	0.18	0.26
		t_{PHL}	0.08	0.23	0.11	0.14	0.21

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
INV6 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.32

Equivalent Gates:.....2.0
Bolt Syntax:.....Q .INV6 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.70	nA
†C_{pd}	0.22	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.11	0.21	0.14	0.17	0.24
		t_{PHL}	0.08	0.19	0.11	0.14	0.20

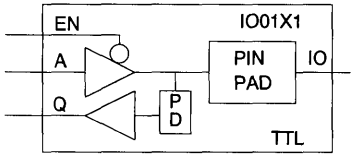
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IO01X1

CYX 1.0 micron CMOS Standard Cells

Description:
IO01X1 is a 1mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.46

Bolt Syntax: .....IO Q .IO01X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	19.85	nA
†C_{pd}	8.14	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

10 micron Mixed Signal

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.67	1.15	0.84	1.01	1.36
		t_{PHL}	0.61	0.83	0.73	0.85	1.10

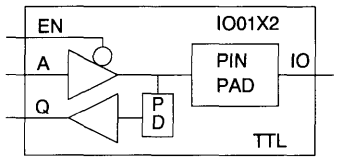
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.00	0.32	8.09	16.17	24.26	32.34
		t_{PHL}	0.00	0.41	10.29	20.58	30.87	41.15
EN	IO	t_{HZ}	0.85					
		t_{LZ}	0.46					
		t_{ZH}	0.19	0.32	8.27	16.36	24.44	32.53
		t_{ZL}	0.00	0.41	10.29	20.58	30.87	41.15

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO01X2 is a 2mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.47

Bolt Syntax: .....IO Q .IO01X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	19.85	nA
†C_{pd}	8.26	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.68	1.16	0.84	1.01	1.37
		t_{PHL}	0.61	0.81	0.73	0.85	1.10

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.23	0.16	4.27	8.31	12.35	16.39
		t_{PHL}	0.34	0.21	5.48	10.61	15.75	20.89
EN	IO	t_{HZ}	1.02					
		t_{LZ}	0.57					
		t_{ZH}	0.42	0.16	4.46	8.50	12.54	16.57
		t_{ZL}	0.38	0.21	5.52	10.66	15.80	20.93

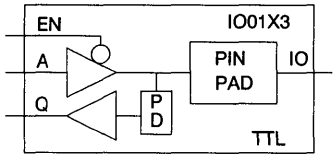
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IO01X3

CYX 1.0 micron CMOS Standard Cells

Description:
IO01X3 is a 4mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.45

Bolt Syntax: .....IO Q .IO01X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	19.85	nA
$^{\dagger}C_{pd}$	8.47	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

10 micron Mixed Signal

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

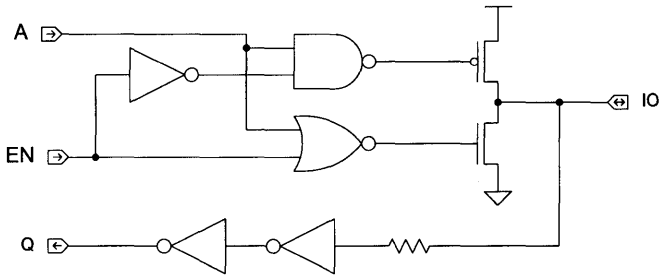
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.68	1.15	0.85	1.02	1.37
		t_{PHL}	0.62	0.82	0.74	0.86	1.11

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.52	0.08	2.54	4.56	6.58	8.59
		t_{PHL}	0.87	0.10	3.44	6.02	8.59	11.17
EN	IO	t_{HZ}	1.36					
		t_{LZ}	0.77					
		t_{ZH}	0.70	0.08	2.72	4.74	6.76	8.78
		t_{ZL}	0.91	0.10	3.48	6.06	8.63	11.21

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

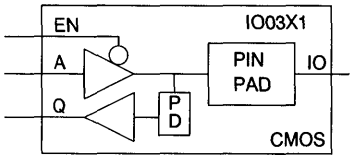


IO03X1

CYX 1.0 micron CMOS Standard Cells

Description:
IO03X1 is a 1mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.47

Bolt Syntax: .....IO Q .IO03X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	21.71	nA
†C_{pd}	8.22	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.62	0.86	0.75	0.88	1.14
		t_{PHL}	0.47	0.72	0.57	0.68	0.90

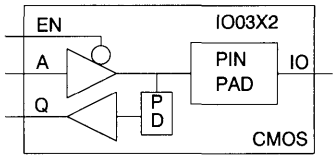
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.00	0.59	14.83	29.66	44.48	59.31
		t_{PHL}	0.02	0.28	6.92	13.83	20.74	27.65
EN	IO	t_{HZ}	0.85					
		t_{LZ}	0.46					
		t_{ZH}	0.00	0.59	14.83	29.66	44.48	59.31
		t_{ZL}	0.06	0.28	6.97	13.88	20.78	27.69

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO03X2 is a 2mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.48

Bolt Syntax: .....IO Q .IO03X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	21.71	nA
†C_{pd}	8.34	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH} t_{PHL}	0.62 0.47	0.85 0.69	0.74 0.57	0.87 0.67	1.13 0.88

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

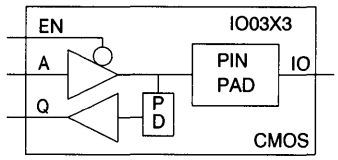
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH} t_{PHL}	0.00 0.45	0.30 0.14	7.41 3.90	14.82 7.35	22.23 10.81	29.64 14.26
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.02 0.57 0.16 0.49	 0.30 0.14	 7.57 3.94	 14.98 7.40	 22.38 10.85	 29.79 14.30

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
IO03X3 is a 4mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.47

Bolt Syntax: .....IO Q .IO03X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	21.71	nA
†C_{pd}	8.52	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.58	0.86	0.70	0.83	1.09
		t_{PHL}	0.44	0.71	0.54	0.64	0.86

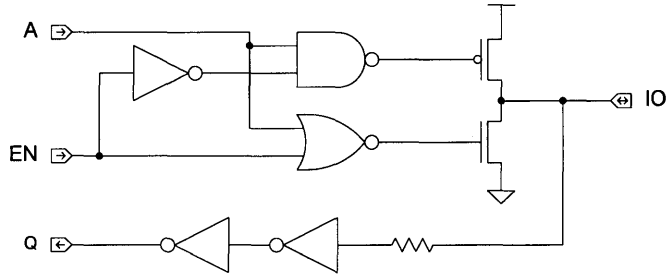
Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.40	0.15	4.11	7.81	11.52	15.22
		t_{PHL}	0.90	0.07	2.63	4.36	6.09	7.82
EN	IO	t_{HZ}	1.36					
		t_{LZ}	0.77					
		t_{ZH}	0.59	0.15	4.29	8.00	11.70	15.40
		t_{ZL}	0.94	0.07	2.67	4.40	6.14	7.87

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

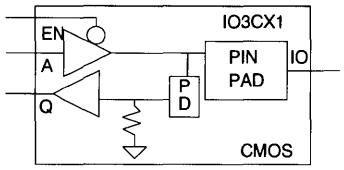


IO3CX1

CYX 1.0 micron CMOS Standard Cells

Description:
IO3CX1 is a 1mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.14
EN	0.14
IO	7.63

Bolt Syntax: .....IO Q .IO3CX1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	21.90	nA
†C_{pd}	8.40	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.63	0.83	0.75	0.87	1.13
		t_{PHL}	0.49	0.66	0.58	0.68	0.88

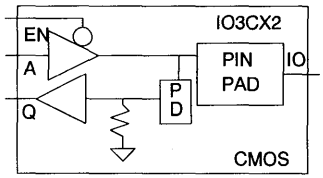
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.00	0.60	15.04	30.07	45.11	60.14
		t_{PHL}	0.00	0.27	6.74	13.48	20.22	26.96
EN	IO	t_{HZ}	0.82					
		t_{LZ}	0.46					
		t_{ZH}	0.00	0.60	15.04	30.07	45.11	60.14
		t_{ZL}	0.16	0.27	6.90	13.64	20.38	27.12

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO3CX2 is a 2mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.14
EN	0.14
IO	7.63

Bolt Syntax: .....IO Q .IO3CX2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	21.90	nA
†C_{pd}	8.51	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.63	0.83	0.75	0.87	1.13
		t_{PHL}	0.49	0.65	0.58	0.68	0.87

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

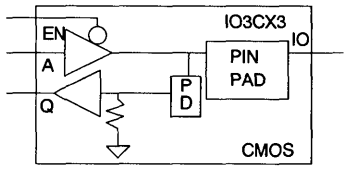
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.00	0.30	7.46	14.91	22.37	29.83
		t_{PHL}	0.47	0.14	3.88	7.29	10.70	14.11
EN	IO	t_{HZ}	0.99					
		t_{LZ}	0.56					
		t_{ZH}	0.20	0.30	7.65	15.11	22.57	30.03
		t_{ZL}	0.54	0.14	3.95	7.36	10.77	14.18

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
IO3CX3 is a 4mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.14
EN	0.13
IO	7.64

Bolt Syntax: ..... IO Q .IO3CX3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	21.90	nA
†C_{pd}	8.76	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

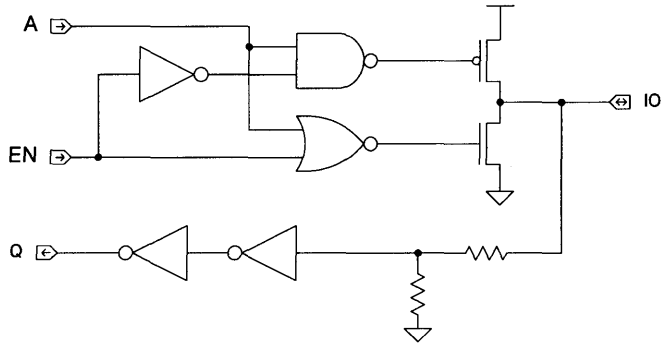
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.63	0.84	0.75	0.88	1.13
		t_{PHL}	0.49	0.66	0.58	0.68	0.88

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.39	0.15	4.11	7.82	11.54	15.25
		t_{PHL}	0.90	0.07	2.62	4.34	6.06	7.78
EN	IO	t_{HZ}	1.35					
		t_{LZ}	0.78					
		t_{ZH}	0.60	0.15	4.31	8.03	11.75	15.46
		t_{ZL}	0.95	0.07	2.67	4.38	6.10	7.82

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

Logic Schematic

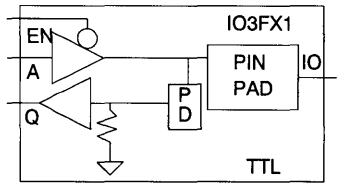


IO3FX1

CYX 1.0 micron CMOS Standard Cells

Description:
IO3FX1 is a 1mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.14
EN	0.14
IO	7.61

Bolt Syntax: .....IO Q .IO3FX1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	20.04	nA
†C_{pd}	8.35	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.74	1.15	0.90	1.07	1.42
		t_{PHL}	0.68	0.78	0.79	0.91	1.15

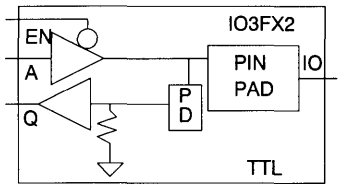
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.00	0.33	8.17	16.33	24.50	32.67
		t_{PHL}	0.00	0.40	10.09	20.17	30.26	40.35
EN	IO	t_{HZ}	0.82					
		t_{LZ}	0.46					
		t_{ZH}	0.07	0.33	8.23	16.40	24.57	32.73
		t_{ZL}	0.00	0.40	10.09	20.17	30.26	40.35

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO3FX2 is a 2mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.14
EN	0.14
IO	7.61

Bolt Syntax: .....IO Q .IO3FX2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	20.04	nA
†C_{pd}	8.46	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.74	1.16	0.90	1.08	1.43
		t_{PHL}	0.68	0.78	0.79	0.91	1.15

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

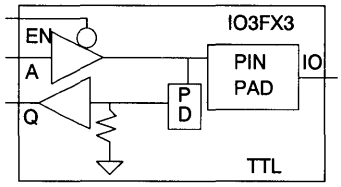
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.14	0.16	4.21	8.29	12.36	16.44
		t_{PHL}	0.27	0.20	5.38	10.48	15.58	20.68
EN	IO	t_{HZ}	0.99					
		t_{LZ}	0.56					
		t_{ZH}	0.35	0.16	4.43	8.50	12.58	16.65
		t_{ZL}	0.35	0.20	5.45	10.55	15.65	20.76

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
IO3FX3 is a 4mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.14
EN	0.13
IO	7.61

Bolt Syntax: .....IO Q .IO3FX3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	20.05	nA
†C_{pd}	8.70	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

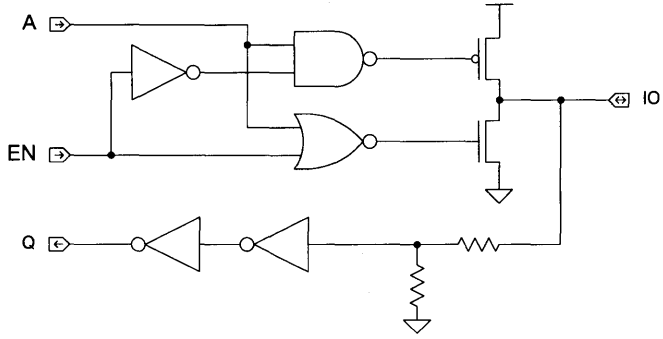
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.75	1.15	0.91	1.08	1.43
		t_{PHL}	0.69	0.79	0.80	0.92	1.16

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.40	0.08	2.45	4.49	6.54	8.58
		t_{PHL}	0.81	0.10	3.39	5.96	8.54	11.11
EN	IO	t_{HZ}	1.34					
		t_{LZ}	0.78					
		t_{ZH}	0.61	0.08	2.65	4.70	6.74	8.79
		t_{ZL}	0.86	0.10	3.44	6.01	8.59	11.16

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

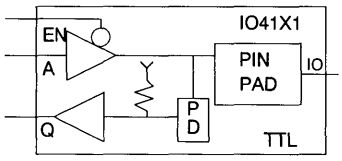


IO41X1

CYX 1.0 micron CMOS Standard Cells

Description:
IO41X1 is a 1mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.62

Bolt Syntax: .....IO Q .IO41X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	20.36	nA
†C_{pd}	8.30	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.67	1.15	0.84	1.01	1.36
		t_{PHL}	0.61	0.81	0.72	0.84	1.09

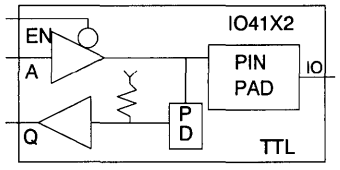
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.00	0.31	7.84	15.69	23.53	31.37
		t_{PHL}	0.00	0.41	10.36	20.73	31.09	41.46
EN	IO	t_{HZ}	0.82					
		t_{LZ}	0.47					
		t_{ZH}	10.15	0.31	18.00	25.84	33.68	41.53
		t_{ZL}	0.00	0.41	10.36	20.73	31.09	41.46

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO41X2 is a 2mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.63

Bolt Syntax: .....IO Q .IO41X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	20.36	nA
†C_{pd}	8.40	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.67	1.15	0.83	1.00	1.35
		t_{PHL}	0.60	0.82	0.72	0.84	1.09

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

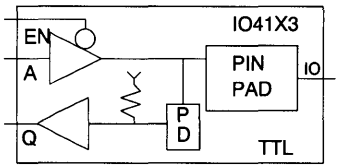
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.22	0.16	4.20	8.18	12.16	16.14
		t_{PHL}	0.37	0.21	5.53	10.69	15.85	21.02
EN	IO	t_{HZ}	1.00					
		t_{LZ}	0.56					
		t_{ZH}	0.44	0.16	4.42	8.40	12.38	16.36
		t_{ZL}	0.41	0.21	5.57	10.73	15.90	21.06

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
IO41X3 is a 4mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.64

Bolt Syntax: .....IO Q .IO41X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	20.36	nA
†C_{pd}	8.65	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

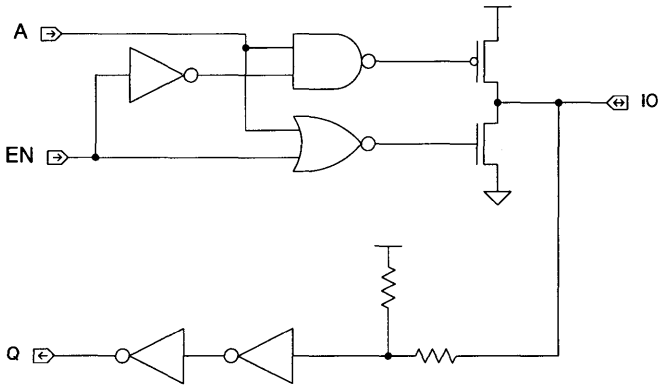
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.67	1.15	0.83	1.01	1.36
		t_{PHL}	0.60	0.82	0.72	0.84	1.09

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.50	0.08	2.50	4.51	6.51	8.51
		t_{PHL}	0.88	0.10	3.46	6.04	8.62	11.20
EN	IO	t_{HZ}	1.34					
		t_{LZ}	0.78					
		t_{ZH}	0.70	0.08	2.71	4.71	6.71	8.71
		t_{ZL}	0.92	0.10	3.50	6.08	8.66	11.24

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

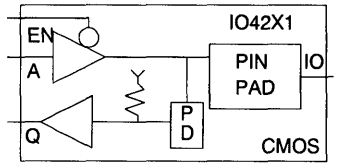


IO42X1

CYX 1.0 micron CMOS Standard Cells

Description:
IO42X1 is a 1mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.64

Bolt Syntax: .....IO Q .IO42X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	22.22	nA
†C_{pd}	8.43	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.69	0.86	0.81	0.94	1.20
		t_{PHL}	0.51	0.74	0.61	0.73	0.95

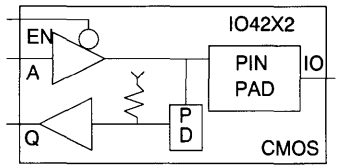
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.00	0.58	14.45	28.90	43.35	57.79
		t_{PHL}	0.10	0.28	7.05	14.00	20.95	27.90
EN	IO	t_{HZ}	0.82					
		t_{LZ}	0.46					
		t_{ZH}	0.00	0.58	14.45	28.90	43.35	57.79
		t_{ZL}	0.15	0.28	7.09	14.04	20.99	27.94

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO42X2 is a 2mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.64

Bolt Syntax: .....IO Q .IO42X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	22.23	nA
†C_{pd}	8.55	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.69	0.86	0.81	0.94	1.20
		t_{PHL}	0.52	0.72	0.62	0.73	0.94

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx}) (ns)	k_{tdx} (ns/pF)	Capacitive Load pF) 25	50	75	100
A	IO	t_{PLH}	0.00	0.29	7.31	14.63	21.94	29.26
		t_{PHL}	0.44	0.14	3.90	7.37	10.84	14.30
EN	IO	t_{HZ}	1.00					
		t_{LZ}	0.56					
		t_{ZH}	0.20	0.29	7.51	14.83	22.14	29.46
		t_{ZL}	0.48	0.14	3.95	7.41	10.88	14.34

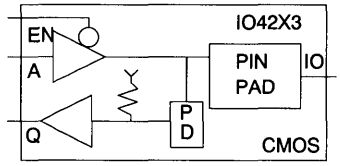
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IO42X3

CYX 1.0 micron CMOS Standard Cells

Description:
IO42X3 is a 4mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.65

Bolt Syntax: .....IO Q .IO42X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	22.22	nA
†C_{pd}	8.68	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

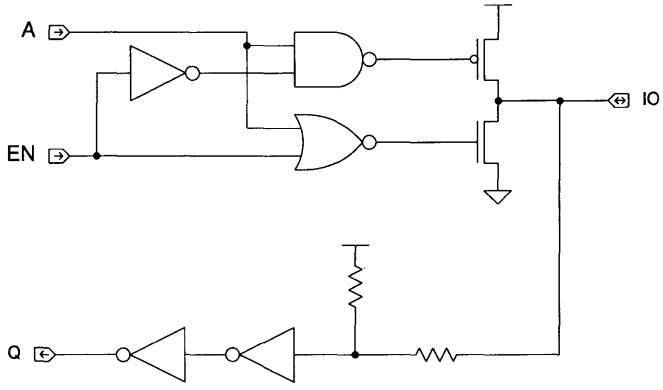
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.56	0.86	0.69	0.81	1.08
		t_{PHL}	0.42	0.70	0.52	0.63	0.84

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.38	0.15	4.06	7.74	11.42	15.10
		t_{PHL}	0.89	0.07	2.63	4.36	6.10	7.84
EN	IO	t_{HZ}	1.35					
		t_{LZ}	0.78					
		t_{ZH}	0.58	0.15	4.26	7.94	11.62	15.31
		t_{ZL}	0.94	0.07	2.67	4.41	6.14	7.88

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

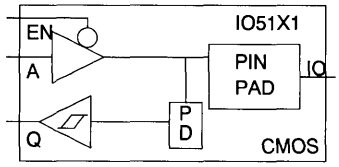


IO51X1

CYX 1.0 micron CMOS Standard Cells

Description:
IO51X1 is a 1mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.48

Bolt Syntax: .....IO Q .IO51X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	21.15	nA
†C_{pd}	8.44	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	2.11	0.99	2.25	2.40	2.70
		t_{PHL}	1.72	0.82	1.84	1.96	2.21

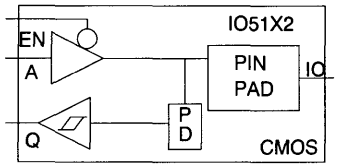
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.00	0.59	14.83	29.67	44.50	59.33
		t_{PHL}	0.09	0.28	7.00	13.91	20.82	27.73
EN	IO	t_{HZ}	0.84					
		t_{LZ}	0.46					
		t_{ZH}	0.00	0.59	14.83	29.67	44.50	59.33
		t_{ZL}	0.13	0.28	7.04	13.96	20.87	27.78

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO51X2 is a 2mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.48

Bolt Syntax: .....IO Q .IO51X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	21.15	nA
†C_{pd}	8.55	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	2.10	1.01	2.25	2.40	2.70
		t_{PHL}	1.73	0.82	1.84	1.96	2.21

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

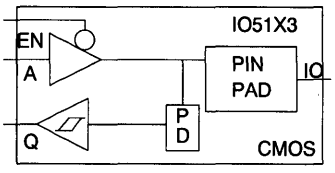
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.00	0.30	7.41	14.82	22.23	29.63
		t_{PHL}	0.48	0.14	3.93	7.38	10.84	14.29
EN	IO	t_{HZ}	1.01					
		t_{LZ}	0.56					
		t_{ZH}	0.18	0.30	7.58	14.99	22.40	29.81
		t_{ZL}	0.52	0.14	3.98	7.43	10.88	14.34

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
IO51X3 is a 4mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
IO	7.48

Bolt Syntax: .....IO Q .IO51X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	21.15	nA
†C_{pd}	8.78	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

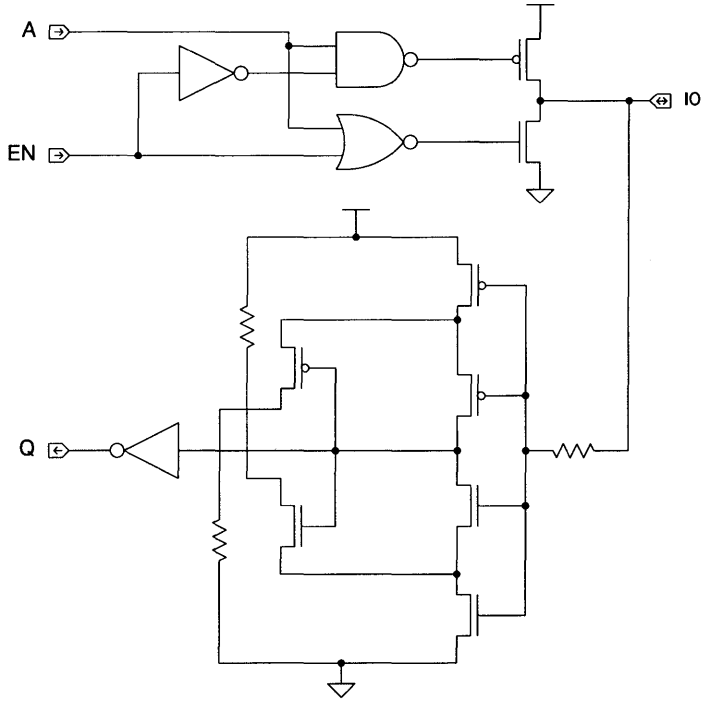
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	2.11	0.99	2.25	2.40	2.70
		t_{PHL}	1.72	0.83	1.84	1.96	2.21

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.40	0.15	4.10	7.80	11.51	15.21
		t_{PHL}	0.90	0.07	2.63	4.36	6.09	7.82
EN	IO	t_{HZ}	1.37					
		t_{LZ}	0.77					
		t_{ZH}	0.59	0.15	4.29	8.00	11.70	15.40
		t_{ZL}	0.94	0.07	2.67	4.40	6.13	7.87

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



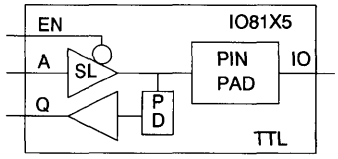
IO81X5

AMI SEMICONDUCTORS

CYX 1.0 micron CMOS Standard Cells

Description:
IO81X5 is an 8mA, non-inverting, TTL-level, bidirectional buffer pad with an active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.32
EN	0.21
IO	7.73

Bolt Syntax: .....IO Q .IO81X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	25.26	nA
$^{\dagger}C_{pd}$	9.96	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.78	1.15	0.94	1.11	1.46
		t_{PHL}	0.52	0.78	0.64	0.75	0.99

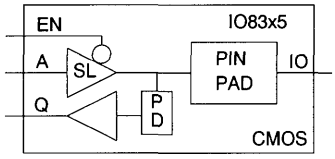
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.51	0.05	1.84	3.18	4.52	5.86
		t_{PHL}	0.97	0.10	3.53	6.08	8.64	11.20
EN	IO	t_{HZ}	1.33					
		t_{LZ}	1.09					
		t_{ZH}	0.83	0.05	2.17	3.51	4.85	6.19
		t_{ZL}	1.00	0.10	3.56	6.11	8.67	11.23

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO83X5 is an 8mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.32
EN	0.21
IO	7.75

Bolt Syntax: .....IO Q .IO83X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	27.11	nA
†C_{pd}	10.03	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.69	0.84	0.81	0.93	1.19
		t_{PHL}	0.53	0.66	0.63	0.73	0.93

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.43	0.10	2.90	5.36	7.82	10.28
		t_{PHL}	0.96	0.07	2.69	4.42	6.16	7.89
EN	IO	t_{HZ}	1.33					
		t_{LZ}	1.09					
		t_{ZH}	0.77	0.10	3.23	5.69	8.16	10.62
		t_{ZL}	0.99	0.07	2.72	4.45	6.18	7.92

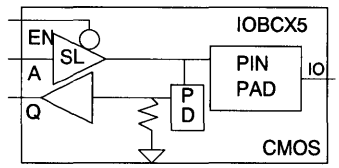
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IOBCX5

CYX 1.0 micron CMOS Standard Cells

Description:
IOBCX5 is an 8mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.33
EN	0.21
IO	7.93

Bolt Syntax: .....IO Q .IOBCX5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	27.31	nA
†C_{pd}	10.21	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.68	0.84	0.80	0.92	1.18
		t_{PHL}	0.52	0.67	0.62	0.72	0.92

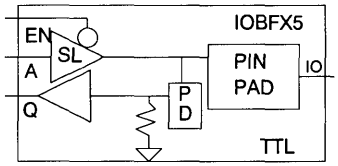
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.45	0.10	2.91	5.38	7.85	10.31
		t_{PHL}	0.96	0.07	2.69	4.42	6.15	7.87
EN	IO	t_{HZ}	1.33					
		t_{LZ}	1.07					
		t_{ZH}	0.79	0.10	3.25	5.72	8.19	10.65
		t_{ZL}	0.99	0.07	2.72	4.44	6.17	7.90

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IOBFX5 is an 8mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.33
EN	0.21
IO	7.91

Bolt Syntax:.....IO Q .IOBFX5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	25.46	nA
†C_{pd}	10.14	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.78	1.15	0.94	1.11	1.46
		t_{PHL}	0.67	0.87	0.80	0.93	1.19

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.42	0.05	1.78	3.14	4.50	5.86
		t_{PHL}	0.91	0.10	3.47	6.03	8.60	11.16
EN	IO	t_{HZ}	1.34					
		t_{LZ}	1.07					
		t_{ZH}	0.75	0.05	2.11	3.47	4.83	6.19
		t_{ZL}	0.94	0.10	3.50	6.06	8.62	11.18

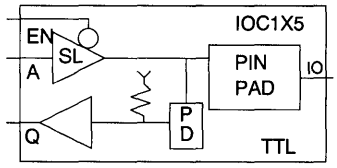
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IOC1X5

CYX 1.0 micron CMOS Standard Cells

Description:
IOC1X5 is an 8mA, non-inverting TTL-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.32
EN	0.21
IO	7.93

Bolt Syntax: ..... IO Q .IOC1X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	25.78	nA
†C_{pd}	10.17	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.79	1.15	0.95	1.12	1.47
		t_{PHL}	0.53	0.78	0.64	0.76	0.99

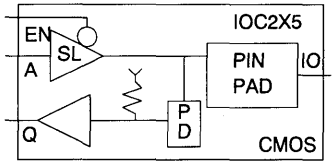
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.50	0.05	1.84	3.17	4.51	5.84
		t_{PHL}	0.97	0.10	3.53	6.09	8.65	11.21
EN	IO	t_{HZ}	1.34					
		t_{LZ}	1.07					
		t_{ZH}	0.84	0.05	2.17	3.51	4.84	6.18
		t_{ZL}	1.00	0.10	3.56	6.12	8.68	11.24

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IOC2X5 is an 8mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.32
EN	0.21
IO	7.94

Bolt Syntax: .....IO Q .IOC2X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	27.63	nA
†C_{pd}	10.23	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	0.69	0.83	0.81	0.93	1.18
		t_{PHL}	0.53	0.66	0.62	0.72	0.92

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.43	0.10	2.89	5.34	7.79	10.25
		t_{PHL}	0.97	0.07	2.71	4.45	6.19	7.92
EN	IO	t_{HZ}	1.33					
		t_{LZ}	1.07					
		t_{ZH}	0.77	0.10	3.22	5.68	8.13	10.58
		t_{ZL}	1.00	0.07	2.74	4.48	6.21	7.95

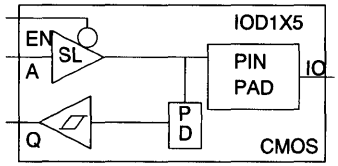
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IOD1X5

CYX 1.0 micron CMOS Standard Cells

Description:
IOD1X5 is an 8mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.31
EN	0.19
IO	7.75

Bolt Syntax: .....IO Q .IOD1X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	26.56	nA
†C_{pd}	10.15	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
IO	Q	t_{PLH}	2.08	1.00	2.22	2.37	2.67
		t_{PHL}	1.71	0.81	1.83	1.95	2.20

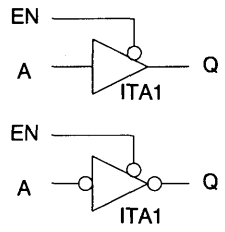
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	0.42	0.10	2.88	5.34	7.80	10.26
		t_{PHL}	0.95	0.07	2.68	4.41	6.15	7.88
EN	IO	t_{HZ}	1.32					
		t_{LZ}	1.05					
		t_{ZH}	0.76	0.10	3.22	5.68	8.13	10.59
		t_{ZL}	0.98	0.07	2.71	4.44	6.17	7.91

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
ITA1 is a non-inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.06
EN	0.09
Q	0.06

Equivalent Gates:.....1.9
Bolt Syntax:.....Q .ITA1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.92	nA
†C_{pd}	0.29	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.47	1.98	0.75	1.04	1.64
		t_{PHL}	0.44	1.37	0.64	0.84	1.26
EN	Q	t_{HZ}	0.17				
		t_{LZ}	0.21				
		t_{ZH}	0.17	1.98	0.46	0.75	1.35
		t_{ZL}	0.26	1.37	0.46	0.66	1.08

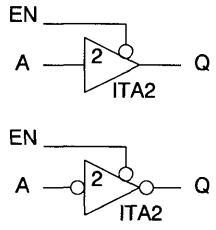
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ITA2

CYX 1.0 micron CMOS Standard Cells

Description:
ITA2 is a non-inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.06
EN	0.16
Q	0.10

Equivalent Gates:.....2.3
Bolt Syntax:.....QN .ITA2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	4.95	nA
†C_{pd}	0.54	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

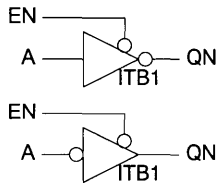
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	0.54	0.69	0.64	0.74	0.95
		t_{PHL}	0.56	0.52	0.63	0.71	0.87
EN	Q	t_{HZ}	0.17				
		t_{LZ}	0.27				
		t_{ZH}	0.14	0.69	0.23	0.34	0.55
		t_{ZL}	0.27	0.52	0.34	0.42	0.58

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
ITB1 is an inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.06
EN	0.09
QN	0.06

Equivalent Gates:..... 1.4
Bolt Syntax:..... QN .ITB1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.97	nA
†C_{pd}	0.18	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	QN	t_{LH}	0.31	1.98	0.59	0.89	1.49
		t_{PHL}	0.24	1.38	0.44	0.65	1.07
EN	QN	t_{HZ}	0.17				
		t_{LZ}	0.21				
		t_{ZH}	0.17	1.98	0.45	0.75	1.35
		t_{ZL}	0.26	1.38	0.46	0.66	1.08

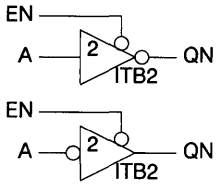
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ITB2

CYX 1.0 micron CMOS Standard Cells

Description:
ITB2 is an inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.17
EN	0.16
QN	0.09

Equivalent Gates:.....2.1
Bolt Syntax:.....QN .ITB2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	4.00	nA
†C_{pd}	0.32	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

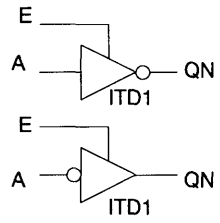
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	QN	t_{PLH}	0.28	0.68	0.38	0.48	0.69
		t_{PHL}	0.22	0.50	0.29	0.37	0.52
EN	QN	t_{HZ}	0.17				
		t_{LZ}	0.27				
		t_{ZH}	0.14	0.68	0.24	0.34	0.54
		t_{ZL}	0.26	0.50	0.33	0.41	0.56

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
ITD1 is an inverting internal tri-state buffer with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.06
E	0.08
QN	0.06

Equivalent Gates:.....1.3
Bolt Syntax:.....QN .ITD1 A E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.97	nA
†C_{pd}	0.19	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

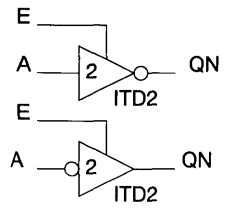
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	QN	t_{PLH}	0.33	1.97	0.61	0.90	1.50
		t_{PHL}	0.24	1.38	0.44	0.64	1.06
E	QN	t_{HZ}	0.30				
		t_{LZ}	0.12				
		t_{ZH}	0.30	1.97	0.58	0.87	1.47
		t_{ZL}	0.13	1.38	0.33	0.53	0.95

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
ITD2 is an inverting internal tri-state buffer with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.17
E	0.12
QN	0.10

Equivalent Gates:.....2.2
Bolt Syntax:.....QN .ITD2 A E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	4.00	nA
†C_{pd}	0.37	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

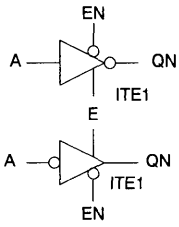
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	QN	t_{PLH}	0.30	0.68	0.40	0.50	0.71
		t_{PHL}	0.21	0.50	0.28	0.35	0.50
E	QN	t_{HZ}	0.47				
		t_{LZ}	0.12				
		t_{ZH}	0.32	0.68	0.42	0.52	0.73
		t_{ZL}	0.09	0.50	0.16	0.23	0.39

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
ITE1 is a two-phase inverting internal tri-state buffer.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

Pin Loading

	Ci (pF)
A	0.06
E	0.03
EN	0.04
QN	0.06

Equivalent Gates:.....1.3
Bolt Syntax:.....QN .ITE1 A E EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.02	nA
†C_{pd}	0.10	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	QN	t_{PLH} t_{PHL}	0.32 0.24	1.97 1.37	0.60 0.44	0.89 0.64	1.49 1.06
EN	QN	t_{HZ} t_{ZH}	0.17 0.24	1.97	0.52	0.81	1.42
E	QN	t_{LZ} t_{ZL}	0.13 0.22	1.37	0.41	0.62	1.04

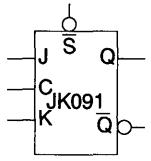
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

JK091

CYX 1.0 micron CMOS Standard Cells

Description:
JK091 is a static, master-slave, JK flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	H	L
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Change

Pin Loading

	Ci (pF)
J	0.07
K	0.06
C	0.18
SN	0.12

Equivalent Gates: 7.2
Bolt Syntax: ..... Q QN .JK091 C J K SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	11.60	nA
†C_{pd}	1.38	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.89 1.14	1.45 1.39	1.10 1.34	1.32 1.55	1.76 1.97
C	QN	t_{PLH} t_{PHL}	0.85 0.45	1.94 1.36	1.12 0.64	1.41 0.84	2.00 1.25
SN	Q	t_{PLH}	0.29	1.45	0.50	0.71	1.15
SN	QN	t_{PHL}	0.94	1.36	1.14	1.34	1.75
Min C Width	High	t_w				1.55	
Min C Width	Low	t_w	1.42				
Min SN Width	Low	t_w				1.34	
Min J Setup		t_{su}	1.42				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.24				

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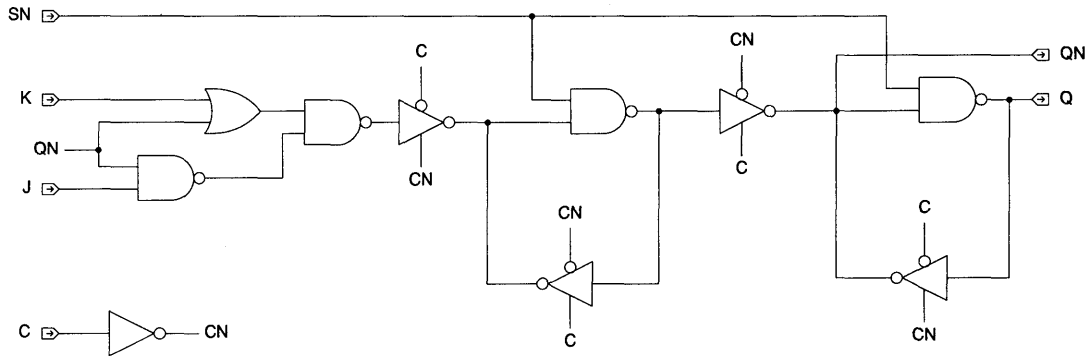
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min K Hold		t_h	0.00				
Min SN Setup		t_{su}	0.27				
Min SN Hold		t_h	0.27				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

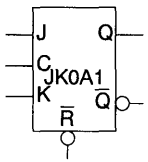


JK0A1

CYX 1.0 micron CMOS Standard Cells

Description:
JK0A1 is a static, master-slave, JK flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	L	H
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Charge

Pin Loading

	Ci (pF)
J	0.07
K	0.06
C	0.18
RN	0.06

Equivalent Gates:.....8.1
Bolt Syntax:.....Q QN .JK0A1 C J K RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	11.30	nA
†C_{pd}	1.57	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.99 1.12	2.02 1.32	1.28 1.31	1.58 1.50	2.20 1.90
C	QN	t_{PLH} t_{PHL}	0.86 0.45	1.95 1.36	1.13 0.64	1.42 0.84	2.02 1.26
RN	Q	t_{PHL}	0.50	1.32	0.69	0.88	1.28
RN	QN	t_{PLH}	1.40	1.95	1.67	1.96	2.56
Min C Width	High	t_w				1.58	
Min C Width	Low	t_w	1.51				
Min RN Width	Low	t_w				1.96	
Min J Setup		t_{su}	1.51				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.33				

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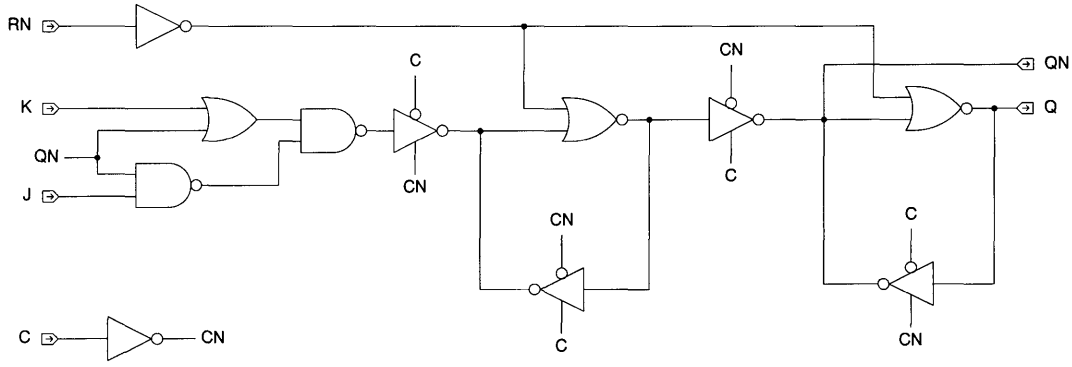
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	0.74				
Min RN Hold		t_h	0.57				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

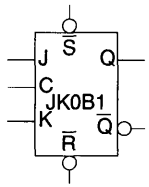


JK0B1

CYX 1.0 micron CMOS Standard Cells

Description:
JK0B1 is a static, master-slave, JK flip-flop. SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

Pin Loading

	Ci (pF)
J	0.07
K	0.06
C	0.18
SN	0.12
RN	0.13

Equivalent Gates: 9.9
Bolt Syntax: .....Q QN .JK0B1 C J K RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	13.01	nA
†C_{pd}	1.78	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.93 1.23	1.47 1.40	1.14 1.43	1.36 1.64	1.81 2.07
C	QN	t_{PLH} t_{PHL}	0.93 0.47	1.94 1.35	1.20 0.66	1.49 0.86	2.08 1.27
RN	Q	t_{PHL}	1.71	1.40	1.91	2.12	2.55
RN	QN	t_{PLH}	1.40	1.94	1.67	1.96	2.56
SN	Q	t_{PLH}	0.30	1.47	0.51	0.72	1.17
SN	QN	t_{PHL}	1.11	1.35	1.31	1.51	1.92
Min C Width	High	t_w				1.64	
Min C Width	Low	t_w	1.56				
Min RN Width	Low	t_w				2.12	
Min SN Width	Low	t_w				1.51	

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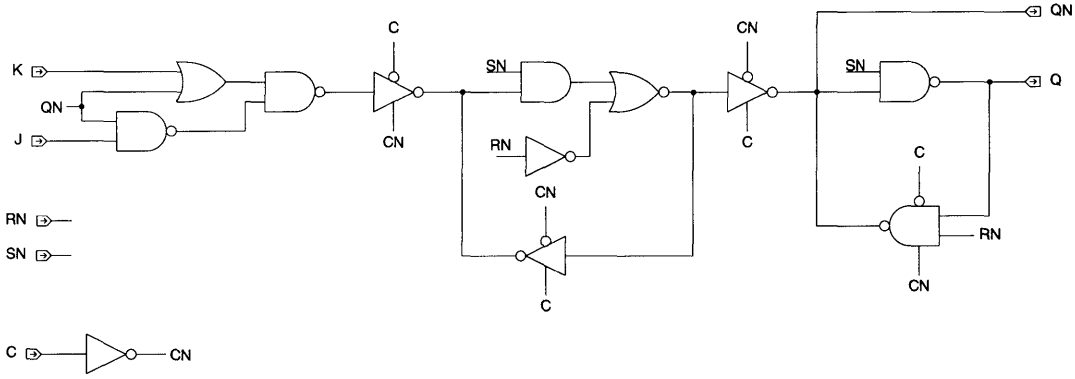
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min J Setup		t_{su}	1.56				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.35				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	0.73				
Min RN Hold		t_h	0.60				
Min SN Setup		t_{su}	0.42				
Min SN Hold		t_h	0.29				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

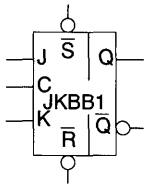


JKBB1

CYX 1.0 micron CMOS Standard Cells

Description:
JKBB1 is a static, master-slave, JK flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

Pin Loading

	Ci (pF)
J	0.06
K	0.06
C	0.17
SN	0.12
RN	0.13

Equivalent Gates:.....11.5
Bolt Syntax:.....Q QN .JKBB1 C J K RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	14.11	nA
†C_{pd}	1.89	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

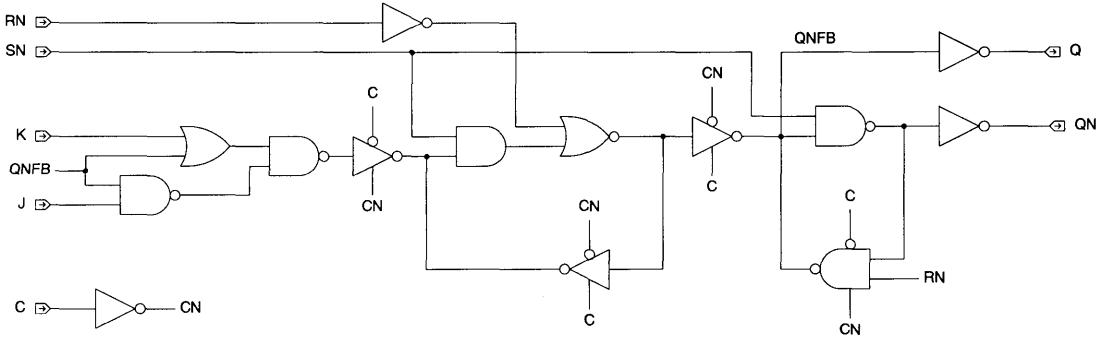
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH}	0.82	1.34	1.01	1.21	1.62
		t_{PHL}	1.13	1.31	1.32	1.52	1.92
C	QN	t_{PLH}	1.62	1.20	1.79	1.97	2.33
		t_{PHL}	1.22	0.98	1.36	1.51	1.80
RN	Q	t_{PHL}	1.57	1.31	1.75	1.95	2.35
RN	QN	t_{PLH}	2.05	1.20	2.22	2.40	2.77
SN	Q	t_{PLH}	1.48	1.34	1.67	1.87	2.28
SN	QN	t_{PHL}	0.53	0.98	0.67	0.82	1.12
Min C Width	High	t_w	1.38				
Min C Width	Low	t_w	1.54				
Min RN Width	Low	t_w	2.21				
Min SN Width	Low	t_w	1.14				

(continued on next page)

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Min J Setup		t_{su}	1.54				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.23				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	0.66				
Min RN Hold		t_h	1.43				
Min SN Setup		t_{su}	0.36				
Min SN Hold		t_h	0.61				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

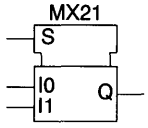
Logic Schematic



CYX 1.0 micron CMOS Standard Cells

Description:
MX21 is a 2-input to 1-output digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Pin Loading

	Ci (pF)
I0	0.06
I1	0.06
S	0.10

Equivalent Gates:.....2.2
Bolt Syntax:.....Q .MX21 I0 I1 S;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.46	nA
†C_{pd}	0.36	pF

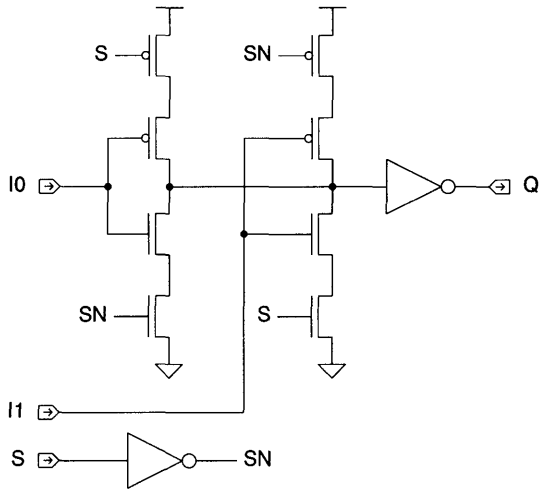
Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

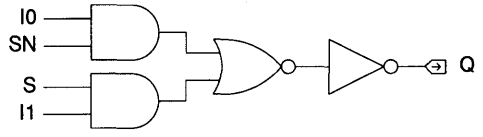
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Ix Input	Q	t_{PLH}	0.59	1.19	0.75	0.93	1.29
		t_{PHL}	0.56	1.14	0.72	0.89	1.24
S	Q	t_{PLH}	0.87	1.19	1.04	1.22	1.58
		t_{PHL}	0.87	1.14	1.03	1.20	1.55

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



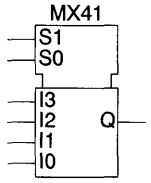
LOGICAL



CYX 1.0 micron CMOS Standard Cells

Description:
MX41 is a four-to-one digital multiplexer.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

Pin Loading

	Ci (pF)
I0	0.07
I1	0.07
I2	0.06
I3	0.07
S0	0.18
S1	0.19

Equivalent Gates:.....5.6
Bolt Syntax:.....Q .MX41 I0 I1 I2 I3 S0 S1;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	6.93	nA
†C_{pd}	0.94	pF

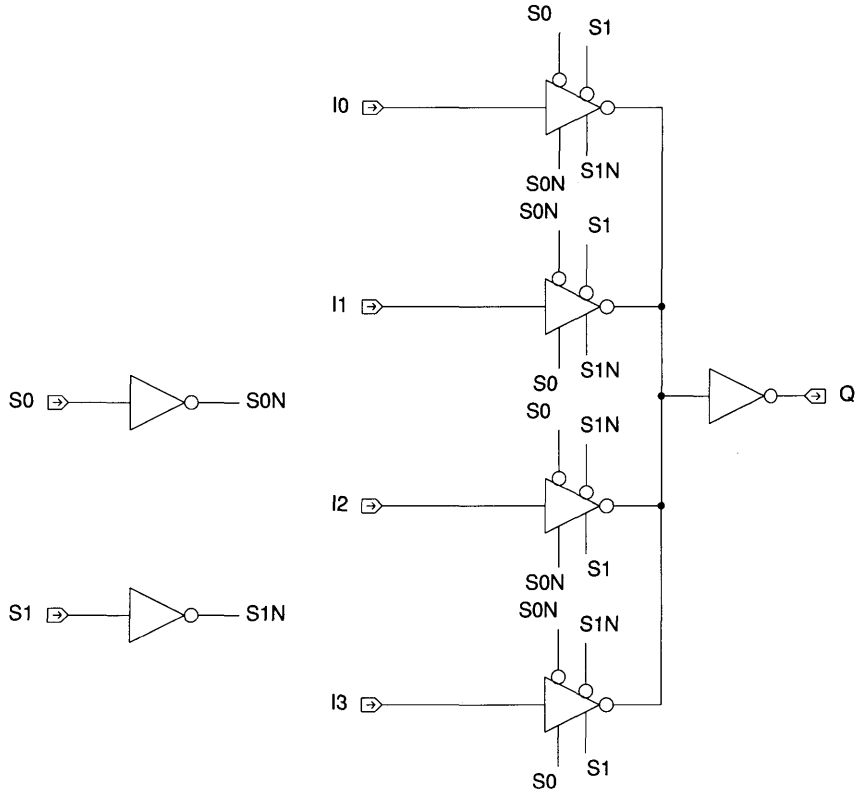
Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Ix Input	Q	t_{PLH}	1.44	1.42	1.64	1.85	2.28
		t_{PHL}	1.16	1.82	1.42	1.69	2.25
Any Sx Input	Q	t_{PLH}	1.45	1.42	1.65	1.86	2.29
		t_{PHL}	1.46	1.82	1.72	1.99	2.55

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

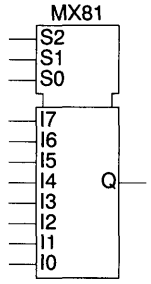


MX81

CYX 1.0 micron CMOS Standard Cells

Description:
MX81 is an eight-to-one digital multiplexer.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

Pin Loading

	Ci (pF)
I0	0.07
I1	0.07
I2	0.07
I3	0.07
I4	0.07
I5	0.06
I6	0.07
I7	0.07
S0	0.31
S1	0.19
S2	0.12

Equivalent Gates:.....13.5
Bolt Syntax:.....Q .MX81 I0 I1 I2 I3 I4 I5 I6 I7 S0 S1 S2;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	18.04	nA
†C_{pd}	2.13	pF

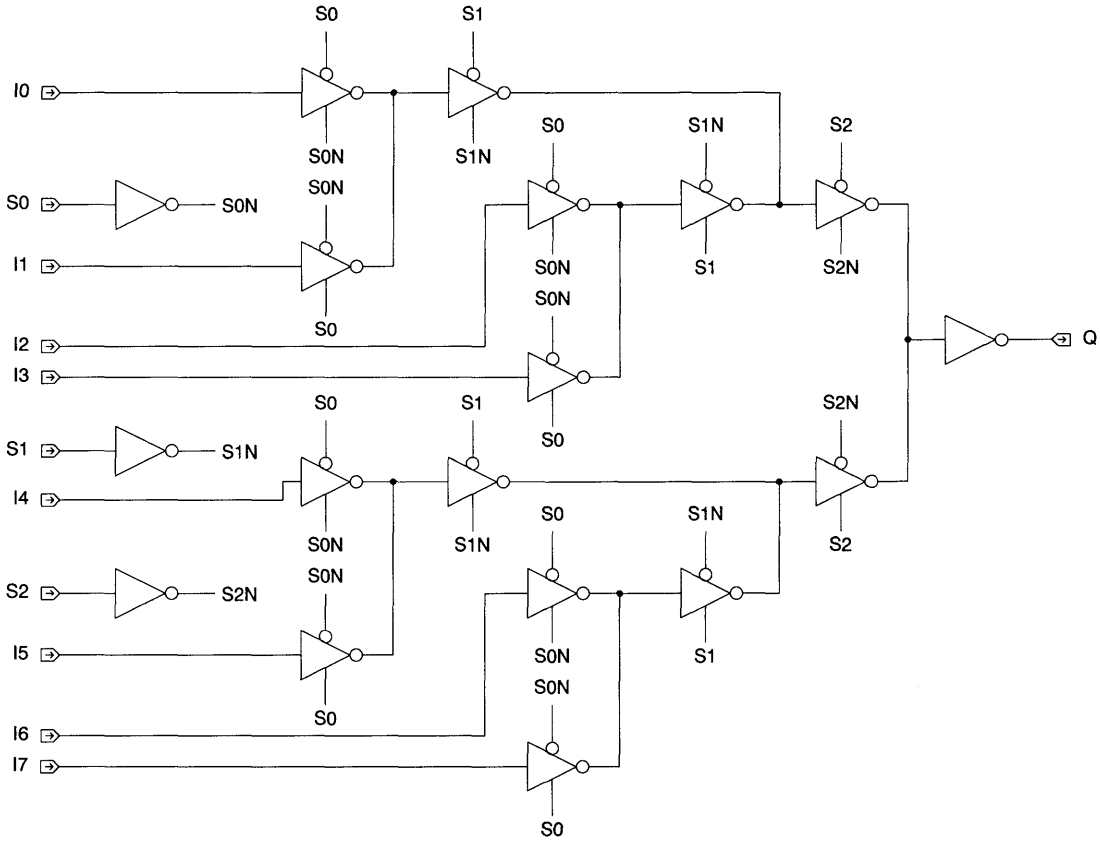
Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Ix Input	Q	t_{PLH} t_{PHL}	1.59 1.49	1.19 1.16	1.76 1.66	1.94 1.83	2.30 2.18
Any Sx Input	Q	t_{PLH} t_{PHL}	1.57 1.54	1.19 1.16	1.74 1.70	1.92 1.87	2.28 2.23

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

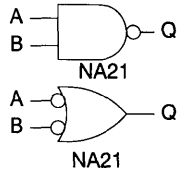
Logic Schematic



CYX 1.0 micron CMOS Standard Cells

Description:
NA21 is a two-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06

Equivalent Gates: 1.0
Bolt Syntax: ..... Q .NA21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.65	nA
†C_{pd}	0.08	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

10 micron Mixed Signal

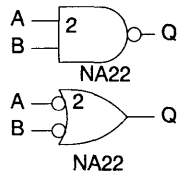
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.23	1.29	0.41	0.61	1.00
		t_{PHL}	0.16	1.03	0.30	0.46	0.77

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NA22 is a two-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

Pin Loading

	Ci (pF)
A	0.11
B	0.11

Equivalent Gates:.....1.6
Bolt Syntax:.....Q .NA22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.29	nA
†C_{pd}	0.20	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

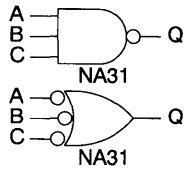
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.24	0.66	0.34	0.43	0.63
		t_{PHL}	0.17	0.53	0.24	0.32	0.48

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
NA31 is a three-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06

Equivalent Gates:.....1.3
Bolt Syntax:.....Q .NA31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.47	nA
†C_{pd}	0.13	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

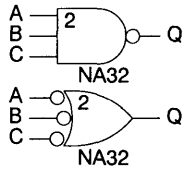
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.32	1.31	0.51	0.70	1.10
		t_{PHL}	0.28	1.38	0.48	0.68	1.10

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NA32 is a three-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Pin Loading

	Ci (pF)
A	0.12
B	0.12
C	0.12

Equivalent Gates:.....2.3
Bolt Syntax:.....Q .NA32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	4.93	nA
†C_{pd}	0.20	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.29	0.67	0.39	0.49	0.69
		t_{PHL}	0.25	0.71	0.35	0.46	0.67

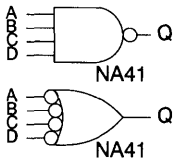
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

NA41

CYX 1.0 micron CMOS Standard Cells

Description:
NA41 is a four-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .NA41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.03	nA
†C_{pd}	0.17	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

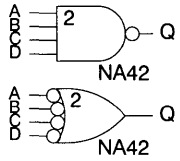
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.44	1.46	0.64	0.86	1.30
		t_{PHL}	0.41	1.61	0.64	0.88	1.37

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

1.0 micron Mixed Signal

Description:
NA42 is a four-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.12
B	0.12
C	0.12
D	0.12

Equivalent Gates:.....2.8
Bolt Syntax:.....Q .NA42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	6.06	nA
†C_{pd}	0.27	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

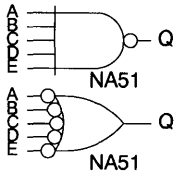
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.40	0.75	0.51	0.62	0.85
		t_{PHL}	0.37	0.82	0.48	0.60	0.86

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
NA51 is a five-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06
E	0.06

Equivalent Gates:.....2.0
Bolt Syntax:.....Q .NA51 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.47	nA
†C_{pd}	0.20	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

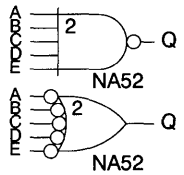
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.55	1.63	0.78	1.03	1.53
		t_{PHL}	0.52	1.82	0.78	1.05	1.60

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NA52 is a five-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.12
B	0.12
C	0.12
D	0.12
E	0.13

Equivalent Gates:.....3.8
Bolt Syntax:.....Q .NA52 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	6.94	nA
†C_{pd}	0.36	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.53	0.85	0.65	0.77	1.03
		t_{PHL}	0.49	0.92	0.62	0.76	1.04

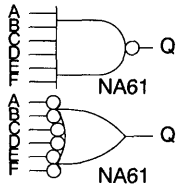
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

NA61

CYX 1.0 micron CMOS Standard Cells

Description:
NA61 is a six-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06
E	0.06
F	0.06

Equivalent Gates:.....3.8
Bolt Syntax:.....Q .NA61 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	6.90	nA
†C_{pd}	0.56	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

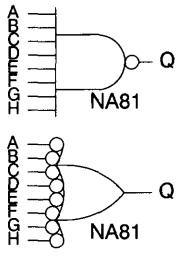
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.81	1.11	0.97	1.14	1.48
		t_{PHL}	0.90	0.97	1.03	1.18	1.47

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NA81 is an eight-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06
E	0.06
F	0.06
G	0.06
H	0.06

Equivalent Gates:.....4.4
Bolt Syntax:.....Q .NA81 A B C D E F G H;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	8.03	nA
†C_{pd}	0.60	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.94	1.11	1.10	1.26	1.60
		t_{PHL}	1.03	0.97	1.17	1.31	1.61

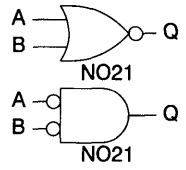
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

NO21

CYX 1.0 micron CMOS Standard Cells

Description:
NO21 is a two-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06

Equivalent Gates:.....1.0
Bolt Syntax:.....Q .NO21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.02	nA
†C_{pd}	0.09	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

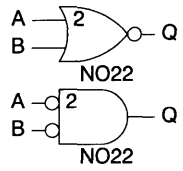
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.26	1.98	0.55	0.84	1.44
		t_{PHL}	0.18	0.91	0.31	0.45	0.73

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NO22 is a two-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Pin Loading

	Ci (pF)
A	0.11
B	0.11

Equivalent Gates:.....1.6
Bolt Syntax:.....Q .NO22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.04	nA
†C_{pd}	0.14	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

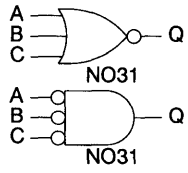
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.25	1.00	0.39	0.54	0.84
		t_{PHL}	0.17	0.50	0.24	0.31	0.46

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
NO31 is a three-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06

Equivalent Gates:.....1.3
Bolt Syntax:.....Q .NO31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.09	nA
†C_{pd}	0.13	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

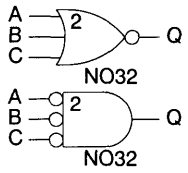
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.49	2.74	0.88	1.29	2.13
		t_{PHL}	0.25	1.05	0.40	0.55	0.88

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NO32 is a three-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

Pin Loading

	Ci (pF)
A	0.11
B	0.12
C	0.12

Equivalent Gates:.....2.1
Bolt Syntax:.....Q .NO32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.17	nA
†C_{pd}	0.22	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.46	1.39	0.66	0.86	1.29
		t_{PHL}	0.22	0.57	0.31	0.39	0.56

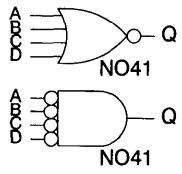
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

AMI SEMICONDUCTORS

CYX 1.0 micron CMOS Standard Cells

Description:
NO41 is a four-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06

Equivalent Gates:.....1.6
Bolt Syntax:.....Q .NO41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.15	nA
†C_{pd}	0.16	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

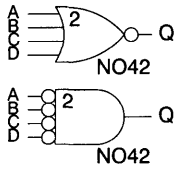
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.74	3.42	1.22	1.73	2.78
		t_{PHL}	0.30	1.25	0.47	0.66	1.04

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NO42 is a four-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.12
B	0.12
C	0.12
D	0.12

Equivalent Gates:.....2.7
Bolt Syntax:.....Q .NO42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.30	nA
†C_{pd}	0.29	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.70	1.74	0.95	1.21	1.74
		t_{PHL}	0.27	0.67	0.37	0.47	0.67

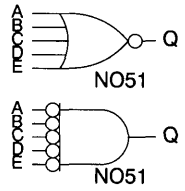
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

NO51

CYX 1.0 micron CMOS Standard Cells

Description:
NO51 is a five-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06
E	0.06

Equivalent Gates:.....2.0
Bolt Syntax:.....Q .NO51 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.22	nA
†C_{pd}	0.21	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

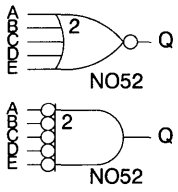
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	1.06	4.03	1.63	2.23	3.46
		t_{PHL}	0.37	1.51	0.58	0.81	1.27

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

1.0 micron Mixed Signal

Description:
NO52 is a five-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.12
B	0.12
C	0.12
D	0.12
E	0.12

Equivalent Gates:.....3.3
Bolt Syntax:.....Q .NO52 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.43	nA
†C_{pd}	0.38	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	1.01	2.06	1.30	1.61	2.24
		t_{PHL}	0.34	0.80	0.46	0.58	0.82

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

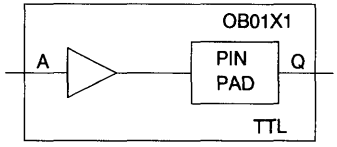
1.0 micron Mixed Signal

OB01X1

CYX 1.0 micron CMOS Standard Cells

Description:
OB01X1 is a 1mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.07

Bolt Syntax: .....Q .OB01X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	15.79	nA
†C_{pd}	7.49	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

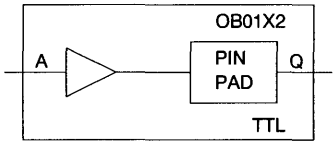
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	2.27	0.32	10.35	18.44	26.52	34.60
		t_{PHL}	2.74	0.41	13.00	23.27	33.54	43.80

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

Description:
OB01X2 is a 2mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.07

Bolt Syntax: ..... Q .OB01X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	15.79	nA
†C_{pd}	7.60	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	1.47	0.16	5.51	9.55	13.59	17.63
		t_{PHL}	1.86	0.20	6.99	12.11	17.23	22.35

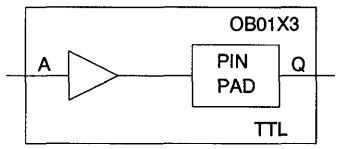
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB01X3

CYX 1.0 micron CMOS Standard Cells

Description:
OB01X3 is a 4mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.14

Bolt Syntax: ..... Q .OB01X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	17.41	nA
†C_{pd}	7.92	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

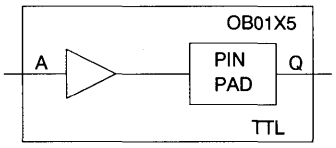
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.97	0.08	2.99	5.01	7.03	9.05
		t_{PHL}	1.09	0.10	3.65	6.21	8.77	11.33

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

Description:
OB01X5 is an 8mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.28

Bolt Syntax: ..... Q .OB01X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	19.64	nA
†C_{pd}	17.34	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, *Typical Process*

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.66	0.04	1.66	2.67	3.68	4.69
		t_{PHL}	0.88	0.05	2.15	3.42	4.70	5.97

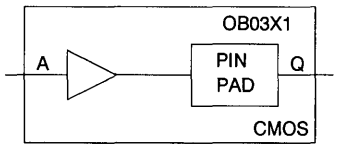
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB03X1

CYX 1.0 micron CMOS Standard Cells

Description:
OB03X1 is a 1mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.07

Bolt Syntax: .....Q .OB03X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	15.79	nA
†C_{pd}	7.49	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

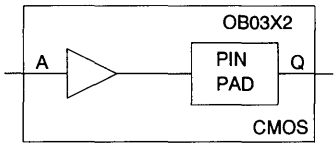
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	3.72	0.59	18.55	33.39	48.22	63.05
		t_{PHL}	1.93	0.28	8.83	15.73	22.64	29.54

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB03X2 is a 2mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.07

Bolt Syntax: .....Q .OB03X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	15.79	nA
†C_{pd}	7.60	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	2.18	0.30	9.59	17.00	24.41	31.82
		t_{PHL}	1.40	0.14	4.85	8.30	11.75	15.20

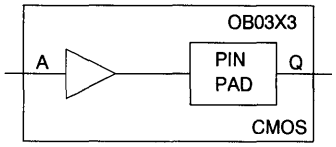
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB03X3

CYX 1.0 micron CMOS Standard Cells

Description:
OB03X3 is a 4mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.12

Bolt Syntax: .....Q .OB03X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	16.74	nA
†C_{pd}	7.89	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

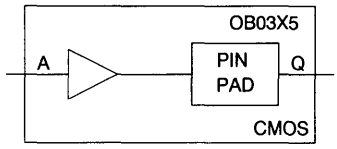
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	1.32	0.15	5.02	8.72	12.42	16.12
		t_{PHL}	1.00	0.07	2.73	4.45	6.17	7.90

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

1.0 micron Mixed Signal

Description:
OB03X5 is an 8mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.28

Bolt Syntax: .....Q .OB03X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	19.64	nA
†C_{pd}	17.34	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.84	0.07	2.69	4.55	6.40	8.25
		t_{PHL}	0.74	0.03	1.60	2.46	3.32	4.19

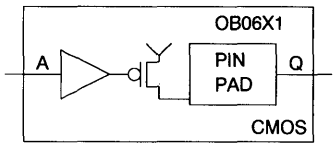
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB06X1

CYX 1.0 micron CMOS Standard Cells

Description:
OB06X1 is a 1mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.07
Q	7.25

Bolt Syntax: ..... Q .OB06X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	16.74	nA
†C_{pd}	7.53	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

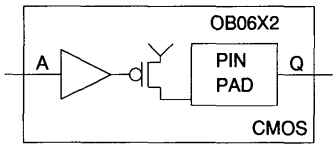
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH} t_{HZ}	0.00 0.59	0.59	14.83	29.66	44.48	59.31

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

1.0 micron Mixed Signal

Description:
OB06X2 is a 2mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.07
Q	7.26

Bolt Syntax: .....Q .OB06X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	16.74	nA
†C_{pd}	7.58	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH} t_{HZ}	0.07 0.74	0.30	7.47	14.87	22.27	29.68

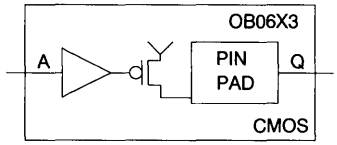
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

OB06X3

CYX 1.0 micron CMOS Standard Cells

Description:
OB06X3 is a 4mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.07
Q	7.26

Bolt Syntax: .....Q .OB06X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	17.41	nA
†C_{pd}	7.71	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

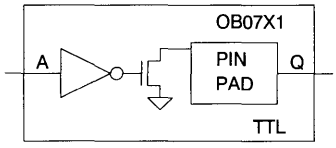
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH} t_{HZ}	0.52 0.94	0.15	4.22	7.92	11.62	15.32

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

1.0 micron Mixed Signal

Description:
OB07X1 is a 1mA, non-inverting, TTL-level, N-channel, open-drain (pull-down) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Ci (pF)
A	0.07
Q	7.25

Bolt Syntax: .....Q .OB07X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	15.79	nA
†C_{pd}	7.42	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PHL} t_{LZ}	0.00 0.35	0.41	10.28	20.56	30.84	41.12

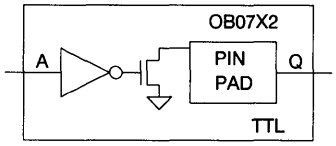
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB07X2

CYX 1.0 micron CMOS Standard Cells

Description:
OB07X2 is a 2mA, non-inverting, TTL-level, N-channel, open-drain (pull-down) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Ci (pF)
A	0.07
Q	7.26

Bolt Syntax: ..... Q .OB07X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	15.79	nA
†C_{pd}	7.47	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

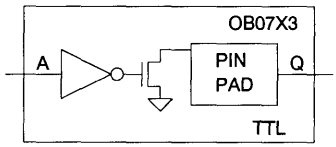
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PHL} t_{LZ}	0.03 0.44	0.21	5.17	10.31	15.44	20.58

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

1.0 micron Mixed Signal

Description:
OB07X3 is a 4mA, non-inverting,TTL-level, N-channel, open-drain (pull-down) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Ci (pF)
A	0.07
Q	7.26

Bolt Syntax: .....Q .OB07X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	16.13	nA
†C_{pd}	7.59	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

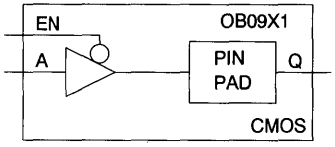
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PHL} t_{LZ}	0.29 0.89	0.10	2.85	5.41	7.98	10.54

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
OB09X1 is a 1mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
Q	7.25

Bolt Syntax: ..... Q .OB09X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	18.44	nA
†C_{pd}	7.76	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

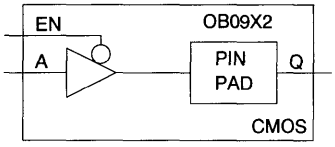
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.00	0.59	14.83	29.66	44.49	59.32
		t_{PHL}	0.12	0.28	7.03	13.93	20.84	27.75
EN	Q	t_{HZ}	0.85					
		t_{LZ}	0.46					
		t_{ZH}	0.00	0.59	14.83	29.66	44.49	59.32
		t_{ZL}	0.16	0.28	7.07	13.98	20.88	27.79

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB09X2 is a 2mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
Q	7.26

Bolt Syntax: .....Q .OB09X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	18.44	nA
†C_{pd}	7.88	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.00	0.30	7.40	14.81	22.21	29.62
		t_{PHL}	0.48	0.14	3.93	7.37	10.81	14.26
EN	Q	t_{HZ}	1.02					
		t_{LZ}	0.57					
		t_{ZH}	0.18	0.30	7.59	14.99	22.40	29.80
		t_{ZL}	0.52	0.14	3.97	7.41	10.86	14.30

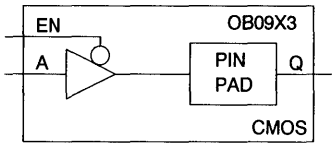
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB09X3

CYX 1.0 micron CMOS Standard Cells

Description:
OB09X3 is a 4mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.16
EN	0.14
Q	7.26

Bolt Syntax: .....Q .OB09X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	19.97	nA
†C_{pd}	8.20	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

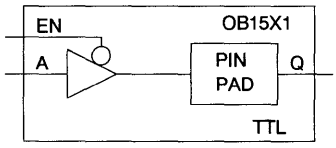
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.28	0.15	3.97	7.67	11.36	15.06
		t_{PHL}	0.70	0.07	2.43	4.16	5.89	7.61
EN	Q	t_{HZ}	1.23					
		t_{LZ}	1.02					
		t_{ZH}	0.42	0.15	4.12	7.82	11.51	15.21
		t_{ZL}	0.74	0.07	2.47	4.20	5.93	7.66

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB15X1 is a 1mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
Q	7.25

Bolt Syntax: .....Q .OB15X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	18.44	nA
†C_{pd}	7.76	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.00	0.32	8.08	16.16	24.25	32.33
		t_{PHL}	0.00	0.41	10.28	20.56	30.84	41.12
EN	Q	t_{HZ}	0.85					
		t_{LZ}	0.46					
		t_{ZH}	0.10	0.32	8.18	16.26	24.34	32.43
		t_{ZL}	0.00	0.41	10.28	20.56	30.84	41.12

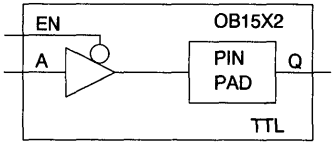
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB15X2

CYX 1.0 micron CMOS Standard Cells

Description:
OB15X2 is a 2mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.13
EN	0.13
Q	7.26

Bolt Syntax: .....Q .OB15X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	18.44	nA
$^{\dagger}C_{pd}$	7.88	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

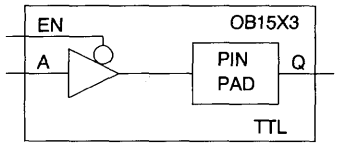
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.26	0.16	4.30	8.34	12.37	16.41
		t_{PHL}	0.46	0.20	5.58	10.69	15.80	20.91
EN	Q	t_{HZ}	1.02					
		t_{LZ}	0.57					
		t_{ZH}	0.45	0.16	4.49	8.53	12.56	16.60
		t_{ZL}	0.50	0.20	5.61	10.73	15.84	20.95

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB15X3 is a 4mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.16
EN	0.14
Q	7.26

Bolt Syntax: .....Q .OB15X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	19.97	nA
†C_{pd}	8.20	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.39	0.08	2.41	4.42	6.43	8.44
		t_{PHL}	0.67	0.10	3.24	5.82	8.39	10.96
EN	Q	t_{HZ}	1.23					
		t_{LZ}	1.02					
		t_{ZH}	0.54	0.08	2.55	4.57	6.58	8.59
		t_{ZL}	0.73	0.10	3.30	5.87	8.44	11.01

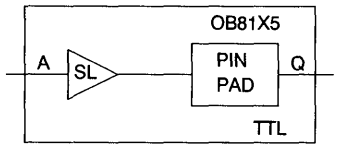
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB81X5

CYX 1.0 micron CMOS Standard Cells

Description:
OB81X5 is an 8mA, non-inverting, TTL-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.31
Q	7.58

Bolt Syntax: .....Q .OB81X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	20.39	nA
†C_{pd}	18.04	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

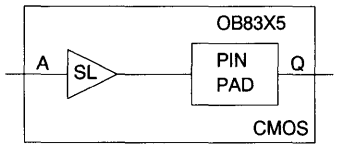
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.79	0.05	2.13	3.48	4.82	6.16
		t_{PHL}	1.23	0.10	3.75	6.26	8.78	11.29

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB83X5 is an 8mA, non-inverting, CMOS-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.31
Q	7.58

Bolt Syntax: .....Q .OB83X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	20.39	nA
†C_{pd}	18.04	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	1.06	0.10	3.51	5.96	8.41	10.86
		t_{PHL}	0.98	0.07	2.70	4.43	6.15	7.88

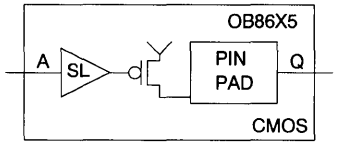
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB86X5

CYX 1.0 micron CMOS Standard Cells

Description:
OB86X5 is an 8mA, inverting, CMOS-level, output buffer pad with a P-channel open-drain (pull-up) and controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.07
Q	7.50

Bolt Syntax: ..... Q .OB86X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	19.33	nA
†C_{pd}	8.46	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

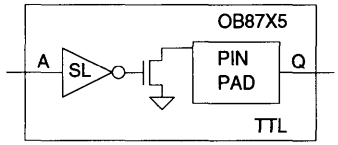
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH} t_{HZ}	1.33 1.17	0.10	3.78	6.23	8.68	11.13

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

1.0 micron Mixed Signal

Description:
OB87X5 is an 8mA, non-inverting, TTL-level, output buffer pad with N-channel open-drain (pull-down) and controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Ci (pF)
A	0.15
Q	7.52

Bolt Syntax: ..... Q .OB87X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	16.86	nA
†C_{pd}	17.63	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†*Note: C_{pd} does not include interconnect capacitance.*

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PHL} t_{LZ}	1.23 0.86	0.10	3.74	6.26	8.78	11.30

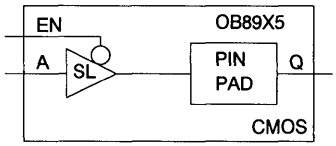
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB89X5

CYX 1.0 micron CMOS Standard Cells

Description:
OB89X5 is an 8mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.32
EN	0.21
Q	7.58

Bolt Syntax: ..... Q .OB89X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	23.67	nA
†C_{pd}	18.60	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

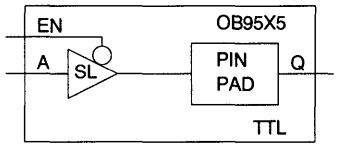
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.43	0.10	2.89	5.35	7.81	10.26
		t_{PHL}	0.98	0.07	2.71	4.44	6.17	7.90
EN	Q	t_{HZ}	1.37					
		t_{LZ}	1.08					
		t_{ZH}	0.76	0.10	3.22	5.68	8.14	10.60
		t_{ZL}	1.00	0.07	2.73	4.47	6.20	7.93

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB95X5 is an 8mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.32
EN	0.21
Q	7.58

Bolt Syntax: .....Q .OB95X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	23.67	nA
†C_{pd}	18.60	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

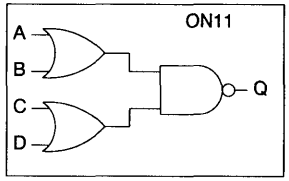
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	0.51	0.05	1.84	3.18	4.52	5.86
		t_{PHL}	0.98	0.10	3.53	6.08	8.62	11.17
EN	Q	t_{HZ}	1.38					
		t_{LZ}	1.08					
		t_{ZH}	0.83	0.05	2.17	3.51	4.85	6.19
		t_{ZL}	1.01	0.10	3.56	6.11	8.65	11.20

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
ON11 is an OR-NAND circuit consisting of two 2-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
H	X	H	X	L
H	X	X	H	L
X	H	H	X	L
X	H	X	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .ON11 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.04	nA
†C_{pd}	0.22	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

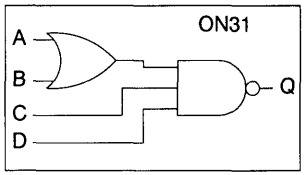
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.56	1.98	0.84	1.13	1.73
		t_{PHL}	0.32	1.03	0.47	0.62	0.94

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
ON31 is an OR-NAND circuit consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	X	H	H	L
X	H	H	H	L

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .ON31 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.47	nA
†C_{pd}	0.18	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.44	2.46	0.79	1.15	1.90
		t_{PHL}	0.33	1.38	0.52	0.73	1.15

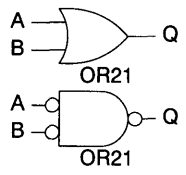
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

OR21

CYX 1.0 micron CMOS Standard Cells

Description:
OR21 is a two-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06

Equivalent Gates:.....1.3
Bolt Syntax:.....Q .OR21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.97	nA
†C_{pd}	0.20	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

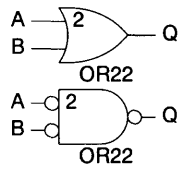
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.37	1.13	0.53	0.70	1.04
		t_{PHL}	0.50	0.97	0.64	0.78	1.08

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OR22 is a two-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06

Equivalent Gates:.....1.6
Bolt Syntax:.....Q .OR22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.92	nA
†C_{pd}	0.26	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.42	0.60	0.50	0.59	0.78
		t_{PHL}	0.59	0.63	0.68	0.77	0.97

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

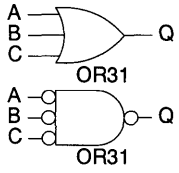
OR31

AMI SEMICONDUCTORS

CYX 1.0 micron CMOS Standard Cells

Description:
OR31 is a three-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06

Equivalent Gates:.....1.6
Bolt Syntax:.....Q .OR31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.04	nA
†C_{pd}	0.25	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

1.0 micron Mixed Signal

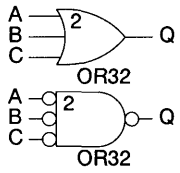
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.48	1.16	0.64	0.82	1.17
		t_{PHL}	0.80	1.13	0.96	1.13	1.47

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OR32 is a three-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06

Equivalent Gates:.....1.9
Bolt Syntax:.....Q .OR32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.99	nA
†C_{pd}	0.31	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.52	0.64	0.61	0.71	0.90
		t_{PHL}	0.91	0.74	1.01	1.12	1.35

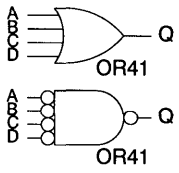
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OR41

CYX 1.0 micron CMOS Standard Cells

Description:
OR41 is a four-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06

Equivalent Gates:.....1.9
Bolt Syntax:.....Q .OR41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.10	nA
†C_{pd}	0.28	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

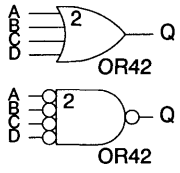
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.56	1.21	0.74	0.92	1.28
		t_{PHL}	1.08	1.27	1.26	1.45	1.84

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

1.0 micron Mixed Signal

Description:
OR42 is a four-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Pin Loading

	Ci (pF)
A	0.06
B	0.06
C	0.06
D	0.06

Equivalent Gates:.....2.3
Bolt Syntax:.....Q .OR42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.05	nA
†C_{pd}	0.34	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
Any Input	Q	t_{PLH}	0.62	0.67	0.72	0.82	1.02
		t_{PHL}	1.22	0.83	1.34	1.46	1.72

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

PORA

CYX 1.0 micron CMOS Standard Cells

Description:

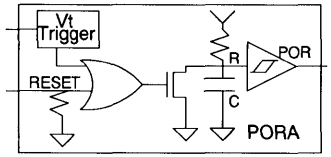
PORA is a power-on-reset circuit for 5 volt operation.

When power is applied, the POR output is asserted low for at least 400 nanoseconds after the logic circuits become operational. The active-high RESET input also drives the POR signal to its active low state.

For proper operation, user-designed external circuitry must limit the slew rate of Vdd power to a maximum of one volt per microsecond. This ensures that the reset pulse will be properly output when Vdd falls to zero and immediately returns to its valid range.

PORA will work at Vdd voltages down to 3.0 volts. For operation with Vdd voltage below 4.5 volts, user-designed external circuitry must limit maximum Vdd slew rate to 0.5 volts per microsecond.

Logic Symbol



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Ci (pF)
RESET	0.24

Equivalent Gates: 98.2

Bolt Syntax: ..... POR .PORA RESET;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	8.39	nA
†C_{pd}	45.97	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
RESET	POR	t_{PLH} t_{PHL}	3827.05 18.24	1.30 0.83	3827.23 18.36	3827.43 18.48	3827.82 18.73
VDD	POR	t_{PLH}	4602.93	1.30	4603.11	4603.31	4603.71

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:

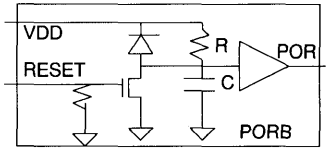
PORB is a power-on-reset circuit for 3 volt operation.

The POR output is active low. The active-high RESET input can also drive the POR line low.

PORB is designed for rapidly rising Vdd power associated with battery-operated equipment. For proper operation, Vdd slew rate must be faster than 7.5 volts per microsecond.

The POR output will remain low at least 50 ns after Vdd reaches a valid 3 volt level.

Logic Symbol



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Ci (pF)
RESET	0.12

Equivalent Gates:.....104.7

Bolt Syntax:.....POR .PORB RESET;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	7.03	nA
†C_{pd}	42.10	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

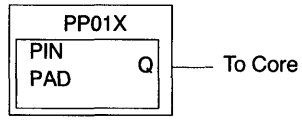
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
RESET	POR	t_{PLH} t_{PHL}	1142.50 21.33	1.00 3.66	1142.64 21.85	1142.79 22.39	1143.10 23.51
VDD	POR	t_{PLH}	1122.46	1.00	1122.60	1122.75	1123.06

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

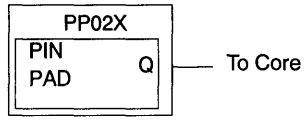
PP01X

CYX 1.0 micron CMOS Standard Cells

Description:
PP01X is a Vss power supply pin for output buffers, input buffers, and core cells combined. The PP01X is intended for circumstances where output and core busses are to be tied together. It should not be used in conjunction with PPP1X or PPC1X.

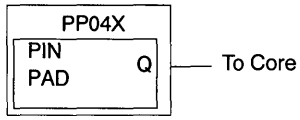


Description:
PP02X is a Vdd power supply pin for output buffers, input buffers, and core cells combined. One PP02X must be used for each power (VDD) pin.

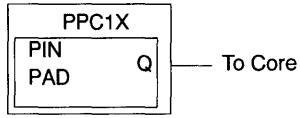


CYX 1.0 micron CMOS Standard Cells

Description:
PP04X is an optional power supply pin for connecting additional buses.



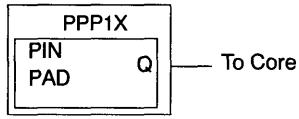
Description:
PPC1X is a Vss power supply pin for core cells and input buffers only. One PPC1X must be used for each ground (VSS) pin for the core cells and input buffers.



PPP1X

CYX 1.0 micron CMOS Standard Cells

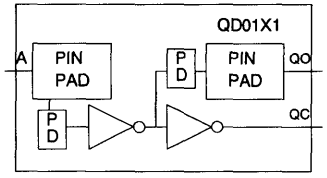
Description:
PPP1X is a Vss power supply pin for output buffers only. One PPP1X must be used for each ground (VSS) pin.



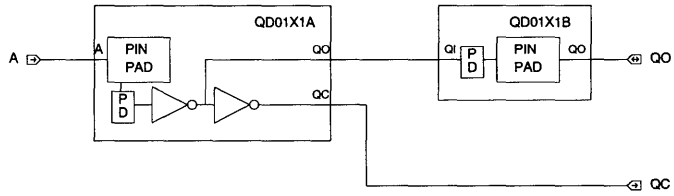
Description:

QD01X1 is a 3.58 MHz(1MHz - 10 MHz) crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Ci (pF)
A	5.16
QO	5.16

Bolt Syntax: .....QC QO .QD01X1A A;

.....QI QO .QD01X1B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.78	nA
†C_{pd}	5.74	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
QO	QC	t_{PLH}	0.30	0.96	0.43	0.58	0.87
		t_{PHL}	0.35	1.06	0.51	0.99	0.99

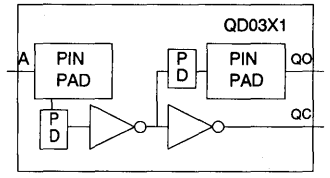
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

QD03X1

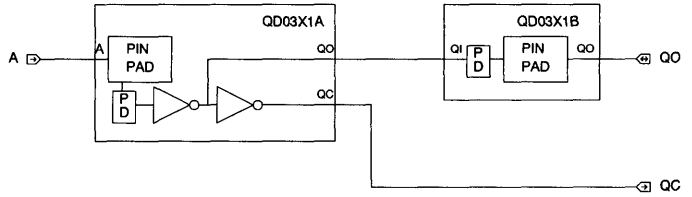
CYX 1.0 micron CMOS Standard Cells

Description:
QD03X1 is a 20 MHz (10 MHz - 32 MHz) crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Ci (pF)
A	5.30
QO	5.30

Bolt Syntax: .....QC QO .QD03X1A A;
.....QI QO .QD03X1B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	6.54	nA
†C_{pd}	6.08	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

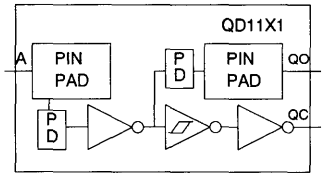
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
QO	QC	t_{PLH}	0.24	0.77	0.35	0.46	0.70
		t_{PHL}	0.36	0.94	0.50	0.64	0.92

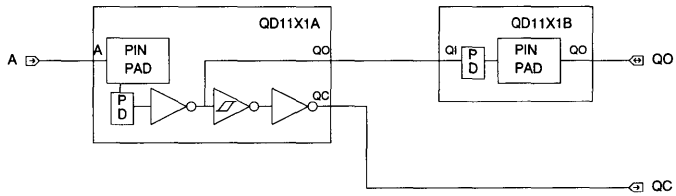
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
QD11X1 is a 32kHz (32kHz - 1MHz) crystal oscillator with Schmitt trigger. QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	H	H
H	L	L

Pin Loading

	Ci (pF)
A	5.15
QO	5.15

Bolt Syntax: .....QC QO .QD11X1A A;
.....QI QO .QD11X1B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.99	nA
†C_{pd}	5.71	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

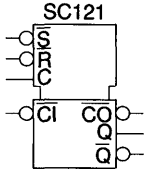
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
QO	QC	t_{PLH}	2.01	1.02	2.15	2.30	2.61
		t_{PHL}	1.54	0.87	1.67	1.80	2.06

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CYX 1.0 micron CMOS Standard Cells

Description:
SC121 is a static, master-slave, synchronous up-counter bit with ripple carry. SET and RESET are asynchronous and active low. Outputs are buffered. The output toggles on the rising edge of the clock when CIN is active low.

Logic Symbol



Truth Table

RN	SN	CIN	C	CON(n+1)	Q(n+1)	QN(n+1)
L	L	X	X	-	IL	IL
L	H	X	X	-	L	H
H	L	X	X	-	H	L
H	H	L	↑	-	QN(n)	Q(n)
H	H	H	↑	-	NC	NC
X	X	L	X	QN(n+1)	-	-
X	X	H	X	H	-	-

IL = Illegal NC=No Change

Pin Loading

	Ci (pF)
C	0.17
SN	0.12
RN	0.12
CIN	0.12

Equivalent Gates:.....12.1
Bolt Syntax:.....CON Q QN .SC121 C CIN RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.06	nA
†C_{pd}	2.02	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

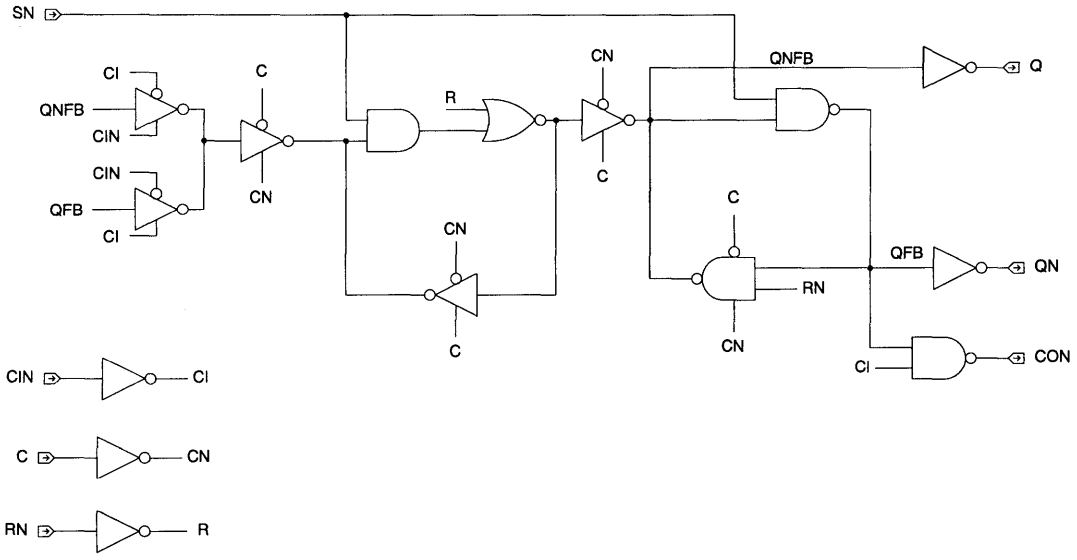
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.73 0.98	1.29 1.23	0.91 1.15	1.10 1.34	1.49 1.71
C	QN	t_{PLH} t_{PHL}	1.66 1.31	1.28 1.12	1.84 1.47	2.03 1.63	2.42 1.98
C	CON	t_{PLH} t_{PHL}	1.72 1.37	1.44 1.31	1.92 1.56	2.14 1.75	2.58 2.15
CIN	CON	t_{PLH} t_{PHL}	0.44 0.41	1.44 1.31	0.64 0.60	0.85 0.79	1.29 1.19
RN	Q	t_{PHL}	1.45	1.23	1.63	1.81	2.19
RN	QN	t_{PLH}	2.13	1.28	2.31	2.50	2.90
RN	CON	t_{PLH}	2.19	1.44	2.40	2.61	3.05
SN	Q	t_{PLH}	1.61	1.29	1.79	1.98	2.38

(continued on next page)

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
SN	QN	t_{PHL}	0.71	1.12	0.87	1.04	1.38
SN	CON	t_{PHL}	0.78	1.31	0.96	1.16	1.55
Min C Width	High	t_w	1.39				
Min C Width	Low	t_w	0.91				
Min RN Width	Low	t_w	2.18				
Min SN Width	Low	t_w	1.28				
Min CIN Setup		t_{su}	1.26				
Min CIN Hold		t_h	0.00				
Min RN Setup		t_{su}	0.66				
Min RN Hold		t_h	1.41				
Min SN Setup		t_{su}	0.36				
Min SN Hold		t_h	0.59				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



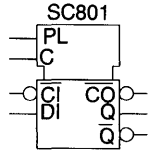
1.0 micron Mixed Signal

SC801

CYX 1.0 micron CMOS Standard Cells

Description:
SC801 is a static, master-slave, synchronous up-counter bit with ripple carry. The output toggles on the rising edge of the clock when CIN is active low. Parallel load is asynchronous and active high. Outputs are buffered.

Logic Symbol



Truth Table

DI	PL	CIN	C	CON	Q(n+1)	QN(n+1)
X	L	H	↑	-	NC	NC
X	L	L	↑	-	QN(n)	Q(n)
L	H	X	X	-	L	H
H	H	X	X	-	H	L
X	X	H	X	H	-	-
X	X	L	X	QN(n)	-	-

NC=No Change

Pin Loading

	Ci (pF)
DI	0.12
CIN	0.12
C	0.17
PL	0.12

Equivalent Gates:.....16.6
Bolt Syntax:.....CON Q QN .SC801 C CIN DI PL;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	19.69	nA
†C_{pd}	2.59	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

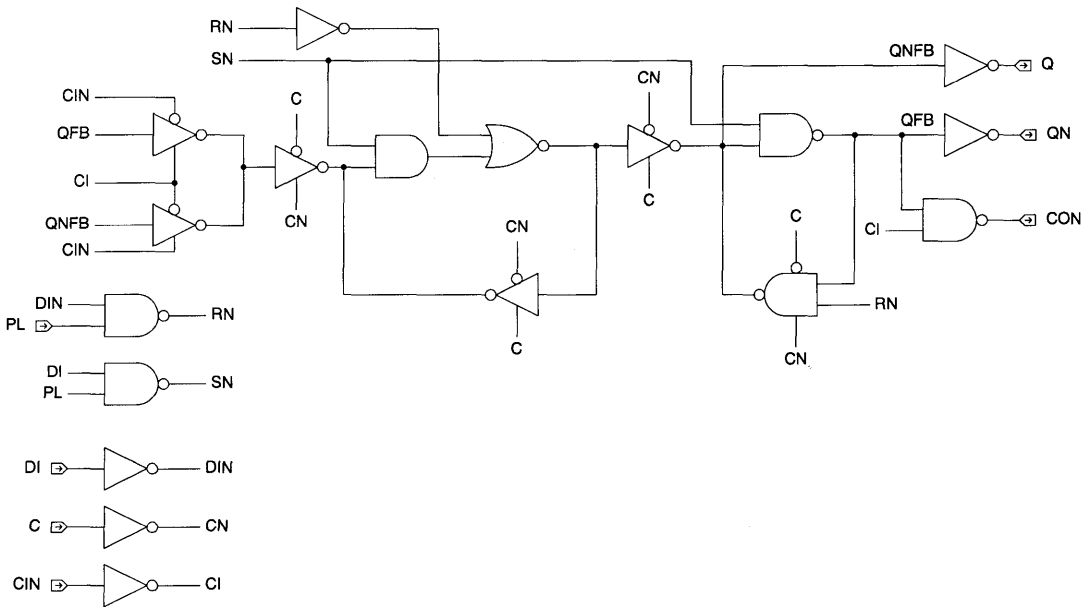
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.74 1.03	1.29 1.24	0.92 1.20	1.12 1.39	1.51 1.77
C	QN	t_{PLH} t_{PHL}	1.72 1.33	1.29 1.12	1.90 1.49	2.09 1.66	2.49 2.00
C	CON	t_{PLH} t_{PHL}	1.78 1.39	1.44 1.31	1.99 1.58	2.20 1.77	2.64 2.17
DI	Q	t_{PLH} t_{PHL}	2.11 2.03	1.29 1.24	2.30 2.21	2.49 2.39	2.88 2.77
DI	QN	t_{PLH} t_{PHL}	2.72 1.04	1.29 1.12	2.90 1.20	3.09 1.37	3.49 1.71
DI	CON	t_{PLH}	2.78	1.44	2.98	3.20	3.64
PL	Q	t_{PLH} t_{PHL}	1.95 1.81	1.29 1.24	2.13 1.99	2.32 2.18	2.72 2.55

(continued on next page)

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
PL	QN	t_{PLH} t_{PHL}	2.50 1.07	1.29 1.12	2.69 1.23	2.88 1.40	3.27 1.74
PL	CON	t_{PLH} t_{PHL}	2.56 1.13	1.44 1.31	2.77 1.32	2.98 1.51	3.42 1.91
CIN	CON	t_{PLH} t_{PHL}	0.44 0.42	1.44 1.31	0.64 0.60	0.86 0.80	1.30 1.20
Min C Width	High	t_w	1.45				
Min C Width	Low	t_w	0.90				
Min CIN Setup		t_{su}	1.55				
Min CIN Hold		t_h	0.00				
Min PL Width	High	t_w	2.44				
Min DI Setup to PL		t_s	0.34				
Min DI Hold to PL		t_h	2.44				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

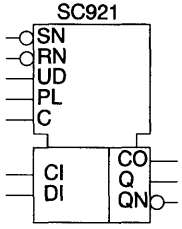
Logic Schematic



CYX 1.0 micron CMOS Standard Cells

Description:
SC921 is a static, master-slave, synchronous up/down-counter bit with ripple carry. The output toggles on the rising edge of the clock when CI is active high. SET and RESET are asynchronous and active low. Parallel load is synchronous and active high. Outputs are buffered.

Logic Symbol



Pin Loading

	Ci (pF)
DI	0.06
CI	0.18
C	0.18
PL	0.12
UD	0.12
RN	0.13
SN	0.12

Truth Table

RN	SN	CI	UD	PL	DI	C	CO	Q(n+1)	QN(n+1)
H	H	X	X	H	L	↑	-	L	H
H	H	X	X	H	H	↑	-	H	L
H	H	X	X	X	X	L	-	NC	NC
H	H	L	X	L	X	↑	-	NC	NC
H	H	H	X	L	X	↑	-	QN(n)	Q(n)
L	H	X	X	X	X	X	-	L	H
H	L	X	X	X	X	X	-	H	L
L	L	X	X	X	X	X	-	IL	IL
X	X	L	X	X	X	X	L	-	-
X	X	H	H	X	X	X	Q(n)	-	-
X	X	H	L	X	X	X	QN(n)	-	-

IL = Illegal NC = No Change

Equivalent Gates:.....18.3
Bolt Syntax:.....CO Q QN .SC921 C CI DI PL RN SN UD;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	23.62	nA
†C_{pd}	3.04	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

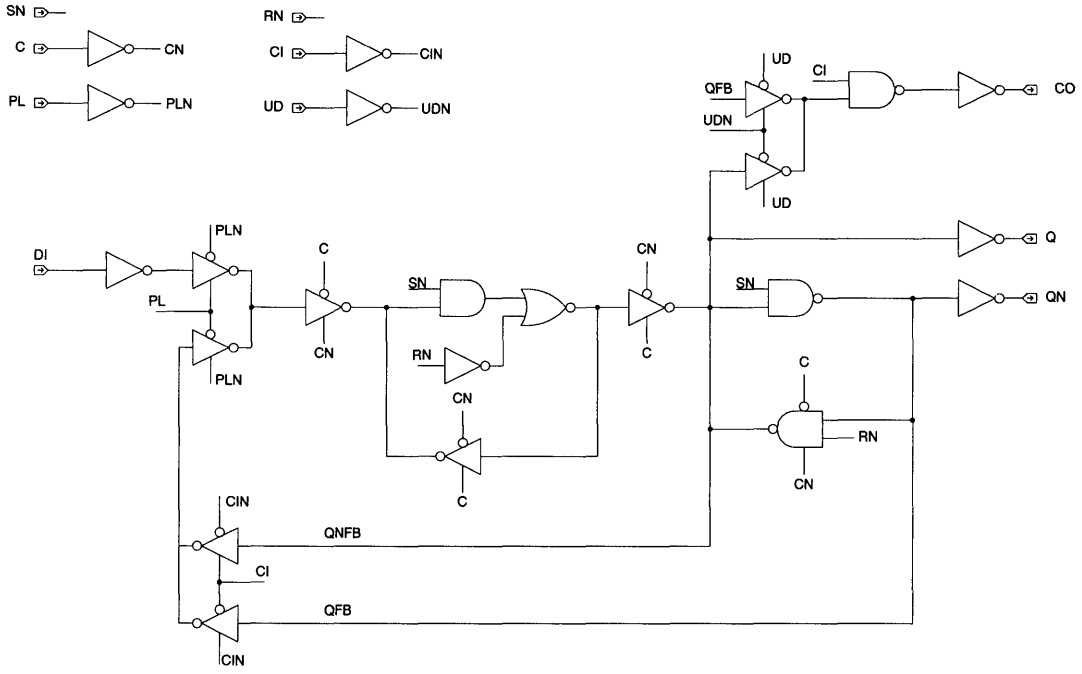
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
C	Q	t_{PLH} t_{PHL}	0.84 1.15	1.34 1.33	1.03 1.34	1.23 1.53	1.64 1.94
C	QN	t_{PLH} t_{PHL}	1.87 1.45	1.28 1.13	2.05 1.61	2.25 1.78	2.64 2.12
C	CO	t_{PLH} t_{PHL}	1.57 2.02	1.14 0.87	1.73 2.14	1.90 2.27	2.25 2.54
CI	CO	t_{PLH} t_{PHL}	0.37 0.38	1.14 0.87	0.53 0.50	0.70 0.63	1.05 0.90
UD	CO	t_{PLH} t_{PHL}	0.96 1.06	1.14 0.87	1.12 1.18	1.29 1.31	1.64 1.58
RN	Q	t_{PHL}	1.61	1.33	1.80	2.00	2.40
RN	QN	t_{PLH}	2.35	1.28	2.53	2.72	3.11
SN	Q	t_{PHL}	1.70	1.34	1.89	2.09	2.50
SN	QN	t_{PLH}	0.72	1.13	0.88	1.05	1.39
Min C Width	High	t_w	1.61				
Min C Width	Low	t_w	0.98				
Min RN Width	Low	t_w	2.07				
Min SN Width	Low	t_w	1.35				
Min CI Setup		t_{su}	1.93				
Min CI Hold		t_h	0.00				
Min CI Setup to PL		t_s	0.97				
Min DI Setup		t_{su}	1.56				
Min DI Hold		t_h	0.00				
Min DI Setup to PL		t_s	0.36				
Min PL Setup		t_{su}	1.29				
Min PL Hold		t_h	0.00				
Min RN Setup		t_{su}	0.69				
Min RN Hold		t_h	0.75				
Min SN Setup		t_{su}	0.38				
Min SN Hold		t_h	0.43				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

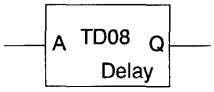
CYX 1.0 micron CMOS Standard Cells

Logic Schematic



Description:
TD08 is a non-inverting time delay.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.09

Equivalent Gates:.....5.1
Bolt Syntax:.....Q .TD08 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	6.26	nA
†C_{pd}	1.66	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.14pF)	4 (0.29pF)	8 (0.60pF)
A	Q	t_{PLH}	6.62	0.69	6.71	6.82	7.03
		t_{PHL}	6.62	0.57	6.70	6.78	6.96

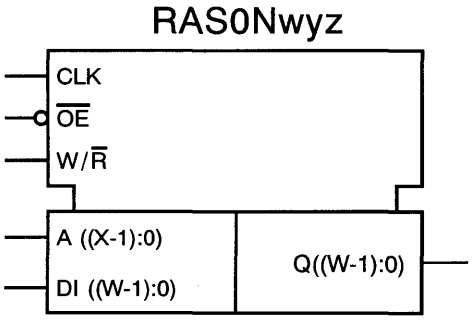
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

SECTION 10
CYX ROM/RAM DATA SHEETS

Features

- 8.24 nsec typical cycle time for a 32 x 4 RAM with a 0.5pF load
- Read-Modify-Write cycle possible
- Low standby power when the clock is stopped
- Separate input and output ports with full parallel access
- 3-State outputs interface internal data buses directly
- Precharged design for faster operation with less silicon area

FIGURE 1: LOGIC SYMBOL



Note 1: A0 is the LSB

Note 2: X represents the number of address lines

General Description

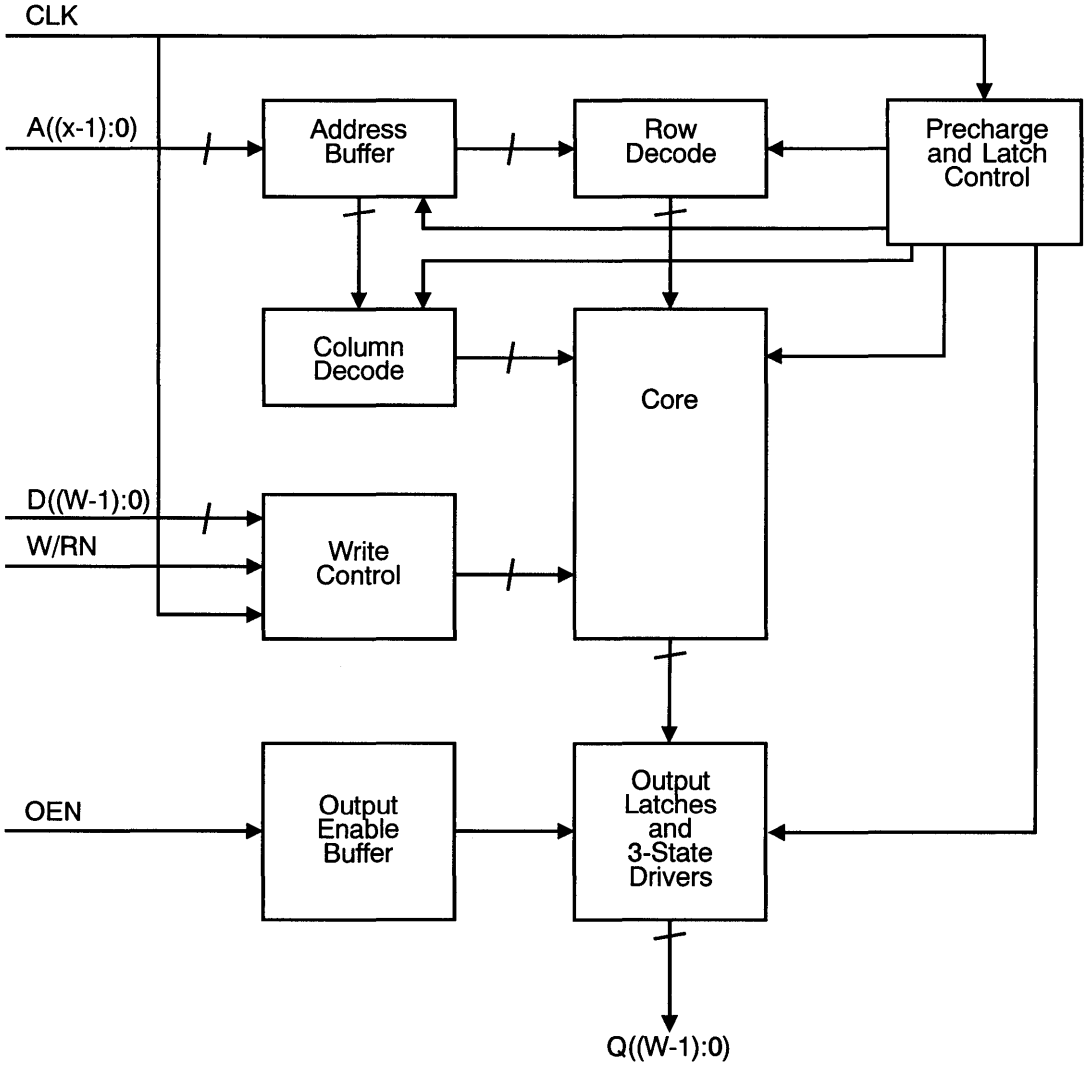
This series of 1.0 micron double-metal MxN RAMs operates within a power supply voltage range of 4.5V to 5.5V. The RASON series has 3-state outputs with active low Output Enable Not (OEN). The circuit is precharged when the clock is high, and the read and write operations occur when the clock is low. The outputs become valid a short time after the falling edge of the clock and stay valid until the next falling edge of the clock. The address lines are latched on the falling edge of the clock. The clock is used only to precharge the circuit and operate the latches; the memory does not need a refresh signal. The clock and all of the other inputs can be held stable indefinitely with no loss of memory as long as power is supplied to the RAM.

Within limits specified below, the user has flexibility in specifying the logical size of the RAM, including both word size and number of address locations. Within the name as shown above, the "wyz" represents a three character sequence assigned to each RAM configuration which uniquely identifies that particular configuration. Furthermore, the "S", "0", and "N" represent a single port RAM, version 0, and an active low output enable, respectively. The "W" represents a mod-36 alpha-numeric digit using the integers 1-9 and letters A-Z excluding O,Q,and V. For example, "N" represents a word-length of 23 and "P" represents a word-length of 24. The "yz" represents a hexadecimal value for the number of address locations divided by 16. For example, "04" represents 64 address locations.

In the logic symbol of figure 1, the "X" denotes the number of address lines. This value can be calculated by taking the log to the base 2 of the number of address locations. If the value returned is not an integer, round up. For example, for 64 address locations, "X" would be 6; for 80 address locations, "X" would be 7.

Performance data is listed below for two example sizes. To obtain data and a workstation installation (symbol and simulation model) for a specific size, contact the factory.

FIGURE 2: M X N RAM BLOCK DIAGRAM



Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Address Inputs	5	10	1(A0 is the LSB)
Word Size (Data Outputs)	1 bit	32 bits	1 bit
Address Locations (Words)	32	1024 (1K)	16
Total bits in a core (Word size times address locations)	32	32,768 (32K)	

Pin Description and Input Capacitance

SIGNAL	TYPE	32 X 4	1K X 16	SIGNAL DESCRIPTIONS
Ai	Input	0.08pF	0.08pF	Address Inputs
CLK	Input	0.25pF	0.38pF	Clock Input
OEN	Input	0.17pF	0.26pF	3-State Output Control
Q (High-Z)	Output	0.08pF	0.08pF	Data Outputs
W/RN	Input	0.05pF	0.05pF	Write/Read Not Control
Di	Input	0.06pF	0.06pF	Data Inputs

Contact the factory to obtain capacitance information about MXN RAM
Area relative to a 2 Input Nand
32 x 4: 409
1K x 16: 10938

Bolt Syntax

Q00 Q01 . . . Qw, .RASONwyz A0 A1 . . . Ax CLK DI00 DI01 . . . DIw OEN WRN;

Note: A0 is the LSB

AC Characteristics: t(CL)=tdx + Ktdx * CL

The data in the following examples are specified at 5.OV, Tj = 25°C, and typical process performance parameters. Performance at other operating points may be estimated by use of the Voltage, Process, and Temperature derating curves. Contact the factory to obtain the AC characteristics and input capacitance for different logical sizes of RAMs.

CYX 1.0 micron CMOS Standard Cells

32 x 4

CHARACTERISTIC	SYMBOL	tdx (ns)	ktdx (ns/pF)	t(0.5pF) (ns)
Min CLK Period Read	tclkr	7.74	1.00	8.24
Min CLK Period Write	tclkw	6.08		
Min CLK Width High	twch	2.7		
Min CLK Width Low During Read	twclr	5.05		
Max CLK Low to Q Delay	tpcq	5.05	1.00	5.55
Max OEN to Q Delay	toenq	0.81	1.00	1.31
Max OEN to High-Z Delay	toenz	0.63		
Min Address Setup Time**	tasu	1.29		
Min Address Hold Time**	tah	0.92		
Min W/RN High to Valid Write*	twvw	2.08		
Min Data in (Di) Stable to Valid Write*	tdvw	2.11		
Min CLK Low to Valid Write*	tcvw	3.38		
Min Data in (Di) Hold Time after Rising edge of CLK when W/RN is High*	tdh	1.08		
Min W/RN Hold Time After Read	twh	0.27		
Min Q Hold Time	tqh	0.89		

1K x 16

CHARACTERISTIC	SYMBOL	tdx (ns)	ktdx (ns/pF)	t(0.5pF) (ns)
Min CLK Period Read	tclkr	15.54	1.08	16.08
Min CLK Period Write	tclkw	12.59		
Min CLK Width High	twch	6.13		
Min CLK Width Low During Read	twclr	9.41		
Max CLK Low to Q Delay	tpcq	9.41	1.08	9.95
Max OEN to Q Delay	toenq	0.86	1.08	1.40
Max OEN to High-Z Delay	toenz	0.66		
Min Address Setup Time**	tasu	1.63		
Min Address Hold Time**	tah	1.13		
Min W/RN High to Valid Write	twvw	4.78		
Min Data in (Di) Stable to Valid Write*	tdvw	4.67		
Min CLK Low to Valid Write*	tcvw	6.46		
Min Data in (Di) Hold Time after Rising edge of CLK when W/RN is High*	tdh	1.44		
Min W/RN Hold Time After Read	twh	0.25		
Min Q Hold Time	tqh	1.0		

* If the W/RN line is high at the same time that the CLK line is low, all three timing terms twvw, tdvw, and tcvw must be met or else invalid data may be written into the RAM. A Read-Modify-Write cycle may be executed by leaving W/RN low until the read is accomplished, then meeting the twvw, tdvw, and tcvw timing terms to accomplish a valid write. The Q outputs will change to the value that is written. After a write, the Data In (Di) pins must be held stable until after W/RN falls or CLK rises.

** If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it will not show corrupted data.

Power Dissipation:

PARAMETER	32 X 4	1K X 16
Typical C_{pd} (Equivalent Power Dissipation Capacitance (pF))	20	160
Typical Static IDD Tj=85°C (μa)	1.20	6.8

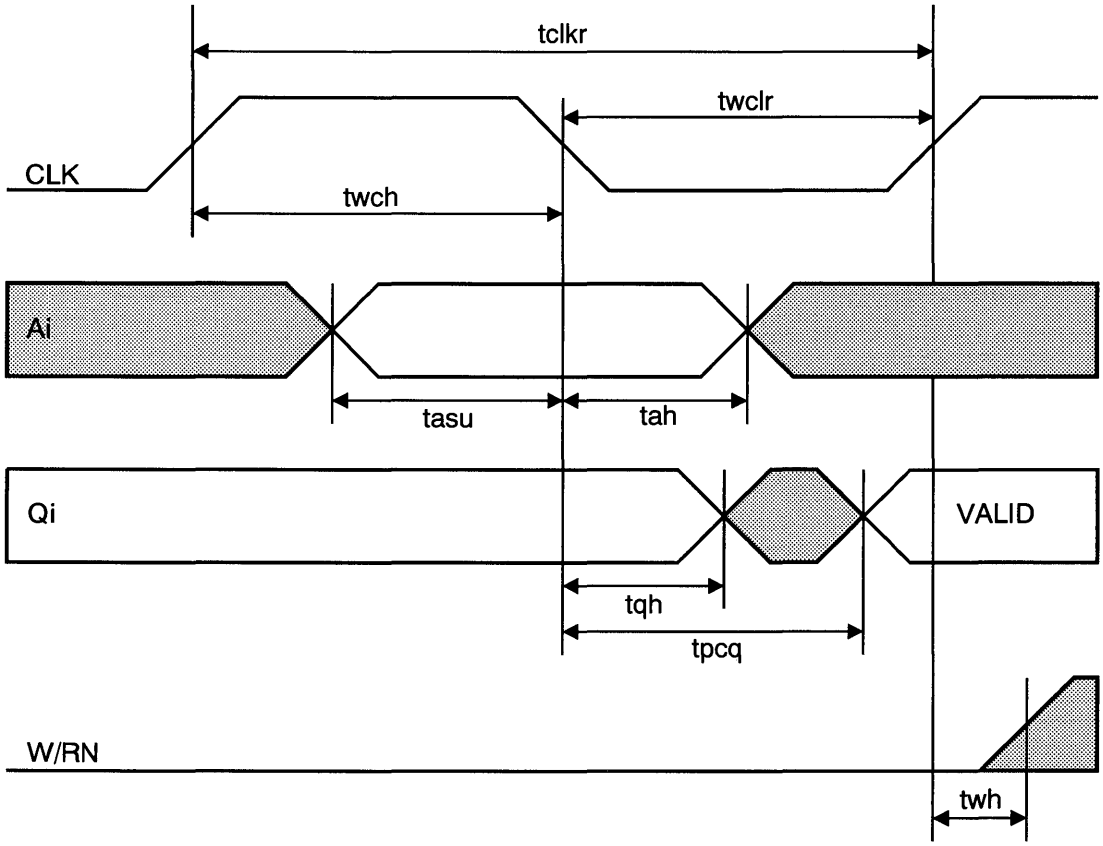
(See data book for power dissipation notes.)

Testing Notes:

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. For a more detailed description of the testing of memory elements in ICs, refer to the RAM testing application notes.

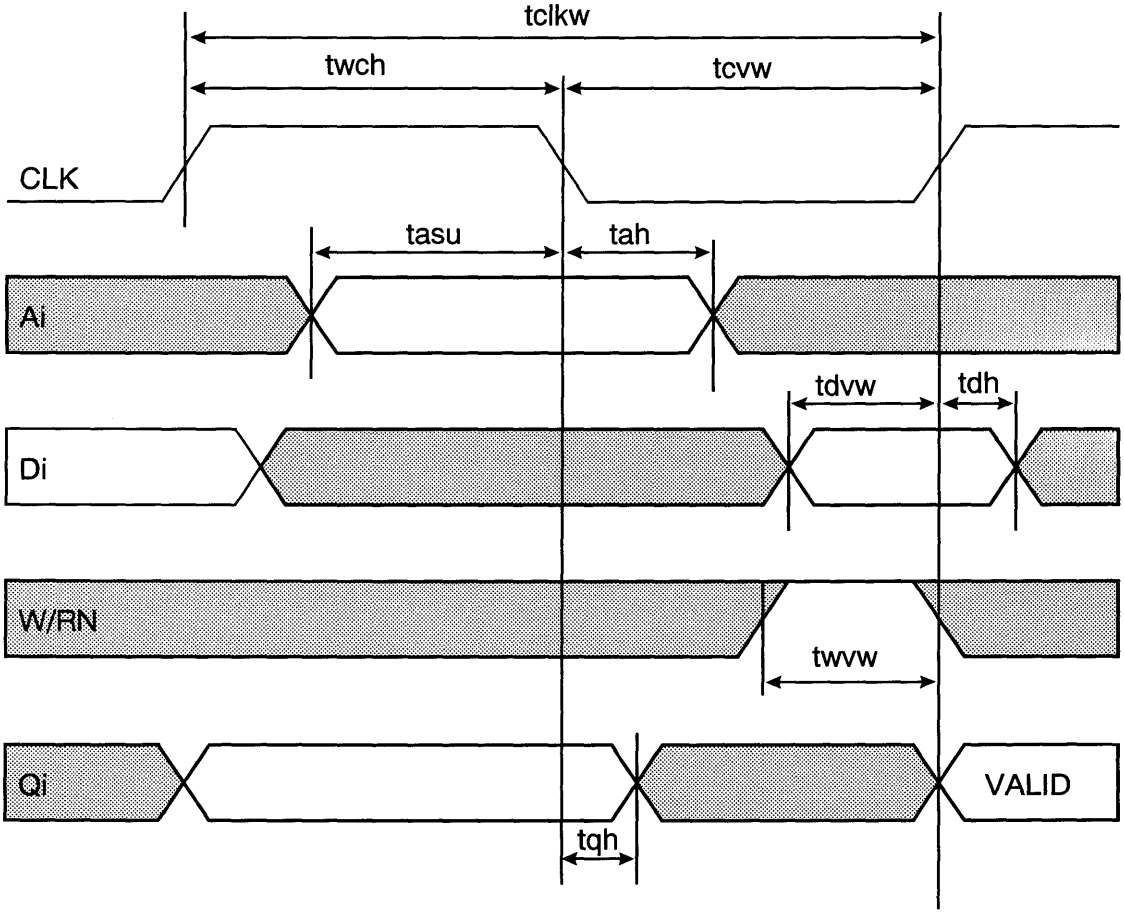
M X N RAM
Timing Diagram

Read Cycle



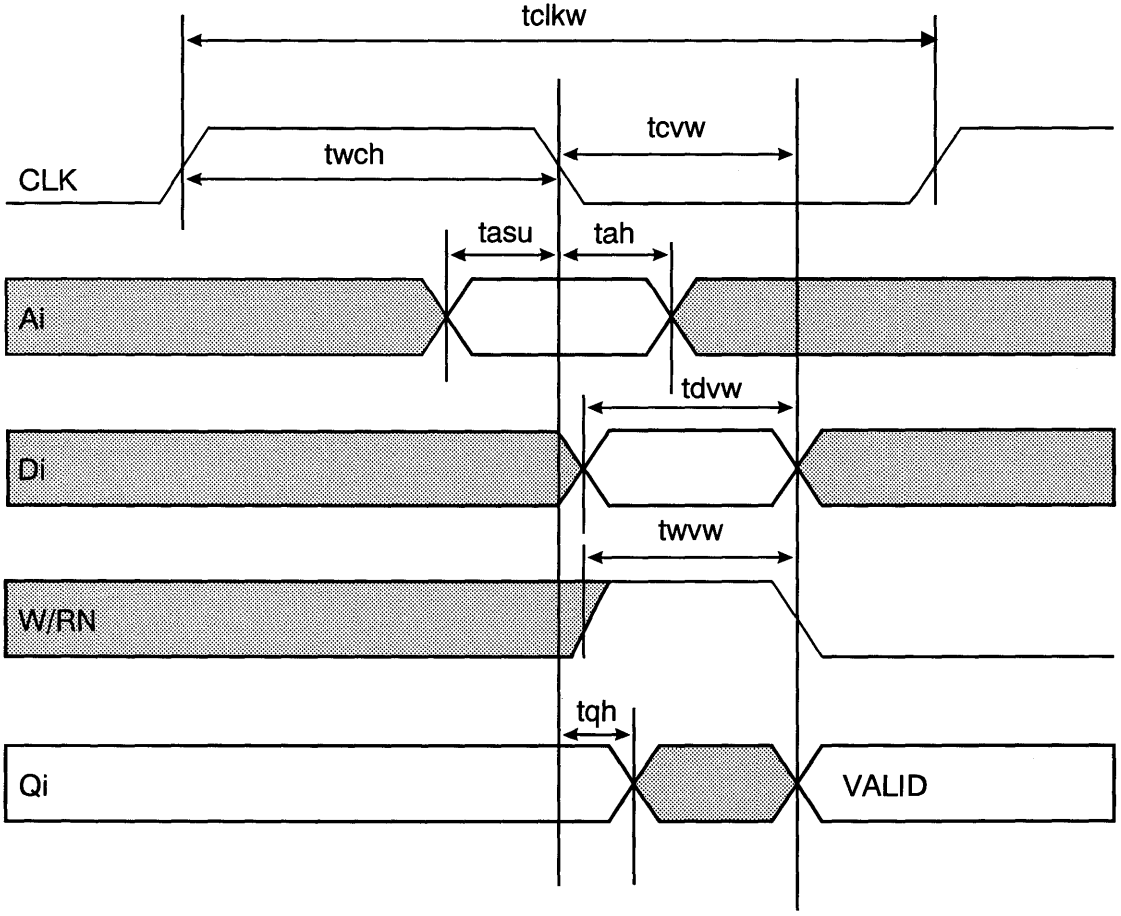
M X N RAM
Timing Diagram

Write Cycle 1 (See Notes 1 and 2)



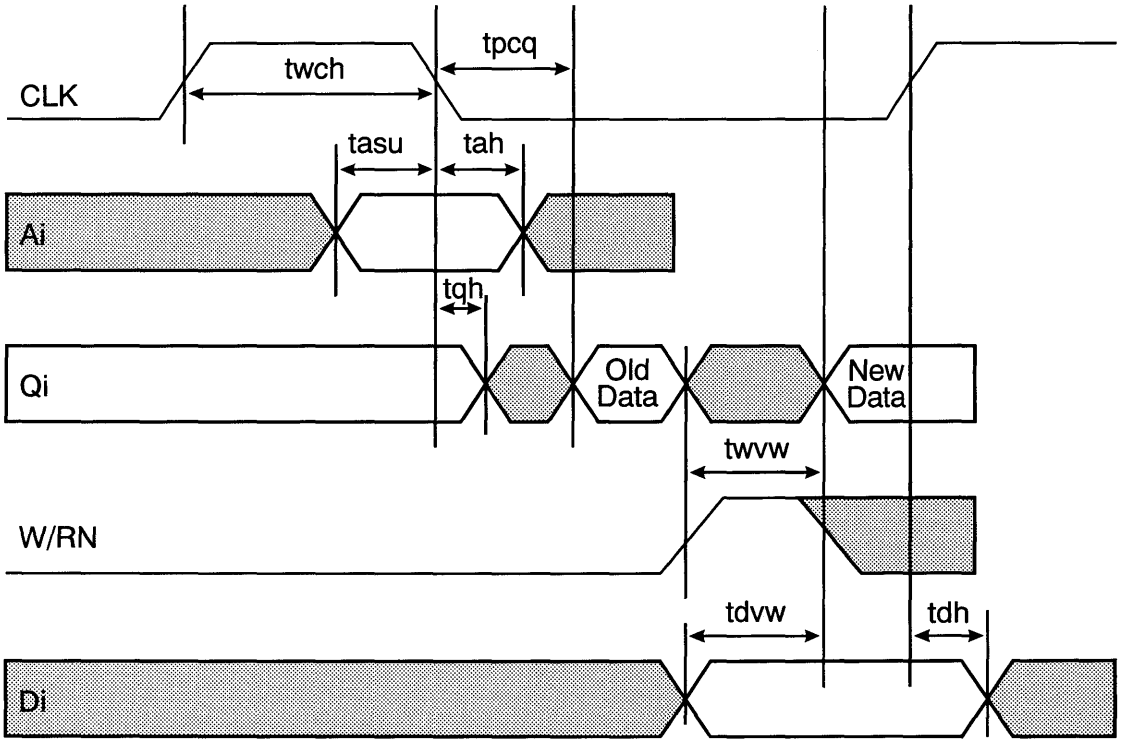
M X N RAM
Timing Diagram

Write Cycle 2 (See Notes 1 and 3)

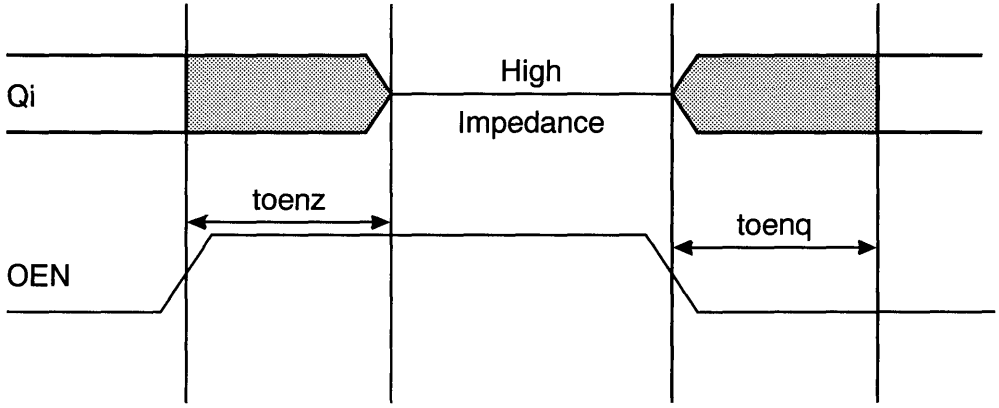


M X N RAM
Timing Diagram

Read-Modify-Write Cycle (See Note 4)



3-State Control Timing



Timing Diagram Notes

1. During a write cycle, the data that is written in becomes valid at the Q outputs as soon as the tcvw, tdvw, and twvw timing terms are met. The clock does not have to rise, and the W/RN signal does not have to fall first.
2. The data hold time in write cycle 1 is referenced to the rising edge of CLK when W/RN is held high.
3. The data hold time in write cycle 2 is referenced to the falling edge of W/RN and is equal to zero.
4. The data hold time in the Read-Modify-Write cycle has to be met only when W/RN is held high.

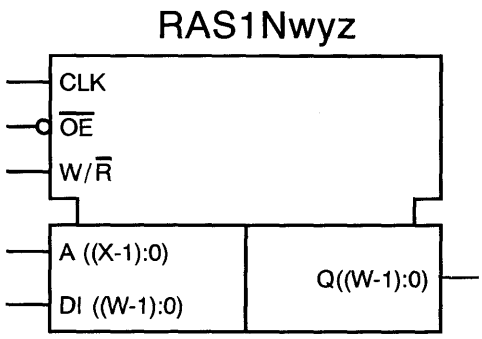
RAS1Nwyz
Mid-Speed Static RAM

CYX 1.0 micron CMOS Standard Cells

Features

- Slightly larger but faster than the version 0 RAM
- 7.15 nsec typical cycle time for a 32 x 4 RAM with a 0.5pF load
- Read-Modify-Write cycle possible
- Low standby power when the clock is stopped
- Separate input and output ports with full parallel access
- 3-State outputs interface internal data buses directly
- Precharged design for faster operation with less silicon area

FIGURE1: LOGIC SYMBOL



Note 1: A0 is the LSB

Note 2: X represents the number of address lines

General Description

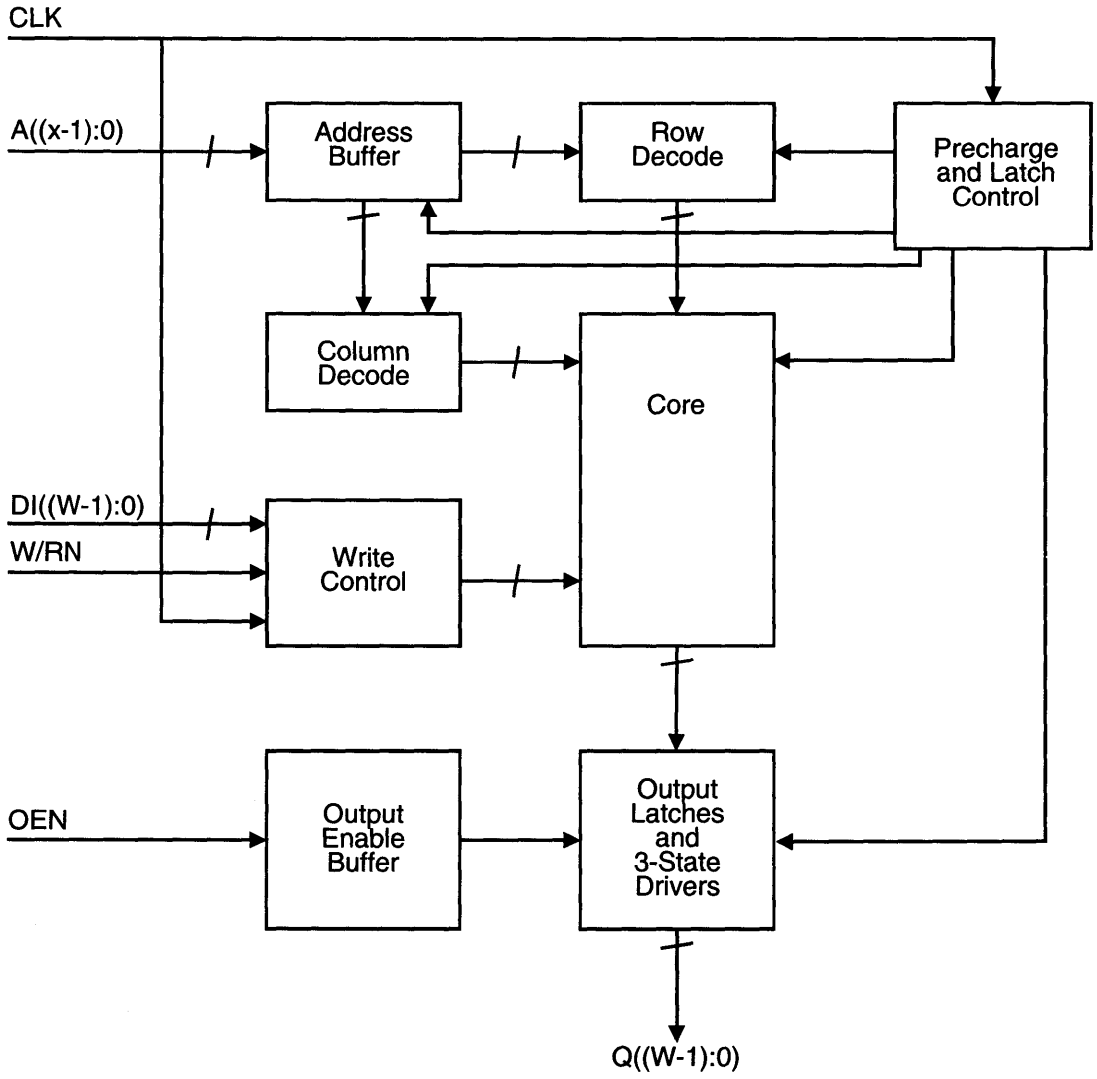
This series of 1.0 micron double-metal MxN RAMs operates within a power supply voltage range of 4.5V to 5.5V, and can operate with reduced performance at supply voltages as low as 2.5V. The RAS1N series is similar to RAS0N except that this version is slightly larger and faster. This series has 3-state outputs with active low Output Enable Not (OEN). The circuit is precharged when the clock is high, and the read and write operations occur when the clock is low. The outputs become valid a short time after the falling edge of the clock and stay valid until the next falling edge of the clock. The address lines are latched on the falling edge of the clock. The clock is used only to precharge the circuit and operate the latches; the memory does not need a refresh signal. The clock and all of the other inputs can be held stable indefinitely with no loss of memory as long as power is supplied to the RAM.

Within limits specified below, the user has flexibility in specifying the logical size of the RAM, including both word size and number of address locations. Within the name shown above, the "wyz" represents a three character sequence assigned to each RAM configuration which uniquely identifies that particular configuration. Furthermore, the "S", "1", and "N" represent a single port RAM, version 1, and an active low output enable respectively. The "w" signifies the word-length in a mod-36 alpha-numeric digit using the integers 1-9 and letters A-Z excluding O, Q, and V. For example, "N" represents a word length of 23 and "P" is a word-length of 24. The "yz" represents a hexadecimal value for the number of address locations divided by 16. For example, "04" represents 64 address locations.

In the logic symbol of figure 1, the "X" denotes the number of address lines. This value can be calculated by taking the log to the base 2 of the number of address locations. If the value returned is not an integer, round up. For example, for 64 address locations, "X" would be 6; for 80 address locations, "X" would be 7.

Performance data is listed below for two example sizes. To obtain data and a workstation installation (symbol and simulation model) for a specific size, contact the factory.

FIGURE 2: M X N RAM BLOCK DIAGRAM



Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Address Inputs	5	10	1(A0 is the LSB)
Word Size (Data Outputs)	1 bit	32 bits	1 bit
Address Locations (Words)	32	1024 (1K)	16
Total bits in a core (Word size times address locations)	32	32,768 (32K)	

Pin Description and Input Capacitance

SIGNAL	TYPE	32 X 4	1K X 16	SIGNAL DESCRIPTIONS
Ai	Input	0.11pF	0.11pF	Address Inputs
CLK	Input	0.28pF	0.52pF	Clock Input
OEN	Input	0.17pF	0.35pF	3-State Output Control
Q (High-Z)	Output	0.11pF	0.11pF	Data Outputs
W/RN	Input	0.06pF	0.06pF	Write/Read Not Control
Di	Input	0.07pF	0.07pF	Data Inputs

Contact the factory to obtain capacitance information about MXN RAM
Area relative to a 2 Input Nand
32 x 4: 434
1K x 16: 12852

Bolt Syntax

Q00 Q01 . . . Qw, .RAS1Nwyz A0 A1 . . . Ax CLK DI00 DI01 . . . DIw OEN WRN;

Note: A0 is the LSB

AC Characteristics: t(CL)=tdx + Ktdx * CL

The data in the following examples are specified at 5.OV, Tj = 25°C, and typical process performance parameters. Performance at other operating points may be estimated by use of the Voltage, Process, and Temperature derating curves. Contact the factory to obtain the AC characteristics and input capacitance for different logical sizes of RAMs.

RAS1Nwyz
Mid-Speed Static RAM

AMI SEMICONDUCTORS

CYX 1.0 micron CMOS Standard Cells

32 x 4

CHARACTERISTIC	SYMBOL	tdx (ns)	ktdx (ns/pF)	t(0.5pF) (ns)
Min CLK Period Read	tclkr	6.79	0.72	7.15
Min CLK Period Write	tclkw	5.42		
Min CLK Width High	twch	2.33		
Min CLK Width Low During Read	twclr	4.45		
Max CLK Low to Q Delay	tpcq	4.45	0.72	4.81
Max OEN to Q Delay	toenq	0.71	0.72	1.07
Max OEN to High-Z Delay	toenz	0.54		
Min Address Setup Time**	tasu	1.26		
Min Address Hold Time**	tah	0.85		
Min W/RN High to Valid Write*	twvw	1.96		
Min Data in (Di) Stable to Valid Write*	tdvw	2.08		
Min CLK Low to Valid Write*	tcvw	3.08		
Min Data in (Di) Hold Time after Rising edge of CLK when W/RN is High*	tdh	0.96		
Min W/RN Hold Time After Read	twh	0.25		
Min Q Hold Time	tqh	0.83		

* If the W/RN line is high at the same time that CLK is low, all three timing terms twvw, tdvw, and tcvw must be met or else invalid data may be written into the RAM. A Read-Modify-Write cycle may be executed by leaving W/RN low until the Read is accomplished, then meeting the twvw, tdvw, and tcvw timing terms to accomplish a valid Write. The Q outputs will change to the value that is written. After a Write, the Data In (Di) pins must be held stable until after W/RN falls or CLK rises.

** If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it will not show corrupted data.

1K x 16

CHARACTERISTIC	SYMBOL	tdx (ns)	ktdx (ns/pF)	t(0.5pF) (ns)
Min CLK Period Read	tclkr	13.12	0.81	13.52
Min CLK Period Write	tclkw	10.82		
Min CLK Width High	twch	4.94		
Min CLK Width Low During Read	twclr	8.18		
Max CLK Low to Q Delay	tpcq	8.18	0.81	8.58
Max OEN to Q Delay	toenq	0.84	0.81	1.24
Max OEN to High-Z Delay	toenz	0.65		
Min Address Setup Time**	tasu	1.63		
Min Address Hold Time**	tah	1.09		
Min W/RN High to Valid Write*	twvw	4.43		
Min Data in (Di) Stable to Valid Write*	tdvw	4.32		
Min CLK Low to Valid Write*	tcvw	5.87		
Min Data in (Di) Hold Time after Rising edge of CLK when W/RN is High*	tdh	1.41		
Min W/RN Hold Time After Read	twh	0.25		
Min Q Hold Time	tqh	0.96		

* If the W/RN line is high at the same time that CLK is low, all three timing terms twvw, tdvw, and tcvw must be met or else invalid data may be written into the RAM. A Read-Modify-Write cycle may be executed by leaving W/RN low until the Read is accomplished, then meeting the twvw, tdvw, and tcvw timing terms to accomplish a valid Write. The Q outputs will change to the value that is written. After a Write, the Data In (Di) pins must be held stable until after W/RN falls or CLK rises.

** If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it will not show corrupted data.

Power Dissipation

PARAMETER	32 X 4	1K X 16
Typical C_{pd} (Equivalent Power Dissipation Capacitance (pF))	21	178
Typical Static IDD Tj=85°C (μa)	1.35	10

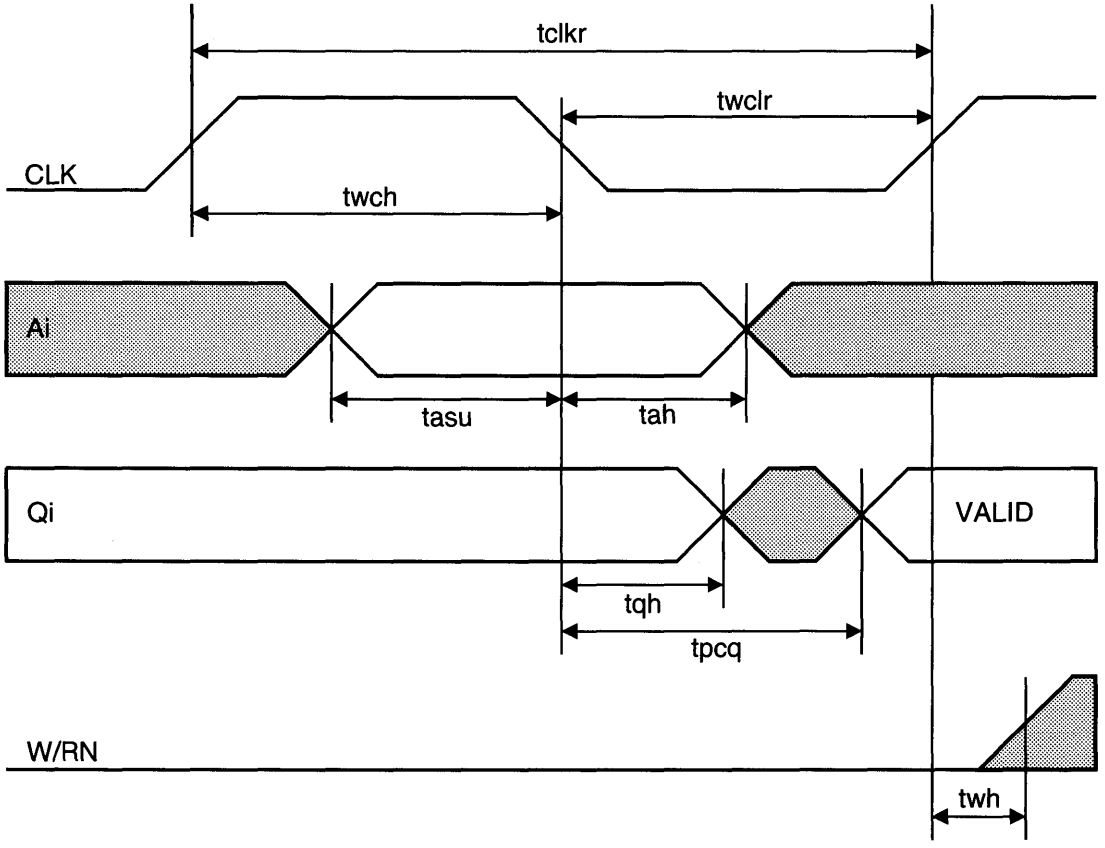
(See data book for power dissipation notes.)

Testing Notes:

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. The minimum pattern used to test a RAM should write and read both a zero and a one to every core bit. In addition, a variable pattern used to test for address decode faults and write disturb problems by writing the entire memory then reading it all back. One example of a variable pattern for these tests is to write the address value to each location. There are many methodologies for testing RAMs that have test time versus fault coverage trade-offs. For more information on testing RAMs, refer to the AMI application note titled "Testing RAM Elements In IC Designs."

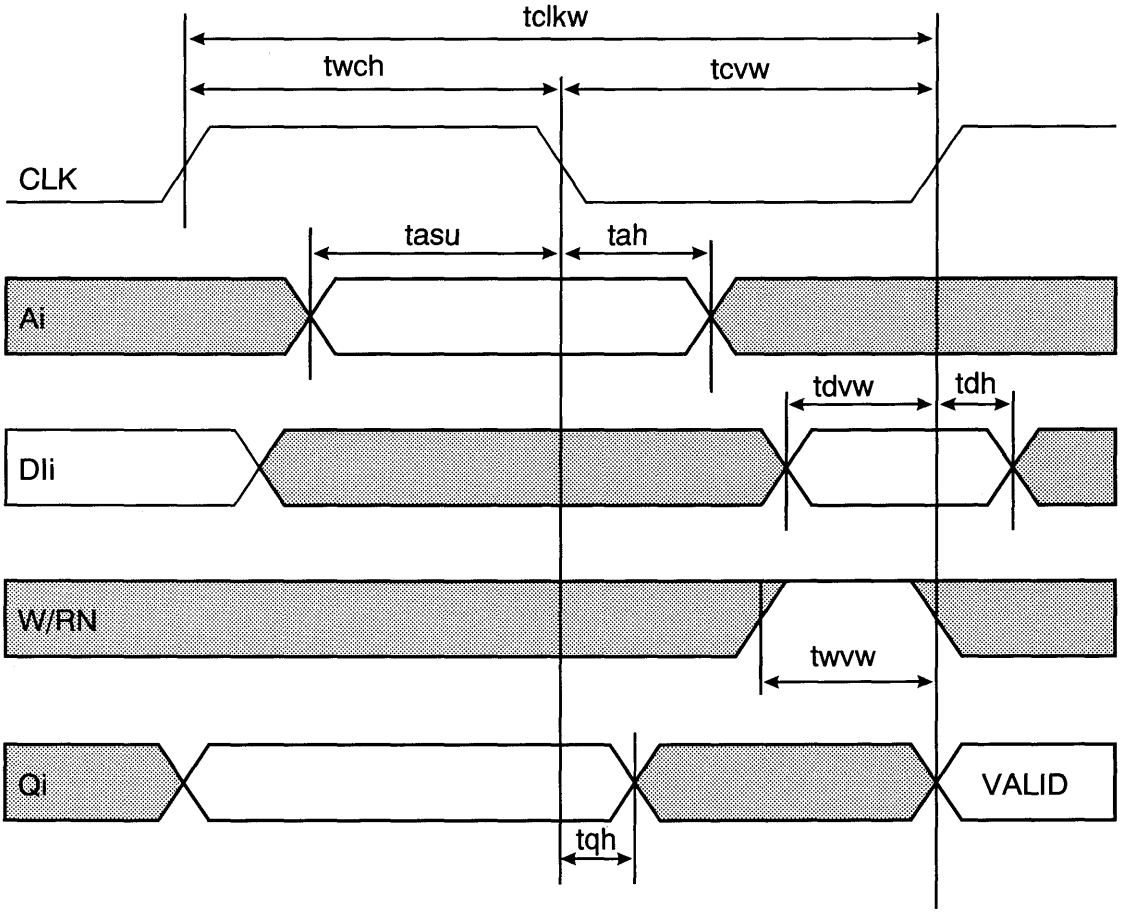
M X N RAM
Timing Diagram

Read Cycle



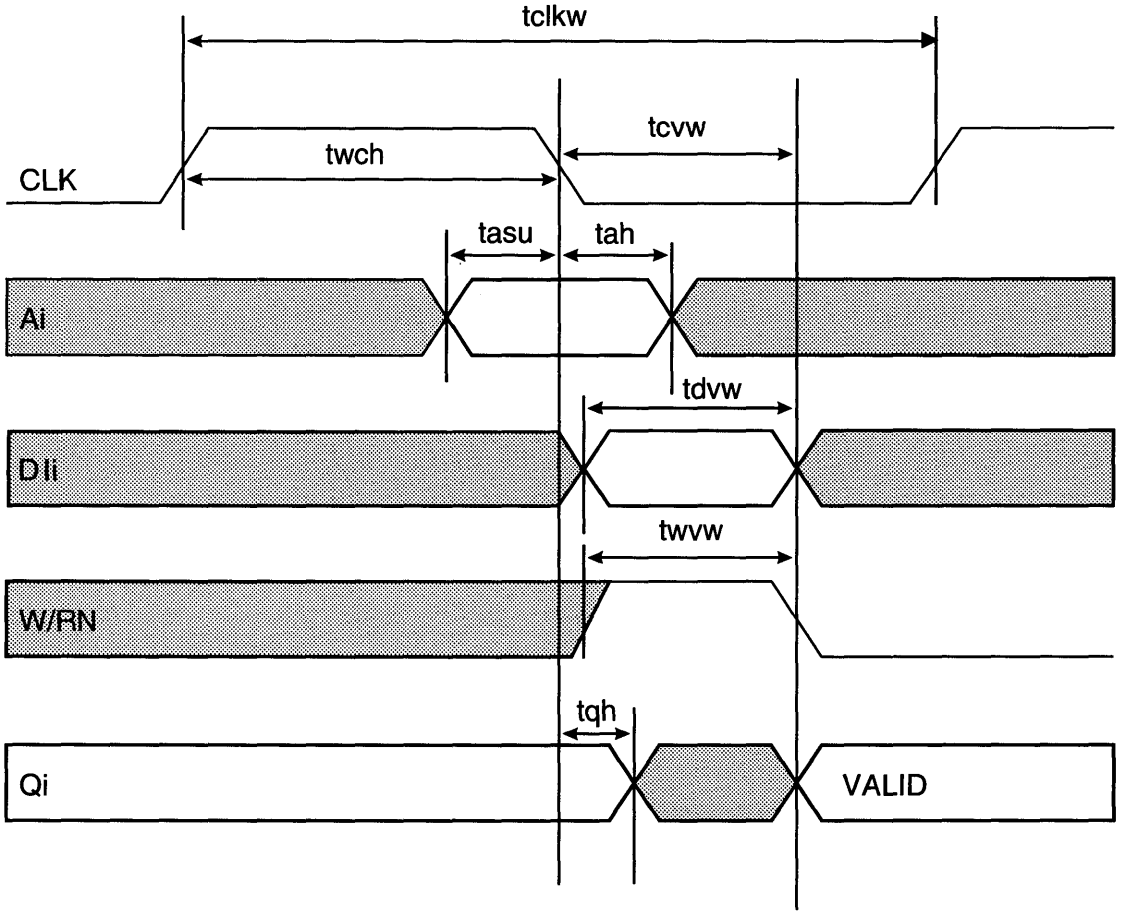
M X N RAM
Timing Diagram

Write Cycle 1 (See Notes 1 and 2)



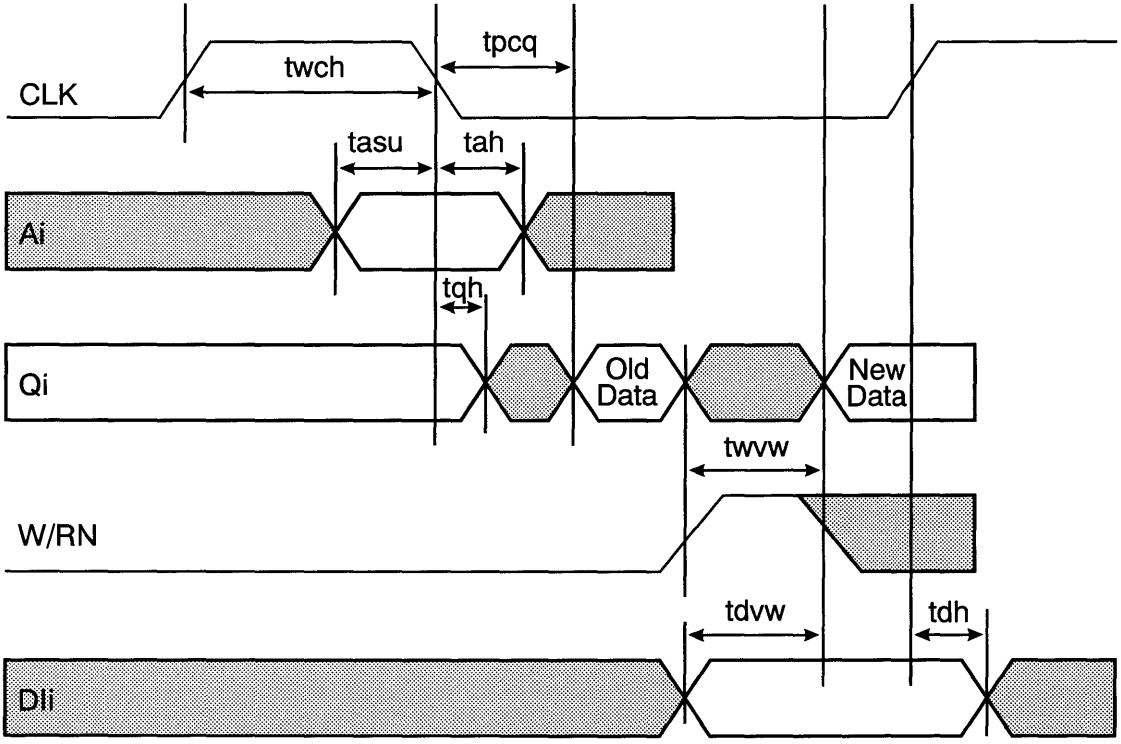
M X N RAM
Timing Diagram

Write Cycle 2 (See Notes 1 and 3)

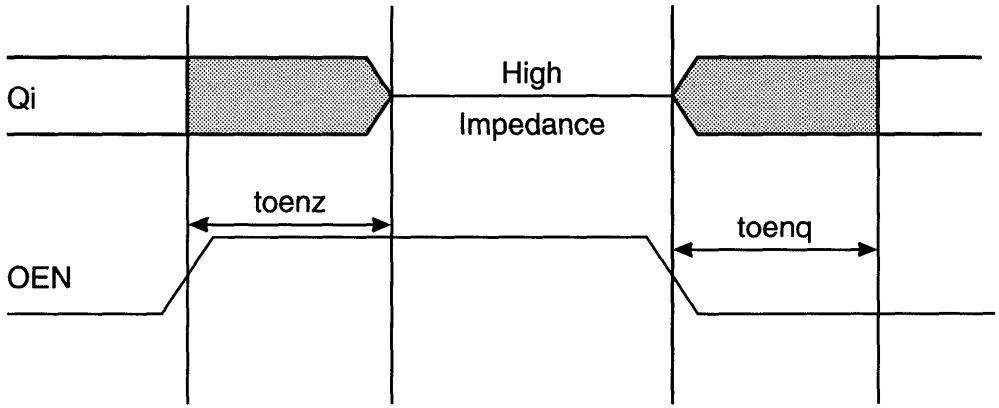


M X N RAM
Timing Diagram

Read-Modify-Write Cycle (See Note 4)



3-State Control Timing



Timing Diagram Notes

1. During a write cycle, the data that is written in becomes valid at the Q outputs as soon as the tcvw, tdvw, and twvw timing terms are met. The clock does not have to rise, and the W/RN signal does not have to fall first. In write cycle 1, the rising edge of CLK ends the write cycle. In write cycle 2, the falling edge of W/RN ends the write cycle. This is the only difference between write cycle 1 and write cycle 2.
2. The data hold time in write cycle 1 is referenced to the rising edge of CLK when W/RN is held high.
3. The data hold time in write cycle 2 is referenced to the falling edge of W/RN and is equal to zero.
4. The data hold time in the Read-Modify-Write cycle has to be met only when W/RN is held high.

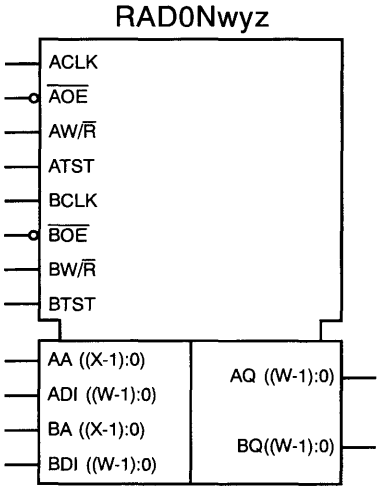
RADONwyz
Dual Port Static RAM

CYX 1.0 micron CMOS Standard Cells

Features

- Two independent ports access the same core array.
- 9.11 nsec typical cycle time for a 32 x 4 RAM with a 0.5pF load
- Read-Modify-Write cycle possible
- Low standby power when the clocks are stopped
- Separate input and output ports with full parallel access
- 3-State outputs interface internal data buses directly
- Precharged design for faster operation with less silicon area

FIGURE 1: LOGIC SYMBOL



Note 1: AA00 is the LSB
Note 2: X represents the number of address lines

General Description

This series of 1.0μ double-metal MxN RAMs operates within a power supply voltage range of 4.5V to 5.5V. The RADON series has 3-state outputs with active low Output Enable Not (OEN). When either clock is high, the corresponding port circuitry is precharged. Read and write operations occur when the corresponding clock is low. Port outputs become valid a short time after the falling edge of the related clock and stay valid until the next falling edge of the related clock. The address lines are latched on the falling edges of the clocks. The clocks are used only to precharge the circuitry and operate the latches; the memory does not need a refresh signal. The clocks and all of the other inputs can be held stable indefinitely with no loss of memory as long as power is supplied to the RAM.

The dual port RAM consists of two ports, each port having its own CLK, Address, Data, Output, Output enable, and Write/Read control lines. This enables the RAM to have four basic operations: Write A, Read A, Write B, and Read B. Each of these operations can be performed independently of the others. There is no internal address arbitration.

Write A, Write B: If both ports are writing the same address, then unknown data will be written to that address.

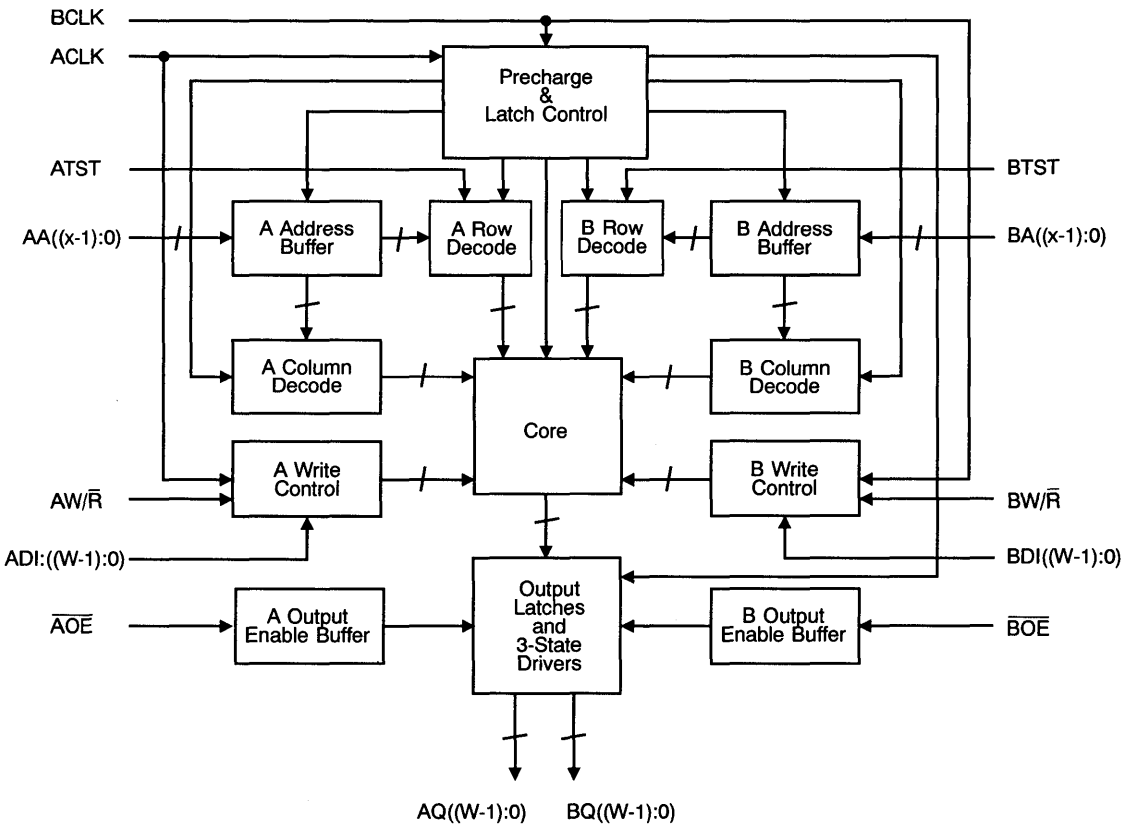
Read A, Read B: Ports A and B may read data from different addresses, or both ports may read simultaneously from the same address.

Write A, Read B, or Write B, Read A: If each port is accessing a different address, then uncorrupted data will be read/written for both operations. If each port is accessing the same address, then the data that is read will be equal to that currently being written if sufficient time has elapsed for a valid write to propagate to the read port. The read will reflect the previous contents of the accessed address if the new data has not yet been written. For further information consult the timing diagrams.

Within limits specified below, the user has flexibility in specifying the logical size of the RAM, including both word size and the number of address locations. Within the name as shown above, the "wyz" represents a three character sequence assigned to each RAM configuration which uniquely identifies that particular configuration. Furthermore, the "D", "0", and "N" represent a dual port RAM, version 0, and an active low output enable, respectively. The "W" represents a mod-36 alpha-numeric digit using the integers 1-9 and letters A-Z excluding O, Q, and V. For example, "N" represents a word length of 23 and "P" represents a word length of 24. The "yz" represents a hexadecimal value for the number of address locations divided by 16. For example, "04" represents 64 address locations.

In the logic symbol of Figure 1, the "X" denotes the number of address lines. This value can be calculated by taking the log to the base 2 of the number of address locations. If the value returned is not an integer, round up. For example, for 64 address locations, "X" would be 6; for 80 address locations, "X" would be 7.

FIGURE 2: M X N DUAL PORT STATIC RAM BLOCK DIAGRAM



Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Address Inputs	5	10	1(AA00 is the LSB)
Word Size (Data Outputs)	1 bit	32 bits	1 bit
Address Locations (Words)	32	1024 (1K)	16
Total bits in a core (Word size times address locations)	32	32,768 (32K)	

Pin Description and Input Capacitance

SIGNAL	TYPE	32 X 4	1K X 16	SIGNAL DESCRIPTIONS
AAi,BAi	Input	0.08pF	0.08pF	Address Inputs
ACLK, BCLK	Input	0.21pF	0.38pF	Clock Input
AOEN, BOEN	Input	0.12pF	0.26pF	3-State Output Control
AQ, BQ (High-Z)	Output	0.16pF	0.16pF	Data Outputs
AW/RN, BW/RN	Input	0.07pF	0.07pF	Write/Read Not Control
ADi, BDi	Input	0.10pF	0.10pF	Data Inputs

Contact the factory to obtain capacitance information about MXN RAM
Area relative to a 2 Input Nand
32 x 4: 901
1k x 16: 28384

Performance data is listed below for two example sizes. To obtain data and a workstation installation (symbol and simulation model) for a specific size, contact the factory.

Bolt Syntax

AQ00 AQ01....AQ(W-1) BQ00 BQ01....BQ(W-1), .RAD0Nwyz AA00 AA01....AA0(X-1) ACLK ADI00 ADI01....ADI(W-1) AOEN ATST AWRN BA00 BA01....BA0(X-1) BCLK BDI00 BDI01 BDI(W-1) BOEN BTST BWRN;

Note: AA00 and BA00 are the LSBs for their respective ports.

AC Characteristics: t(CL)=tdx + Ktdx * CL

The data in the following examples are specified at 5.0V, Tj=25°C, and typical process performance parameters. Performance at other operating points may be estimated by use of the Voltage, Process, and Temperature derating curves. Contact the factory to obtain the AC characteristics and input capacitance for different logical size RAMs.

CYX 1.0 micron CMOS Standard Cells

32 x 4

CHARACTERISTIC	SYMBOL	tdx (ns)	ktdx (ns/pF)	t(0.5pF) (ns)
Min CLK Period Read	tclkr	8.67	0.88	9.11
Min CLK Period Write	tclkw	6.72		
Min CLK Width High	twch	2.91		
Min CLK Width Low During Read	twclr	5.75		
Max CLK Low to Q Delay	tpcq	5.75	0.88	6.19
Max OEN to Q Delay	toenq	0.80	0.88	1.24
Max OEN to High-Z Delay	toenz	0.57		
Min Address Setup Time**	tasu	1.30		
Min Address Hold Time**	tah	0.91		
Min W/RN High to Valid Write*	twvw	4.07		
Min Data in (Di) Stable to Valid Write*	tdvw	4.22		
Min CLK Low to Valid Write*	tcvw	3.81		
Min Data in (Di) Hold Time after Rising edge of CLK when W/RN is High*	tdh	0.99		
Min W/RN Hold Time After Read	twh	0.29		
Min Q Hold Time	tqh	0.89		
Min Test Setup Time***	ttsu	1.30		
Min Test Hold Time***	tth	0.91		

* If the W/RN line is high at the same time that the CLK line is low, all three timing terms twvw, tdvw, and tcvw must be met or else invalid data may be written into the RAM. A Read-Modify-Write cycle may be executed by leaving W/RN low until the read is accomplished, then meeting the twvw, tdvw, and tcvw timing terms to accomplish a valid write. The Q outputs will change to the value that is written. After a write, the Data In (Di) pins must be held stable until after W/RN falls or CLK rises.

** If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during the read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it will not show corrupted data.

***ttsu = tasu and tth = tah.

1K x 16

CHARACTERISTIC	SYMBOL	tdx (ns)	ktdx (ns/pF)	t(0.5pF) (ns)
Min CLK Period Read	tclkr	18.80	0.96	19.28
Min CLK Period Write	tclkw	14.94		
Min CLK Width High	twch	7.53		
Min CLK Width Low During Read	twclr	11.28		
Max CLK Low to Q Delay	tpcq	11.28	0.96	11.76
Max OEN to Q Delay	toenq	0.94	0.96	1.42
Max OEN to High-Z Delay	toenz	0.69		
Min Address Setup Time**	tasu	1.67		
Min Address Hold Time**	tah	1.14		
Min W/RN High to Valid Write*	twvw	10.0		
Min Data in (Di) Stable to Valid Write*	tdvw	9.65		
Min CLK Low to Valid Write*	tcvw	7.41		
Min Data in (Di) Hold Time after Rising edge of CLK when W/RN is High*	tdh	1.61		
Min W/RN Hold Time After Read	twh	0.28		
Min Q Hold Time	tqh	1.01		
Min Test Setup Time***	ttsu	1.67		
Min Test Hold Time***	tth	1.14		

* If the W/RN line is high at the same time that the CLK line is low, all three timing terms twvw, tdvw, and tcvw must be met or else invalid data may be written into the RAM. A Read-Modify-Write cycle may be executed by leaving W/RN low until the read is accomplished, then meeting the twvw, tdvw, and tcvw timing terms to accomplish a valid write. The Q outputs will change to the value that is written. After a write, the Data In (Di) pins must be held stable until after W/RN falls or CLK rises.

** If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during the read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it will not show corrupted data.

***ttsu = tasu and tth = tah.

CYX 1.0 micron CMOS Standard Cells

Power Dissipation:

PARAMETER	32 x 4	1K x 16
Typical Cpd (Equivalent Power Dissipation Capacitance (pF))	77	354
Typical Static IDD Tj=85°C (μa)	3	20

Testing Notes:

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. For a more detailed description of the testing of memory elements in ICs, refer to the RAM testing application notes.

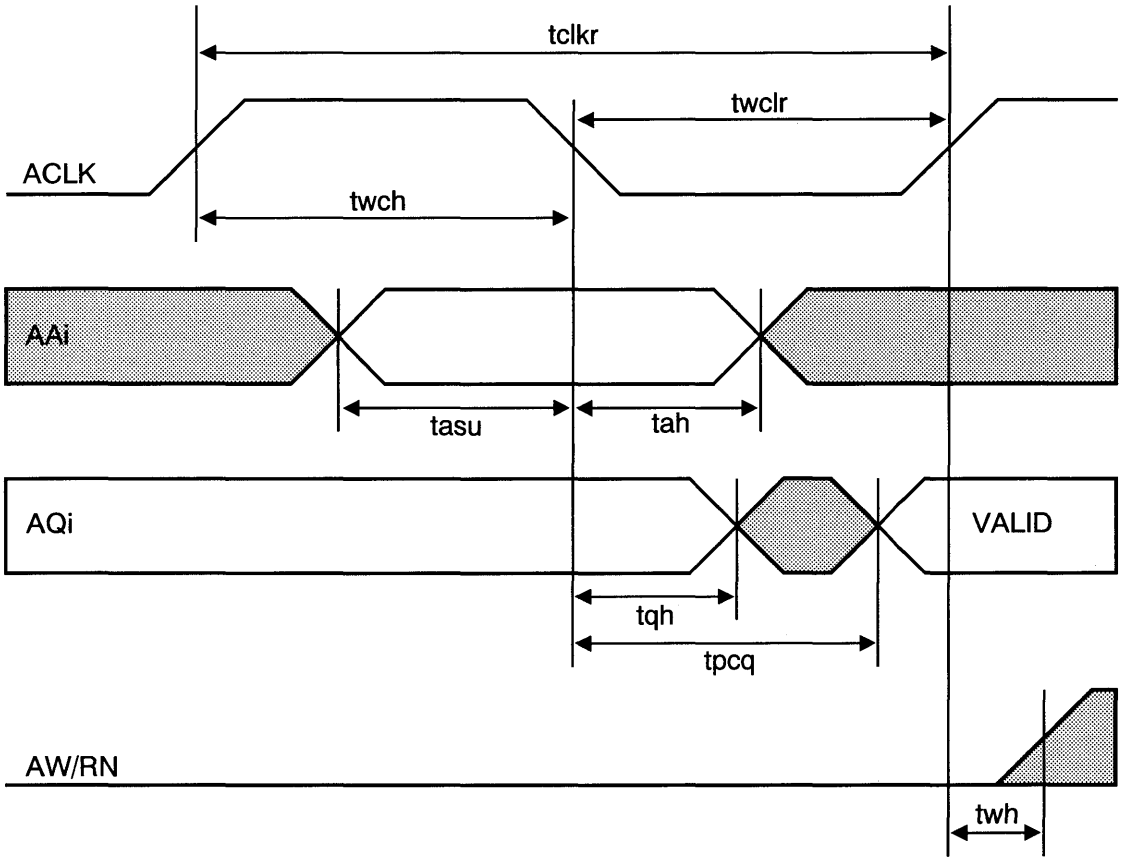
Shadow Write Test Mode

The shadow write feature (ATST and BTST) was incorporated in the design to detect short circuits that may exist between adjacent A and B port BIT lines. As such, the ATST and BTST circuits were only designed to be used in the test mode.

To test for shorts between adjacent BIT lines, the core cells must be initialized to some known value (0 or 1). The shadow write mode operates by selecting a common address to be placed on both A and B ports, then either ATST or BTST is pulled high (1), thus disabling the row select lines associated with that port. A read operation is then performed by the port whose row select line is not disabled, simultaneous with a write operation that is performed by the other port. A short is detected if the read produces corrupted data. In order to test for all possible shorts that could occur between adjacent BIT lines, both a 0 and a 1 must be written to the address under test (keeping the core value constant).

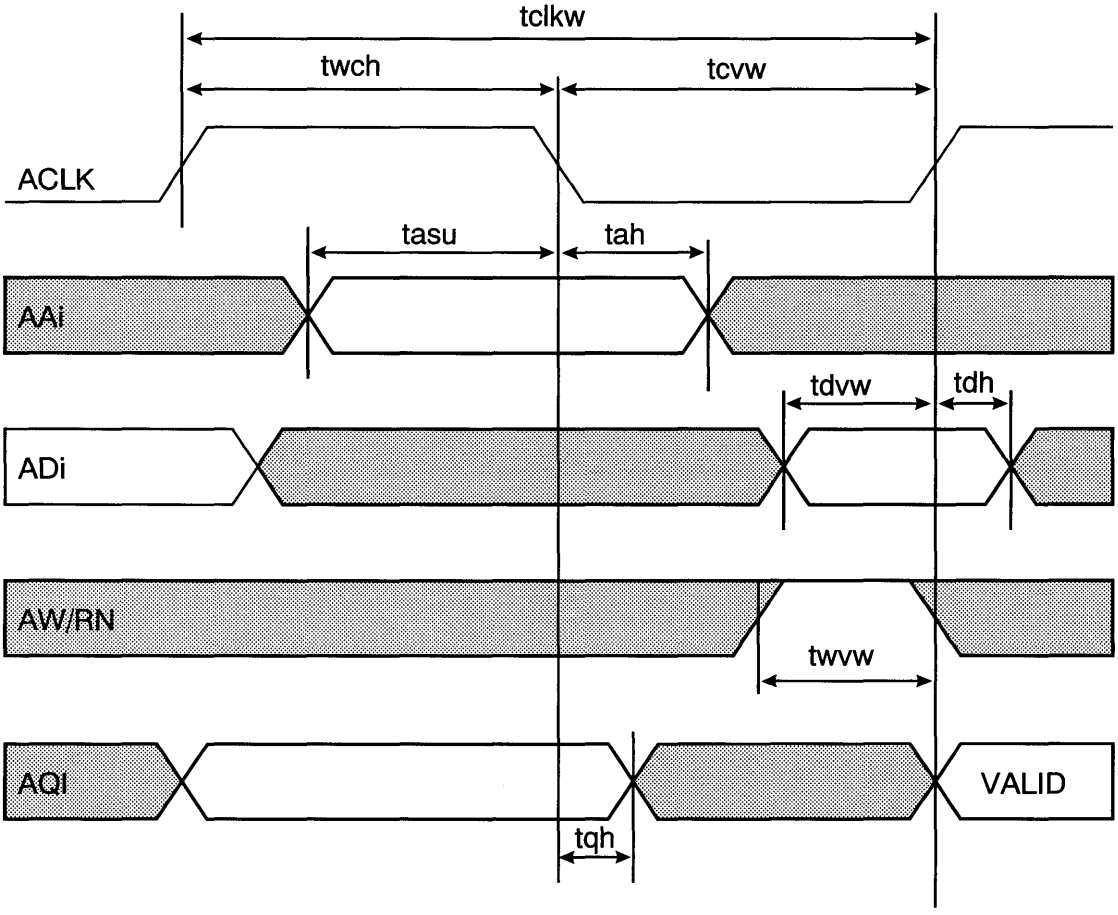
M X N RAM
Timing Diagram

Read Cycle (see Notes 5 and 6)



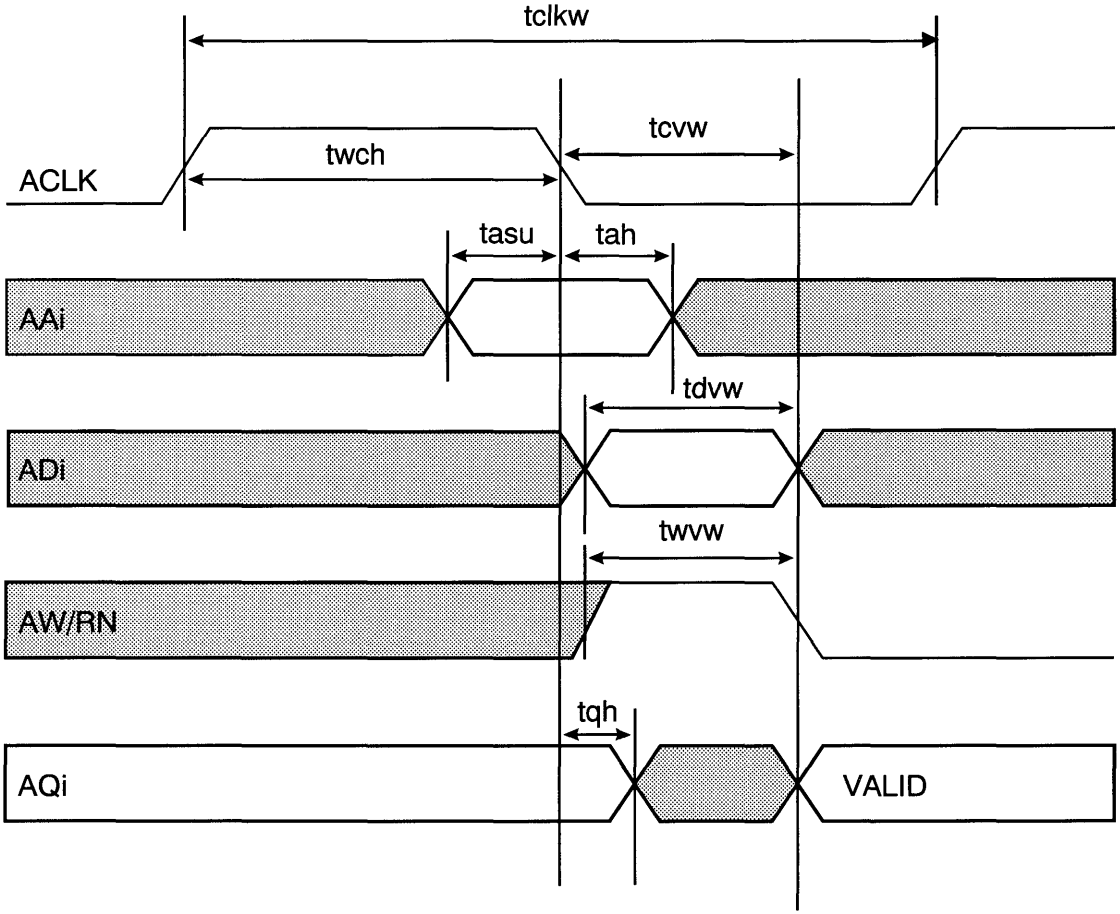
M X N RAM
Timing Diagram

Write Cycle 1 (See Notes 1, 2, 5 and 6)



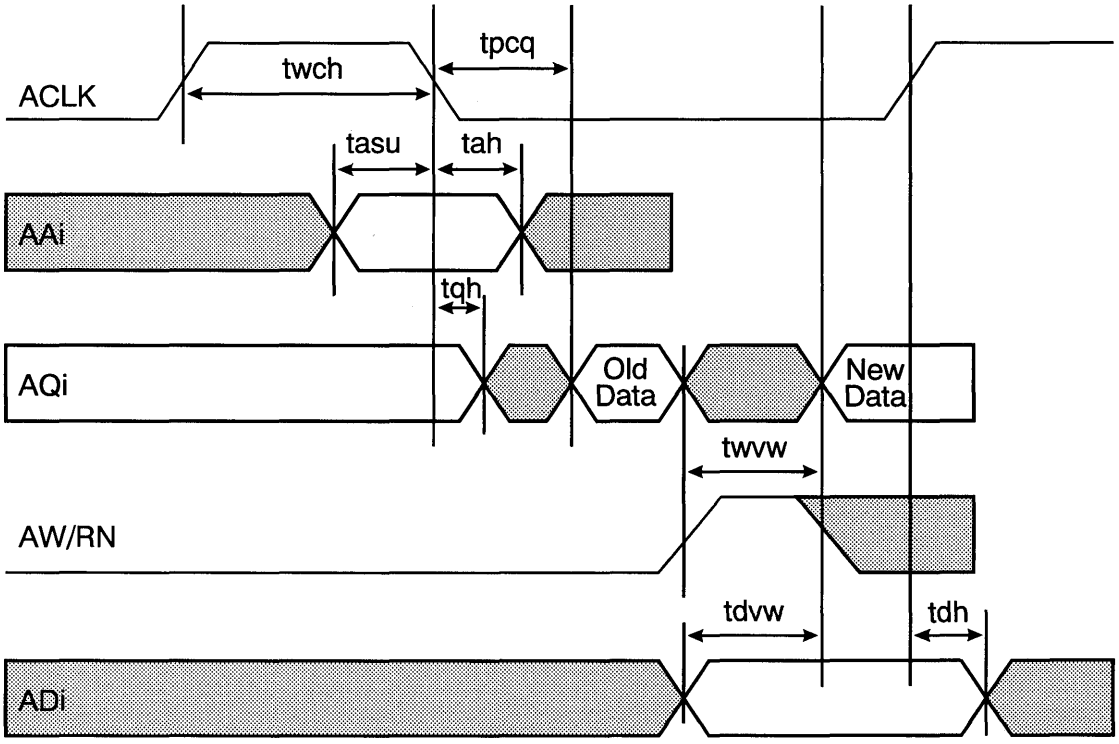
M X N RAM
Timing Diagram

Write Cycle 2 (See Notes 1, 3, 5 and 6)



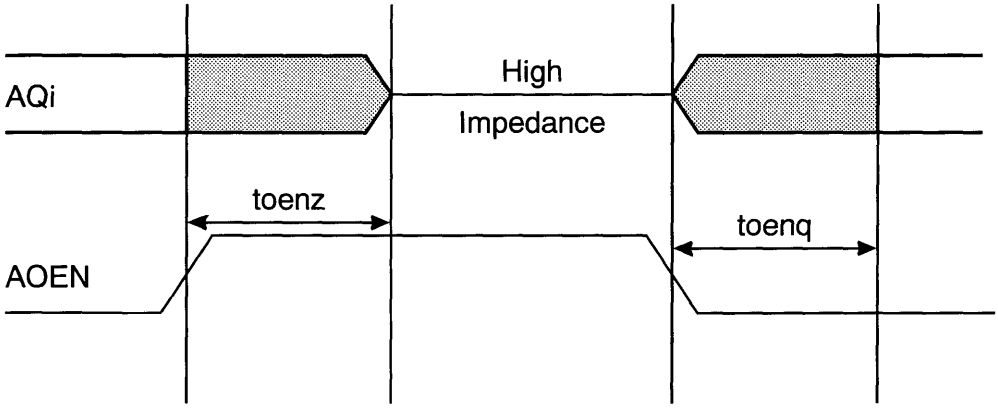
M X N RAM
Timing Diagram

Read-Modify-Write Cycle (See Notes 4, 5 and 6)



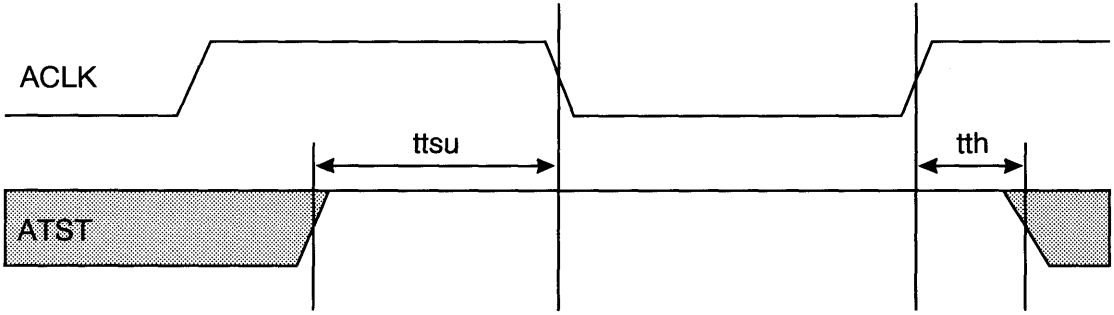
3-State Control Timing

(See Notes 5 and 6)



M X N RAM
Timing Diagram

Test Mode (See Notes 5, 6 and 7)



TIMING DIAGRAM NOTES

1. During a write cycle, the data that is written becomes valid at the outputs as soon as the tcvw, tdvw, and twvw timing terms are met. The clock does not have to rise, and the AW/RN signal does not have to fall first.
2. The data hold time in write cycle 1 is referenced to the rising edge of ACLK when AW/RN is held high.
3. The data hold time in write cycle 2 is referenced to the falling edge of AW/RN and is equal to zero.
4. The data hold time in the Read-Modify-Write cycle has to be met only when AW/RN is held high.
5. Note that only the "A" port signals are shown on the timing diagrams. The "B" port functions in a similar manner.
6. ATST and BTST are equal to zero unless they are in the test mode.
7. During the test mode the signal timing for read and write operations is identical to that shown on their respective timing diagrams.

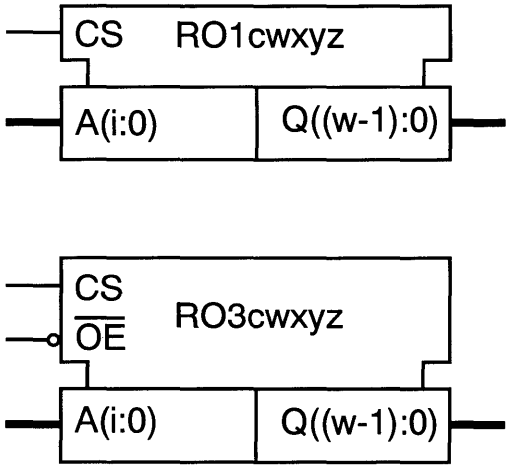
RO1cwxyz ROM
RO3cwxyz ROM

CYX 1.0 micron CMOS Standard Cells

Features

- Low standby power when chip select is stopped.
- Buffered or 3-state outputs. 3-state outputs are active low enable
- Pre-charged design for faster operation with less silicon area

FIGURE 1: LOGIC SYMBOL



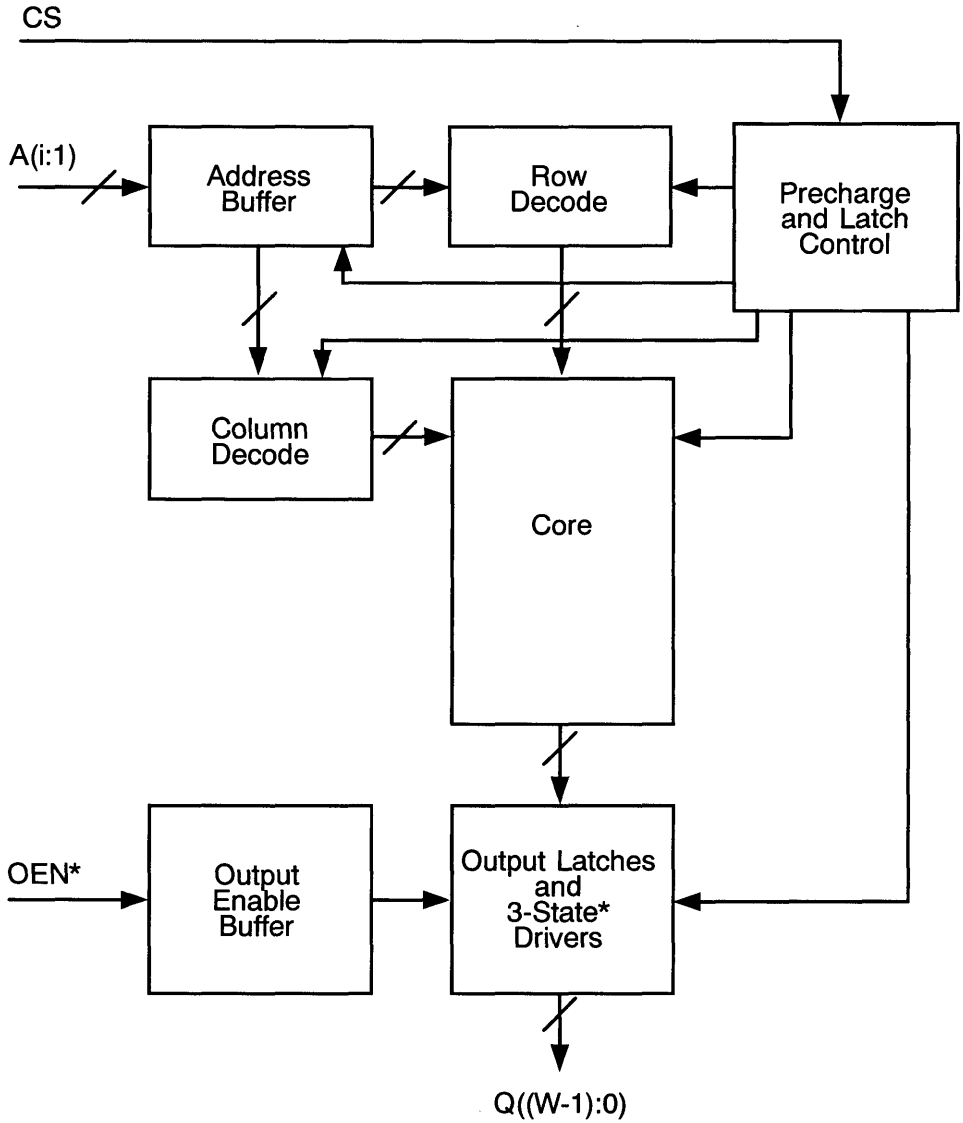
General Description

This series of 1.0 micron double-metal MxN ROMs operates within a power supply voltage range of 4.5V to 5.5V (will operate at 2.5V with lower performance). The RO1 series has always active outputs. The RO3 series has 3-state outputs with active low Output Enable Not (OEN). The circuit is precharged when the chip select (CS) line is low, and the read operation occurs when the chip select (CS) is high. The outputs become valid a short time after the rising edge of the chip select and are latched on the falling edge of the chip select keeping the outputs valid until the next rising edge of the chip select. The address lines are latched on the rising edge of chip select.

Within limits specified below, the user has flexibility in specifying the logical size of the ROM, including both word size and number of address locations. Within the name as shown above, the "cwxyz" represents a five character sequence assigned to each ROM configuration which uniquely identifies that particular configuration. The "c" represents the number column address lines, which is limited to 3, 4, or 5. The "w" represents a mod-36 alpha-numeric digit using the integers 1-9 and the letters A-Z excluding O, Q, and V. For example, "N" represents a word-length of 23 and "P" represents a word-length of 24. The "xyz" represents a hexadecimal value for the number of address locations divided by 16. For example, "00C" represents 192 address locations. The columns are represented because the ROM can be built using different aspect ratios i.e., rows vs. columns.

Performance data is listed below for an example size. To obtain data and a workstation installation (symbol and simulation model) for a particular size, contact the factory.

FIGURE 2: ROM BLOCK DIAGRAM



*For RO1 series, OEN input is removed and output driver is never High-Z
*For RO3 series, as shown

Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Address Inputs	6	14	1
Word Size(Data outputs)	1	32	1
Address locations	64	16,384(16K)	64
Total bits in core (Word size times address locations)	64	524,288(512K)	

Pin Description and Input Capacitance

SIGNAL	TYPE	256K X 16	SIGNAL DESCRIPTIONS
Ai	Input	0.03 pF	Address inputs
CS	Input	0.41 pF	Chip Select
OEN	Input	0.20 pF	3-State Output Control
Q(High-Z)	Output	0.11 pF	Data Outputs

Contact factory to obtain input capacitance values for MXN ROM
Area Relative to a 2 Input Nand: 256 x 16 : 827

Bolt Syntax:

RO1cwxyz:Q00 Q01...RO1cwxyz A00 A01...CS;
RO3cwxyz:Q00 Q01...RO3cwxyz A00 A01...CS OEN;
NOTE: A0 is the LSB

AC Characteristics:t(CL)=tdx+Ktdx*CL

The data in the following examples is specified at 5.0V, Tj=25°C, and typical process parameters. Performance at other operating points may be estimated by use of the Voltage, Process, and Temperature derating curves. Contact the factory to obtain the AC characteristics and input capacitance for different logical sizes of ROMs.

256 X 16

CHARACTERISTIC	SYMBOL	tdx(ns)	ktdx(ns/pF)	t(0.5pF)(ns)
Max CS to Q Delay	tpcsq	5.29	1.08	5.83
Max OEN to Q Delay	tpoenq	0.91	1.08	1.45
Max OEN to High-Z Delay	tpoenz	1.36		
Min Address Setup time	tasu	1.74		
Min Address hold time	tah	0.0		
Min CS Width Low	twcsl	3.23		
Min CS Width High	twcsh	5.29		
Min Q Hold Time	tqh	1.32		

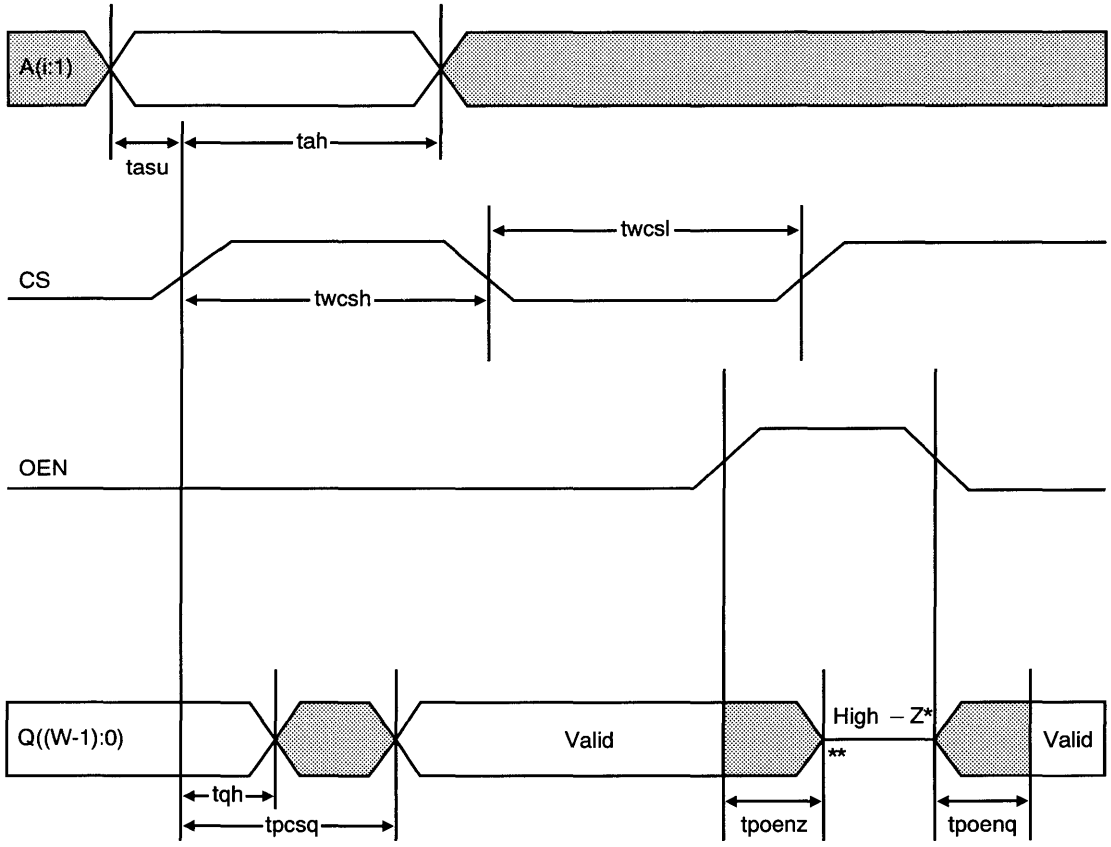
Power Dissipation:

PARAMETER	256 X 16
Typical Cpd (Equivalent Power Dissipation Capacitance (pF))	55.0
Typical Static IDD Tj=85°C(μA)	0.7

Testing Notes

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. For a more detailed description of the testing of memory elements in ICs refer to the ROM testing application notes.

M X N ROM
Timing Diagram



*High-Z=High Impedance Q Output

**For RO1 series, OEN is not applicable and the Q((W-1):0) is never High-Z.
For RO3 series, as shown.

Using Synchronous RAMs in ASIC Designs

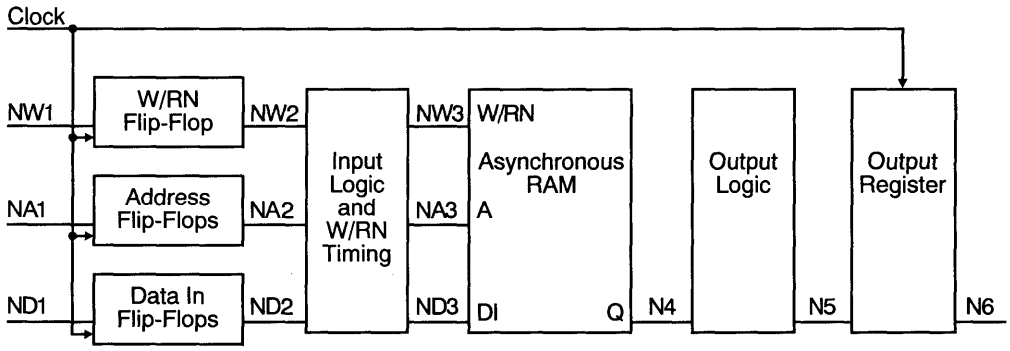
ASIC RAM Application Note

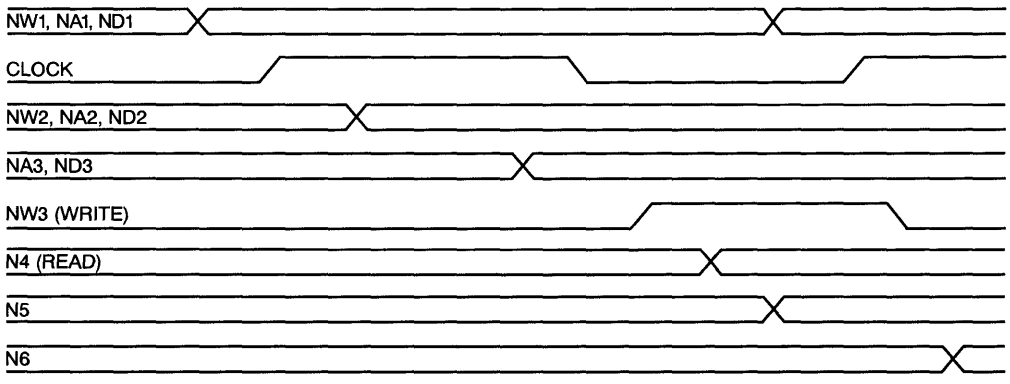
The purpose of this application note is to show how synchronous RAMs can easily be used in synchronous application specific integrated circuit (ASIC) designs. Asynchronous RAMs are often used in ASIC designs, even when the ASIC is synchronous, because the designer is more familiar with asynchronous RAMs or they are more readily available. In synchronous ASICs, it may be advantageous to use synchronous RAMs. Depending on the RAM design, synchronous RAMs can be smaller, faster, more robust, or consume less power than asynchronous RAMs. In many applications, the timing of the Write Enable (W/RN) signal is easier to meet in a synchronous RAM because W/RN can be held in a register that uses the same clock as the address register. This eliminates the considerations about W/RN setup and hold time specifications required by asynchronous RAMs.

The method for incorporating a synchronous RAM into an ASIC design will depend on the circuit configuration surrounding the RAM and the clock speed. This application note gives some general examples of how AMI's synchronous RAMs can replace asynchronous RAMs in ASIC designs. The following examples will assume the three-state output enable is always active. All flip-flops shown are positive-edge triggered and the D-latches have active low gate transparency.

Figure 1 gives an example of how an asynchronous RAM might be used in an ASIC. The Input Logic, Output Logic, and Output Register are optional blocks. The timing diagram in figure 1 gives the relative timing transitions for the signals as they propagate through the circuit. Assuming all the timing specifications can be met, AMI's RAS0Nwyz synchronous RAM will directly replace the asynchronous RAM by making the additional connection of the clock line to the CLK input of the RAS0Nwyz RAM.

Figure 1: Asynchronous RAM Example A





ASIC RAM Application Note

Figure 2 shows an optional way that AMI's RAS0Nwyx synchronous RAM can be substituted into the circuit of figure 1. The RAS0Nwyz RAM READs or WRITEs when the clock is low and precharges when the clock is high. The address inputs are latched in the RAM on the falling edge of the clock. This allows the address register flip-flops in figure 1 to be replaced by the smaller D-latch register in figure 2, unless the input logic timing needs flip-flops. The Write Enable (W/RN) and Data Inputs are not latched in the RAM, so they must be held stable externally.

A comparison of the timing diagrams in figures 1 and 2 reveals that the input signals (NW1, NA1, and ND1) and the output signals (N6) of the circuit have the same timing in both figures. Small timing changes internal to the circuit include the following: 1) the NA2 signals transition sooner in figure 2 because transparent latches were used to latch NA1 instead of flip-flops; 2) the NW2 signal can be connected directly to the synchronous RAM because it does not require an address setup time before Write Enable; and 3) the timing of the RAM outputs (N4) will depend on the falling edge of the clock and the RAM access time.

Figure 2: Synchronous RAM Example A

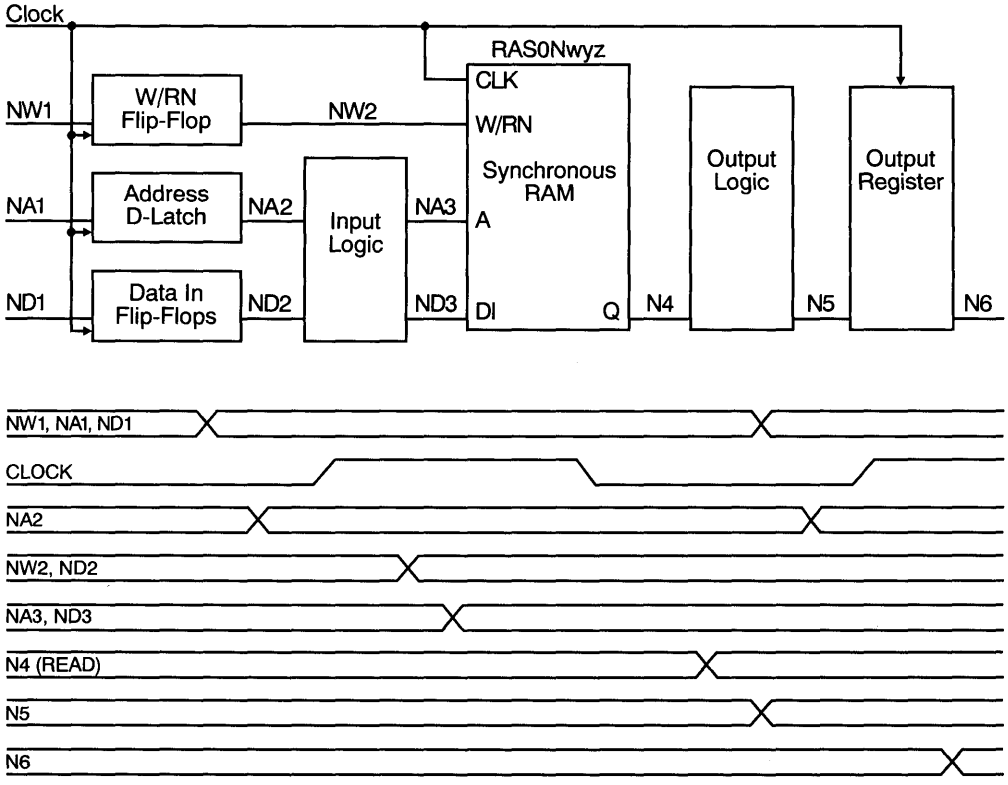


Figure 3 shows a high-speed pipelined design with a flip-flop register, an asynchronous RAM, and some output logic creating one stage of the pipeline. In this case, AMI's RAS3Nwyz RAM would work better than the RAS0Nwyz series because it READs or WRITEs when the clock is high and has a faster access time. Figure 4 shows the circuit of figure 3 with the RAS3Nwyz RAM inserted. The address inputs are latched in the RAM on the rising edge of the clock, so the address register flip-flops can be eliminated. The W/RN and Data inputs must be held stable only while the clock is high, so D-latches are used on these signals instead of flip-flops. These changes will reduce the area and price of your ASIC.

If an asynchronous RAM is used in a circuit that has a Write Enable signal (WE) pulsed every write cycle and a Read Enable signal (RE) pulsed every read cycle, the WE and RE signals can be used to generate the clock for a synchronous RAM. Figure 5 shows some example timing for this type of configuration that will work with AMI's RAS0Nwyz RAM. The clock signal is generated by NORing WE and RE (CLK = WE NOR RE).

Explore AMI's expanding memory capabilities for your next ASIC design to improve your price and performance. Contact your AMI sales representative for more information or for copies of data sheets.

Figure 3: High Speed Pipelined Design Using Asynchronous RAM

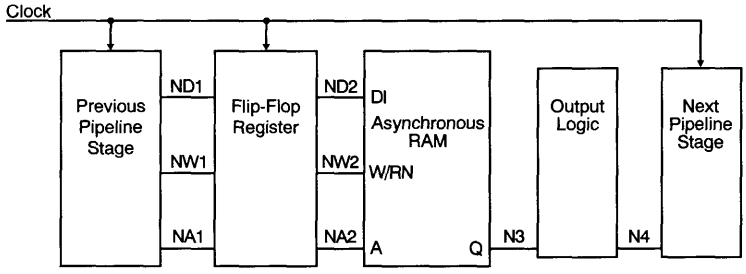


Figure 4: High Speed Pipelined Design Using Synchronous RAM

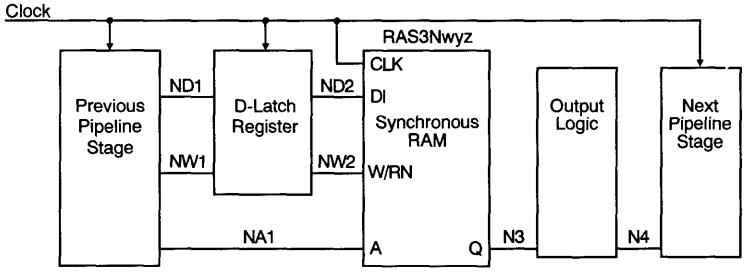
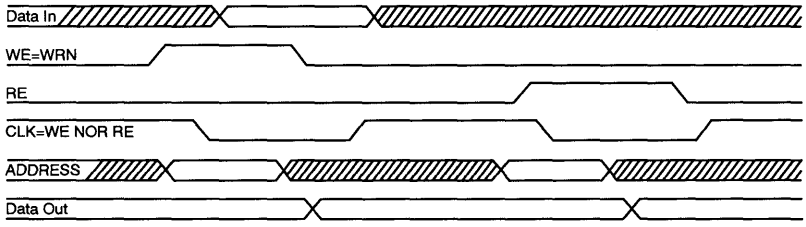


Figure 5: Pulsed WE and RE Signals



AMI SEMICONDUCTORS

Testing RAM Elements in IC Designs

ASIC RAM Application Note

Features

When a RAM is incorporated into an application specific integrated circuit (ASIC) design, special testing considerations arise. This application note points out those special testing considerations and illustrates some possible ways to test a RAM in an ASIC design. The methods described below are not the only ways to test a RAM in an ASIC design; other methods may work better in many instances. The method described is recommended because of its simplicity to generate and its short test time.

The first issue to consider is the controllability and observability of the RAM in your ASIC design. If the RAM is buried in other logic, it may be very difficult to write and read a good test pattern to and from the RAM. One way to solve this problem is to multiplex the inputs and outputs of the RAM directly to available pad cells in the chip design (see figure 1). If there are not enough pad cells, some sort of serial shift scheme could be used. A test pin could be added to the chip to control the multiplexers and any other test circuitry, or an internal test signal could be generated by decoding an otherwise unused input pattern.

The second issue to consider is the test pattern itself. An understanding of the physical layout of the RAS0Nwyz RAM will help in choosing a proper test pattern; therefore, the layout will be explained first. Each output data bit of the RAM has an array of memory bits, as shown in figure 2. As the addresses start at zero and increase, the memory bits accessed start at row 0 column 0, advance to row 0 column 7, advance to row 2 column 0, and follow this pattern through the whole array.

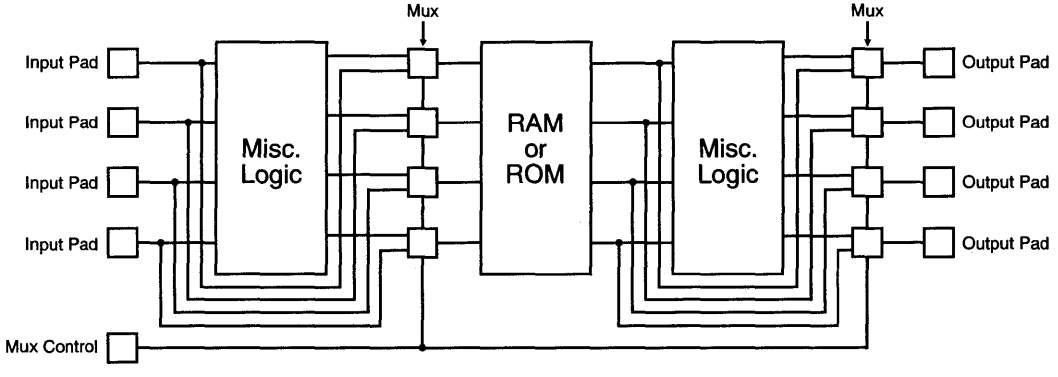
One possible test pattern will now be discussed. Testing all possible input combinations is usually impractical. A better strategy is to find a set of input vectors that exercises all the logic without going through all possible inputs. Preferred vectors are such that each node in the circuit is toggled at least once. Definition of a 100 percent toggled node means starting at zero or one, changing to the opposite state, and then back again. Figure 2 is a view of a RAM core section loaded with a test pattern. If this pattern is loaded and read six times with the rows rotated down one row with each load, the RAM will receive a complete toggle test. Consecutive addressing is used to write data to the RAM, starting at row 0 and column 0, then advancing to column 7. The address then steps to row 1 column 0, and gain advances to column 7. This process is repeated to address all bits of the RAM. Then all the bits are read out to check if they were written properly.

This pattern was selected because it tests the RAM and also has a repetitive characteristic, making test vectors easy to write. Rows are repetitive every 5th row and digits are repetitive every 5th digit.

This pattern also tests for adjacent cells shorted together. This can be seen in figure 2. Each 1 in the memory array is physically surrounded by zeros. If two adjacent memory cells are shorted together, an error should be detected in the test program during the read cycle.

In the notation used below, N(X,Y,Z) means repeat the pattern (X,Y,Z) N times. Note that the pattern is shifted by two places for each adjacent output data bit. This ensures that when a 1 is read out of a data bit, both of the adjacent

Figure 1: Mux Utilization for Testability



data bits should be a zero. This scheme checks for shorts between adjacent output data bits. The data patterns for the six separate writes are as follows:

Where K=0, 1, 2, 3

1st Write

DATA (0+K*5) N(0, 0, 0, 0,1)
DATA (1+K*5) 0, 1, N(0, 0, 0, 0, 1)
DATA (2+K*5) 0, 0, 0, 1, N(0, 0, 0, 0, 1)
DATA (3+K*5) 1, N(0, 0, 0, 0, 1)
DATA (4+K*5) 0, 0, 1, N(0, 0, 0, 0, 1)

2nd Write

DATA (0+K*5) 0, 1, N(0, 0, 0, 0, 1)
DATA (1+K*5) 0, 0, 0, 1, N(0, 0, 0, 0, 1)
DATA (2+K*5) 1, N(0, 0, 0, 0, 1)
DATA (3+K*5) 0, 0, 1, N(0, 0, 0, 0, 1)
DATA (4+K*5) N(0, 0, 0, 0, 1)

3rd Write

DATA (0+K*5) 0, 0, 0, 1, N(0, 0, 0, 0, 1)
DATA (1+K*5) 1, N(0, 0, 0, 0, 1)
DATA (2+K*5) 0, 0, 1, N(0, 0, 0, 0, 1)
DATA (3+K*5) N(0, 0, 0, 0, 1)
DATA (4+K*5) 0, 1, N(0, 0, 0, 0, 1)

4th Write

DATA (0+K*5) 1, N(0, 0, 0, 0, 1)
DATA (1+K*5) 0, 0, 1, N(0, 0, 0, 0, 1)
DATA (2+K*5) N(0, 0, 0, 0, 1)
DATA (3+K*5) 0, 1, N(0, 0, 0, 0, 1)
DATA (4+K*5) 0, 0, 0, 1, N(0, 0, 0, 0, 1)

5th Write

DATA (0+K*5) 0, 0, 1, N(0, 0, 0, 0, 1)
DATA (1+K*5) N(0, 0, 0, 0, 1)
DATA (2+K*5) 0, 1, N(0, 0, 0, 0, 1)
DATA (3+K*5) 0, 0, 0, 1, N(0, 0, 0, 0, 1)
DATA (4+K*5) 1, N(0, 0, 0, 0, 1)

6th Write

DATA (0+K*5) N(0, 0, 0, 0, 1)
DATA (1+K*5) 0, 1, N(0, 0, 0, 0, 1)
DATA (2+K*5) 0, 0, 0, 1, N(0, 0, 0, 0, 1)
DATA (3+K*5) 1, N(0, 0, 0, 0, 1)
DATA (4+K*5) 0, 0, 1, N(0, 0, 0, 0, 1)

N is determined by dividing the address locations by 5 and setting N to an integer such that:

$$\frac{\text{address locations}}{5} \leq N < \frac{\text{address locations}}{5} + 1$$

Care must be taken with the above test patterns when assembling tests that contain more than one Write and Read pattern. Extra vectors are contained in the Write patterns that have "X, X, ...N(..." or if (address locations/ 5) is not a whole number.

EXAMPLE: 64 X 8 RAM

An example of a 64 X 8 RAM will be used to demonstrate how to apply the Data patterns and adjust for any extra vectors.

For an 8 bit wide RAM, K will have the values of 0 and 1 to provide DATA0 through DATA7. N will have the value of:

$$\frac{64}{5} \leq N < \frac{64}{5} + 1 \quad \text{OR} \quad \begin{array}{c} 12.8 \leq N < 13.8 \\ N = 13 \end{array}$$

Figure 2: RAM core physical layout loaded with the suggested pattern

			* **	* **	
10000100	00100001	00001000	01000010	00010000	Row 5
00100001	00001000	01000010	00010000	10000100	Row 4
00001000	01000010	00010000	10000100	00100001	
01000010	00010000	10000100	00100001	00001000	
00010000	10000100	00100001	00001000	01000010	
10000100	00100001	00001000	01000010	00010000	Row 0
Databit 4	Databit 3	Databit 2	Databit 1	Databit 0	
			* Column 7	**Column 0	

A Write and Read cycle will contain 128 vectors; therefore, all six Write and Reads will be less than the maximum of 4096 vectors. One test pattern will be generated for all six Write and Read cycles.

The clock and control inputs are:
WR 6[64(1), 64(0)]
CLK First half of cycle = 1 Second half of cycle = 0

Data for the first Write and Read are:
DATA0 & DATA5 13(0, 0, 0, 0, 1), 63(0)
DATA1 & DATA6 0, 1, 13(0, 0, 0, 0, 1), 61(0)
DATA2 & DATA7 0, 0, 0, 1, 13(0, 0, 0, 0, 1), 59(0)
DATA3 1, 13(0, 0, 0, 0, 1), 62(0)
DATA4 0, 0, 1, 13(0, 0, 0, 0, 1), 60(0)

The total number of vectors should equal 128. The first 64 vectors are for writing into the 64 address locations, and the second 64 vectors are for the time it takes to read the 64 address locations.

Data for the second Write and Read are:
DATA0 & DATA5 0, 1, 13(0, 0, 0, 0, 1), 61(0)
DATA1 & DATA6 0, 0, 0, 1, 13(0, 0, 0, 0, 1), 59(0)
DATA2 & DATA7 1, 13(0, 0, 0, 0, 1), 62(0)
DATA3 0, 0, 1, 13(0, 0, 0, 0, 1), 60(0)
DATA4 13(0, 0, 0, 0, 1), 63(0)

Data for the third Write and Read are:
DATA0 & DATA5 0, 0, 0, 1, 13(0, 0, 0, 0, 1), 59(0)
DATA1 & DATA6 1, 13(0, 0, 0, 0, 1), 62(0)
DATA2 & DATA7 0, 0, 1, 13(0, 0, 0, 0, 1), 60(0)
DATA3 13(0, 0, 0, 0, 1), 63(0)
DATA4 0, 1, 13(0, 0, 0, 0, 1), 61(0)

Data for the fourth Write and Read are:
DATA0 & DATA5 1, 13(0, 0, 0, 0, 1), 62(0)
DATA1 & DATA6 0, 0, 1, 13(0, 0, 0, 0, 1), 60(0)
DATA2 & DATA7 13(0, 0, 0, 0, 1), 63(0)
DATA3 0, 1, 13(0, 0, 0, 0, 1), 61(0)
DATA4 0, 0, 0, 1, 13(0, 0, 0, 0, 1), 59(0)

Data for the fifth Write and Read are:
DATA0 & DATA5 0, 0, 1, 13(0, 0, 0, 0, 1), 60(0)
DATA1 & DATA6 13(0, 0, 0, 0, 1), 63(0)
DATA2 & DATA7 0, 1, 13(0, 0, 0, 0, 1), 61(0)
DATA3 0, 0, 0, 1, 13(0, 0, 0, 0, 1), 59(0)
DATA4 1, 13(0, 0, 0, 0, 1), 62(0)

Data for the sixth Write and Read are the same as the first Write and Read.

These six Writes and Reads should then be combined into one test pattern.

DATA0 & DATA5
13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 59(0), 1, 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 60(0), 13(0, 0, 0, 0, 1), 63(0)

DATA1 & DATA6
0, 1, 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 59(0), 1, 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 60(0), 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 61(0)

DATA2 & DATA7
0, 0, 0, 1, 13(0, 0, 0, 0, 1), 59(0), 1, 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 60(0), 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 59(0)

DATA3
1, 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 60(0), 13(0, 0, 0, 0, 1), 64(0), 1, 13 (0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 59(0), 1, 13(0, 0, 0, 0, 1), 62(0)

DATA4
0, 0, 1, 13(0, 0, 0, 0, 1), 60(0), 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 64(0), 1, 13(0, 0, 0, 0, 1), 59(0), 1, 13(0, 0, 0, 0, 1), 64(0), 1, 13 (0, 0, 0, 0, 1), 60(0)

The nomenclature of this pattern can be further simplified, but its present form is sufficient to demonstrate a method of developing a test pattern.

Numerous books and articles are available that discuss various strategies for testing RAMs. Some of these strategies test RAMs more thoroughly than the one mentioned above, and some of these strategies are not as thorough as the one mentioned above. You may decide which testing strategy to use as long as it adequately tests the RAM with a reasonable number of test vectors.

Additional references:

M.S. Abadir and H.K. Reghbati. Sept. 1983. Functional testing of semiconductor random access memories. *ACM Computer Surveys.* 15 (3): 174-198.

D.S. Suk and S.M. Reddy. Dec. 1981. A march test for functional faults in semiconductor random access memories. *IEEE Transactions on Computer.* C-30: 982-985.

M.A. Breuer and A.D. Friedman. 1976. *Diagnosis and Reliable Design of Digital Systems.* Rockville, MD: Computer Science Press.

C.A. Papachristou and N.B. Sehgal. Feb. 1985. An improved method for detecting functional faults in semiconductor random access memories. *IEEE Transactions on Computers.* C-34(2): 110-116.

SECTION 11
INTRODUCTION TO ABX LIBRARY WITH LIBRARY CHARACTERISTICS

ABX 3.5 micron CMOS Standard Cells

INTRODUCTION

The ABX Standard Cell Library sections 11 through 13 of the data book contain electrical characteristics, delay characteristics, and cell data sheets. The library is designed for operation from 2.5V to 11V. Two libraries are provided. The ABOHS library is implemented in the AB n-well process with a separate p-substrate bus. The ABEHS library is implemented in the AB p-well process with a separate n-substrate bus. Both libraries have explicit power pins so that the digital power can be wired separately from the analog cells.

The ABO2S library is not included in this data book. This library is designed for operation from 2.5V to 8.0V. The library is implemented in the AB n-well process with a separate p-substrate bus. Explicit power pins are used in this library so that digital power can be wired separately from the analog cell. Using this library results in better speed and area performance when voltages higher than 8V are not needed.

LIBRARY FEATURES

The library implements a CMOS subset of AMI's ASIC Standard Library. The ASIC Standard Library is the core offering for both standard cells and gate arrays.

Standard cell libraries are functionally compatible with gate array libraries because of the ASIC Standard approach. Both libraries use the same transistor level schematics except for transistor sizes, because standard cells take advantage of the ability to vary transistor widths to optimize the switch point of the gates. The standard cells have comparable delays with the gate array cells so that designs can be migrated from one library to the other with minimum effort.

This standard cell library was developed using AMI's internal design system called Accolade. This system is a complete cell design system featuring symbolic graph compaction, mask data extraction, characterization, logic model data creation, and data sheet creation. This system makes the libraries more process independent for faster cell migration to new process technologies.

Megacells are available, such as core processors, RAMs, DPRAMs, ROMs, EE memories, FIFOs, and DSP type cells. These libraries also support mixed signal applications.

ABX 3.5 micron CMOS Standard Cells

LIBRARY CHARACTERISTICS

DC OPERATING CHARACTERISTICS

Table 1 contains the absolute maximum ratings for ABX ASIC library chips using the standard cell libraries. Tables 2 through 5 contain the input and output operating specifications for the library at 5V and 10V operation. The library is characterized for operation from 2.5V to 11V. Pad drivers in table 4 and data sheets are referenced by their worst case output current drive at 5V, i.e., the 1mA driver in table 4. The output current drive will vary with the supply voltage, Vol, and Voh specifications. Contact the factory for operating specifications at supply voltages other than 5V or 10V.

Table 1: Absolute Maximum Ratings

Parameter	Range	Units
VDD, Supply Voltage	-0.3 to 12.0	Volts
Input Pin Voltage	-0.3 to VDD+0.3	Volts
Input Pin Current	-10.0 to 10.0	mA
Storage Temperature Plastic Packages	-55 to 125	°C
Storage Temperature Ceramic Packages	-65 to 150	°C
Lead Temperature	300	°C for 10 sec.

Note that these specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect the long-term reliability of the device.

Table 2: Operating Specifications

Parameter	Minimum	Maximum	Units
VDD, Supply Voltage	2.5	11.0	Volts
Ambient Temperature - Military	-55	125	°C
Ambient Temperature - Commercial	0	70	°C

Table 3: Input Operating Specifications

Parameter	Minimum	Maximum	Units
CMOS Input Specifications, (9.0V ≤ VDD ≤ 11.0V, Commercial T_A)			
Vil Low Level Input Voltage		0.3*VDD	Volts
Vih High Level Input Voltage	0.7*VDD		Volts
Iil Low Level Input Current		-1.0	µA
Iih High Level Input Current		1.0	µA
Iil Input Pull-up Current	-45	-166	µA
Iih Input Pull-down Current	39	173	µA
Vt- Schmitt Negative Threshold	0.2*VDD		Volts
Vt+ Schmitt Positive Threshold		0.8*VDD	Volts
Vh Schmitt Hysteresis	3.0		Volts

Parameter	Minimum	Maximum	Units
CMOS Input Specifications, (4.5V ≤ VDD ≤ 5.5V, Commercial T_A)			
Vil Low Level Input Voltage		0.3*VDD	Volts
Vih High Level Input Voltage	0.7*VDD		Volts
Iil Low Level Input Current		-1.0	µA
Iih High Level Input Current		1.0	µA
Iil Input Pull-up Current	-12	-46	µA
Iih Input Pull-down Current	11	42	µA
Vt- Schmitt Negative Threshold	0.2*VDD		Volts
Vt+ Schmitt Positive Threshold		0.8*VDD	Volts
Vh Schmitt Hysteresis	1.0		Volts

Table 4: Output Operating Specifications

	VDD = 5.0V ± 10%		VDD = 10V ± 10%		
Parameter	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Units**
1.0mA Driver					
Vol Low Level Output Voltage		0.4		0.1*VDD	Volts
Voh High Level Output Voltage	2.4		0.9*VDD		Volts
Iol Low Level Output Current		1.0		4.0	mA
Ioh High Level Output Current		-1.0		-2.2	mA
2.0mA Driver					
Vol Low Level Output Voltage		0.4		0.1*VDD	Volts
Voh High Level Output Voltage	2.4		0.9*VDD		Volts
Iol Low Level Output Current		2.0		8.1	mA
Ioh High Level Output Current		-2.0		-4.4	mA
4.0mA Driver					
Vol Low Level Output Voltage		0.4		0.1*VDD	Volts
Voh High Level Output Voltage	2.4		0.9*VDD		Volts
Iol Low Level Output Current		4.0		16.2	mA
Ioh High Level Output Current		-4.0		-8.8	mA
8.0mA Driver					
Vol Low Level Output Voltage		0.4		0.1*VDD	Volts
Voh High Level Output Voltage	2.4		0.9*VDD		Volts
Iol Low Level Output Voltage		8.0		32.4	mA
Ioh High Level Output Current		-8.0		-17.5	mA

Figures 1 through 4 show typical current voltage curves for the pad driver transistors from 1mA to 8mA and VDD equal to both 5 volts and 10 volts. References to "typical" mean the data was characterized for Tj = 25° C, VDD = 5 volts or 10 volts, and typical (nominal) process. Figures 5 through 8 show the typical current voltage curves for input pads with pull-up and pull-down devices.

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Figure 1: Typical CMOS N-Channel Driver DC Characteristics at VDD = 10V

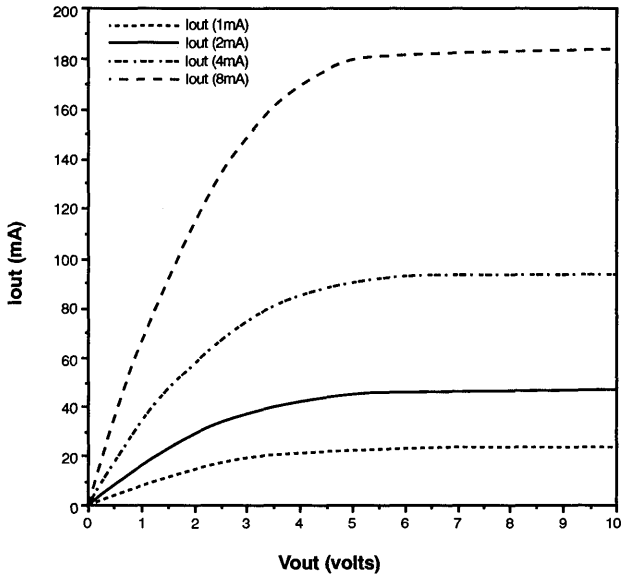

Figure 2: Typical CMOS P-Channel Driver DC Characteristics at VDD = 10V

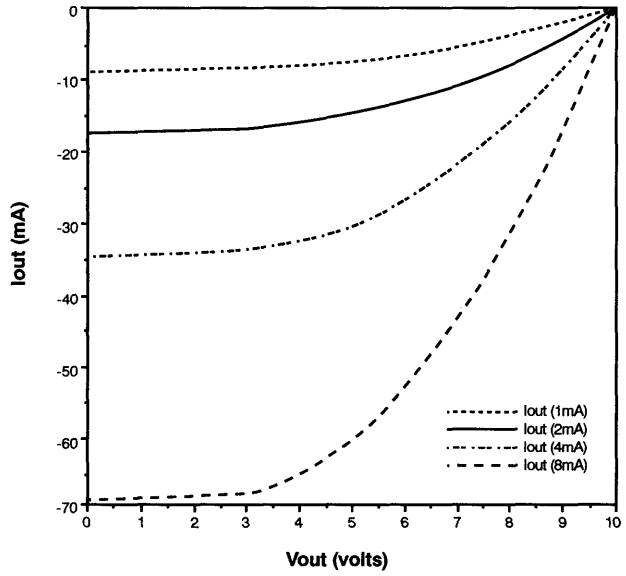

Figure 3: Typical CMOS N-Channel Driver DC Characteristics at VDD = 5V

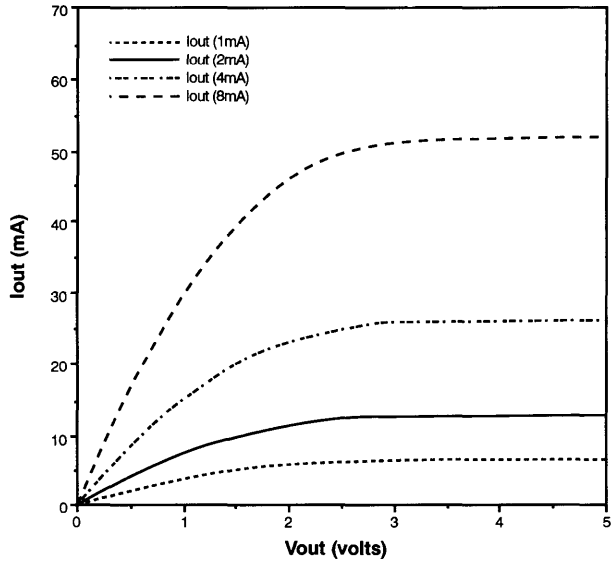

Figure 4: Typical CMOS P-Channel Driver DC Characteristics at VDD = 5V

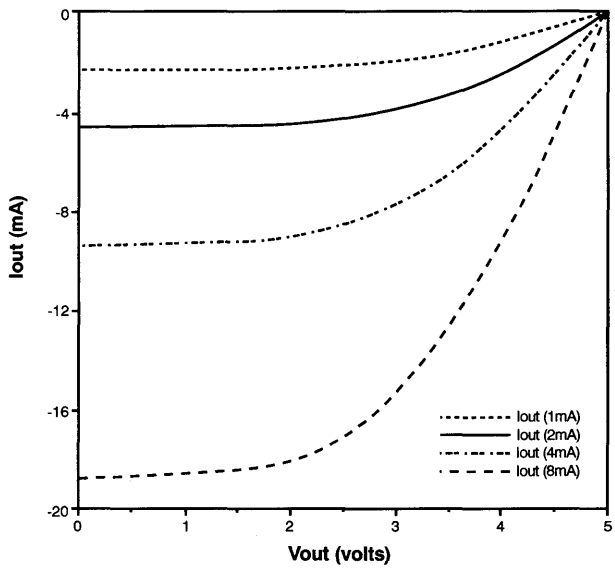

Figure 5: Typical Input Pull-down Characteristics at VDD = 10V

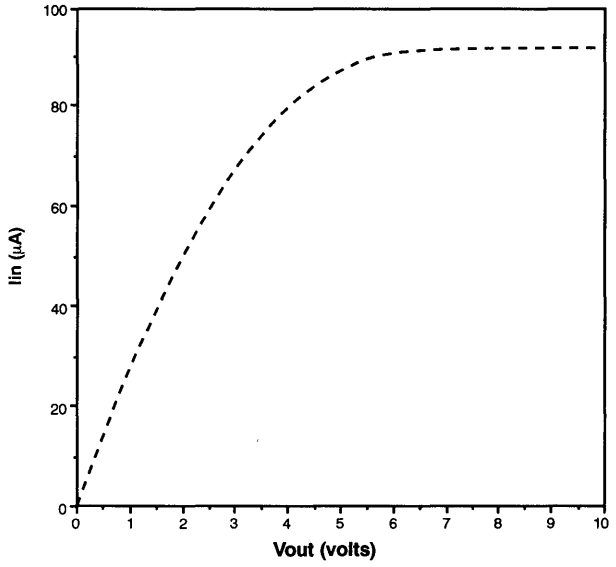

Figure 6: Typical Input Pull-up Characteristics at VDD = 10V

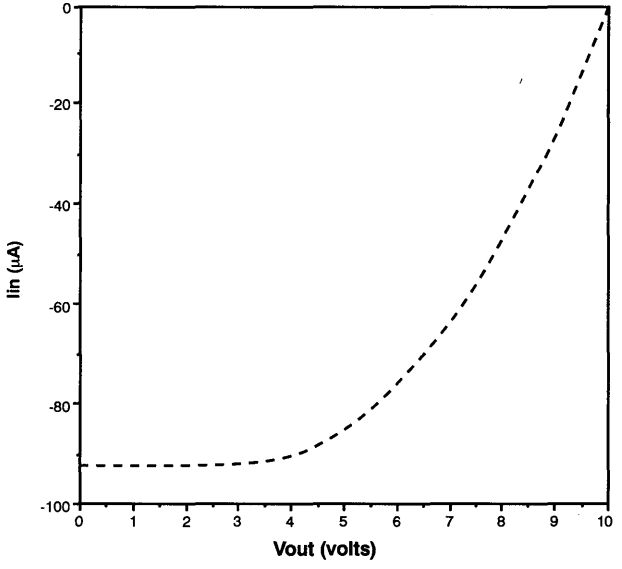

Figure 7: Typical Input Pull-down Characteristics at VDD = 5V

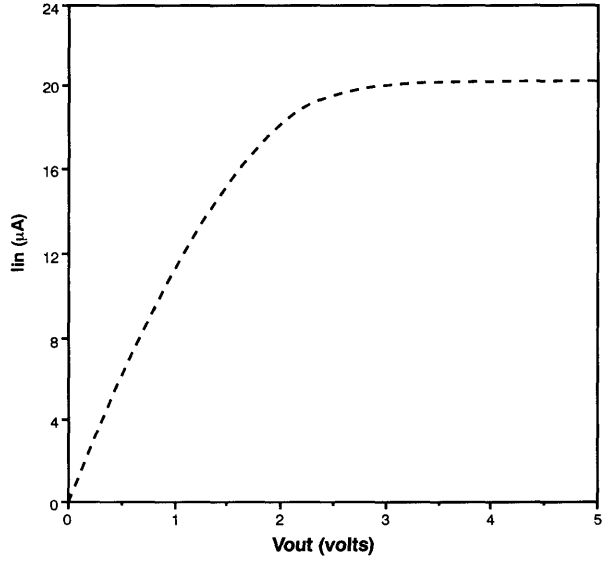

Figure 8: Typical Input Pull-up Characteristics at VDD = 5V

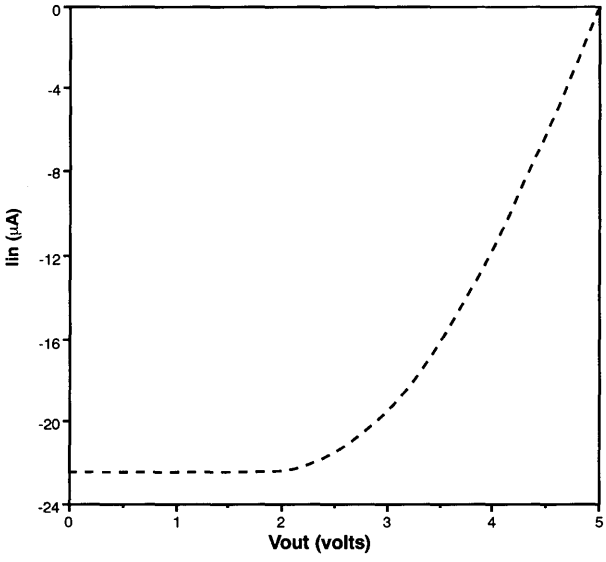

Figure 9, table 5, and table 6 show derating factors for the current due to temperature voltage and process for 10V operation. Figure 10, table 7, and table 8 show derating factors for the current due to temperature voltage and process for 5V operation. To obtain a current value at conditions other than typical, multiply the derating factors corresponding to those conditions to the current values from the figures 1 through 8, i.e., $K_{TDC}*K_{VDC}*K_{PDC}*I_{DC}$. More precise estimates for current at different conditions can be obtained from the MSDS workstation or by contacting the factory.

Figure 9: Temperature Derating Factors for DC Characteristics at VDD = 10V

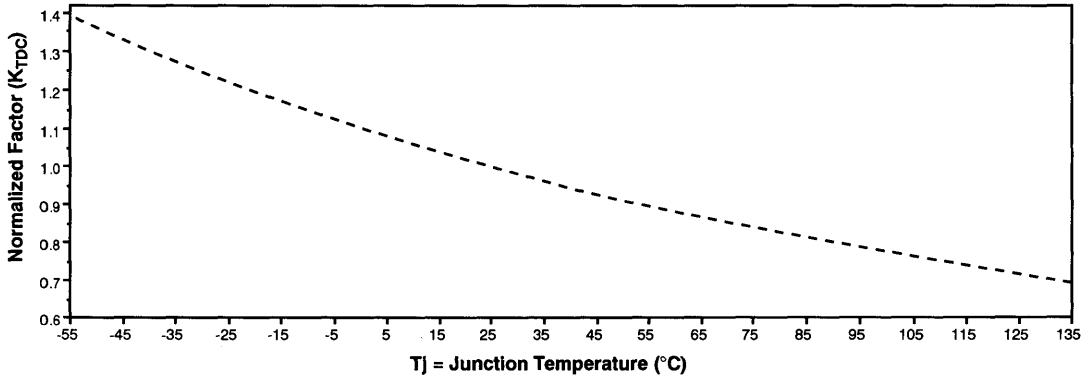

Table 5: Voltage Derating Factors for DC Characteristics at VDD = 10V

	N-Channel (Vol = .1VDD)			P-Channel (Voh = .9VDD)		
VDD	9.0	10.0	11.0	9.0	10.0	11.0
K_{VDC}	0.82	1.00	1.19	0.84	1.00	1.16

Table 6: Process Derating Factors for DC Characteristics at VDD = 10V

	N-Channel (Vol = .1VDD)			P-Channel (Voh = .9VDD)		
Process	WCS	TYP	BCS	WCS	TYP	BCS
K_{PDC}	0.83	1.00	1.21	.82	1.00	1.23

Figure 10: Temperature Derating Factors for DC Characteristics at VDD = 5V

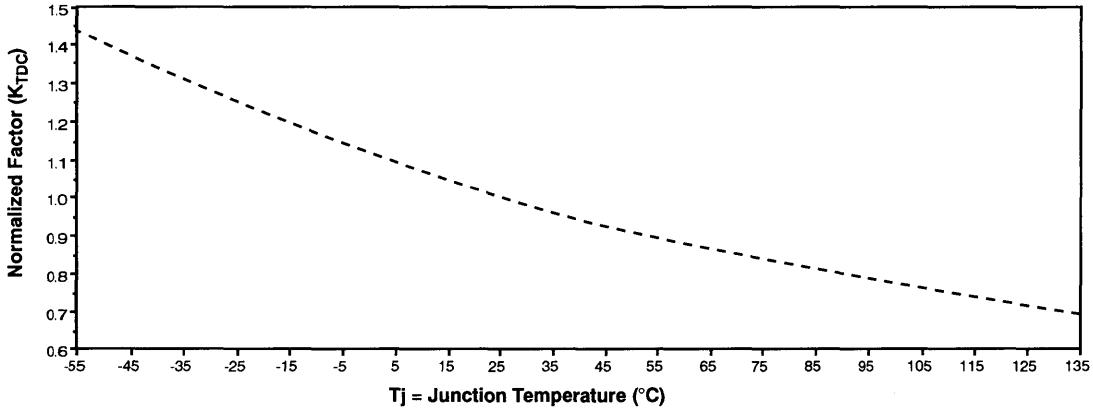

Table 7: Voltage Derating Factors for DC Characteristics at VDD = 5V

	N-Channel (Vol = 0.4V)			P-Channel (Voh = 2.4V)		
VDD	4.5	5.0	5.5	4.5	5.0	5.5
K_{VDC}	0.88	1.00	1.11	0.76	1.00	1.26

Table 8: Process Derating Factors for DC Characteristics at VDD = 5V

	N-Channel (Vol = 0.4V)			P-Channel (Voh = 2.4V)		
Process	WCS	TYP	BCS	WCS	TYP	BCS
K_{PDC}	0.78	1.00	1.28	0.72	1.00	1.38

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DELAY OPERATING CHARACTERISTICS

Delay values for CMOS cells are measured between the input and output 50% voltage supply (Vdd) crossing points. All delays are characterized at typical conditions (Tj = 25 °C, Vdd = 10 volts, and typical process).

Figures 11, 12, and table 9 contain derating factors for various temperatures, voltages, and process variations respectively. To obtain a delay value at conditions other than typical, multiply the derating factors corresponding to those conditions to the current values from the delays in the data sheets, i.e., $K_T*K_V*K_P*T_D$, where T_D can be a delay from the delay characteristics table mentioned on page 11-13 or a value calculated from the propagation delay equations, also mentioned on page 11-13.

Figure 11: Temperature Derating Factors for Delay Characteristics

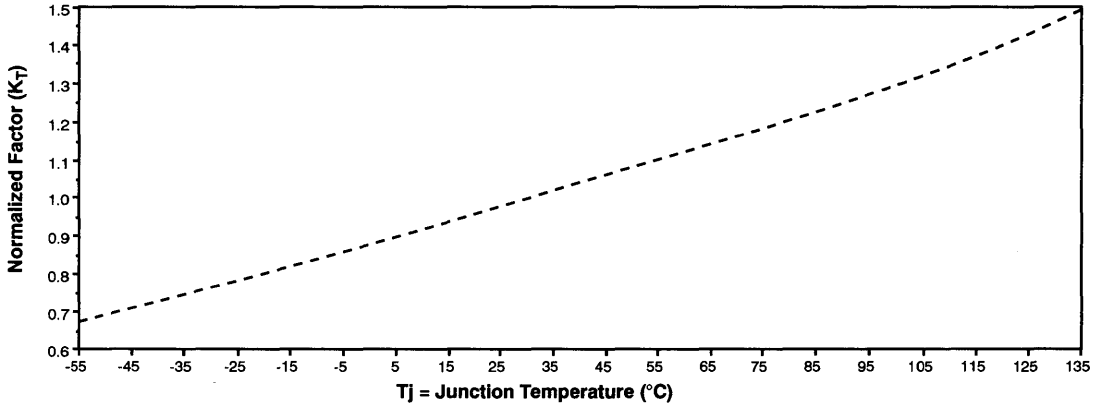


Figure 12: Voltage Derating Factors for Delay Characteristics

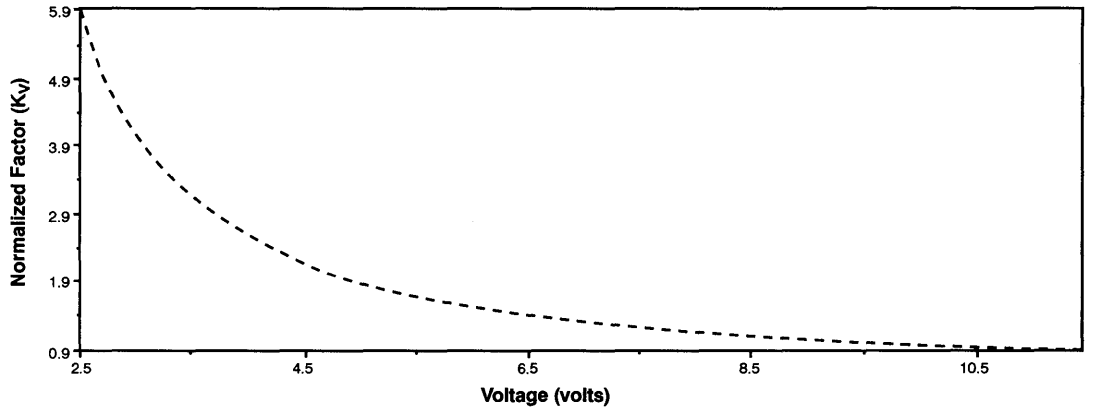


Table 9: Process Derating Factors for Delay Characteristics

	WORST CASE	TYPICAL CASE	BEST CASE
K_P	1.33	1.00	0.75

INTERPRETING THE DATA SHEET

Figure 13 shows a typical data sheet and points out the main features of the data sheet. Not shown is a schematic which accompanies some of the more complex cells.

Figure 13

Cell Name →

AA21

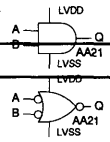
AMI SEMICONDUCTORS

Library Type →

ABX 3.5 micron CMOS Standard Cells

Description →

Description:
AA21 is a two-input gate which performs the logical AND function.

Logic Symbol	Truth Table	Pin Loading
Logic Symbol → 	Truth Table →	Pin Loading →

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

	Cl (pF)
A	0.09
B	0.09

Equivalent Gates →
Equivalent Gates:.....1.3

Bolt Syntax →
Bolt Syntax:.....Q .AA21 A B LVDD LVSS;

Power Characteristics →

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.93	nA
†C_{pd}	0.24	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay Characteristics →

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.50	3.39	2.45	3.40	5.29
		t_{PHL}	1.57	3.51	2.55	3.54	5.51

Propagation Delay Equations →
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

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A description of these features of the data sheet are as follows.

LIBRARY TYPE: Designates the feature size and library type such as standard cell or gate array.

CELL NAME: AMI's cell name.

DESCRIPTION: A brief sentence about the function of the cell.

LOGIC SYMBOL: Shows a picture of the symbol as it appears as an icon in the workstation design kits.

TRUTH TABLE: A boolean table showing the output logic levels as a function of the input logic levels.

Types of logic levels found in the logic tables are as follows:

H	=	High level steady state,
L	=	Low level steady state,
↑	=	Transition from Low level to High level,
↓	=	Transition from High level to Low level,
X	=	Any level including transitions,
NC	=	No Change in output level for a given set of input levels,
IL	=	The output level is unknown for this set of illegal input levels,
Z	=	High impedance level,
UN	=	Undriven Node or input,
Q(n)	=	The level of Q before an active transition on the affecting node, and
QN(n)	=	The level of QN before an active transition on the affecting node.

PIN LOADING: A table of cell input capacitances in picofarads. Output pin capacitance is given for 3 state cells only. This information can be used to determine the fan-out loading on cell outputs.

EQUIVALENT GATES: Equivalent gates for the cell is defined as the cell area normalized to the area of the NA21 (2 input nand gate).

BOLT SYNTAX: BOLT (Block Oriented Logic Translator) is an AMI proprietary netlist format. This line shows the BOLT syntax for the cell. One example of the use of BOLT is as a design interface from the workstation design kits to AMI.

POWER CHARACTERISTICS:

Power for the cell can be described in three parts. The first part is the power dissipated due to the leakage current across the channels and through the formed diodes. The second part is due to the switching voltage across capacitance on the internal nodes of the cell. The third part is due to the switching voltage across a load capacitance.

The power characteristics table provides the static leakage current for a junction temperature of 85 ° C, and the capacitance for all the switching nodes in the cell. It also gives the equation calculating power from these two values. It does not include the power due to the load capacitance. This capacitance can be obtained by adding up all the input capacitances of the driven cells and adding the interconnect capacitance. The average interconnect capacitance for the ABxHS ASIC Standard Library is 0.051pF. AMI can prepare an estimate of the power upon submission of a netlist which uses a statistical model of the interconnect based on die size and fan-out.

$$POWER = (Static\ I_{DD})\ V_{DD} + C_{pd}\ V^2_{DD} f + C_L V^2_{DD} f$$

where

Static I_{DD} = static leakage current of the cell
V_{DD} = operating voltage
C_{pd} = capacitance of the switching nodes in the cell
f = frequency of operation
C_L = capacitance of the driven pins and interconnect

The frequency term of the power equation dominates, making the static leakage current term insignificant. However, the static leakage current term can be used to find the standby current.

DELAY CHARACTERISTICS: This table contains delay data for the various input to output paths in the cells. Table 10 explains each column in the delay characteristics table.

Table 10: EXPLANATION OF COLUMNS IN THE CELL CHARACTERISTICS TABLE

Column Name	Explanation	
Delay (ns) From To	Names the two pins that identify the path for the delay	
Parameter	Mnemonic for the propagation delay or timing parameter whose value can be calculated by using the tdx and Ktdx columns in conjunction with the propagation delay equation.	
	t_{PLH}	Input to output propagation delay for a rising edge on the output
	t_{PHL}	Input to output propagation delay for a falling edge on the output
	t_{ZH}	High impedance to high level delay
	t_{ZL}	High impedance to low level delay
	t_{HZ}	High level to high impedance delay
	t_{LZ}	Low level to high impedance delay
	t_{su}	Input setup time with respect to clock
	t_h	Input hold time
	t_w	Input pulse width
tdx (ns)	Contains values for the intrinsic delay through the cell. The x in t_{dx} is a variable representing r for the rising output delay (t_{PLH}), f for the falling output delay (t_{PHL}), or x for any of the other parameters. The values are given in nanoseconds.	
Ktdx (ns/pF)	Contains delay per capacitance values to determine the delay due to capacitance loading on the "To" pin. The x in K_{tdx} has the same meaning as in the t_{dx}. The values are given in nanoseconds/picofarad.	
Number of fan-outs	Contains the capacitance value and delay values for different loads. For output pad cells 25pF, 50pF, 75pF, and 100pF loads are used. For core cells and input pad cells fan-outs of 2, 4, and 8 gates are used. These fan-out loads are determined by the indicated number of NA21 inputs and an interconnect capacitance from a statistical table of fan-out values for a chip that is 250 mils on a side.	

PROPAGATION DELAY EQUATION: This equation shows how to calculate the total delay for the load dependent delay paths using the delay characteristics table. Here are some notes to help in understanding how to use the equations.

$K_PK_VK_T$ equals $K_P*K_V*K_T$, which are the derating factors for finding delays at conditions other than typical. Use figures 11 and 12 and table 9 for these values of K_P, K_V, and K_T.

When the equations use t_{dx} and K_{tdx}, use either rise delay values or fall delay values for both variables.

If rise and fall delay numbers need to be inter-mixed, the equations will specifically state this, i.e., $t_{dr} + K_{tdf}(C_L)$.

If the equations inter-mix delays from different paths, then the delay variable will designate this with a pin value in parentheses at the end of the variable.

ABX 3.5 micron CMOS Standard Cells

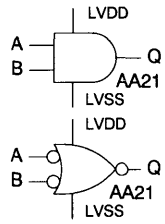
ABX Process Families

Features	ABC	ABD	ABE	ABF	ABG	ABM	ABN	ABO	ABP	ABQ
N Substrate	X	X	X	X	X					
P Substrate						X	X	X	X	X
Bipolar	X			X	X	X	X		X	
EE Devices	X	X				X				X
Double Metal	X	X	X	X	X	X	X	X	X	X
Double Poly	X	X	X	X	X	X	X	X		X
Single Poly									X	
12V/5V Operation	X	X	X	X	X	X	X	X	X	X
Program Device					X					

SECTION 12
ABX LIBRARY

Description:
AA21 is a two-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Ci (pF)
A	0.09
B	0.09

Equivalent Gates:.....1.3
Bolt Syntax:.....Q .AA21 A B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.93	nA
†C_{pd}	0.24	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

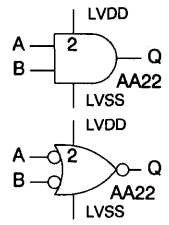
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.50	3.39	2.45	3.40	5.29
		t_{PHL}	1.57	3.51	2.55	3.54	5.51

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ABX 3.5 micron CMOS Standard Cells

Description:
AA22 is a two-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Ci (pF)
A	0.09
B	0.09

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .AA22 A B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.59	nA
†C_{pd}	0.34	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

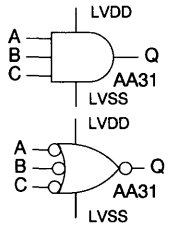
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.82	1.82	2.33	2.84	3.86
		t_{PHL}	1.82	1.82	2.33	2.84	3.86

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
AA31 is a three-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .AA31 A B C LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.42	nA
†C_{pd}	0.28	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.90	3.50	2.88	3.86	5.82
		t_{PHL}	1.91	3.58	2.91	3.92	5.93

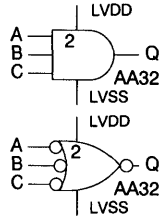
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

AA32

ABX 3.5 micron CMOS Standard Cells

Description:
AA32 is a three-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09

Equivalent Gates:.....2.0
Bolt Syntax:.....Q .AA32 A B C LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.09	nA
†C_{pd}	0.39	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

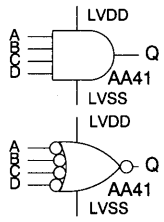
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	2.34	1.98	2.89	3.45	4.56
		t_{PHL}	2.23	1.95	2.77	3.31	4.40

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
AA41 is a four-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Pin Loading

	Ci (pF)
A	0.08
B	0.10
C	0.09
D	0.09

Equivalent Gates:.....2.0
Bolt Syntax:.....Q .AA41 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.87	nA
†C_{pd}	0.31	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	2.38	3.66	3.41	4.43	6.48
		t_{PHL}	2.30	3.68	3.33	4.36	6.42

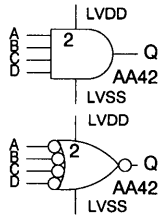
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

AA42

ABX 3.5 micron CMOS Standard Cells

Description:
AA42 is a four-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09
D	0.09

Equivalent Gates:.....2.3
Bolt Syntax:.....Q .AA42 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.53	nA
†C_{pd}	0.40	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

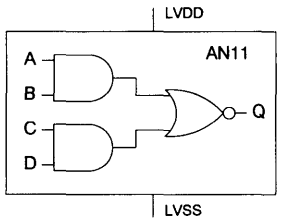
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	2.73	2.11	3.33	3.92	5.10
		t_{PHL}	2.53	2.02	3.09	3.66	4.79

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
AN11 is an AND-NOR circuit consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

Pin Loading

	Ci (pF)
A	0.09
B	0.08
C	0.08
D	0.08

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .AN11 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.40	nA
†C_{pd}	0.23	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.24	4.60	2.53	3.82	6.40
		t_{PHL}	1.80	5.43	3.32	4.85	7.89

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

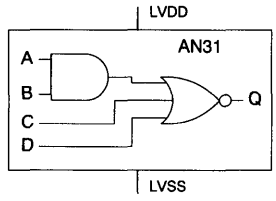
AN31

ABX 3.5 micron CMOS Standard Cells

Description:

AN31 is an AND-NOR circuit consisting of a 2-input AND gate and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09
D	0.08

Equivalent Gates:.....1.6
Bolt Syntax:.....Q .AN31 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.59	nA
†C_{pd}	0.22	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

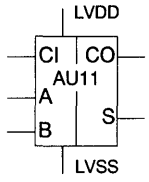
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.69	7.57	3.81	5.93	10.17
		t_{PHL}	2.82	9.45	5.46	8.11	13.40

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
AU11 is a combinational one-bit full adder.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Pin Loading

	Ci (pF)
A	0.35
B	0.35
CI	0.30

Equivalent Gates:.....6.3
Bolt Syntax:.....CO S .AU11 A B CI LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.45	nA
†C_{pd}	1.04	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} $V_{DD}{}^2$ f
†Note: C_{pd} does not include interconnect capacitance.

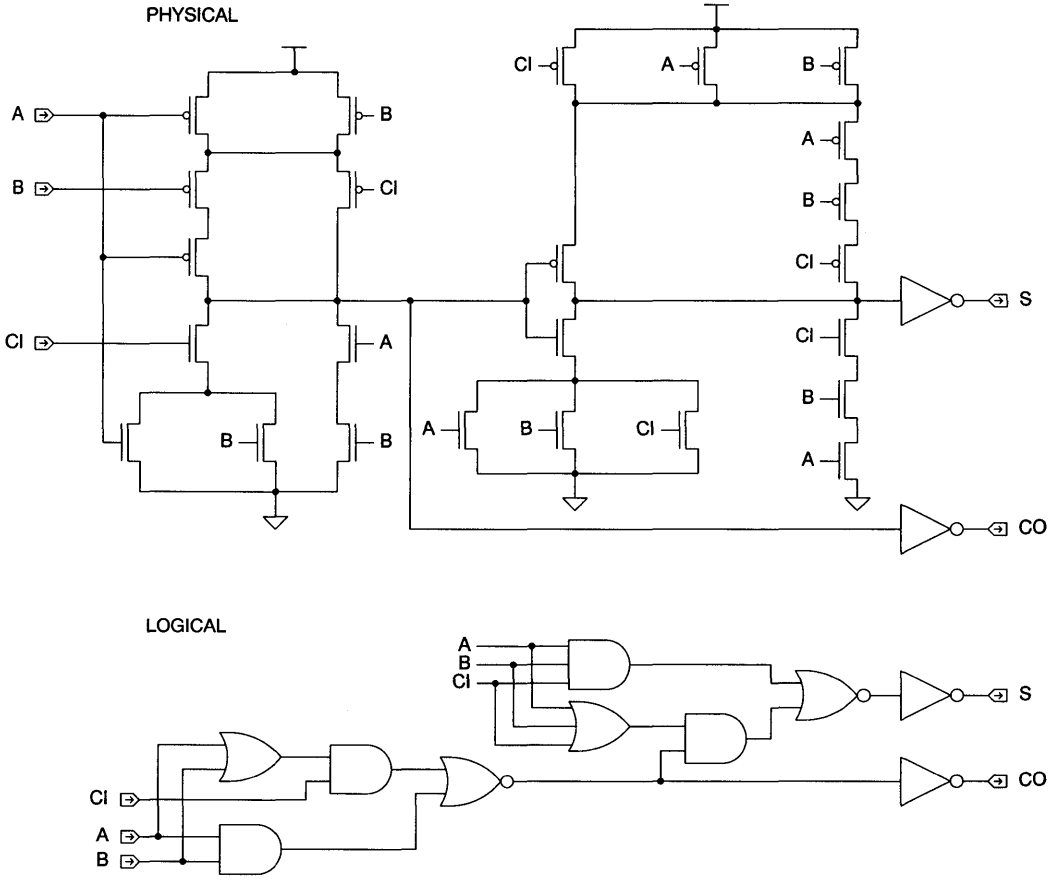
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	S	t_{PLH}	6.32	3.67	7.35	8.38	10.43
		t_{PHL}	7.12	4.06	8.26	9.40	11.67
B	S	t_{PLH}	6.84	3.67	7.87	8.90	10.96
		t_{PHL}	3.44	4.06	4.58	5.72	7.99
CI	S	t_{PLH}	6.39	3.67	7.42	8.45	10.50
		t_{PHL}	3.04	4.06	4.18	5.32	7.59
A	CO	t_{PLH}	5.56	4.20	6.74	7.91	10.27
		t_{PHL}	3.19	4.19	4.37	5.54	7.88
B	CO	t_{PLH}	5.38	4.20	6.56	7.73	10.08
		t_{PHL}	3.40	4.19	4.57	5.75	8.09
CI	CO	t_{PLH}	4.31	4.20	5.49	6.66	9.01
		t_{PHL}	2.60	4.19	3.77	4.94	7.29

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

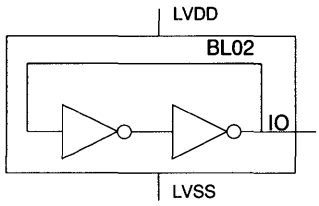
ABX 3.5 micron CMOS Standard Cells

Logic Schematic



Description:
BL02 is a tri-state bus latch that stores the final binary level on the bus when left undriven.

Logic Symbol



Truth Table

N/A

Pin Loading

	Ci (pF)
IO	0.13

Equivalent Gates:.....1.4
Bolt Syntax:.....IO .BL02 LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.02	nA
†C_{pd}	0.30	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)
IO	IO	t_{PLH} t_{PHL}	2.18 2.14

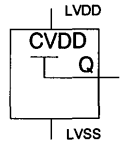
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

CVDD

ABX 3.5 micron CMOS Standard Cells

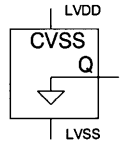
Description:
CVDD is the resistive tie-up to the core Vdd bus for all cell inputs.

Equivalent Gates:.....1.0
Bolt Syntax:..... Q .CVDD LVDD LVSS;



Description:
CVSS is the resistive tie-down to the core Vss bus for all cell inputs.

Equivalent Gates:.....1.0
Bolt Syntax: ..... Q .CVSS LVDD LVSS;

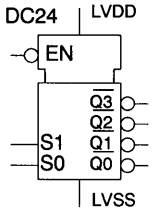


ABX 3.5 micron CMOS Standard Cells

Description:

DC24 is a two-to-four line decoder/demultiplexer with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Pin Loading

	Ci (pF)
S0	0.29
S1	0.27
EN	0.09

Equivalent Gates:.....6.8

Bolt Syntax:.....Q0N Q1N Q2N Q3N .DC24 EN S0 S1 LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.08	nA
†C_{pd}	1.48	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

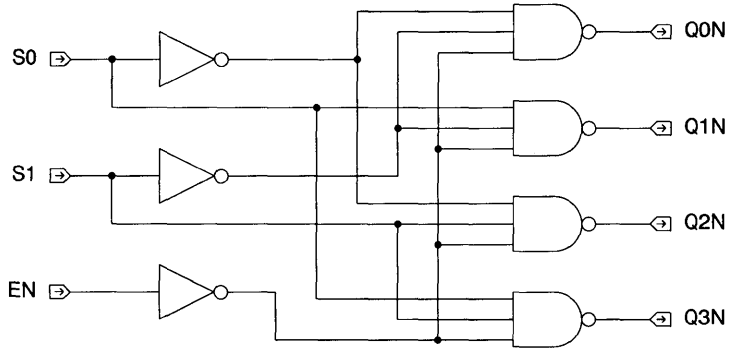
Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Sx	QN	t_{PLH}	2.11	3.93	3.22	4.32	6.52
		t_{PHL}	0.95	5.11	2.38	3.81	6.67
EN	QN	t_{PLH}	3.05	3.93	4.16	5.26	7.46
		t_{PHL}	2.70	5.11	4.13	5.55	8.41

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

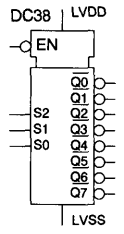


DC38

ABX 3.5 micron CMOS Standard Cells

Description:
DC38 is a three-to-eight line decoder/demultiplexer with active low enable.

Logic Symbol



Truth Table

Truth Table Appears On Next Page

Pin Loading

	Ci (pF)
S0	0.51
S1	0.46
S2	0.48
EN	0.09

Equivalent Gates:.....16.7
Bolt Syntax:.....Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N .DC38 EN S0 S1 S2 LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	20.51	nA
†C_{pd}	3.51	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

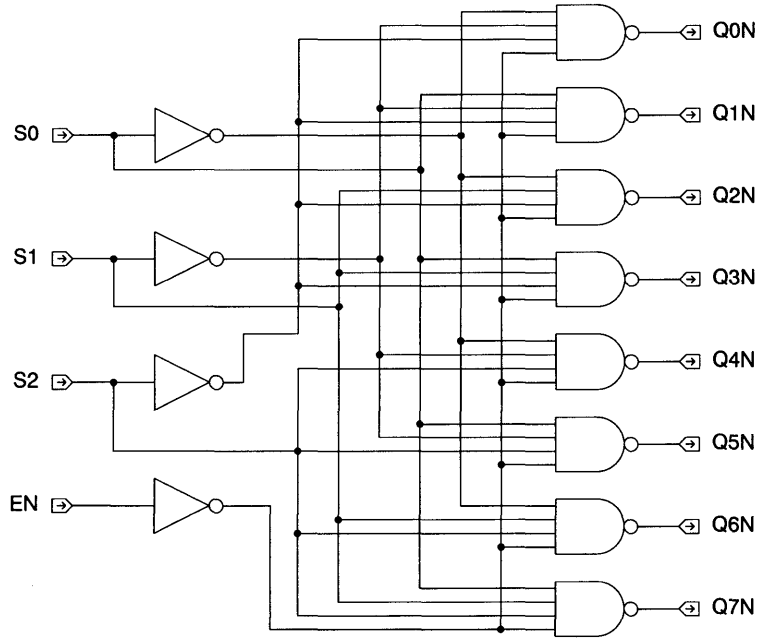
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Sx	QN	t_{PLH}	3.41	4.27	4.60	5.80	8.19
		t_{PHL}	1.23	5.87	2.88	4.52	7.81
EN	QN	t_{PLH}	5.00	4.27	6.19	7.39	9.78
		t_{PHL}	4.16	5.87	5.80	7.45	10.73

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

Logic Schematic

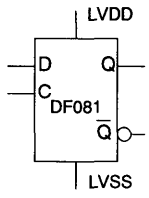


DF081

ABX 3.5 micron CMOS Standard Cells

Description:
DF081 is a static, master-slave D flip-flop without SET or RESET. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
H	↑	H	L
L	↑	L	H
X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.10
C	0.27

Equivalent Gates:.....4.1
Bolt Syntax:.....Q QN .DF081 C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.33	nA
†C_{pd}	0.95	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	2.46 0.70	6.00 5.30	4.14 2.18	5.82 3.67	9.18 6.64
C	QN	t_{PLH} t_{PHL}	3.19 3.92	3.62 4.04	4.21 5.05	5.22 6.18	7.25 8.44
Min C Width	High	t_w				6.18	
Min C Width	Low	t_w	2.96				
Min D Setup		t_{su}	2.96				
Min D Hold		t_h	0.00				

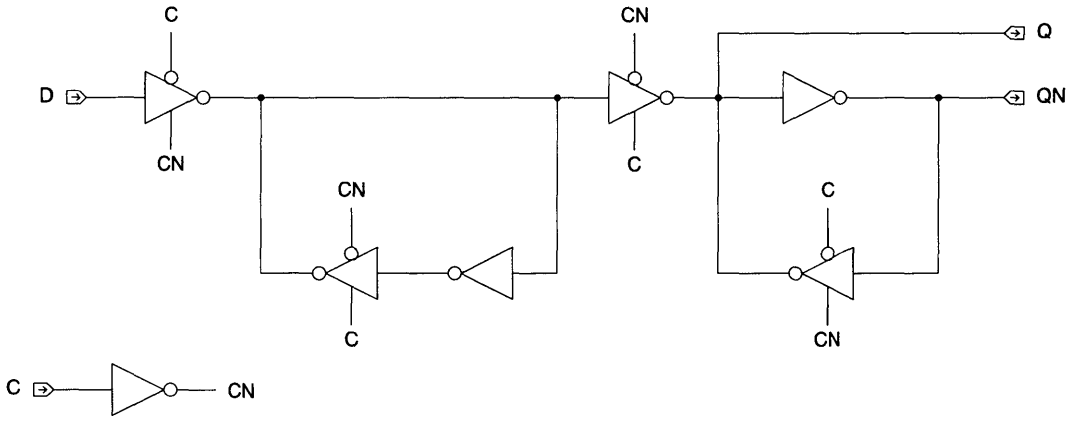
For Q Delays:

$$t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$$

For QN Delays:

$$t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{dr}(QN) + (k_{tdr}(QN)\, C_L(QN)) + (k_{tdf}(Q)\, C_L(Q))]$$
$$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{df}(QN) + (k_{tdf}(QN)\, C_L(QN)) + (k_{tdr}(Q)\, C_L(Q))]$$

Logic Schematic

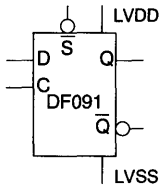


DF091

ABX 3.5 micron CMOS Standard Cells

Description:
DF091 is a static, master-slave D flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.10
C	0.27
SN	0.20

Equivalent Gates:.....5.0
Bolt Syntax:.....Q QN .DF091 C D SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.94	nA
†C_{pd}	1.14	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

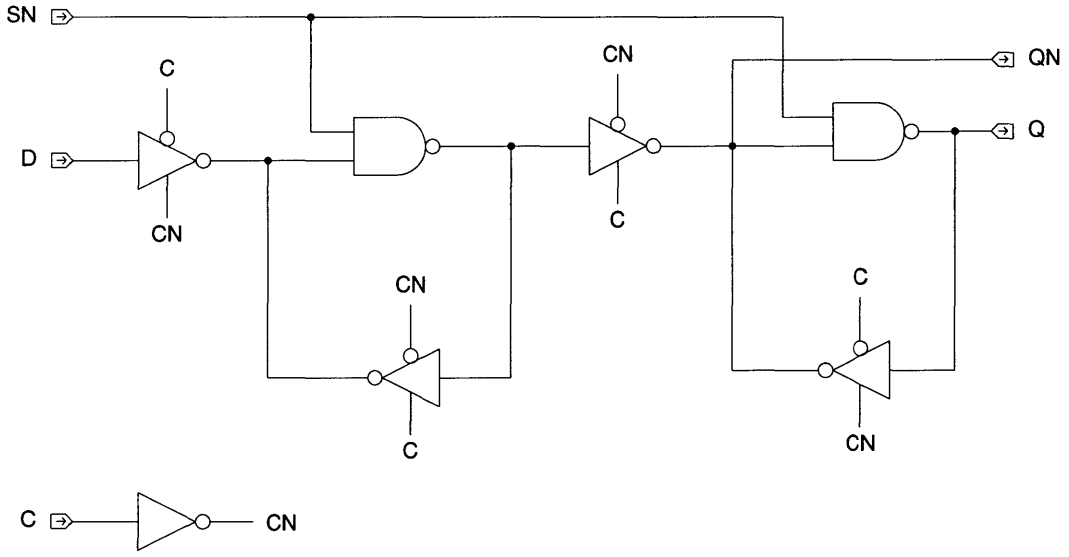
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	2.72 4.29	3.89 4.76	3.81 5.62	4.90 6.96	7.08 9.63
C	QN	t_{PLH} t_{PHL}	2.61 1.28	6.00 5.36	4.29 2.78	5.97 4.28	9.33 7.29
SN	Q	t_{PLH}	0.93	3.89	2.02	3.12	5.30
SN	QN	t_{PHL}	3.00	5.36	4.50	6.00	9.00
Min C Width	High	t_w				6.96	
Min C Width	Low	t_w	3.93				
Min SN Width	Low	t_w				6.00	
Min D Setup		t_{su}	3.21				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	1.32				
Min SN Hold		t_h	1.26				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

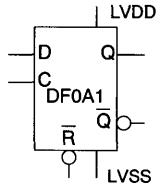


DF0A1

ABX 3.5 micron CMOS Standard Cells

Description:
DF0A1 is a static, master-slave D flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.10
C	0.28
RN	0.09

Equivalent Gates:.....5.7
Bolt Syntax:..... Q QN .DF0A1 C D RN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.67	nA
†C_{pd}	1.40	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

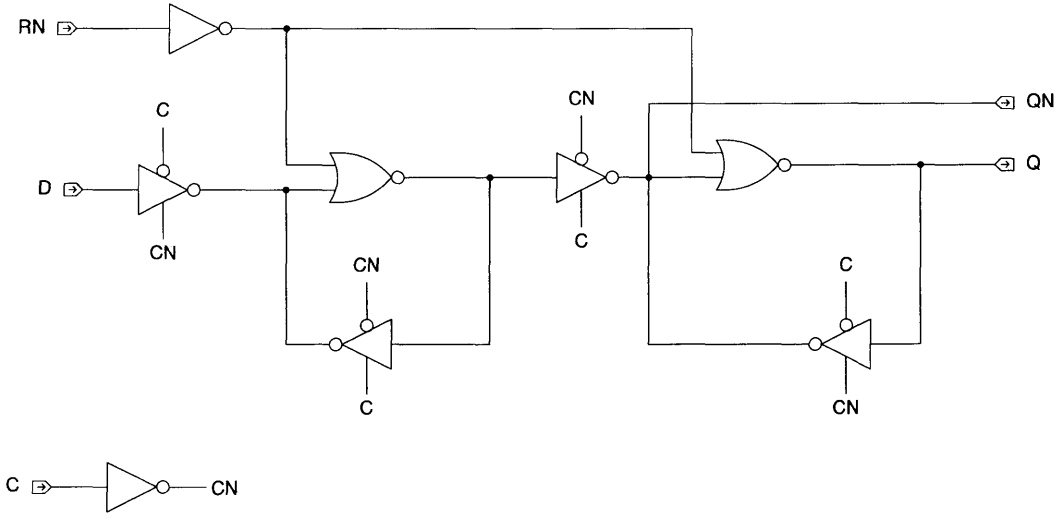
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	2.96 4.67	5.58 5.18	4.52 6.12	6.09 7.57	9.21 10.47
C	QN	t_{PLH} t_{PHL}	2.68 1.29	6.02 5.35	4.37 2.79	6.06 4.29	9.43 7.28
RN	Q	t_{PHL}	2.64	5.18	4.09	5.54	8.44
RN	QN	t_{PLH}	4.94	6.02	6.63	8.31	11.69
Min C Width	High	t_w				7.57	
Min C Width	Low	t_w	4.20				
Min RN Width	Low	t_w				8.31	
Min D Setup		t_{su}	3.43				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	2.89				
Min RN Hold		t_h	2.34				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

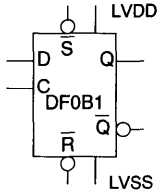


DF0B1

ABX 3.5 micron CMOS Standard Cells

Description:
DF0B1 is a static, master-slave D flip-flop. SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

NC = No Change
IL = Illegal

Pin Loading

	Ci (pF)
D	0.09
C	0.28
SN	0.18
RN	0.19

Equivalent Gates:.....7.1
Bolt Syntax:.....Q QN .DF0B1 C D RN SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.06	nA
†C_{pd}	1.53	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	2.85 5.02	3.88 4.78	3.94 6.35	5.03 7.69	7.20 10.37
C	QN	t_{PLH} t_{PHL}	3.24 1.32	6.15 5.37	4.96 2.82	6.68 4.33	10.13 7.33
RN	Q	t_{PHL}	7.04	4.78	8.38	9.72	12.39
RN	QN	t_{PLH}	5.24	6.15	6.97	8.69	12.14
SN	Q	t_{PLH}	1.00	3.88	2.09	3.17	5.35
SN	QN	t_{PHL}	3.65	5.37	5.15	6.66	9.66
Min C Width	High	t_w				7.69	
Min C Width	Low	t_w	4.80				
Min RN Width	Low	t_w				9.72	

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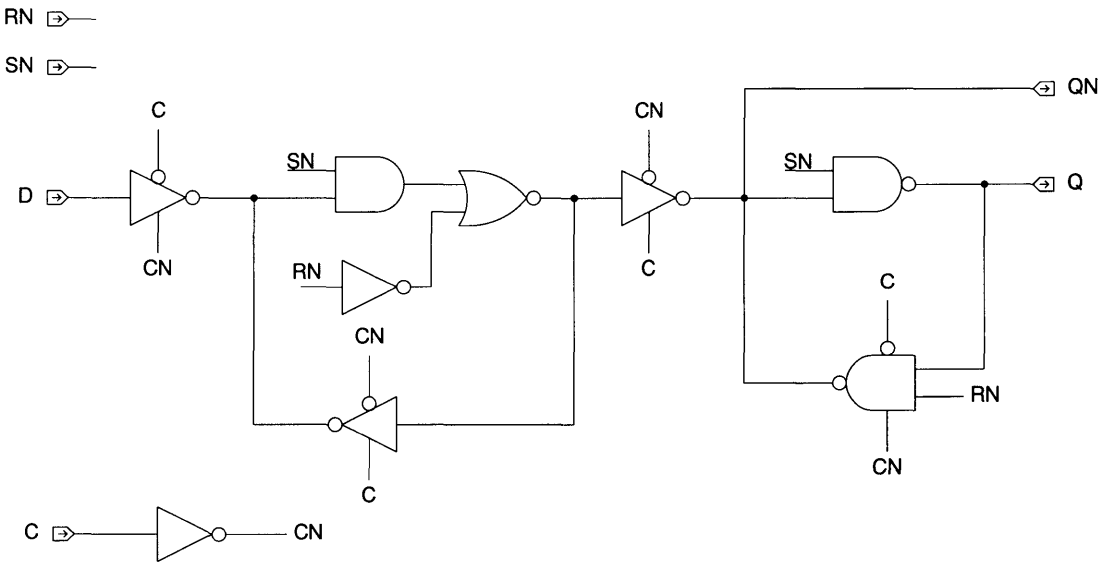
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min SN Width	Low	t_w				6.66	
Min D Setup		t_{su}	4.80				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	2.76				
Min RN Hold		t_h	2.29				
Min SN Setup		t_{su}	2.92				
Min SN Hold		t_h	1.22				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

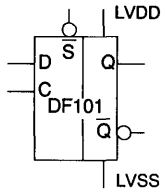


DF101

ABX 3.5 micron CMOS Standard Cells

Description:
DF101 is a static, master-slave D flip-flop. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.09
C	0.25
SN	0.18

Equivalent Gates:.....6.2
Bolt Syntax:.....Q QN .DF101 C D SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.87	nA
†C_{pd}	1.31	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	2.36 3.80	3.69 4.07	3.40 4.94	4.43 6.08	6.50 8.36
C	QN	t_{PLH} t_{PHL}	5.30 3.84	3.50 3.62	6.28 4.85	7.26 5.86	9.22 7.89
SN	Q	t_{PLH}	4.08	3.69	5.12	6.15	8.22
SN	QN	t_{PHL}	1.93	3.62	2.95	3.96	5.99
Min C Width	High	t_w	4.61				
Min C Width	Low	t_w	3.02				
Min SN Width		t_w	3.32				
Min D Setup		t_{su}	2.90				
Min D Hold		t_h	0.00				

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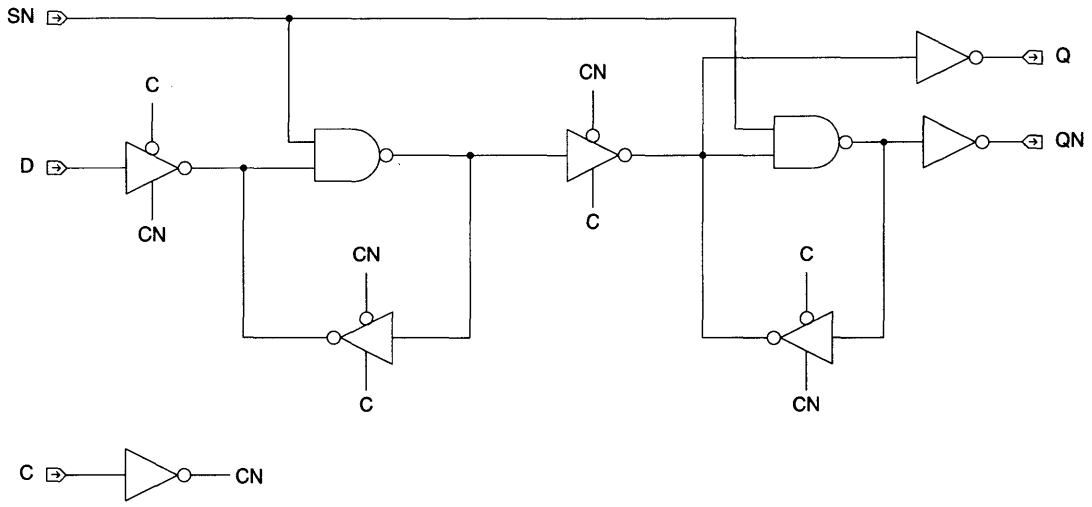
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min SN Setup		t_{su}	1.21				
Min SN Hold		t_h	1.21				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

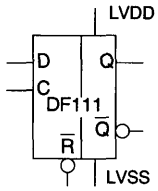


DF111

ABX 3.5 micron CMOS Standard Cells

Description:
DF111 is a static, master-slave D flip-flop. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Ci (pF)
D	0.09
C	0.26
RN	0.09

Equivalent Gates:.....7.2

Bolt Syntax:..... Q QN .DF111 C D RN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.63	nA
†C_{pd}	1.60	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

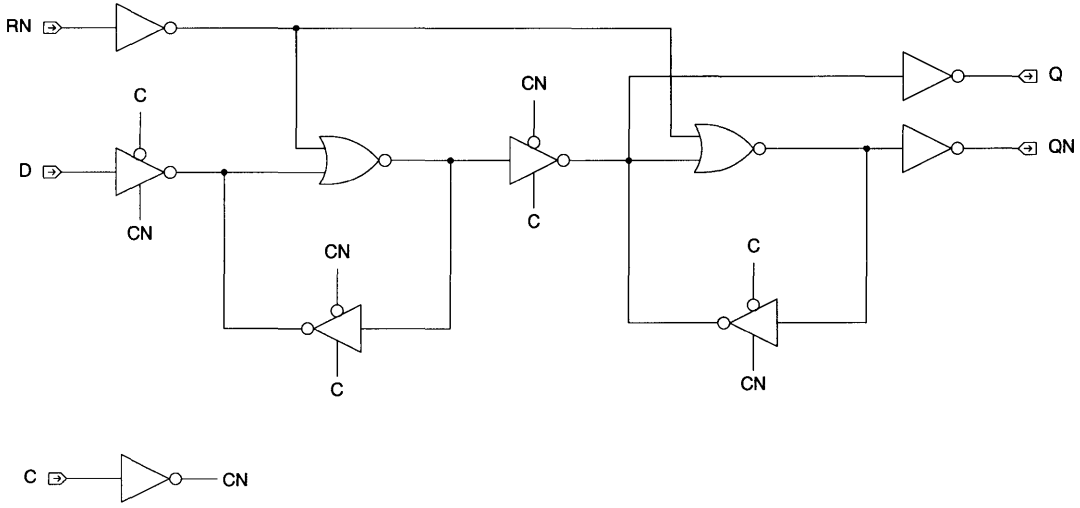
Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	2.42 3.96	3.69 4.10	3.45 5.10	4.48 6.25	6.55 8.55
C	QN	t_{PLH} t_{PHL}	5.86 4.56	3.46 3.95	6.83 5.66	7.80 6.77	9.73 8.98
RN	Q	t_{PHL}	6.26	4.10	7.41	8.56	10.85
RN	QN	t_{PLH}	3.78	3.46	4.75	5.72	7.65
Min C Width	High	t_w	5.14				
Min C Width	Low	t_w	3.23				
Min RN Width		t_w	7.49				
Min D Setup		t_{su}	3.10				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	2.74				
Min RN Hold		t_h	4.63				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

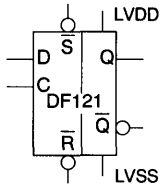


DF121

ABX 3.5 micron CMOS Standard Cells

Description:
DF121 is a static, master-slave D flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL=Illegal NC=No Change

Pin Loading

	Ci (pF)
D	0.09
C	0.27
SN	0.20
RN	0.18

Equivalent Gates:.....8.3
Bolt Syntax:.....Q QN .DF121 C D RN SN LVDD LVSS;
Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.00	nA
†C_{pd}	1.70	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	2.46 3.90	3.72 4.11	3.51 5.05	4.55 6.20	6.63 8.50
C	QN	t_{PLH} t_{PHL}	5.47 4.02	3.54 3.64	6.46 5.04	7.46 6.05	9.44 8.09
SN	Q	t_{PLH}	4.97	3.72	6.01	7.06	9.14
SN	QN	t_{PHL}	1.98	3.64	2.99	4.01	6.05
RN	Q	t_{PHL}	6.43	4.11	7.58	8.74	11.04
RN	QN	t_{PLH}	8.02	3.54	9.01	10.00	11.99
Min C Width	High	t_w	4.75				
Min C Width	Low	t_w	4.39				
Min RN Width	Low	t_w	8.32				
Min SN Width	Low	t_w	4.04				

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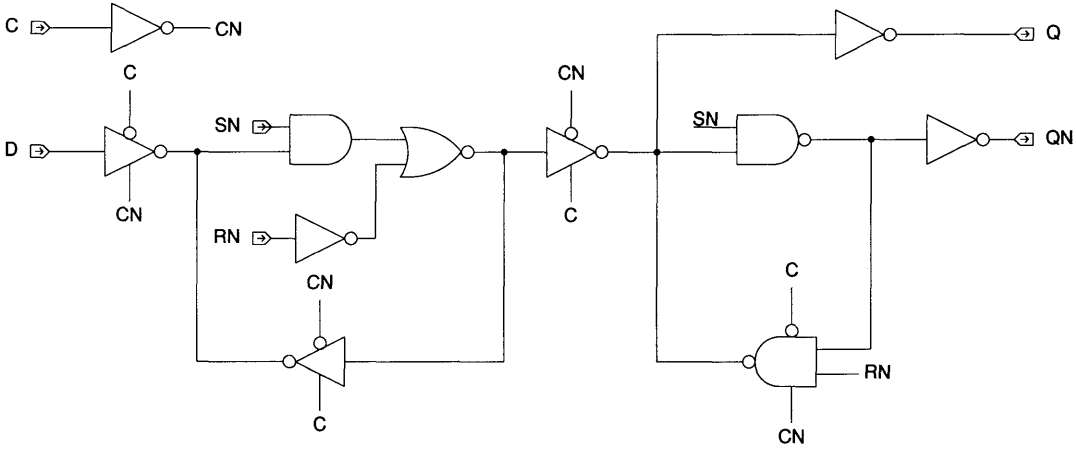
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min D Setup		t_{su}	4.39				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	2.52				
Min RN Hold		t_h	4.84				
Min SN Setup		t_{su}	2.57				
Min SN Hold		t_h	1.79				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



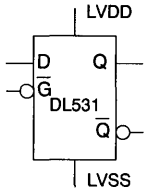
DL531

AMI SEMICONDUCTORS

ABX 3.5 micron CMOS Standard Cells

Description:
DL531 is a single-phase, unbuffered D latch with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

GN	D	Q	QN
L	L	L	H
L	H	H	L
H	X	NC	NC

NC=No Change

Pin Loading

	Ci (pF)
D	0.10
GN	0.18

Equivalent Gates:.....2.1
Bolt Syntax:.....Q QN .DL531 D GN LVDD LVSS;
Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.71	nA
†C_{pd}	0.51	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

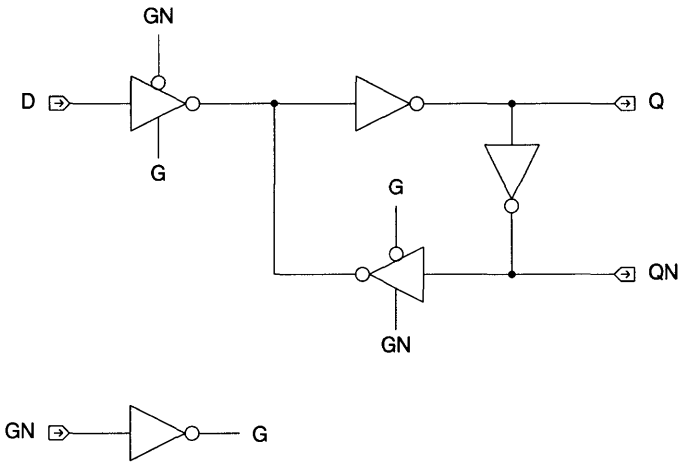
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
D	Q	t_{PLH} t_{PHL}	2.68 2.87	3.63 4.06	3.48 3.76	4.35 4.74	6.09 6.68
D	QN	t_{PLH} t_{PHL}	1.53 1.53	6.13 5.36	2.88 2.71	4.35 3.99	7.30 6.56
GN	Q	t_{PLH} t_{PHL}	3.15 2.53	3.63 4.06	3.95 3.43	4.82 4.40	6.56 6.35
GN	QN	t_{PLH} t_{PHL}	1.19 2.00	6.13 5.36	2.54 3.18	4.01 4.46	6.96 7.03
Min GN Width	Low	t_w				4.82	
Min D Setup		t_{su}				4.74	
Min D Hold		t_h	0.00				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

1.5/3.5 micron Mixed Signal

Logic Schematic

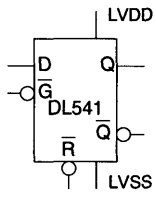


DL541

ABX 3.5 micron CMOS Standard Cells

Description:
DL541 is a single-phase, unbuffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC=No Change

Pin Loading

	Ci (pF)
D	0.09
GN	0.18
RN	0.09

Equivalent Gates:.....3.4
Bolt Syntax:.....Q QN .DL541 D GN RN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.71	nA
†C_{pd}	0.75	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
D	Q	t_{PLH} t_{PHL}	2.92 3.19	5.50 4.84	4.13 4.26	5.45 5.42	8.09 7.75
D	QN	t_{PLH} t_{PHL}	3.90 3.83	3.61 4.27	4.70 4.77	5.56 5.79	7.29 7.84
GN	Q	t_{PLH} t_{PHL}	2.87 2.85	5.50 4.84	4.07 3.92	5.39 5.08	8.03 7.40
GN	QN	t_{PLH} t_{PHL}	3.55 3.77	3.61 4.27	4.35 4.71	5.21 5.74	6.94 7.79
RN	Q	t_{PHL}	2.28	4.84	3.34	4.50	6.83
RN	QN	t_{PLH}	3.03	3.61	3.83	4.69	6.42
Min GN Width	Low	t_w				5.45	
Min RN Width	Low	t_w				7.47	
Min D Setup		t_{su}				5.45	

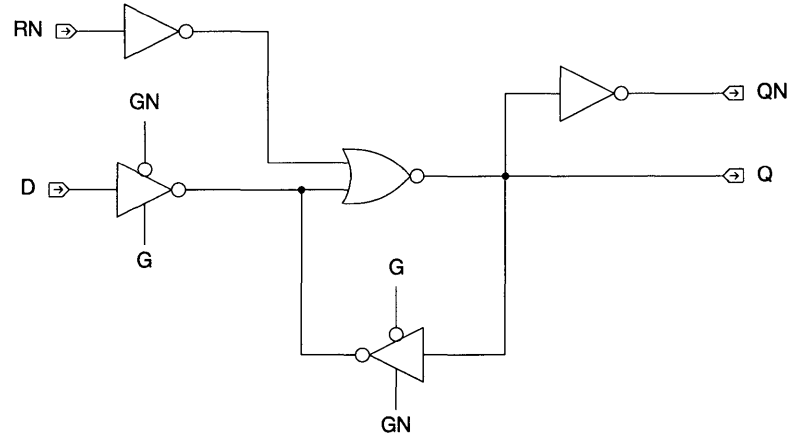
(continued on next page)

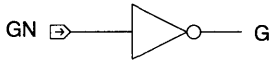
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	2.30				
Min RN Hold		t_h	4.48				

For Q Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{dr}(QN) + (k_{tdr}(QN) C_L(QN)) + (k_{tdf}(Q) C_L(Q))]$

Logic Schematic





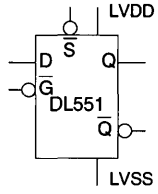
DL551

AMI SEMICONDUCTORS

ABX 3.5 micron CMOS Standard Cells

Description:
DL551 is a single-phase, unbuffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC=No Change

Pin Loading

	Ci (pF)
D	0.09
GN	0.17
SN	0.08

Equivalent Gates:.....2.9
Bolt Syntax:.....Q QN .DL551 D GN SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.51	nA
†C_{pd}	0.57	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
D	Q	t_{PLH} t_{PHL}	2.71 2.71	3.67 4.41	3.52 3.68	4.40 4.74	6.16 6.86
D	QN	t_{PLH} t_{PHL}	3.40 3.48	3.71 3.84	4.21 4.32	5.10 5.25	6.88 7.09
GN	Q	t_{PLH} t_{PHL}	2.67 2.37	3.67 4.41	3.48 3.35	4.36 4.41	6.12 6.52
GN	QN	t_{PLH} t_{PHL}	3.07 3.44	3.71 3.84	3.88 4.28	4.77 5.20	6.55 7.05
SN	Q	t_{PLH}	0.96	3.67	1.76	2.64	4.40
SN	QN	t_{PHL}	1.69	3.84	2.54	3.46	5.30
Min GN Width	Low	t_w				4.74	
Min SN Width	Low	t_w				2.70	
Min D Setup		t_{su}				4.74	

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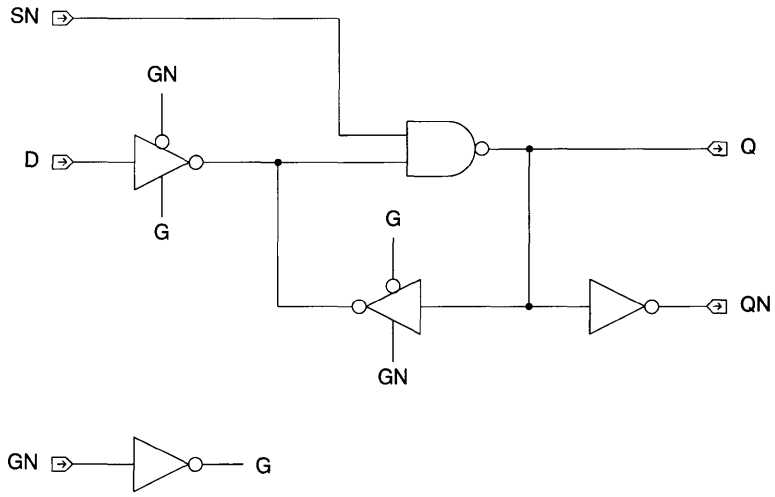
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	1.16				
Min SN Hold		t_h	1.80				

For Q Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{dr}(QN) + (k_{tdr}(QN) C_L(QN)) + (k_{tdf}(Q) C_L(Q))]$
$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{df}(QN) + (k_{tdf}(QN) C_L(QN)) + (k_{tdr}(Q) C_L(Q))]$

Logic Schematic

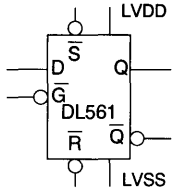


DL561

ABX 3.5 micron CMOS Standard Cells

Description:
DL561 is a single-phase, unbuffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

NC=No Change IL = Illegal

Pin Loading

	Ci (pF)
D	0.10
GN	0.18
SN	0.09
RN	0.11

Equivalent Gates:.....3.7
Bolt Syntax:.....Q QN .DL561 D GN RN SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.22	nA
†C_{pd}	0.71	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
D	Q	t_{PLH} t_{PHL}	3.21 3.25	3.80 4.52	4.04 4.24	4.96 5.33	6.78 7.50
D	QN	t_{PLH} t_{PHL}	5.81 5.54	4.46 4.55	6.79 6.55	7.86 7.64	10.00 9.82
GN	Q	t_{PLH} t_{PHL}	3.11 2.84	3.80 4.52	3.94 3.84	4.85 4.92	6.68 7.09
GN	QN	t_{PLH} t_{PHL}	3.48 3.81	4.46 4.55	4.46 4.81	5.53 5.90	7.67 8.09
SN	Q	t_{PLH}	1.11	3.80	1.95	2.86	4.68
SN	QN	t_{PHL}	1.82	4.55	2.82	3.91	6.10
RN	Q	t_{PHL}	2.39	4.52	3.39	4.47	6.64
RN	QN	t_{PLH}	3.00	4.46	3.99	5.06	7.20
Min GN Width	Low	t_w				5.33	

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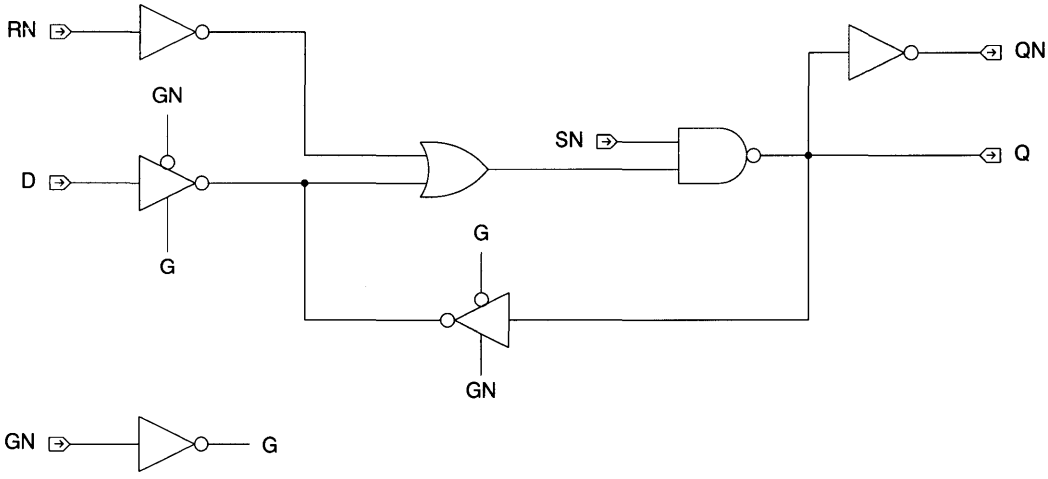
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min RN Width	Low	t_w				4.47	
Min SN Width	Low	t_w				3.63	
Min D Setup		t_{su}				5.33	
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	1.23				
Min SN Hold		t_h	2.36				
Min RN Setup		t_{su}	3.46				
Min RN Hold		t_h	1.13				

For Q Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

For QN Delays: $t_{plh}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{dr}(QN) + (k_{tdr}(QN) C_L(QN)) + (k_{tdf}(Q) C_L(Q))]$
$t_{phl}(C_{L(QN)}, C_{L(Q)}) = K_P K_V K_T[t_{df}(QN) + (k_{tdf}(QN) C_L(QN)) + (k_{tdr}(Q) C_L(Q))]$

Logic Schematic

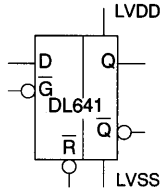


DL641

ABX 3.5 micron CMOS Standard Cells

Description:
DL641 is a single-phase, buffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC=No Change

Pin Loading

	Ci (pF)
D	0.09
GN	0.17
RN	0.09

Equivalent Gates:.....4.5
Bolt Syntax:.....Q QN .DL641 D GN RN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.08	nA
†C_{pd}	1.05	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
D	Q	t_{PLH} t_{PHL}	4.92 4.92	3.34 3.53	5.66 5.70	6.46 6.55	8.06 8.24
D	QN	t_{PLH} t_{PHL}	4.06 4.17	3.63 4.20	4.86 5.09	5.73 6.10	7.47 8.12
GN	Q	t_{PLH} t_{PHL}	4.84 4.58	3.34 3.53	5.58 5.36	6.38 6.21	7.98 7.90
GN	QN	t_{PLH} t_{PHL}	3.72 4.09	3.63 4.20	4.51 5.02	5.39 6.03	7.13 8.04
RN	Q	t_{PHL}	4.21	3.53	4.99	5.83	7.53
RN	QN	t_{PLH}	3.35	3.63	4.14	5.01	6.75
Min GN Width	High	t_w	1.65				
Min GN Width	Low	t_h	3.39				
Min RN Width	Low	t_w	7.36				

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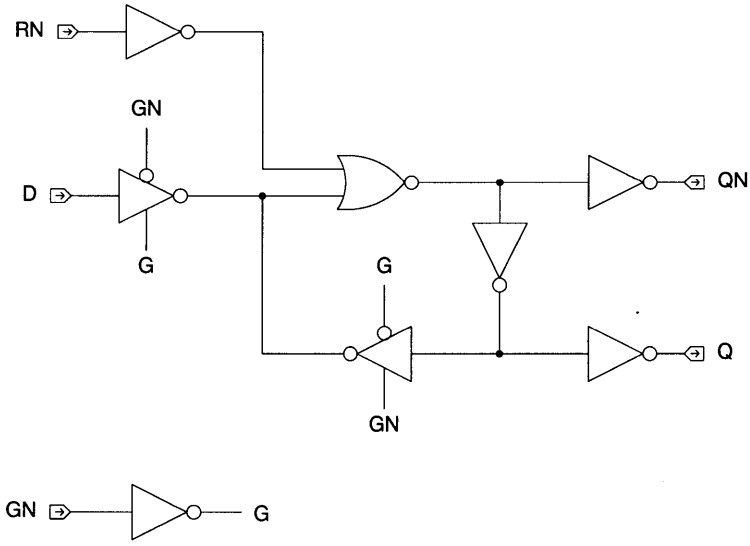
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min D Setup		t_{su}	3.39				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	2.69				
Min RN Hold		t_h	4.07				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

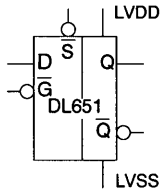


DL651

ABX 3.5 micron CMOS Standard Cells

Description:
DL651 is a single-phase, buffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC=No Change

Pin Loading

	Ci (pF)
D	0.09
GN	0.17
SN	0.09

Equivalent Gates:.....3.9
Bolt Syntax:.....Q QN .DL651 D GN SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.87	nA
†C_{pd}	0.86	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
D	Q	t_{PLH} t_{PHL}	4.45 4.53	3.34 3.54	5.18 5.31	5.98 6.16	7.58 7.85
D	QN	t_{PLH} t_{PHL}	3.69 3.78	3.73 3.80	4.51 4.62	5.40 5.53	7.19 7.36
GN	Q	t_{PLH} t_{PHL}	4.38 4.20	3.34 3.54	5.11 4.97	5.91 5.82	7.51 7.52
GN	QN	t_{PLH} t_{PHL}	3.35 3.71	3.73 3.80	4.17 4.55	5.07 5.46	6.85 7.29
SN	Q	t_{PLH}	2.63	3.34	3.37	4.17	5.77
SN	QN	t_{PHL}	1.97	3.80	2.81	3.72	5.55
Min GN Width	High	t_w	1.58				
Min GN Width	Low	t_h	3.04				
Min SN Width	Low	t_w	3.03				

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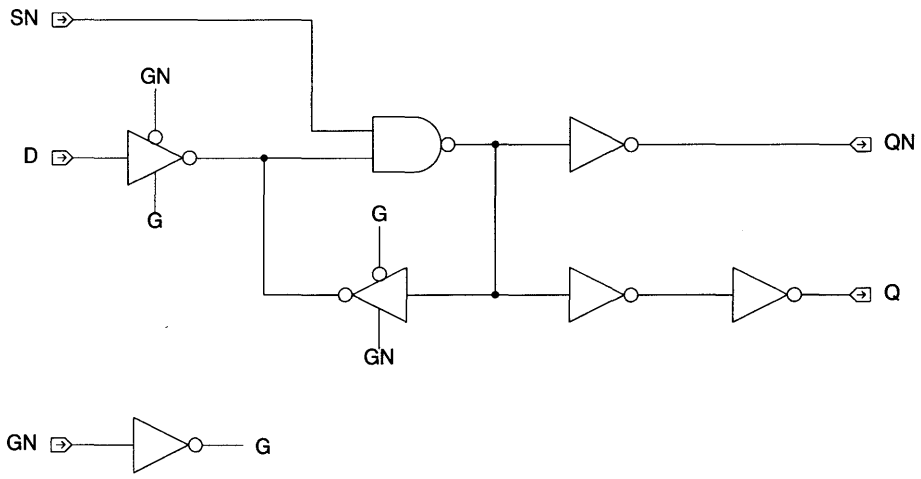
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min D Setup		t_{su}	3.04				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	1.46				
Min SN Hold		t_h	1.83				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

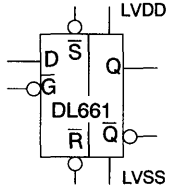


DL661

ABX 3.5 micron CMOS Standard Cells

Description:
DL661 is a single-phase, buffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL=Illegal NC=No Change

Pin Loading

	Ci (pF)
D	0.11
GN	0.17
SN	0.10
RN	0.10

Equivalent Gates:.....4.4
Bolt Syntax:.....Q QN .DL661 D GN RN SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.56	nA
†C_{pd}	1.00	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
D	Q	t_{PLH} t_{PHL}	4.68 5.13	3.34 3.54	5.41 5.91	6.21 6.76	7.81 8.45
D	QN	t_{PLH} t_{PHL}	4.31 4.03	3.74 3.81	5.13 4.87	6.03 5.79	7.82 7.62
GN	Q	t_{PLH} t_{PHL}	4.63 4.66	3.34 3.54	5.37 5.44	6.17 6.29	7.77 7.99
GN	QN	t_{PLH} t_{PHL}	3.84 3.99	3.74 3.81	4.66 4.83	5.56 5.75	7.36 7.58
SN	Q	t_{PLH}	2.75	3.34	3.48	4.28	5.88
SN	QN	t_{PHL}	2.11	3.81	2.95	3.86	5.69
RN	Q	t_{PHL}	4.52	3.54	5.29	6.14	7.84
RN	QN	t_{PLH}	3.69	3.74	4.52	5.42	7.21
Min GN Width	High	t_w	1.69				

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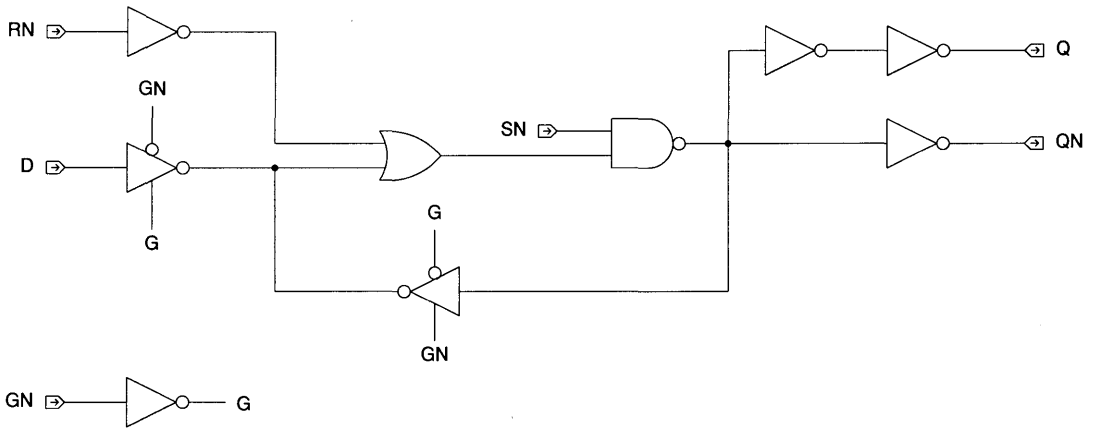
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min GN Width	Low	t_w	3.65				
Min RN Width	Low	t_w	2.70				
Min SN Width	Low	t_w	3.98				
Min D Setup		t_{su}	3.65				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	1.46				
Min SN Hold		t_h	2.33				
Min RN Setup		t_{su}	3.50				
Min RN Hold		t_h	1.18				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

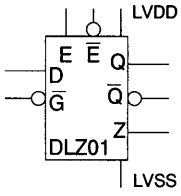


DLZ01

ABX 3.5 micron CMOS Standard Cells

Description:
DLZ01 is a single-phase, unbuffered D latch with active low gate transparency and with a dual-enable tri-state output.

Logic Symbol



Truth Table

D	GN	E	EN	Q	QN	Z
L	L	H	X	L	H	L
H	L	X	L	H	L	H
L	L	L	X	L	H	Z
H	L	X	H	H	L	Z
X	H	H	L	NC	NC	NC
X	H	L	H	NC	NC	Z

Z = High Impedance NC=No Change

Pin Loading

	Ci (pF)
D	0.10
GN	0.19
E	0.03
EN	0.06
Z	0.06

Equivalent Gates:.....2.9
Bolt Syntax:.....Q QN Z .DLZ01 D E EN GN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.40	nA
†C_{pd}	0.70	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
D	Q	t_{PLH} t_{PHL}	3.27 3.53	3.84 4.28	4.11 4.47	5.04 5.50	6.88 7.55
D	QN	t_{PLH} t_{PHL}	2.06 1.97	6.13 5.36	3.40 3.15	4.88 4.43	7.82 7.00
D	Z	t_{PLH} t_{PHL}	3.19 3.45	6.15 5.66	4.54 4.69	6.02 6.05	8.97 8.77
GN	Q	t_{PLH} t_{PHL}	3.78 3.19	3.84 4.28	4.62 4.13	5.55 5.16	7.39 7.22
GN	QN	t_{PLH} t_{PHL}	1.72 2.48	6.13 5.36	3.06 3.66	4.54 4.94	7.48 7.51
GN	Z	t_{PLH} t_{PHL}	3.70 3.11	6.15 5.66	5.05 4.36	6.52 5.71	9.47 8.43
E	Z	t_{PLZ} t_{PZL}	0.60 0.84				

(continued on next page)

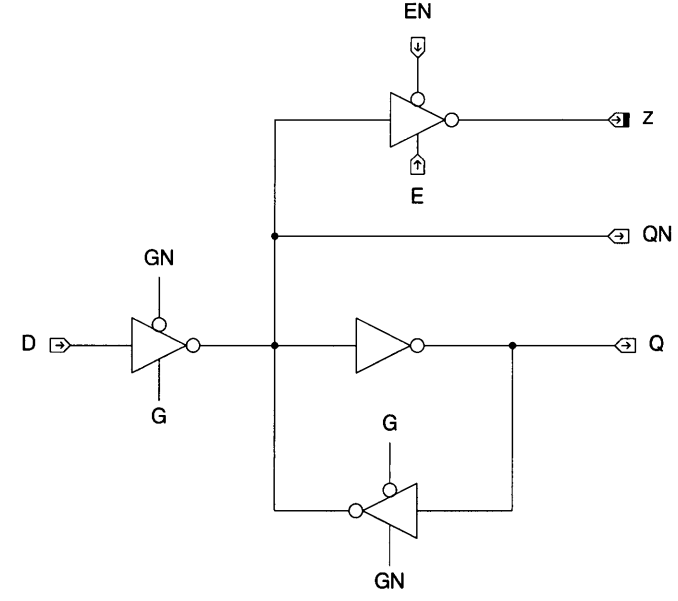
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
EN	Z	t_{PHZ} t_{PZH}	0.82 0.69				
Min GN Width	Low	t_w				5.55	
Min D Setup		t_{su}				5.50	
Min D Hold		t_h	0.00				

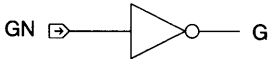
For Q Delays:
$t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

For QN Delays:
$t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

For Z Delays:
$t_{plh}(C_{L(Z)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Z) + (K_{tdr}(Z) * C_L(Z)) + (K_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Z)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Z) + (K_{tdf}(Z) * C_L(Z)) + (K_{tdr}(QN) * C_L(QN))]$

Logic Schematic



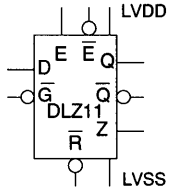


DLZ11

ABX 3.5 micron CMOS Standard Cells

Description:
DLZ11 is a single-phase, unbuffered D latch with active low gate transparency and with a dual-enable tri-state output. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	E	EN	Q	QN	Z
H	L	L	H	X	L	H	L
H	H	L	X	L	H	L	H
H	L	L	L	X	L	H	Z
H	H	L	X	H	H	L	Z
H	X	H	H	L	NC	NC	NC
H	X	H	L	H	NC	NC	Z
L	X	X	H	L	L	H	L
L	X	X	L	H	L	H	Z

Z = High Impedance NC=No Change

Pin Loading

	Ci (pF)
D	0.09
GN	0.20
RN	0.09
E	0.04
EN	0.07
Z	0.06

Equivalent Gates:.....3.6
Bolt Syntax:.....Q QN Z .DLZ11 D E EN GN RN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.09	nA
†C_{pd}	0.81	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
D	Q	t_{PLH} t_{PHL}	4.47 3.83	4.27 4.34	5.41 4.78	6.44 5.82	8.49 7.91
D	QN	t_{PLH} t_{PHL}	2.25 2.87	6.13 7.26	3.60 4.46	5.07 6.21	8.02 9.69
GN	Q	t_{PLH} t_{PHL}	4.82 3.48	4.27 4.34	5.76 4.44	6.79 5.48	8.84 7.56
GN	QN	t_{PLH} t_{PHL}	1.90 3.21	6.13 7.26	3.25 4.81	4.72 6.55	7.67 10.04
RN	Q	t_{PHL}	2.64	4.34	3.60	4.64	6.72
RN	QN	t_{PLH}	1.29	6.13	2.64	4.11	7.05
RN	Z	t_{PHL} t_{PLH}	2.56 4.58	5.70 6.37	3.82 5.98	5.18 7.51	7.92 10.57

(continued on next page)

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
D	Z	t_{PLH} t_{PHL}	4.28 3.69	6.37 5.70	5.68 4.94	7.21 6.31	10.27 9.05
GN	Z	t_{PLH} t_{PHL}	4.63 3.34	6.37 5.70	6.03 4.59	7.56 5.96	10.62 8.70
E	Z	t_{PLZ} t_{PZL}	0.74 0.84				
EN	Z	t_{PHZ} t_{PZH}	0.82 0.50				
Min GN Width	Low	t_w				6.79	
Min RN Width	Low	t_w				4.64	
Min D Setup		t_{su}				6.44	
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	4.73				
Min RN Hold		t_h	1.38				

For Q Delays:

$$t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$$
$$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$$

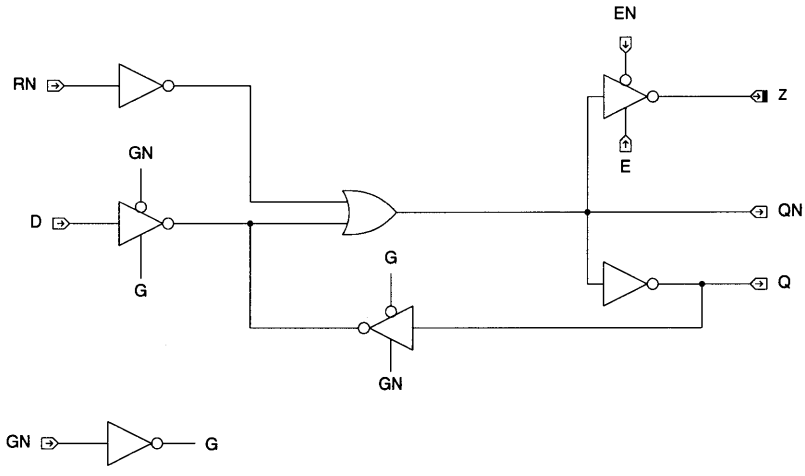
For QN Delays:

$$t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$$

For Z Delays:

$$t_{plh}(C_{L(Z)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Z) + (K_{tdr}(Z) * C_L(Z)) + (K_{tdf}(QN) * C_L(QN))]$$
$$t_{phl}(C_{L(Z)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Z) + (K_{tdf}(Z) * C_L(Z)) + (K_{tdr}(QN) * C_L(QN))]$$

Logic Schematic



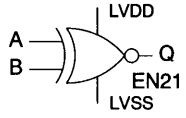
EN21

AMI SEMICONDUCTORS

ABX 3.5 micron CMOS Standard Cells

Description:
EN21 is a 2-input gate which performs the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

Pin Loading

	Ci (pF)
A	0.18
B	0.18

Equivalent Gates:.....2.0
Bolt Syntax:.....Q .EN21 A B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.54	nA
†C_{pd}	0.33	pF

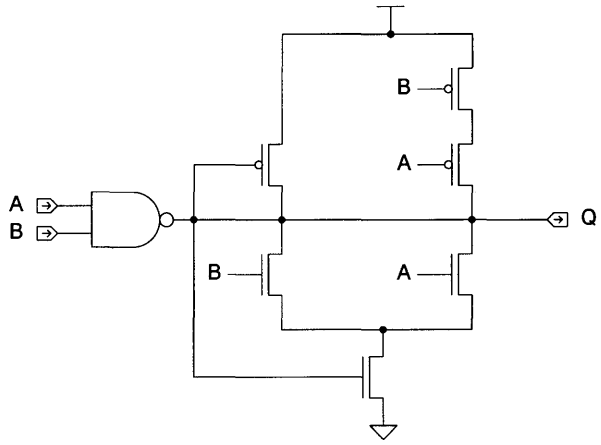
Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

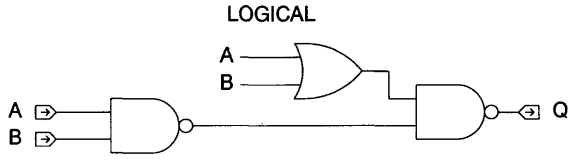
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	0.97	6.61	2.43	4.01	7.19
		t_{PHL}	1.72	4.40	2.68	3.74	5.85

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



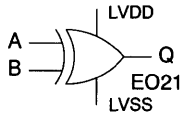


EO21

ABX 3.5 micron CMOS Standard Cells

Description:
EO21 is a 2-input gate which performs the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

Pin Loading

	Ci (pF)
A	0.17
B	0.18

Equivalent Gates:.....1.9
Bolt Syntax:.....Q .EO21 A B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.56	nA
†C_{pd}	0.36	pF

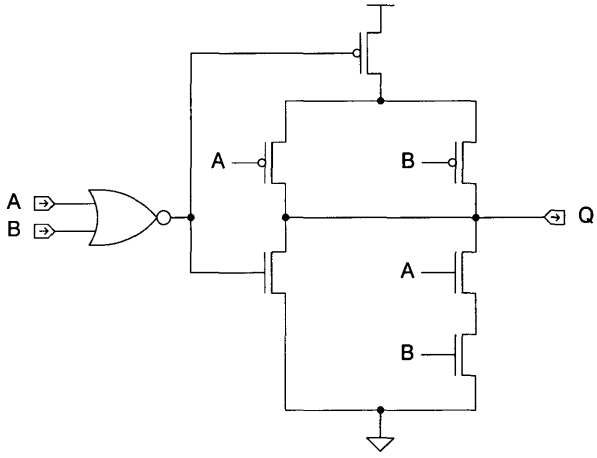
Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

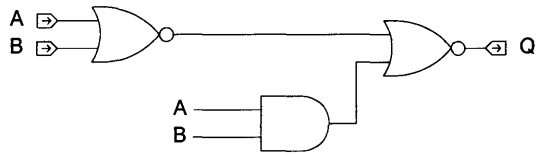
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	2.44	5.46	3.65	4.96	7.58
		t_{PHL}	2.96	4.59	3.97	5.07	7.28

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



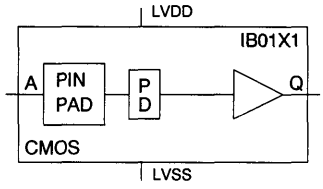
LOGICAL



ABX 3.5 micron CMOS Standard Cells

Description:
IB01X1 is a non-inverting, CMOS-level input buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	5.46

Bolt Syntax: .....Q .IB01X1 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.80	nA
†C_{pd}	0.30	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

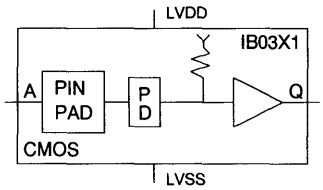
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	1.62	3.27	2.34	3.12	4.69
		t_{PHL}	1.76	3.38	2.51	3.32	4.94

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IB03X1 is a non-inverting, CMOS-level input buffer pad with pull-up.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	5.52

Bolt Syntax: .....Q .IB03X1 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.41	nA
†C_{pd}	0.28	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

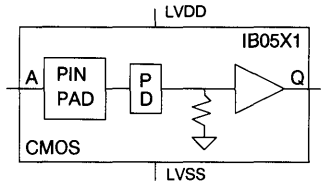
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	1.58	3.27	2.30	3.12	4.65
		t_{PHL}	1.72	3.39	2.46	3.27	4.90

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ABX 3.5 micron CMOS Standard Cells

Description:
IB05X1 is a non-inverting, CMOS-level input buffer pad with pull-down.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	5.49

Bolt Syntax: .....Q .IB05X1 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.09	nA
†C_{pd}	0.29	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

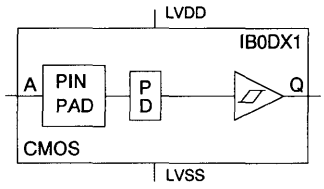
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	1.61	3.27	2.33	3.12	4.69
		t_{PHL}	1.76	3.39	2.50	3.31	4.94

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IB0DX1 is a non-inverting, CMOS-level Schmitt trigger input buffer pad with voltage hysteresis.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	5.51

Bolt Syntax: .....Q .IB0DX1 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.16	nA
†C_{pd}	0.62	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

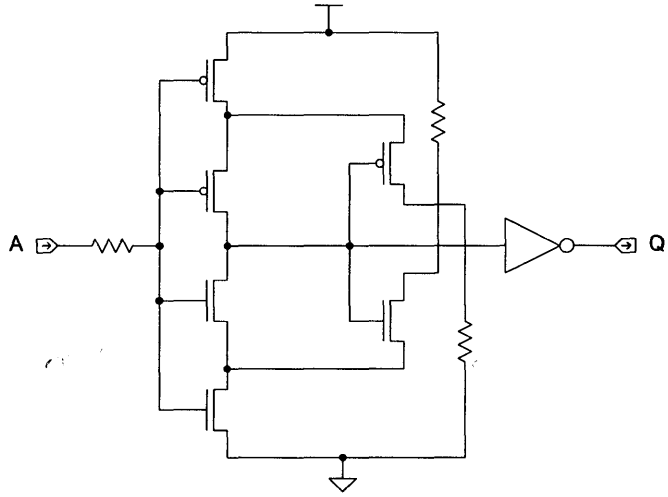
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	4.01	3.38	4.75	5.56	7.19
		t_{PHL}	4.69	3.99	5.57	6.52	8.44

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

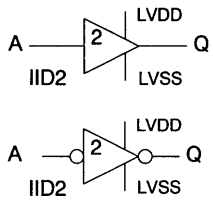
ABX 3.5 micron CMOS Standard Cells

Logic Schematic



Description:
IID2 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.16

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .IID2 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.68	nA
†C_{pd}	0.30	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

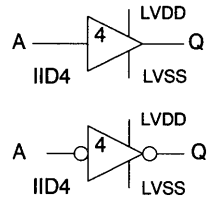
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	0.98	1.63	1.34	1.73	2.51
		t_{PHL}	1.03	1.67	1.40	1.80	2.60

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ABX 3.5 micron CMOS Standard Cells

Description:
IID4 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.16

Equivalent Gates:.....2.3
Bolt Syntax:.....Q .IID4 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.01	nA
†C_{pd}	0.57	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

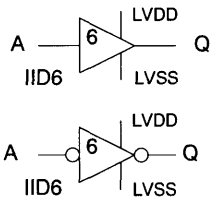
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	1.35	0.92	1.55	1.77	2.22
		t_{PHL}	1.40	0.97	1.61	1.84	2.31

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IID6 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.17

Equivalent Gates:.....2.7
Bolt Syntax:.....Q .IID6 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.31	nA
†C_{pd}	0.84	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	1.68	0.69	1.83	2.00	2.33
		t_{PHL}	1.74	0.75	1.90	2.08	2.44

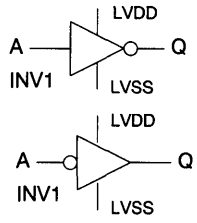
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

INV1

ABX 3.5 micron CMOS Standard Cells

Description:
INV1 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.09

Equivalent Gates:.....0.7
Bolt Syntax:.....Q .INV1 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.69	nA
†C_{pd}	0.06	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

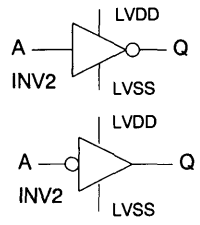
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	0.45	3.35	1.19	1.99	3.60
		t_{PHL}	0.58	3.57	1.36	2.22	3.93

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
INV2 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.17

Equivalent Gates:.....1.0
Bolt Syntax:.....Q .INV2 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.36	nA
†C_{pd}	0.14	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	0.44	1.67	0.80	1.21	2.01
		t_{PHL}	0.52	1.73	0.90	1.32	2.15

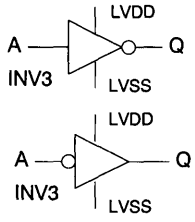
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

INV3

ABX 3.5 micron CMOS Standard Cells

Description:
INV3 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.25

Equivalent Gates:..... 1.3
Bolt Syntax:..... Q .INV3 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.02	nA
†C_{pd}	0.15	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

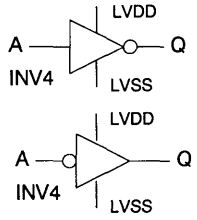
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	0.39	1.14	0.64	0.91	1.46
		t_{PHL}	0.44	1.21	0.71	1.00	1.58

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
INV4 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.33

Equivalent Gates:.....1.4
Bolt Syntax:.....Q .INV4 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.66	nA
†C_{pd}	0.19	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	0.36	0.89	0.56	0.77	1.20
		t_{PHL}	0.41	0.94	0.62	0.84	1.30

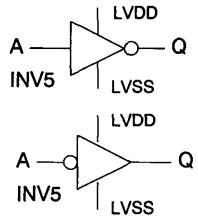
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

INV5

ABX 3.5 micron CMOS Standard Cells

Description:
INV5 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.41

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .INV5 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.32	nA
†C_{pd}	0.21	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

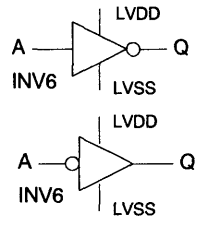
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	0.34	0.74	0.50	0.68	1.04
		t_{PHL}	0.39	0.79	0.56	0.75	1.13

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
INV6 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Ci (pF)
A	0.48

Equivalent Gates:.....1.8
Bolt Syntax:.....Q .INV6 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.97	nA
†C_{pd}	0.25	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	0.33	0.64	0.47	0.62	0.93
		t_{PHL}	0.38	0.68	0.53	0.69	1.01

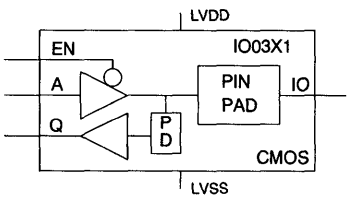
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IO03X1

ABX 3.5 micron CMOS Standard Cells

Description:
IO03X1 is a 1mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.20
EN	0.20
IO	7.94

Bolt Syntax: .....IO Q .IO03X1 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	21.50	nA
†C_{pd}	9.28	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.48	3.27	2.20	2.98	4.55
		t_{PHL}	1.61	3.39	2.35	3.17	4.79

Output Delay Characteristics:

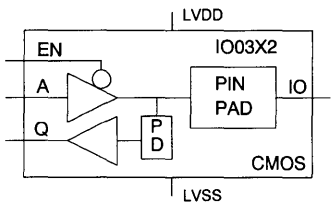
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	2.13	0.51	14.77	27.41	40.05	52.69
		t_{PHL}	3.17	0.19	7.99	12.81	17.63	22.45
EN	IO	t_{HZ}	5.56					
		t_{LZ}	5.45					
		t_{ZH}	2.59	0.51	15.23	27.87	40.51	53.15
		t_{ZL}	3.25	0.19	8.07	12.90	17.72	22.54

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO03X2 is a 2mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.20
EN	0.21
IO	7.93

Bolt Syntax: .....IO Q .IO03X2 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	21.50	nA
†C_{pd}	9.83	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.49	3.27	2.21	2.99	4.56
		t_{PHL}	1.63	3.38	2.37	3.18	4.80

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

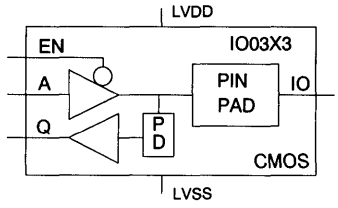
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	4.95	0.25	11.10	17.26	23.41	29.56
		t_{PHL}	4.85	0.11	7.48	10.11	12.74	15.37
EN	IO	t_{HZ}	8.25					
		t_{LZ}	8.57					
		t_{ZH}	4.88	0.25	11.03	17.19	23.34	29.50
		t_{ZL}	4.84	0.11	7.47	10.10	12.73	15.36

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ABX 3.5 micron CMOS Standard Cells

Description:
IO03X3 is a 4mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.33
EN	0.27
IO	9.76

Bolt Syntax: .....IO Q .IO03X3 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	32.36	nA
†C_{pd}	13.12	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.58	3.27	2.30	3.09	4.66
		t_{PHL}	1.72	3.39	2.46	3.28	4.90

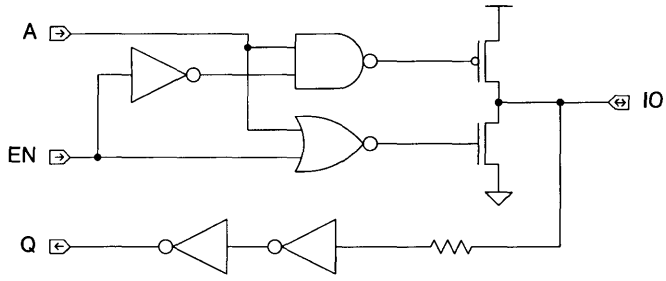
Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	4.52	0.12	7.55	10.59	13.63	16.67
		t_{PHL}	4.05	0.06	5.53	7.01	8.49	9.98
EN	IO	t_{HZ}	8.11					
		t_{LZ}	7.14					
		t_{ZH}	4.80	0.12	7.84	10.88	13.92	16.96
		t_{ZL}	3.95	0.06	5.43	6.91	8.40	9.88

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

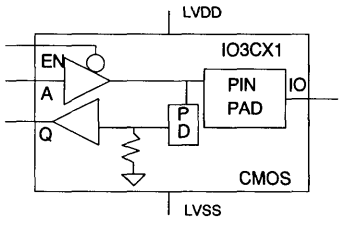


IO3CX1

ABX 3.5 micron CMOS Standard Cells

Description:
IO3CX1 is a 1mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.20
EN	0.21
IO	8.00

Bolt Syntax: .....IO Q .IO3CX1 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	22.46	nA
†C_{pd}	9.39	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.57	3.27	2.29	3.07	4.64
		t_{PHL}	1.71	3.38	2.45	3.26	4.88

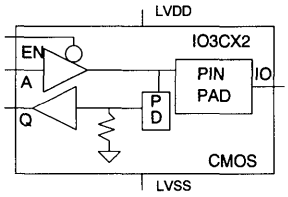
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	2.14	0.51	14.85	27.56	40.26	52.97
		t_{PHL}	3.22	0.19	8.00	12.78	17.56	22.34
EN	IO	t_{HZ}	5.54					
		t_{LZ}	5.52					
		t_{ZH}	2.59	0.51	15.30	28.01	40.71	53.42
		t_{ZL}	3.33	0.19	8.11	12.89	17.67	22.45

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO3CX2 is a 2mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.21
EN	0.21
IO	8.00

Bolt Syntax: .....IO Q .IO3CX2 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	22.45	nA
†C_{pd}	9.96	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.62	3.27	2.34	3.12	4.69
		t_{PHL}	1.76	3.37	2.50	3.31	4.93

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

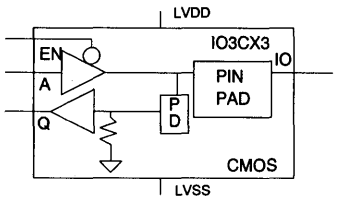
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	4.99	0.25	11.15	17.32	23.48	29.65
		t_{PHL}	4.89	0.11	7.51	10.14	12.77	15.40
EN	IO	t_{HZ}	8.25					
		t_{LZ}	8.64					
		t_{ZH}	4.91	0.25	11.08	17.24	23.41	29.57
		t_{ZL}	4.88	0.11	7.51	10.13	12.76	15.39

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ABX 3.5 micron CMOS Standard Cells

Description:
IO3CX3 is a 4mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.33
EN	0.26
IO	9.83

Bolt Syntax: .....IO Q .IO3CX3 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	33.24	nA
†C_{pd}	13.29	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

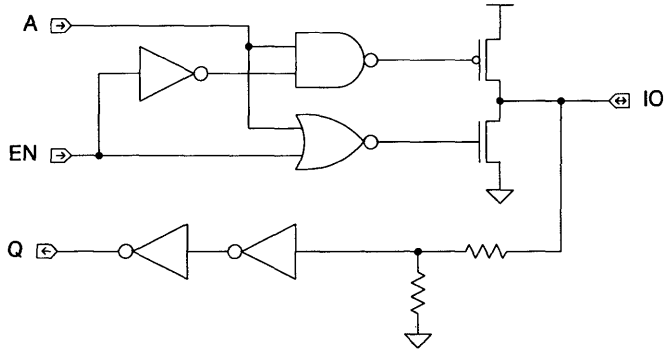
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.59	3.27	2.30	3.09	4.66
		t_{PHL}	1.72	3.38	2.47	3.28	4.90

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	4.68	0.12	7.74	10.80	13.86	16.92
		t_{PHL}	4.08	0.06	5.55	7.02	8.49	9.96
EN	IO	t_{HZ}	8.50					
		t_{LZ}	7.11					
		t_{ZH}	5.04	0.12	8.10	11.16	14.22	17.29
		t_{ZL}	3.93	0.06	5.40	6.87	8.34	9.81

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

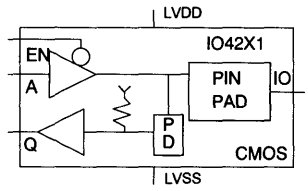


IO42X1

ABX 3.5 micron CMOS Standard Cells

Description:
IO42X1 is a 1mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.22
EN	0.20
IO	8.01

Bolt Syntax: .....IO Q .IO42X1 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	22.16	nA
†C_{pd}	9.34	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.49	3.28	2.21	2.99	4.57
		t_{PHL}	1.62	3.39	2.36	3.18	4.80

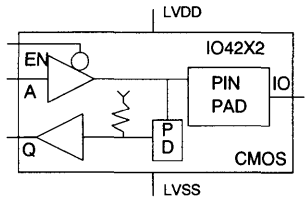
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	2.14	0.50	14.65	27.15	39.65	52.15
		t_{PHL}	3.27	0.19	8.10	12.93	17.76	22.60
EN	IO	t_{HZ}	5.56					
		t_{LZ}	5.52					
		t_{ZH}	2.58	0.50	15.08	27.58	40.08	52.59
		t_{ZL}	3.34	0.19	8.17	13.00	17.83	22.67

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO42X2 is a 2mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.23
EN	0.20
IO	7.99

Bolt Syntax: .....IO Q .IO42X2 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	22.17	nA
†C_{pd}	9.94	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.50	3.27	2.22	3.01	4.58
		t_{PHL}	1.63	3.38	2.38	3.19	4.81

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx}) (ns)	k_{tdx} (ns/pF)	Capacitive Load pF) 25	50	75	100
A	IO	t_{PLH}	5.18	0.25	11.31	17.44	23.57	29.70
		t_{PHL}	4.98	0.11	7.62	10.26	12.90	15.53
EN	IO	t_{HZ}	8.67					
		t_{LZ}	8.70					
		t_{ZH}	5.14	0.25	11.27	17.40	23.53	29.66
		t_{ZL}	4.94	0.11	7.58	10.21	12.85	15.49

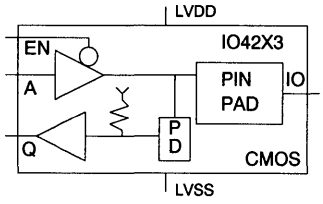
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IO42X3

ABX 3.5 micron CMOS Standard Cells

Description:
IO42X3 is a 4mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.34
EN	0.26
IO	9.85

Bolt Syntax: .....IO Q .IO42X3 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	33.59	nA
†C_{pd}	13.26	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

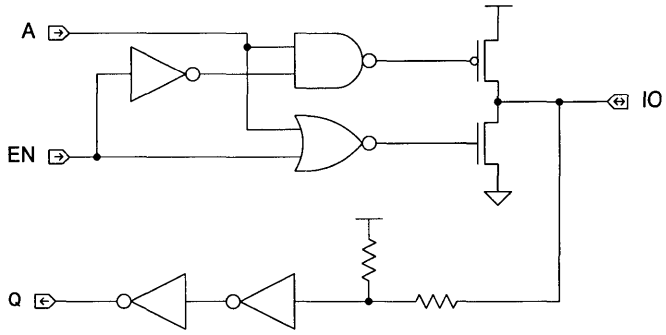
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.56	3.28	2.28	3.07	4.65
		t_{PHL}	1.69	3.40	2.44	3.25	4.88

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	4.64	0.12	7.68	10.73	13.77	16.81
		t_{PHL}	4.08	0.06	5.56	7.03	8.51	9.98
EN	IO	t_{HZ}	8.39					
		t_{LZ}	7.11					
		t_{ZH}	6.15	0.12	9.20	12.24	15.28	18.32
		t_{ZL}	4.52	0.06	6.00	7.47	8.95	10.42

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

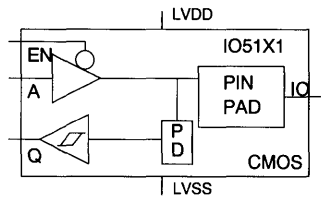


IO51X1

ABX 3.5 micron CMOS Standard Cells

Description:
IO51X1 is a 1mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.20
EN	0.20
IO	7.98

Bolt Syntax: .....IO Q .IO51X1 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	22.58	nA
†C_{pd}	9.75	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	4.21	3.50	4.98	5.82	7.50
		t_{PHL}	4.98	4.13	5.89	6.88	8.87

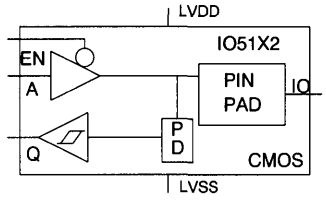
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	2.15	0.51	14.79	27.43	40.07	52.71
		t_{PHL}	3.27	0.19	8.10	12.92	17.74	22.57
EN	IO	t_{HZ}	5.64					
		t_{LZ}	5.56					
		t_{ZH}	2.63	0.51	15.27	27.91	40.55	53.19
		t_{ZL}	3.35	0.19	8.18	13.00	17.82	22.65

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IO51X2 is a 2mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.20
EN	0.20
IO	7.98

Bolt Syntax: .....IO Q .IO51X2 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	22.58	nA
†C_{pd}	10.34	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	4.25	3.45	5.01	5.84	7.49
		t_{PHL}	4.98	4.14	5.89	6.89	8.88

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	5.13	0.25	11.27	17.41	23.56	29.70
		t_{PHL}	5.00	0.11	7.64	10.29	12.94	15.58
EN	IO	t_{HZ}	8.49					
		t_{LZ}	8.81					
		t_{ZH}	5.06	0.25	11.21	17.35	23.49	29.64
		t_{ZL}	4.98	0.11	7.62	10.27	12.92	15.56

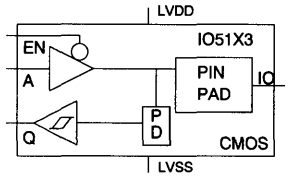
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IO51X3

ABX 3.5 micron CMOS Standard Cells

Description:
IO51X3 is a 4mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.33
EN	0.26
IO	9.83

Bolt Syntax: .....IO Q .IO51X3 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	33.52	nA
†C_{pd}	13.65	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

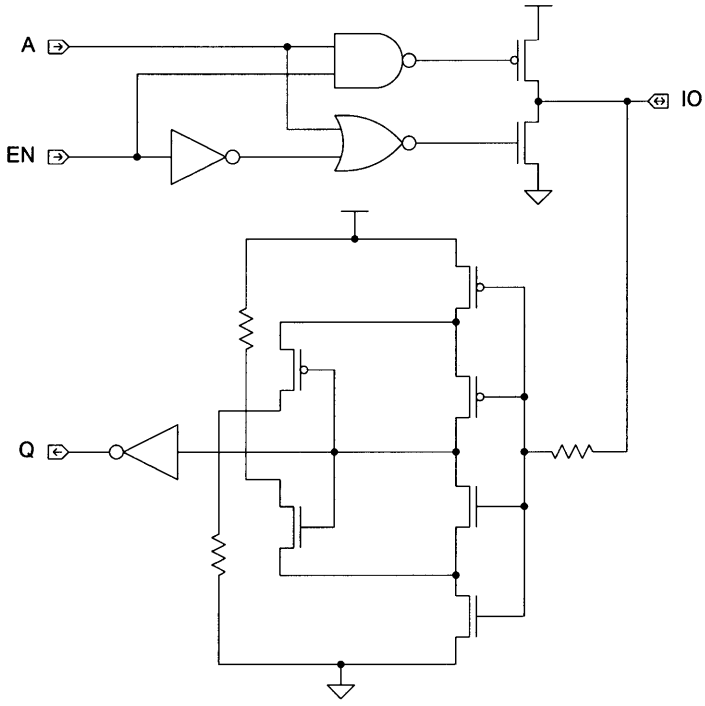
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	4.23	3.46	4.99	5.82	7.48
		t_{PHL}	4.96	4.08	5.86	6.84	8.79

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	4.64	0.12	7.70	10.76	13.82	16.88
		t_{PHL}	4.08	0.06	5.55	7.03	8.50	9.98
EN	IO	t_{HZ}	8.41					
		t_{LZ}	7.14					
		t_{ZH}	4.97	0.12	8.03	11.09	14.15	17.21
		t_{ZL}	3.96	0.06	5.43	6.91	8.38	9.86

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

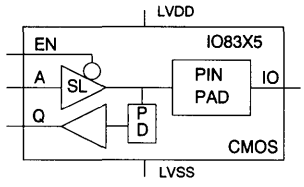
Logic Schematic



ABX 3.5 micron CMOS Standard Cells

Description:
IO83X5 is an 8mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.69
EN	0.43
IO	13.88

Bolt Syntax: .....IO Q .IO83X5 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	54.88	nA
†C_{pd}	20.51	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.69	3.28	2.41	3.19	4.77
		t_{PHL}	1.83	3.38	2.57	3.39	5.01

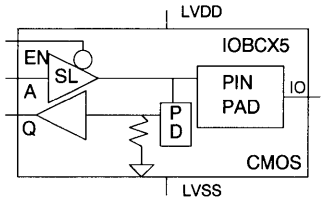
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	5.43	0.08	7.35	9.26	11.17	13.08
		t_{PHL}	4.29	0.06	5.71	7.12	8.54	9.95
EN	IO	t_{HZ}	10.87					
		t_{LZ}	9.42					
		t_{ZH}	5.66	0.08	7.57	9.48	11.40	13.31
		t_{ZL}	3.94	0.06	5.36	6.77	8.19	9.60

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IOBCX5 is an 8mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state and controlled slew rate output, and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.67
EN	0.42
IO	13.98

Bolt Syntax: .....IO Q .IOBCX5 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	55.41	nA
†C_{pd}	20.53	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.64	3.28	2.36	3.15	4.72
		t_{PHL}	1.79	3.37	2.53	3.34	4.96

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	5.42	0.08	7.33	9.24	11.15	13.06
		t_{PHL}	4.31	0.06	5.72	7.14	8.56	9.98
EN	IO	t_{HZ}	10.70					
		t_{LZ}	9.37					
		t_{ZH}	5.53	0.08	7.44	9.35	11.26	13.17
		t_{ZL}	3.96	0.06	5.38	6.80	8.22	9.64

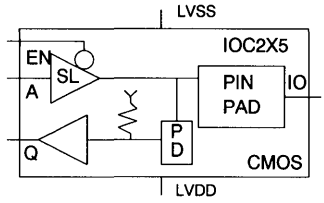
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

IOC2X5

ABX 3.5 micron CMOS Standard Cells

Description:
IOC2X5 is an 8mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state and controlled slew rate output, and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.67
EN	0.42
IO	13.97

Bolt Syntax: .....IO Q .IOC2X5 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	55.41	nA
†C_{pd}	20.53	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	1.64	3.28	2.36	3.15	4.72
		t_{PHL}	1.79	3.37	2.53	3.34	4.96

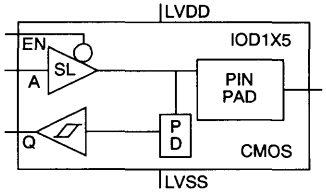
Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	5.43	0.08	7.33	9.24	11.14	13.05
		t_{PHL}	4.32	0.06	5.74	7.16	8.58	10.00
EN	IO	t_{HZ}	10.69					
		t_{LZ}	9.37					
		t_{ZH}	5.52	0.08	7.42	9.33	11.23	13.14
		t_{ZL}	3.99	0.06	5.41	6.83	8.25	9.66

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
IOD1X5 is an 8mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state and controlled slew rate output, and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Ci (pF)
A	0.72
EN	0.47
IO	14.09

Bolt Syntax: .....IO Q .IOD1X5 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	55.59	nA
†C_{pd}	21.23	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Input Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
IO	Q	t_{PLH}	5.10	3.52	5.88	6.72	8.42
		t_{PHL}	6.13	4.18	7.05	8.05	10.06

Output Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	IO	t_{PLH}	5.51	0.08	7.42	9.32	11.22	13.12
		t_{PHL}	4.31	0.06	5.73	7.15	8.58	10.00
EN	IO	t_{HZ}	10.70					
		t_{LZ}	9.67					
		t_{ZH}	5.69	0.08	7.60	9.50	11.40	13.30
		t_{ZL}	4.00	0.06	5.42	6.85	8.27	9.69

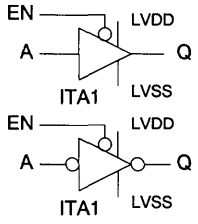
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ITA1

ABX 3.5 micron CMOS Standard Cells

Description:
ITA1 is a non-inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.08
EN	0.14
Q	0.08

Equivalent Gates:.....1.9
Bolt Syntax:.....Q .ITA1 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.07	nA
†C_{pd}	0.35	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

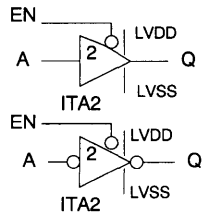
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	1.81	6.10	3.16	4.62	7.55
		t_{PHL}	1.78	5.37	2.96	4.25	6.83
EN	Q	t_{HZ}	0.82				
		t_{LZ}	0.81				
		t_{ZH}	0.55	6.10	1.89	3.35	6.28
		t_{ZL}	0.77	5.37	1.95	3.24	5.82

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
ITA2 is a non-inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.09
EN	0.24
Q	0.11

Equivalent Gates:.....2.2
Bolt Syntax:.....QN .ITA2 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.35	nA
†C_{pd}	0.62	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	2.21	2.03	2.66	3.15	4.12
		t_{PHL}	2.19	1.77	2.58	3.00	3.85
EN	Q	t_{HZ}	0.82				
		t_{LZ}	1.01				
		t_{ZH}	0.37	2.03	0.82	1.31	2.28
		t_{ZL}	0.75	1.77	1.14	1.57	2.42

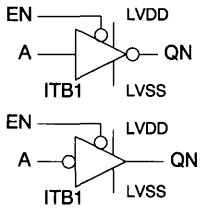
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ITB1

ABX 3.5 micron CMOS Standard Cells

Description:
ITB1 is an inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.09
EN	0.14
QN	0.06

Equivalent Gates:.....1.2
Bolt Syntax:.....QN .ITB1 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.37	nA
†C_{pd}	0.18	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

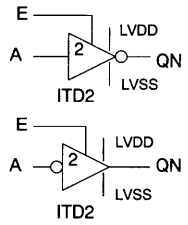
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	QN	t_{LH}	0.92	6.10	2.27	3.73	6.66
		t_{PHL}	1.02	5.38	2.21	3.50	6.08
EN	QN	t_{HZ}	0.82				
		t_{LZ}	0.92				
		t_{ZH}	0.51	6.10	1.85	3.32	6.25
		t_{ZL}	0.74	5.38	1.93	3.22	5.80

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
ITD2 is an inverting internal tri-state buffer with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

Pin Loading

	Ci (pF)
A	0.25
E	0.16
QN	0.12

Equivalent Gates:.....1.8
Bolt Syntax:.....QN .ITD2 A E LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.68	nA
†C_{pd}	0.43	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	QN	t_{PLH}	0.88	2.05	1.33	1.82	2.80
		t_{PHL}	0.84	1.71	1.22	1.63	2.45
E	QN	t_{HZ}	2.13				
		t_{LZ}	0.61				
		t_{ZH}	1.36	2.05	1.82	2.31	3.29
		t_{ZL}	0.31	1.71	0.68	1.09	1.91

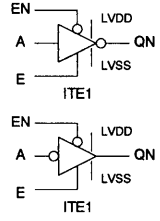
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ITE1

ABX 3.5 micron CMOS Standard Cells

Description:
ITE1 is a two-phase inverting internal tri-state buffer.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

Pin Loading

	Ci (pF)
A	0.10
E	0.04
EN	0.06
QN	0.06

Equivalent Gates:.....0.9
Bolt Syntax:.....QN .ITE1 A E EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	0.71	nA
†C_{pd}	0.09	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

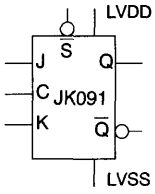
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	QN	t_{PLH} t_{PHL}	0.94 1.02	6.09 5.37	2.28 2.21	3.74 3.49	6.67 6.07
EN	QN	t_{HZ} t_{ZH}	0.00 0.71	6.09	2.05	3.51	6.44
E	QN	t_{LZ} t_{ZL}	0.74 0.88	5.37	2.06	3.35	5.93

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
JK091 is a static, master-slave, JK flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	H	L
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Change

Pin Loading

	Ci (pF)
J	0.09
K	0.10
C	0.29
SN	0.19

Equivalent Gates:.....7.2
Bolt Syntax:.....Q QN .JK091 C J K SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	8.49	nA
†C_{pd}	1.76	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	3.84 5.65	4.36 5.21	4.79 6.79	5.84 8.04	7.93 10.54
C	QN	t_{PLH} t_{PHL}	3.77 2.22	6.02 5.39	5.09 3.40	6.54 4.70	9.43 7.28
SN	Q	t_{PLH}	0.87	4.36	1.83	2.88	4.97
SN	QN	t_{PHL}	4.01	5.39	5.19	6.48	9.07
Min C Width	High	t_w				8.04	
Min C Width	Low	t_w	5.62				
Min SN Width	Low	t_w				6.48	
Min J Setup		t_{su}	5.62				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	4.48				

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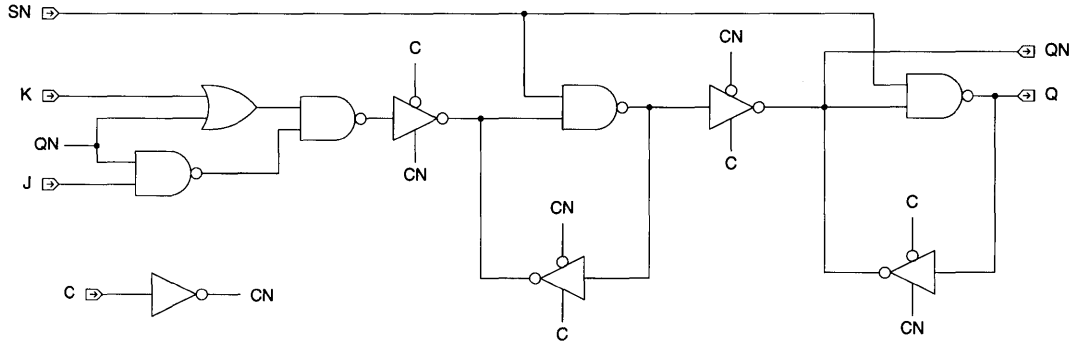
ABX 3.5 micron CMOS Standard Cells

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min K Hold		t_h	0.00				
Min SN Setup		t_{su}	1.38				
Min SN Hold		t_h	1.21				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

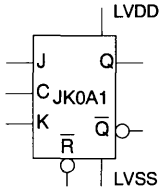
For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



Description:
JK0A1 is a static, master-slave, JK flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	L	H
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Charge

Pin Loading

	Ci (pF)
J	0.09
K	0.10
C	0.28
RN	0.10

Equivalent Gates: 7.8
Bolt Syntax: ..... Q QN .JK0A1 C J K RN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	8.22	nA
†C_{pd}	2.02	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	4.00 5.92	5.95 5.72	5.31 7.18	6.73 8.55	9.59 11.29
C	QN	t_{PLH} t_{PHL}	3.77 2.19	6.05 5.38	5.10 3.37	6.55 4.66	9.46 7.25
RN	Q	t_{PHL}	2.52	5.72	3.78	5.15	7.90
RN	QN	t_{PLH}	6.13	6.05	7.46	8.91	11.82
Min C Width	High	t_w				8.55	
Min C Width	Low	t_w	4.21				
Min RN Width	Low	t_w				8.91	
Min J Setup		t_{su}	5.87				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	4.75				

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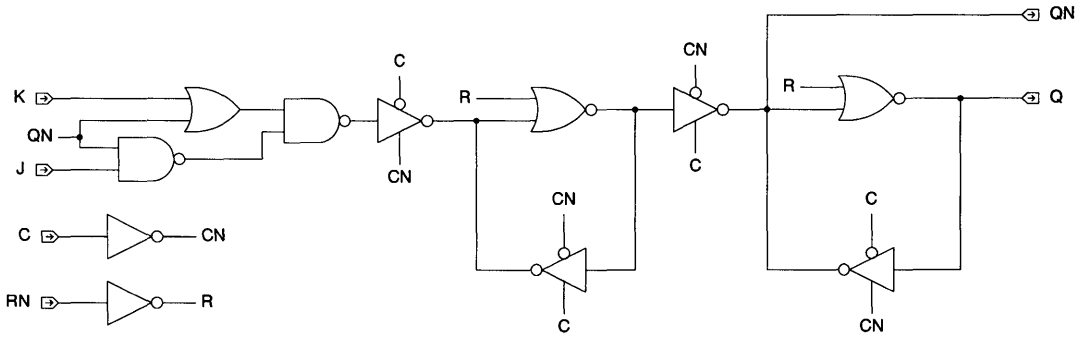
ABX 3.5 micron CMOS Standard Cells

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	2.95				
Min RN Hold		t_h	2.27				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

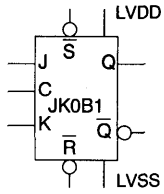
For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



Description:
JK0B1 is a static, master-slave, JK flip-flop. SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

Pin Loading

	Ci (pF)
J	0.09
K	0.10
C	0.30
SN	0.20
RN	0.19

Equivalent Gates:.....9.9
Bolt Syntax:.....Q QN .JK0B1 C J K RN SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	9.67	nA
†C_{pd}	2.16	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	3.96 5.76	4.30 5.22	4.91 6.90	5.94 8.16	8.00 10.66
C	QN	t_{PLH} t_{PHL}	3.81 2.23	6.03 5.39	5.14 3.42	6.58 4.71	9.48 7.30
RN	Q	t_{PHL}	8.66	5.22	9.81	11.06	13.57
RN	QN	t_{PLH}	6.65	6.03	7.98	9.43	12.32
SN	Q	t_{PLH}	0.96	4.30	1.90	2.94	5.00
SN	QN	t_{PHL}	4.71	5.39	5.90	7.19	9.78
Min C Width	High	t_w				8.16	
Min C Width	Low	t_w	6.97				
Min RN Width	Low	t_w				11.06	
Min SN Width	Low	t_w				7.19	

(continued on next page)

JK0B1

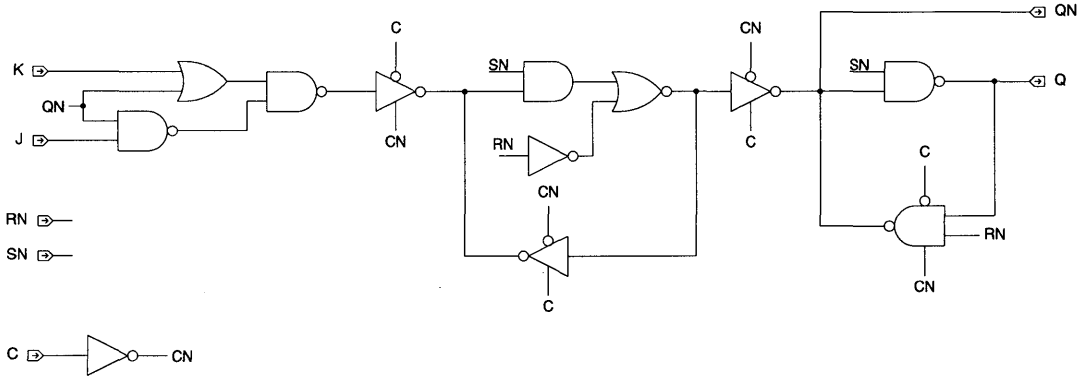
ABX 3.5 micron CMOS Standard Cells

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min J Setup		t_{su}	6.97				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	6.15				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	2.91				
Min RN Hold		t_h	2.33				
Min SN Setup		t_{su}	3.09				
Min SN Hold		t_h	1.24				

For Q Delays: $t_{plh}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{dr}(Q) + (k_{tdr}(Q) * C_L(Q)) + (k_{tdf}(QN) * C_L(QN))]$
$t_{phl}(C_{L(Q)}, C_{L(QN)}) = K_P K_V K_T[t_{df}(Q) + (k_{tdf}(Q) * C_L(Q)) + (k_{tdr}(QN) * C_L(QN))]$

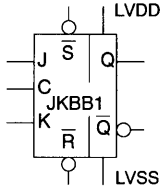
For QN Delays: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



Description:
JKBB1 is a static, master-slave, JK flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

Pin Loading

	Ci (pF)
J	0.10
K	0.09
C	0.27
SN	0.18
RN	0.19

Equivalent Gates:.....11.2
Bolt Syntax:.....Q QN .JKBB1 C J K RN SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	10.61	nA
†C_{pd}	2.31	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	3.55 5.18	4.35 4.85	4.51 6.24	5.56 7.41	7.65 9.73
C	QN	t_{PLH} t_{PHL}	7.02 5.35	3.68 3.75	7.82 6.18	8.71 7.08	10.47 8.88
RN	Q	t_{PHL}	7.71	4.85	8.77	9.94	12.26
RN	QN	t_{PLH}	9.56	3.68	10.37	11.25	13.01
SN	Q	t_{PLH}	6.26	4.35	7.21	8.26	10.35
SN	QN	t_{PHL}	2.01	3.75	2.84	3.74	5.54
Min C Width	High	t_w	6.21				
Min C Width	Low	t_w	6.76				
Min RN Width	Low	t_w	8.80				
Min SN Width	Low	t_w	5.17				

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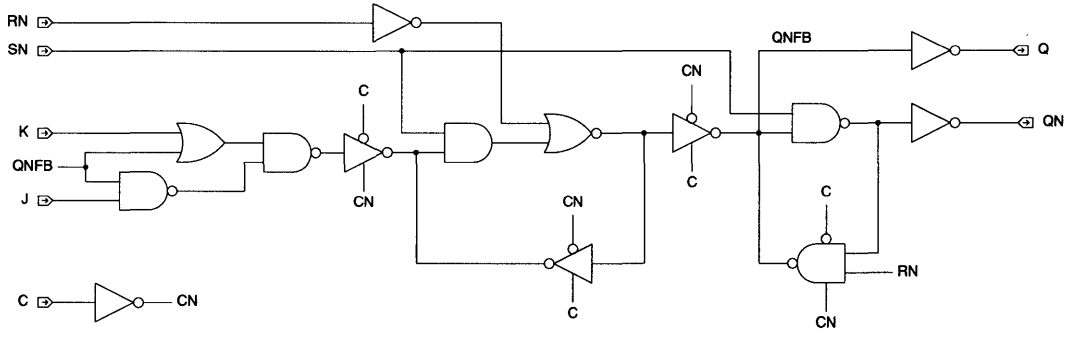
ABX 3.5 micron CMOS Standard Cells

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Min J Setup		t_{su}	6.76				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	5.48				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	2.52				
Min RN Hold		t_h	4.74				
Min SN Setup		t_{su}	2.53				
Min SN Hold		t_h	1.76				

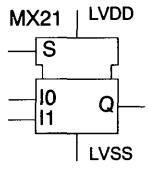
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



Description:
MX21 is a 2-input to 1-output digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Pin Loading

	Ci (pF)
I0	0.09
I1	0.10
S	0.15

Equivalent Gates:.....2.1
Bolt Syntax:.....Q .MX21 I0 I1 S LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.40	nA
†C_{pd}	0.42	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

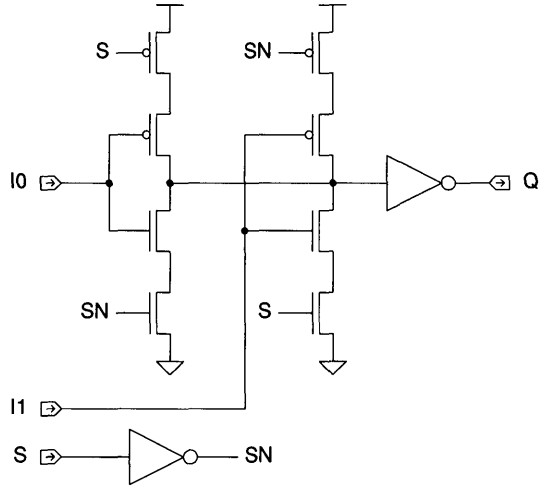
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

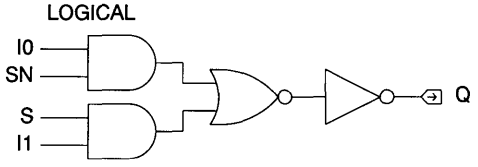
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Ix Input	Q	t_{PLH} t_{PHL}	2.26 2.28	3.52 4.15	3.03 3.19	3.88 4.19	5.56 6.18
S	Q	t_{PLH} t_{PHL}	3.46 3.42	3.52 4.15	4.23 4.33	5.08 5.33	6.76 7.32

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ABX 3.5 micron CMOS Standard Cells

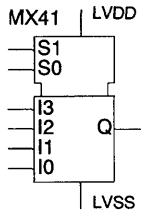
Logic Schematic





Description:
MX41 is a four-to-one digital multiplexer.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

Pin Loading

	Ci (pF)
I0	0.10
I1	0.10
I2	0.10
I3	0.10
S0	0.29
S1	0.29

Equivalent Gates:.....5.8
Bolt Syntax:.....Q .MX41 I0 I1 I2 I3 S0 S1 LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	4.94	nA
†C_{pd}	1.06	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†*Note: C_{pd} does not include interconnect capacitance.*

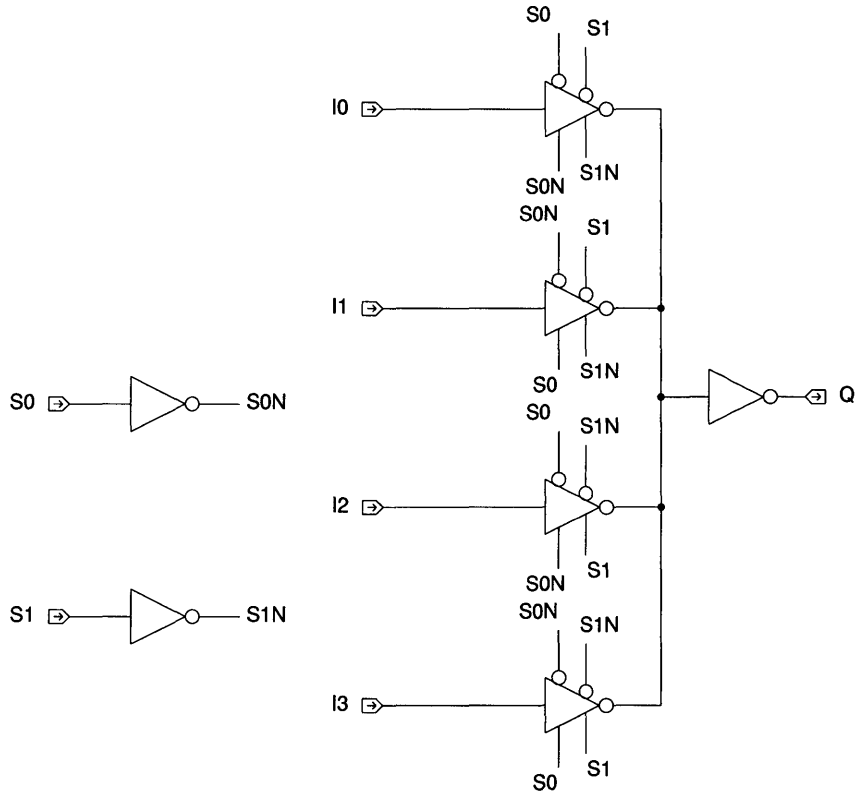
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Ix Input	Q	t_{PLH}	5.26	4.43	6.23	7.29	9.42
		t_{PHL}	4.69	5.83	5.97	7.37	10.17
Any Sx Input	Q	t_{PLH}	5.14	4.43	6.11	7.18	9.30
		t_{PHL}	5.11	5.83	6.39	7.79	10.59

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

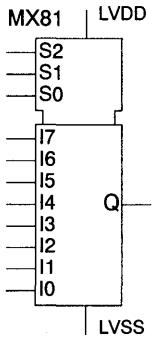
ABX 3.5 micron CMOS Standard Cells

Logic Schematic



Description:
MX81 is an eight-to-one digital multiplexer.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

Pin Loading

	Ci (pF)
I0	0.10
I1	0.11
I2	0.11
I3	0.10
I4	0.10
I5	0.10
I6	0.10
I7	0.10
S0	0.50
S1	0.31
S2	0.19

Equivalent Gates:.....14.0
Bolt Syntax:.....Q .MX81 I0 I1 I2 I3 I4 I5 I6 I7 S0 S1 S2 LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	12.57	nA
†C_{pd}	2.64	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

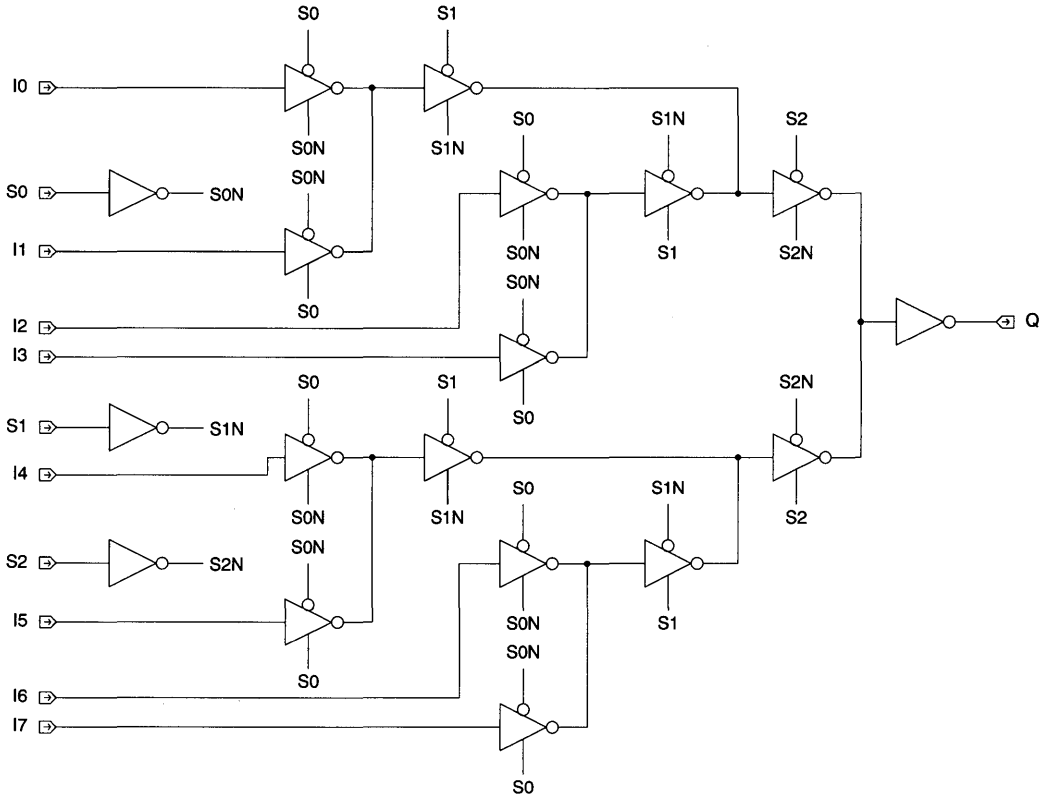
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Ix Input	Q	t_{PLH}	6.21	3.57	6.99	7.85	9.56
		t_{PHL}	6.00	4.22	6.93	7.95	9.98
Any Sx Input	Q	t_{PLH}	6.07	3.57	6.86	7.71	9.43
		t_{PHL}	5.97	4.22	6.90	7.91	9.94

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

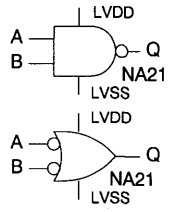
ABX 3.5 micron CMOS Standard Cells

Logic Schematic



Description:
NA21 is a two-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

Pin Loading

	Ci (pF)
A	0.08
B	0.09

Equivalent Gates:.....1.0
Bolt Syntax:.....Q .NA21 A B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.26	nA
†C_{pd}	0.09	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	0.65	3.63	1.45	2.32	4.06
		t_{PHL}	0.67	4.40	1.64	2.69	4.80

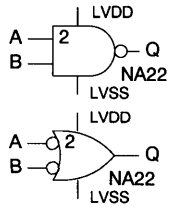
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

NA22

ABX 3.5 micron CMOS Standard Cells

Description:
NA22 is a two-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

Pin Loading

	Ci (pF)
A	0.17
B	0.17

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .NA22 A B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.50	nA
†C_{pd}	0.25	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

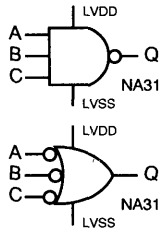
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	0.70	1.75	1.09	1.51	2.35
		t_{PHL}	0.70	2.07	1.15	1.65	2.64

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NA31 is a three-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Pin Loading

	Ci (pF)
A	0.08
B	0.08
C	0.08

Equivalent Gates:.....1.3
Bolt Syntax:.....Q .NA31 A B C LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.76	nA
†C_{pd}	0.13	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	0.90	3.97	1.77	2.72	4.63
		t_{PHL}	0.94	5.16	2.07	3.31	5.79

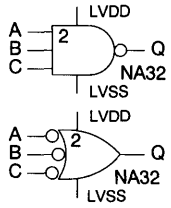
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

NA32

ABX 3.5 micron CMOS Standard Cells

Description:
NA32 is a three-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Pin Loading

	Ci (pF)
A	0.17
B	0.18
C	0.18

Equivalent Gates:.....2.3
Bolt Syntax:.....Q .NA32 A B C LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.48	nA
†C_{pd}	0.23	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

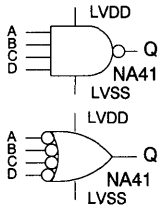
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	0.82	1.90	1.24	1.70	2.61
		t_{PHL}	0.89	2.63	1.46	2.10	3.36

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NA41 is a four-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.08
D	0.09

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .NA41 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.21	nA
†C_{pd}	0.18	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

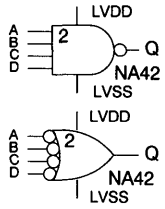
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.20	4.31	2.14	3.18	5.25
		t_{PHL}	1.33	5.89	2.63	4.05	6.87

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ABX 3.5 micron CMOS Standard Cells

Description:
NA42 is a four-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.17
B	0.18
C	0.19
D	0.19

Equivalent Gates:.....3.0
Bolt Syntax:.....Q .NA42 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	4.38	nA
†C_{pd}	0.31	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

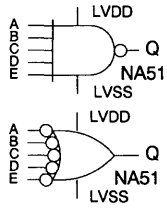
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.07	2.08	1.52	2.02	3.02
		t_{PHL}	1.24	2.99	1.90	2.61	4.05

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NA51 is a five-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09
D	0.09
E	0.09

Equivalent Gates:.....2.0
Bolt Syntax:.....Q .NA51 A B C D E LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.59	nA
†C_{pd}	0.21	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.47	4.74	2.51	3.65	5.92
		t_{PHL}	1.66	6.50	3.09	4.65	7.77

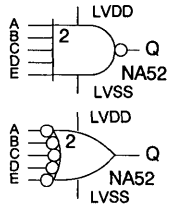
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

AMI SEMICONDUCTORS

ABX 3.5 micron CMOS Standard Cells

Description:
NA52 is a five-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.18
B	0.18
C	0.18
D	0.18
E	0.18

Equivalent Gates:.....2.9
Bolt Syntax:.....Q .NA52 A B C D E LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	5.09	nA
†C_{pd}	0.37	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

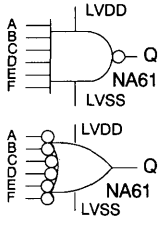
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.30	2.30	1.81	2.36	3.47
		t_{PHL}	1.58	3.29	2.30	3.09	4.67

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NA61 is a six-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.09
B	0.08
C	0.09
D	0.09
E	0.08
F	0.09

Equivalent Gates: 3.9
Bolt Syntax: ..... Q .NA61 A B C D E F LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	4.95	nA
†C_{pd}	0.66	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

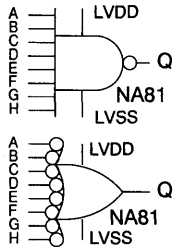
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	3.26	3.36	4.00	4.81	6.42
		t_{PHL}	3.27	3.78	4.11	5.02	6.83

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ABX 3.5 micron CMOS Standard Cells

Description:
NA81 is an eight-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

Pin Loading

	Ci (pF)
A	0.08
B	0.08
C	0.08
D	0.08
E	0.09
F	0.09
G	0.09
H	0.09

Equivalent Gates:.....4.5
Bolt Syntax:.....Q .NA81 A B C D E F G H LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	5.85	nA
†C_{pd}	0.71	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

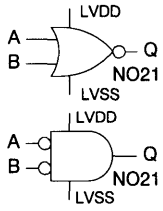
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	3.63	3.37	4.37	5.18	6.80
		t_{PHL}	3.67	3.81	4.51	5.43	7.25

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NO21 is a two-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Pin Loading

	Ci (pF)
A	0.09
B	0.09

Equivalent Gates:.....1.0
Bolt Syntax:.....Q .NO21 A B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	0.78	nA
†C_{pd}	0.09	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	0.77	5.47	1.98	3.29	5.92
		t_{PHL}	1.09	4.71	2.13	3.26	5.52

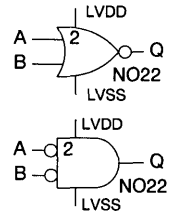
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

NO22

ABX 3.5 micron CMOS Standard Cells

Description:
NO22 is a two-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Pin Loading

	Ci (pF)
A	0.16
B	0.19

Equivalent Gates:.....1.4
Bolt Syntax:.....Q .NO22 A B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.51	nA
†C_{pd}	0.17	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

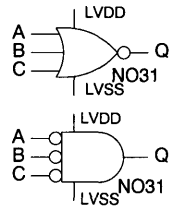
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	0.76	2.76	1.37	2.03	3.36
		t_{PHL}	0.93	2.12	1.39	1.90	2.92

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NO31 is a three-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

Pin Loading

	Ci (pF)
A	0.08
B	0.09
C	0.09

Equivalent Gates:.....1.3
Bolt Syntax:.....Q .NO31 A B C LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	0.84	nA
†C_{pd}	0.13	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.38	7.60	3.05	4.88	8.52
		t_{PHL}	1.69	6.08	3.02	4.48	7.40

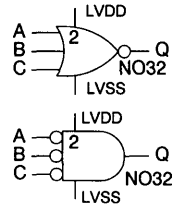
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

NO32

ABX 3.5 micron CMOS Standard Cells

Description:
NO32 is a three-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

Pin Loading

	Ci (pF)
A	0.16
B	0.17
C	0.18

Equivalent Gates:.....1.8
Bolt Syntax:.....Q .NO32 A B C LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.61	nA
†C_{pd}	0.23	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

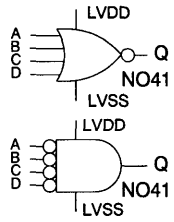
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.30	3.85	2.15	3.07	4.92
		t_{PHL}	1.34	2.65	1.93	2.56	3.84

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

Description:
NO41 is a four-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09
D	0.09

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .NO41 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	0.87	nA
†C_{pd}	0.16	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	2.19	9.99	4.38	6.78	11.57
		t_{PHL}	1.90	6.37	3.31	4.84	7.90

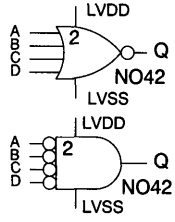
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

NO42

ABX 3.5 micron CMOS Standard Cells

Description:
NO42 is a four-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.18
B	0.18
C	0.19
D	0.18

Equivalent Gates:.....2.3
Bolt Syntax:.....Q .NO42 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.66	nA
†C_{pd}	0.28	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

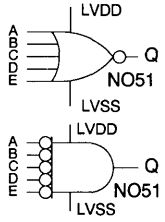
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	2.06	5.07	3.18	4.39	6.82
		t_{PHL}	1.45	2.85	2.08	2.76	4.13

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
NO51 is a five-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09
D	0.09
E	0.09

Equivalent Gates:.....2.0
Bolt Syntax:.....Q .NO51 A B C D E LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	0.91	nA
†C_{pd}	0.20	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	3.26	12.36	5.98	8.95	14.88
		t_{PHL}	2.04	6.70	3.51	5.12	8.33

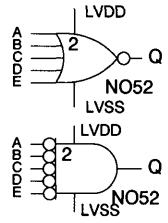
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

NO52

ABX 3.5 micron CMOS Standard Cells

Description:
NO52 is a five-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

Pin Loading

	Ci (pF)
A	0.18
B	0.19
C	0.19
D	0.20
E	0.19

Equivalent Gates:.....2.8
Bolt Syntax:.....Q .NO52 A B C D E LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.70	nA
†C_{pd}	0.35	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

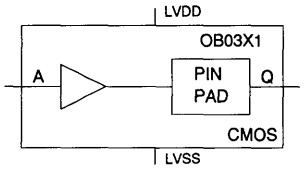
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	3.08	6.29	4.46	5.97	8.99
		t_{PHL}	1.52	3.01	2.18	2.90	4.35

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB03X1 is a 1mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.09

Bolt Syntax: .....Q .OB03X1 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	17.53	nA
†C_{pd}	8.51	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	6.99	0.51	19.64	32.28	44.93	57.58
		t_{PHL}	5.10	0.19	9.90	14.70	19.49	24.29

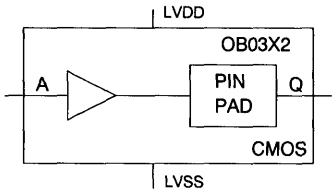
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB03X2

ABX 3.5 micron CMOS Standard Cells

Description:
OB03X2 is a 2mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.17

Bolt Syntax: .....Q .OB03X2 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	18.16	nA
†C_{pd}	9.17	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

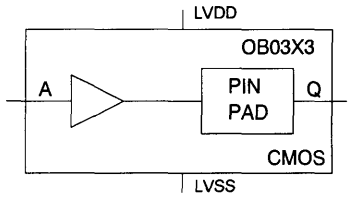
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	5.07	0.25	11.33	17.59	23.85	30.10
		t_{PHL}	4.19	0.10	6.60	9.01	11.43	13.84

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

1.5/3.5 micron Mixed Signal

Description:
OB03X3 is a 4mA, non-inverting,CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.30

Bolt Syntax: .....Q .OB03X3 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	28.41	nA
†C_{pd}	12.15	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	4.24	0.12	7.34	10.43	13.53	16.63
		t_{PHL}	3.56	0.05	4.84	6.12	7.39	8.67

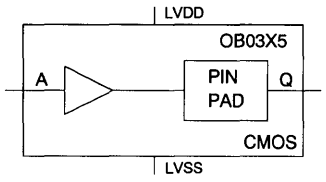
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB03X5

ABX 3.5 micron CMOS Standard Cells

Description:
OB03X5 is an 8mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.58

Bolt Syntax: ..... Q .OB03X5 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	48.53	nA
†C_{pd}	18.60	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

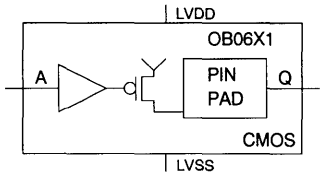
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	3.99	0.06	5.52	7.05	8.57	10.10
		t_{PHL}	3.17	0.03	3.92	4.67	5.42	6.17

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB06X1 is a 1mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.09
Q	7.76

Bolt Syntax: .....Q .OB06X1 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	18.11	nA
†C_{pd}	8.34	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH} t_{HZ}	1.76 4.71	0.51	14.43	27.10	39.77	52.44

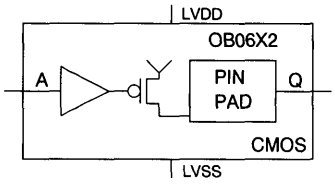
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

OB06X2

ABX 3.5 micron CMOS Standard Cells

Description:
OB06X2 is a 2mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.10
Q	7.76

Bolt Syntax: ..... Q .OB06X2 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	18.11	nA
†C_{pd}	8.63	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

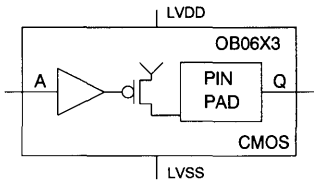
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH} t_{HZ}	3.65 7.31	0.25	9.94	16.23	22.52	28.81

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

Description:
OB06X3 is a 4mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.10
Q	7.61

Bolt Syntax: .....Q .OB06X3 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	25.55	nA
†C_{pd}	9.20	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH} t_{HZ}	3.61 7.27	0.13	6.75	9.89	13.03	16.17

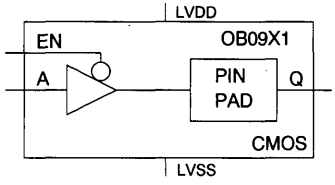
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB09X1

ABX 3.5 micron CMOS Standard Cells

Description:
OB09X1 is a 1mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.20
EN	0.19
Q	7.76

Bolt Syntax: .....Q .OB09X1 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	19.39	nA
†C_{pd}	8.88	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

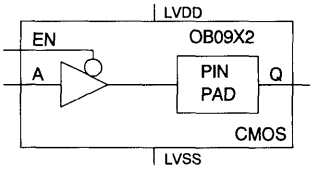
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	2.23	0.51	14.86	27.49	40.13	52.76
		t_{PHL}	3.31	0.19	8.14	12.96	17.79	22.61
EN	Q	t_{HZ}	5.62					
		t_{LZ}	5.60					
		t_{ZH}	2.66	0.51	15.30	27.93	40.56	53.20
		t_{ZL}	3.38	0.19	8.21	13.03	17.86	22.68

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB09X2 is a 2mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.20
EN	0.19
Q	7.76

Bolt Syntax: .....Q .OB09X2 A EN LVDD LVSS; ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	19.39	nA
†C_{pd}	9.47	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	5.12	0.25	11.27	17.43	23.58	29.73
		t_{PHL}	5.02	0.11	7.67	10.33	12.98	15.63
EN	Q	t_{HZ}	8.43					
		t_{LZ}	8.83					
		t_{ZH}	5.01	0.25	11.16	17.31	23.47	29.62
		t_{ZL}	4.99	0.11	7.64	10.30	12.95	15.60

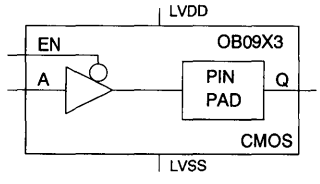
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OB09X3

ABX 3.5 micron CMOS Standard Cells

Description:
OB09X3 is a 4mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.32
EN	0.26
Q	9.58

Bolt Syntax: .....Q .OB09X3 A EN LVDD LVSS; ;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	30.24	nA
†C_{pd}	12.67	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

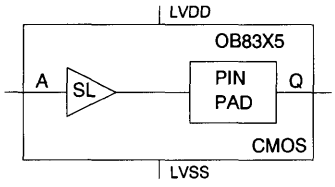
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	4.53	0.12	7.55	10.58	13.60	16.63
		t_{PHL}	4.09	0.06	5.59	7.08	8.58	10.07
EN	Q	t_{HZ}	8.10					
		t_{LZ}	7.22					
		t_{ZH}	4.83	0.12	7.85	10.88	13.90	16.93
		t_{ZL}	3.99	0.06	5.48	6.98	8.47	9.97

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB83X5 is an 8mA, non-inverting, CMOS-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.71
Q	13.77

Bolt Syntax: .....Q .OB83X5 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	49.81	nA
†C_{pd}	19.22	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

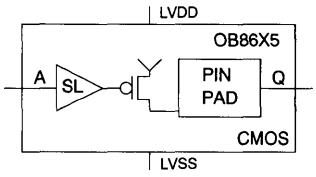
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	4.85	0.08	6.75	8.66	10.57	12.47
		t_{PHL}	3.57	0.05	4.78	5.99	7.20	8.41

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ABX 3.5 micron CMOS Standard Cells

Description:
OB86X5 is an 8mA, inverting, CMOS-level, output buffer pad with a P-channel open-drain (pull-up) and controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Ci (pF)
A	0.10
Q	13.62

Bolt Syntax: .....Q .OB86X5 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	47.18	nA
†C_{pd}	16.87	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

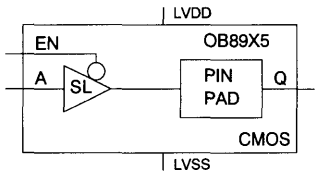
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH} t_{HZ}	5.77 10.18	0.08	7.87	9.98	12.08	14.18

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OB89X5 is an 8mA, non-inverting,CMOS-level, tri-state output buffer pad with active low enable and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Ci (pF)
A	0.70
EN	0.45
Q	13.84

Bolt Syntax: .....Q .OB89X5 A EN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	52.84	nA
†C_{pd}	20.11	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Capacitive Load (pF) 25	50	75	100
A	Q	t_{PLH}	5.45	0.08	7.35	9.25	11.15	13.05
		t_{PHL}	4.26	0.06	5.68	7.10	8.53	9.95
EN	Q	t_{HZ}	10.64					
		t_{LZ}	9.51					
		t_{ZH}	5.65	0.08	7.55	9.45	11.35	13.25
		t_{ZL}	3.95	0.06	5.37	6.80	8.22	9.64

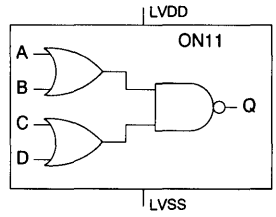
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

ON11

ABX 3.5 micron CMOS Standard Cells

Description:
ON11 is an OR-NAND circuit consisting of two 2-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
H	X	H	X	L
H	X	X	H	L
X	H	H	X	L
X	H	X	H	L

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09
D	0.09

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .ON11 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.42	nA
†C_{pd}	0.25	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

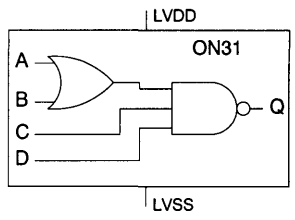
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.62	6.13	2.97	4.44	7.38
		t_{PHL}	1.29	4.05	2.18	3.15	5.10

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
ON31 is an OR-NAND circuit consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	X	H	H	L
X	H	H	H	L

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09
D	0.09

Equivalent Gates:.....1.5
Bolt Syntax:.....Q .ON31 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.79	nA
†C_{pd}	0.21	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.20	7.17	2.78	4.50	7.94
		t_{PHL}	1.13	5.14	2.26	3.50	5.96

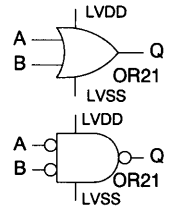
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OR21

ABX 3.5 micron CMOS Standard Cells

Description:
OR21 is a two-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Pin Loading

	Ci (pF)
A	0.08
B	0.09

Equivalent Gates:.....1.3
Bolt Syntax:.....Q .OR21 A B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.45	nA
†C_{pd}	0.23	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

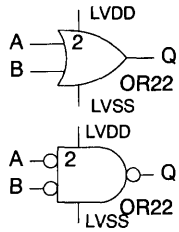
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	1.93	3.37	2.67	3.48	5.10
		t_{PHL}	1.88	3.77	2.71	3.61	5.42

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OR22 is a two-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Pin Loading

	Ci (pF)
A	0.09
B	0.09

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .OR22 A B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.11	nA
†C_{pd}	0.33	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	2.30	1.88	2.71	3.16	4.06
		t_{PHL}	2.30	2.13	2.76	3.27	4.30

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

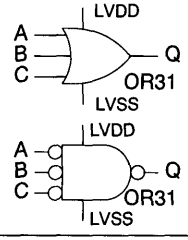
OR31

AMI SEMICONDUCTORS

ABX 3.5 micron CMOS Standard Cells

Description:
OR31 is a three-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09

Equivalent Gates:.....1.7
Bolt Syntax:.....Q .OR31 A B C LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.51	nA
†C_{pd}	0.28	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

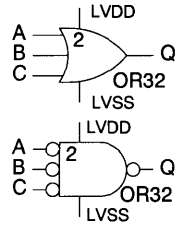
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	2.82	3.56	3.60	4.46	6.16
		t_{PHL}	2.85	4.18	3.77	4.78	6.78

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
OR32 is a three-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Pin Loading

	Ci (pF)
A	0.09
B	0.09
C	0.09

Equivalent Gates:.....2.0
Bolt Syntax:.....Q .OR32 A B C LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.17	nA
†C_{pd}	0.37	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	3.25	2.12	3.71	4.22	5.24
		t_{PHL}	3.40	2.44	3.94	4.53	5.70

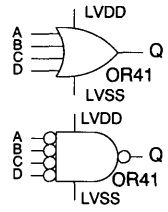
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

OR41

ABX 3.5 micron CMOS Standard Cells

Description:
OR41 is a four-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Pin Loading

	Ci (pF)
A	0.10
B	0.09
C	0.09
D	0.09

Equivalent Gates:.....2.0
Bolt Syntax:.....Q .OR41 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	1.54	nA
†C_{pd}	0.31	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

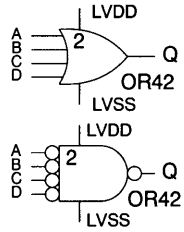
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	3.14	3.68	3.95	4.83	6.60
		t_{PHL}	4.01	4.61	5.03	6.13	8.35

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

Description:
OR42 is a four-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Pin Loading

	Ci (pF)
A	0.10
B	0.09
C	0.09
D	0.09

Equivalent Gates:.....2.4
Bolt Syntax:.....Q .OR42 A B C D LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	2.20	nA
†C_{pd}	0.41	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
Any Input	Q	t_{PLH}	3.62	2.24	4.12	4.65	5.73
		t_{PHL}	4.80	2.77	5.41	6.08	7.41

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

PORA

ABX 3.5 micron CMOS Standard Cells

Description:

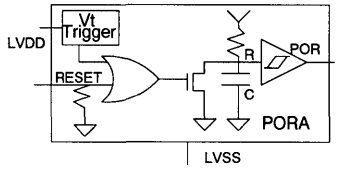
PORA is a power-on-reset circuit for 5-10 volt operation.

When power is applied, the POR output is asserted low for at least 400 nanoseconds after the logic circuits become operational. The active-high RESET input also drives the POR signal to its active low state.

For proper operation, user-designed external circuitry must limit the slew rate of Vdd power to a maximum of one volt per microsecond. This ensures that the reset pulse will be properly output when Vdd falls to zero and immediately returns to its valid range.

PORA will work at Vdd voltages down to 4.0 volts.

Logic Symbol



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Ci (pF)
RESET	0.33

Equivalent Gates:.....23.7

Bolt Syntax:.....POR .PORA RESET LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	21.01	nA
†C_{pd}	22.97	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

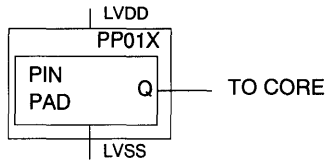
Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
RESET	POR	t_{PLH} t_{PHL}	1628.92 13.33	4.50 2.52	1630.18 14.04	1631.45 14.75	1633.97 16.16
VDD	POR	t_{PLH}	3146.35	4.50	3147.61	3148.88	3151.40

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

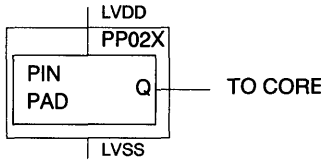
Description:
PP01X is a Vss power supply pin for output buffers, input buffers, and core cells combined.



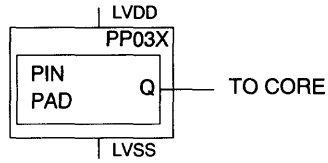
PP02X

ABX 3.5 micron CMOS Standard Cells

Description:
PP02X is a Vdd power supply pin for output buffers, input buffers, and core cells combined.

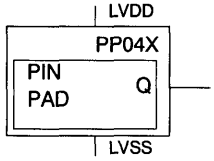


Description:
PP03X is a Vcc power supply pin for output buffers, input buffers, and core cells combined.



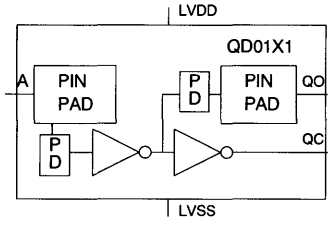
ABX 3.5 micron CMOS Standard Cells

Description:
PP04X is an optional power supply pin for connecting additional buses.

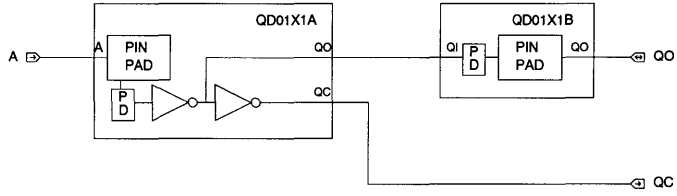


Description:
QD01X1 is a 3.58 MHz(1MHz - 10 MHz) crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Ci (pF)
A	5.45
QO	5.45

Bolt Syntax: .....QC QO .QD01X1A A LVDD LVSS;
.....QI QO .QD01X1B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	8.94	nA
†C_{pd}	0.30	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
QO	QC	t_{PLH}	0.96	4.06	1.85	2.82	4.77
		t_{PHL}	1.14	5.10	2.26	5.93	5.93

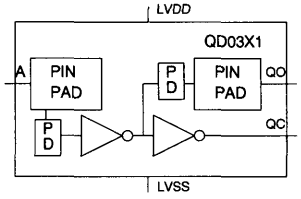
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

QD03X1

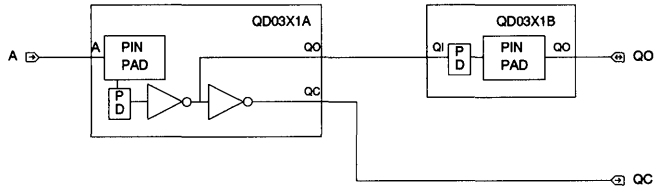
ABX 3.5 micron CMOS Standard Cells

Description:
QD03X1 is a 20 MHz (10 MHz - 32 MHz) crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Ci (pF)
A	5.70
QO	5.70

Bolt Syntax: .....QC QO .QD03X1A A LVDD LVSS;
.....QI QO .QD03X1B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	14.04	nA
†C_{pd}	1.11	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

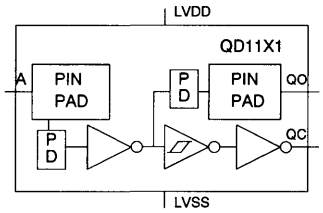
Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
QO	QC	t_{PLH}	0.63	0.89	0.83	1.04	1.47
		t_{PHL}	0.81	0.97	1.03	1.26	1.73

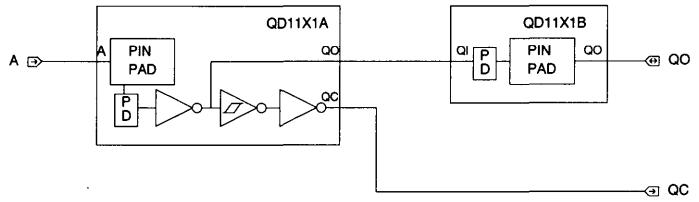
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Description:
QD11X1 is a 32kHz (32kHz - 1MHz) crystal oscillator with Schmitt trigger. QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	H	H
H	L	L

Pin Loading

	Ci (pF)
A	5.45
QO	5.45

Bolt Syntax: .....QC QO .QD11X1A A LVDD LVSS;
.....QI QO .QD11X1B LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	10.66	nA
†C_{pd}	10.66	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
QO	QC	t_{PLH}	4.15	5.22	5.30	6.55	9.06
		t_{PHL}	4.96	6.35	6.35	7.88	10.93

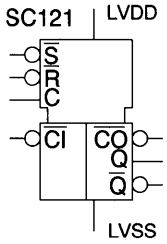
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

SC121

ABX 3.5 micron CMOS Standard Cells

Description:
SC121 is a static, master-slave, synchronous up-counter bit with ripple carry. SET and RESET are asynchronous and active low. Outputs are buffered. The output toggles on the rising edge of the clock when CIN is active low.

Logic Symbol



Truth Table

RN	SN	CIN	C	CON(n+1)	Q(n+1)	QN(n+1)
L	L	X	X	-	IL	IL
L	H	X	X	-	L	H
H	L	X	X	-	H	L
H	H	L	↑	-	QN(n)	Q(n)
H	H	H	↑	-	NC	NC
X	X	L	X	QN(n+1)	-	-
X	X	H	X	H	-	-

IL = Illegal NC=No Change

Pin Loading

	Ci (pF)
C	0.27
SN	0.20
RN	0.19
CIN	0.18

Equivalent Gates:.....12.3
Bolt Syntax:.....CON Q QN .SC121 C CIN RN SN LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.21	nA
†C_{pd}	2.59	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

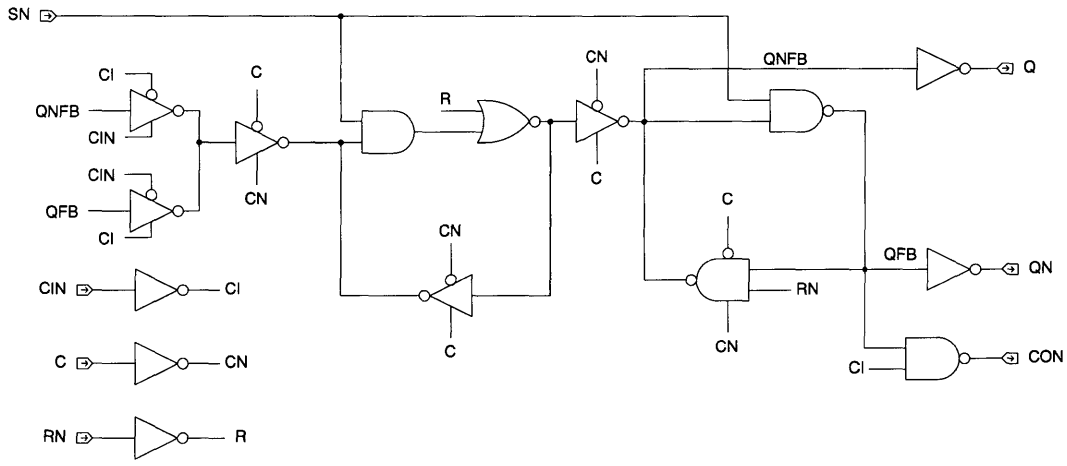
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	3.14 4.68	4.08 4.57	4.04 5.68	5.02 6.78	6.97 8.98
C	QN	t_{PLH} t_{PHL}	7.47 5.79	4.08 4.12	8.37 6.70	9.35 7.69	11.31 9.67
C	CON	t_{PLH} t_{PHL}	7.62 5.94	4.34 4.82	8.57 7.00	9.61 8.16	11.70 10.47
CIN	CON	t_{PLH} t_{PHL}	1.70 1.68	4.34 4.82	2.66 2.74	3.70 3.89	5.78 6.21
RN	Q	t_{PHL}	7.28	4.57	8.28	9.38	11.58
RN	QN	t_{PLH}	10.07	4.08	10.97	11.95	13.91
RN	CON	t_{PLH}	10.21	4.34	11.17	12.21	14.30
SN	Q	t_{PLH}	6.73	4.08	7.62	8.60	10.56

(continued on next page)

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
SN	QN	t_{PHL}	2.84	4.12	3.75	4.74	6.72
SN	CON	t_{PHL}	2.99	4.82	4.05	5.21	7.52
Min C Width	High	t_w	6.58				
Min C Width	Low	t_w	4.02				
Min RN Width	Low	t_w	9.20				
Min SN Width	Low	t_w	5.66				
Min CIN Setup		t_{su}	5.94				
Min CIN Hold		t_h	0.00				
Min RN Setup		t_{su}	2.59				
Min RN Hold		t_h	4.64				
Min SN Setup		t_{su}	2.57				
Min SN Hold		t_h	1.71				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx}C_L)$

Logic Schematic

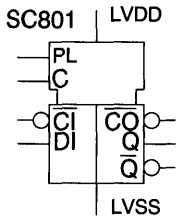


SC801

ABX 3.5 micron CMOS Standard Cells

Description:
SC801 is a static, master-slave, synchronous up-counter bit with ripple carry. The output toggles on the rising edge of the clock when CIN is active low. Parallel load is asynchronous and active high. Outputs are buffered.

Logic Symbol



Truth Table

DI	PL	CIN	C	CON	Q(n+1)	QN(n+1)
X	L	H	↑	-	NC	NC
X	L	L	↑	-	QN(n)	Q(n)
L	H	X	X	-	L	H
H	H	X	X	-	H	L
X	X	H	X	H	-	-
X	X	L	X	QN(n)	-	-

NC=No Change

Pin Loading

	Ci (pF)
DI	0.18
CIN	0.18
C	0.27
PL	0.18

Equivalent Gates:.....16.0
Bolt Syntax:.....CON Q QN .SC801 C CIN DI PL LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	14.73	nA
†C_{pd}	3.28	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
† Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	3.14 4.66	4.09 4.58	4.04 5.67	5.02 6.77	6.99 8.97
C	QN	t_{PLH} t_{PHL}	7.46 5.80	4.09 4.13	8.36 6.71	9.35 7.70	11.31 9.68
C	CON	t_{PLH} t_{PHL}	7.58 5.93	4.36 4.84	8.54 6.99	9.59 8.15	11.68 10.47
DI	Q	t_{PLH} t_{PHL}	8.51 9.69	4.09 4.58	9.41 10.70	10.39 11.80	12.36 14.00
DI	QN	t_{PLH} t_{PHL}	12.49 4.43	4.09 4.13	13.39 5.34	14.37 6.33	16.33 8.31
DI	CON	t_{PLH}	12.61	4.36	13.57	14.61	16.71
PL	Q	t_{PLH} t_{PHL}	8.41 8.87	4.09 4.58	9.31 9.87	10.29 10.98	12.25 13.18

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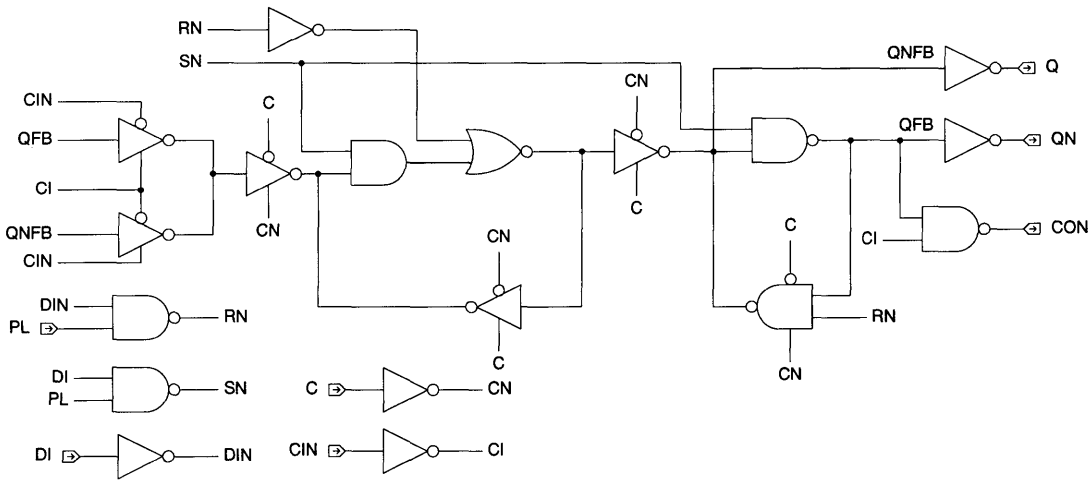
Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
PL	QN	t_{PLH} t_{PHL}	11.66 4.67	4.09 4.13	12.56 5.58	13.55 6.57	15.51 8.55
PL	CON	t_{PLH} t_{PHL}	11.78 4.73	4.36 4.84	12.74 5.79	13.79 6.95	15.88 9.28
CIN	CON	t_{PLH} t_{PHL}	1.69 1.66	4.36 4.84	2.65 2.72	3.70 3.89	5.79 6.21
Min C Width	High	t_w	6.57				
Min C Width	Low	t_w	3.99				
Min CIN Setup		t_{su}	7.16				
Min CIN Hold		t_h	0.00				
Min PL Width	High	t_w	10.80				
Min DI Setup to PL		t_s	1.45				
Min DI Hold to PL		t_h	10.80				

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic

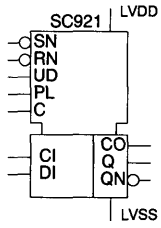


SC921

ABX 3.5 micron CMOS Standard Cells

Description:
SC921 is a static, master-slave, synchronous up/down-counter bit with ripple carry. The output toggles on the rising edge of the clock when CI is active high. SET and RESET are asynchronous and active low. Parallel load is synchronous and active high. Outputs are buffered.

Logic Symbol



Pin Loading

	Ci (pF)
DI	0.08
CI	0.29
C	0.27
PL	0.19
UD	0.17
RN	0.20
SN	0.19

Truth Table

RN	SN	CI	UD	PL	DI	C	CO	Q(n+1)	QN(n+1)
H	H	X	X	H	L	↑	-	L	H
H	H	X	X	H	H	↑	-	H	L
H	H	X	X	X	X	L	-	NC	NC
H	H	L	X	L	X	↑	-	NC	NC
H	H	H	X	L	X	↑	-	QN(n)	Q(n)
L	H	X	X	X	X	X	-	L	H
H	L	X	X	X	X	X	-	H	L
L	L	X	X	X	X	X	-	IL	IL
X	X	L	X	X	X	X	L	-	-
X	X	H	H	X	X	X	Q(n)	-	-
X	X	H	L	X	X	X	QN(n)	-	-

IL = Illegal NC = No Change

Equivalent Gates:.....17.9
Bolt Syntax:.....CO Q QN .SC921 C CI DI PL RN SN UD LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	17.11	nA
†C_{pd}	3.73	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f

†Note: C_{pd} does not include interconnect capacitance.

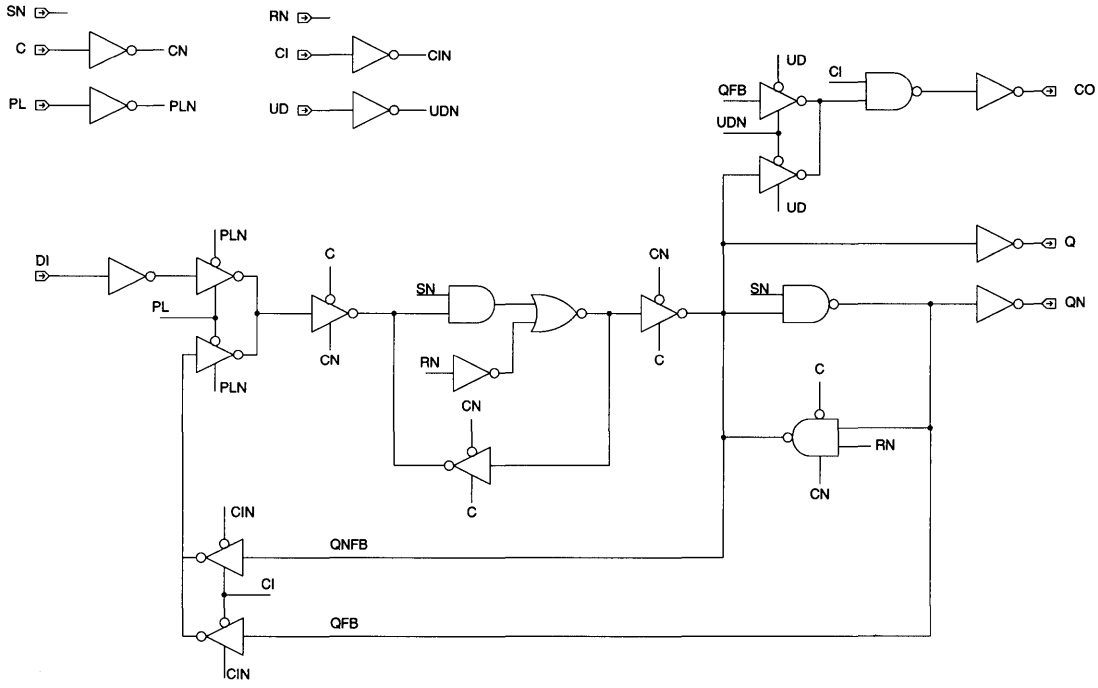
Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
C	Q	t_{PLH} t_{PHL}	3.72 5.46	4.34 4.88	4.68 6.53	5.72 7.70	7.80 10.05
C	QN	t_{PLH} t_{PHL}	8.52 6.61	4.13 4.16	9.43 7.53	10.42 8.53	12.40 10.52
C	CO	t_{PLH} t_{PHL}	6.35 8.29	3.44 3.56	7.11 9.07	7.93 9.93	9.59 11.64
CI	CO	t_{PLH} t_{PHL}	1.48 1.40	3.44 3.56	2.24 2.19	3.07 3.04	4.72 4.75
UD	CO	t_{PLH} t_{PHL}	3.69 3.78	3.44 3.56	4.44 4.56	5.27 5.41	6.92 7.12
RN	Q	t_{PHL}	7.95	4.88	9.03	10.20	12.54
RN	QN	t_{PLH}	11.08	4.13	11.99	12.98	14.96
SN	Q	t_{PHL}	7.18	4.34	8.14	9.18	11.26
SN	QN	t_{PLH}	2.91	4.16	3.83	4.83	6.82
Min C Width	High	t_w	7.70				
Min C Width	Low	t_w	4.34				
Min RN Width	Low	t_w	10.17				
Min SN Width	Low	t_w	6.05				
Min CI Setup		t_{su}	9.02				
Min CI Hold		t_h	0.00				
Min CI Setup to PL		t_s	3.87				
Min DI Setup		t_{su}	7.40				
Min DI Hold		t_h	0.00				
Min DI Setup to PL		t_s	1.51				
Min PL Setup		t_{su}	6.34				
Min PL Hold		t_h	0.00				
Min RN Setup		t_{su}	2.56				
Min RN Hold		t_h	3.15				
Min SN Setup		t_{su}	2.69				
Min SN Hold		t_h	1.87				

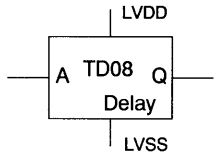
Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

Logic Schematic



Description:
TD08 is a non-inverting time delay.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Ci (pF)
A	0.13

Equivalent Gates:.....3.4
Bolt Syntax:.....Q .TD08 A LVDD LVSS;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85° C)	3.47	nA
†C_{pd}	0.89	pF

Power= (Static I_{DD})(V_{DD}) + C_{pd} V_{DD}^2 f
†Note: C_{pd} does not include interconnect capacitance.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 10.0V, Typical Process

Delay (ns) From	To	Parameter	t_{dx} (ns)	k_{tdx} (ns/pF)	Number of Fan-outs 2 (0.22pF)	4 (0.46pF)	8 (0.94pF)
A	Q	t_{PLH}	7.45	3.88	8.30	9.23	11.09
		t_{PHL}	7.49	3.98	8.36	9.32	11.23

Propagation Delay Equation: $t_p(C_L) = K_P K_V K_T(t_{dx} + k_{tdx} C_L)$

SECTION 13
ABX RAM/ROM DATA SHEETS

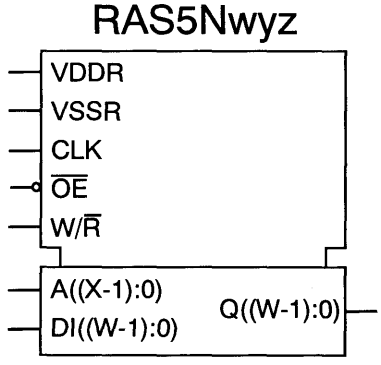
RAS5Nwyz Static RAM

ABX CMOS N-Well Process Family

Features

- 17.84 nsec typical cycle time for a 32 x 4 RAM with a 0.5pF load.
- Read-Modify-Write cycle possible.
- Low standby power when the clock is stopped.
- Separate input and output ports with full parallel access.
- 3-State outputs interface internal data buses directly.
- Precharged design for faster operation with less silicon area.

FIGURE 1: LOGIC SYMBOL



NOTES:
1: A0 is the LSB.
2: X represents the number of address lines.
3: Power supply voltages VDDR and VSSR are pinned out.

General Description

This series of 1.5μm double-metal MxN RAMs operates within a power supply voltage range of 4.5V to 5.5V. The RAS5N series has 3-state outputs with active low Output Enable Not (OEN). The circuit is precharged when the clock is high, and the read and write operations occur when the clock is low. The outputs become valid a short time after the falling edge of the clock and stay valid until the next falling edge of the clock. The address lines are latched on the falling edge of the clock. The clock is used only to precharge the circuit and operate the latches; the memory does not need a refresh signal. The clock and all of the other inputs can be held stable indefinitely with no loss of memory as long as power is supplied to the RAM.

Within limits specified below, the user has flexibility in specifying the logical size of the RAM, including both word size and number of address locations. Within the name shown above, the "wyz" represents a three character sequence assigned to each RAM configuration which uniquely identifies that particular configuration. Furthermore, the "S", "5", and "N" represent a single port RAM, version 5, and an active low output enable respectively. The "w" signifies the word-length in a mod-36 alpha-numeric digit using the integers 1-9 and letters A-Z excluding O, Q, and V. For example, "N" represents a word-length of 23 and "P" represents a word-length of 24. The "yz" represents a hexadecimal value for the number of address locations divided by 16. For example, "04" represents 64 address locations.

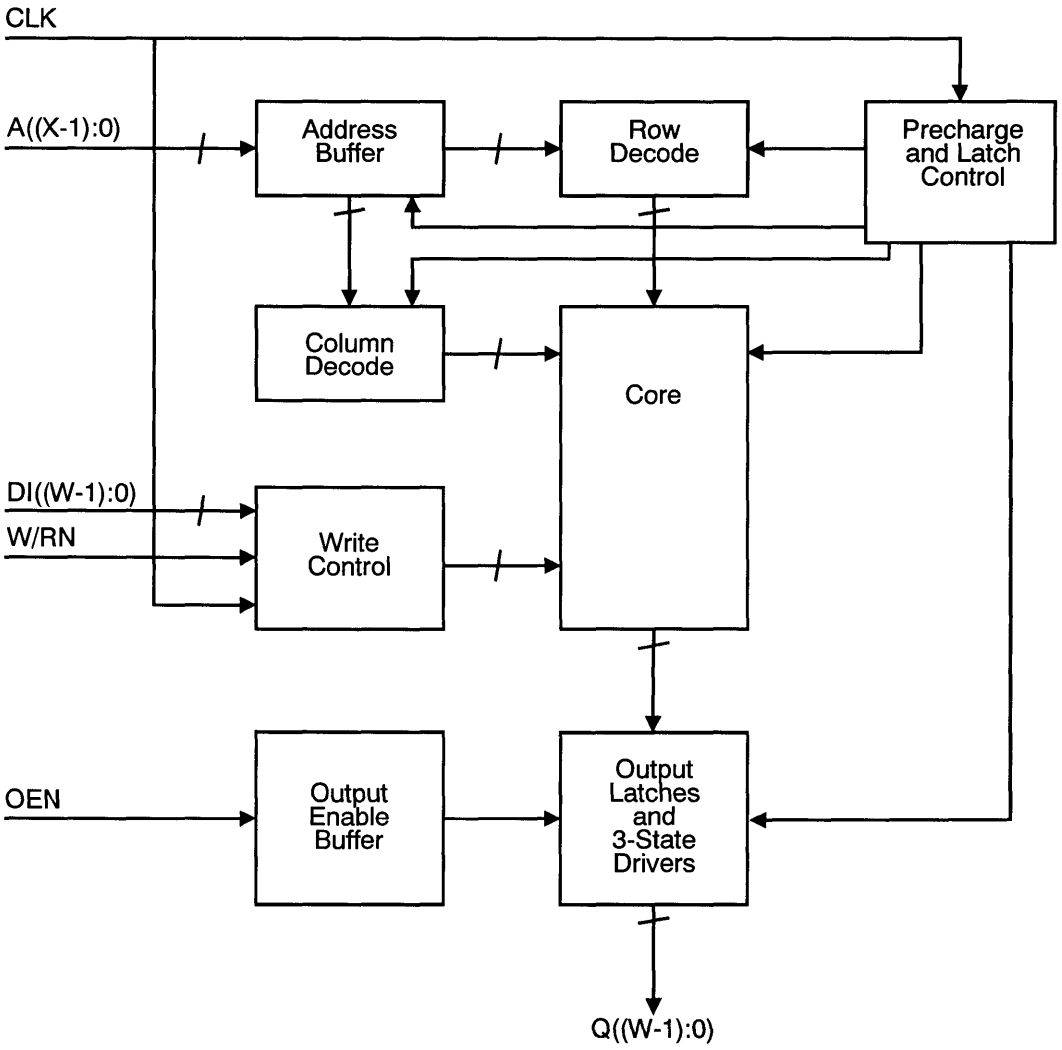
In the logic symbol of figure 1, the "X" denotes the number of address lines. This value can be calculated by taking the log to the base 2 of the number of address locations. If the value returned is not an integer, round up. For example, for 64 address locations, "X" would be 6; for 80 address locations, "X" would be 7.

The power supply connections are pinned out as VDDR and VSSR. A quiet bus of P+ guard ring surrounds the RAM and should be tied to VSSR for 5V usage only. For 10V operation, see the AMI application note titled "Using the 5 Volt ABO RAM with 10 Volt Standard Cells."

Performance data is listed below for two example sizes. To obtain data and a workstation installation (symbol and simulation model) for a specific size, contact the factory.

ABX CMOS N-Well Process Family

FIGURE 2: M X N RAM BLOCK DIAGRAM



Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Address Inputs	5	10	1 (A0 is the LSB)
Word Size (Data Outputs)	1 bit	32 bits	1 bit
Address Locations (Words)	32	1024 (1K)	16
Total Bits In Core (Word Size Times Address Locations)	32	32,768 (32K)	

Pin Description and Input Capacitance

SIGNAL	TYPE	32 X 4	1K X 16	SIGNAL DESCRIPTIONS
Ai	Input	0.14pF	0.14pF	Address Inputs
CLK	Input	0.33pF	0.62pF	Clock Input
OEN	Input	0.20pF	0.43pF	3-State Output Control
Qi (High-Z)	Output	0.14pF	0.14pF	Data Outputs
W/RN	Input	0.08pF	0.08pF	Write/Read Not Control
Dli	Input	0.10pF	0.10pF	Data Inputs

Contact the factory to obtain capacitance information for MXN RAM.

Area relative to a 10 Volt 2 Input Nand
32 x 4: 307
1K x 16: 9517

Bolt Syntax:

Qw. . . Q1 Q0 .RAS5Nwyz Ax . . .A1 A0 CLK Dlw . . . DI1 DI0 OEN WRN VDDR VSSR;

Note: A0 is the LSB

AC Characteristics: t(CL) = tdx + Ktdx * CL

The data in the following examples are specified at 5.OV, Tj = 25°C, and typical process performance parameters Performance at other operating points may be estimated by use of the Voltage, Process, and Temperature derating curves. Contact the factory to obtain the AC characteristics and input capacitance for different logical sizes of RAMs.

ABX CMOS N-Well Process Family

32 X 4

CHARACTERISTIC	SYMBOL	tdx (ns)	ktdx (ns/pF)	t(0.5pF) (ns)
Min CLK Period Read	tclkr	17.20		
Min CLK Period Write	tclkw	12.15		
Min CLK Width High	twch	4.62		
Min CLK Width Low During Read	twclr	12.58		
Max CLK Low To Q Delay	tpcq	12.58	1.27	13.22
Max OEN To Q Delay	toenq	1.31	1.27	1.95
Max OEN To High-Z Delay	toenz	1.00		
Min Address Setup Time**	tasu	2.26		
Min Address Hold Time**	tah	1.49		
Min W/RN High To Valid Write*	twvw	5.26		
Min Data In (DI) Stable To Valid Write*	tdvw	5.24		
Min CLK Low To Valid Write*	tcvw	7.53		
Min Data In (DI) Hold Time After Rising Edge Of CLK When W/RN Is High*	tdh	1.75		
Min W/RN Hold Time After Read	twh	0.43		
Min Q Hold Time	tqh	1.53		

1K x 16

CHARACTERISTIC	SYMBOL	tdx (ns)	ktdx (ns/pF)	t(0.5pF) (ns)
Min CLK Period Read	tclkr	39.19		
Min CLK Period Write	tclkw	27.21		
Min CLK Width High	twch	11.09		
Min CLK Width Low During Read	twclr	28.10		
Max CLK Low To Q Delay	tpcq	28.10	1.35	28.78
Max OEN To Q Delay	toenq	1.46	1.35	2.14
Max OEN To High-Z Delay	toenz	1.09		
Min Address Setup Time**	tasu	2.91		
Min Address Hold Time**	tah	1.87		
Min W/RN High To Valid Write*	twvw	13.39		
Min Data In (DI) Stable To Valid Write*	tdvw	12.76		
Min CLK Low To Valid Write*	tcvw	16.12		
Min Data In (DI) Hold Time After Rising Edge Of CLK When W/RN Is High*	tdh	2.47		
Min W/RN Hold Time After Read	twh	0.41		
Min Q Hold Time	tqh	1.73		

* If the W/RN line is high at the same time that the CLK line is low, all three timing terms twvw, tdvw, and tcvw must be met or else invalid data may be written into the RAM. A Read-Modify-Write cycle may be executed by leaving W/RN low until the read is accomplished, then meeting the twvw, tdvw, and tcvw timing terms to accomplish a valid write. The Q outputs will change to the value that is written. After a write, the Data In (DI) pins must be held stable until after W/RN falls or CLK rises.

** If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it will not show corrupted data.

Power Dissipation

PARAMETER	32 X 4	1K X 16
Typical C_{pd} (Equivalent Power Dissipation Capacitance (pF))	34	251
Typical Static IDD Tj = 85° (μA)	0.34	5

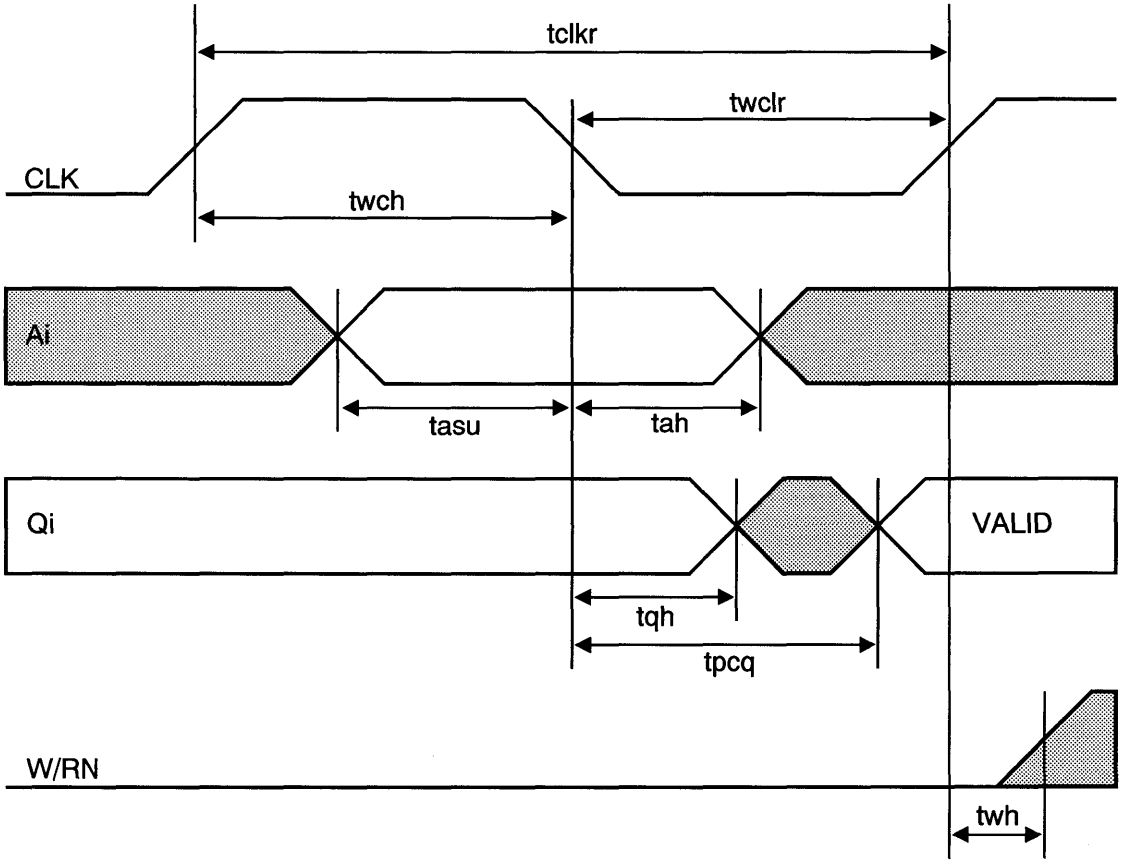
Testing Notes:

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. For a more detailed description of the testing of memory elements in ICs, refer to the RAM testing application notes.

ABX CMOS N-Well Process Family

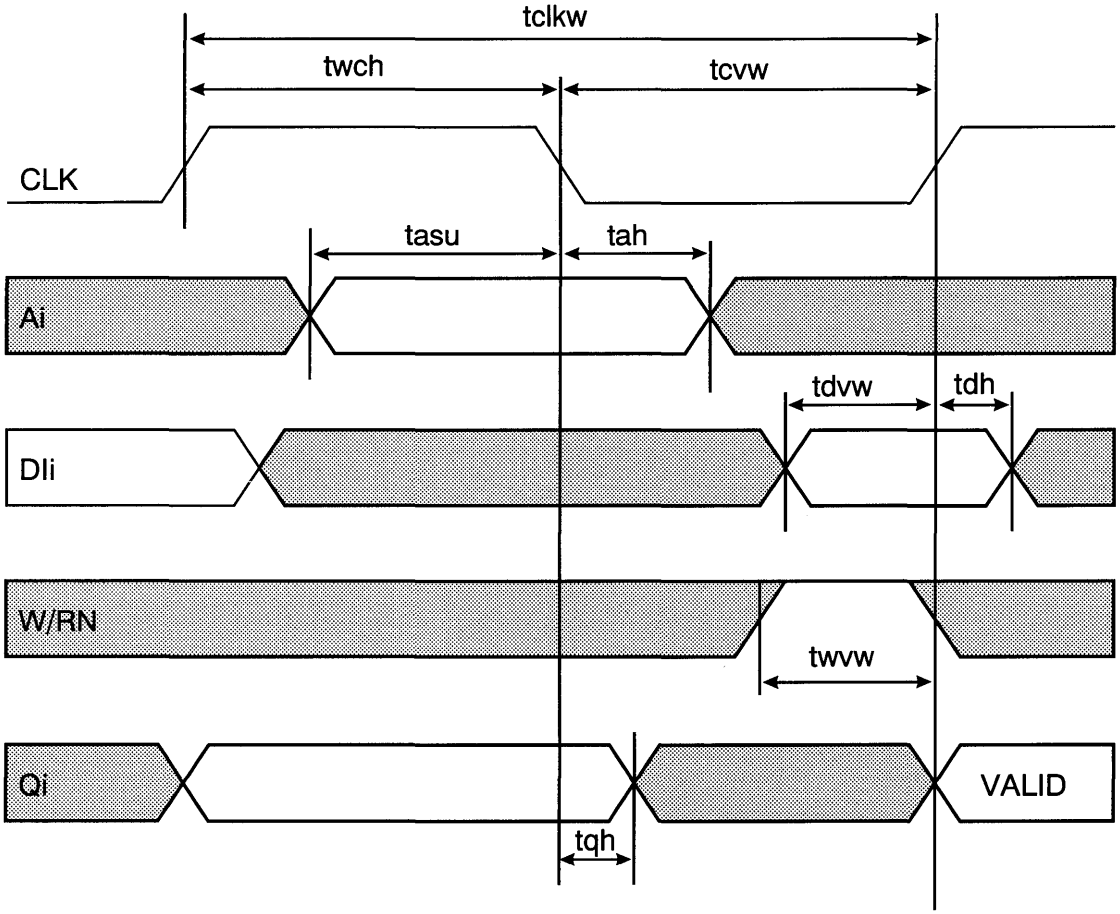
M X N RAM
Timing Diagram

Read cycle



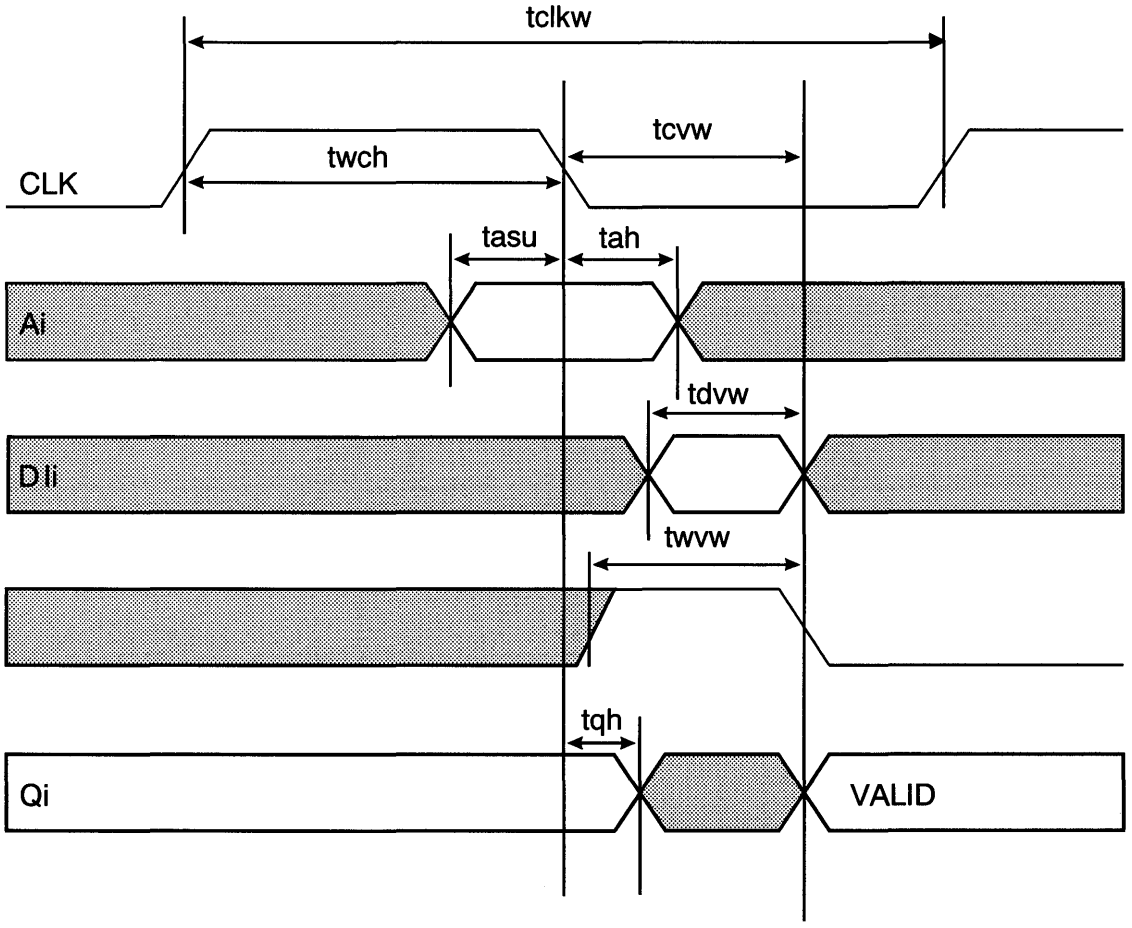
M X N RAM
Timing Diagram

Write Cycle 1 (See Notes 1 and 2)



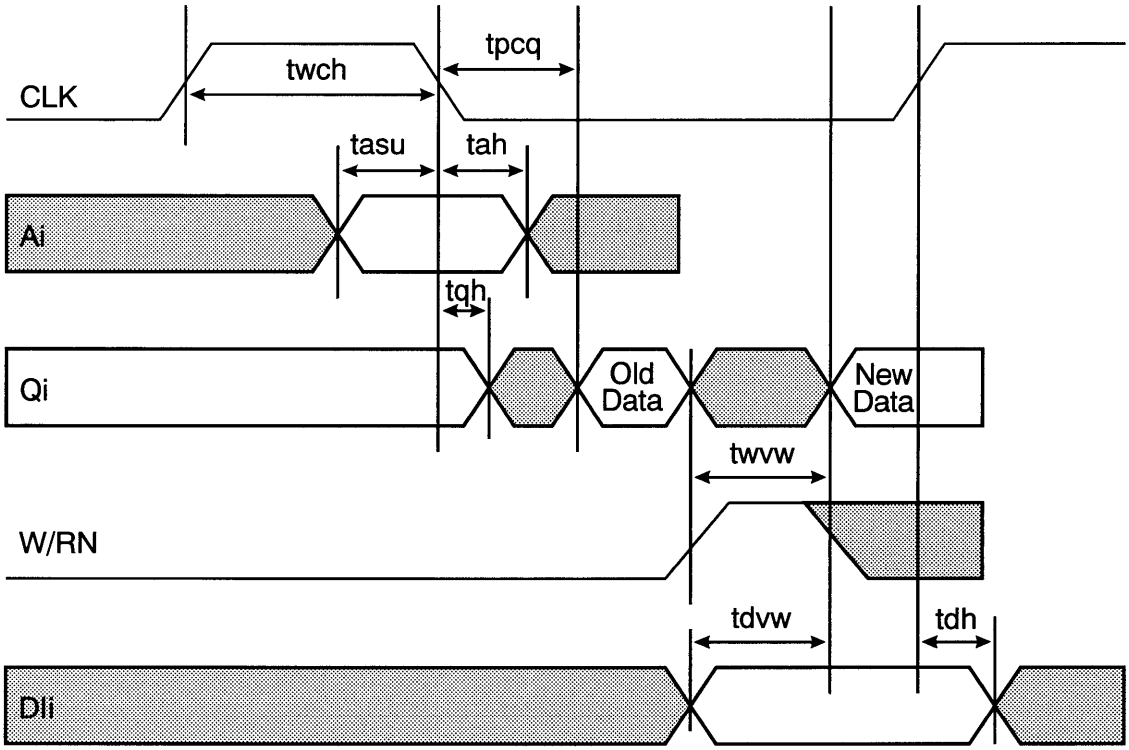
M X N RAM
Timing Diagram

Write Cycle 2 (See Notes 1 and 3)



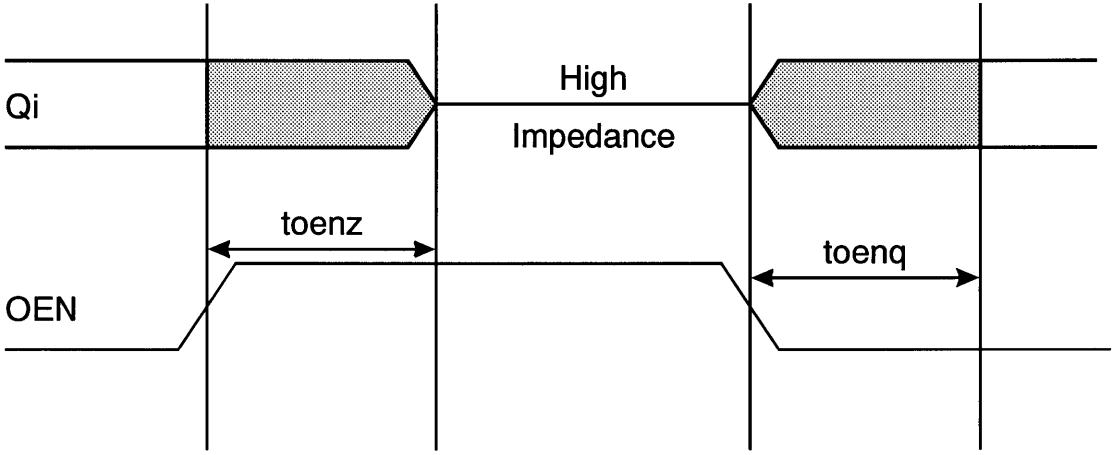
M X N RAM
Timing Diagram

Read-Modify-Write Cycle (See Note 4)



ABX CMOS N-Well Process Family

3-State Control Timing



Timing Diagram Notes

1. During a write cycle, the data that is written in becomes valid at the Q outputs as soon as the tcvw, tdvw, and twvw timing terms are met. The clock does not have to rise, and the W/RN signal does not have to fall first.
2. The data hold time in write cycle 1 is referenced to the rising edge of CLK when W/RN is held high.
3. The data hold time in write cycle 2 is referenced to the falling edge of W/RN and is equal to zero.
4. The data hold time in the Read-Modify-Write cycle has to be met only when W/RN is held high.

FIGURE 3: LOGIC SYMBOL

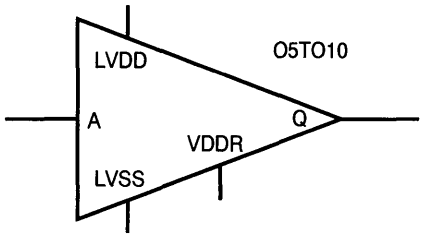


FIGURE 4: TRUTH TABLE

A	Q
VDDR (0V)	LVDD (5V)
LVSS (-5V)	LVSS (-5V)

The O5TO10 5V to 10V level shifter is used to take an output differential of 5V from the RAM to a differential output voltage range of 10V. This was designed to allow a 5V RAM to operate in a 10V circuit.

In the logic symbol of Figure 3, LVDD, LVSS, and VDDR are pinned out and must be connected to the correct supplies. LVDD is the +5V positive supply, VDDR is the RAM positive supply (equal to LVSS+5V), and LVSS is the -5V negative supply voltage.

The O5TO10 level shifter cell is designed to abut next to regular standard cells in a row. The LVDD, LVSS, and SUB supplies will connect by abutment while the VDDR supply is an input signal pin. For more information, refer to the AMI application note titled "Using the 5 Volt ABO RAM with 10 Volt Standard Cells."

The logic operations of the O5TO10 level shifter are shown in the truth table of Figure 4.

Operating Ranges

DESCRIPTION	NAME	VOLTAGE LEVEL
Digital Positive Supply	LVDD	+5V
Digital And RAM Negative Supply	LVSS	-5V
RAM Positive Supply	VDDR	OV
Quiet Substrate Bus	SUB	LVSS

Area Relative to 10V 2 input NAND: 3.98.
Input Capacitance: 0.166pF.
Bolt Syntax: Q .05TO10 A LVDD LVSS VDDR;

AC Characteristics

CHARACTERISTIC	SYMBOL	tdx	Ktdx	t(0.5pF)
Maximum Input To Q Delay	tpdr	2.03 ns	4.88 ns/pF	4.47 ns
	tpdf	3.77 ns	2.47 ns/pF	5.01 ns

t(CL) = tdx + Ktdx *CL
Tj = 25°C
LVDD - LVSS = 10V
VDDR - LVSS = 5V
Typical Process

O10TO5
Level Shifter

ABX CMOS N-Well Process Family

FIGURE 5: LOGIC SYMBOL

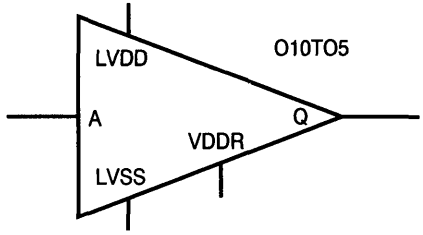


FIGURE 6: TRUTH TABLE

A	Q
LVDD (5V)	VDDR (0V)
LVSS (-5V)	LVSS (-5V)

The O10TO5 10V to 5V level shifter is used to take a differential input voltage range of 10V and convert it to a 5V differential for RAM operation. This was designed to allow a 5V RAM to operate in a 10V circuit.

In the logic symbol of Figure 5, LVDD, LVSS, and VDDR are pinned out and must be connected to the correct supplies. LVDD is the +5V positive supply, VDDR is the RAM positive supply (equal to LVSS+5V), and LVSS is the -5V negative supply voltage.

The O10TO5 level shifter cell is designed to abut next to regular standard cells in a row. The LVDD, LVSS, and SUB supplies will connect by abutment while the VDDR supply is an input signal pin. For more information, refer to the AMI application note titled "Using the 5 Volt ABO RAM with 10 Volt Standard Cells."

The logic operations of the O10TO5 level shifter are shown in the truth table of Figure 6.

Operating Ranges

DESCRIPTION	NAME	VOLTAGE LEVEL
Digital Positive Supply	LVDD	+5V
Digital And RAM Negative Supply	LVSS	-5V
RAM Positive Supply	VDDR	OV
Quiet Substrate Bus	SUB	LVSS

Area Relative to 10V 2 input NAND: 2.79.
Input Capacitance: 0.098pF.
Bolt Syntax: Q .010TO5 A LVDD LVSS VDDR;

AC Characteristics

CHARACTERISTIC	SYMBOL	tdx	Ktdx	t(0.5pF)
Maximum Input To Q Delay	tpdr	0.59 ns	4.78 ns/pF	2.98 ns
	tpdf	2.19 ns	2.65 ns/pF	3.52 ns

t(CL) = tdx + Ktdx *CL
Tj = 25°C
LVDD - LVSS = 10V
VDDR - LVSS = 5V
Typical Process

Using The 5 Volt ABO RAM With 10 Volt Standard Cells

The RAS5Nwyz RAM is intended for use with 4.5 volt to 5.5 volt power supplies and pin voltages; however, it can be used with AMI's ABOHS 10 volt standard cell library as outlined in this application note. For further information, see the data sheets for the RAS5Nwyz RAM, the O5TO10 level shifter cell, and the O10TO5 level shifter cell.

The following description assumes the RAM is connected to a power supply with a -5 volt to 0 volt potential, while the standard cells (SC) are connected to a power supply with a -5 volt to +5 volt potential. The level shifters (LS) interface the RAM to the standard cells and are designed to abut to regular standard cells in a row of cells.

The power connections are as follows:

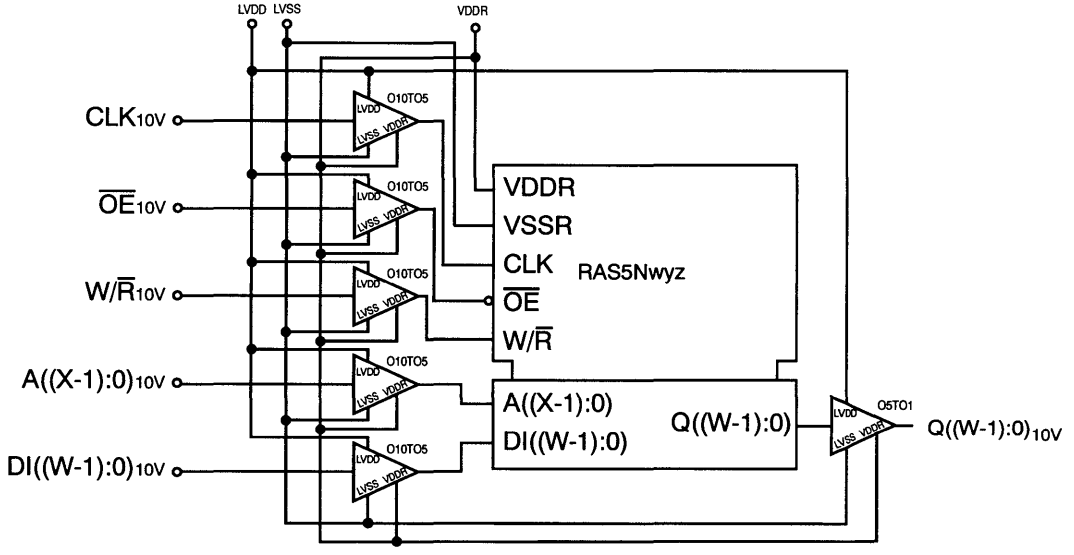
SUB = -5V	Quiet substrate connection (RAM, SC, and LS)
LVDD = +5V	SC and LS positive supply
VDDR = 0V	RAM positive supply and LS reference voltage
LVSS = -5V = VSSR	RAM, SC and LS negative supply

SUB is a global (external) connection to all the cells. VDDR is connected to the level shifters like an input signal: it is a pin on the layout and in the netlist. The rest of the power signals connect like power busses in the layout, but are pinned out like signals in the netlist and schematic symbol.

When the RAS5Nwyz RAM is used with 10 volt standard cells, every RAM input must have an O10TO5 level shifter cell connected to it, and every RAM output must have an O5TO10 level shifter cell connected to it. The power supplies must be connected as shown below in Figure 7.

The Cell Development Engineering Group will assemble the RAM and level shifters into a softcell netlist if requested to do so. The new softcell will be called RASHNwyz to distinguish it as having 10 volt inputs and outputs.

FIGURE 7: RASHNwyz SOFTCELL



RO4cwxyz, RO6cwxyz Synchronous ROM

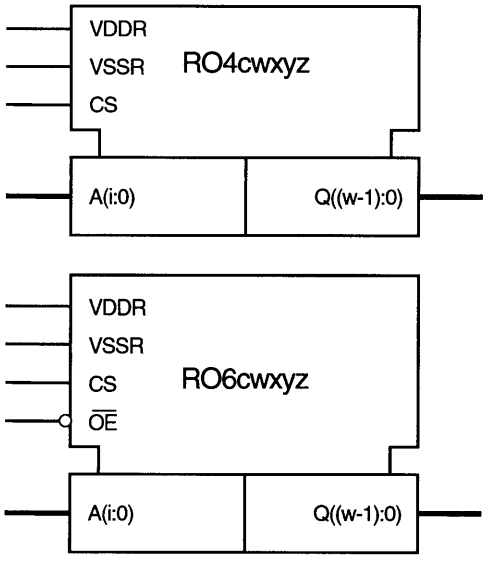
Preliminary

ABX CMOS N-Well Process Family

Features

- Low standby power when chip-select is stopped.
- Buffered or 3-state outputs. 3-state outputs are active low enable.
- Pre-charged design for lower power consumption.

FIGURE 1: LOGIC SYMBOL



General Description

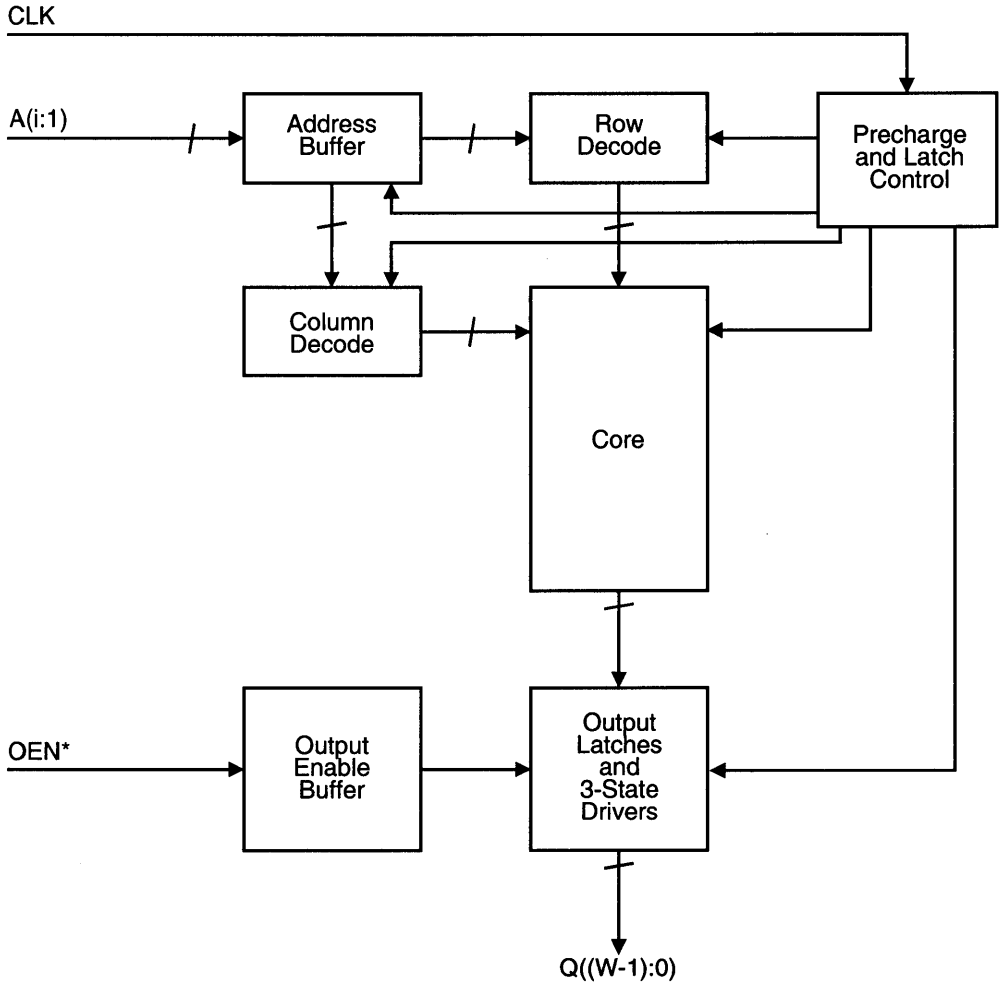
This series of double-metal MxN ROMs operates within a power supply voltage range of 4.5V to 5.5V. (It will operate at 2.5V with lower performance.) The RO4 series has always-active outputs. The RO6 series has 3-state outputs with active low Output Enable Not (OEN). The circuit is precharged when the chip-select (CS) line is low, and the read operation occurs when the chip-select (CS) is high. The outputs become valid a short time after the rising edge of the chip-select and are latched on the falling edge of the chip-select, keeping the outputs valid until the next rising edge of the chip-select. The address lines are latched on the rising edge of chip-select.

Within limits specified below, the user has flexibility in specifying the logical size of the ROM, including both word-size and number of address locations. Within the name as shown above, the "cwxyz" represents a five character sequence assigned to each ROM configuration which uniquely identifies that particular configuration. The "c" represents the number column address lines, which is limited to 3, 4, or 5. The "w" represents the word-length in a mod-36 alpha-numeric digit using the integers 1-9 and the letters A-Z, excluding O, Q, and V. For example, "N" represents a word-length of 23 and "P" represents a word-length of 24. The "xyz" represents a hexadecimal value for the number of address locations divided by 16. For example, "00C" represents 192 address locations. The columns are represented because the ROM can be built using different aspect ratios, i.e., rows vs. columns.

The power supply connections are pinned out as VDDR and VSSR. A quiet bus of P+ guard ring surrounds the ROM and should be tied to VSSR for 5V only usage. For operation on 10V chips, see the AMI application note titled "RAS5Nwyz RAM Application Note - Using The 5 Volt ABO RAM with 10 Volt Standard Cells." This application note applies to ROMs as well as RAMs. Be sure to get the N-Well version of this application note.

Performance data is listed below for an example size. To obtain data and a workstation installation (symbol and simulation model) for a particular size, contact the factory.

FIGURE 2: ROM BLOCK DIAGRAM



*For RO4 series, OEN input is removed and output driver is never High – Z.
*For RO6 series, as shown.

Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Address Inputs	6	14	1
Word Size (Data Outputs)	1	32	1
Address Locations	64	16,384 (16K)	64
Total Bits In Core (Word Size Times Address Locations)	64	524,288 (512K)	

Pin Description and Input Capacitance

SIGNAL	TYPE	256 X 16	SIGNAL DESCRIPTIONS
Ai	Input	TBD	Address Inputs
CS	Input	TBD	Chip-Select
OEN	Input	TBD	3-State Output Control
Q(High–Z)	Output	TBD	Data Outputs

AC Characteristics for 256 X 16

CHARACTERISTIC	SYMBOL	tdx(ns)	ktdx(ns/pF)	t(0.5pF)(ns)
Max CS To Q Delay	tpcsq	TBD	TBD	TBD
Max OEN To Q Delay	tpoenq	TBD	TBD	TBD
Max OEN To High – Z Delay	tpoenz	TBD		
Min Address Setup Time	tasu	TBD		
Min Address Hold Time	tah	TBD		
Min CS Width Low	twcsl	TBD		
Min CS Width High	twcsh	TBD		
Min Q Hold Time	tqh	TBD		

ABX CMOS N-Well Process Family

Preliminary

Power Dissipation

PARAMETER	256 X 16
Typical C_{pd} (Equivalent Power Dissipation Capacitance (pF))	TBD
Typical Static IDD Tj=85°C(μA)	TBD

Area Relative to a 2 Input Nand: 256 x 16 : TBD

Bolt Syntax:

Qw ... Q1 Q0 .R04cwxyz Ai ... A1 A0 CS VDDR VSSR;
Qw ... Q1 Q0 .R06cwxyz Ai ... A1 A0 CS VDDR VSSR;

A0 is the LSB

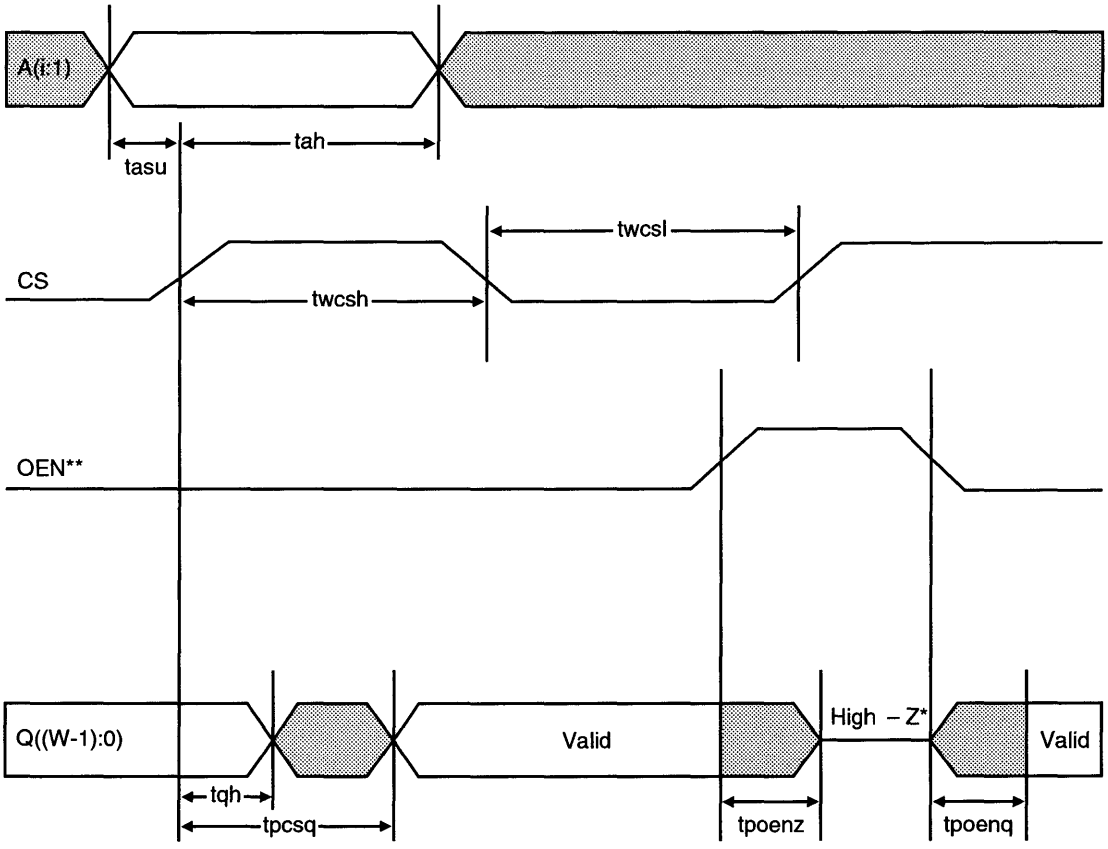
AC Characteristics:t(CL)=tdx+Ktdx*CL

The data in the example above is specified at 5.0V, Tj=25°C, and typical process parameters. Performance at other operating points may be estimated by use of the Voltage, Process, and Temperature derating curves. Contact the factory to obtain the ac characteristics and input capacitance for different logical sizes of ROMs.

Testing Notes:

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. For a more detailed description of the testing of memory elements in ICs, refer to the ROM testing application notes.

M X N ROM Timing Diagram



*High – Z= High Impedance Q Output

**For RO4 series, OEN is not applicable and the Q((W-1):0) is never High – Z.
For RO6 series, as shown.

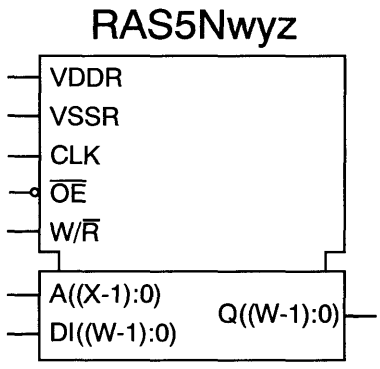
RAS5Nwyz Static RAM

ABX CMOS P-Well Process Family

Features

- 17.86 nsec typical cycle time for a 32 x 4 RAM with a 0.5pF load.
- Read-Modify-Write cycle possible.
- Low standby power when the clock is stopped.
- Separate input and output ports with full parallell access.
- 3-State outputs interface internal data buses directly.
- Precharged design for faster operation with less silicon area.

FIGURE 1: LOGIC SYMBOL



NOTES:
1: A0 is the LSB.
2: X represents the number of address lines.
3: Power supply voltages VDDR and VSSR are pinned out.

General Description

This series of 1.5μm double-metal MxN RAMs operates within a power supply voltage range of 4.5V to 5.5V. The RAS5N series has 3-state outputs with active low Output Enable Not (OEN). The circuit is precharged when the clock is high, and the read and write operations occur when the clock is low. The outputs become valid a short time after the falling edge of the clock and stay valid until the next falling edge of the clock. The address lines are latched on the falling edge of the clock. The clock is used only to precharge the circuit and operate the latches; the memory does not need a refresh signal. The clock and all of the other inputs can be held stable indefinitely with no loss of memory as long as power is supplied to the RAM.

Within limits specified below, the user has flexibility in specifying the logical size of the RAM, including both word size and number of address locations. Within the name shown above, the "wyz" represents a three character sequence assigned to each RAM configuration which uniquely identifies that particular configuration. Furthermore, the "S", "5", and "N" represent a single port RAM, version 5, and an active low output enable respectively. The "w" signifies the word-length in a mod-36 alpha-numeric digit using the integers 1-9 and letters A-Z excluding O, Q, and V. For example, "N" represents a word-length of 23 and "P" represents a word-length of 24. The "yz" represents a hexadecimal value for the number of address locations divided by 16. For example, "04" represents 64 address locations.

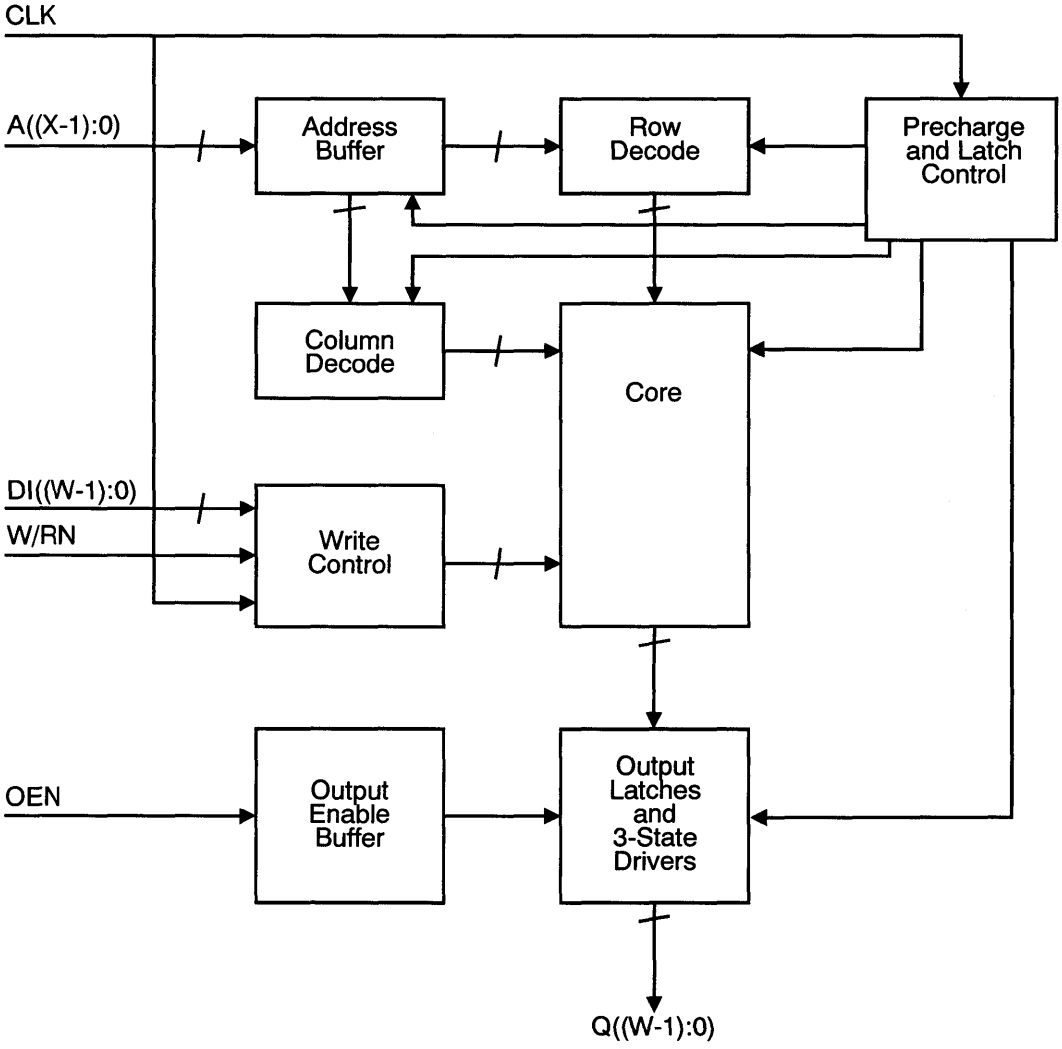
In the logic symbol of figure 1, the "X" denotes the number of address lines. This value can be calculated by taking the log to the base 2 of the number of address locations. If the value returned is not an integer, round up. For example, for 64 address locations, "X" would be 6; for 80 address locations, "X" would be 7.

The power supply connections are pinned out as VDDR and VSSR. A quiet bus of N+ guard ring surrounds the RAM and should be tied to VDDR for 5V usage only. For 10V operation, see the AMI application note titled "Using the 5 Volt ABE RAM with 10 Volt Standard Cells."

Performance data is listed below for two example sizes. To obtain data and a workstation installation (symbol and simulation model) for a specific size, contact the factory.

ABX CMOS P-Well Process Family

FIGURE 2: M X N RAM BLOCK DIAGRAM



Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Address Inputs	5	10	1 (A0 is the LSB)
Word Size (Data Outputs)	1 bit	32 bits	1 bit
Address Locations (Words)	32	1024 (1K)	16
Total Bits In Core (Word Size Times Address Locations)	32	32,768 (32K)	

Pin Description and Input Capacitance

SIGNAL	TYPE	32 X 4	1K X 16	SIGNAL DESCRIPTIONS
Ai	INPUT	0.14pF	0.14pF	Address Inputs
CLK	INPUT	0.33pF	0.62pF	Clock Input
OEN	INPUT	0.20pF	0.43pF	3-State Output Control
Qi (High-Z)	OUTPUT	0.14pF	0.14pF	Data Outputs
W/RN	INPUT	0.08pF	0.08pF	Write/Read Not Control
Dli	INPUT	0.10pF	0.10pF	Data Inputs

Contact the factory to obtain capacitance information for MXN RAM.

Area relative to a 10 Volt 2 Input Nand
32 x 4: 325
1K x 16: 9601

Bolt Syntax:

Qw. . . Q1 Q0 .RAS5Nwyz Ax . . .A1 A0 CLK Dlw . . . Dl1 Dl0 OEN WRN VDDR VSSR;
A0 is the LSB

AC Characteristics: t(CL) = tdx + Ktdx * CL

The data in the following examples are specified at 5.OV, Tj = 25° C, and typical process performance parameters. Performance at other operating points may be estimated by use of the Voltage, Process, and Temperature derating curves. Contact the factory to obtain the AC characteristics and input capacitance for different logical sizes of RAMs.

ABX CMOS P-Well Process Family

32 X 4

CHARACTERISTIC	SYMBOL	tdx (ns)	ktdx (ns/pF)	t(0.5pF) (ns)
Min CLK Period Read	tclkr	17.22		
Min CLK Period Write	tclkw	12.19		
Min CLK Width High	twch	4.63		
Min CLK Width Low During Read	twclr	12.59		
Max CLK Low To Q Delay	tpcq	12.59	1.27	13.23
Max OEN To Q Delay	toenq	1.30	1.27	1.94
Max OEN To High-Z Delay	toenz	0.99		
Min Address Setup Time**	tasu	2.26		
Min Address Hold Time**	tah	1.49		
Min W/RN High To Valid Write*	twvw	5.25		
Min Data In (DI) Stable To Valid Write*	tdvw	5.24		
Min CLK Low To Valid Write*	tcvw	7.56		
Min Data In (DI) Hold Time After Rising Edge Of CLK When W/RN Is High*	tdh	1.75		
Min W/RN Hold Time After Read	twh	0.43		
Min Q Hold Time	tqh	1.53		

* If the W/RN line is high at the same time that the CLK line is low, all three timing terms twvw, tdvw, and tcvw must be met or else invalid data may be written into the RAM. A Read-Modify-Write cycle may be executed by leaving W/RN low until the read is accomplished, then meeting the twvw, tdvw, and tcvw timing terms to accomplish a valid write. The Q outputs will change to the value that is written. After a write, the Data In (DI) pins must be held stable until after W/RN falls or CLK rises.

** If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it will not show corrupted data.

1K x 16

CHARACTERISTIC	SYMBOL	tdx (ns)	ktdx (ns/pF)	t(0.5pF) (ns)
Min CLK Period Read	tclkr	39.14		
Min CLK Period Write	tclkw	27.21		
Min CLK Width High	twch	11.09		
Min CLK Width Low During Read	twclr	28.05		
Max CLK Low To Q Delay	tpcq	28.05	1.35	28.72
Max OEN To Q Delay	toenq	1.47	1.35	2.15
Max OEN To High - Z Delay	toenz	1.09		
Min Address Setup Time**	tasu	2.91		
Min Address Hold Time**	tah	1.87		
Min W/RN High To Valid Write*	twvw	13.33		
Min Data In (DI) Stable To Valid Write*	tdvw	12.79		
Min CLK Low To Valid Write*	tcvw	16.12		
Min Data In (DI) Hold Time After Rising Edge Of CLK When W/RN Is High*	tdh	2.47		
Min W/RN Hold Time After Read	twh	0.41		
Min Q Hold Time	tqh	1.73		

* If the W/RN line is high at the same time that the CLK line is low, all three timing terms twvw, tdvw, and tcvw must be met or else invalid data may be written into the RAM. A Read-Modify-Write cycle may be executed by leaving W/RN low until the read is accomplished, then meeting the twvw, tdvw, and tcvw timing terms to accomplish a valid write. The Q outputs will change to the value that is written. After a write, the Data In (DI) pins must be held stable until after W/RN falls or CLK rises.

** If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it will not show corrupted data.

Power Dissipation

PARAMETER	32 X 4	1K X 16
Typical C_{pd} (Equivalent Power Dissipation Capacitance (pF))	34	251
Typical Static IDD Tj = 85° (μA)	0.34	5

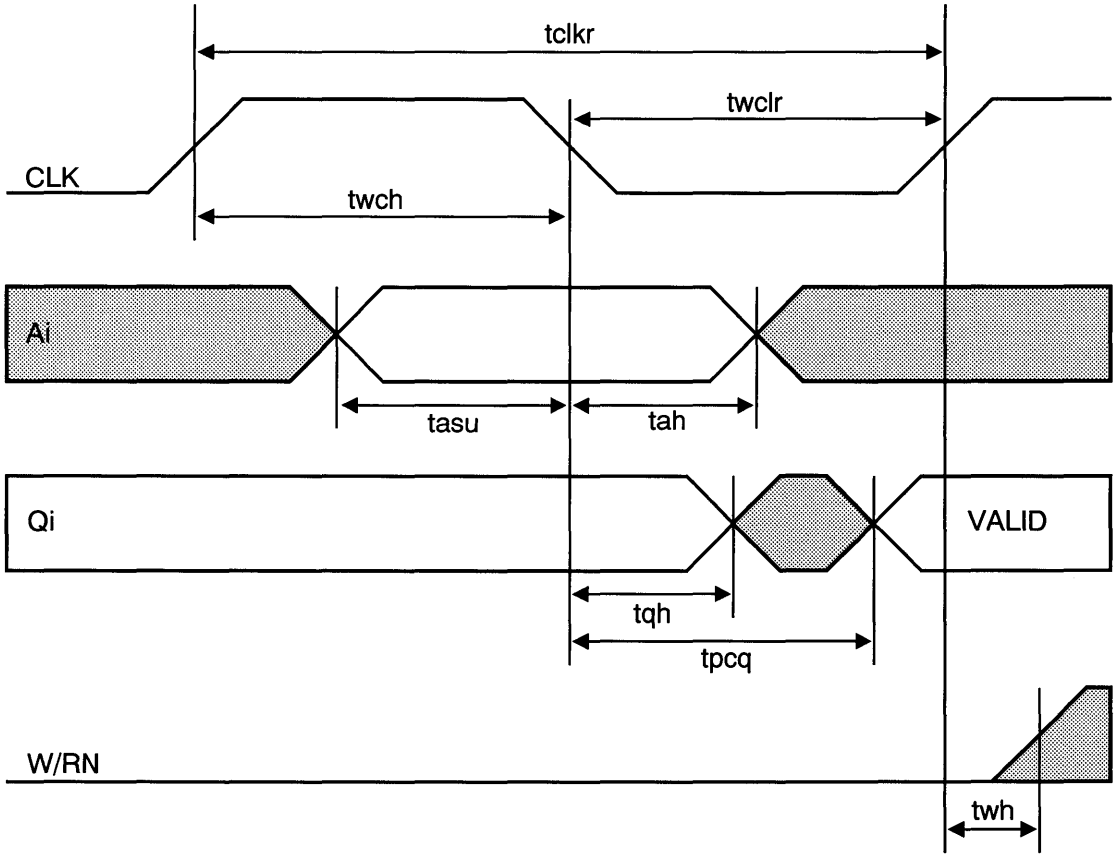
Testing Notes

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. For a more detailed description of the testing of memory elements in ICs, refer to the RAM testing application notes.

ABX CMOS P-Well Process Family

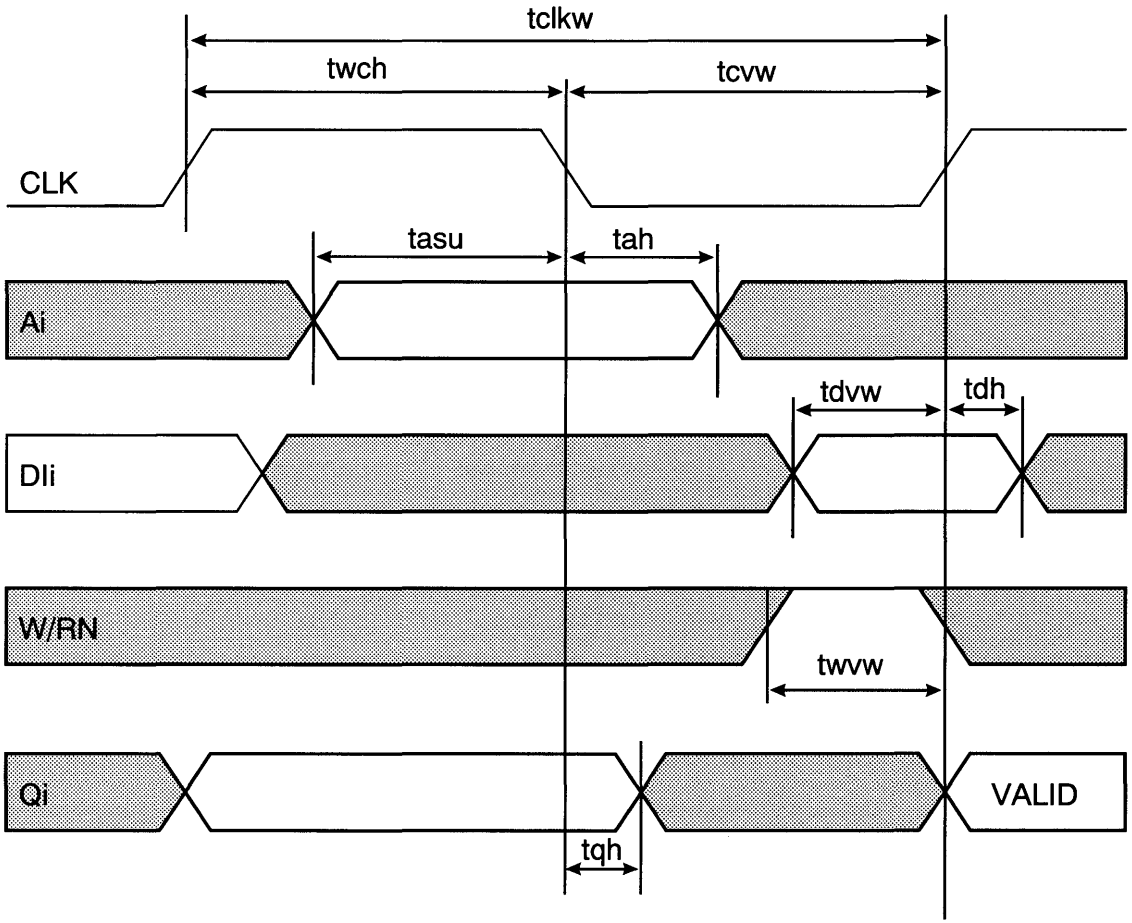
M X N RAM
Timing Diagram

Read cycle



M X N RAM
Timing Diagram

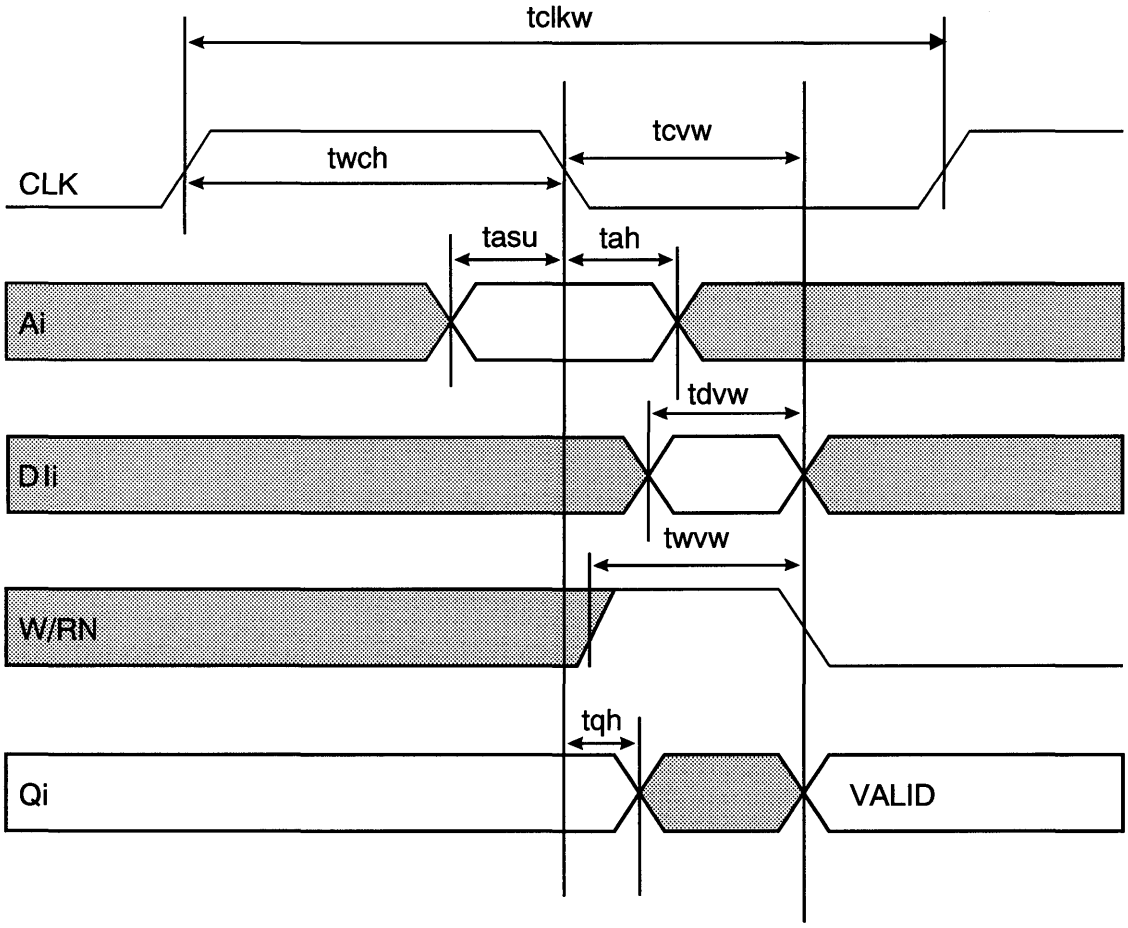
Write Cycle 1 (See Notes 1 and 2)



ABX CMOS P-Well Process Family

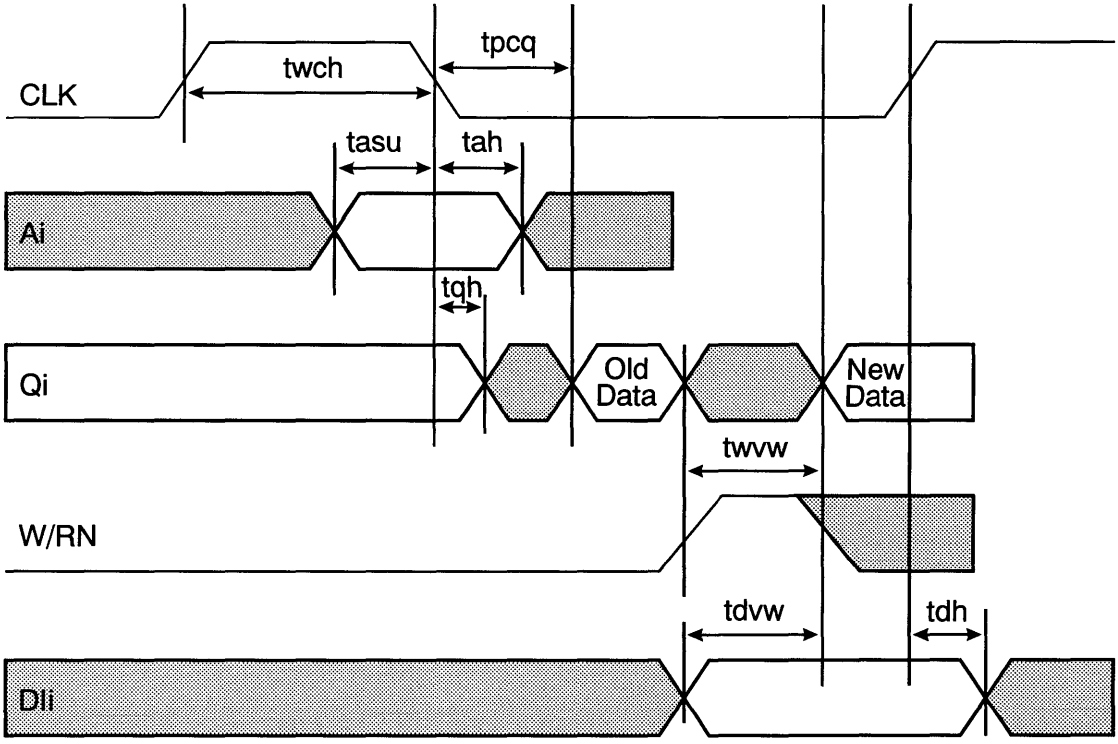
M X N RAM
Timing Diagram

Write Cycle 2 (See Notes 1 and 3)

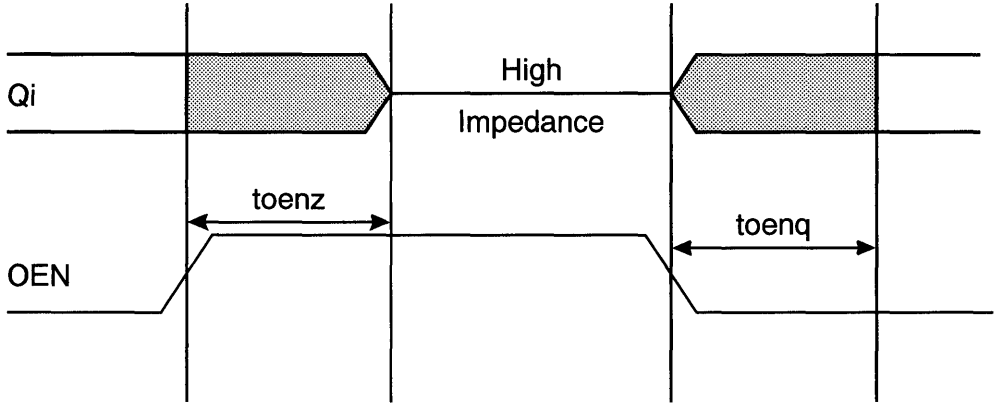


M X N RAM
Timing Diagram

Read-Modify-Write Cycle (See Note 4)



3-State Control Timing



Timing Diagram Notes

1. During a write cycle, the data that is written in becomes valid at the Q outputs as soon as the tcvw, tdvw, and twvw timing terms are met. The clock does not have to rise, and the W/RN signal does not have to fall first.
2. The data hold time in write cycle 1 is referenced to the rising edge of CLK when W/RN is held high.
3. The data hold time in write cycle 2 is referenced to the falling edge of W/RN and is equal to zero.
4. The data hold time in the Read-Modify-Write cycle has to be met only when W/RN is held high.

FIGURE 3: LOGIC SYMBOL

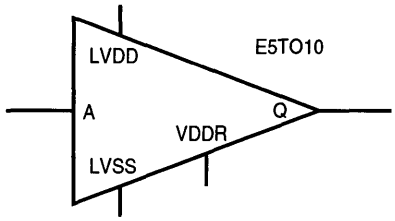


FIGURE 4: TRUTH TABLE

A	Q
LVDD(5V)	LVDD(5V)
VSSR(0V)	LVSS(-5V)

The E5TO10 5V to 10V level shifter is used to take an output differential of 5V from the RAM to a differential output voltage range of 10V. This was designed to allow a 5V RAM to operate in a 10V circuit.

In the logic symbol of Figure 3, LVDD, LVSS, and VSSR are pinned out and must be connected to the correct supplies. LVDD is the +5V positive supply, VSSR is the RAM negative supply (equal to VDD-5V), and LVSS is the -5V negative supply voltage.

The E5TO10 level shifter cell is designed to abut next to regular standard cells in a row. The LVDD, LVSS, and SUB supplies will connect by abutment while the VSSR supply is an input signal pin. For more information, refer to the AMI application note titled "Using the 5 Volt ABE RAM with 10 Volt Standard Cells."

The logic operations of the E5TO10 level shifter are shown in the truth table of Figure 4.

Operating Ranges

DESCRIPTION	NAME	VOLTAGE LEVEL
Digital And RAM Positive Supply	LVDD	+5V
Digital Negative Supply	LVSS	-5V
RAM Negative Supply	VSSR	OV
Quiet Substrate Bus	SUB	LVDD

Area Relative to 10V 2 input NAND: 4.33.
Input Capacitance: 0.194pF.
Bolt Syntax: Q .E5TO10 A LVDD LVSS VSSR;

AC Characteristics

CHARACTERISTIC	SYMBOL	tdx	Ktdx	t(0.5pF)
Maximum Input To Q Delay	tpdr	5.75 ns	3.94 ns/pF	7.72 ns
	tpdf	4.65 ns	4.29 ns/pF	6.80 ns

t(CL) = tdx + Ktdx *CL
Tj = 25°C
LVDD - LVSS = 10V
LVDD - VSSR = 5V
Typical Process

E10TO5
Level Shifter

ABX CMOS P-Well Process Family

FIGURE 5: LOGIC SYMBOL

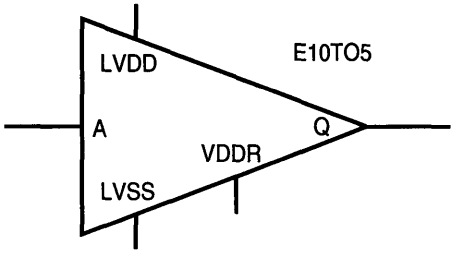


FIGURE 6: TRUTH TABLE

A	Q
LVDD(5V)	LVDD(5V)
LVSS(-5V)	VSSR(OV)

The E10TO5 10V to 5V level shifter is used to take a differential input voltage range of 10V and convert it to a 5V differential for RAM operation. This was designed to allow a 5V RAM to operate in a 10V circuit.

In the logic symbol of Figure 5, LVDD, LVSS, and VSSR are pinned out and must be connected to the correct supplies. LVDD is the +5V positive supply, VSSR is the RAM negative supply (equal to VDD-5V), and LVSS is the -5V negative supply voltage.

The E10TO5 level shifter cell is designed to abut next to regular standard cells in a row. The LVDD, LVSS, and SUB supplies will connect by abutment while the VSSR supply is an input signal pin. For more information, refer to the AMI application note titled "Using the 5 Volt ABE RAM with 10 Volt Standard Cells."

The logic operations of the E10TO5 level shifter are shown in the truth table of Figure 6.

Operating Ranges

DESCRIPTION	NAME	VOLTAGE LEVEL
Digital And RAM Positive Supply	LVDD	+5V
Digital Negative Supply	LVSS	-5V
RAM Negative Supply	VSSR	OV
Quiet Substrate Bus	SUB	LVDD

Area Relative to 10V 2 input NAND: 2.51.
Input Capacitance: 0.088pF.
Bolt Syntax: Q .E10TO5 A LVDD LVSS VSSR;

AC Characteristics

CHARACTERISTIC	SYMBOL	tdx	Ktdx	t(0.5pF)
Maximum Input To Q Delay	tpdr	1.38 ns	3.41 ns/pF	3.09 ns
	tpdf	1.67 ns	4.18 ns/pF	3.76 ns

t(CL) = tdx + Ktdx *CL
Tj = 25°C
LVDD - LVSS = 10V
LVDD - VSSR = 5V
Typical Process

Using the 5 Volt ABE RAM with 10 Volt Standard Cells

The RAS5Nwyz RAM is intended for use with 4.5 volt to 5.5 volt power supplies and pin voltages; however, it can be used with AMI's ABEHS 10 volt standard cell library as outlined in this application note. For further information, see the data sheets for the RAS5Nwyz RAM, the E5TO10 level shifter cell, and the E10TO5 level shifter cell.

The following description assumes the RAM is connected to a power supply with a 0 volt to +5 volt potential, while the standard cells (SC) are connected to a power supply with a -5 volt to +5 volt potential. The level shifters (LS) interface the RAM to the standard cells and are designed to abut to regular standard cells in a row of cells.

The power connections are as follows:

SUB = +5V Quiet substrate connection (RAM, SC, and LS)

LVDD = +5V = VDDR RAM, SC, and LS positive supply

VSSR = 0V RAM negative supply and LS reference voltage

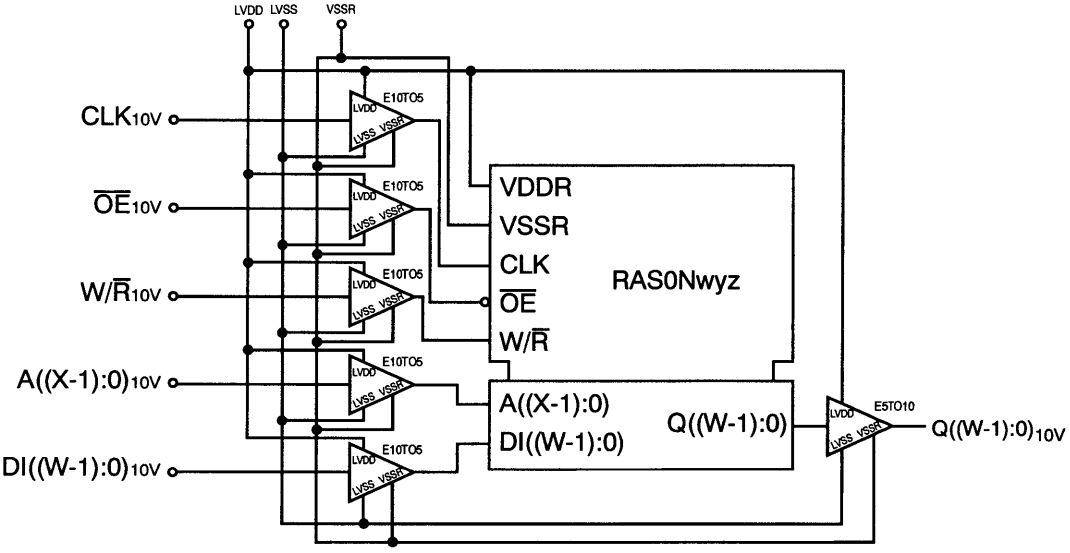
LVSS = -5V SC and LS negative supply

SUB is a global (external) connection to all the cells. VSSR is connected to the level shifters like an input signal: it is a pin on the layout and in the netlist. The rest of the power signals connect like power busses in the layout, but are pinned out like signals in the netlist and schematic symbol.

When the RAS5Nwyz RAM is used with 10 volt standard cells, every RAM input must have an E10TO5 level shifter cell connected to it, and every RAM output must have an E5TO10 level shifter cell connected to it. The power supplies must be connected as shown below in Figure 7.

The Cell Development Engineering Group will assemble the RAM and level shifters into a softcell netlist if requested to do so. The new softcell will be called RASHNwyz to distinguish it as having 10 volt inputs and outputs.

FIGURE 7: RASHNwyz SOFTCELL



RO4cwxyz, RO6cwxyz Synchronous ROM

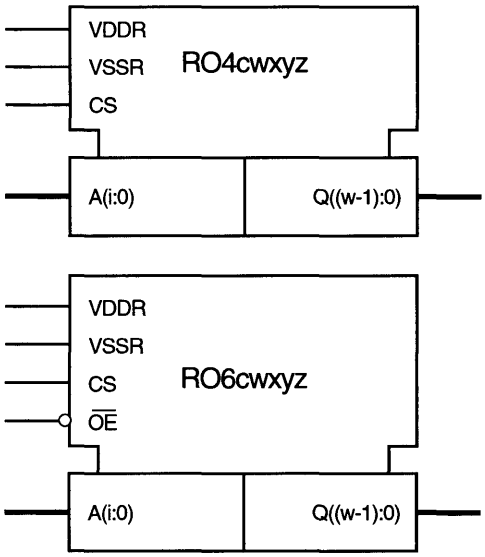
Preliminary

ABX CMOS P-Well Process Family

Features

- Low standby power when chip-select is stopped.
- Buffered or 3-state outputs. 3-state outputs are active low enable.
- Pre-charged design for lower power consumption.

FIGURE 1: LOGIC SYMBOL



General Description

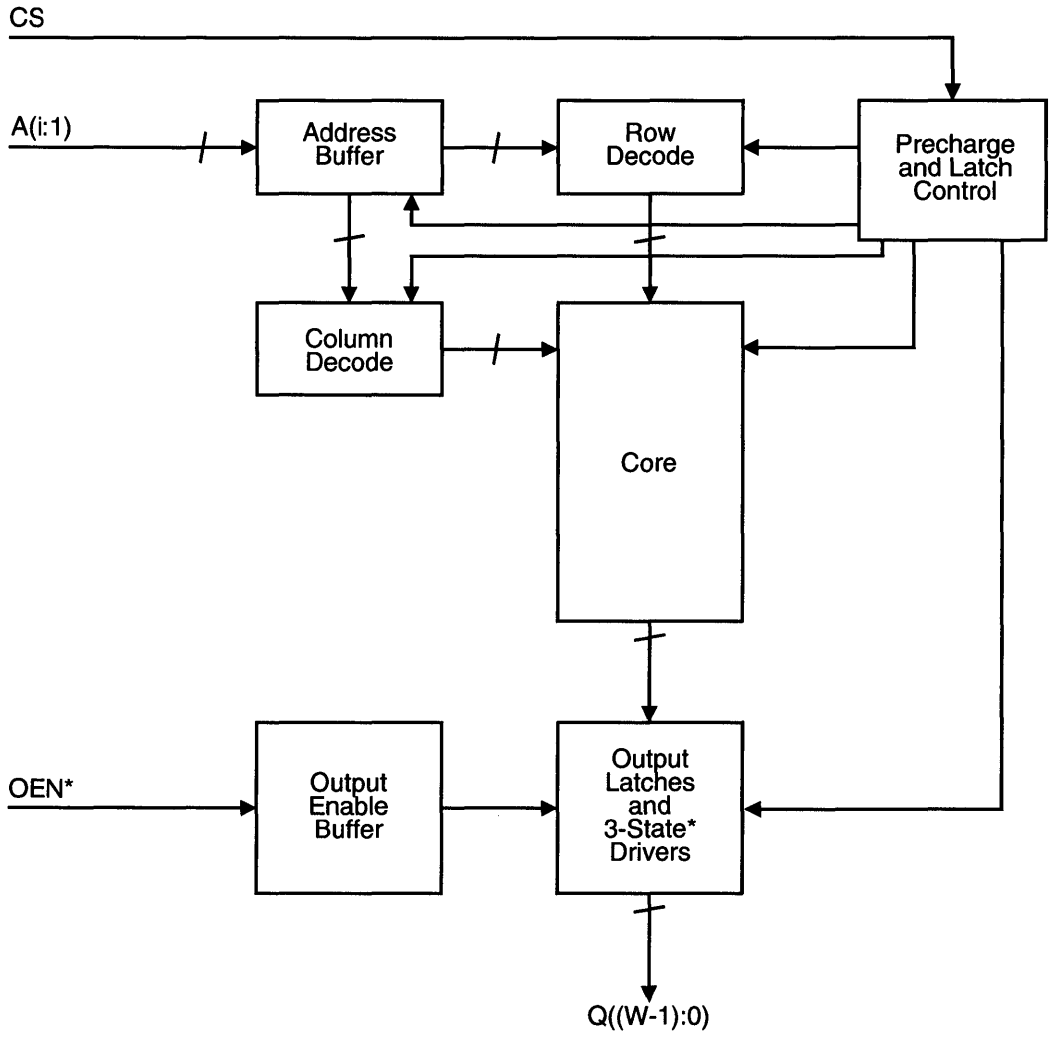
This series of double-metal MxN ROMs operates within a power supply voltage range of 4.5V to 5.5V. (It will operate at 2.5V with lower performance.) The RO4 series has always-active outputs. The RO6 series has 3-state outputs with active low Output Enable Not (OEN). The circuit is precharged when the chip-select (CS) line is low, and the read operation occurs when the chip-select (CS) is high. The outputs become valid a short time after the rising edge of the chip-select and are latched on the falling edge of the chip-select, keeping the outputs valid until the next rising edge of the chip-select. The address lines are latched on the rising edge of the chip-select.

Within limits specified below, the user has flexibility in specifying the logical size of the ROM, including both word-size and number of address locations. Within the name as shown above, the "cwxyz" represents a five character sequence assigned to each ROM configuration which uniquely identifies that particular configuration. The "c" represents the number column address lines, which is limited to 3, 4, or 5. The "w" represents the word-length in a mod-36 alpha-numeric digit using the integers 1-9 and the letters A-Z, excluding O, Q, and V. For example, "N" represents a word-length of 23 and "P" represents a word-length of 24. The "xyz" represents a hexadecimal value for the number of address locations divided by 16. For example, "00C" represents 192 address locations. The columns are represented because the ROM can be built using different aspect ratios, i.e., rows vs. columns.

The power supply connections are pinned out as VDDR and VSSR. A quiet bus of N+ guard ring surrounds the ROM and should be tied to VDDR for 5V only usage. For operation on 10V chips, see the AMI application note titled "RAS5Nwyz RAM Application Note - Using The 5 Volt ABE RAM with 10 Volt Standard Cells." This application note applies to ROMs as well as RAMs. Be sure to get the P-Well version of this application note.

Performance data is listed below for an example size. To obtain data and a workstation installation (symbol and simulation model) for a particular size, contact the factory.

FIGURE 2: ROM BLOCK DIAGRAM



*For RO4 series, OEN input is removed and output driver is never High – Z.

*For RO6 series, as shown.

Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Address Inputs	6	14	1
Word Size (Data Outputs)	1	32	1
Address Locations	64	16,384 (16K)	64
Total Bits In Core (Word Size Times Address Locations)	64	524,288 (512K)	

Pin Description and Input Capacitance

SIGNAL	TYPE	256 X 16	SIGNAL DESCRIPTIONS
Ai	Input	TBD	Address Inputs
CS	Input	TBD	Chip-Select
OEN	Input	TBD	3-State Output Control
Q(High–Z)	Output	TBD	Data Outputs

AC Characteristics for 256 X 16

CHARACTERISTIC	SYMBOL	tdx(ns)	ktdx(ns/pF)	t(0.5pF)(ns)
Max CS To Q Delay	tpcsq	TBD	TBD	TBD
Max OEN To Q Delay	tpoenq	TBD	TBD	TBD
Max OEN To High–Z Delay	tpoenz	TBD		
Min Address Setup Time	tasu	TBD		
Min Address Hold Time	tah	TBD		
Min CS Width Low	twcsl	TBD		
Min CS Width High	twcsh	TBD		
Min Q Hold Time	tqh	TBD		

ABX CMOS P-Well Process Family

Preliminary

Power Dissipation

PARAMETER	256 X 16
Typical C_{pd} (Equivalent Power Dissipation Capacitance (pF))	TBD
Typical Static IDD Tj = 85°C(μA)	TBD

Area Relative to a 2 Input Nand: 256 x 16 : TBD

Bolt Syntax:

Qw ... Q1 Q0 .R04cwxyz Ai ... A1 A0 CS VDDR VSSR;
Qw ... Q1 Q0 .R06cwxyz Ai ... A1 A0 CS VDDR VSSR;

A0 is the LSB

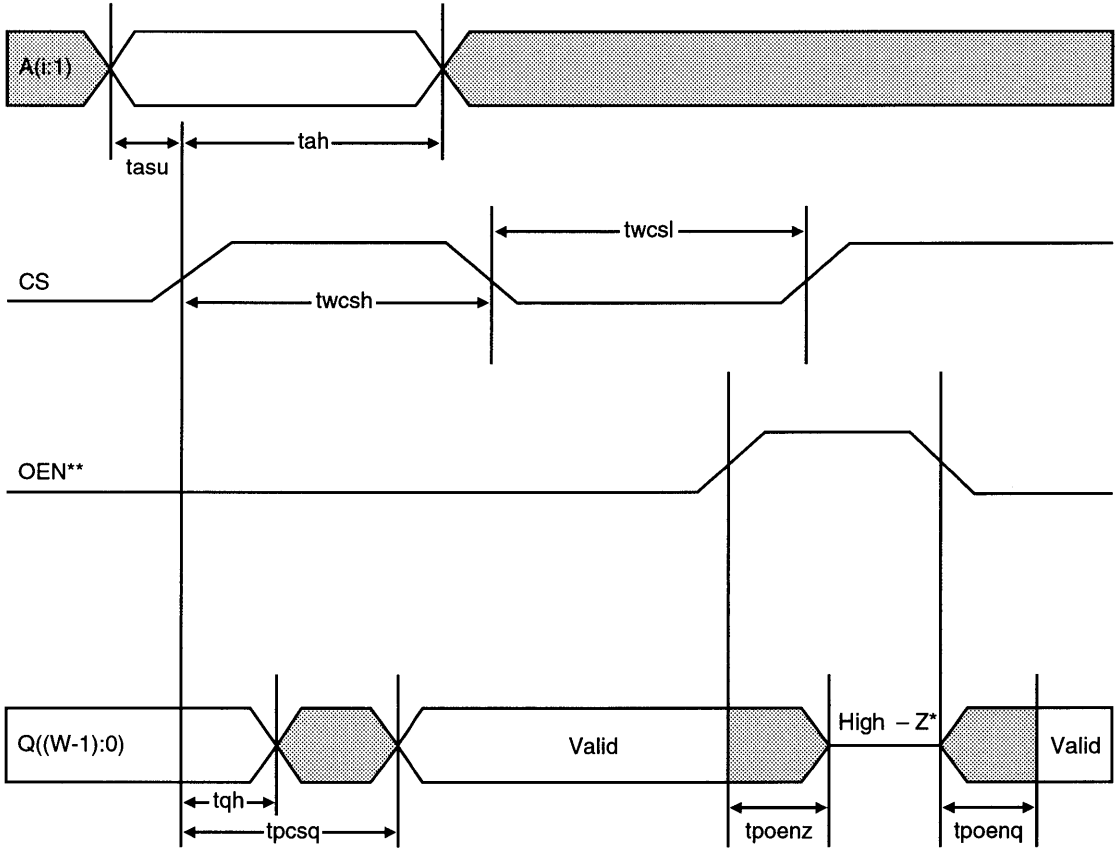
AC characteristics: t(CL) = tdx + Ktdx*CL

The data in the example above is specified at 5.0V, Tj=25°C, and typical process parameters. Performance at other operating points may be estimated by use of the Voltage, Process, and Temperature derating curves. Contact the factory to obtain the AC characteristics and input capacitance for different logical sizes of ROMs.

Testing Notes

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. For a more detailed description of the testing of memory elements in ICs, refer to the ROM testing application notes.

M X N ROM
Timing Diagram



*High – Z= High Impedance Q Output.

**For RO4 series, OEN is not applicable and the Q((W-1):0) is never High – Z.
For RO6 series, as shown.

SECTION 14
ELECTRICALLY ERASABLE CELLS

EEAwwXbb
EE Memory Array

ABX CMOS N-Well Process Family

General Description

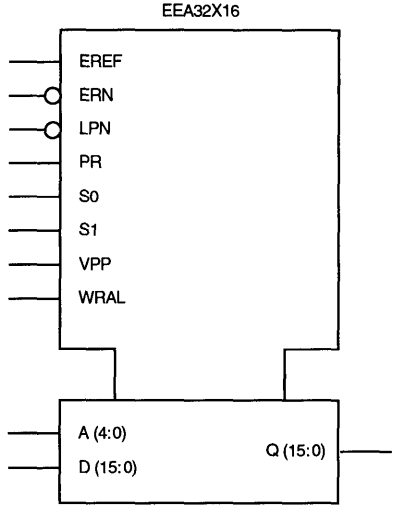
This series of ABX Electrically Erasable Programmable Memory Arrays operates within a power supply voltage range of 4.5V to 6.6V. The READ operation will function at lower voltages with decreased performance. The whole array must be erased at one time before writing. Then one word can be written each WRITE cycle, and one word can be read each READ cycle. The READ operation is similar to that of an asynchronous ROM.

Within the limits specified below, the user has flexibility in determining the logical size of the array, including both word size and number of address locations. Within the name as shown above, the "wwXbb" represents the logical size of the array. The "ww" specifies the number of words, and the "bb" specifies the bits per word.

During testing, all address locations can be written with the same data in one WRITE cycle by holding the WRAL pin high. The READ data retention margins can be tested by baking the programmed array or by using the S0, S1 and EREF pins. Contact the factory for more information.

This data sheet provides a general overview of AMI's available EE Arrays. Certain operating parameters can be altered through customization. Contact AMI for further details.

LOGIC SYMBOL FOR 32 X 16 ARRAY



Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Word Size	2	32	2
Address locations (words)	2	32	2

Pin Description

SIGNAL	TYPE	DESCRIPTION
Ai	Input	Address Inputs
Di	Input	Data Inputs
Qi	Output	Data Outputs
ERN	Input	Erase Not
LPN	Input	Low Power Not
PR	Input	Program Enable (erase or write)
VPP	Input	High Voltage Programming Signal
WRAL	Input	Write All for Testing
EREF	Input	External Reference for Testing
S0, S1	Input	Reference Control

EEAwwXbb
EE Memory Array

AMI SEMICONDUCTORS

ABX CMOS N-Well Process Family

Operating Ranges

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Supply Voltage	4.5	6.6	V
VPPV	Programming Voltage	15.0	16.5	V
TA	Operating Temperature	0.0	+70.0	°C

Power Dissipation

PARAMETER	MAXIMUM (μA) VDD = 5V
IDD for VDD Low Power Mode	5
IDD for VDD Read Mode*	40 + (40 per output)
IPP for VPP Program Mode	100

*40μA for voltage reference plus 40μA for each sense amplifier.

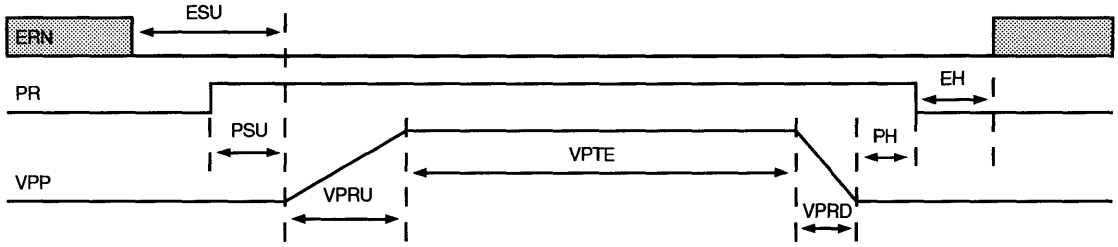
AC Characteristics**

CHARACTERISTIC	SYMBOL	MINIMUM	MAXIMUM	UNITS
ERN setup before VPP starts to rise	ESU	5.0		ns
PR setup before VPP starts to rise	PSU	5.0		ns
Address setup before VPP starts to rise	ASU	10.0		ns
Data setup before VPP starts to rise	DSU	3.0		ns
PR hold after VPP falls to VSS	PH	0.0		ns
ERN hold after PR falls	EH	0.0		ns
Address hold after PR falls	AH	0.0		ns
Data hold after PR falls	DH	2.0		ns
Ramp up rate of VPP	VPRU		0.02	V/μs
Ramp down rate of VPP	VPRD		15.0	V/μs
VPP high erase time	VPTE	100	200	ms
VPP high write time	VPTW	100	200	ms
VPP programming voltage	VPPV	15.0	16.5	V
Address change to valid output	TAQ		100	ns
LPN low to valid output	TLQ		100	μs
Load dependent delay of output	KTAQ		3.0	ns/pF
Output hold time after address change	TQH	0.0		ns
Output hold time after LPN falls	LFQ	0.0		ns

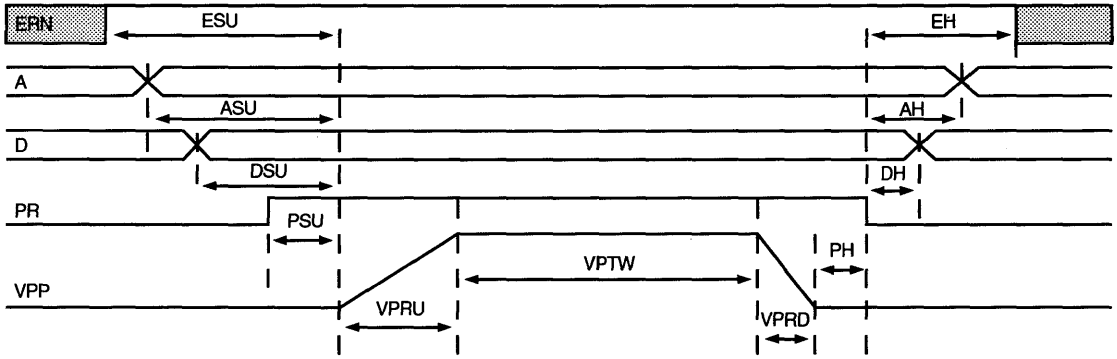
**Over given operating ranges
Bolt Syntax: Q0 Q1 Q2 ... .EEAwwXbb A0 A1 A2 ... D0 D1 D2 ... EREF ERN LPN PR S0 S1 VPP WRAL;

TIMING DIAGRAMS

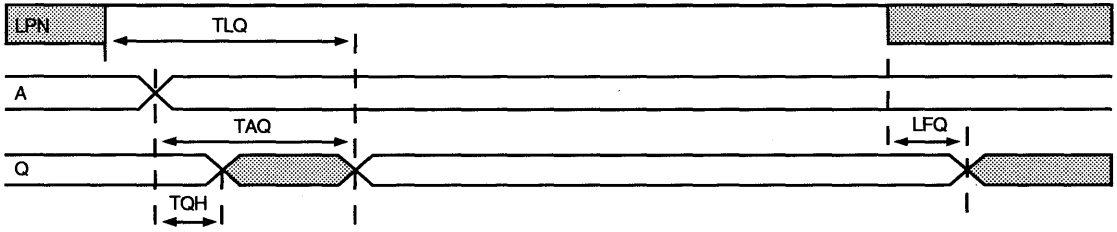
ERASE ARRAY A=DC D=DC LPN=DC Q=X



WRITE WORD LPN=DC Q=X



READ WORD PR=0 VPP=0 ERN=DC D=DC



Notes:
1. X = Don't know.
2. DC = Don't care.
3. S0, S1, EREF and WRAL : test pins that should be held at VSS for normal operation.
4. VPP and PR must be held : VSS unless erasing or writing.

EEVRL2
Voltage Ramp Rate Controller

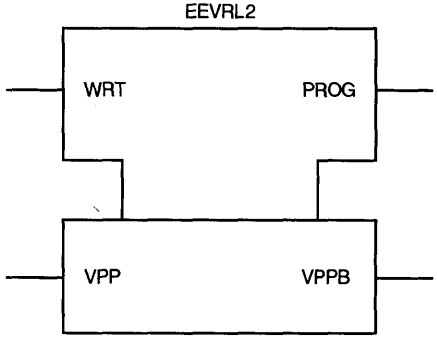
AMI SEMICONDUCTORS

ABX CMOS N-Well Process Family

General Description

This cell is a high voltage interface cell that provides the correct programming voltage ramp rates for the EEAwwXbb EE Memory Arrays. The PROG output should be connected to the PR input of the EE Array, and the VPPB output should be connected to the VPP input of EE Array.

LOGIC SYMBOL FOR EEVRL2 VOLTAGE RAMP RATE CONTROLLER



Pin Description

SIGNAL	TYPE	DESCRIPTION
WRT	Input	Ramp up/down control
VPP	Input	DC high voltage in
PROG	Output	Program enable for EE Array
VPPB	Output	Ramped high voltage programming signal

Operating Ranges

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Supply Voltage	4.5	6.6	V
VPP	High Voltage Input*		16.5	V
TA	Operating Temperature	0.0	+70.0	°C

*See the EEAwwXbb EE Memory Array data sheet for VPP specifications.

Power Dissipation

PARAMETER	MAX (μA) VDD=5V
VDD current while WRT = 1	800.0
VDD current while WRT = PROG = 0	5.0
VPP current while VPPB is ramping up*	1500.0
VPP current while WRT = 1, and VPPB = VPP	20.0
VPP current while WRT = 0, VPP = 16V	2.0

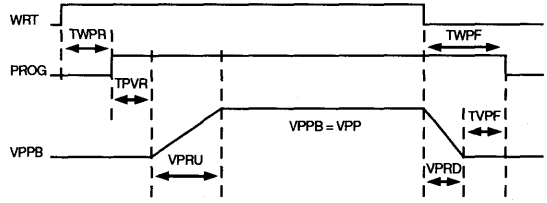
*The VPP supply only needs to be capable of supplying 100μa.

AC Characteristics

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
WRT rise to PROG rise	TWPR	0.0	10.0	ns
PROG rise to VPPB start to rise	TPVR	5.0		ns
WRT fall to PROG fall	TWPF	1.0	5.0	μs
VPPB down to PROG fall	TVPF	0.0		ns
VPPB ramp up rate	VPRU		0.02	V/μs
VPPB ramp down rate	VPRD		16.5	V/μs

Bolt Syntax: PROG VPPB .EEVRL2 WRT VPP;

TIMING DIAGRAM



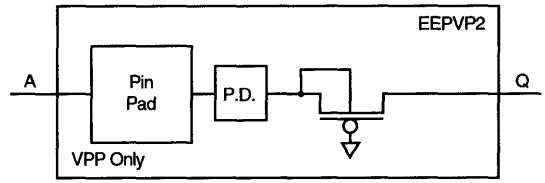
EEPVP2
EE Pad Cell

ABX CMOS N-Well Process Family

General Description

The EEPVP2 pad cell is a special analog pad cell for use with the EE Array only. It should be used to bring the VPP high voltage programming signal on chip. It has a special protection device which can withstand the high voltage of the VPP signal.

LOGIC SYMBOL

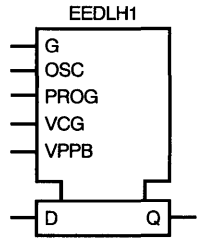


Bolt Syntax: Q .EEPVP2 A;

General Description

EEDLH1 is a 1-bit, nonvolatile (NV), electrically alterable storage cell with a transparent D-latch front end. Data may be stored in the D-latch front end until a nonvolatile write occurs. The Q output reflects the value of the nonvolatile storage cell. The power busses for this cell should be connected to VDD and EVSS, which must have a potential difference of 8 to 12 volts during programming and 2.5 to 12 volts for reading. For a complete description of the use of AMI EE cells, refer to the AMI Application Note on using EE cells in ASIC designs.

LOGIC SYMBOL FOR EEDLH1

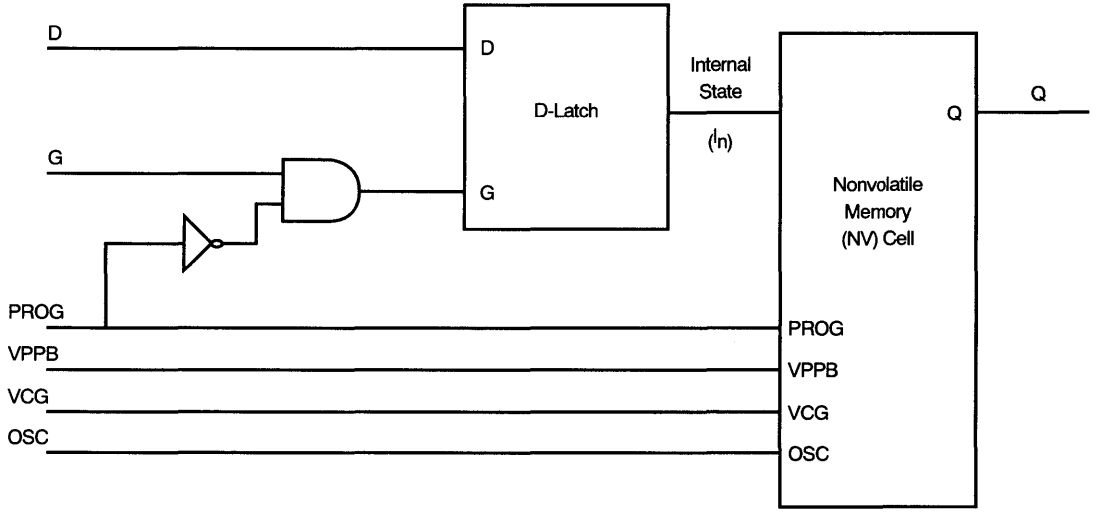


Truth Table for Digital Model

D	G	PROG	VPPB	VCG	Q	INTERNAL STATE (I_n)	DESCRIPTION
0	1	0	X	1	NC	0	Latch is transparent when G = 1 and PROG = 0
1	1	0	X	1	NC	1	Latch is transparent when G = 1 and PROG = 0
X	0	0	X	1	NC	NC	Latch internal state (I_n) when G=0
X	X	1	1	X	NC	NC	Program NV cell to internal state (I_n)*
X	X	↓	0	1	I_n		Q=I_n after PROG falls
X	X	0	X	0	X		Q=X when PROG=0 and VCG=0

*OSC must be oscillating during NV programming; the digital model does NOT check for OSC oscillating.
NC = No Change.

BLOCK DIAGRAM



EEDLH1
EE Latch

AMI SEMICONDUCTORS

ABX CMOS P-Well Process Family

Pin Description and Capacitance

NAME	CAP (pF)	TYPE	DESCRIPTION
D	0.07	Digital Input	Data input
G	0.07	Digital Input	Data latch control
PROG	0.07	Digital Input	Nonvolatile program control
VPPB	0.50	Analog Input	Programming voltage input
VCG	0.50	Analog Input	Control gate reference voltage
OSC	0.07	Digital Input	Oscillator for charge pumps
Q		Digital Output	Nonvolatile memory output

Area Relative to a 2 Input Nand: 36.4
Eq. Gates = 28
Bolt Syntax: Q .EEDLH1 D G OSC PROG VCG VPPB;

Electrical Characteristics

CHARACTERISTIC	MINIMUM	MAXIMUM
VPPB-EVSS during programming	15.0 - Vti	16.0 - Vti
Digital Inputs	-0.3 V	VDD + 0.3 V
EVSS	-6.0 V	-4.0 V
VSS	0V (Ground)	0V (Ground)
VDD	4.0 V	6.0 V
VCC substrate bus	VDD	VDD

See notes 2 and 3.

AC Characteristics: $t(C_L) = tdx + Ktdx * C_L$; $T_j = 25°C$; VDD - EVSS = 10.0V ; Typical Process

CHARACTERISTIC	SYMBOL	SILICON			MODEL	CHECKED
		MIN	MAX	UNITS		
Min D setup to G fall or PROG rise	t_{dsu}	5.3		nsec	5.3ns	Yes
Min D hold after G fall or PROG rise	t_{dh}	7.6		nsec	7.6ns	Yes
Min G low after PROG rises when D changes	t_{tglpr}	7.5		nsec	7.5ns	Yes
Min G high and PROG low (latch width)	t_{ghpl}	12.8		nsec	12.8ns	Yes
Max VCG rise to Q stable	t_{vcgq}		29.2	nsec	29.2ns	Yes
Max PROG fall to Q stable	t_{pq}		35.5	nsec	35.5ns	Yes
Load dependent delay for Q output	ktdx		5.60	nsec/pF	5.60 ns/pF	Yes
OSC oscillator frequency	oscf	1	10	MHz	NC = not checked	No
OSC high when PROG high	osch	50	500	nsec	NC	No
OSC low when PROG high	oscl	50	500	nsec	NC	No
Ramp up rate of VPPB	ruvpp		0.02	volt/μsec	NC	No
VPPB pulse width	vppw	100	150	msec	170ns	No
Ramp down rate of VPPB	rdvpp		16	volt/μsec	NC	No
PROG high before VPPB rise and after VPPB fall	t_{phvh}	0		nsec	NC	No

See note 1.

Timing Diagrams and Notes:

The OSC input must oscillate within the specified frequencies whenever PROG is high and VPPB is ramping up or held high. The simulation model does not check the OSC signal, so it must be verified by hand. The OSC signal can be held at VDD or VSS when not programming to reduce power consumption.

Data may be latched into the EEDLH1 cell using the G input before a nonvolatile program (write) cycle occurs. The timing diagram shown below in figure 1 assumes the G input is used to latch data and the VCG signal is valid. The VCG input must come from the EECGH1 cell.

If you do not wish to latch data with the G input before a nonvolatile program occurs, the G input can be tied to VDD and the data will be latched on the rising edge of PROG. The simplified timing diagram shown below in figure 2 assumes the G input is tied to VDD and that the VCG signal is valid.

Figure 1: Using G to Latch D

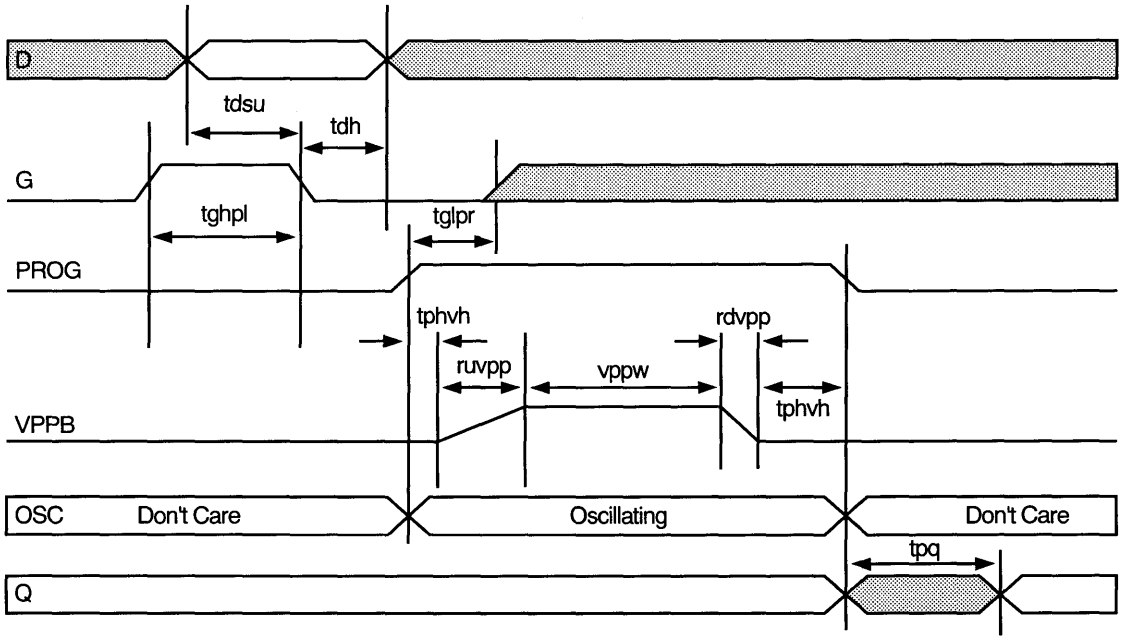


Figure 2: Using PROG to Latch D

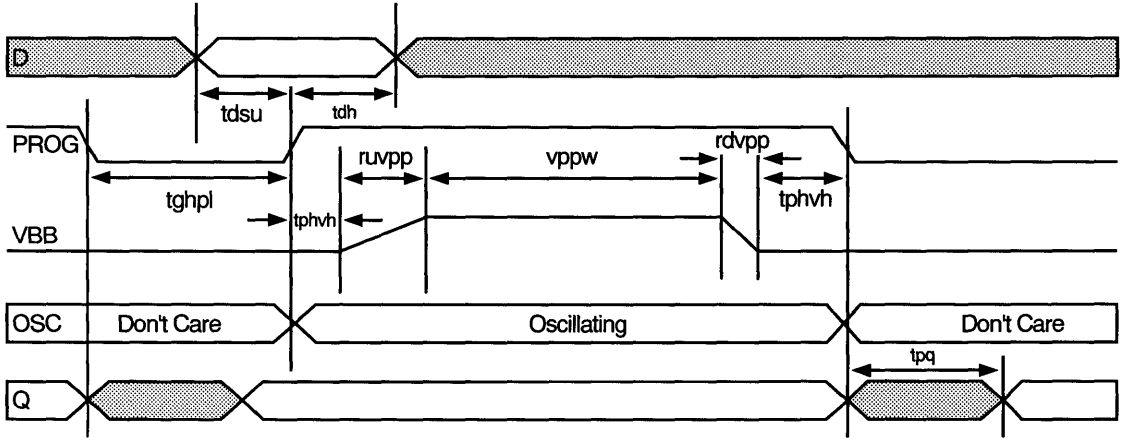
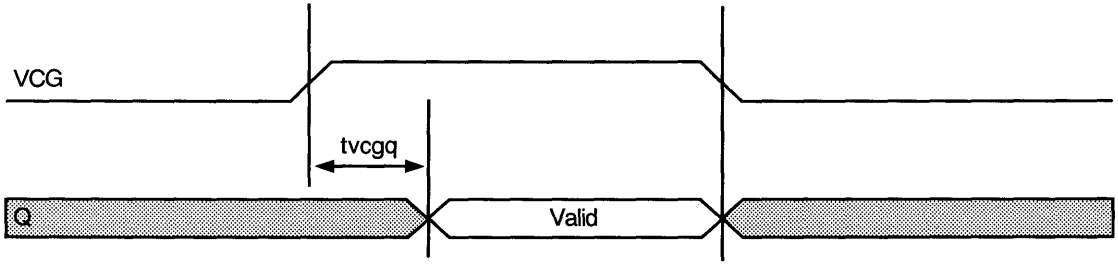


Figure 3: tvcgq Delay

The timing diagram shown below shows the relationship between VCG and Q.



Simulation and Testing Requirements:

The digital simulation model will check to see if your chip design will function properly with the EEDLH1 cell; however, there are several AC timing characteristics for the EEDLH1 cell that the model will not check. Special care must be taken to assure that the unchecked characteristics are met in the chip design. See the "Notes" section below for more information.

Using EE cells in ASIC designs creates special testing requirements that must be considered when designing the circuits and simulating for test vectors. The EE cells must be easily controlled and observed so they may be thoroughly tested. During testing, the nonvolatile memory cells should be run through several program cycles with alternating data to ensure their reliability. Contact an AMI representative for more information on reliability and testing.

Notes:

1. The simulation model is a digital model of an analog/digital cell. The AC characteristics reflect the anticipated analog and digital delays where possible. Some of the AC characteristics are not checked by the digital model and MUST be checked by hand verification. The AC characteristics which must be checked by hand have "NO" written in the column under the "Checked" heading. The vppw characteristic has an invalid value in the model for simulation and must have the valid value verified by hand. This cell is a softcell macro which is made from several hardcells; the interconnect capacitance delays are not included in the AC characteristics given above.

2. The digital inputs are designed to operate from 0 to 5 volts ± 10% so that they will interface with the 5 volt digital library. The analog signals and the power busses are designed to operate with VDD - EVSS = 8 to 12 volts. The EEDLH1 cell has 5 volt to 10 volt level shifters on the digital signals so it can interface with 5 volt digital cells. If you are using 10 volt digital logic, AMI can strip off the 5 volt to 10 volt level shifters so the digital inputs will operate at 10 volts.

3. Vti = threshold voltage of diode connected intrinsic transistor. The VPP programming voltage input to the chip is reduced one Vti by the EEPVP1 pad cell.

4. Data retention = 10 years at Ta = 0 to 70°C. Programming cycles = 10,000.

5. Half of the EEDLH1 cells on a chip should have their OSC signal driven by the opposite phase from the other half to reduce the ripple on the internal programming voltage.

6. The VPPB signal should be held at EVSS while powering up the chip to prevent an inadvertent program (write) from occurring.

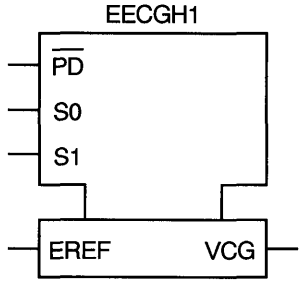
EECGH1
EE Reference Generator

ABX CMOS P-Well Process Family

Description

EECGH1 is an EE core cell used to generate the control gate reference voltage VCG for the EEDLH1 cell. There are two test modes: one test mode outputs the VCG signal on the EREF pin so it may be measured through the EEPCG1 pad cell; the other test mode disables the generation of VCG and gates an external test voltage applied to the EREF pin onto the VCG pin. The power busses for this cell should be connected to VDD and EVSS. For a complete description of the use of AMI EE cells, refer to the AMI Application Note on using EE cells in ASIC designs.

LOGIC SYMBOL FOR EECGH1



Truth Table for Digital Model

S1	S0	PDN	EREF	VCG
0	0	0	X	0
0	0	1	X	1
0	1	X	X	0
1	0	X	X	0
1	1	X	0	0
1	1	X	1	1

Truth Table for Actual Use

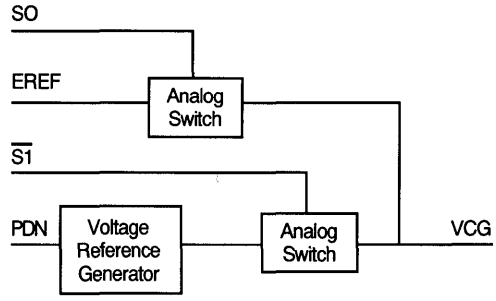
S1	S0	PDN	EREF	MODE
0	0	0	IN	Low power (disabled)
0	0	1	IN	Normal operation: VCG - EVSS = 1 to 2 volts
0	1	1	OUT	Read VCG through EREF
1	0	X	IN	Invalid
1	1	X	IN	Supply external reference voltage through EREF

Pin Description and Capacitance

NAME	CAP (pF)	TYPE	DESCRIPTION
S1	0.07	Digital Input	Test mode select
S0	0.07	Digital Input	Test mode select
PDN	0.07	Digital Input	Powerdown mode select
EREF	Note 1	Analog I/O	Read VCG and supply external reference for testing
VCG		Analog Output	Voltage reference for EEDLH1 cell

See note 1.
Area Relative to a 2 Input Nand: 16.7
Eq. Gates = 10.25
Bolt Syntax: VCG .EECGH1 EREF PDN S0 S1;

Block Diagram



AC Characteristics: $t(C_L) = tdx + Ktdx * C_L$; $T_j = 25°C$; VDD - EVSS = 10.0V ; Typical Process

CHARACTERISTIC	SYMBOL	tdx (ns)	Ktdx (ns/pF)	t(0.5pF) (ns)
Max S1 to VCG Delay	t_{s1vr} t_{s1vf}	22.1 14.1	14.6 5.0	29.4 16.6
Max S0 to VCG Delay	t_{s0vr} t_{s0vf}	22.1 14.1	14.6 5.0	29.4 16.6
Max PDN to VCG Delay	t_{pdvr} t_{pdvf}	22.1 11.2	14.6 5.0	29.4 13.7
Max EREF to VCG Delay	t_{ervr} t_{ervf}	13.5 5.0	14.6 5.0	20.3 7.5

See note 2.

Electrical Characteristics

CHARACTERISTIC	MINIMUM	MAXIMUM
EREF Input Voltage	EVSS - 0.3V	VDD + 0.3V
S1, S0, PDN Voltages	-0.3V	VDD + 0.3V
EVSS	-6.0V	-4.0V
VSS	0V (Ground)	0V (Ground)
VDD	4.0V	6.0V
VCC substrate bus	VDD	VDD

See note 3.

Notes:

1. Since the EREF and VCG pins are connected through an analog switch, any capacitance added to one of these pins will add to the capacitance on the other pin while in the test modes; the simulation model will not reflect this fact.

2. The simulation model is a digital model of an analog/ digital cell. The AC characteristics given reflect the anticipated analog and digital delays. This cell is a softcell macro which is made from several hardcells; the interconnect capacitance delays are not included in the AC characteristics given above.

3. The digital inputs are designed to operate from 0 to 5 volts ±10% so that they will interface with the 5 volt digital library. The analog signals and the power busses are designed to operate with VDD - EVSS = 8 to 12 volts. The 5 volt to 10 volt level shifters can be removed from the digital inputs for use with a 10 volt digital library.

4. The EREF pin should be held at a known DC voltage when not in use.

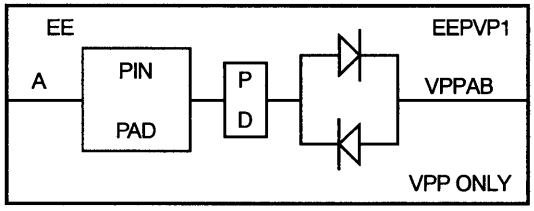
EEPVP1
EE Pad Cell

ABX CMOS P-Well Process Family

Description

EEPVP1 is a special EE pad cell used to input the high voltage programming signal VPP. The power busses for this cell should be connected to VDD and EVSS. For a complete description of the use of AMI EE cells, refer to the AMI Application Note on using EE cells in ASIC designs.

LOGIC SYMBOL FOR EEPVP1



TRUTH TABLE		CAPACITANCE	
A	VPPAB		Ci(pF)
0	0	A	5.50
1	1		

See note 1.
Area Relative to a 2 Input Nand: 37.4
Eq. Gates = 1.0
Bolt Syntax: VPPAB .EEPVP1 A;

AC Characteristics: $t(C_L) = tdx + Ktdx * C_L$; $T_j = 25°C$; VDD - EVSS = 10.0V ; Typical Process

CHARACTERISTIC	SYMBOL	tdx (ns)	Ktdx (ns/pF)	t(0.5pF) (ns)
Max A to VPPAB delay	t_{pdr} t_{pdf}	25.0 25.0	0.0 0.0	25.0 25.0

See note 2.

Electrical Characteristics

CHARACTERISTIC	MINIMUM	MAXIMUM
Input Voltage(VPP)	EVSS - 3.0V	16V
VPPAB Output voltage = VPP - Vti		

See note 3.

Notes:

1. Any capacitance connected to the VPPAB pin will add to the pad capacitance on node A in actual use; the simulation model will not reflect this fact.

2. The simulation model is a digital model of an analog cell. The AC characteristics given are the delays used in the digital model and do not have significant meaning in actual use.

3. Vti = threshold voltage of diode connected intrinsic device.

4. Power bus connections are VCC and EVSS. See EEDLH1 cell for details.

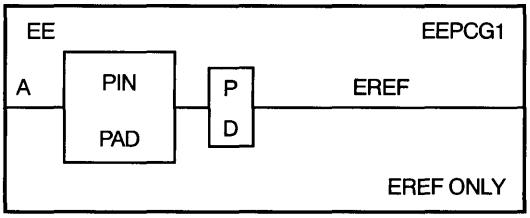
EEPCG1
EE Pad Cell

ABX CMOS P-Well Process Family

Description

EEPCG1 is a special EE analog pad cell used to read the internally generated VCG reference voltage and supply an externally generated VCG signal for testing. The cell consists of a protection device with a 200 ohm series resistor. The power busses for this cell should be connected to VDD and EVSS. For a complete description of the use of AMI EE cells, refer to the AMI Application Note on using EE cells in ASIC designs.

LOGIC SYMBOL FOR EEPCG1



TRUTH TABLE		CAPACITANCE	
A	EREF		Ci(pF)
0	0	A	5.50
1	1		

See note 1.
Area Relative to a 2 Input Nand: 36.4
Eq. Gates = N/A
Bolt Syntax: EREF .EEPCG1 A;

AC Characteristics: $t(C_L) = tdx + Ktdx * C_L$; $T_j = 25°C$; VDD - EVSS = 10.0V ; Typical Process

CHARACTERISTIC	SYMBOL	tdx (ns)	Ktdx (ns/pF)	t(0.5pF) (ns)
Max A to EREF delay	t_{pdr}	10.0	0.0	10.0
	t_{pdf}	10.0	0.0	10.0

See note 2.

Electrical Characteristics

CHARACTERISTIC	MINIMUM	MAXIMUM
Input Voltage	EVSS - 0.3V	VDD + 0.3V

Notes:

1. Any capacitance connected to the EREF pin will add to the pad capacitance on node A in actual use; the simulation model will not reflect this fact.

2. The simulation model is a digital model of an analog cell. The AC characteristics given are the delays used in the digital model and do not have significant meaning in actual use.

3. Power bus connections are VCC and EVSS. See EEDLH1 cell for details.

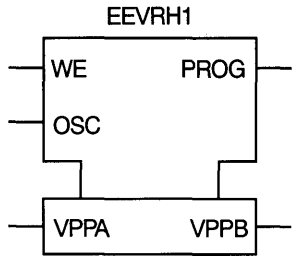
EEVRH1
EE Voltage Ramp Controller

ABX CMOS P-Well Process Family

Description

EEVRH1 is an EE core cell used to waveshape a high voltage input to the correct shape for programming the EEDLH1 memory cell. This cell uses the DC high voltage from the EEPVP1 pad cell as an input. While waveshaping is in progress, the PROG output remains high. The PROG output from this cell can be used directly for the PROG input to the EEDLH1 cell. The power busses for this cell should be connected to VDD and EVSS. For a complete description of the use of AMI EE cells, refer to the AMI application note on using EE cells in ASIC designs.

LOGIC SYMBOL FOR EEVRH1



Truth Table for Digital Model

WE	VPPA	OSC	VPPB	PROG
0	X	(1 OR 0)	0	0
1	0	(1 OR 0)	0	1
1	1	(1 OR 0)	1	1

Truth Table for Actual Use

WE	VPPA	OSC	MODE
1	HIGH - V	Oscillating	VPPB = Ramp up and hold high voltage; PROG = 1
0	X	(0 OR 1)	VPPB = Ramp down to near EVSS; PROG = 0 After VPPB ramps down

Pin Description and Capacitance

NAME	CAP (pF)	TYPE	DESCRIPTION
WE	0.07	Digital Input	Enable ramp up and hold
OSC	0.07	Digital Input	Oscillator for charge pump
VPPA		Analog Input	DC high voltage input
VPPB		Analog Output	Shaped high voltage output
PROG		Digital Output	Waveshaping in progress

Area Relative to a 2 Input Nand: 50.3
Eq. Gates = 30.25
Bolt Syntax: PROG VPPB .EEVRH1 OSC VPPA WE;

AC Characteristics: $t(C_L) = tdx + Ktdx * C_L$; $T_j = 25°C$; VDD - EVSS = 10.0V ; Typical Process

CHARACTERISTIC	SYMBOL	SILICON			MODEL
		MIN	MAX	UNITS	
Max OSC valid (0 or 1) to VPPB Delay	t_{ovpr} t_{ovpf}				14.9 21.9
Max VPPA to VPPB Delay	t_{vvpr} t_{vvpf}				11.9 16.0
Max WE to VPPB Delay	t_{wvpr} t_{wvpf}				11.9 16.0
Max WE to PROG Delay	t_{wpr} t_{wpf}				9.2 9.0
OSC Oscillator Frequency	oscf	1	10	MHz	NC = not checked
OSC High when WE High	osch	50	500	nsec	NC
OSC Low when WE High	oscl	50	500	nsec	NC
Ramp up Rate of VPPB	ruvpp		0.02	V/µsec	NC
Ramp Down Rate of VPPB	rdvpp		15	V/µsec	NC
PROG high before VPPB Rise and After VPPB Fall	t_{phvh}	0		nsec	NC

See note 1.

Electrical Characteristics

Characteristic	Minimum	Maximum
Digital Inputs	-0.3V	VDD + 0.3V
VPPA - EVSS	15V - Vti	16V - Vti
VPPB - EVSS (High)	15V - Vti	16V - Vti
EVSS	-6.0V	-4.0V
VSS	0V (Ground)	0V (Ground)
VDD	4.0V	6.0V
VCC substrate bus	VDD	VDD

See notes 2 and 3.

Notes:

1. The simulation model is a digital model of an analog/digital cell. The AC characteristics shown under the model column are the delays used in the digital model and do not have significant meaning in actual use. This cell will create the correct waveshape to program the EEDLH1 cell if you supply the VPPA and OSC signals as specified above, then hold the WE pin high for 100 to 150msec. The model will not check for the correct AC characteristics on the pins, so you will have to check them by hand. The end of the programming cycle should be determined by testing the PROG output for a low signal as opposed to waiting a specified time after WE falls. This cell is a soft macro which is made from several hardcells; the interconnect capacitance delays are not included in the AC characteristics given above.

2. The digital inputs are designed to operate from 0 to 5 volts ± 10% so that they will interface with the 5 volt digital library. The analog signals and the power busses are designed to operate with VDD - EVSS = 8 to 12 volts. The 5 volt to 10 volt level shifters can be removed from the digital inputs for use with a 10 volt digital library.

3. Vti is the threshold voltage of an intrinsic transistor and is a function of the process. The Vti voltage drop will be controlled by the EEPVP1 cell.

EEDLH1
Application Note

AMI SEMICONDUCTORS

ABX CMOS P-Well Process Family

Using EE Cells in ASIC Designs

Using Electrically Erasable (EE) (or more appropriately Electrically Alterable) nonvolatile memory cells in ASIC designs creates unique design and test considerations. The purpose of this application note is to describe how to properly use the AMI EEDLH1 cell along with the support cells needed.

The EEDLH1 cell is a 1-bit, nonvolatile, electrically alterable memory cell designed to allow a few bits of nonvolatile storage to be added to a cell-based ASIC design. At least three additional support cells are needed to generate and control some special analog signals used by the EEDLH1 cell. Refer to the data sheets for more detailed descriptions of the individual cells, the latest AC characteristic specifications, and block diagrams of the individual cells.

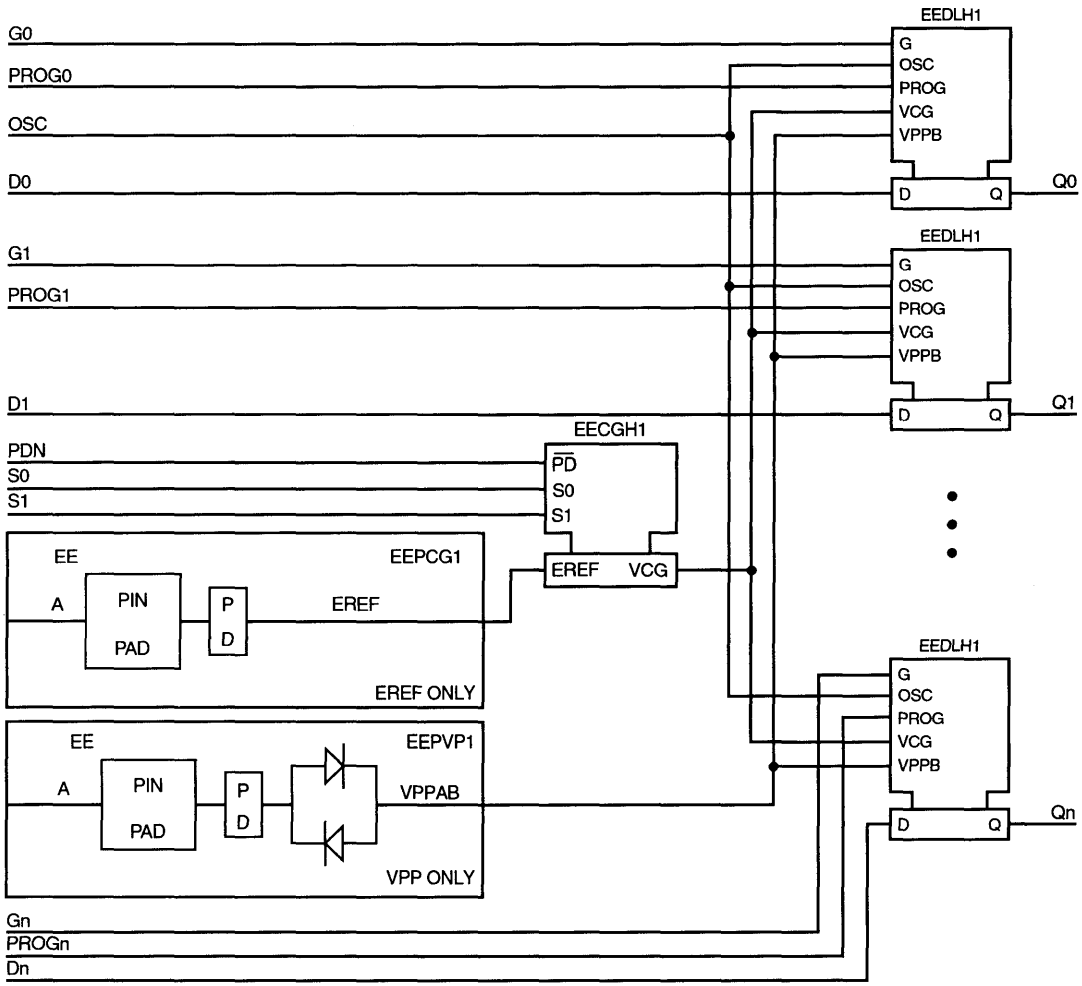
Referring to figure 1 below, the EEDLH1 cell has six inputs and one output. The D input is the data input to the cell. The G input can be used to latch D before a nonvolatile program (write) occurs, or the G input can be tied to VDD and D will be latched on the rising edge of PROG. The PROG input initiates the nonvolatile program cycle. OSC must be oscillating during the program cycle to operate the charge pumps. VPPB is a high voltage programming signal input; the VPPB voltage must input to the chip through the EEPVP1 pad cell. The VCG input supplies a reference voltage (VCG) to the gate of the programmable device while reading; the VCG voltage is generated by the EECGH1 cell. The Q output from EEDLH1 reads the state of the nonvolatile memory bit.

The EEPVP1 pad cell reduces the VPPB voltage by one intrinsic threshold drop (Vti) before it is routed to other cells. The EEDLH1 memory cell then pumps VPPB up by one Vti internal to the cell during programming.

The EECGH1 cell is used to generate the VCG reference voltage for the EEDLH1 cell. During normal operation, the VCG output supplies the correct reference voltage. There are also two test modes that can be used to check the reference voltage and supply an external voltage to VCG for testing. The external reference voltage must be input to the chip through the EEPCG1 cell. The EECGH1 cell uses some DC power. To save power, the PDN pin can be held at 0 volts to disable the cell. See the EECGH1 data sheet for details.

The power busses to the cells mentioned above must be connected to ±5 volt supplies. The digital inputs are driven by 0 to 5 volt signals so that they will interface with the 5 volt digital library. The 5 volt to 10 volt level shifters can be taken off the inputs for use with 10 volt digital cells. The figure shown below gives an example of how to connect the EE cells for typical operation.

While designing ASICs that use EE cells, test requirements should be kept in mind so that the final product can be tested properly. The inputs to the cells should be easily controlled by the test vectors, and the outputs should be easily observed by the test program. During testing, the nonvolatile memory should be cycled through about 10 program/read cycles with alternating data to increase the reliability of the tested parts.



The procedure to implement a nonvolatile program cycle is outlined below. See the data sheets for exact timing and voltage requirements as well as timing diagrams.

Step 1: G=1, PROG=0, VPPB=EVSS, D=(NEW DATA), Q=(OLD DATA).

Step 2: G=0 to latch data if desired.

Step 3: PROG=1 to initiate program cycle (and latch data if G=1).

Step 4: OSC starts oscillating if not already.

Step 5: VPPB driven to specified waveshape (ramp up, hold, ramp down).

Step 6: Oscillator can stop.

Step 7: PROG=0.

Step 8: Q=(NEW DATA).

SECTION 15
SALES INFORMATION

AMI SEMICONDUCTORS

Terms of Sale

1. ACCEPTANCE:

THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. PAYMENT:

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. TAXES:

Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or charges of any nature, imposed by any public authority (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. F.O.B. POINT:

All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, United Parcel Service (UPS), Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. DELIVERY:

Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any reprocurement costs, nor for delay or nondelivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay. In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. PATENTS:

The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements. Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent,

and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. INSPECTION:

Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at the place of manufacture, such inspection shall be so conducted as to not interfere unreasonably with Seller's operations, and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY:

The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller. It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. PRODUCTS NOT WARRANTED BY SELLER:

The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES EXPRESSED, STATUTORY OR IMPLIED INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INFRINGEMENT AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products contact Seller.

10. PRICE ADJUSTMENTS:

Seller's unit prices are based on certain material costs. These materials include, among other things, gold packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in the cost of other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. VARIATION IN QUANTITY:

If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. CONSEQUENTIAL DAMAGES:

In no event shall Seller be liable for special, incidental or consequential damages.

13. GENERAL:

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Section 202 of Executive Order 11246, as amended and where applicable, and other affirmative action requirements made applicable to this order by federal statute, rule or regulation.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities domestic or foreign.

(g) Unless otherwise agreed in a writing signed by both Buyer and Seller, Seller shall retain title to and possession of all tooling of any kind (including but not limited to masks and pattern generator tapes) used in the production of products furnished hereunder.

(h) Buyer, by accepting these products, certifies that he will not export or re-export the products furnished hereunder unless he complies fully with all laws and regulations of the United States relating to such export or re-export, including but not limited to the Export Administration Act of 1979 and the Export Administration Regulations of the U.S. Department of Commerce.

(i) Seller shall own all copyrights in or relating to each product developed by Seller whether or not such product is developed under contract with a third party.

(j) The design, development or manufacture by Seller of product for a specific customer shall not be deemed to produce a work made for hire and shall not give to the customer any copyright interest in the product or any interest in all or any portion of the mask works relating to the product. In addition, all such rights shall remain the property of the Seller. Seller shall retain all rights in mask work on any circuit designed using Seller's standard cell library and Seller shall retain all rights in mask work to the non-personalized portion of any gate array developed for Buyer.

(k) Engineering work performed by the Seller of any kind, including but not limited to, development of test programs, shall only be on a best efforts basis.

14. GOVERNMENT CONTRACT PROVISIONS:

If Buyer's original purchase order indicates by contract number that it is placed under a government contract, only the following provisions of the current Federal Acquisition Regulations are applicable, in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be – i.e., "Contracting Officer" shall mean "Buyer," "Contractor" shall mean "Seller," and the term "Contract" shall mean this order: 52.202-1 Definitions; 52.232-11 Extras; 52.212-9 Variation in Quantity; 52.232-23 Assignment of Claims; 52.228-2 Additional Bond Security; 52.224-11 Certain Communist Areas; 52.222-4 Contract Work Hours and Safety Standards Act-Overtime Compensation; 52.222-20 Walsh-Healey Public Contracts Act, if this order exceeds $10,000; 52.222-26 Equal Opportunity; 52.203-1 Officials Not to Benefit; 52.203-5 Covenant Against Contingent Fees; 52.249-1 Termination for Convenience of the Government if this order does not exceed $500,000 (only to the extent that Buyer's contract is terminated for the convenience of the government); 52.246-1 Contractor Inspection Requirements; 52.247-1 Commercial Bills of Lading; 52.222-35 Affirmative Action Viet Nam Veterans if this order exceeds $10,000; 52.222-36 Affirmative Action Handicapped Workers, if this order exceeds $2,500; 52.222-1 Notice to the Government of Labor Disputes; 52.215-1 Examination of Records by Comptroller General; 52.220-3 Utilization of Labor Surplus Area Subcontracting Concerns.

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Current as of January 1993

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